MOS VLSI PROJECT

5 BIT CARRY LOOK AHEAD ADDER

BY

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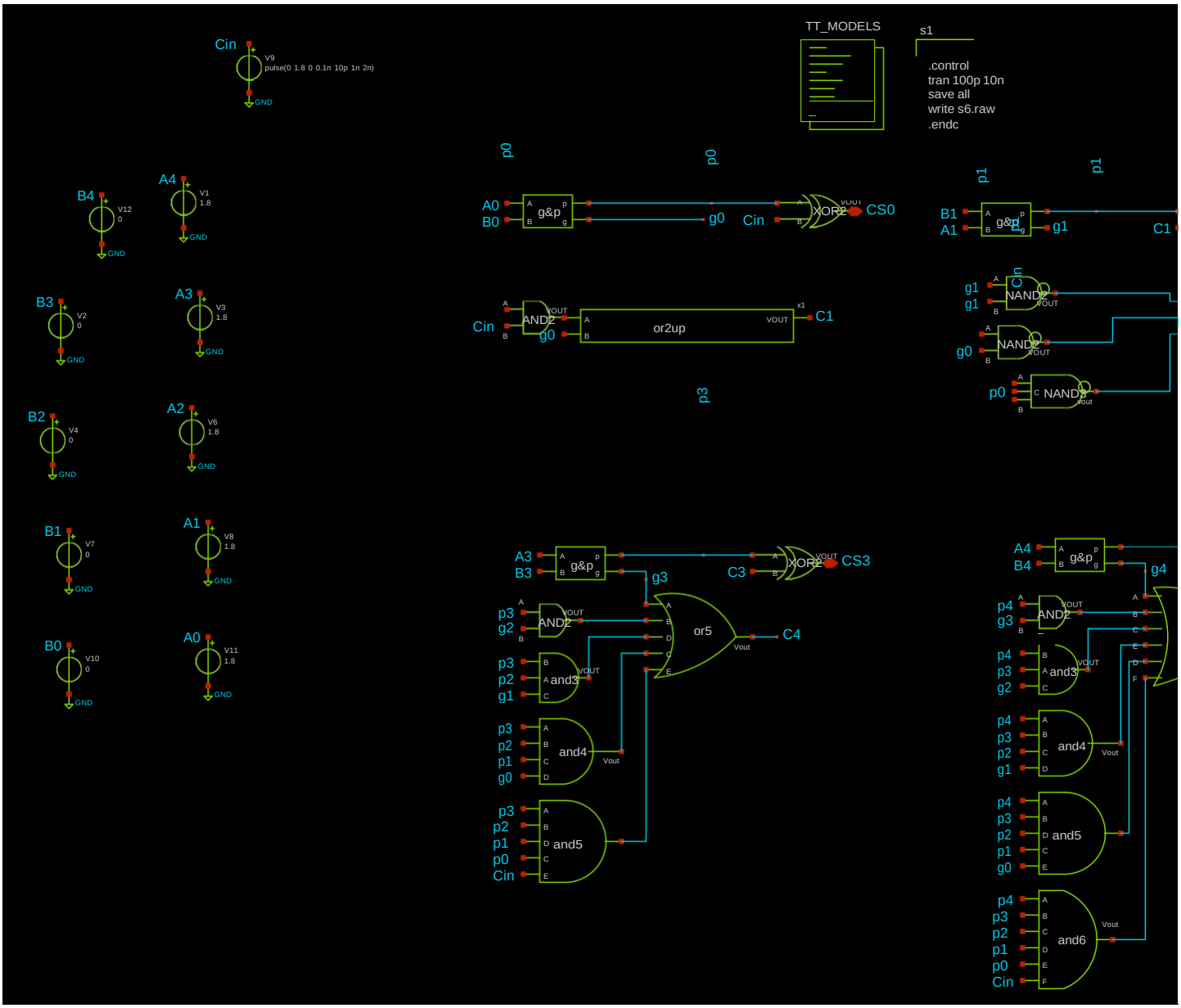
SCHEMATIC AND LOGIC WORKING DIAGRAMS:

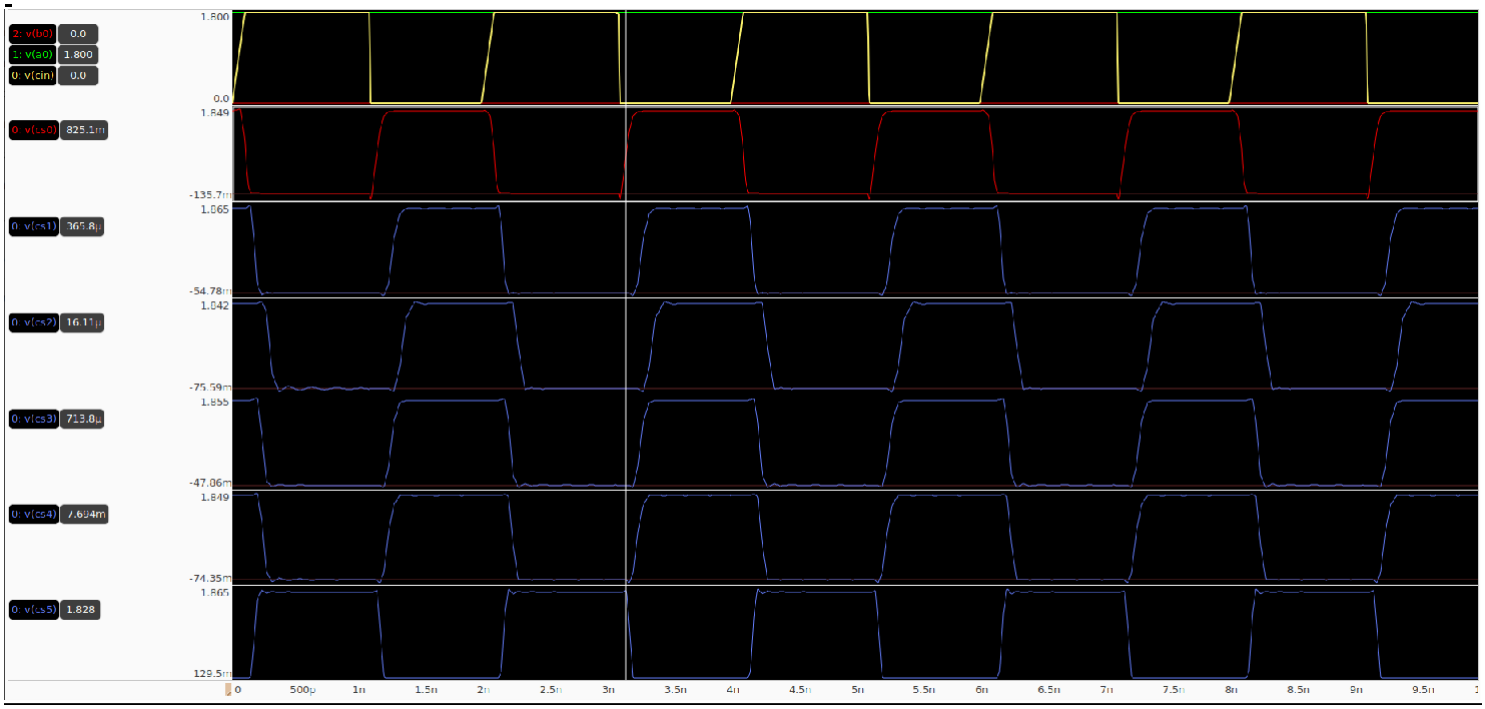


**** All schematics are at the end of the PDF INCLUDING THE MAIN SCHEMATIC****

SPECIFICATION TABLE:

Technology	Skywater 130nm tech
Vdd	1.8 V
Power	
AREA	
Clock Speed(Pulse)	4 GHz

LOGIC WORKING DIAGRAMS:



WHAT DID WE TRY:

We have implemented 5 bit adder using ripple adder architecture which resulted in large delays.so we have tried carrylook ahead adder which resulted in lesser delay than ripple adder architecture . we have designed all basic gates like AND(2-6 input),nor(2-6),OR(2-6),XOR 2 as shown in the above schematic diagram. We used PSEUDO NOR'S to minimizefurther more delay.

LIMITATIONS:

Width of any gate can't be less twice of the technology width parameter, whenever we tried we got errors and also widthtradeoff should be take care as more width also creates delay increase. We got more delay using NAND gates so we avoided AND gates directly from static CMOS logic gate.

THEORY ON CARRY LOOK AHEAD ADDER:

A carry-Look ahead adder is a fast parallel adder as it reduces the propagation delay by more complex hardware, henceit is costlier. In this design, the carry logic over fixed groups of bits of the adder is reduced to two-level logic, which is nothing but a transformation of the ripple carry design.

This method makes use of logic gates so as to look at the lower order bits of the augend and addendto see whether ahigher order carry is to be generated or not

The operation of carry look ahead is based on two scenarios:

Calculate every digit position to know whether that position is propagating a carry bit that comesfrom its right position.

Then combine the calculated values to produce the output for every set of digits where the groupgenerates a propagation bit that comes from the right position.

Carry look ahead adders operate by generating two bits called Carry Propagate and Carry Generate which are represented by Cp and Cg. The Cp bit gets propagated to the next stage and the Cg bit is used for generating the output carry bit and this is independent of the input carry bit.

CRITICAL PATH:

Total delay of CLA=(delay of the generate/propagate gates)+(total delay of the k−bit bloc ks) + (No. of carry look ahead adder blocks ×total delay of the carry look ahead blocks fro m Cin to Cout) + (No. of ripple carry adder blocks ×delay of a ripple carry adder)Total dela y of CLA=(delay of the generate/propagate gates)+(total delay of the k−bit blocks) + (No. of carry look ahead adder blocks ×total delay of the carry look ahead blocks from Cin to C out) + (No. of ripple carry adder blocks ×delay of a ripple carry adder)

Substituting the terms we get,01-10-2022

tCLA=tpg+tpg_block+(Nk−1).tAND_OR+k.Tfa

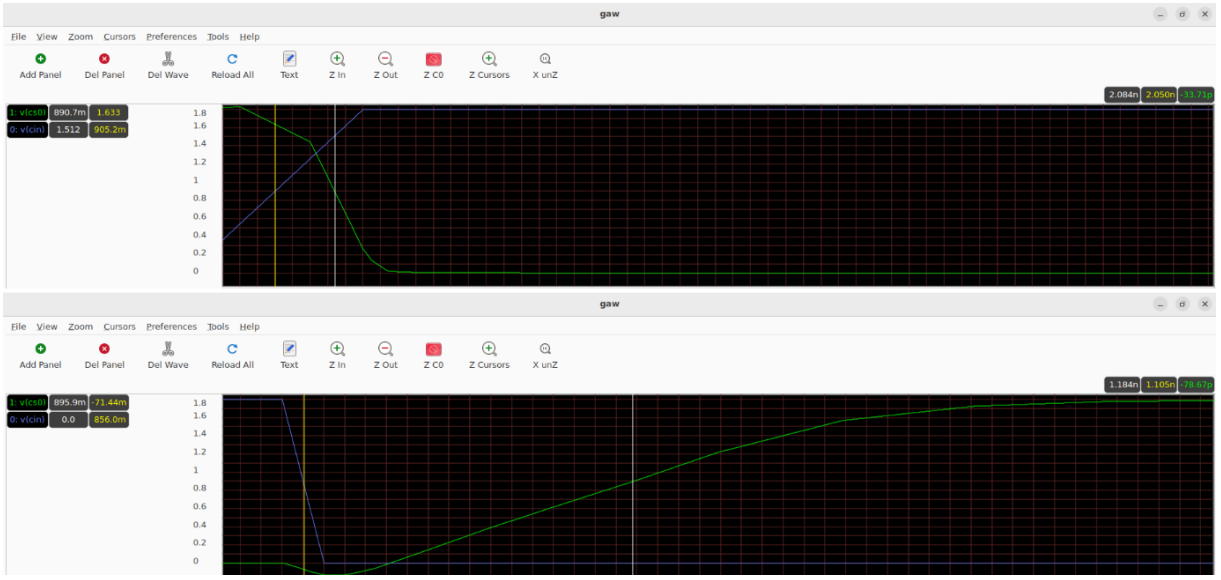
input ->S4 is the critical path.

Critical path is from input ->generator propagate block ->AND blocks->carry of (n-1)th bit ->final sum block of final bit

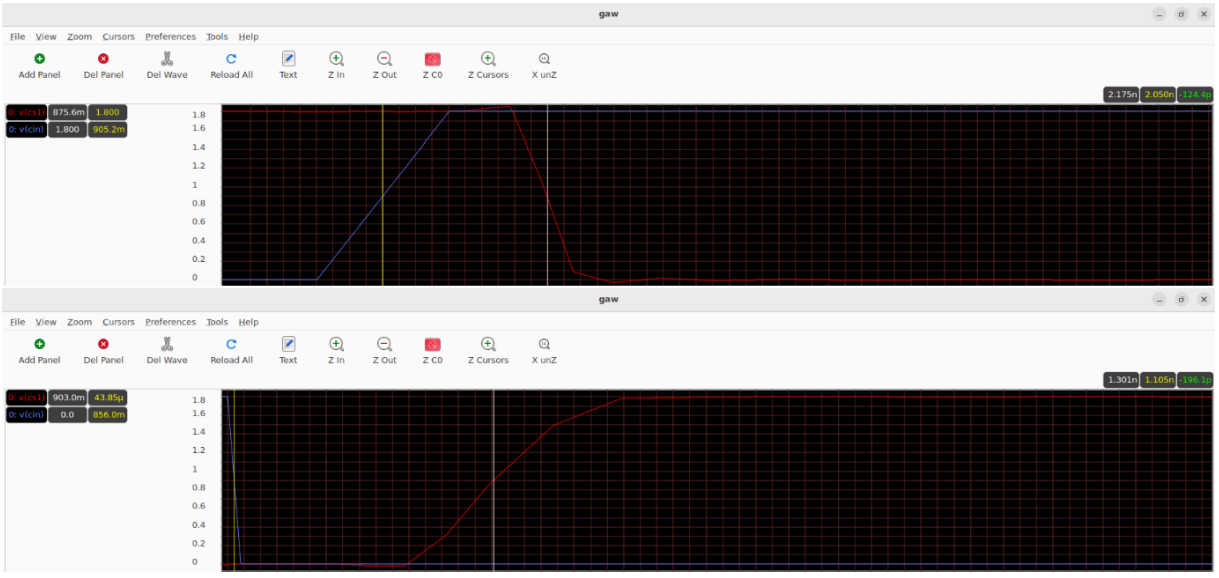
SCHEMATIC SIMULATIONS ACROSS ALL CORNERS (TT,SS,FS,SF,FF) AND TEMPERATURES(-40,27,125):

TT corner - Temperature – (-40)

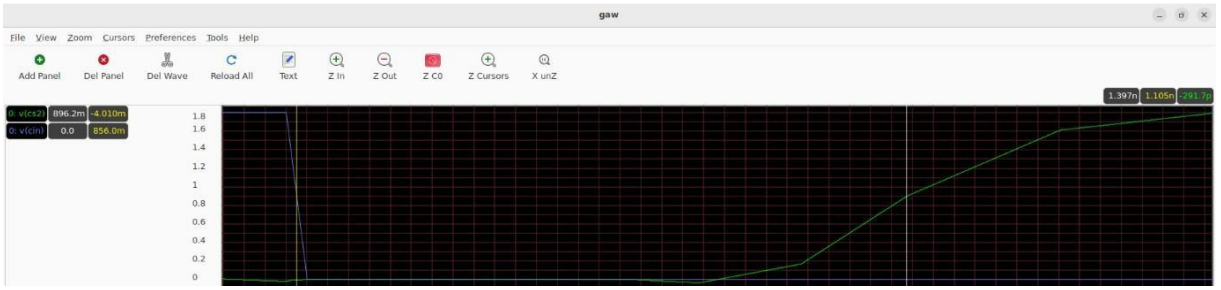
S0 delay = (33.71+78.67)/2 = 56.19 p



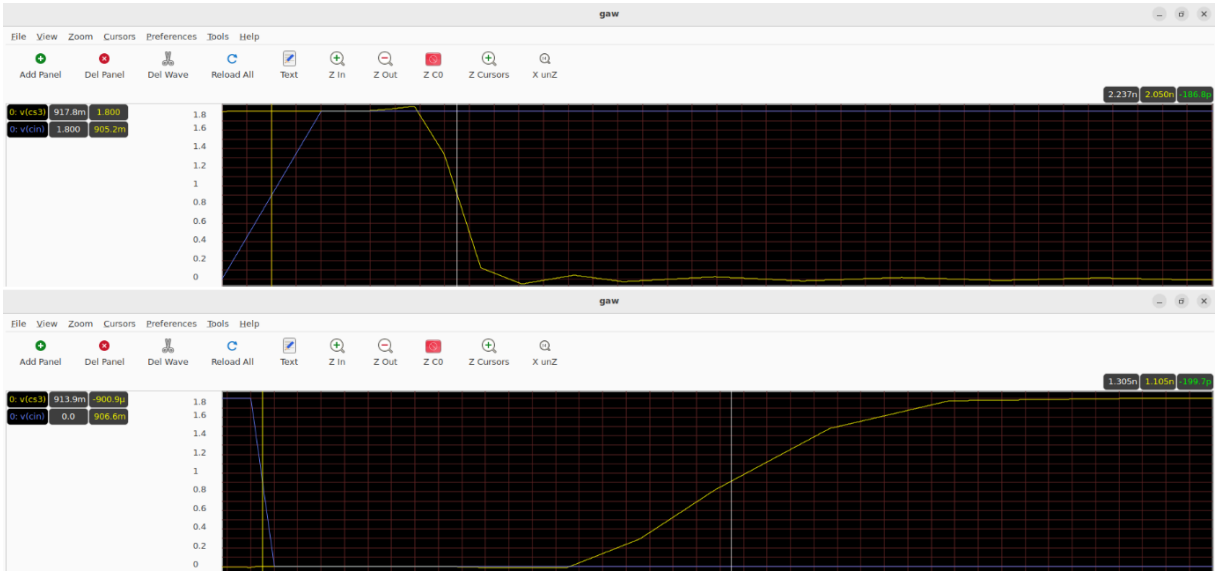
S1 –delay = (196+124)/2 =160p



S2 delay =(259+291)/2 =271

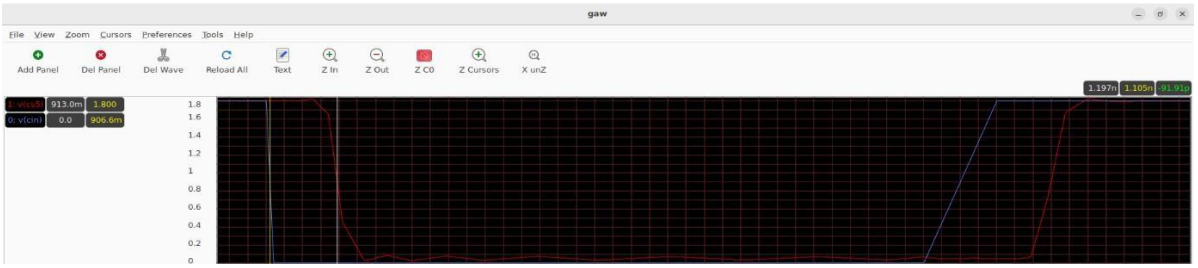


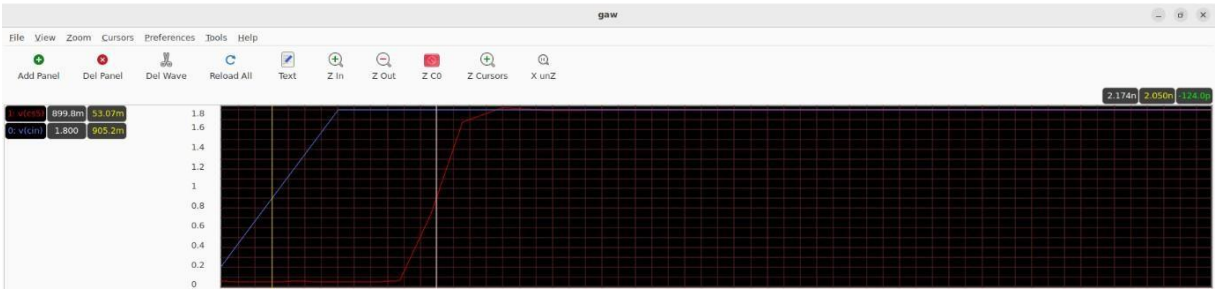
S3 delay = (186+199)/2 = 192.5p



S4 delay = (194+171)/2 =182.5p

S5 delay = (91+124)/2 = 107.5p



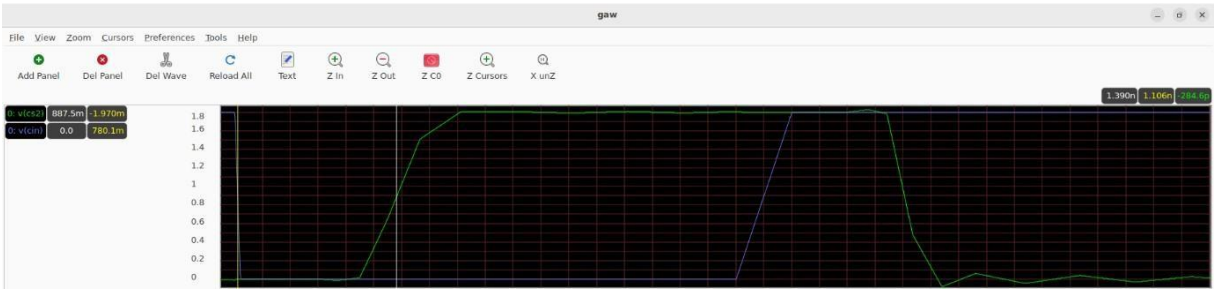


TT corner – Temperature (27)

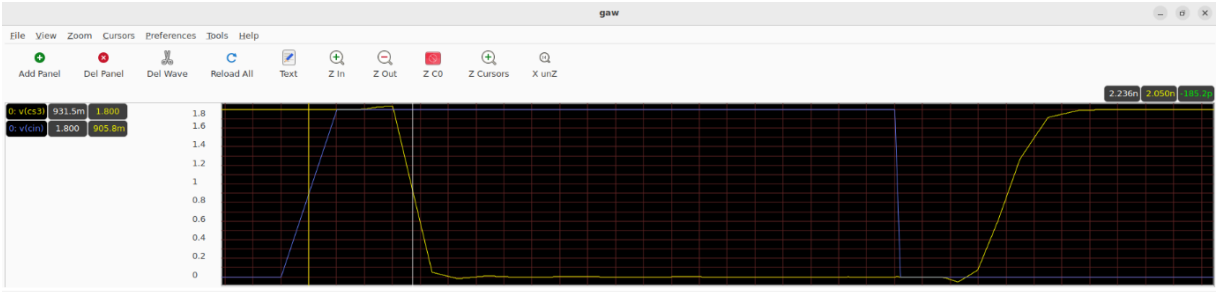
S0 delay = (37.13+74.59)/2 = 56p

S1 delay = (125 + 199)/2 = 162p

S2 delay = (252 + 284)/2 = 268p

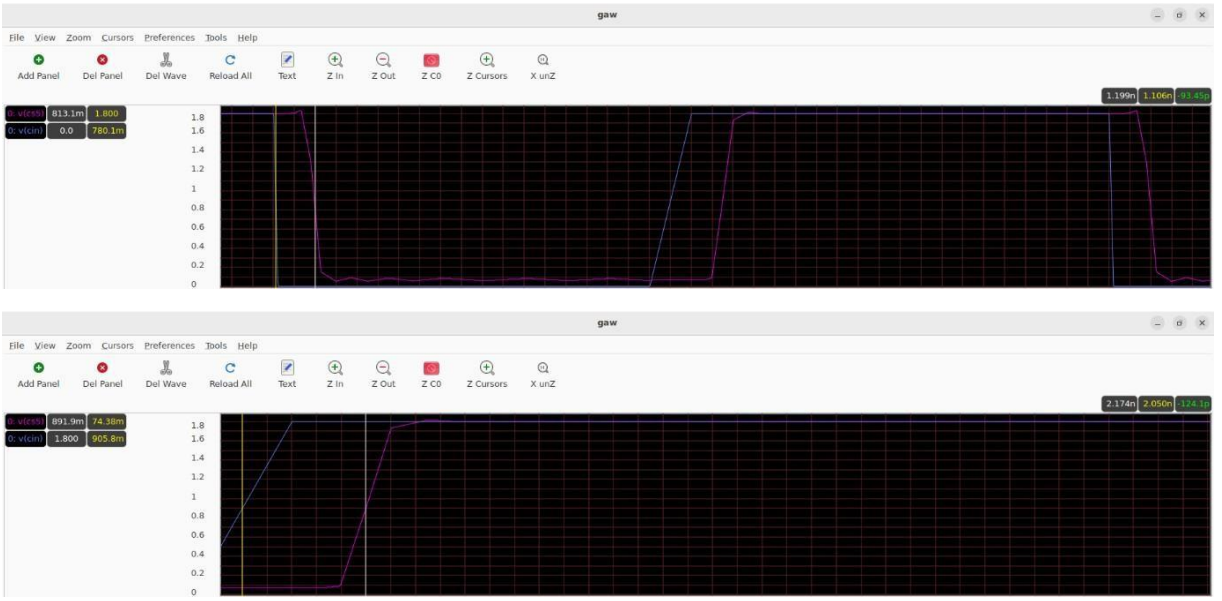


S3 delay = (185+195)/2 = 190



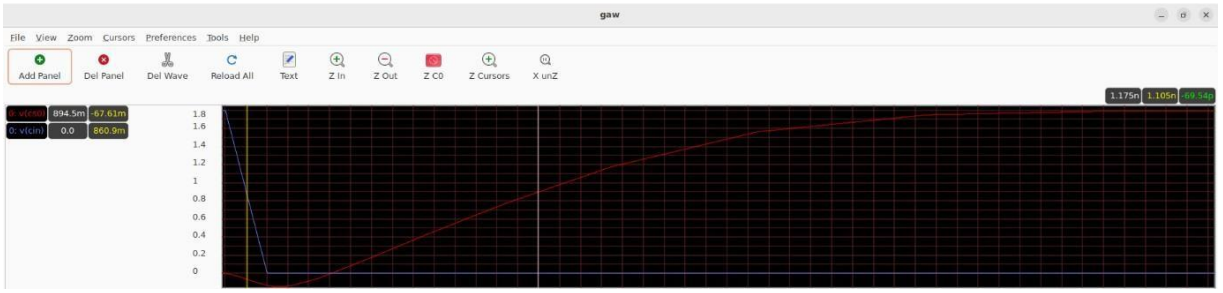
S4 delay = (202+167)/2 = 184.5p

S5 delay = (93.45 +124)/2 = 109p

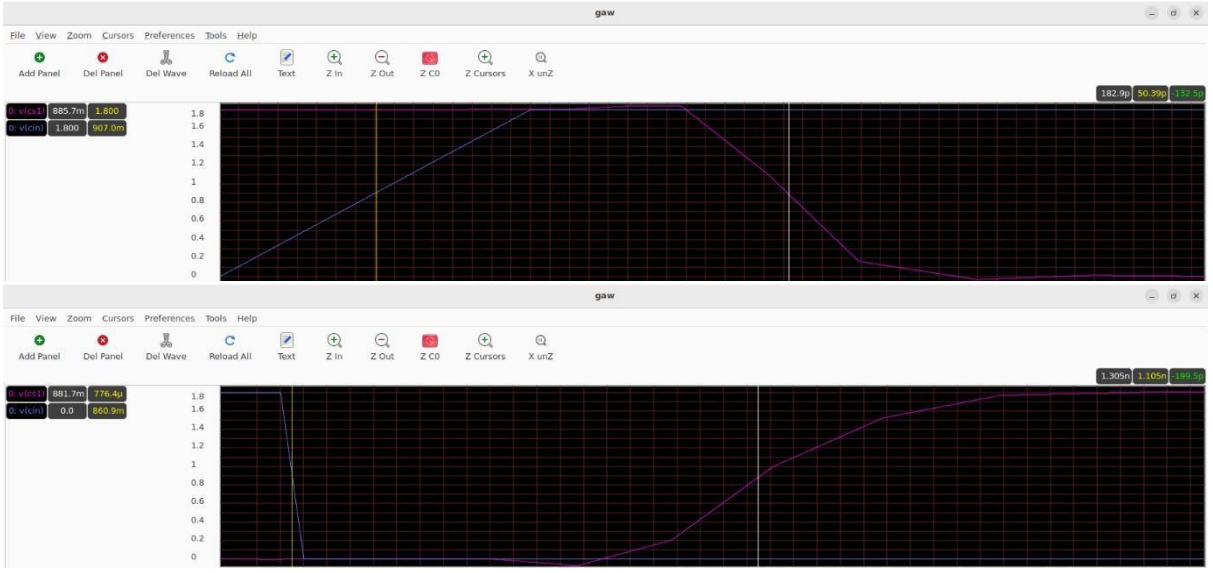


TT corner – Temperature (125)

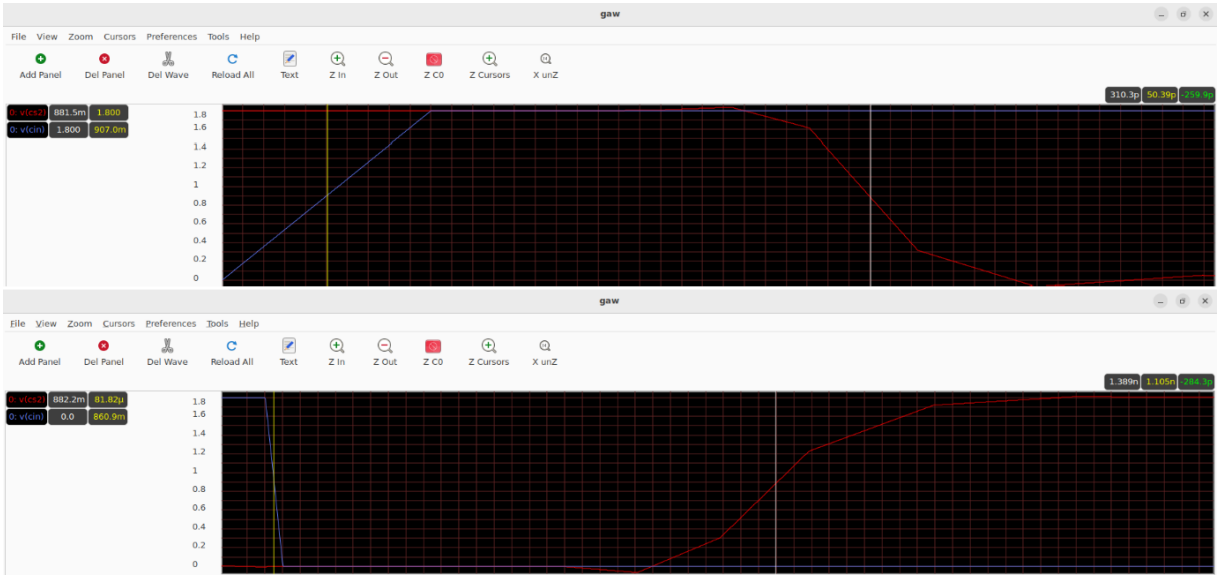
S0 delay = (50 + 69)/2 = 59.5



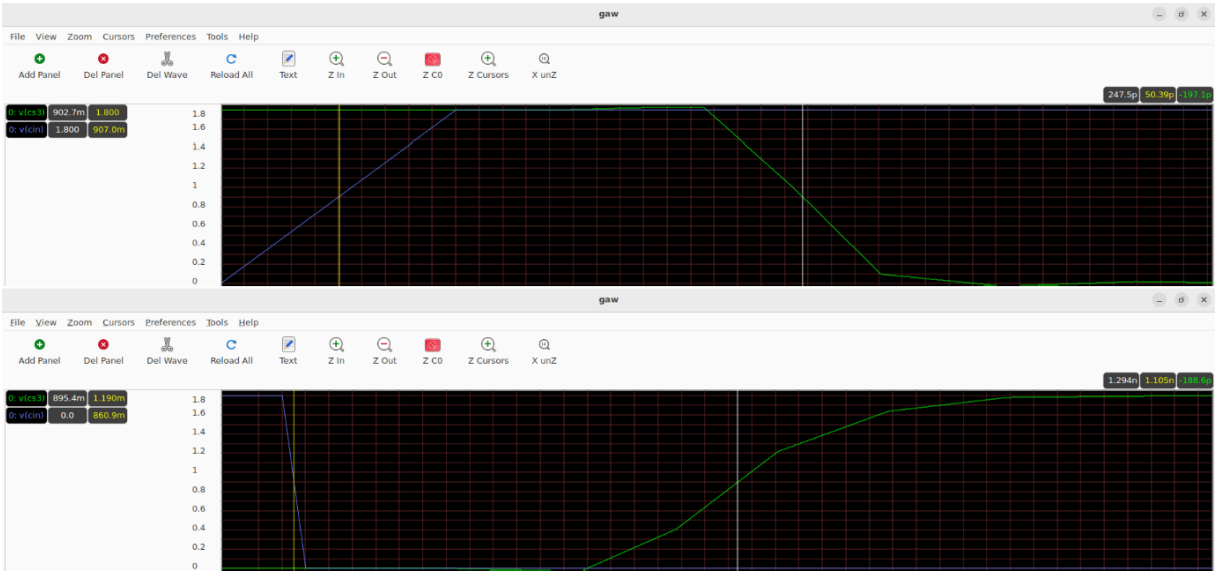
S1 delay = (132+ 199)/2 = 166p



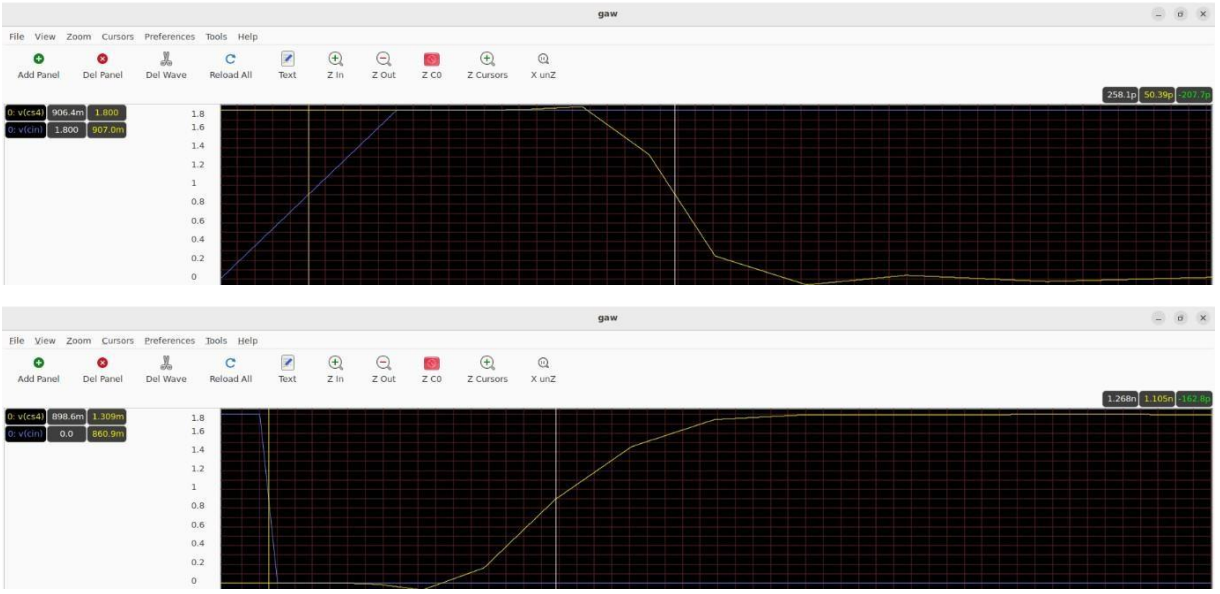
S2 delay = (259+284)/2 = 271.5p



S3 delay = (197+188)/2 = 192.5 p



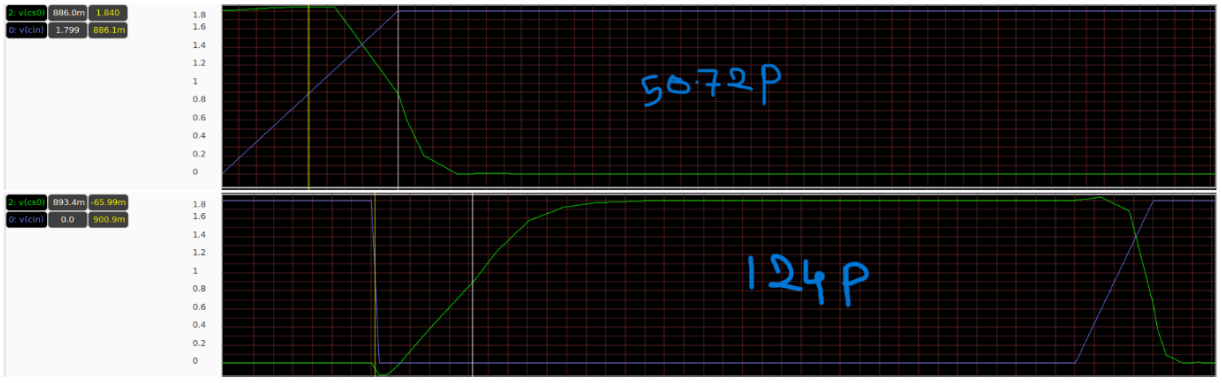
S4 delay = (207+162)/2 = 184.5p



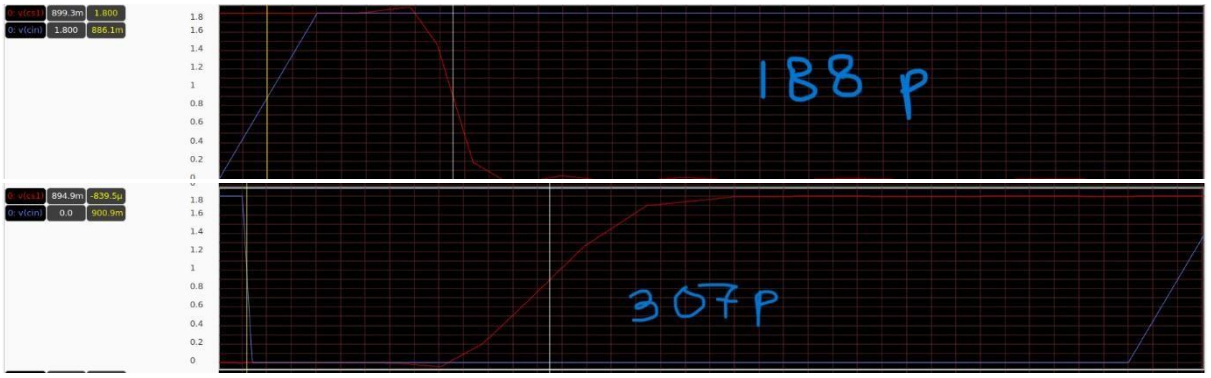
S5 delay = (89+130)/2 = 109.5p

SS corner –Temperature (-40)

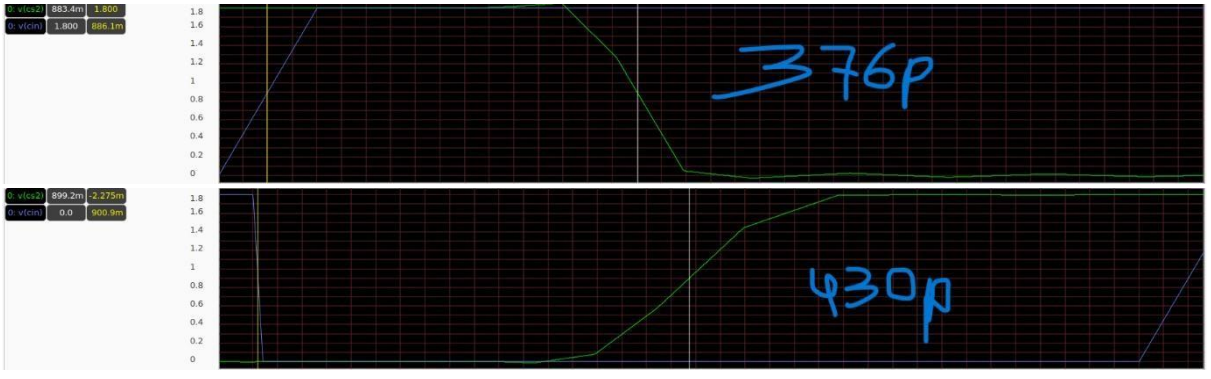
S0 delay = (50.72+124)/2 = 87p



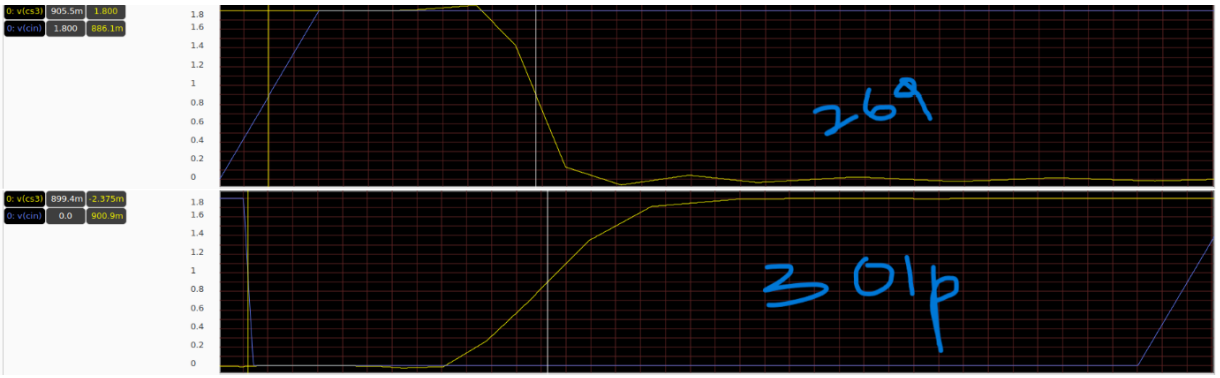
S1 delay = (188 + 307)/2 = 247.5p



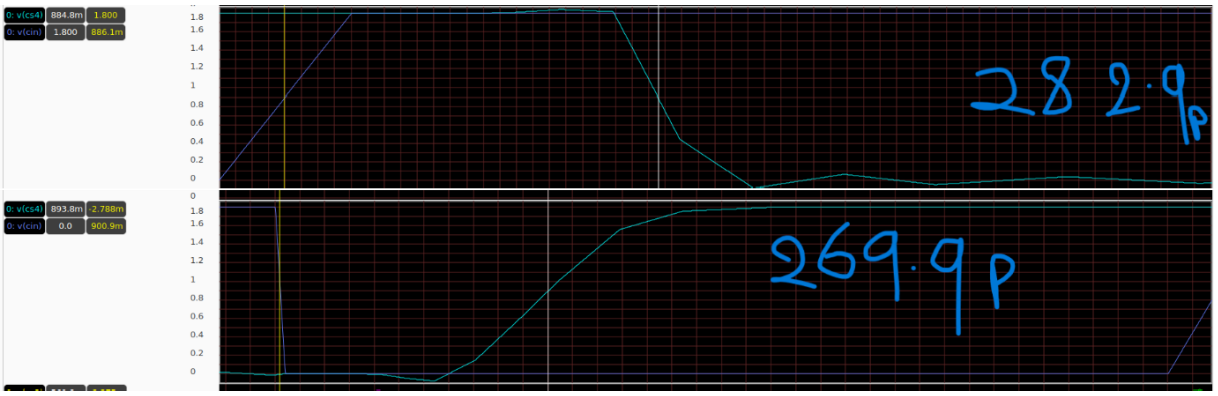
S2 delay =(376+430)/2= 388p



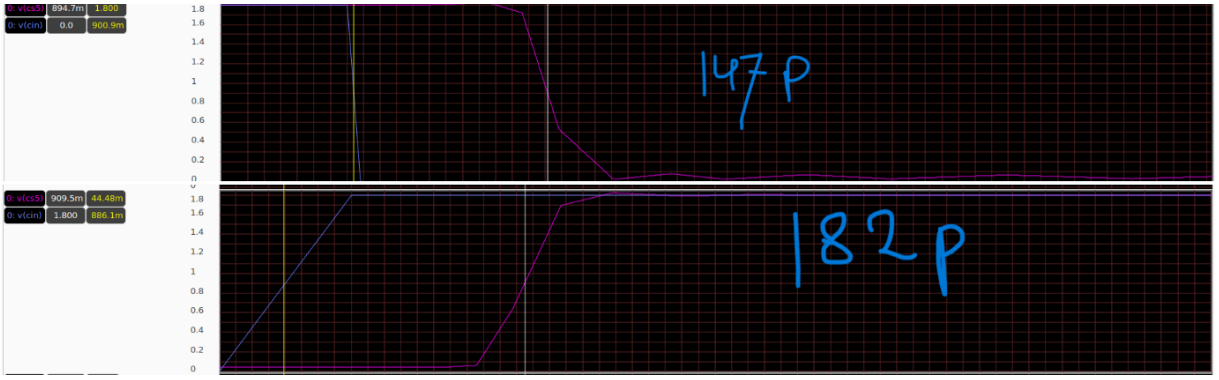
S3 delay = (269 + 301)/2 = 285p



S4 delay = (282.9 + 269.9)/2 = 277p

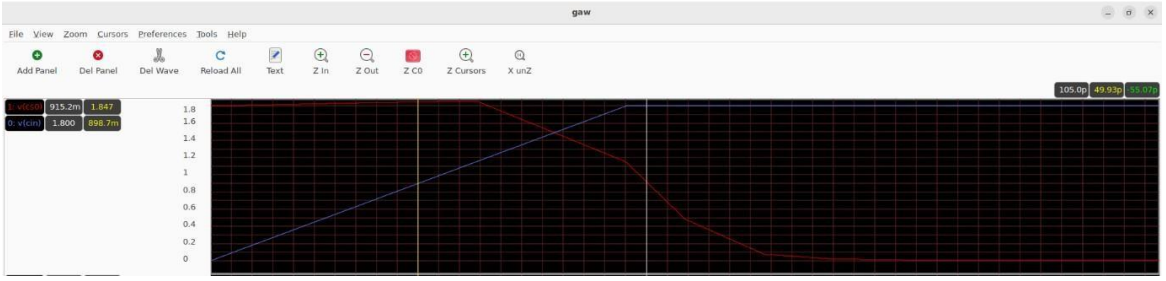


S5 delay = (147+182)/2 = 164.5 P

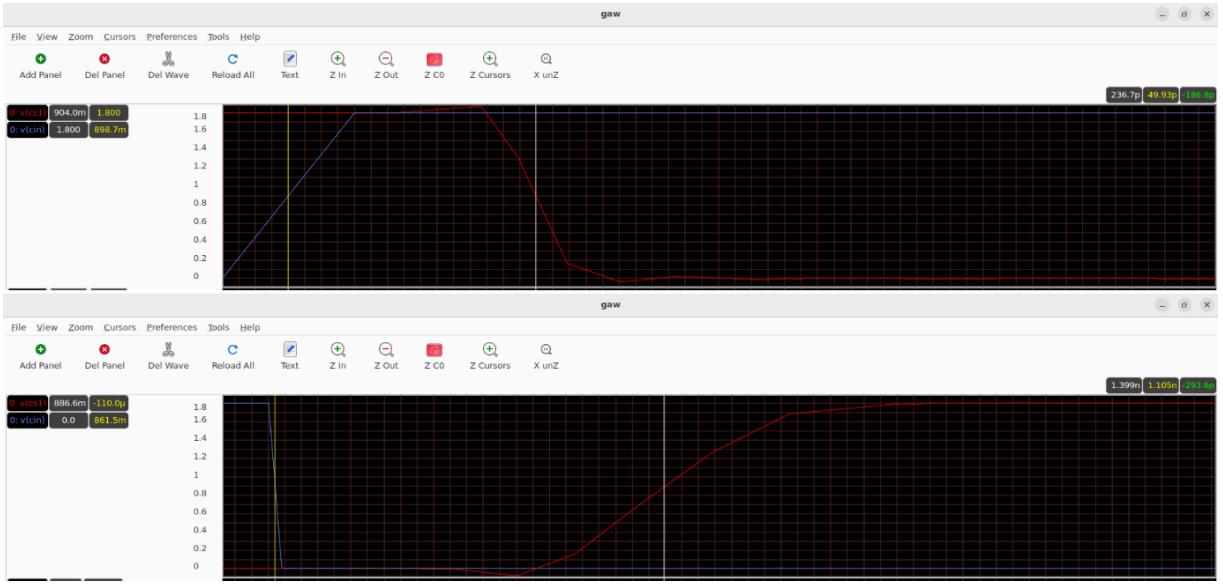


SS CORNER – TEMPERATURE (27)

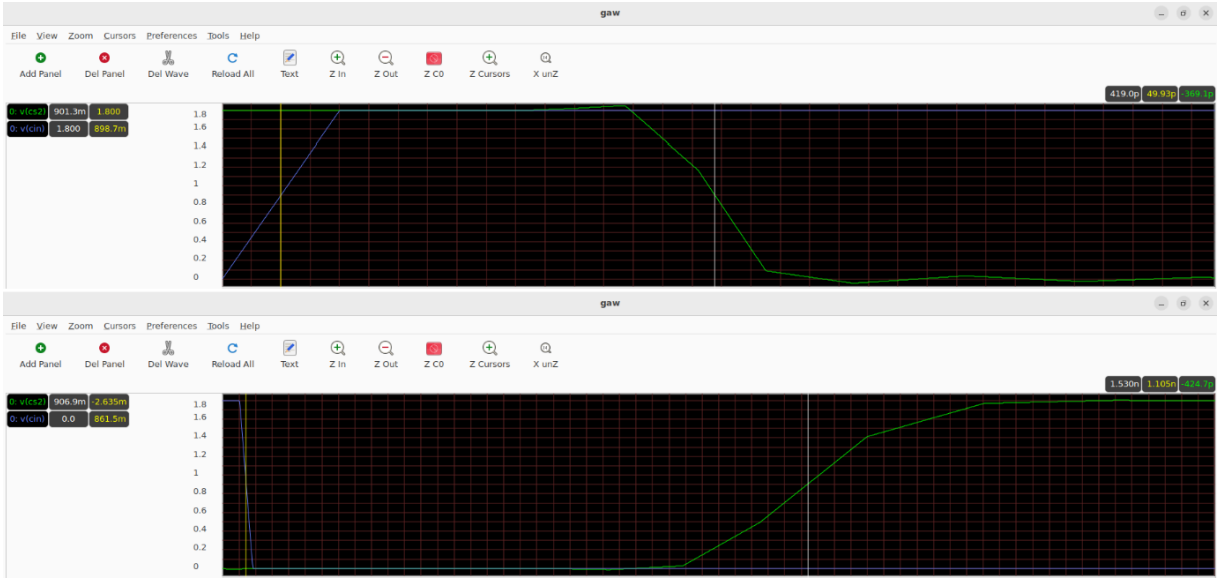
S0 delay = (55+114)/2 = 84.5 p



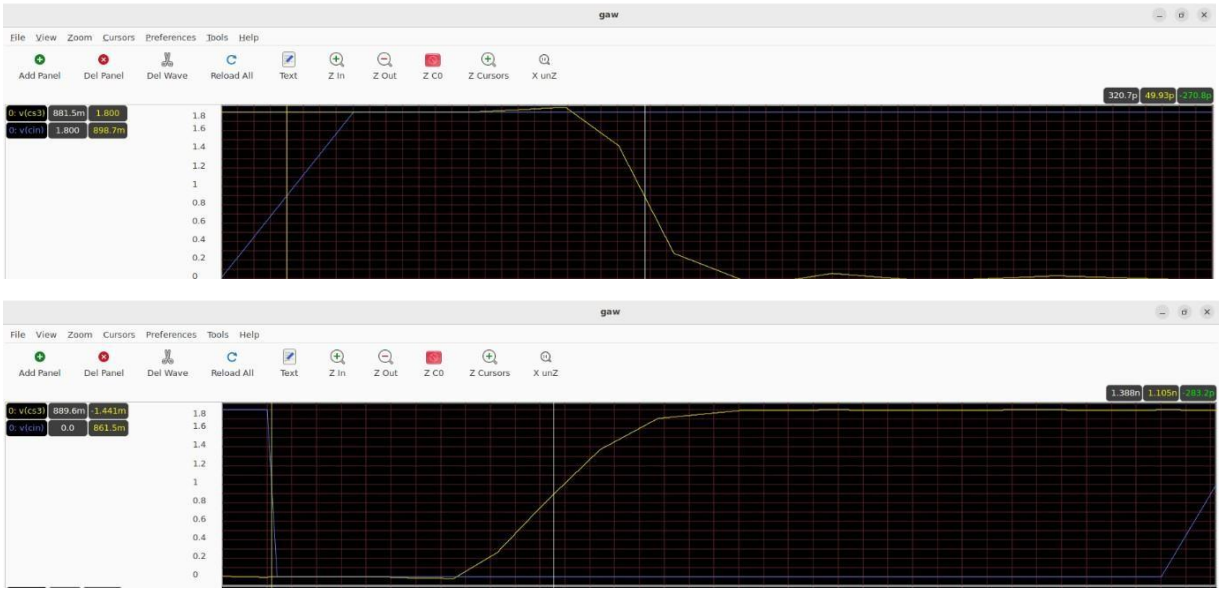
S1 delay = (186+294)/2 = 240p



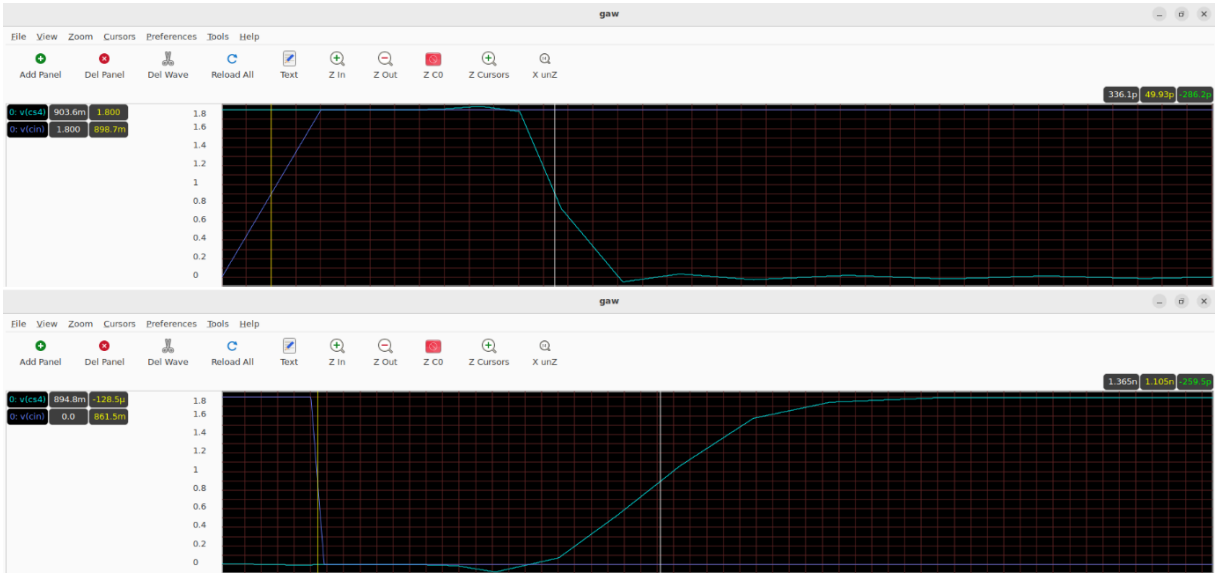
S2 delay = (369+424)/2 = 396.5p



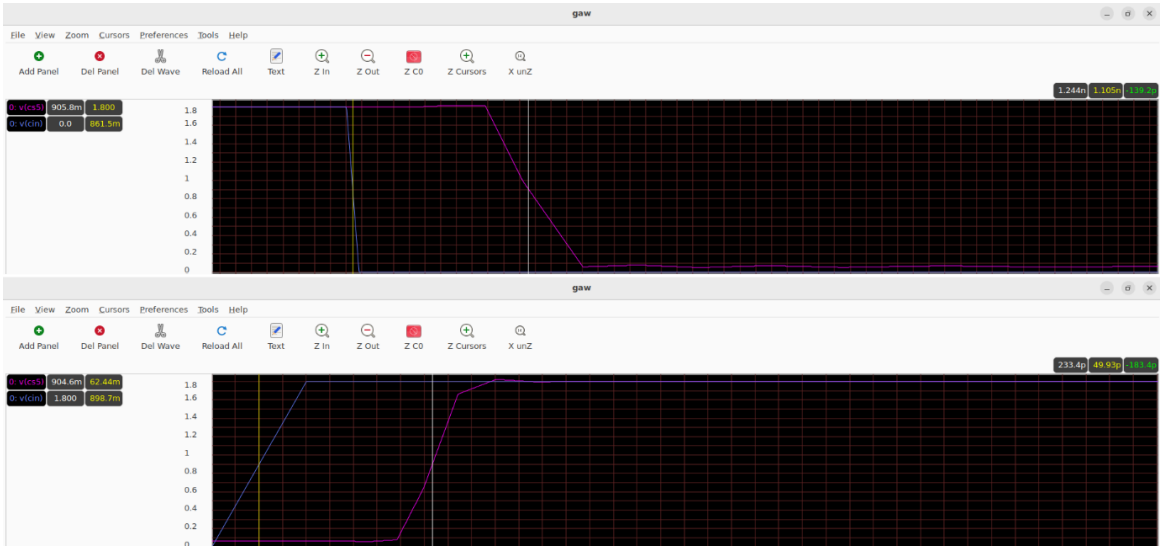
S3 delay = (270+283)/2 = 276.5 p



S4 delay = (286+259)/2 = 272.5 p

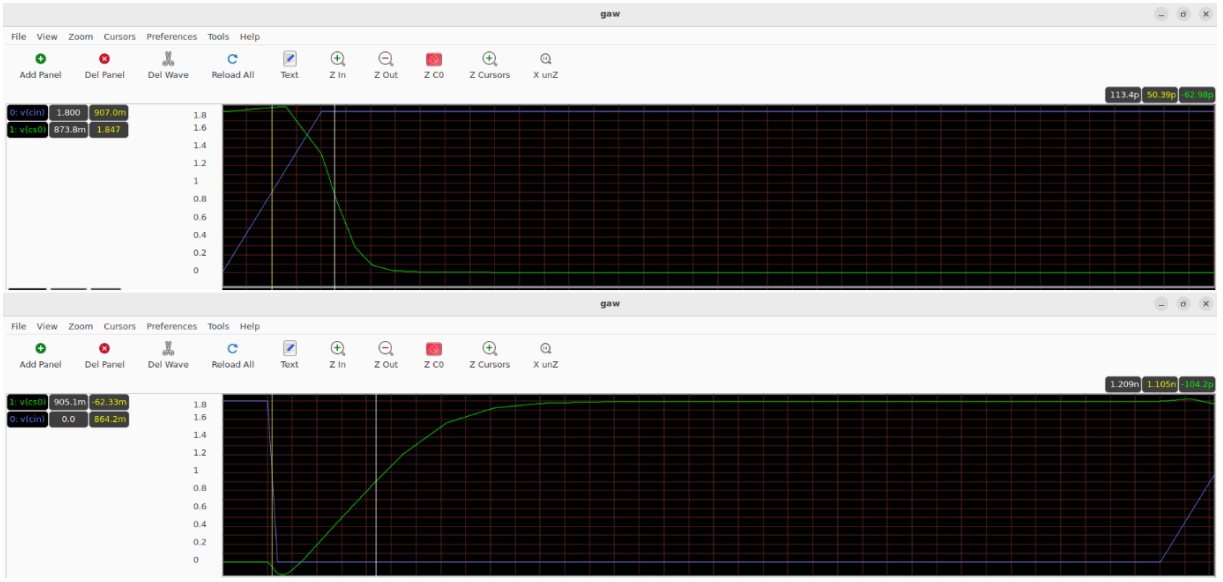


S5 delay = (139+183)/2 = 161p

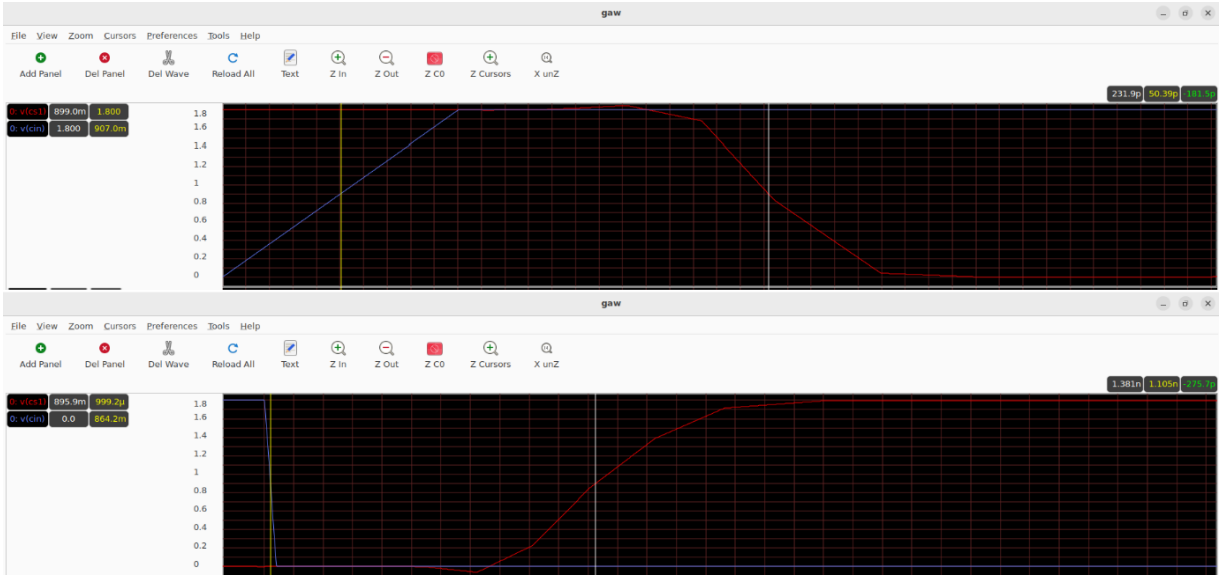


SS corner – Temperature (125)

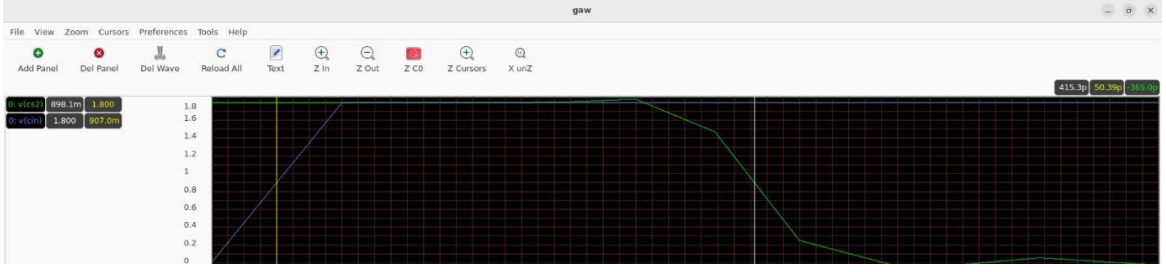
S1 delay = (63+104)/2 = 83.5p



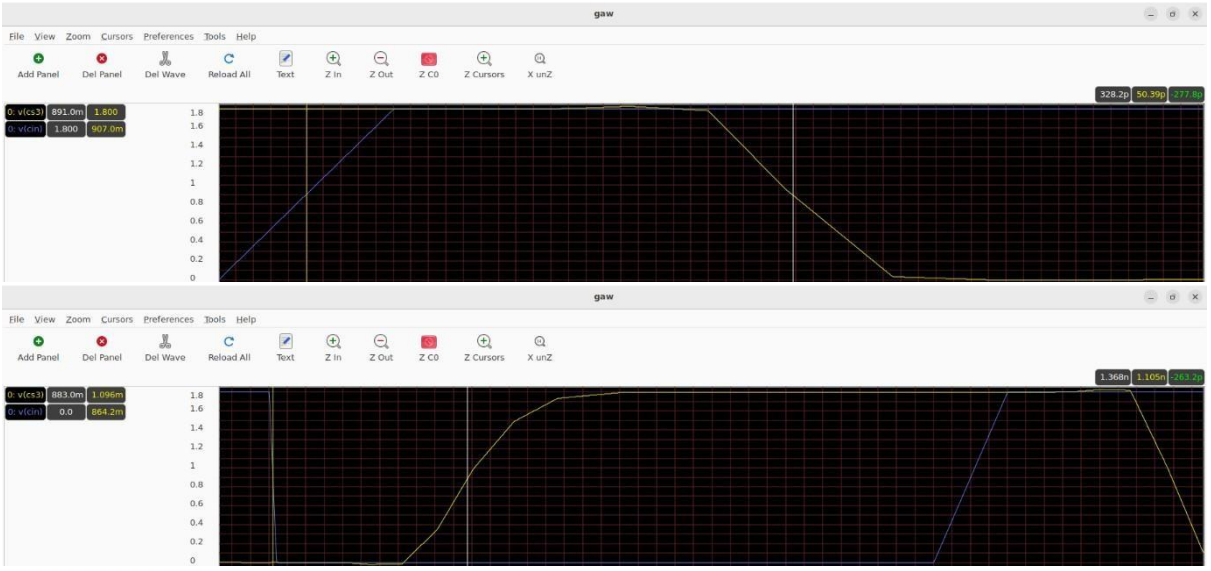
S1 delay = (182+275)/2 = 228p



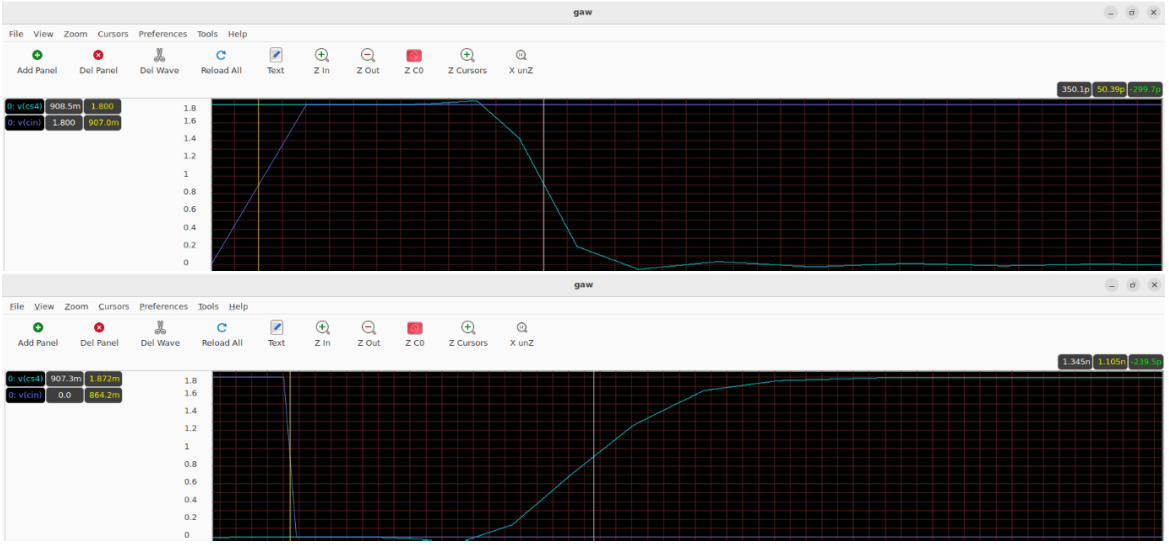
S2 delay = (365 + 414)/2 =389.5p



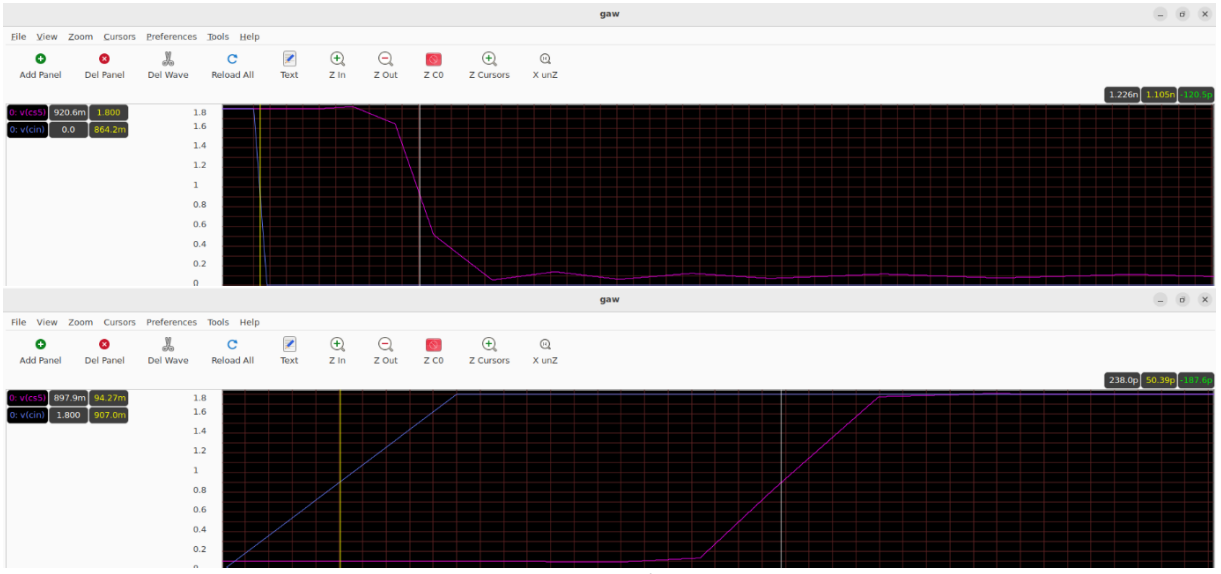
S3 delay = (278+263)/2 = 268p



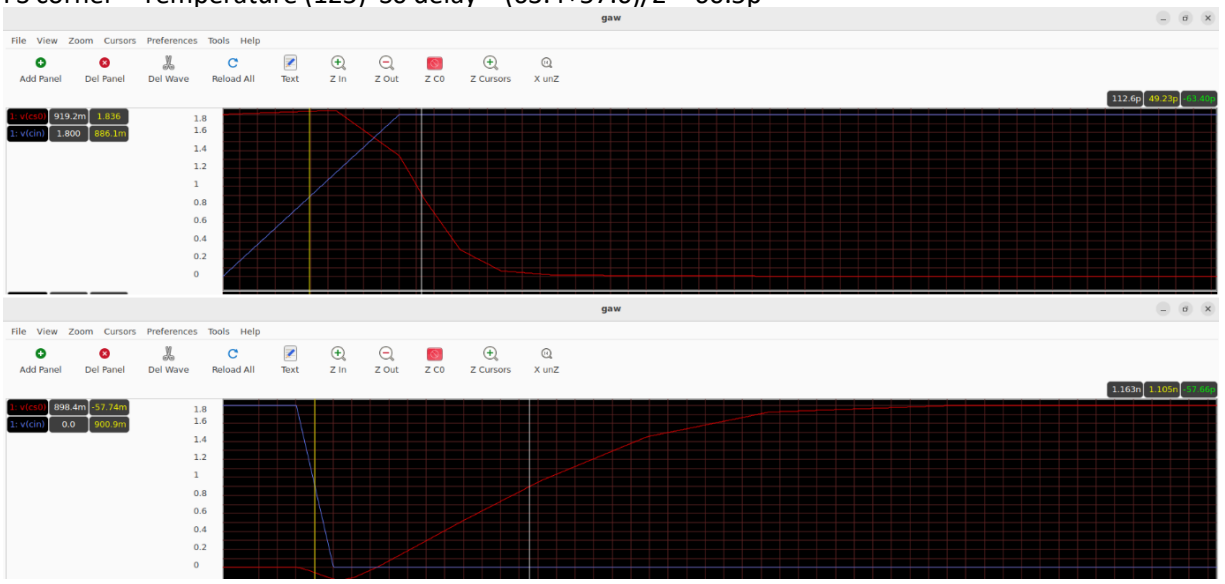
S4 delay = (299+239)/2 = 269p



S5 delay = (120+187)/2 = 153.5p

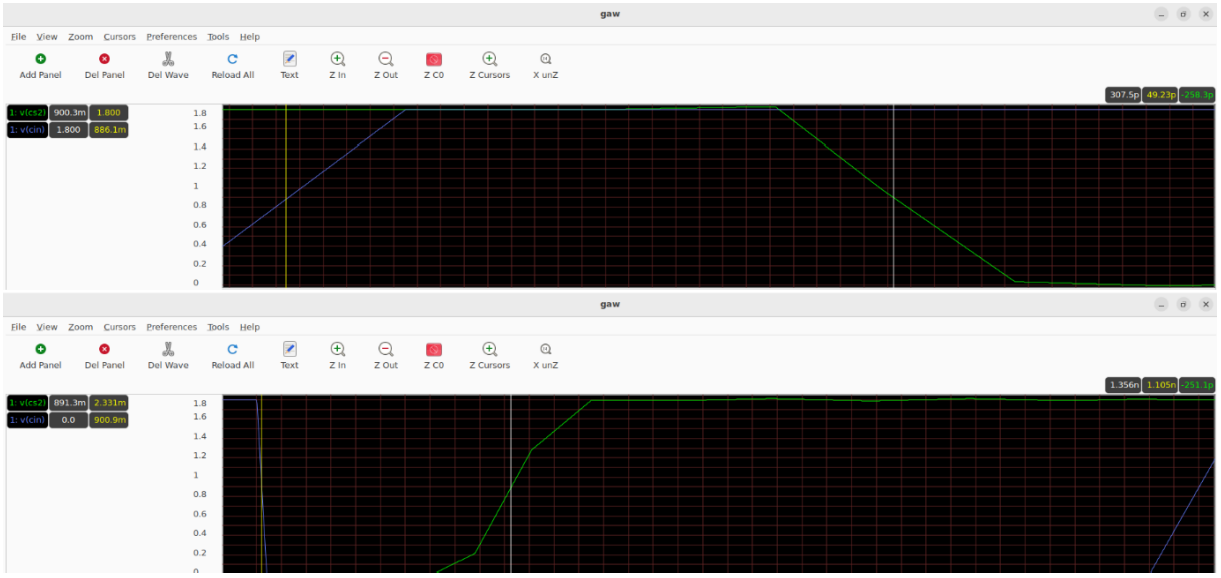


FS corner – Temperature (125) S0 delay = (63.4+57.6)/2 = 60.5p

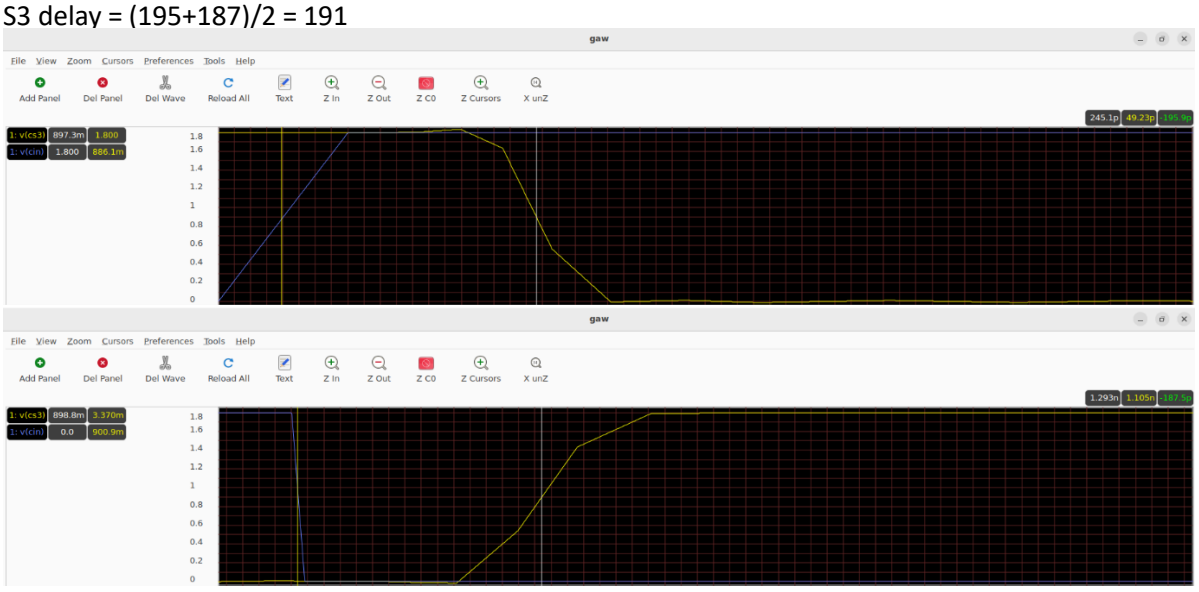


S1 delay = (146+200)/2 = 173p

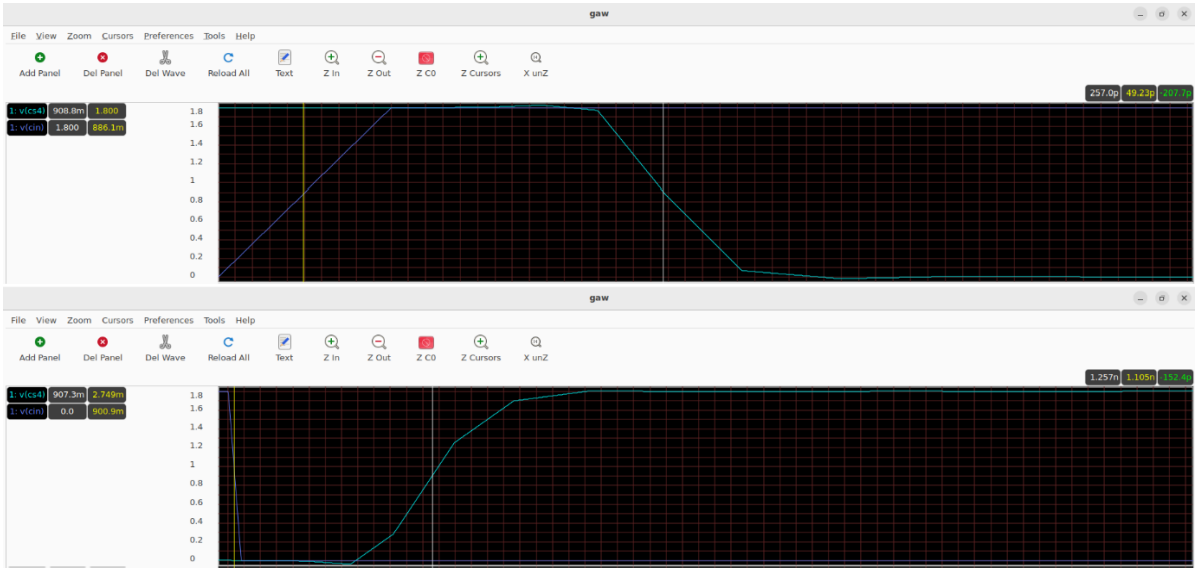
S2 delay = (258+251)/2 = 254.5p



S3 delay = (195+187)/2 = 191



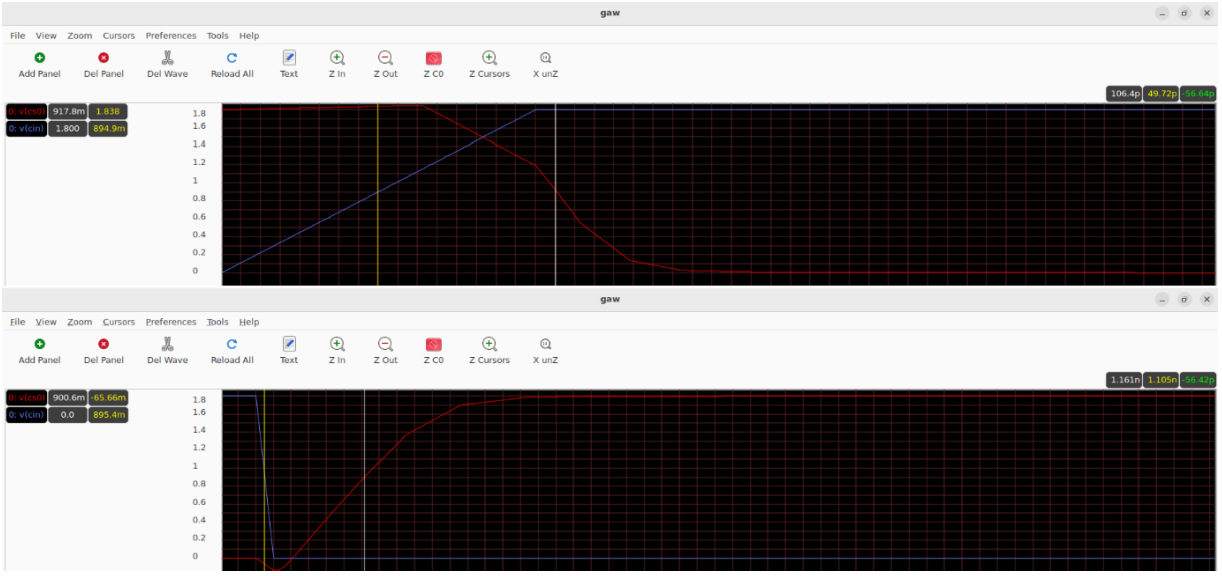
S4 delay = (207+152)/2 = 179.5p



S5 delay = (88+131)/2 = 109.5 p

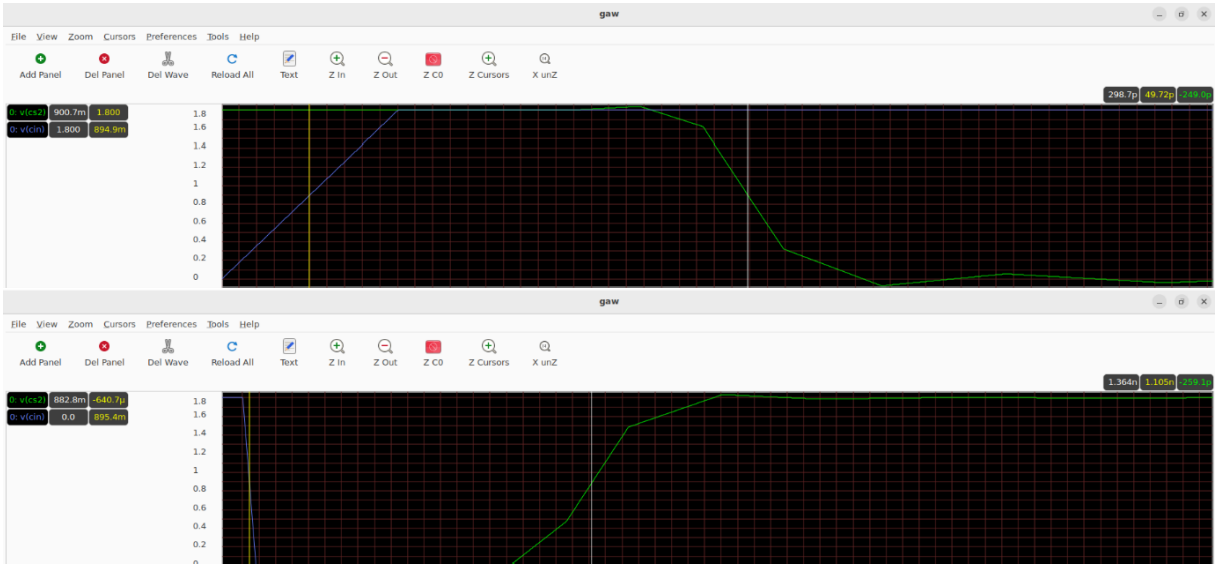
FS corner – temperature (-40)

S0 delay = (56.64+56.42)/2 = 56.5

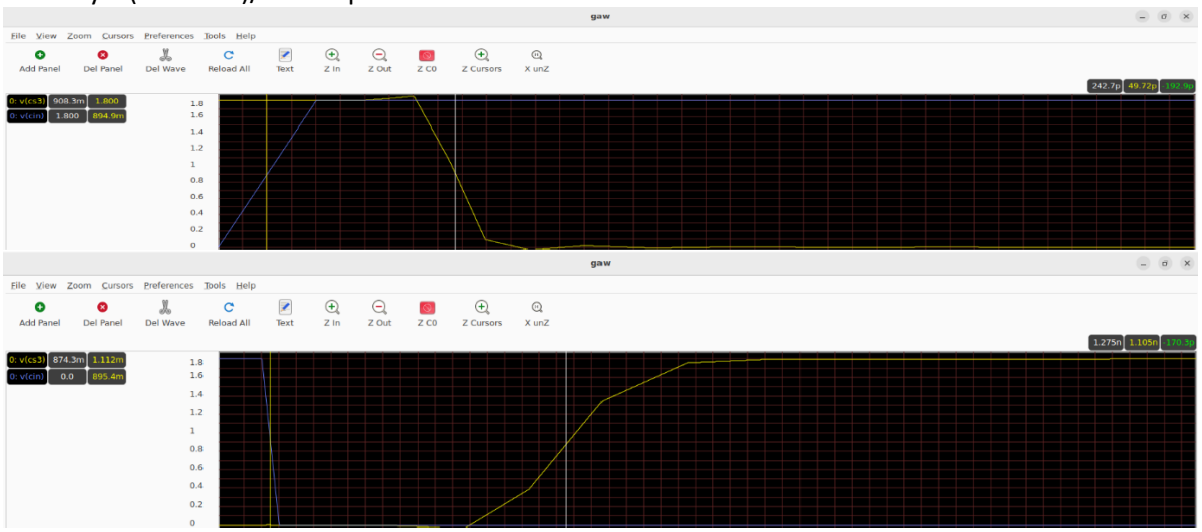


S1 delay = (130+178)/2 = 154

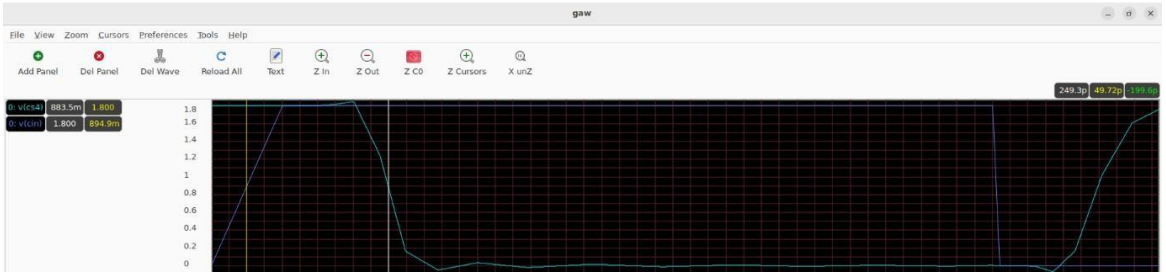
S2 delay = (249+259)/2 = 254

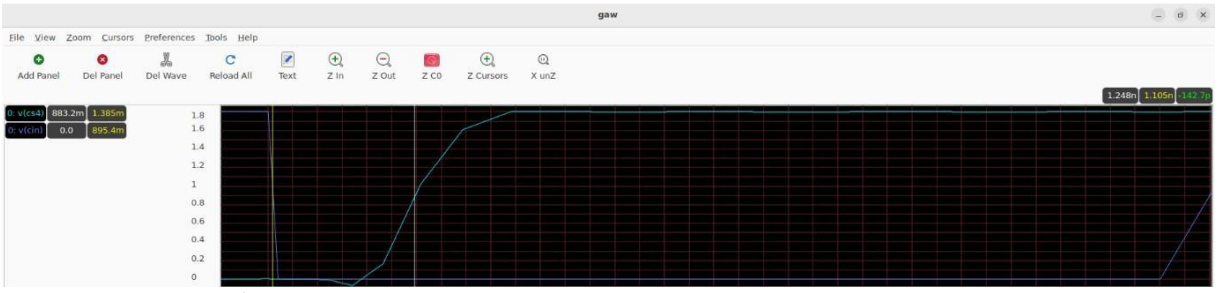


S3 delay = (192+170)/2 = 181p



S4 delay = (199+142)/2 = 170.5

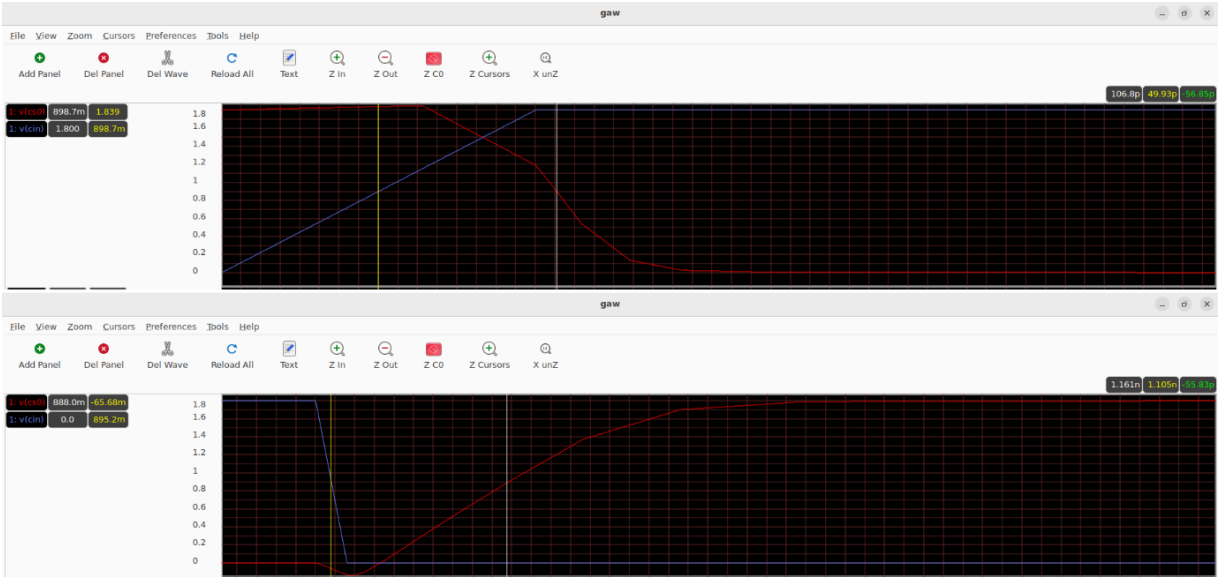




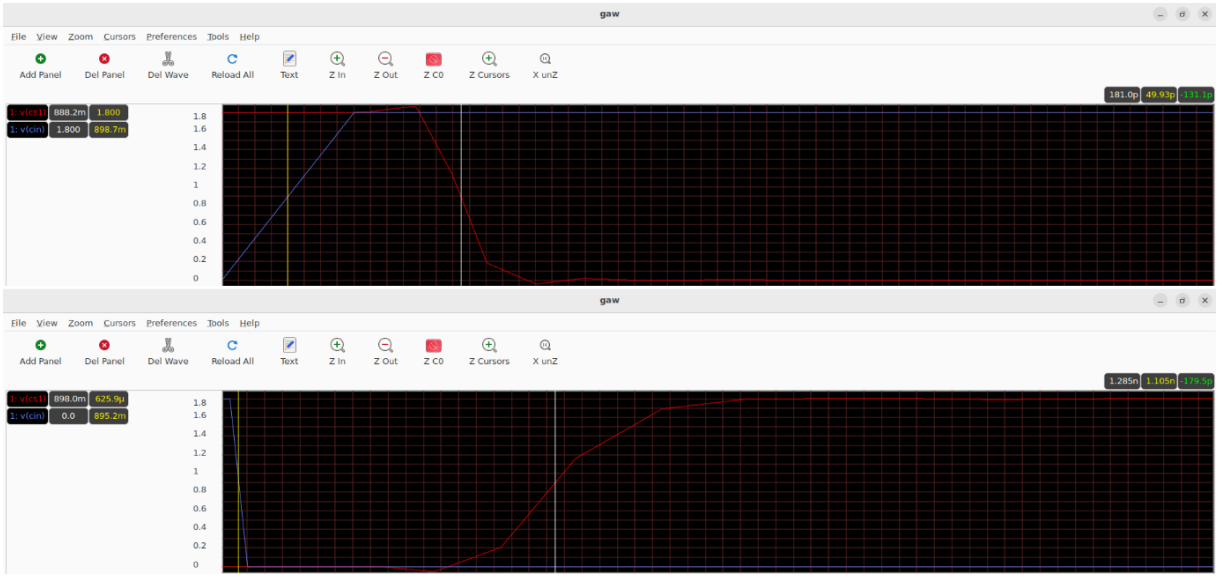
S5 delay = (87+126)/2 = 150p

FS corner – Temperature (27)

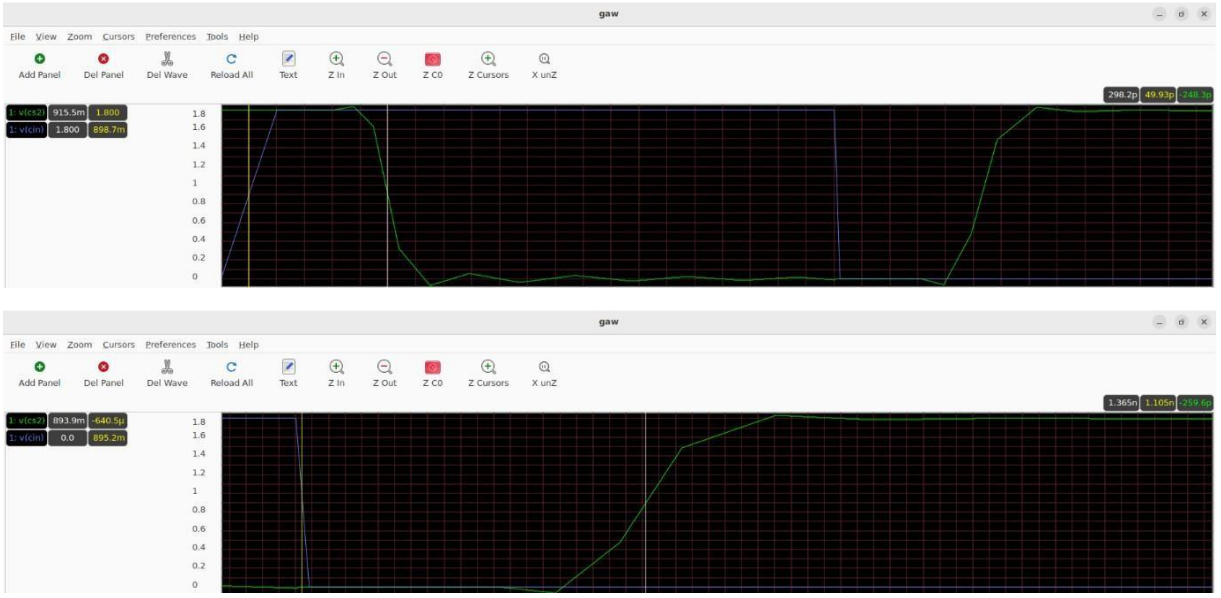
S0 delay = (56.85+55.83)/2 = 56.34



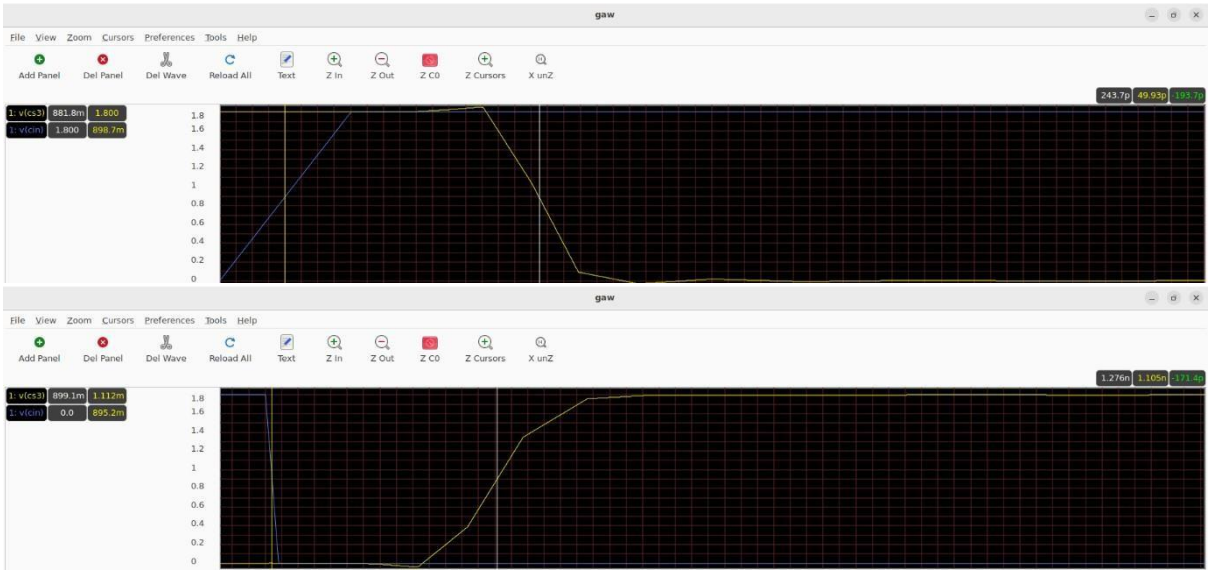
S1 delay = (131.1+179.5)/2 = 155.3 p



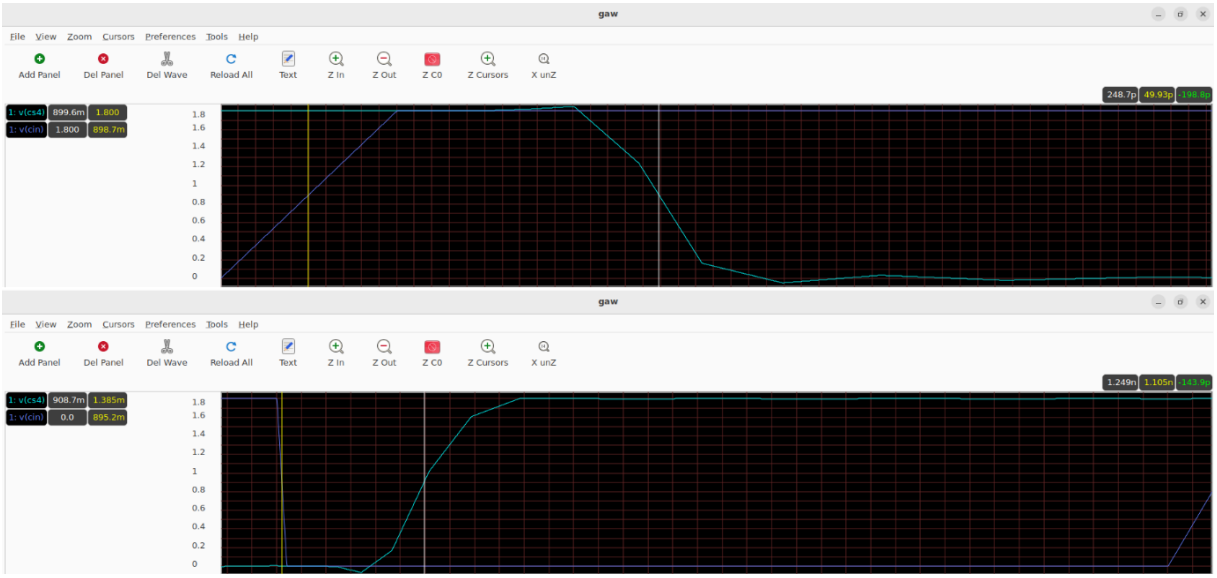
S2 delay = (248.3+259.6)/2 = 253.95 p



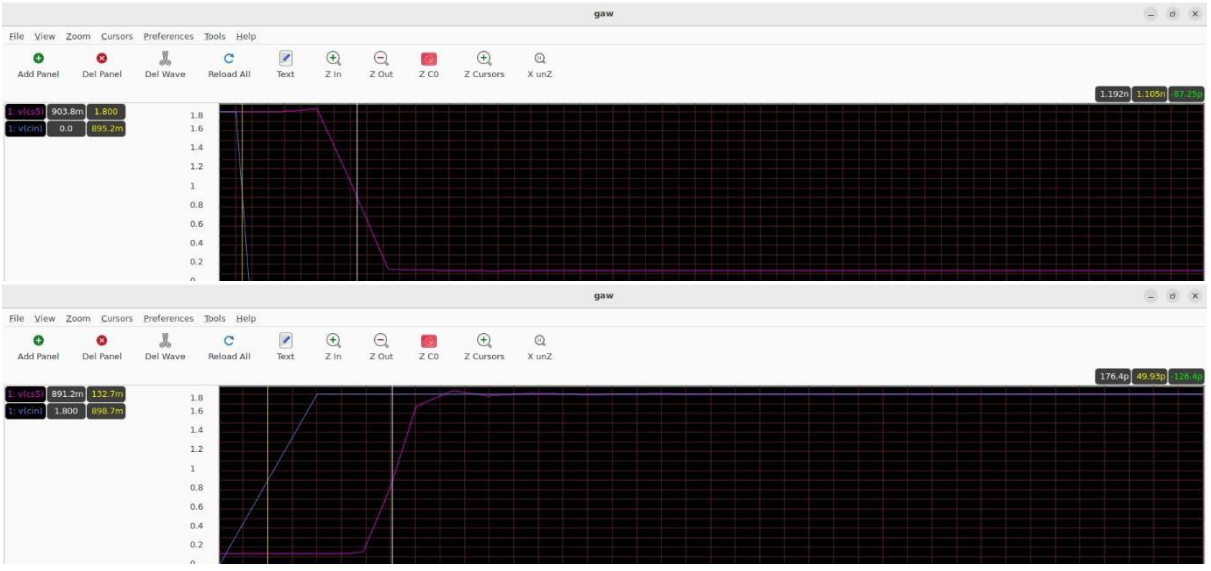
S3 delay = (193.7+171.4)/2 = 182.5 p



S4 delay = (198+143)/2 = 170.5p

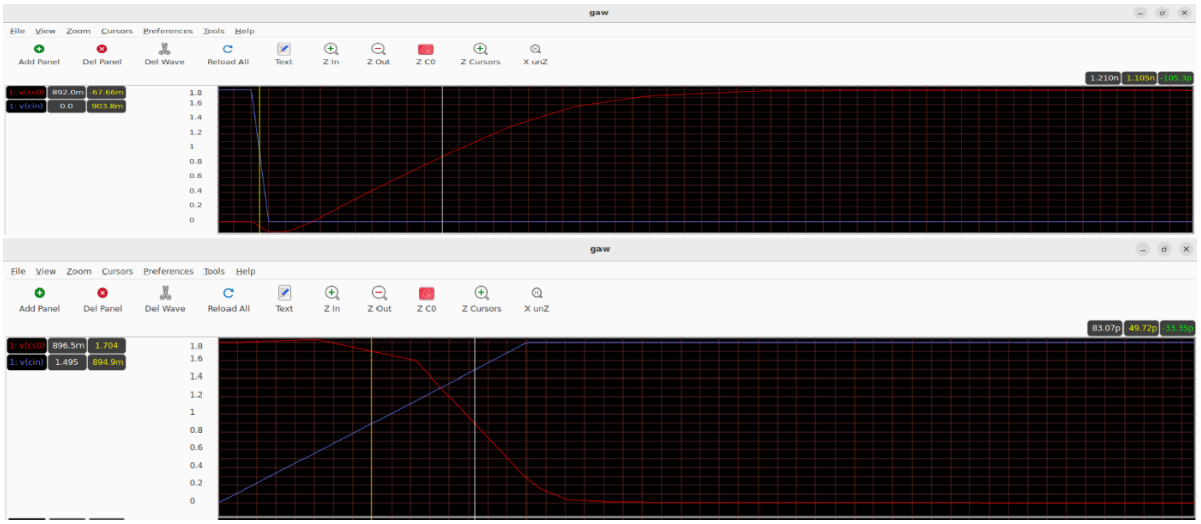


S5 delay = (87.25+126.4)/2 = 106.825p

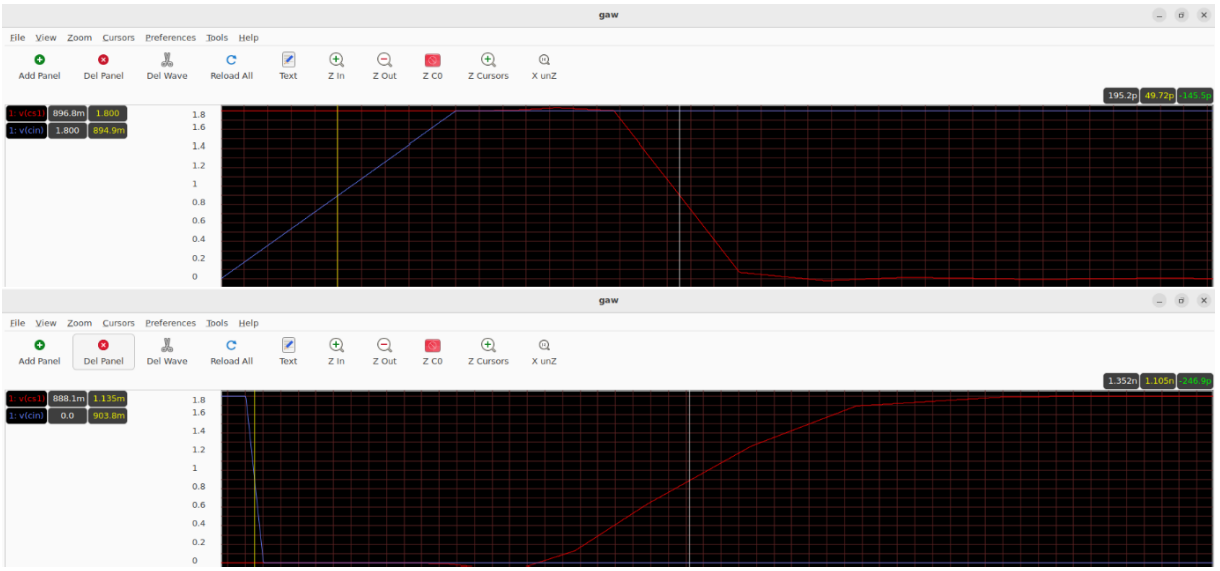


SF corner Temperature (27)

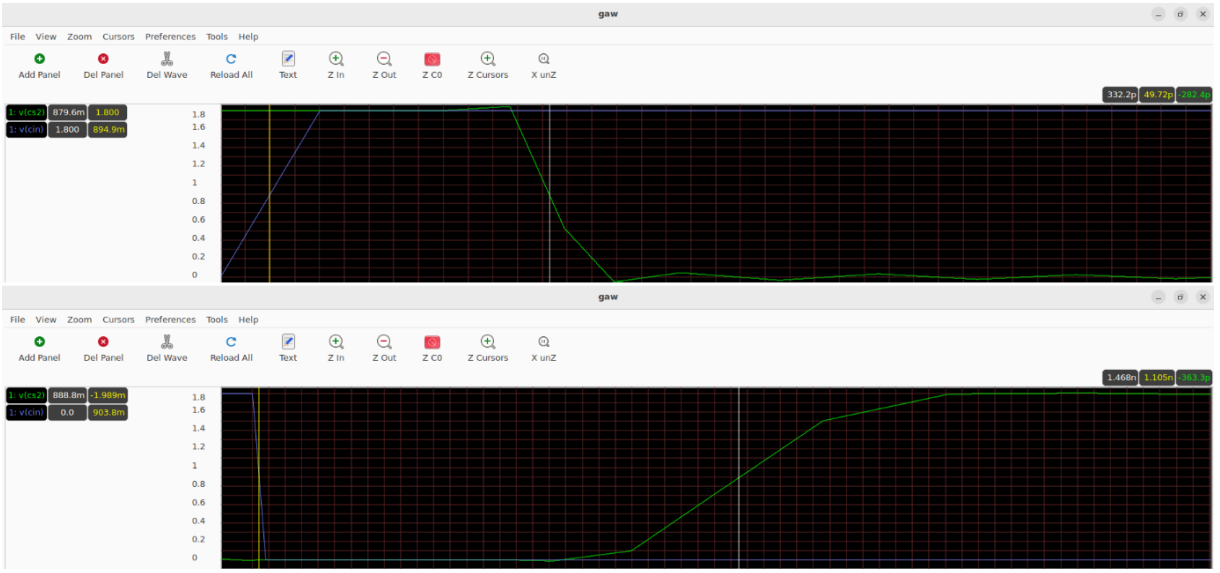
S0 delay = (33.35+105.3)/2 = 69.4



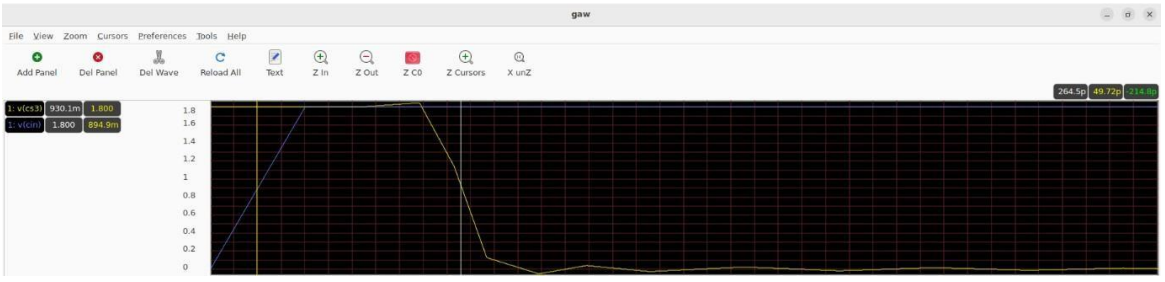
S1 delay = (145 + 246)/2 = 195.5p



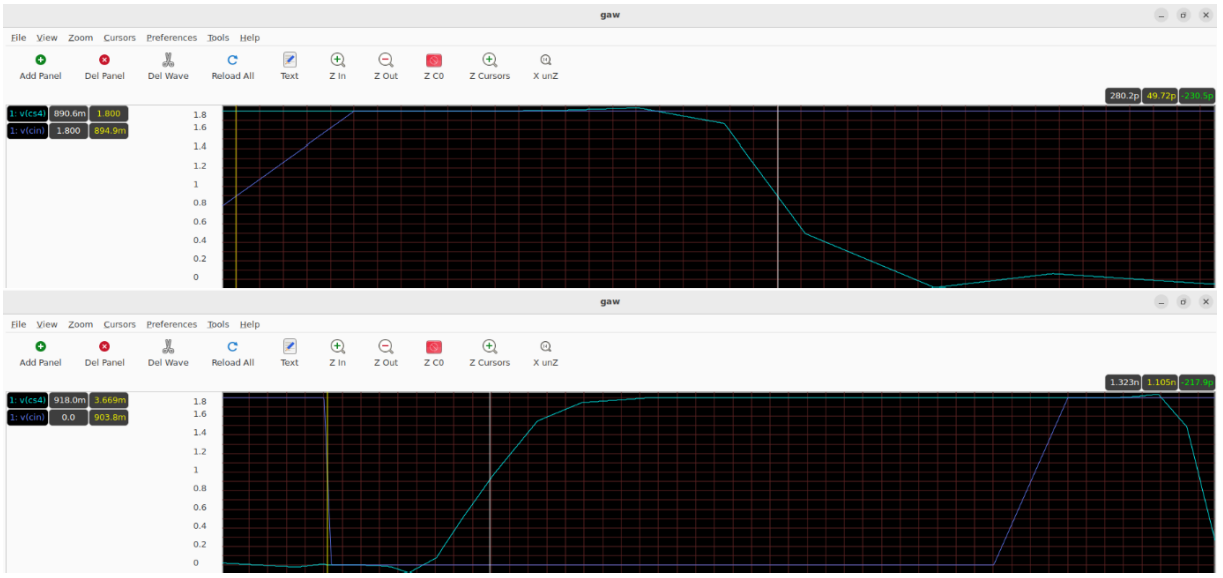
S2 delay = (282.4+ 363.3)/2 = 322.7



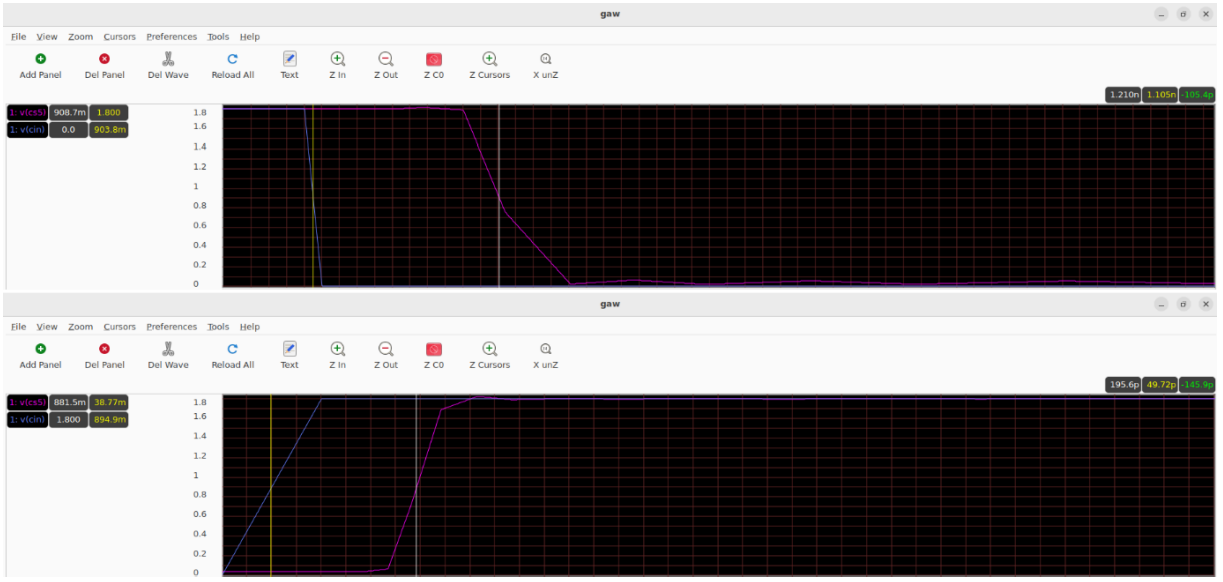
S3 delay = (214.8+239.1)/2 =226.95p



S4 delay = (230.5+217.9)/2 = 224.2p

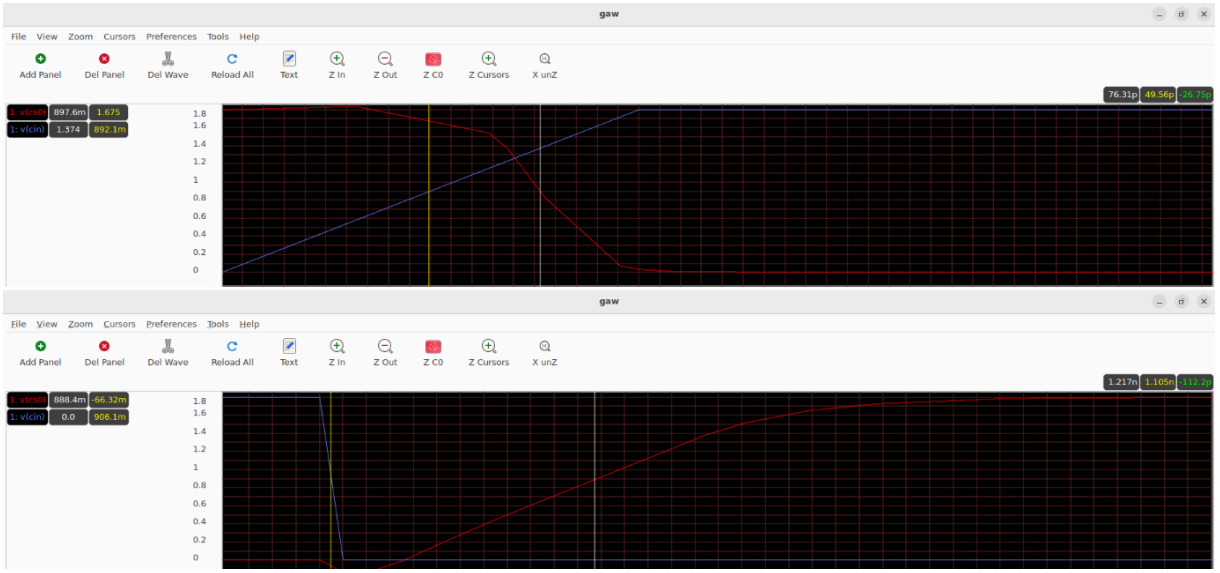


S5 delay = (105+145)/2 = 125p

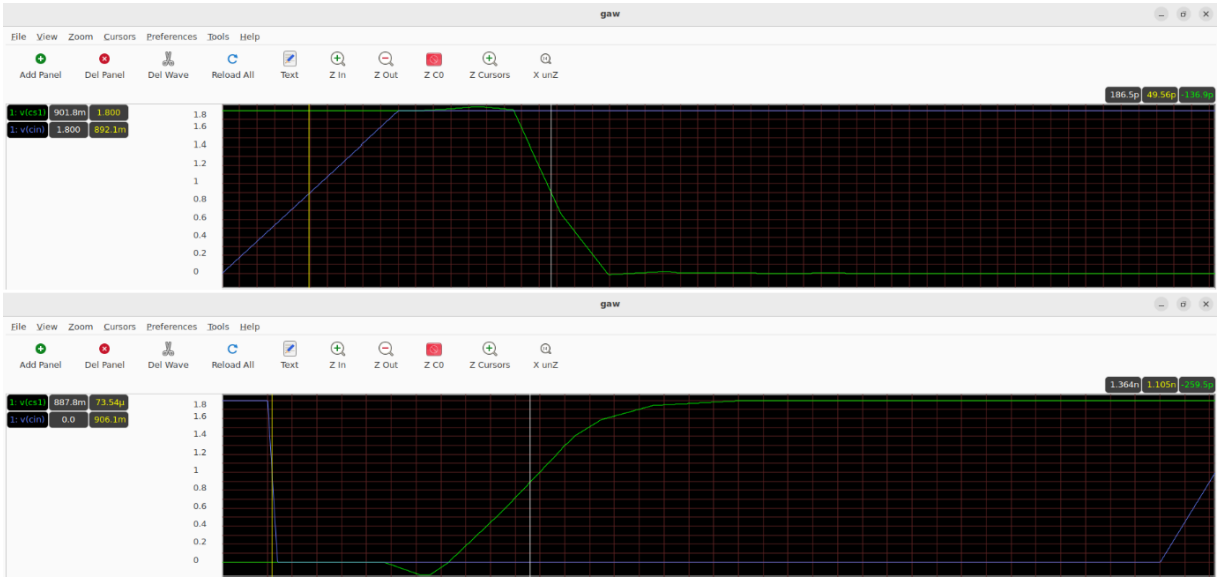


SF corner Temperature (-40)

S0 delay = (26.75+112.2)/2 = 69.475p



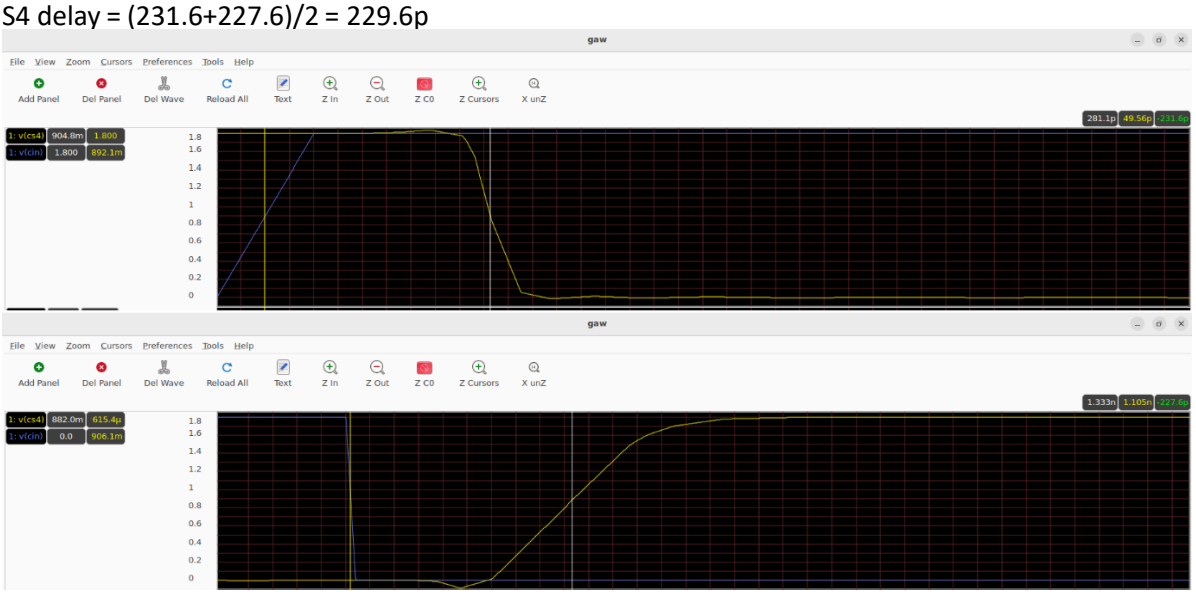
S1 delay = (136.9+259.5)/2 = 198.2p



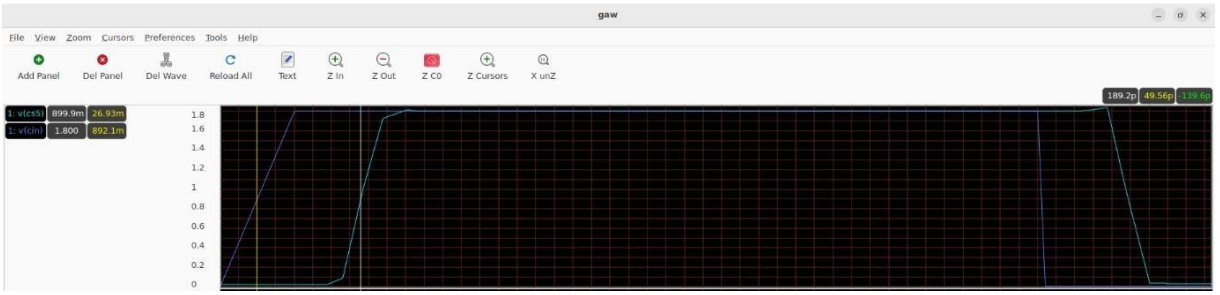
S2 delay = (287.2+363.3)/2 = 325.15

S3 delay = (209+248.5)/3 = 228.75

S4 delay = (231.6+227.6)/2 = 229.6p

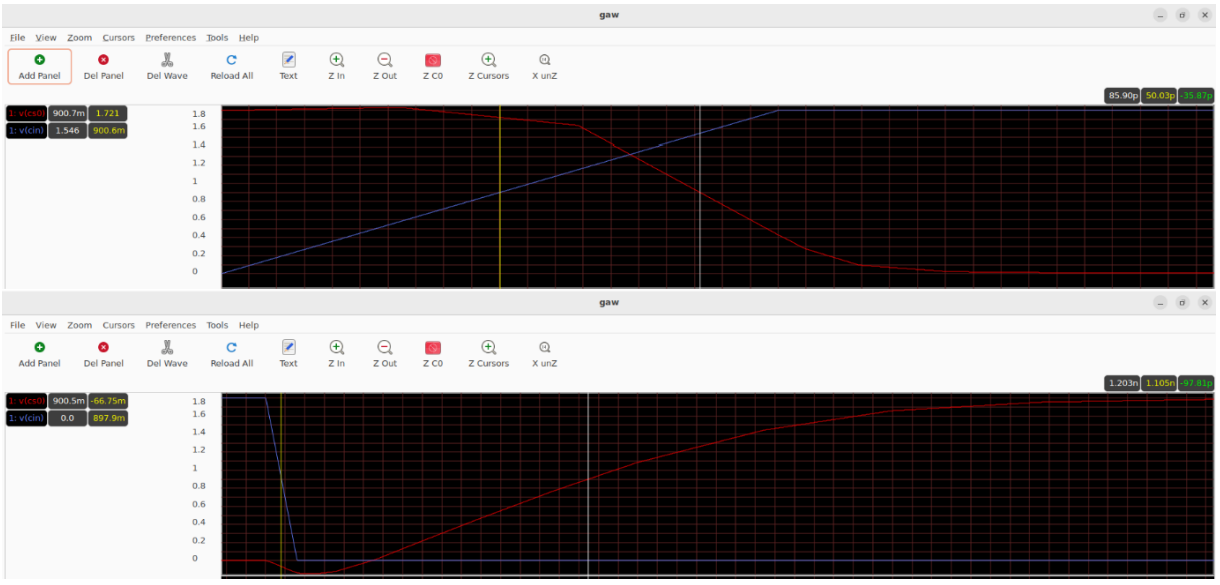


S5 delay = (116+136)/2 = 126p

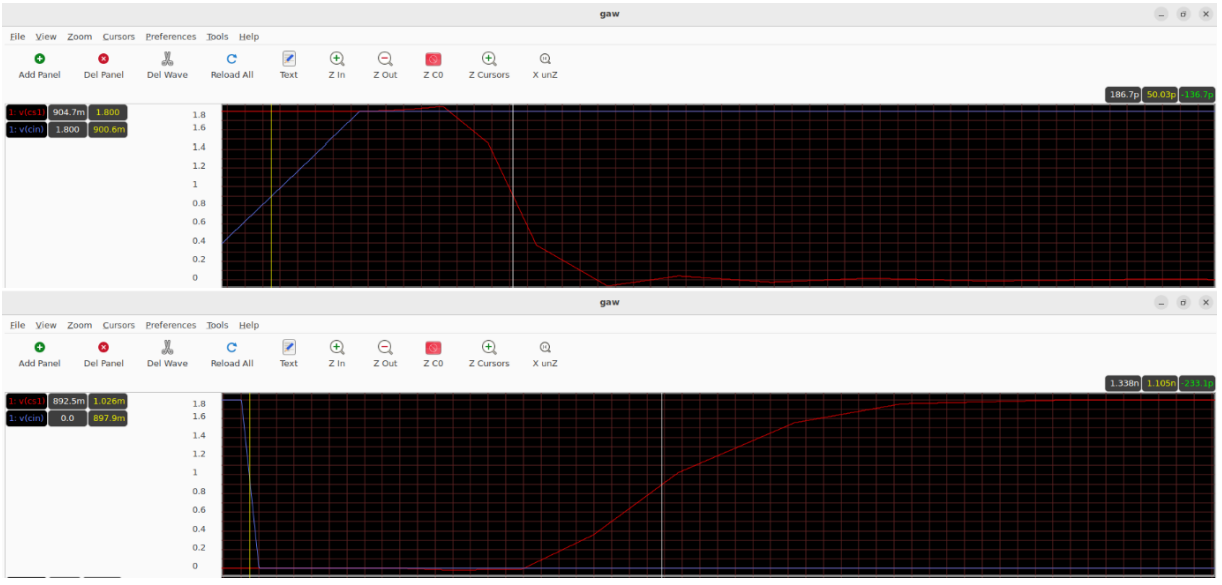


SF corner Temperature (125)

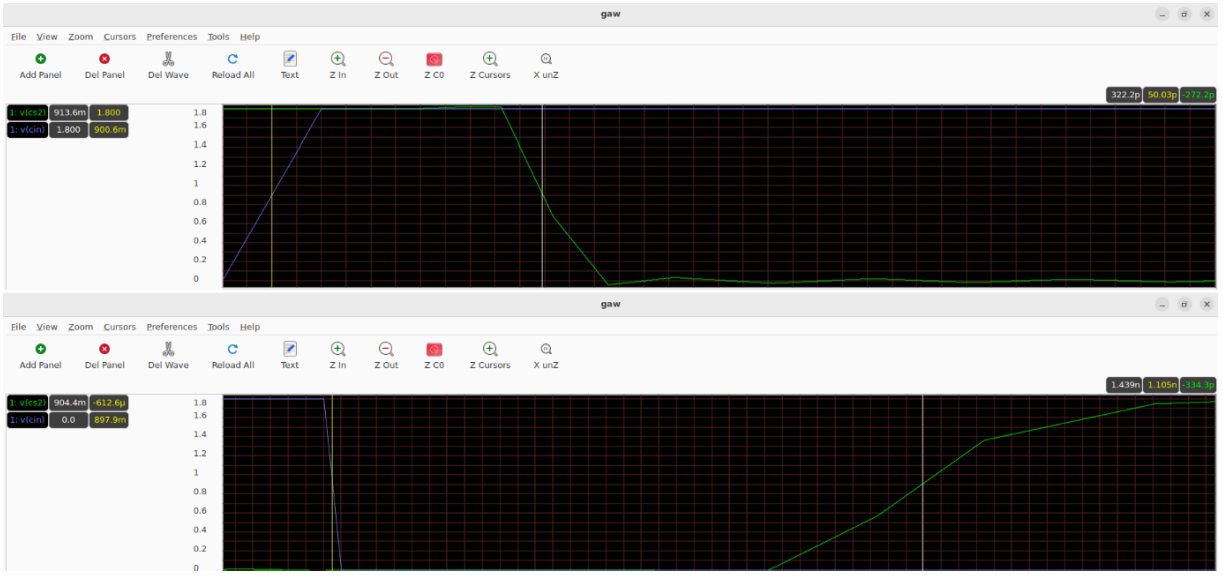
S0 delay = (35.87+97.81)/2 = 66.84p



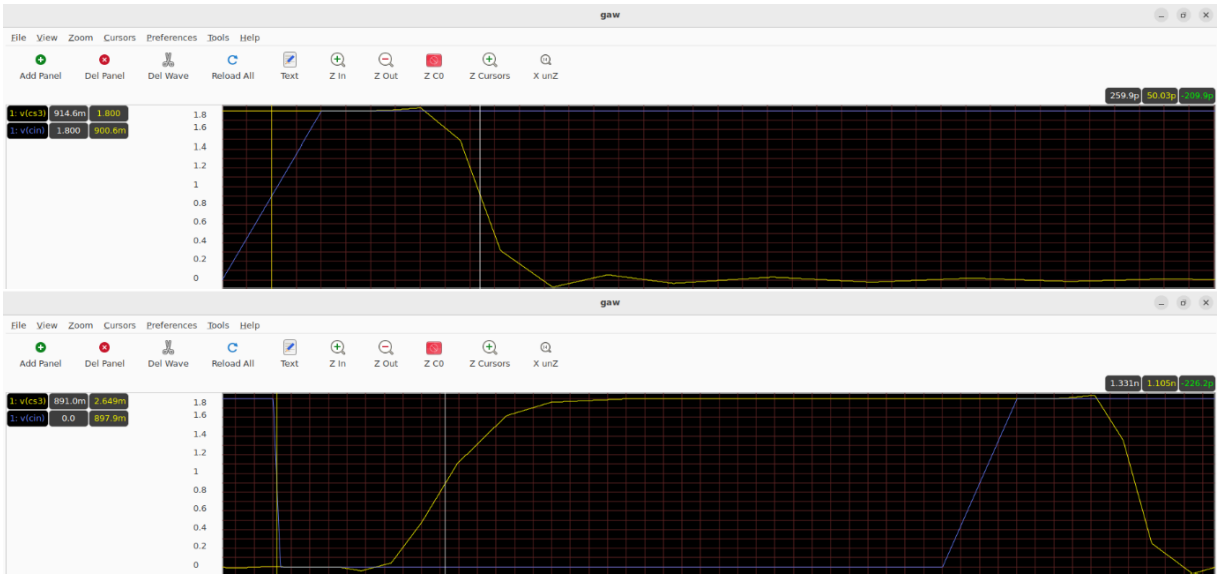
S1 delay = (136.7+233.1)/2 = 184.9p



S2 delay = (272+334)/2 = 303p

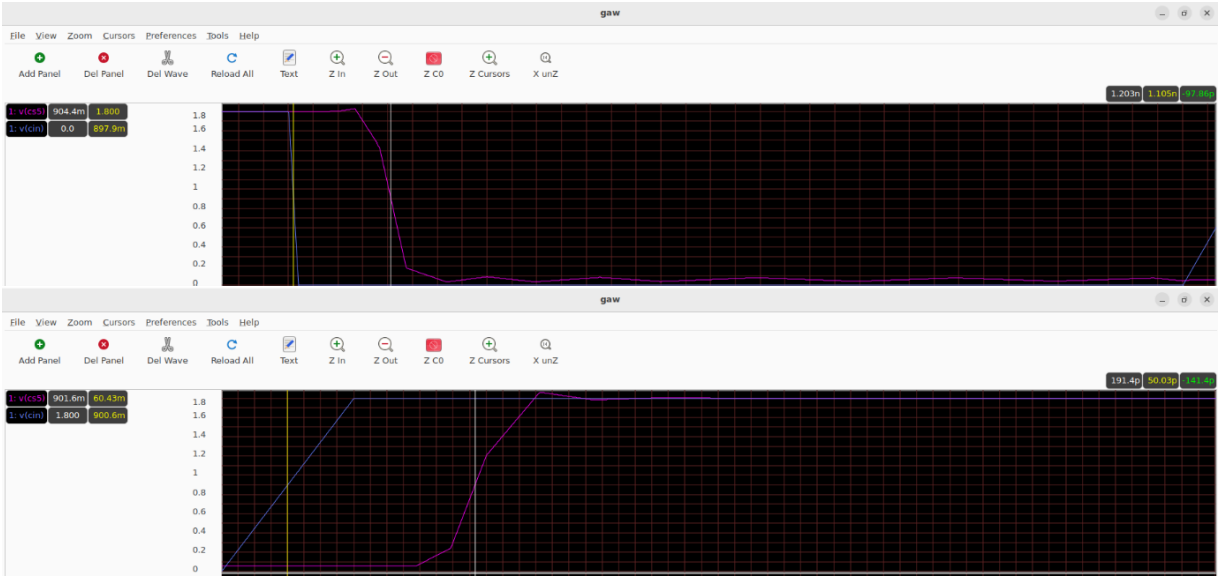


S3 delay = (209+226)/2 = 217.5p



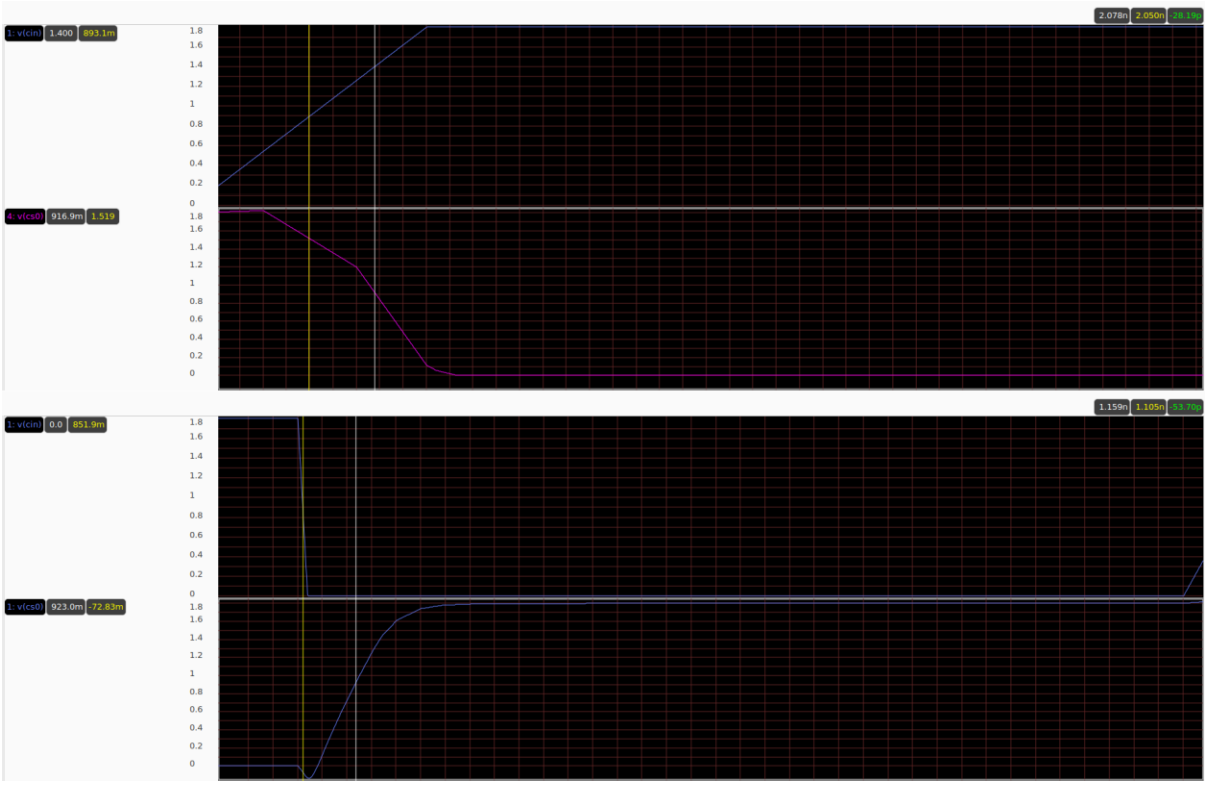
S4 delay = (223+200)/2 = 211.5p

S5 delay = (97.6+ 141.4)/2 = 119.5p

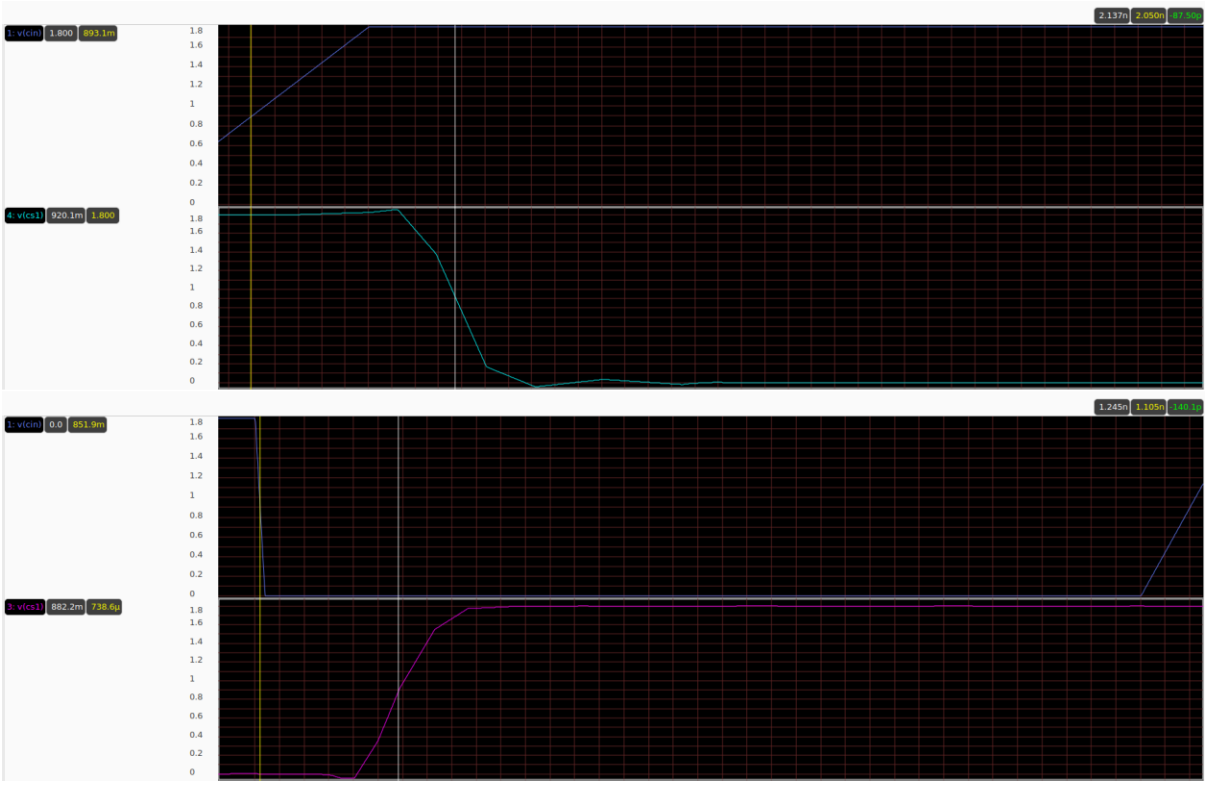


FF corner – Temperature (-40)

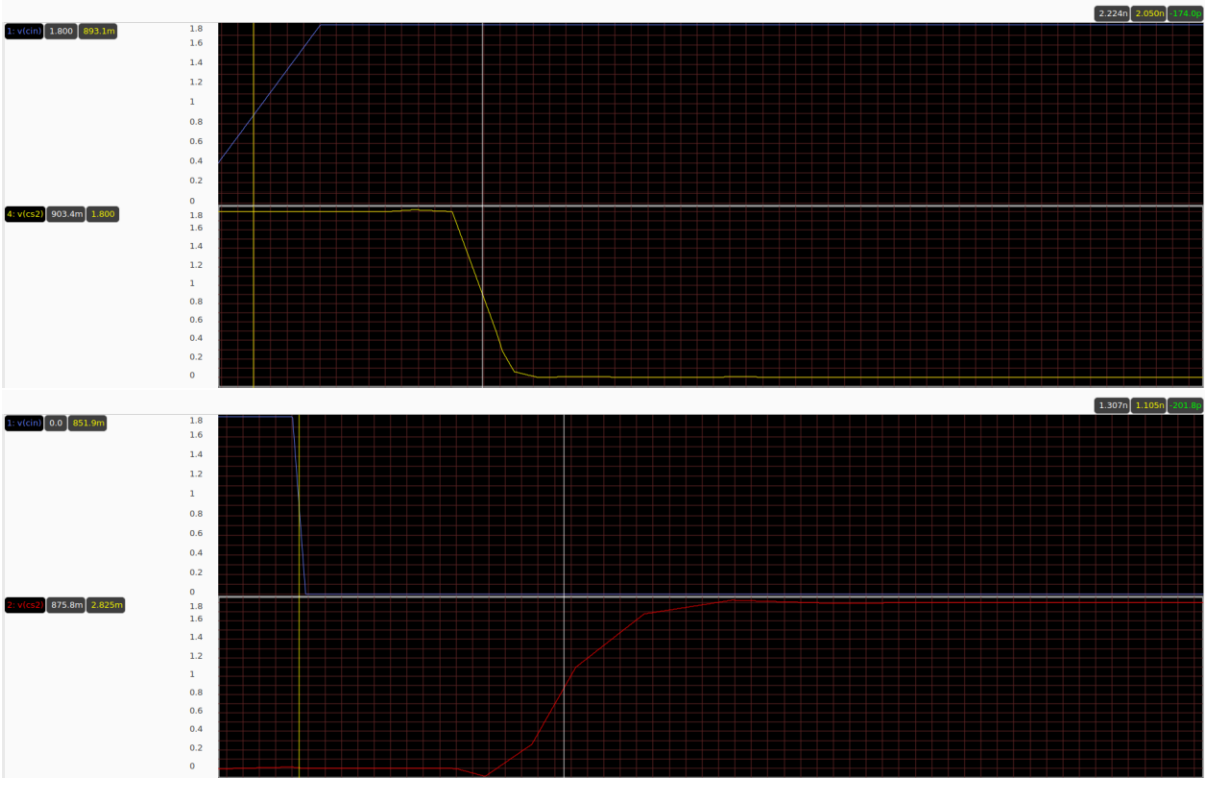
S0 delay = (28.19+53.7)/2 = 40.945p



S1 delay = (87.50+140.1)/2 = 113.8p

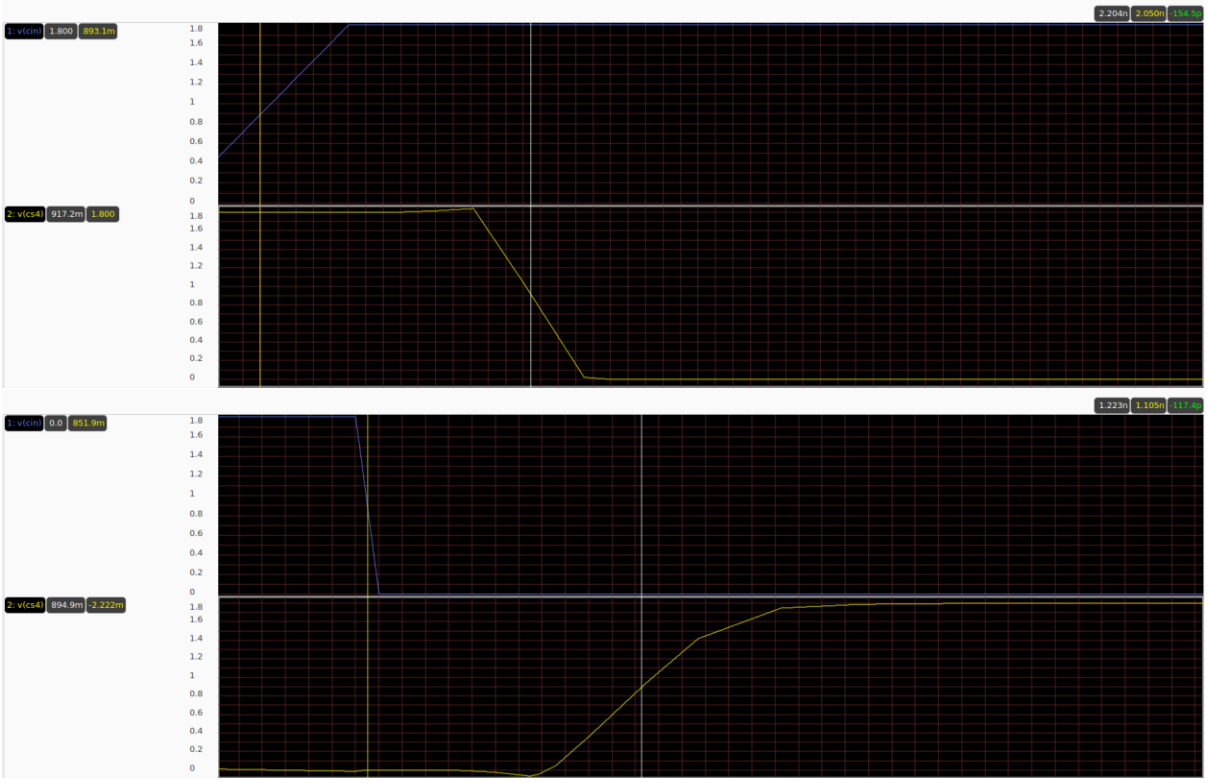


S2 delay = (174+201)/2 = 187.5p

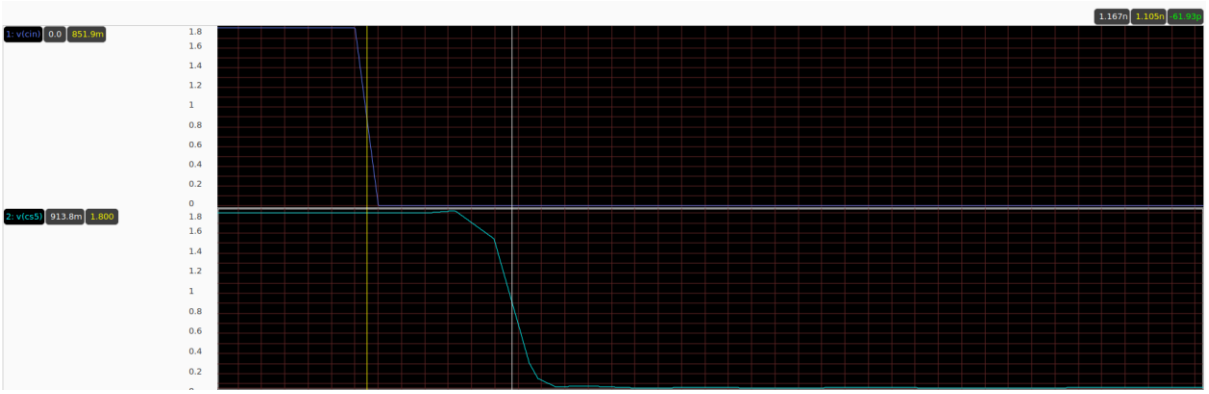


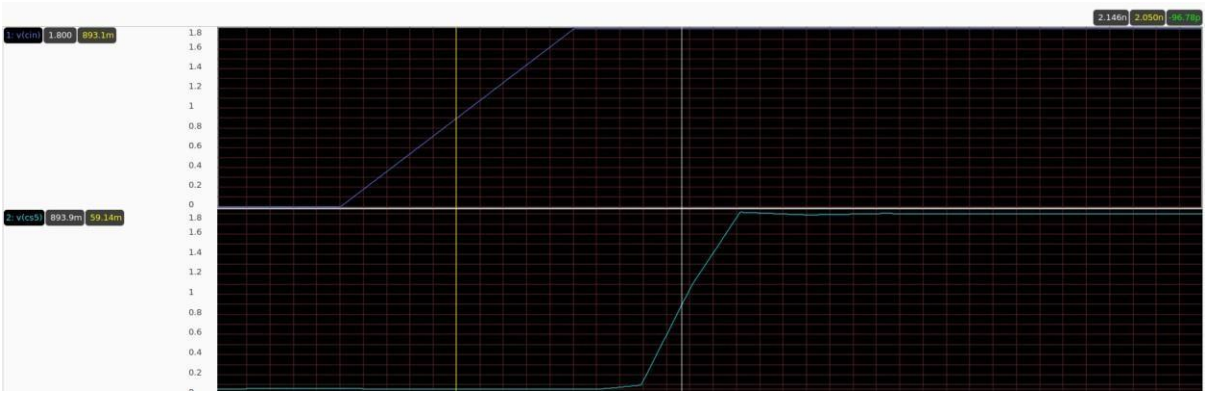
S3 delay = (136.8+138.0)/2 = 137

S4 delay = (154+117.4)/2 = 135.7



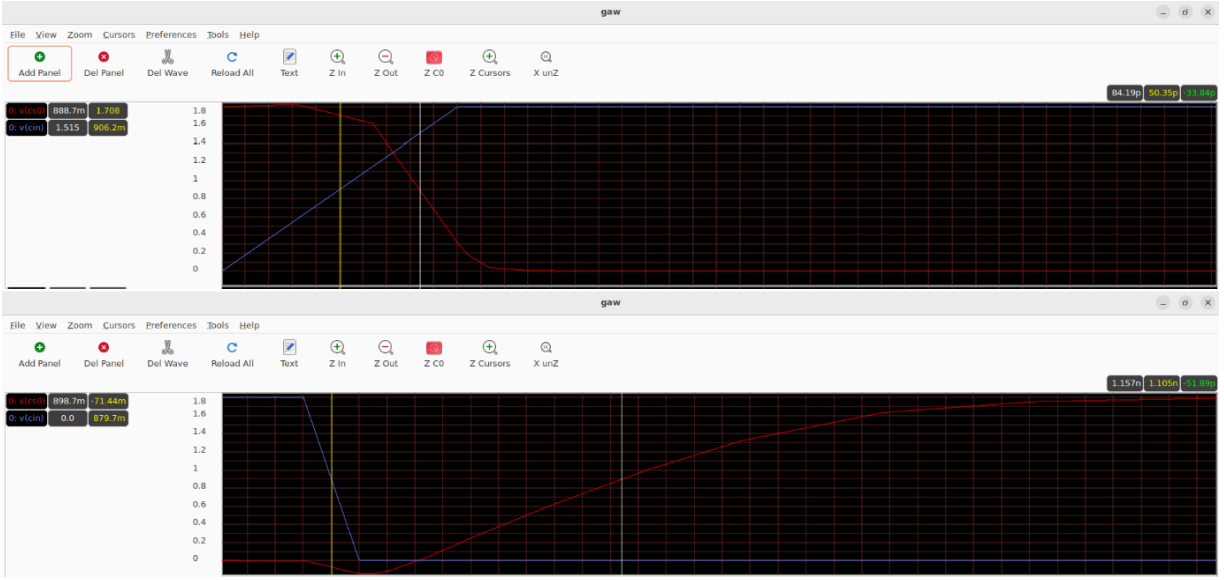
S5 delay = (61.93+96.778)/2 = 79.355p



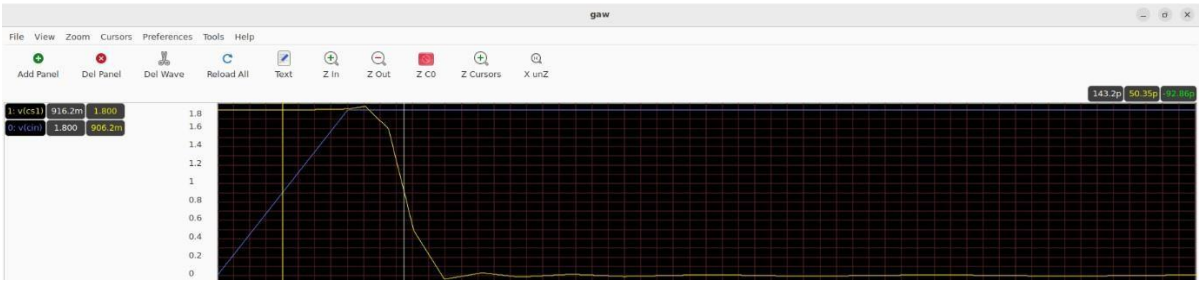


FF corner – Temperature (27)

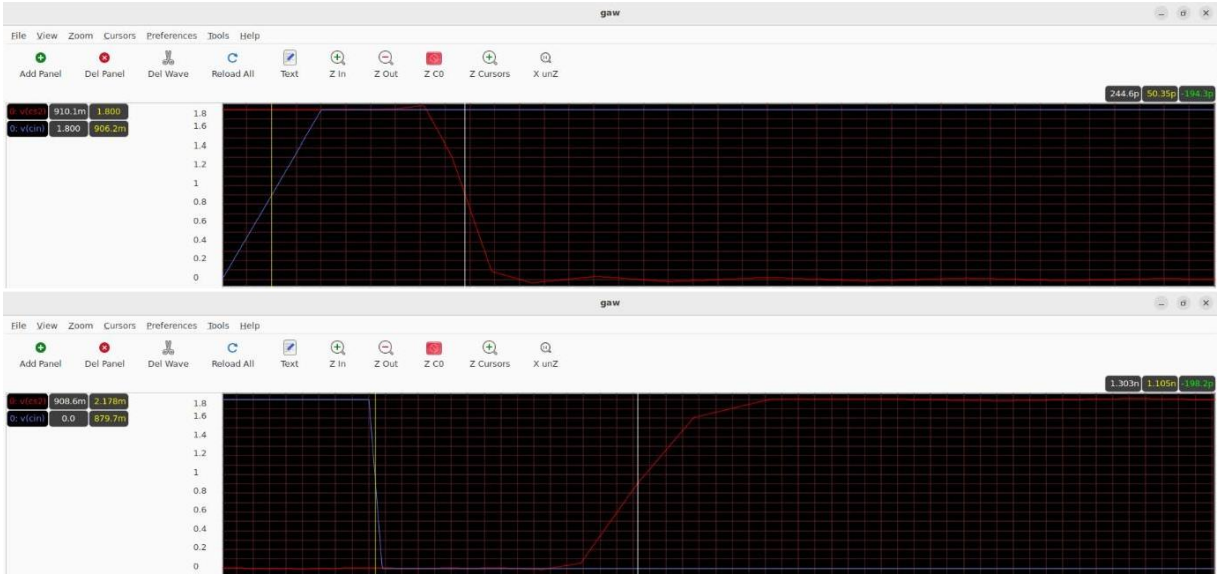
S0 delay = (33.84+ 51.89)/2 = 42.865



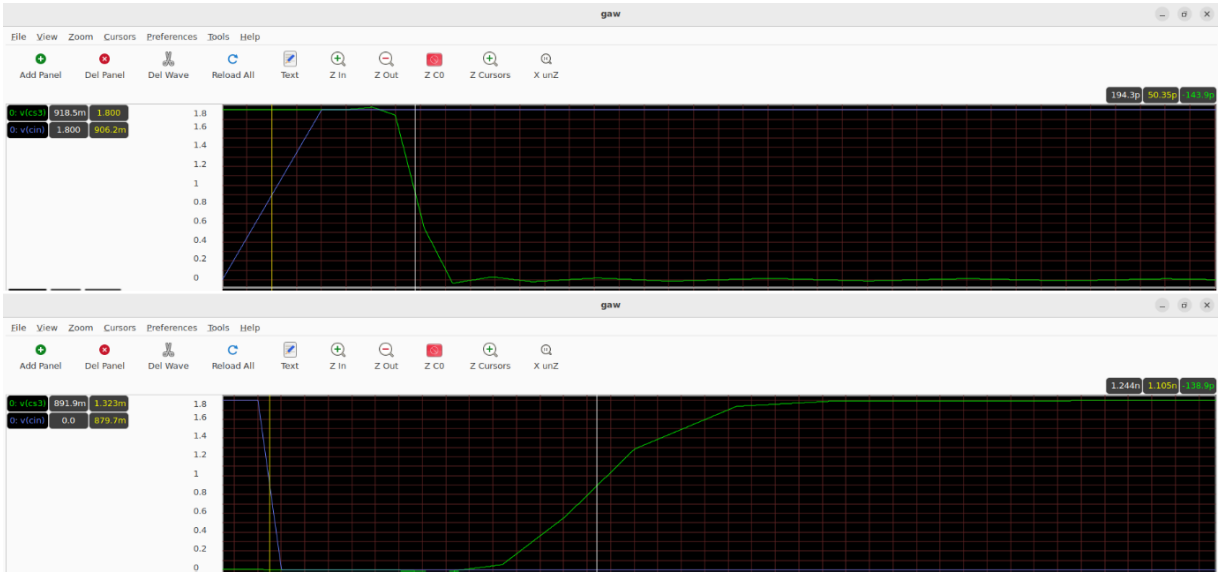
S1 delay = (92.86+142.7)/2 = 117.78



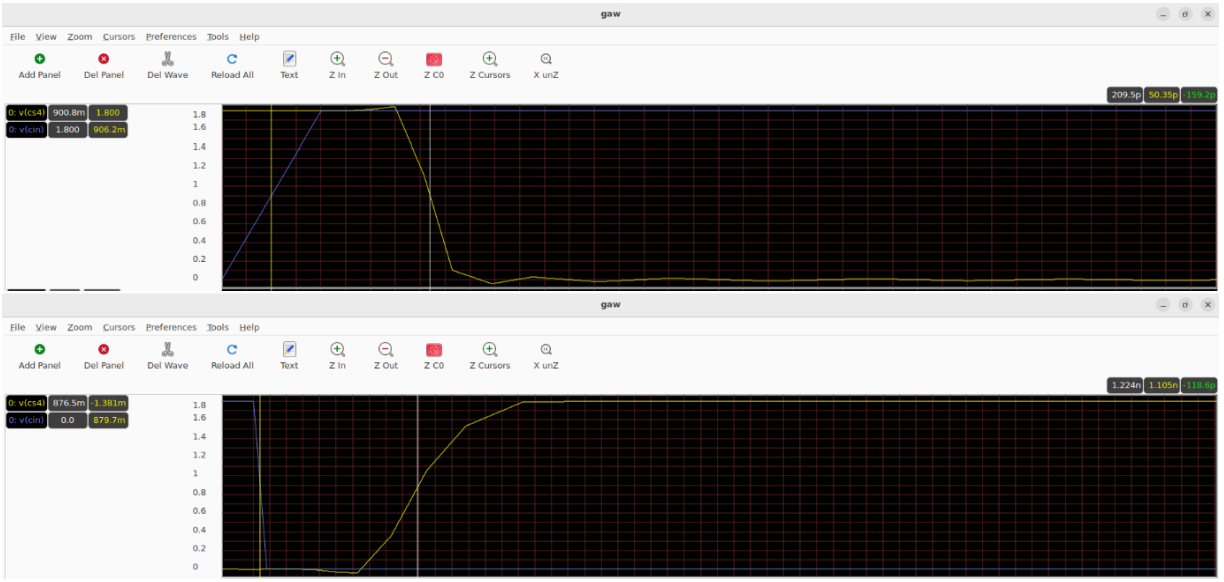
S2 delay = (194.3+ 198.2)/2 = 196.25



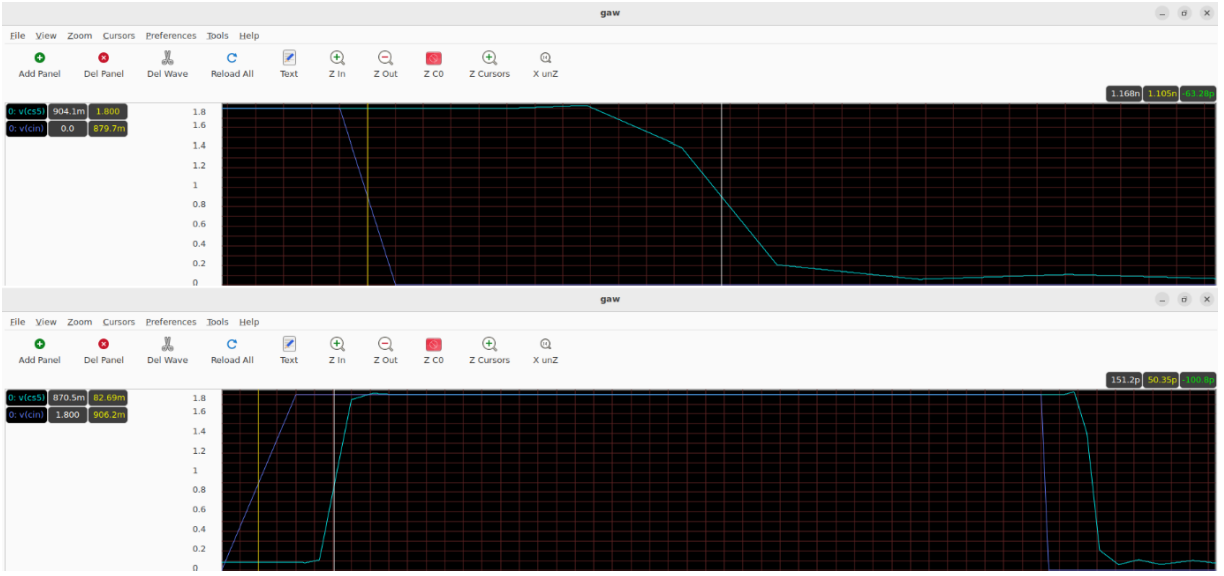
S3 delay= (141.9+ 138.9)/2 = 140.4



S4 delay = (159.2+118.6)/2 = 138.9

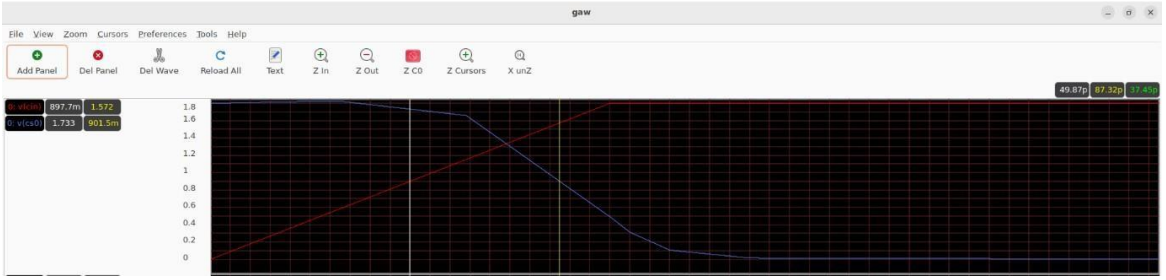


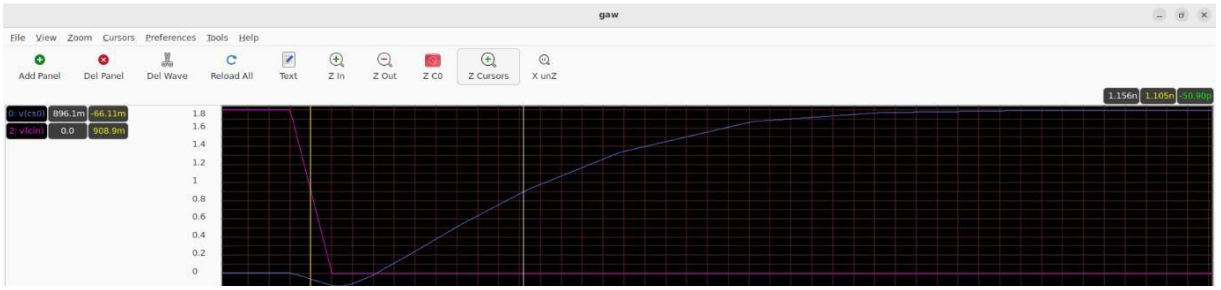
S5 delay = (63.28+ 100.8)/2 = 82.04p



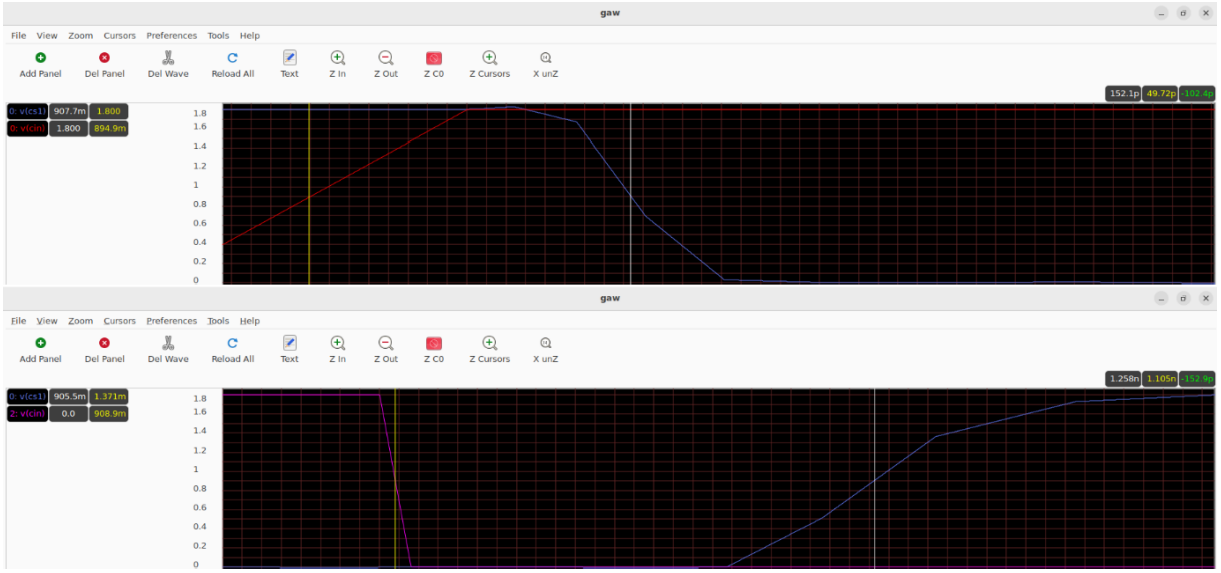
FF corner – Temperature (125)

S0 delay = (37.45+ 50.9)/2 = 44.175p

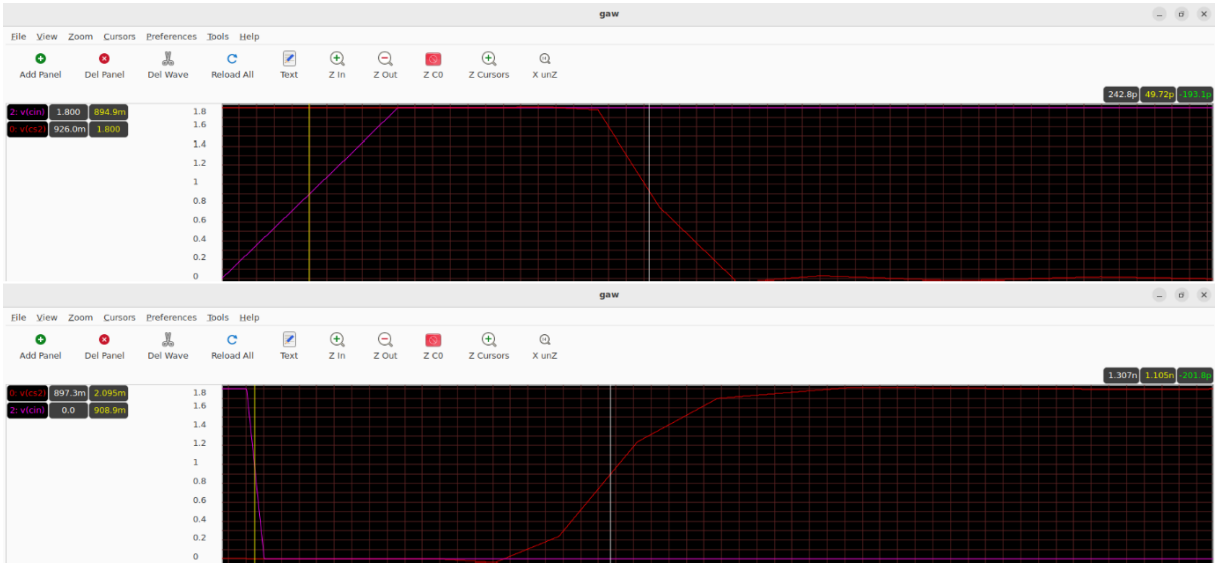




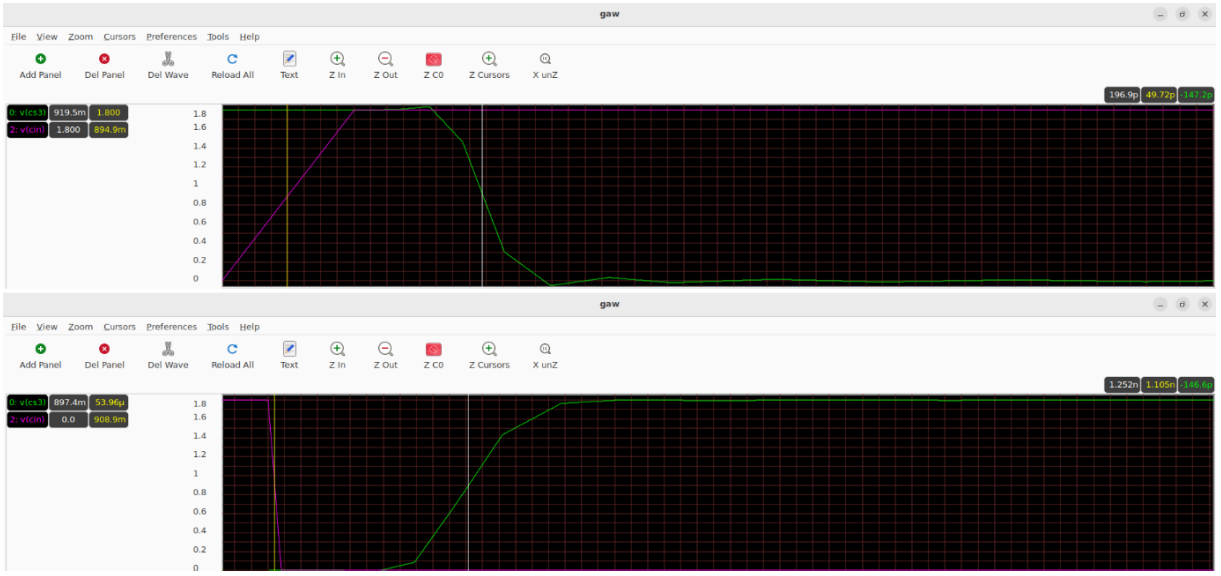
S1 delay = (102.4 + 152.9)/2 = 127.65p



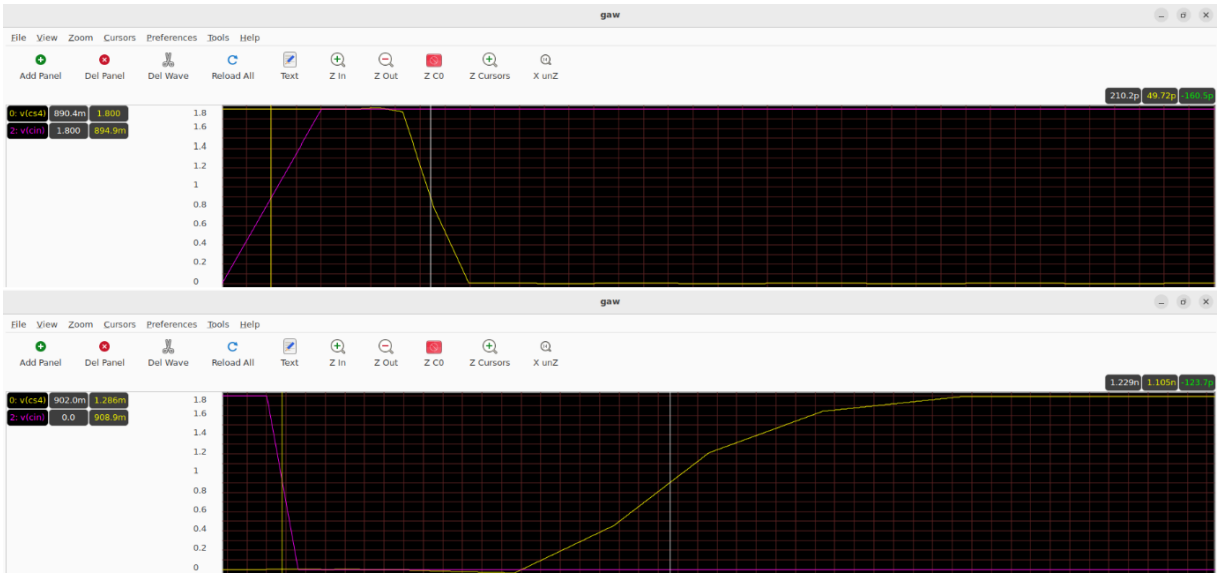
S2 delay = (193.1+201.8)/2 = 197.45



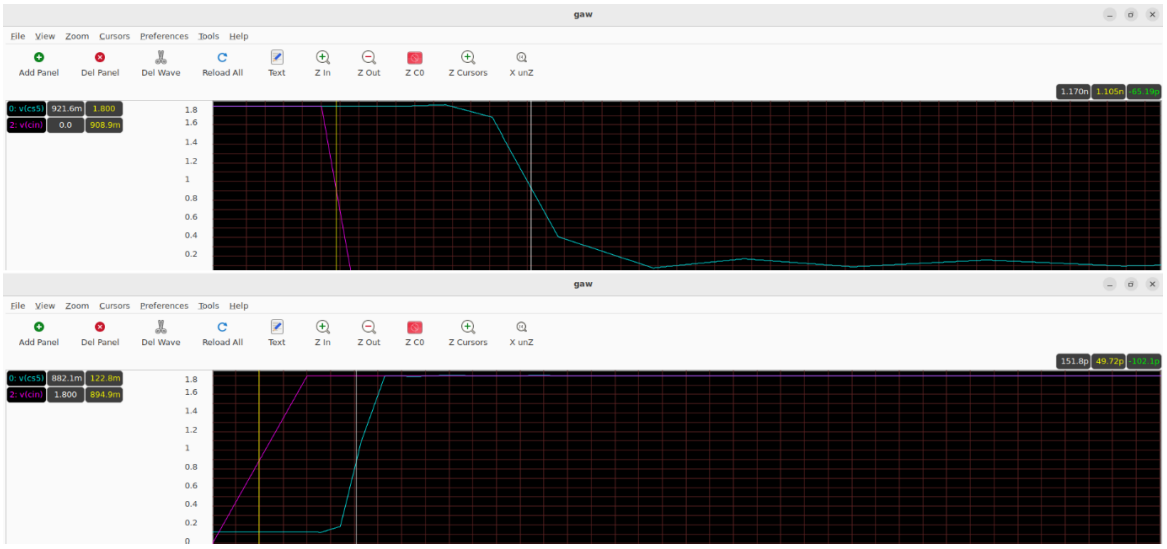
S3 delay = (147.2+146.6)/2 = 147.4



S4 delay = (160.5+123.7)/2 = 142.1p



S5 delay = (65.19+102.1)/2 = 83.645p



TT	-40	27	125
	Delay(ps)	Delay	Delay
S0	56	56	59.5
S1	160	162	166
S2	271	268	270
S3	192	190	192
S4	182	184.5	184.5
S5	107	109	109

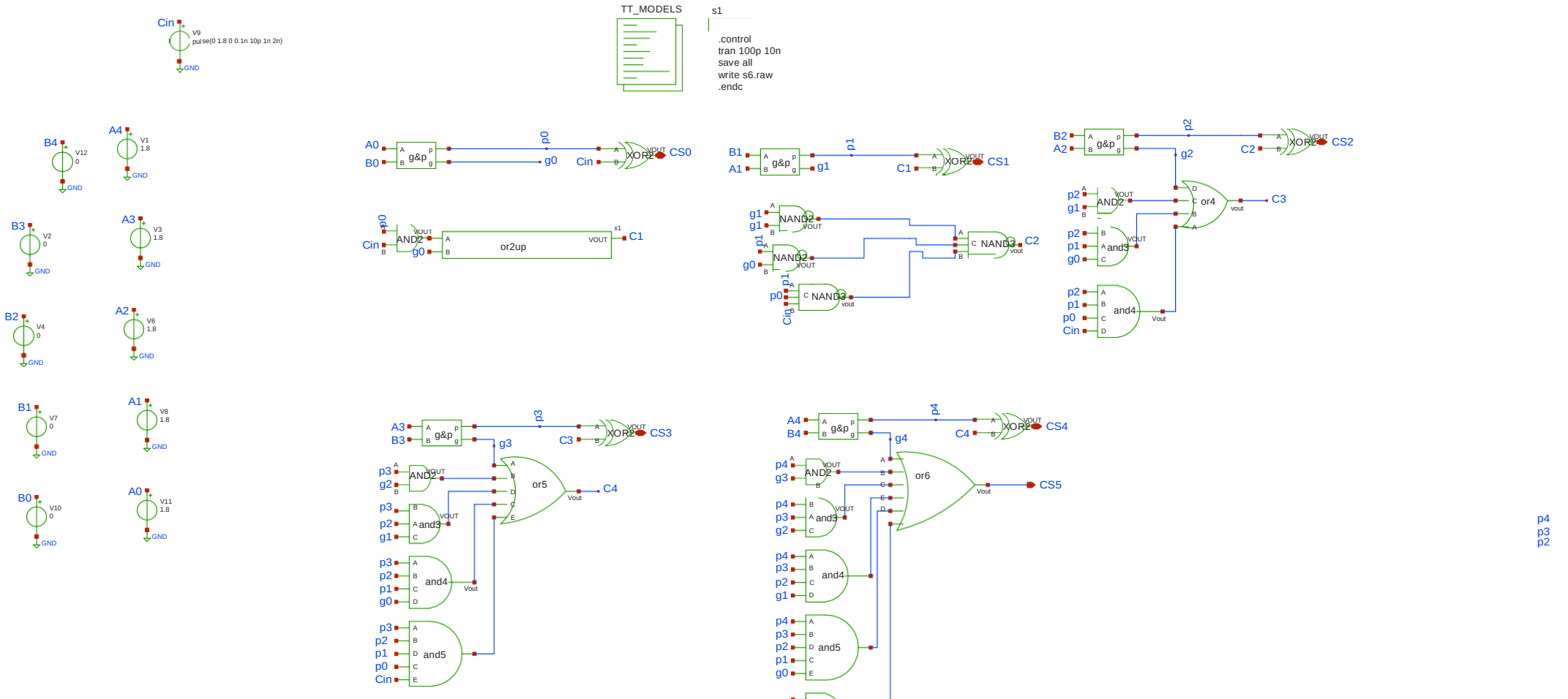
SS	-40	27	125
	Delay(ps)	Delay(ps)	Delay(ps)
S0	87	87.5	83.5
S1	247	240	297
S2	388	396.5	389.5
S3	285	276.5	268
S4	277	272.5	269
S5	164	161	153

SF	-40	27	125
	Delay(ps)	Delay(ps)	Delay(ps)
S0	69.475	69.4	66.84
S1	198.28	195.5	184.9
S2	325.15	322.7	303
S3	228.75	226.95	217.5
S4	229.6	224.2	211.5
S5	126	125	119.5

FS	-40	27	125
	Delay(ps)	Delay(ps)	Delay(ps)
S0	56.5	56.34	60.5
S1	154	155.3	173
S2	252	253.95	254.58
S3	181	182.58	191
S4	170.5	170.5	179.5
S5	106.5	106.825	109.58

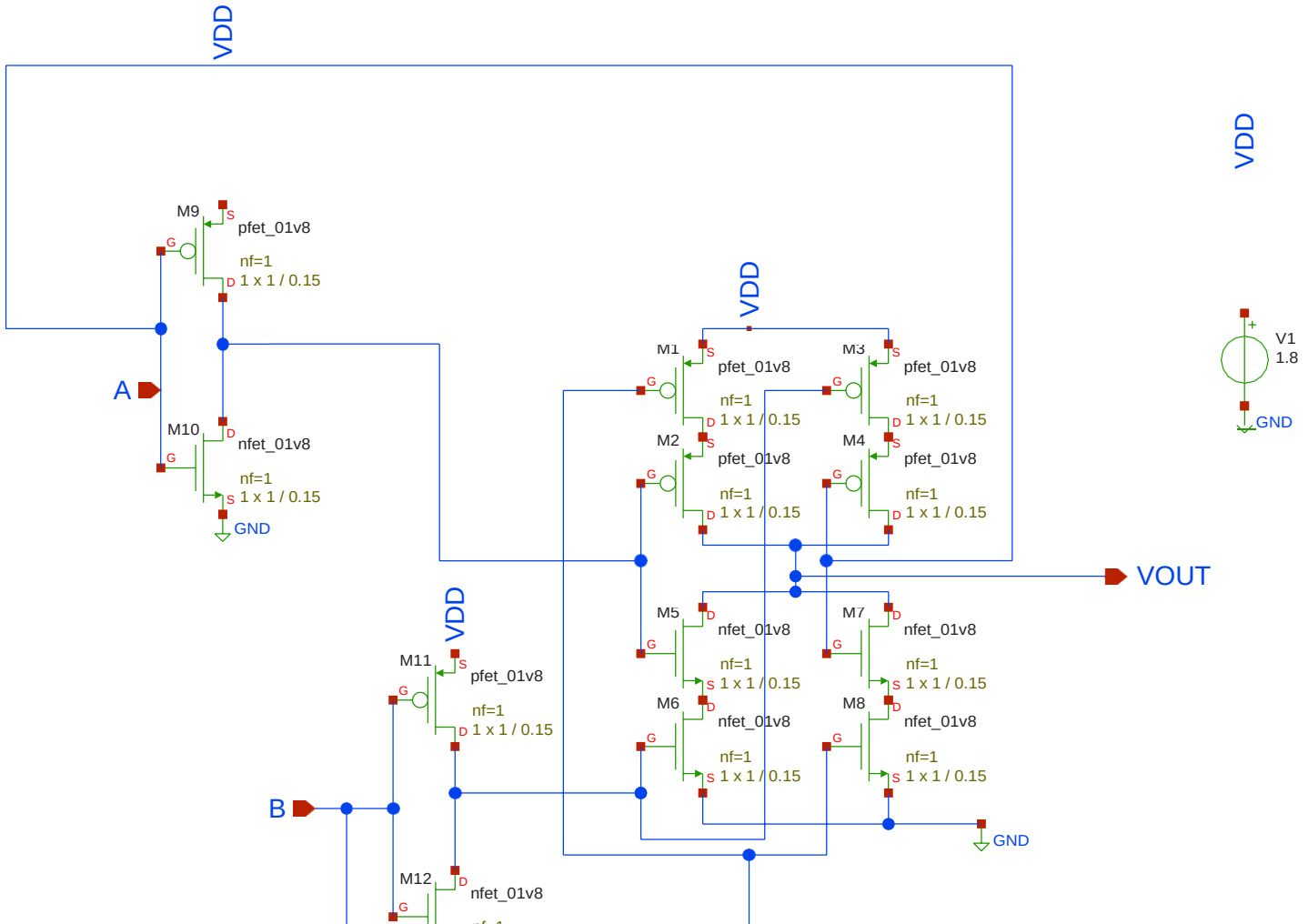
FF MODEL	-40	27	125
	Delay(ps)	Delay(ps)	Delay(ps)
S0	40.945	42.8686	44.17
S1	113.85	117.70	127.65
S2	187.5	196.25	197.45
S3	137	140.4	147.4
S4	135.7	138.9	142.1
S5	79.35	82.4	83.64

s0.sch

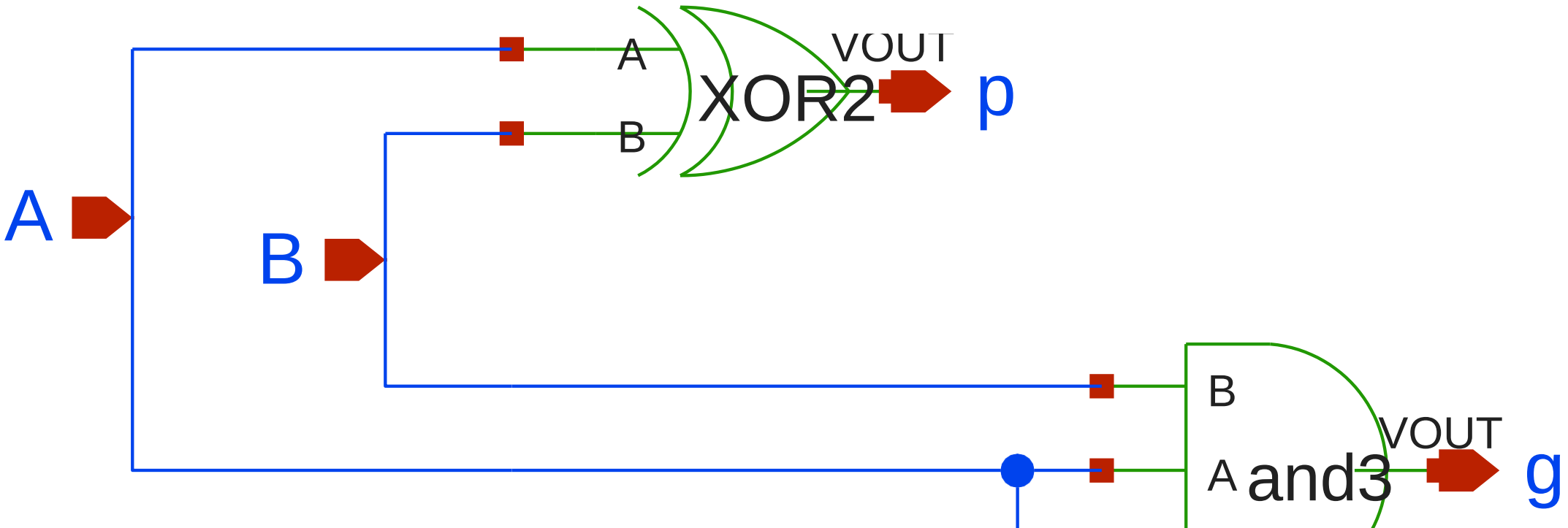

Cin
V9
pulse(0 1.8 0 0.1n 10p 1n 2n)
GND
TT_MODELS
s1
.control
tran 100p 10n
save all
write s6.raw
.endc
B4
A4
B3
A3
B2
A2
B1
A1
B0
A0
V12
V1
V2
V3
V4
V6
V7
V8
V10
V11
0
1.8
g&p
XOR2
CS0
CS1
CS2
CS3
CS4
CS5
AND2
NAND2
NAND3
and3
and4
and5
or2up
or4
or5
or6
C1
C2
C3
C4
Vout
vout
VOUT


F
Vout
Vout
p1
p0
Cin
D
E
F
and6

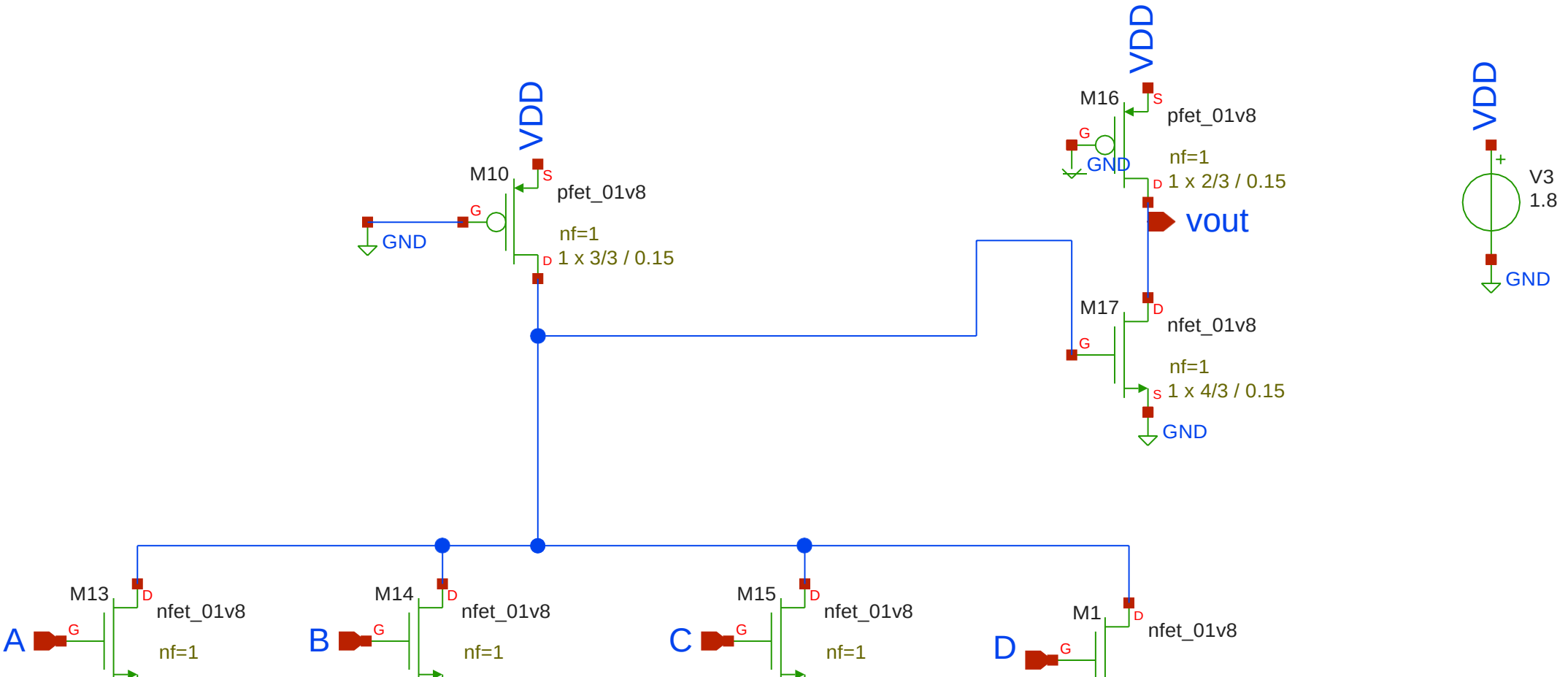
xor2.sch


VDD
VDD
VDD
VDD
M9
pfet_01v8
nf=1
1 x 1 / 0.15
A
M10
nfet_01v8
nf=1
1 x 1 / 0.15
GND
M1
pfet_01v8
nf=1
1 x 1 / 0.15
M3
pfet_01v8
nf=1
1 x 1 / 0.15
M2
pfet_01v8
nf=1
1 x 1 / 0.15
M4
pfet_01v8
nf=1
1 x 1 / 0.15
V1
1.8
GND
VOUT
M5
nfet_01v8
nf=1
1 x 1 / 0.15
M7
nfet_01v8
nf=1
1 x 1 / 0.15
M6
nfet_01v8
nf=1
1 x 1 / 0.15
M8
nfet_01v8
nf=1
1 x 1 / 0.15
GND
M11
pfet_01v8
nf=1
1 x 1 / 0.15
B
M12
nfet_01v8

g&p.sch



or4.sch


VDD
M10
pfet_01v8
G
S
D
GND
nf=1
1 x 3/3 / 0.15
VDD
M16
pfet_01v8
G
S
D
GND
nf=1
1 x 2/3 / 0.15
vout
VDD
V3
1.8
GND
M17
nfet_01v8
G
D
S
nf=1
1 x 4/3 / 0.15
GND
A
M13
nfet_01v8
G
D
nf=1
B
M14
nfet_01v8
G
D
nf=1
C
M15
nfet_01v8
G
D
nf=1
D
M1
nfet_01v8
G
D

s 1 x 4/3 / 0.15

GND

s 1 x 4/3 / 0.15

__GND

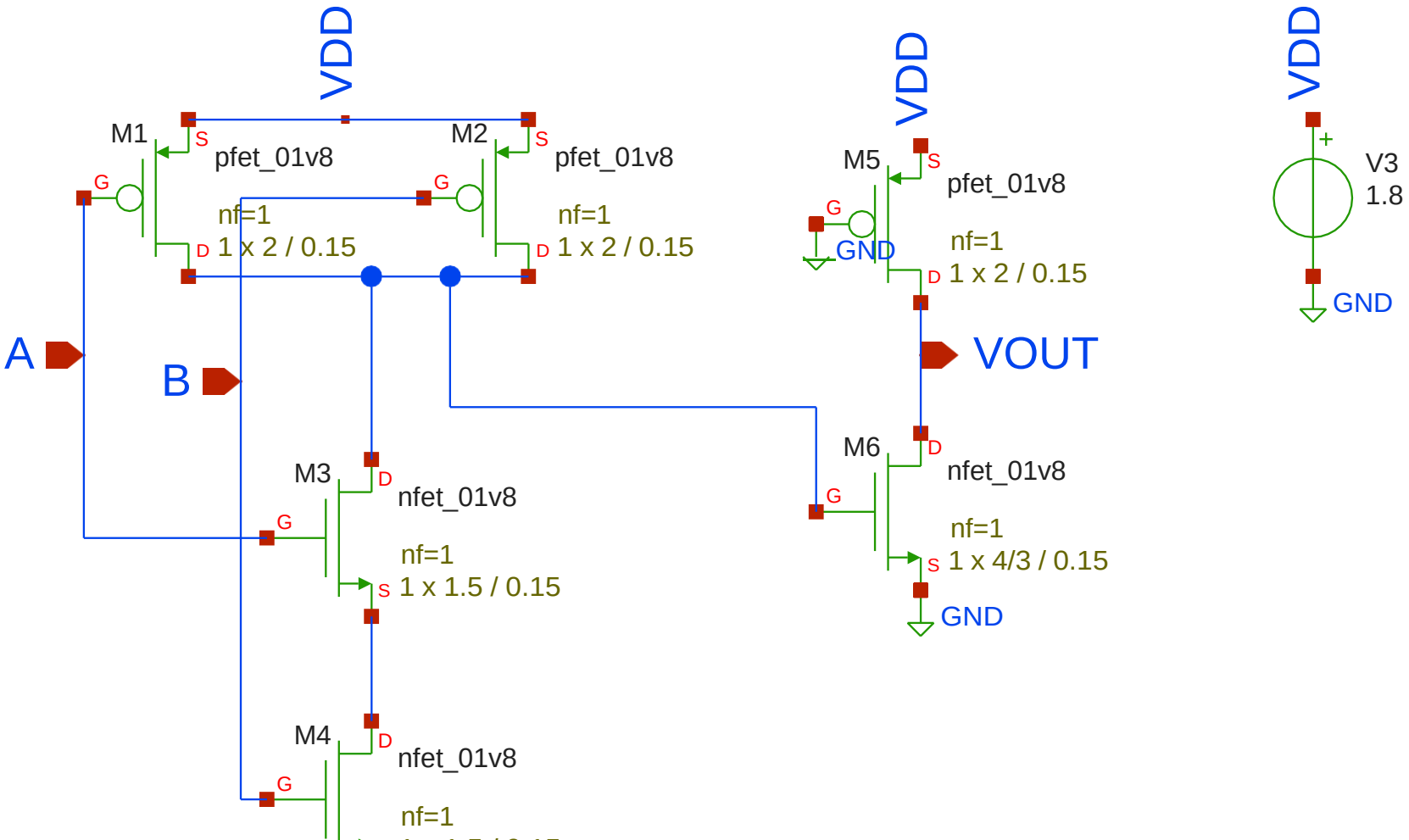
s 1 x 4/3 / 0.15

__GND

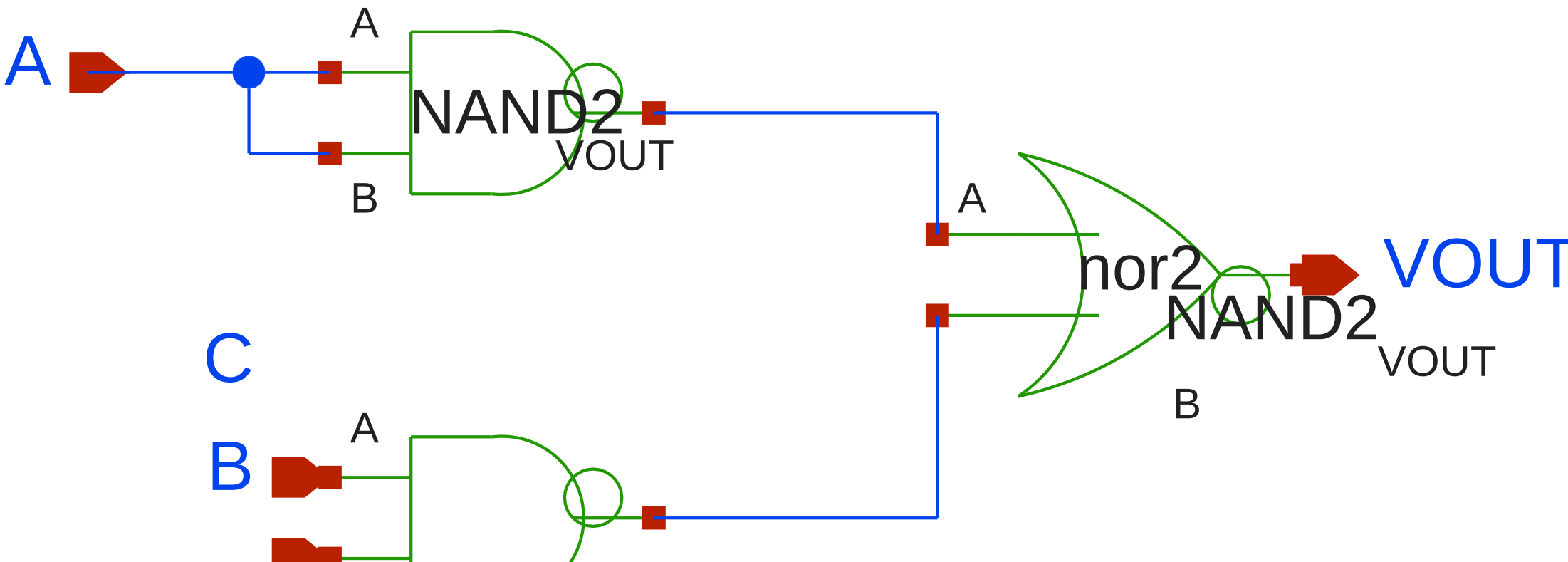
nf=1
s 1 x 4/3 / 0.15

GND

and.sch


VDD
M1
S
pfet_01v8
G
nf=1
D
1 x 2 / 0.15
M2
S
pfet_01v8
G
nf=1
D
1 x 2 / 0.15
A
B
M3
D
nfet_01v8
G
nf=1
S
1 x 1.5 / 0.15
M4
D
nfet_01v8
G
nf=1
VDD
M5
S
pfet_01v8
G
GND
nf=1
D
1 x 2 / 0.15
VOUT
M6
D
nfet_01v8
G
nf=1
S
1 x 4/3 / 0.15
GND
VDD
+
V3
1.8
GND

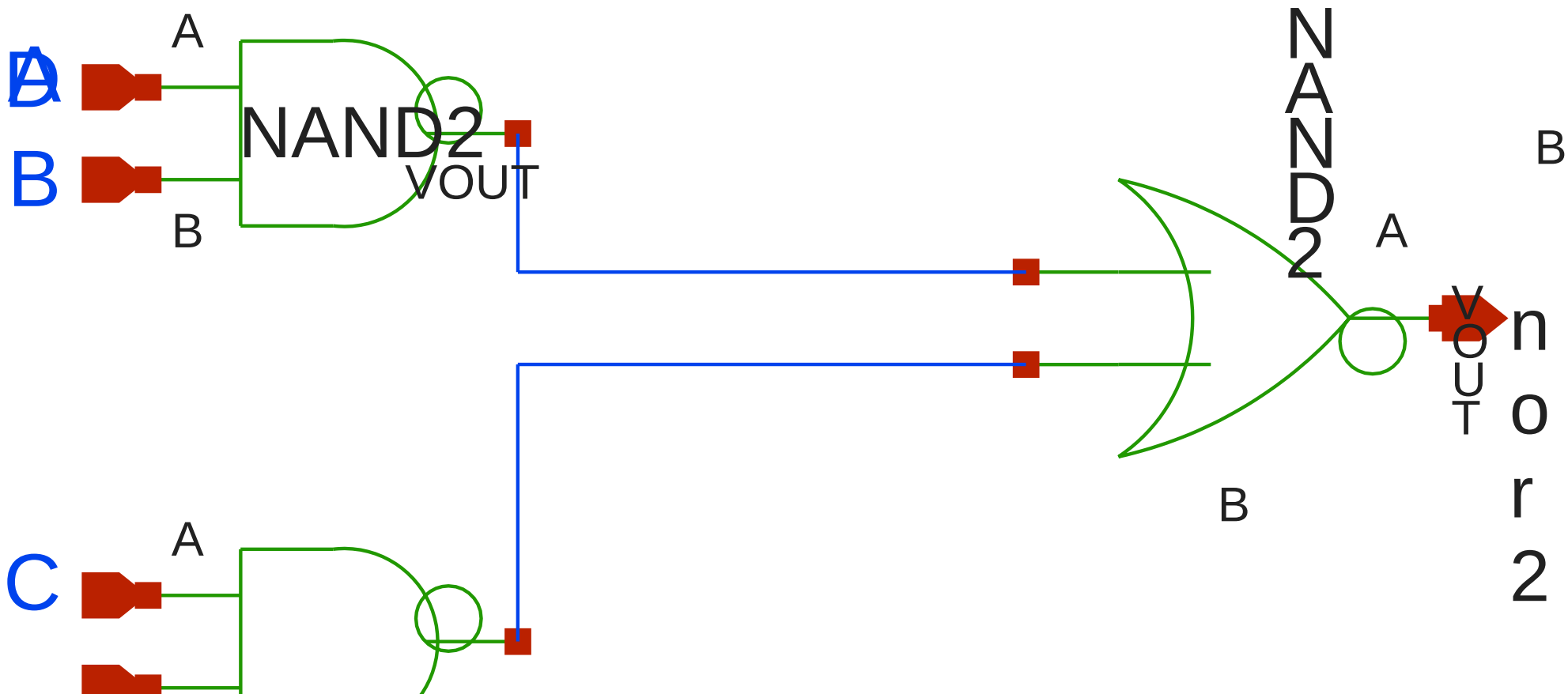
and3.sch



VOUT

B

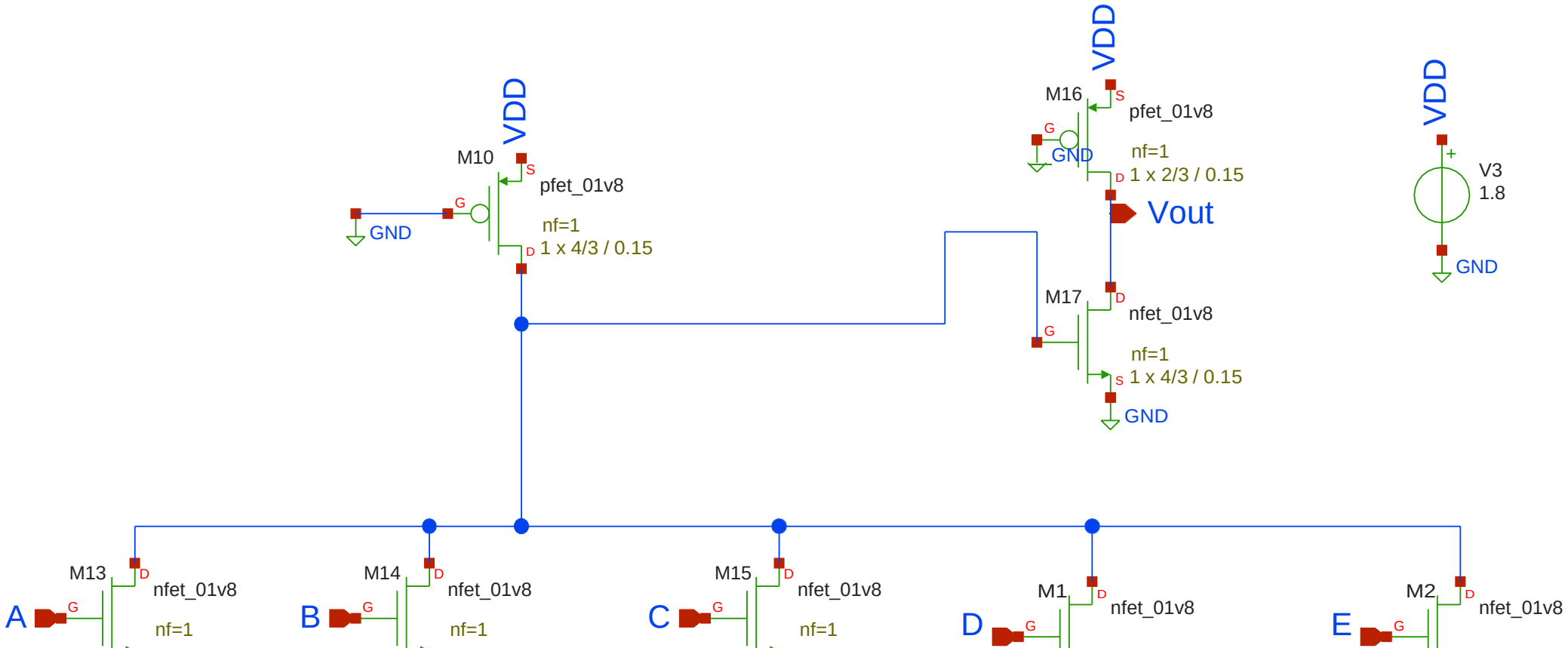
and4.sch



Vout

VOUT

or5.sch


VDD
M10
pfet_01v8
G
GND
nf=1
D
1 x 4/3 / 0.15
VDD
M16
S
pfet_01v8
G
GND
nf=1
D
1 x 2/3 / 0.15
Vout
VDD
V3
1.8
GND
M17
D
nfet_01v8
G
nf=1
S
1 x 4/3 / 0.15
GND
M13
D
nfet_01v8
A
G
nf=1
M14
D
nfet_01v8
B
G
nf=1
M15
D
nfet_01v8
C
G
nf=1
M1
D
nfet_01v8
D
G
M2
D
nfet_01v8
E
G

s 1 x 4/3 / 0.15

GND

s 1 x 4/3 / 0.15

__GND

s 1 x 4/3 / 0.15

__GND

nf=1

s 1 x 4/3 / 0.15

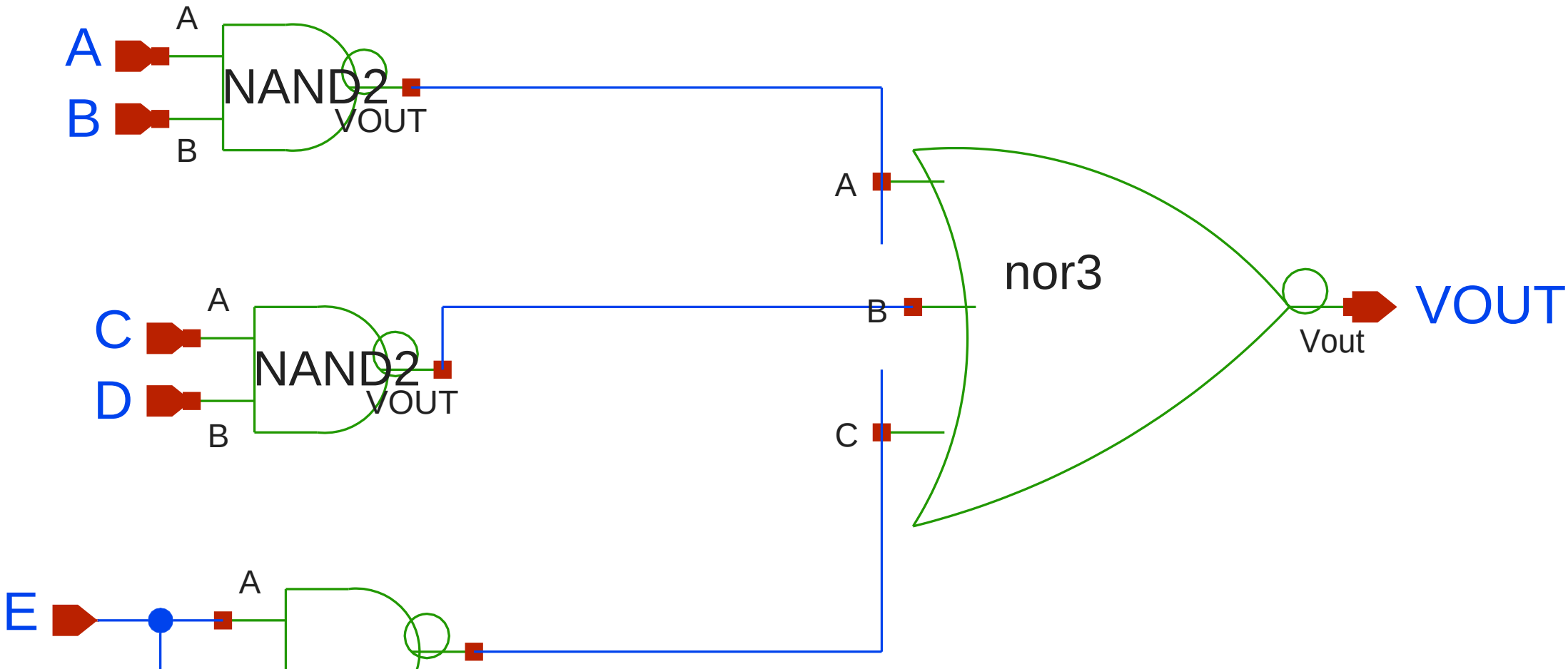
GND

nf=1

s 1 x 4/3 / 0.15

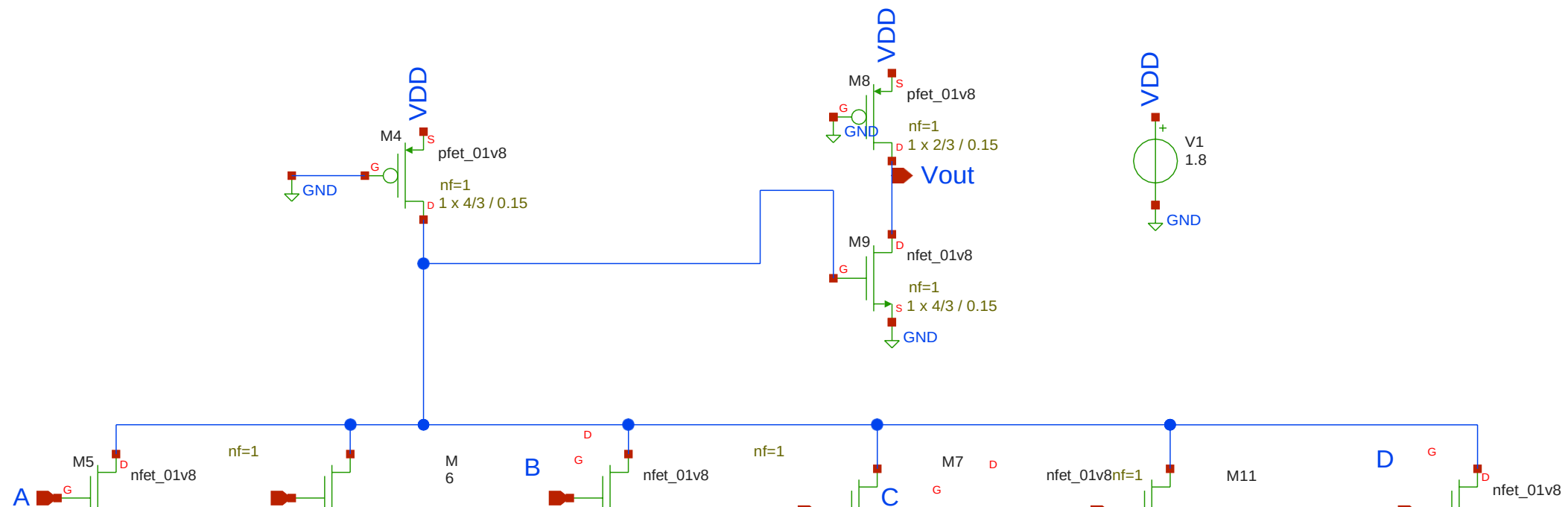
__GND

and5.sch



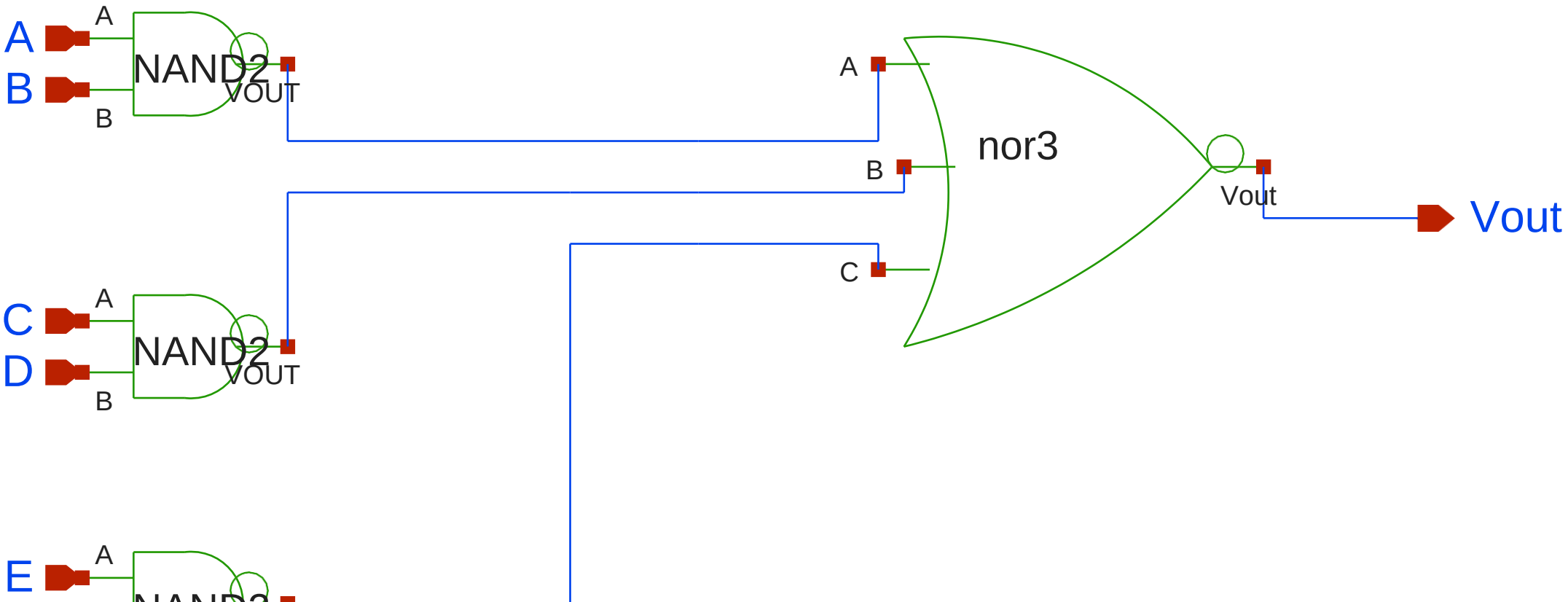

NAND2
VOUT
B

or6.sch


VDD
M4
pfet_01v8
G
GND
nf=1
D
1 x 4/3 / 0.15
VDD
M8
S
pfet_01v8
G
GND
nf=1
D
1 x 2/3 / 0.15
Vout
VDD
V1
1.8
GND
M9
D
nfet_01v8
G
nf=1
S
1 x 4/3 / 0.15
GND
M5
D
nfet_01v8
A
G
nf=1
M
6
D
B
G
nfet_01v8
nf=1
M7
D
C
G
nfet_01v8nf=1
M11
D
G
D
nfet_01v8

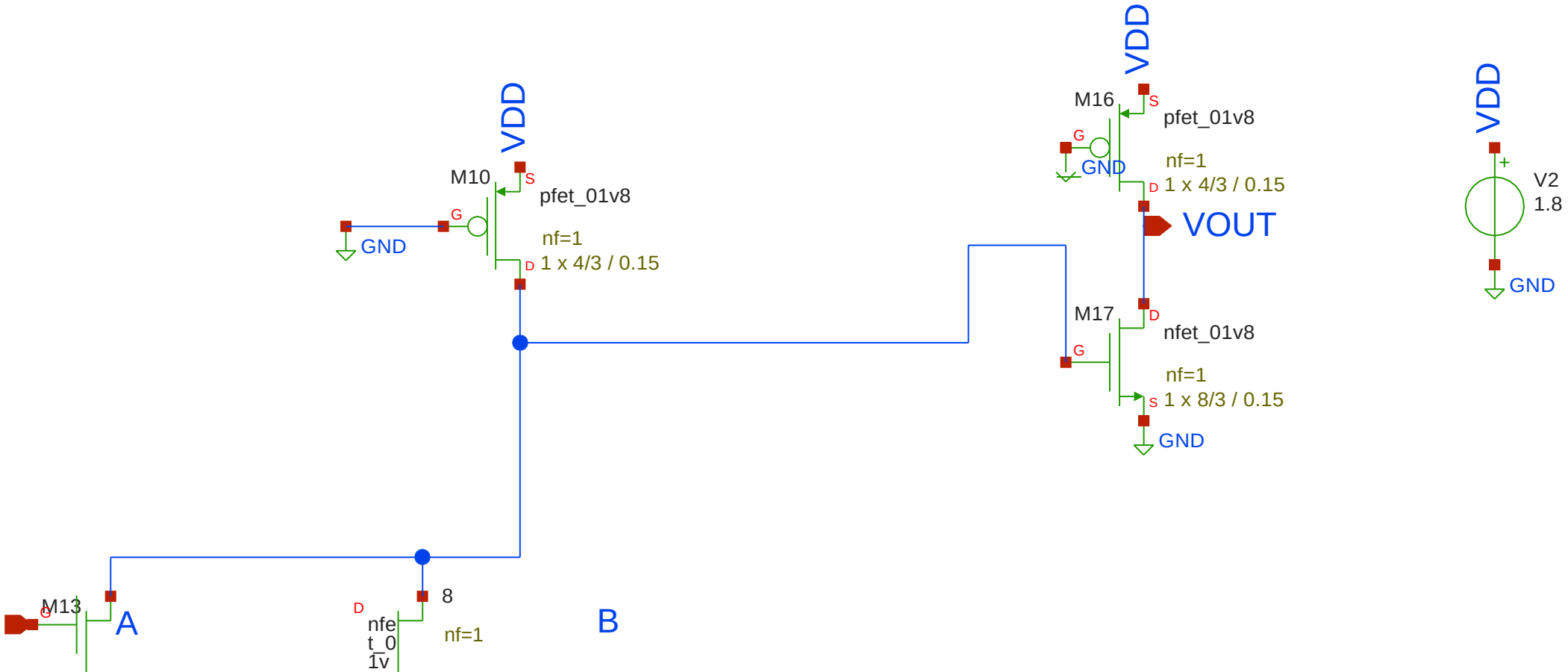

M12
D
nfet_
01v8
E
G
S 1 x 4/3 / 0.15
GND
M18
D
nfet_
01v8
F
G
S 1 x 4/3 / 0.15
GND
S 1 x 4/3 / 0.15
GND
nf=1
S 1 x 4/3 / 0.15
GND
nf=1
S 1 x 4/3 / 0.15
GND
nf=1
S 1 x 4/3 / 0.15
GND

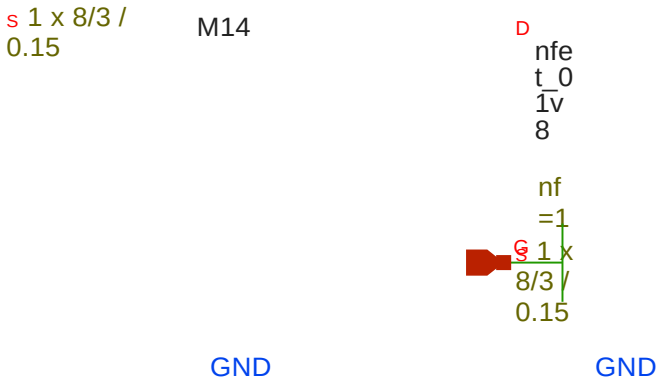
and6.sch



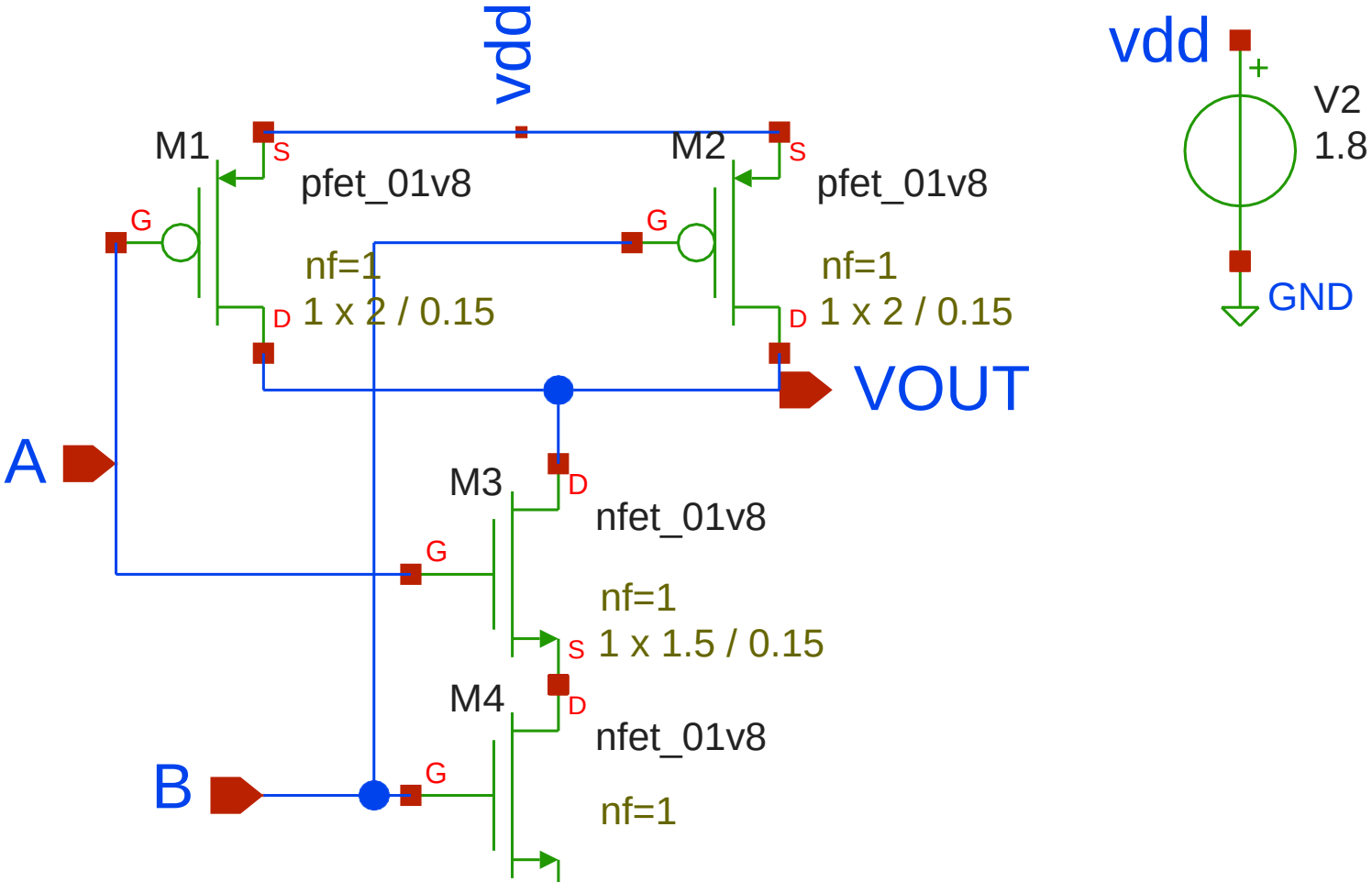
F

or2up.sch


VDD
M10
S
pfet_01v8
G
GND
nf=1
D
1 x 4/3 / 0.15
VDD
M16
S
pfet_01v8
G
GND
nf=1
D
1 x 4/3 / 0.15
VOUT
VDD
V2
1.8
GND
M17
D
nfet_01v8
G
nf=1
S
1 x 8/3 / 0.15
GND
M13
G
A
D
8
nfe
t_0
1v
nf=1
B


S
1 x 8/3 /
0.15
M14
D
nfe
t_0
1v
8
nf
=1
G
S
1 x
8/3 /
0.15
GND
GND

nand2.sch

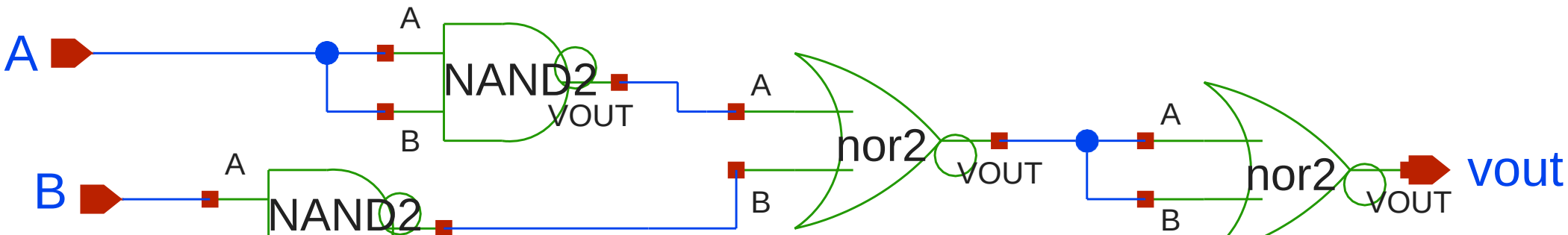

vdd
M1
S
pfet_01v8
G
nf=1
D
1 x 2 / 0.15
M2
S
pfet_01v8
G
nf=1
D
1 x 2 / 0.15
VOUT
A
M3
D
nfet_01v8
G
nf=1
S
1 x 1.5 / 0.15
M4
D
nfet_01v8
B
G
nf=1

vdd
+
V2
1.8
GND

s 1 x 1.5 / 0.15

GND

nand3.sch

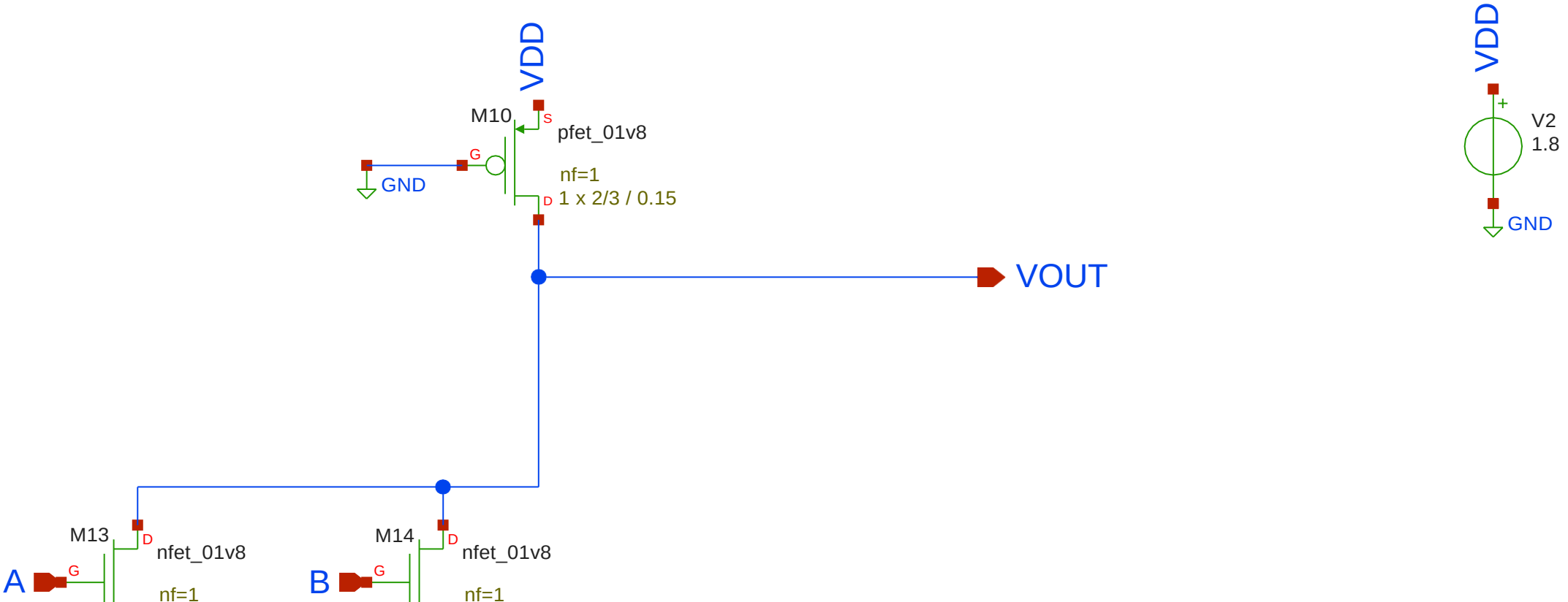


C

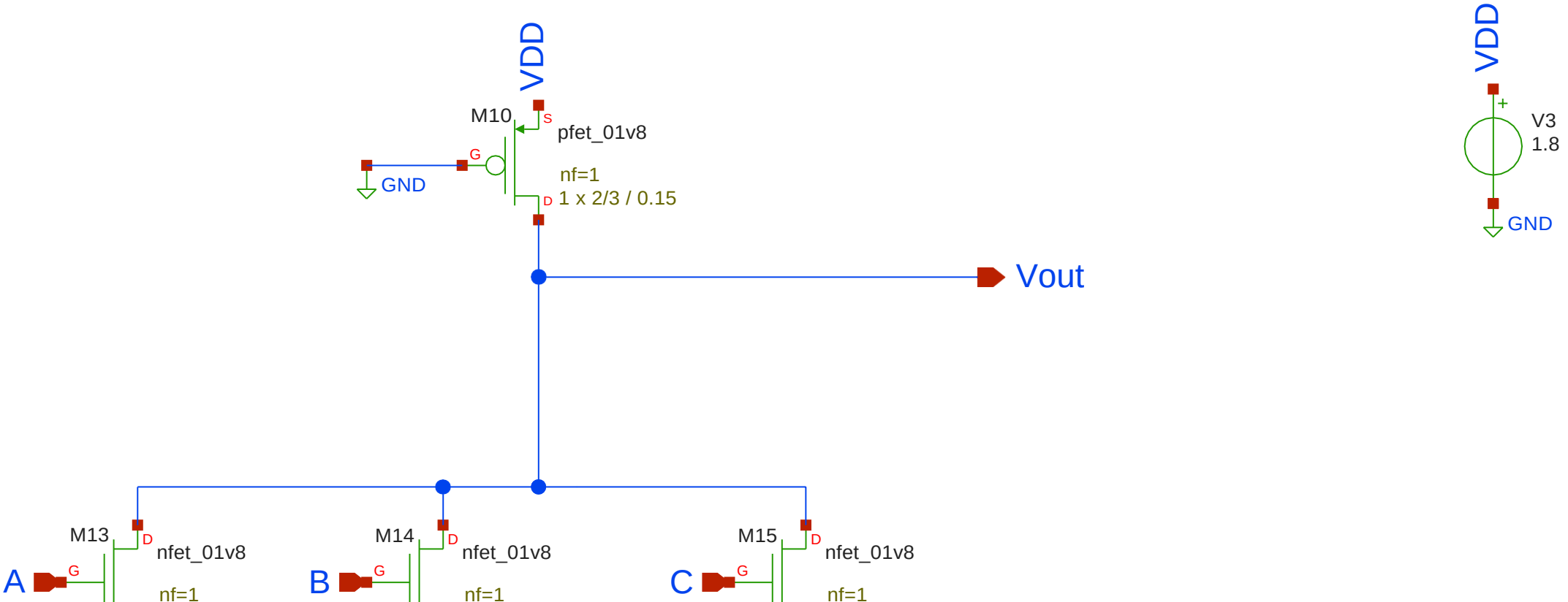
VOUT

B

nor2.sch


VDD
M10
S
pfet_01v8
G
GND
nf=1
D
1 x 2/3 / 0.15
VOUT
VDD
+
V2
1.8
GND
M13
D
nfet_01v8
A
G
nf=1
M14
D
nfet_01v8
B
G
nf=1

nor3.sch


VDD
M10
S
pfet_01v8
G
GND
nf=1
D
1 x 2/3 / 0.15
Vout
VDD
+
V3
1.8
GND
M13
D
nfet_01v8
A
G
nf=1
M14
D
nfet_01v8
B
G
nf=1
M15
D
nfet_01v8
C
G
nf=1