

# **MOS VLSI DESIGN(ELL734)**

## **Final Report: 5-bit Carry Lookahead Adder**



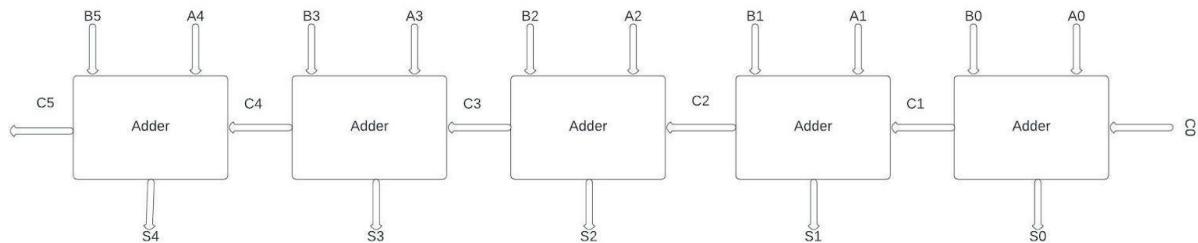
### **Team Members:**

1. K Ram Mohan - 2021VST 9509
2. P Reddy Sai Gagan (2022EEE2022)
3. Vishal Saini - 2019EE10546
4. Abhinav Reddy Oruganti- 2019EE10455

## Adder:

A Binary Adder is a digital circuit that implements the arithmetic sum of two binary numbers supported with any length is known as a binary adder. It is generated using full-adder circuits connected in sequence. The output carries from one full-adder linked to the input carry of the next full-adder.

So, here we are trying to design a 5-bit adder using CMOS logic and optimize the delay and power and the tradeoffs made for each of them.



Schematic of 5-bit Adder

## Truth Table of Carry Look-ahead Adder

For deriving the truth table of this adder, two new terms are introduced – Carry generate and carry propagate. Carry generates  $G_i = 1$  whenever there is a carry  $C_{i+1}$  generated. It depends on  $A_i$  and  $B_i$  inputs.  $G_i$  is 1 when both  $A_i$  and  $B_i$  are 1. Hence,  $G_i$  is calculated as  $G_i = A_i \cdot B_i$ .

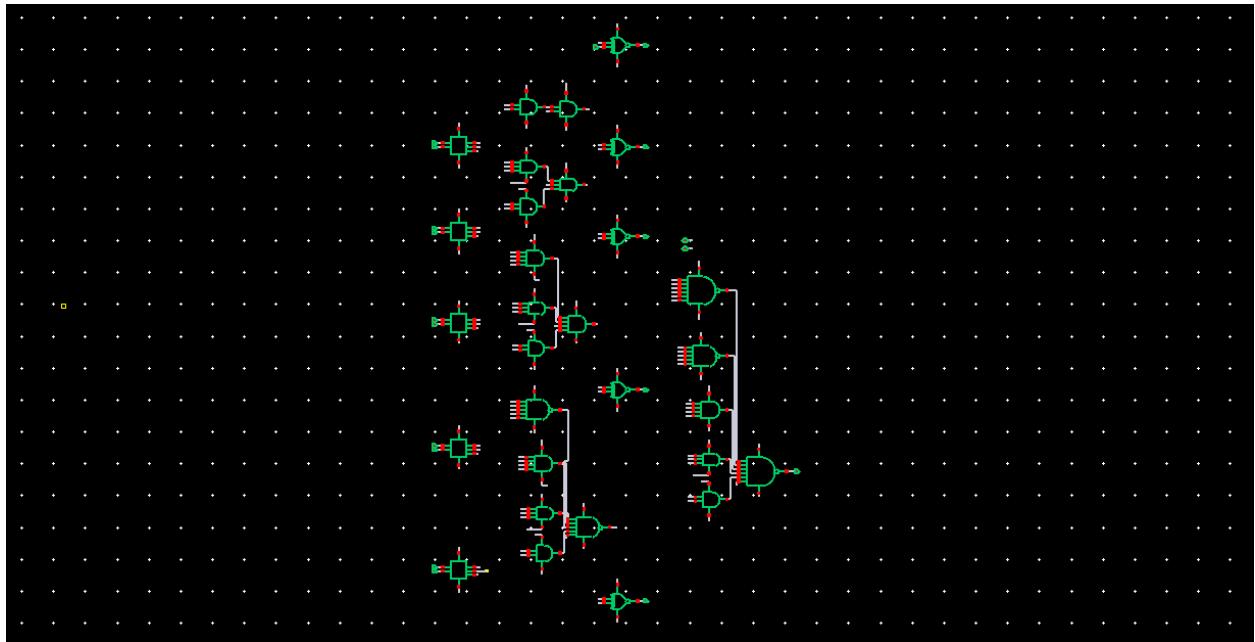
Carry propagated  $P_i$  is associated with the propagation of carry from  $C_i$  to  $C_{i+1}$ . It is calculated as  $P_i = A_i \oplus B_i$ . The truth table of this adder can be derived from modifying the truth table of a full adder.

Using the Gi and Pi terms the Sum Si and Carry Ci+1 are given as below –

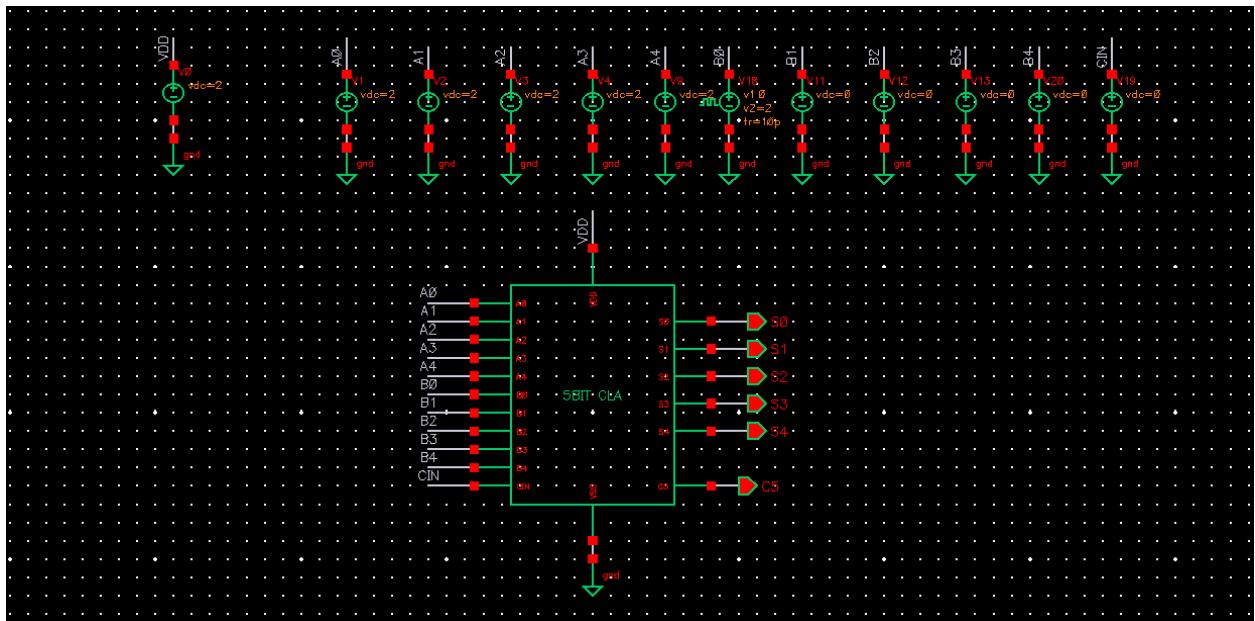
- $S_i = P_i \oplus G_i$ .
- $C_{i+1} = C_i \cdot P_i + G_i$ .

| <b>A</b> | <b>B</b> | <b>Ci</b> | <b>C i +1</b> | <b>Condition</b>   |
|----------|----------|-----------|---------------|--------------------|
| 0        | 0        | 0         | 0             | No carry generate  |
| 0        | 0        | 1         | 0             |                    |
| 0        | 1        | 0         | 0             |                    |
| 0        | 1        | 1         | 1             | No carry propagate |
| 1        | 0        | 0         | 0             |                    |
| 1        | 0        | 1         | 1             |                    |
| 1        | 1        | 0         | 1             | Carry generate     |
| 1        | 1        | 1         | 1             |                    |

# Schematics



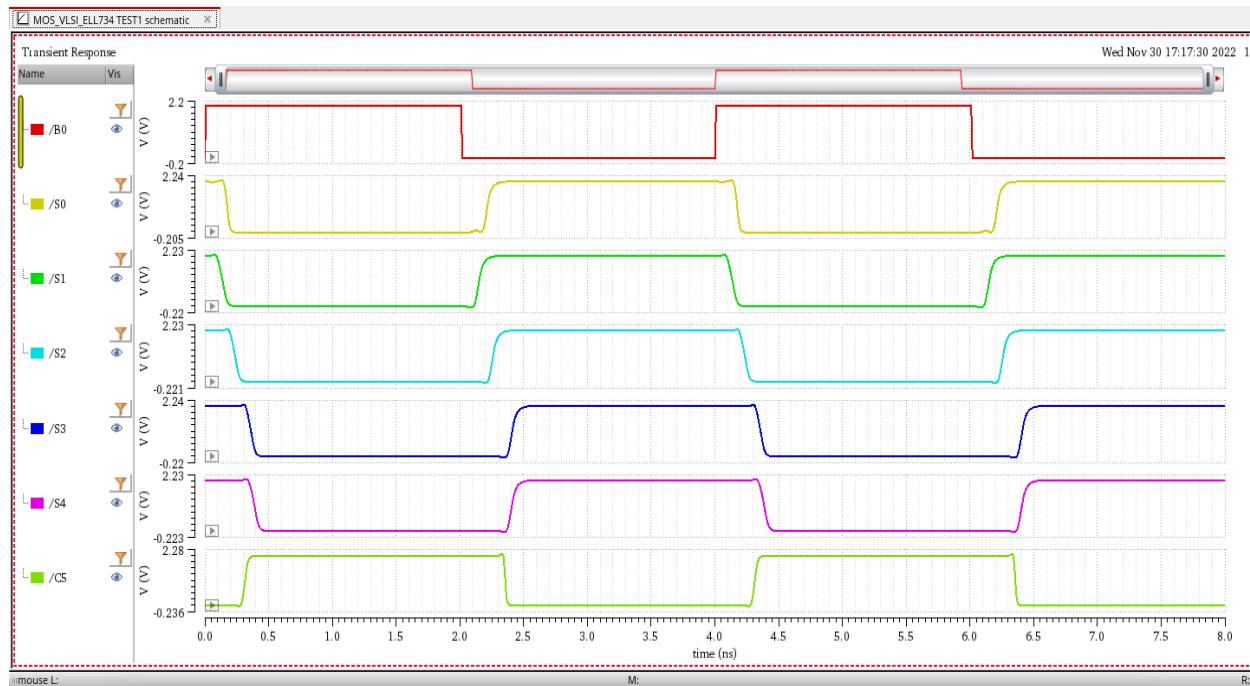
## Test Bench for 5-bit Adder



## Specifications Achieved:

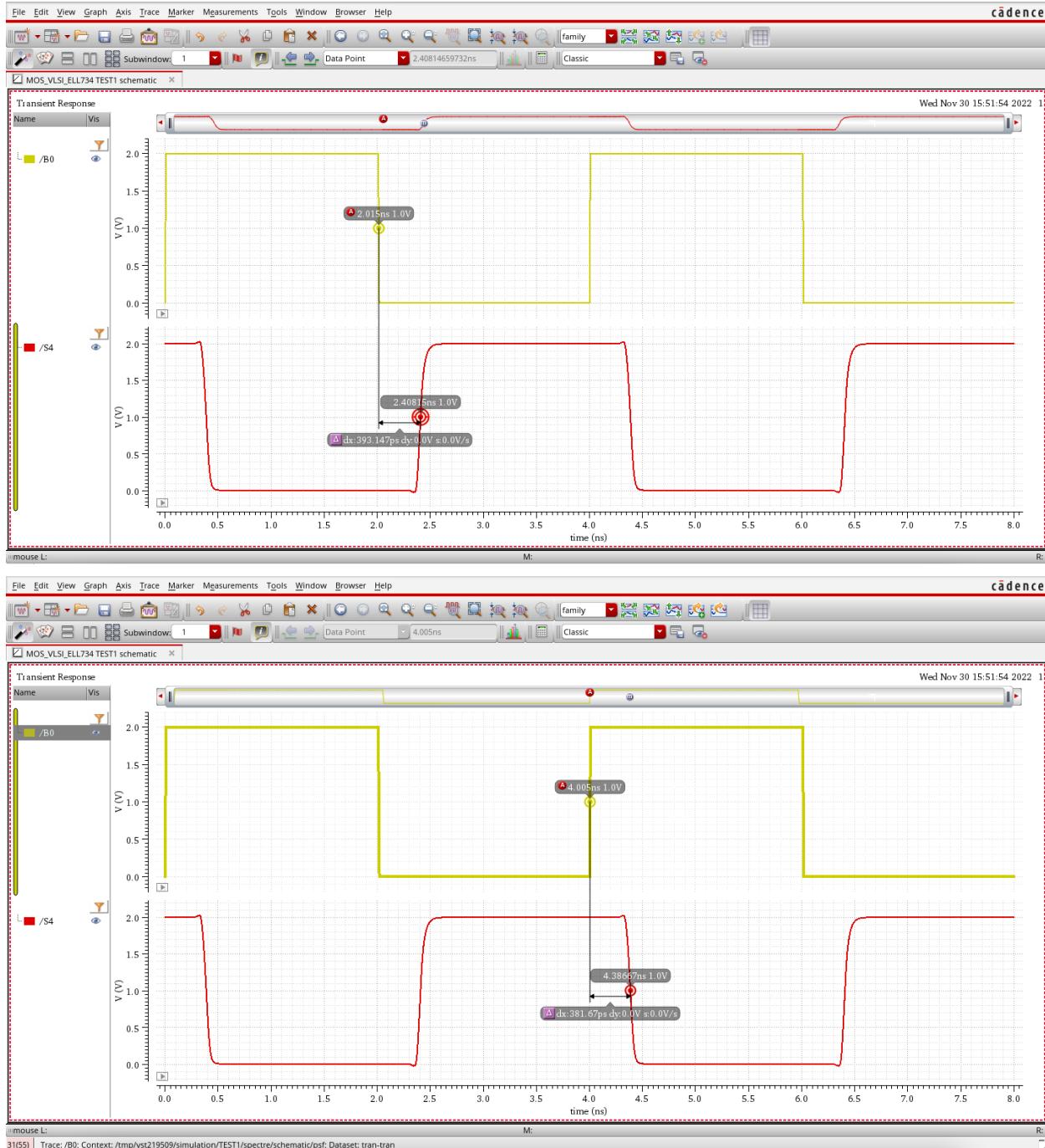
| Specification      | Schematic   | Layout   |
|--------------------|---|--|
| Technology         | TSMC 180nm  | TSMC 180nm   |
| Vdd                | 2V  | 2V   |
| Power              | 3.111E-6  | 3.192E-6   |
| Temperature        | -40,27,125°C  | -40,27,125°C   |
| Clock Speed(Pulse) | At -40°C - 2.9GHz<br>At 27°C - 2.58GHz<br>At 125°C- 2.23GHz | At -40°C - 2.24GHz<br>At 27°C - 2.075GHz<br>At 125°C- 1.783GHz |
| Area               | NA  | 3539.2μm <sup>2</sup>  |

## Functionality of 5-bit Adder



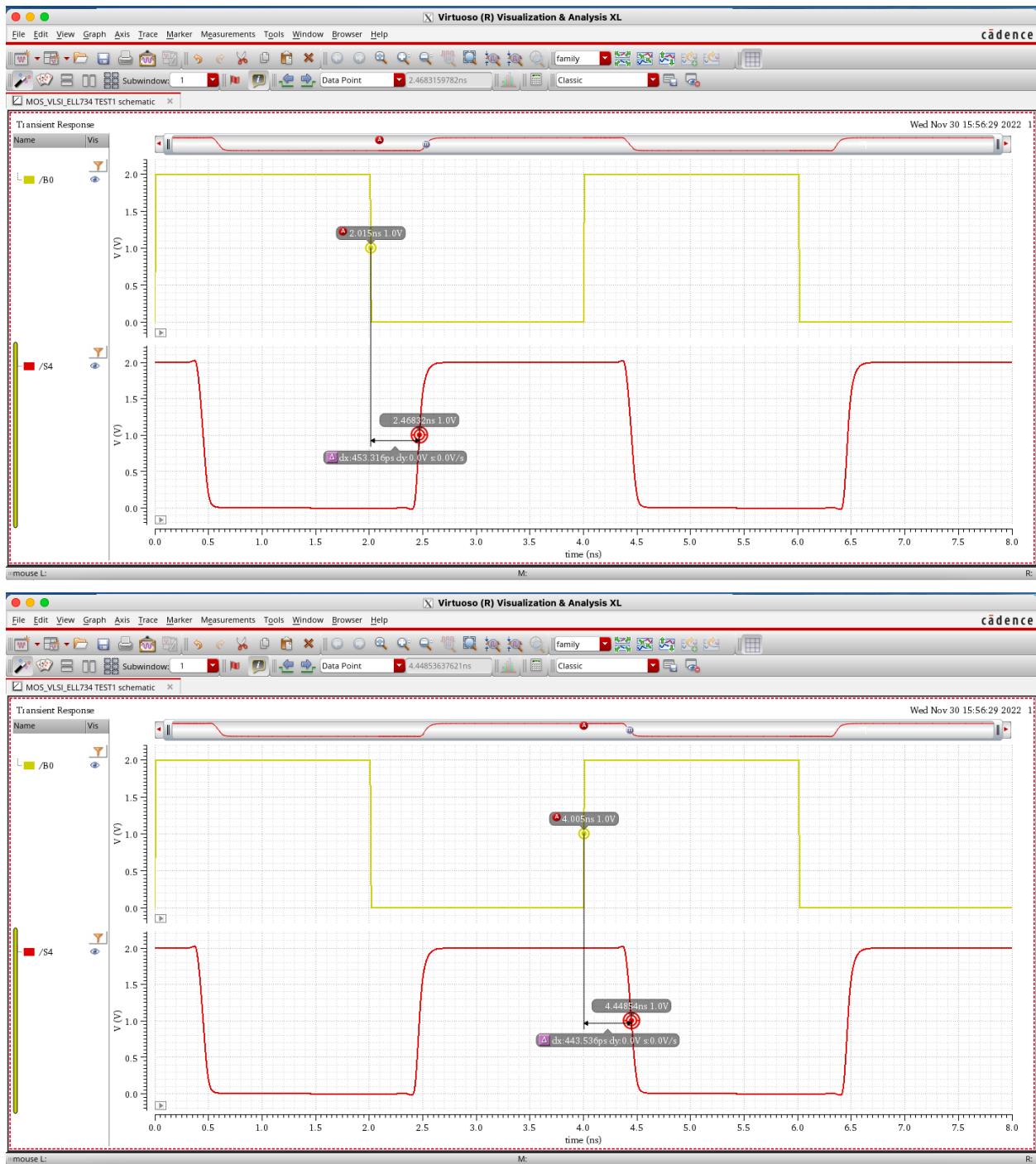
# Delay

## 1. Delay of 5-bit Adder for T=27°C



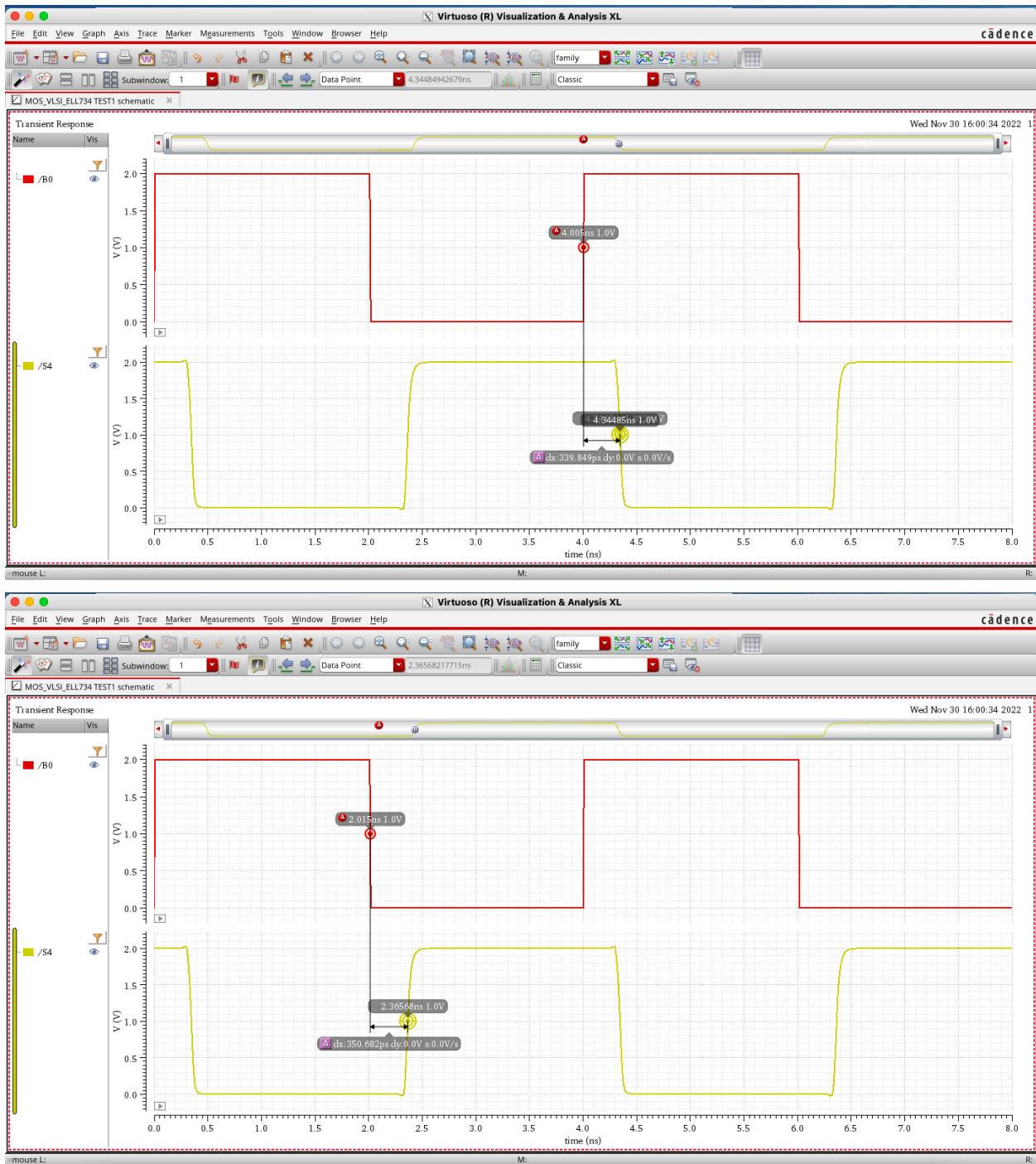
$$\text{Delay} = (\text{T}_{\text{Rise}} + \text{T}_{\text{fall}})/2 = (393.147 + 381.67)/2 = 387.41\text{ps}$$

## 2. Delay of 5-bit Adder for T=125°C



$$\text{Delay} = (\text{T}_{\text{Rise}} + \text{T}_{\text{fall}})/2 = (453.316 + 453.536)/2 = 448.57\text{ps}$$

### 3. Delay of 5-bit Adder for T=-40°C



$$\text{Delay} = (\text{T}_{\text{Rise}} + \text{T}_{\text{fall}})/2 = (339.85 + 350.68)/2 = 345.27\text{ps}$$

## Critical Path

Total delay of CLA=(delay of the generate/propagate gates)+(total delay of the k-bit blocks) + (No. of carry look ahead adder blocks × total delay of the carry look ahead blocks from  $C_{in}$  to  $C_{out}$ ) + (No. of ripple carry adder blocks × delay of a ripple carry adder)

Total delay of CLA=(delay of the generate/propagate gates)+(total delay of the k-bit blocks) + (No. of carry look ahead adder blocks × total delay of the carry look ahead blocks from  $C_{in}$  to  $C_{out}$ ) + (No. of ripple carry adder blocks × delay of a ripple carry adder)

Substituting the terms we get,  $t_{CLA} = t_{pg} + t_{pg\_block} + (N_k - 1).t_{and\_or} + k.T_{fa}$

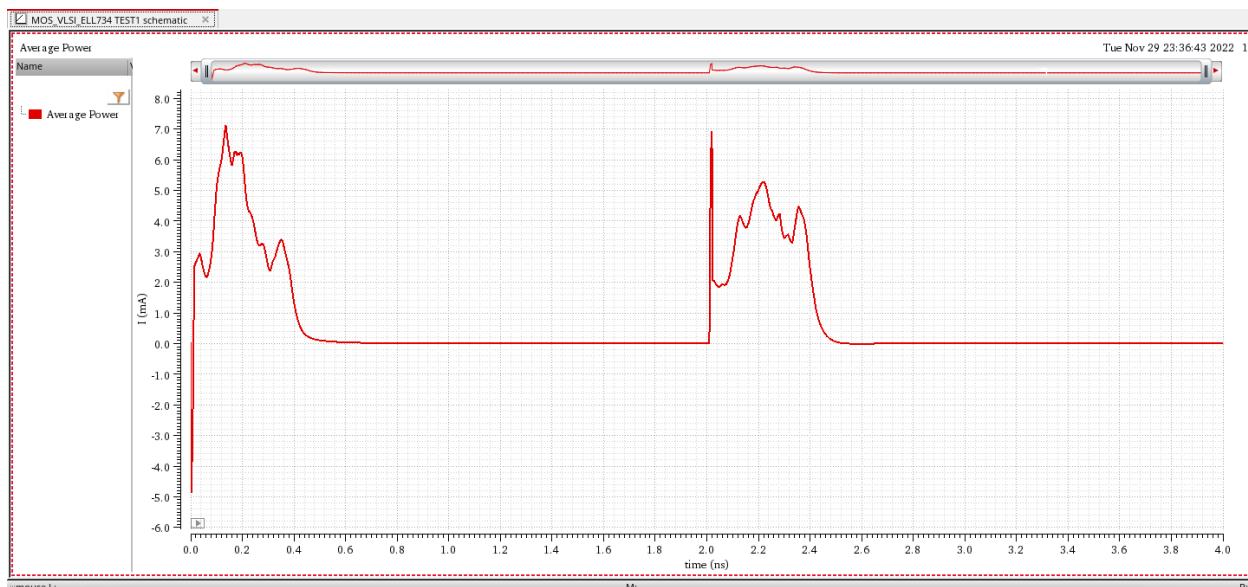
Input  $\rightarrow S_4$  is the critical path.

Critical path is from input  $\rightarrow$  generator propagate block  $\rightarrow$  carry of (n-1)th bit  $\rightarrow$  final sum block of final bit.

It will occur for this case:

$$\begin{aligned} A_4 A_3 A_2 A_1 A_0 &= 11111 \\ B_4 B_3 B_2 B_1 B_0 &= 00001 \\ C_{in} &= 0 \end{aligned}$$

## Power

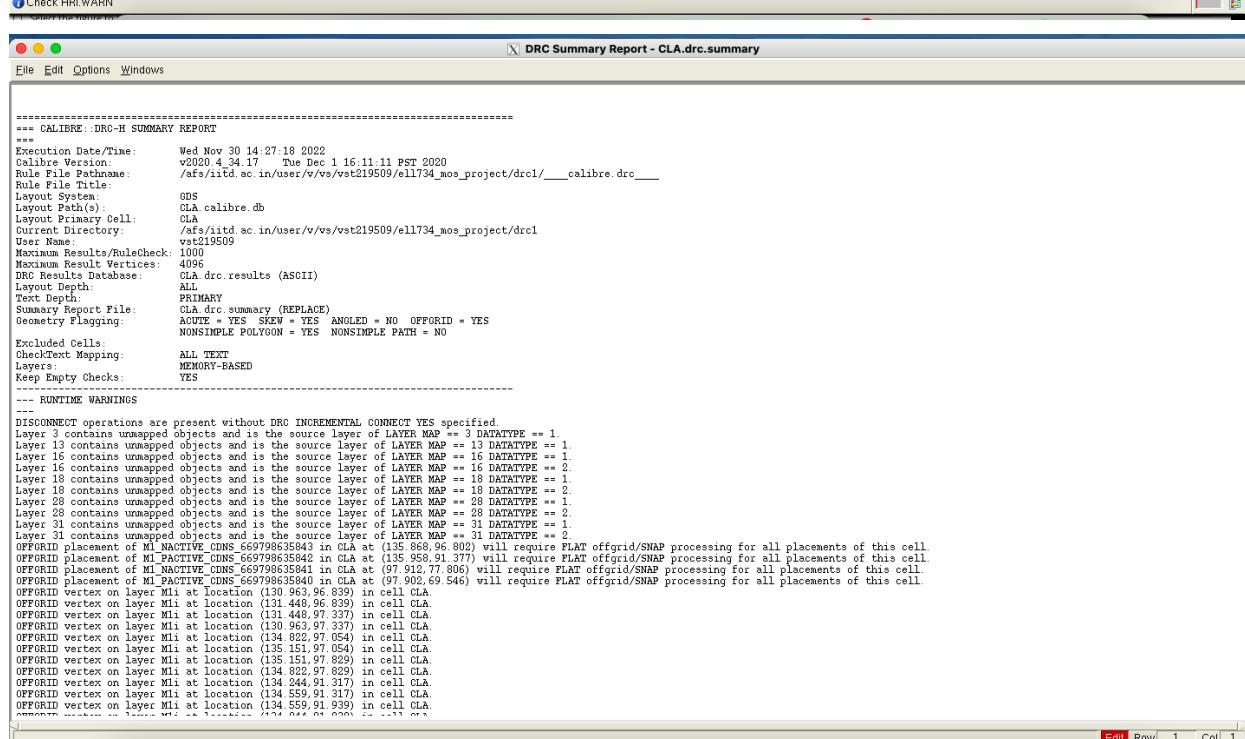
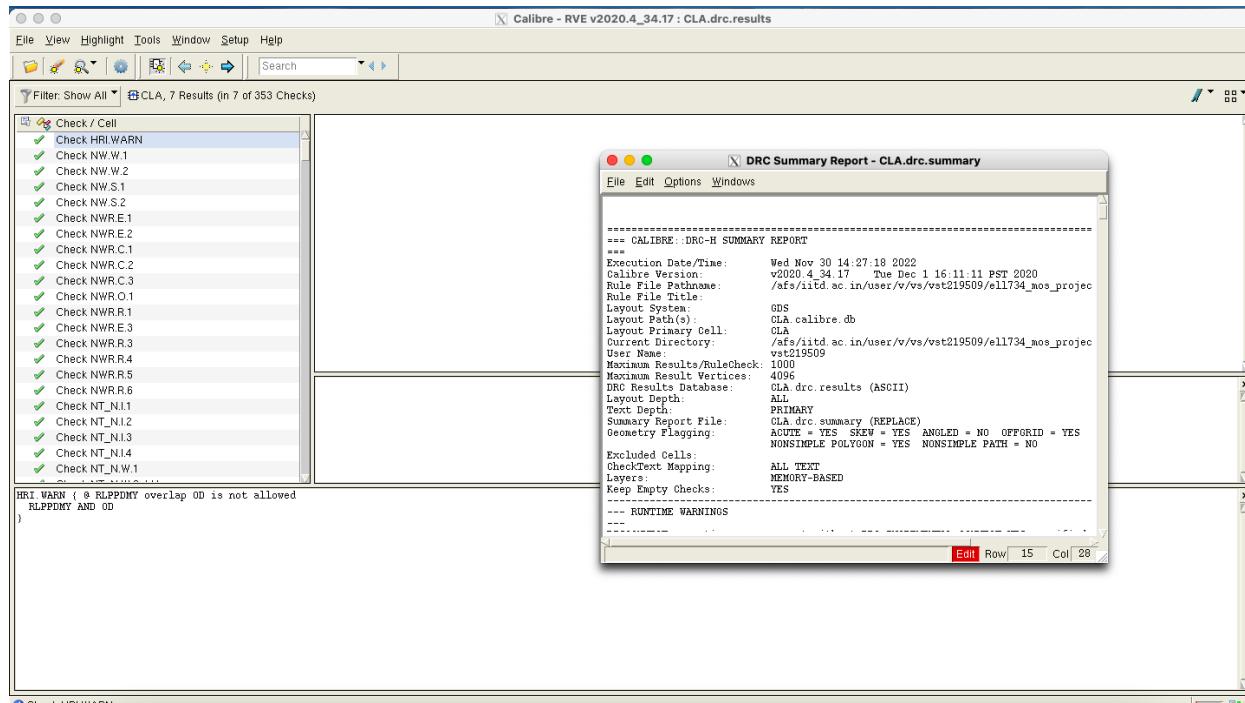


Average Power = 3.111E-6

# DRC(\*\* DRC report attached for reference \*\*)

Report-[https://drive.google.com/file/d/19A7JOH7VvCRfLAdqvYLA9\\_O9RJ8Ks8Ty/view?usp=share\\_link](https://drive.google.com/file/d/19A7JOH7VvCRfLAdqvYLA9_O9RJ8Ks8Ty/view?usp=share_link)

Summary-[https://drive.google.com/file/d/1HA62-rafqoo3-Qlxrl2Q4dk1Y7wCAsS3/view?usp=share\\_link](https://drive.google.com/file/d/1HA62-rafqoo3-Qlxrl2Q4dk1Y7wCAsS3/view?usp=share_link)



# LVS (\*\* LVS report attached for reference \*\*)

Report-[https://drive.google.com/file/d/1ggZOI1DqN9J2wurRW3FkE499grn7Y6A-/view?usp=share\\_link](https://drive.google.com/file/d/1ggZOI1DqN9J2wurRW3FkE499grn7Y6A-/view?usp=share_link)

```
CLAB.lvs_report
## CALIBRE SYSTEM ##
## LVS REPORT ##
#####
REPORT FILE NAME: CLAB.lvs_report
LAYOUT NAME: /afs/iitd.ac.in/user/v/vs/vst219509/el11734_mos_project/lvs/CLAB.sp ('CLAB')
SOURCE NAME: /afs/iitd.ac.in/user/v/vs/vst219509/el11734_mos_project/lvs/CLAB_src.net ('CLAB')
RULE FILE: /afs/iitd.ac.in/user/v/vs/vst219509/el11734_mos_project/lvs/_calibre.lvs_
CREATE TIME: Wed Nov 30 14:19:20 2020
CURRENT DIRECTORY: /afs/iitd.ac.in/user/v/vs/vst219509/el11734_mos_project/lvs
USER NAME: vst219509
CALIBRE VERSION: v2020_4_34.17 Tue Dec 1 16:11:11 PST 2020

OVERALL COMPARISON RESULTS

# # ##### #
# # CORRECT # #
# # ##### #

***** CELL SUMMARY *****
Result Layout Source
----- -----
CORRECT CLAB CLAB

***** LVS PARAMETERS *****
o LVS Setup:
// LVS COMPONENT TYPE PROPERTY
// LVS COMPONENT PROPERTY

Edit Row 1 Col 1
```

```
Calibre - RVE v2020.4_34.17 : svdb CLAB
File View Highlight Tools Window Setup Help
Navigator Comparison Results
Results Extraction Results Comparison Results
ERC ERC Results ERC Summary
Reports Extraction Report LVS Report
Rules Rules File
View Info Finder Schematics
Setup Options

Comparison Results x
Layout Cell / Type Source Cell Nets Instances Ports
CLAB CLAB 114L, 114S 121L, 121S 19L, 19S
Cell CLA Summary (Clean)
CELL COMPARISON RESULTS ( TOP LEVEL )

# # ##### #
# # CORRECT # #
# # ##### #

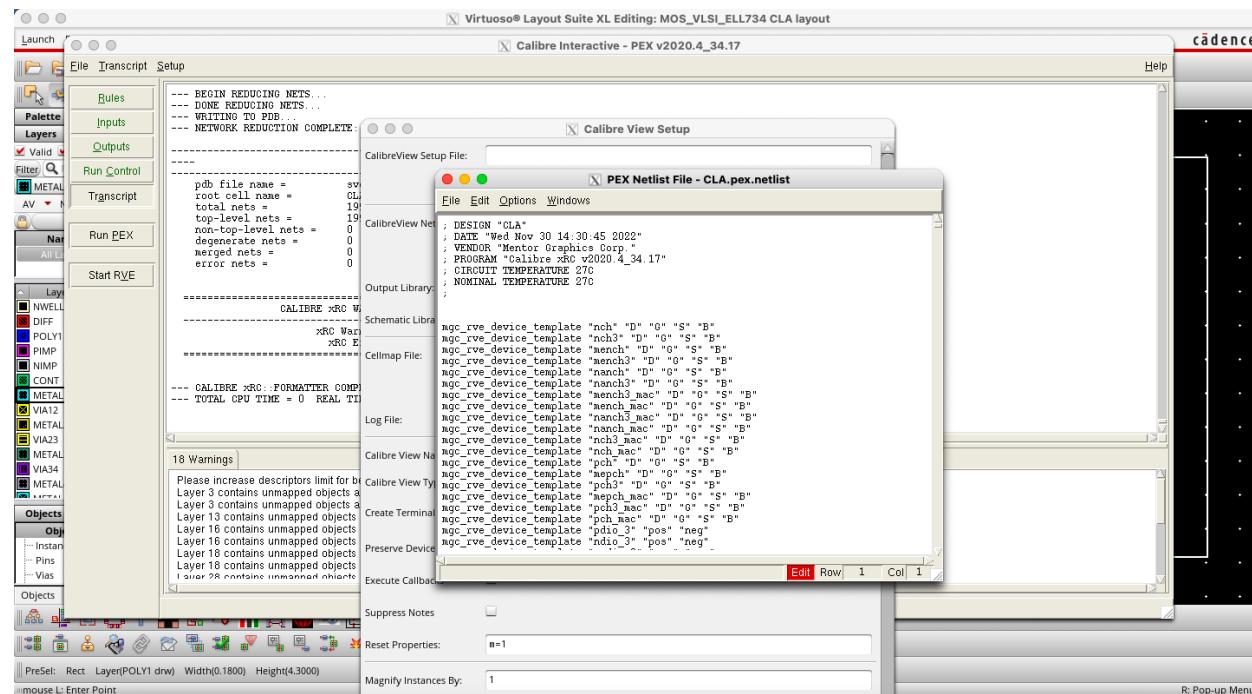
LAYOUT CELL NAME: CLAB
SOURCE CELL NAME: CLAB

INITIAL NUMBERS OF OBJECTS
-----
Layout Source Component Type
Ports: 19 19
Nets: 199 199
Instances: 186 186 MN (4 pins)
186 186 MP (4 pins)
Total Inst: 372 372

NUMBERS OF OBJECTS AFTER TRANSFORMATION
```

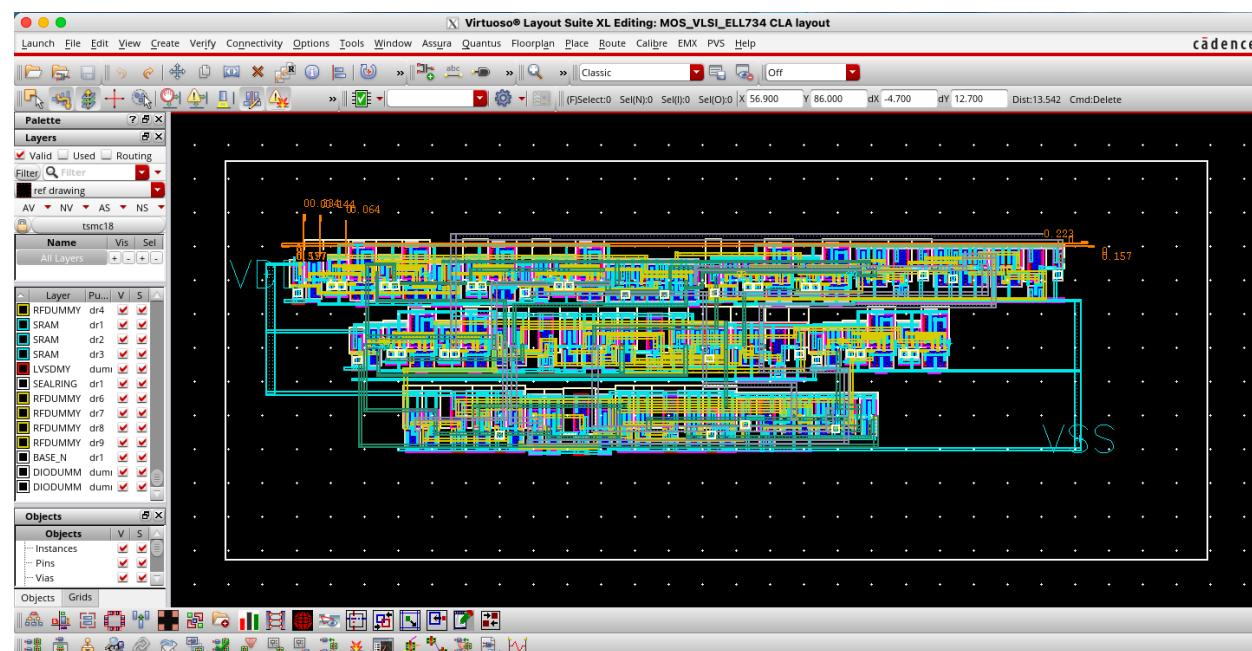
## PEX (\*\* PEX report attached for reference \*\*)

Report-[https://drive.google.com/file/d/1xknoN3OSEpuh4salaOc3mzfWdESm--QK/view?usp=share\\_link](https://drive.google.com/file/d/1xknoN3OSEpuh4salaOc3mzfWdESm--QK/view?usp=share_link)



## Layout

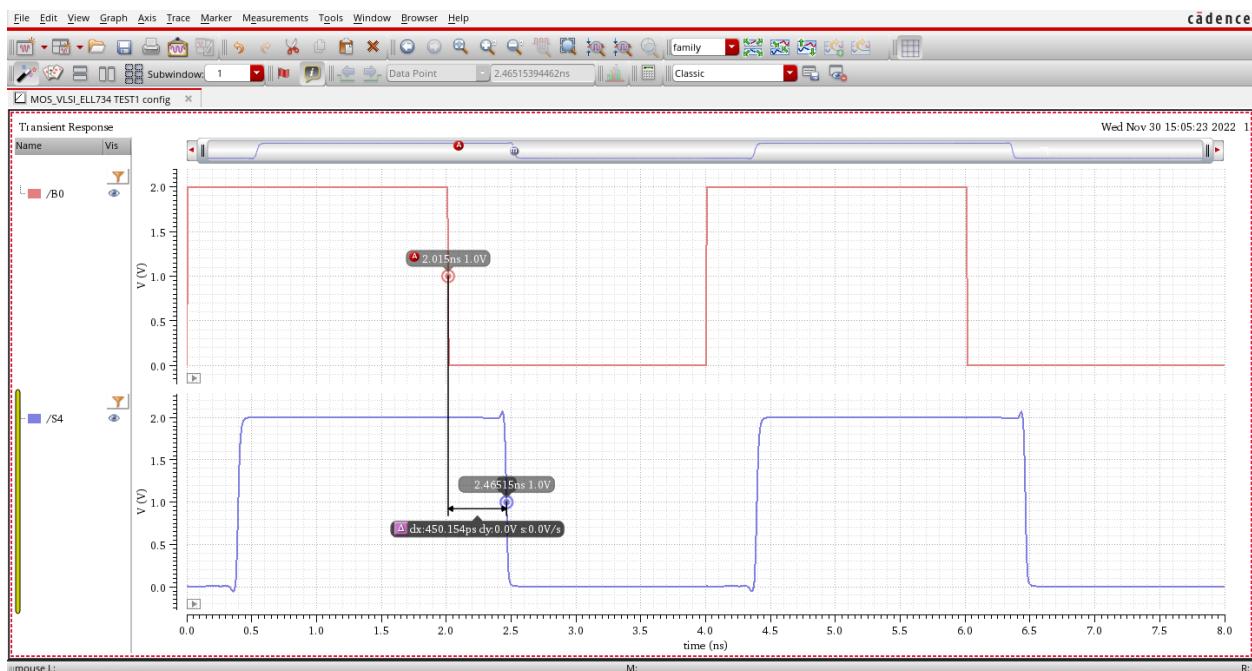
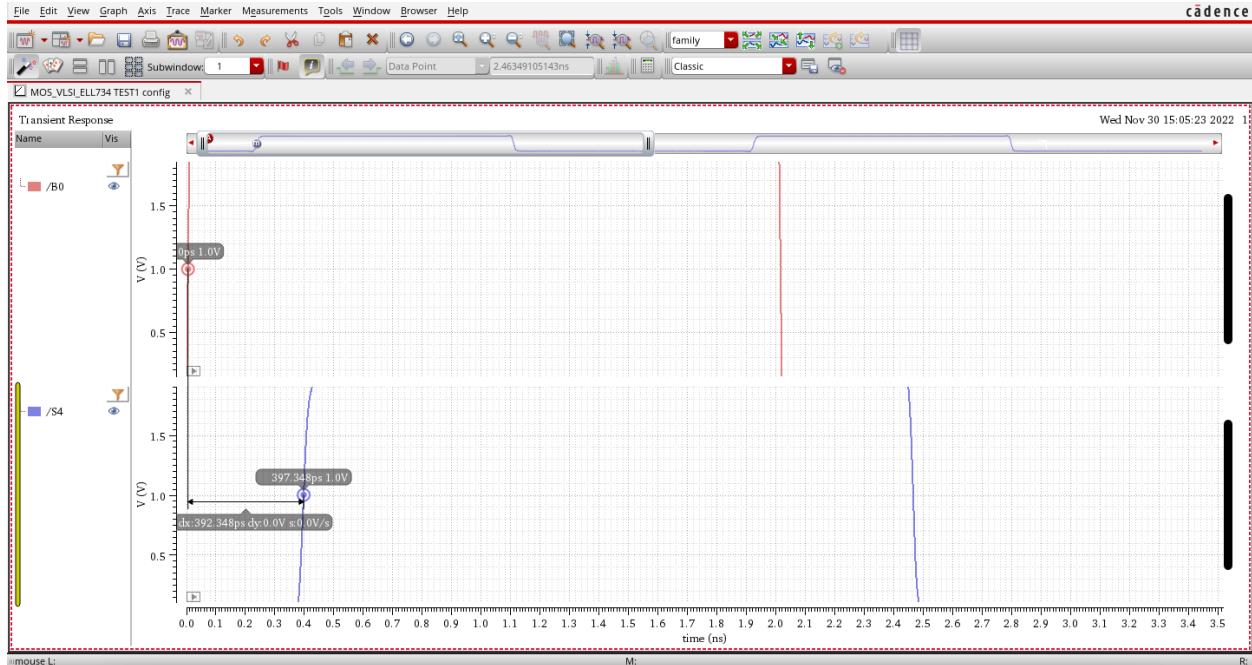
Link-[https://drive.google.com/file/d/14SG1m5vXd7a-13WUEyOXn0UXAnZYW9YI/view?usp=share\\_link](https://drive.google.com/file/d/14SG1m5vXd7a-13WUEyOXn0UXAnZYW9YI/view?usp=share_link)



# Extraction Results

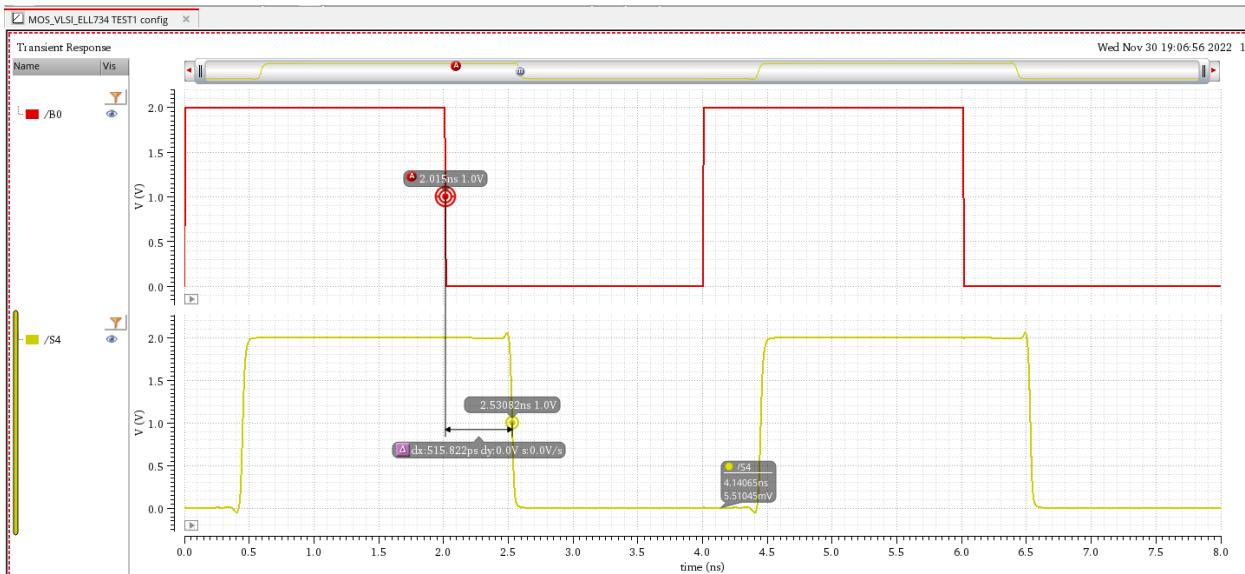
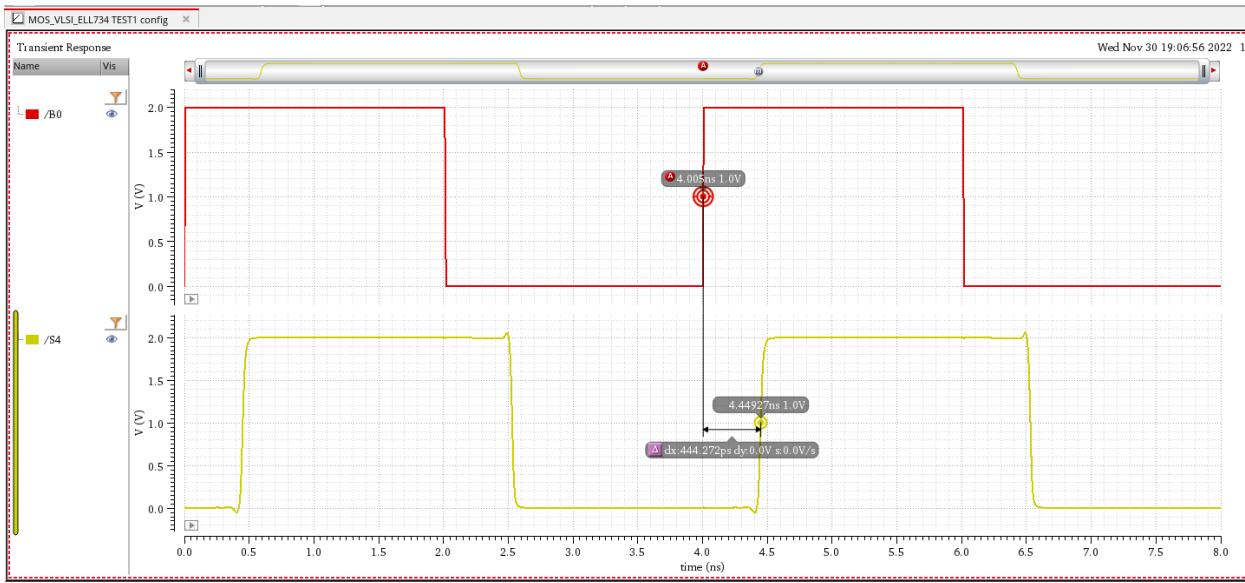
## 1. Delay after extraction:

### A. At 27°C



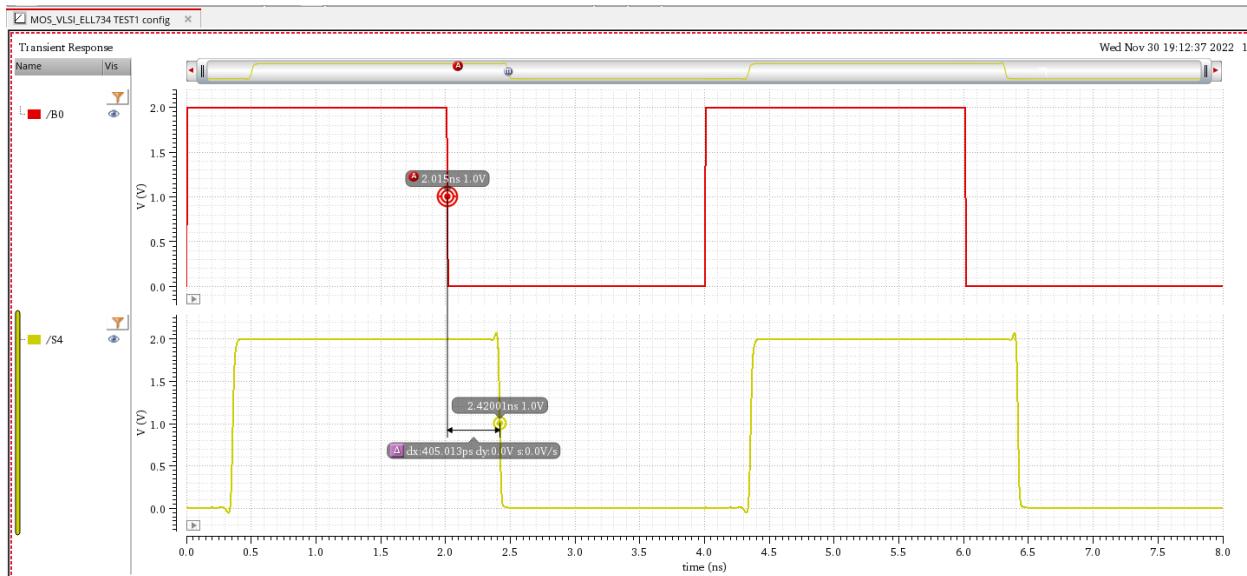
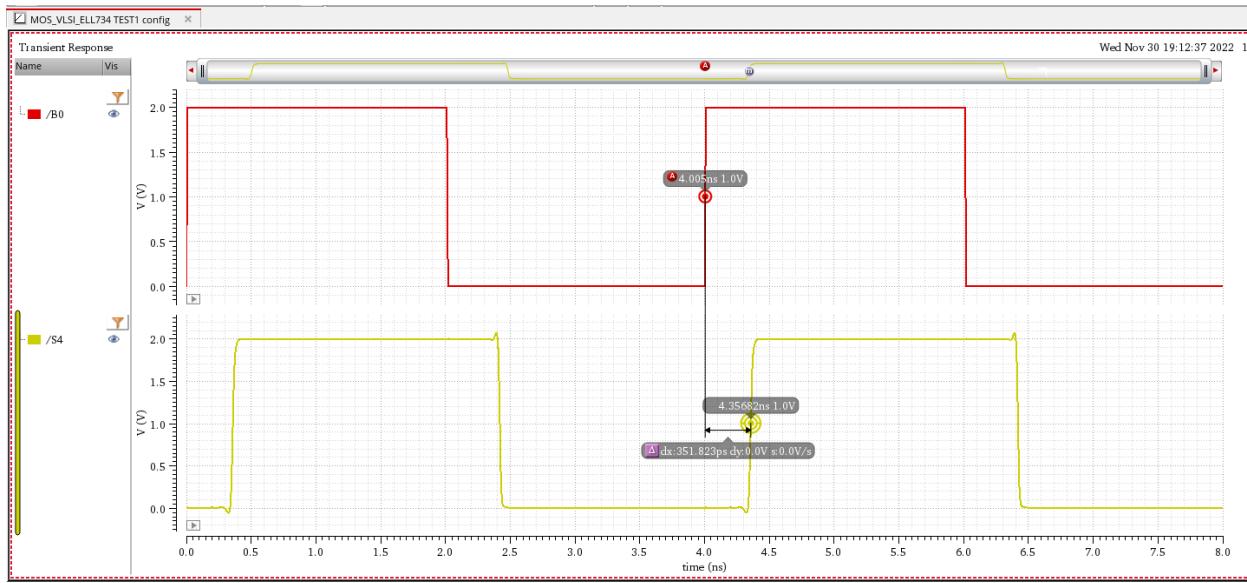
$$\text{Delay} = (\text{T}_{\text{Rise}} + \text{T}_{\text{fall}})/2 = (392 + 450)/2 = 421\text{ps}$$

## B. At 125°C



$$\text{Delay} = (\text{T}_{\text{Rise}} + \text{T}_{\text{fall}})/2 = (444.272 + 515.822)/2 = 480\text{ps}$$

### C. At -40°C



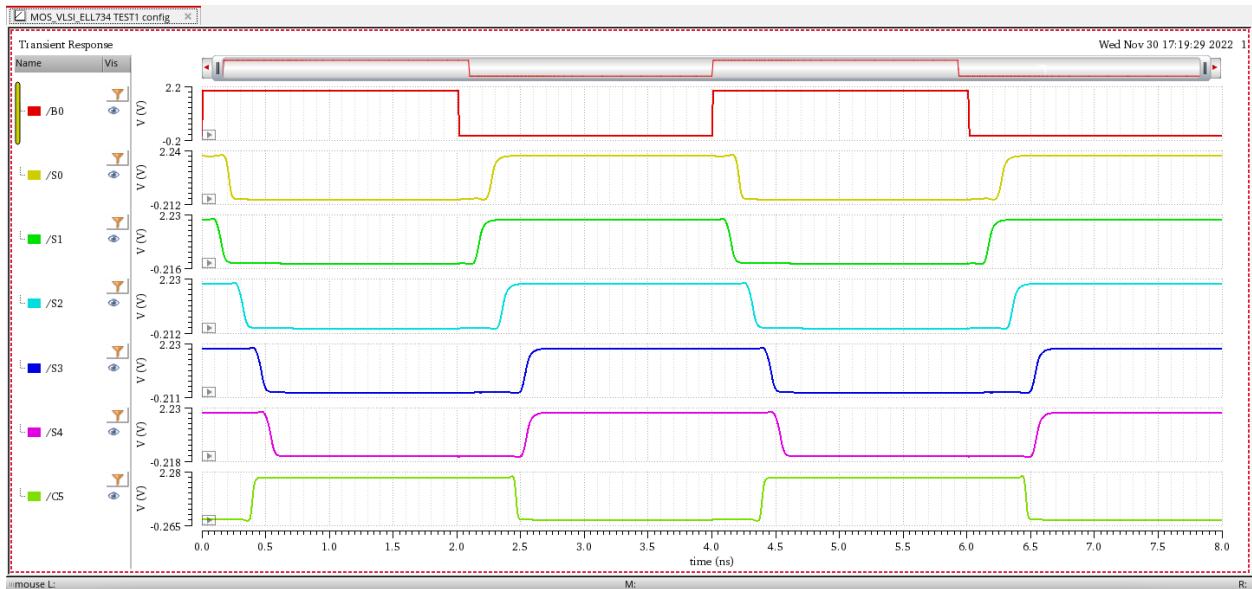
$$\text{Delay} = (\text{T}_{\text{Rise}} + \text{T}_{\text{fall}})/2 = (351.823 + 405.013)/2 = 378.42\text{ps}$$

## 2. Average Power after extraction



Average Power = 3.192E-6

## 3. Functionality after extraction



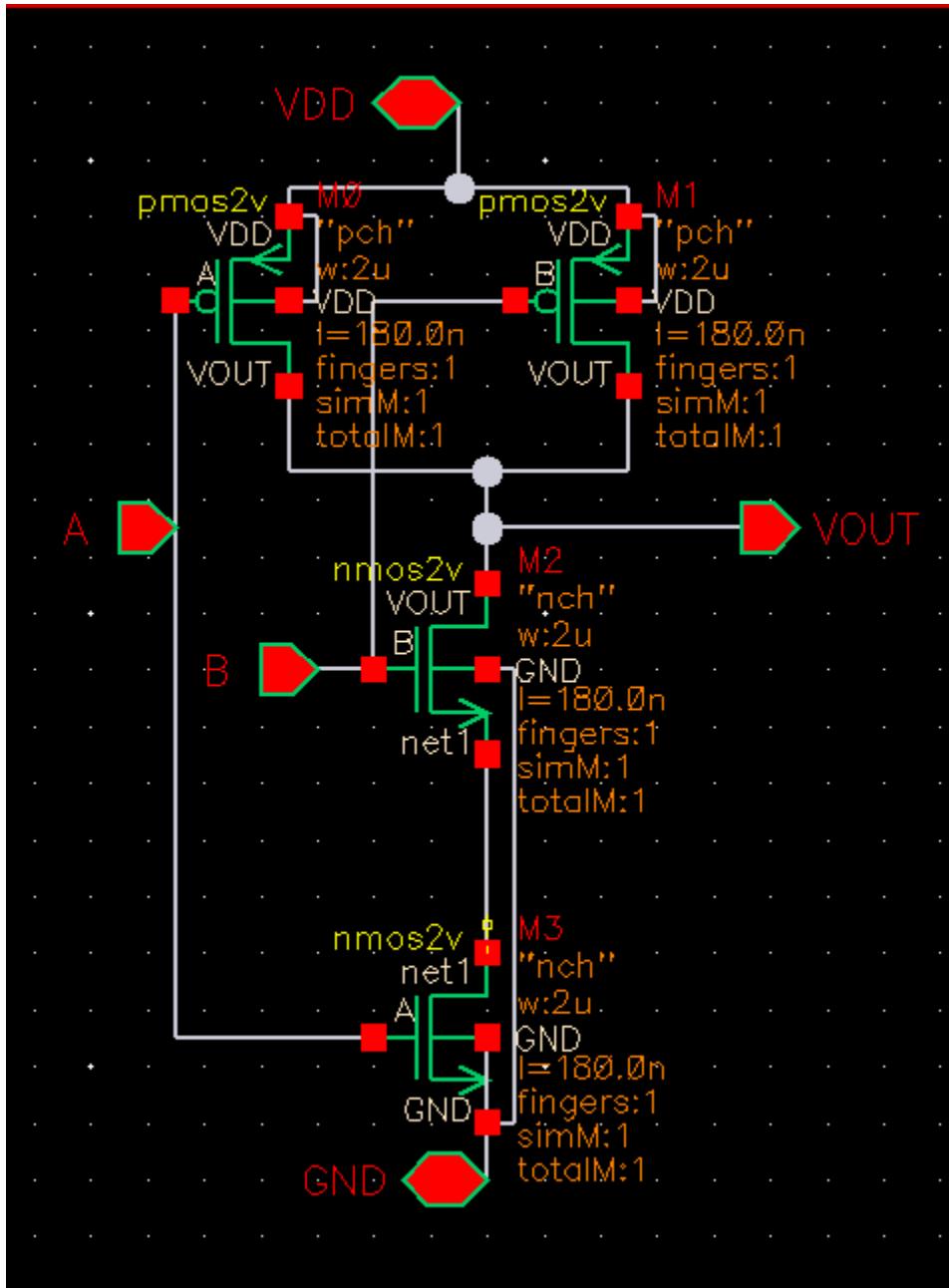
We come to the conclusion that the 5-bit adder's functionality is unchanged after extraction.

# SCHEMATICS

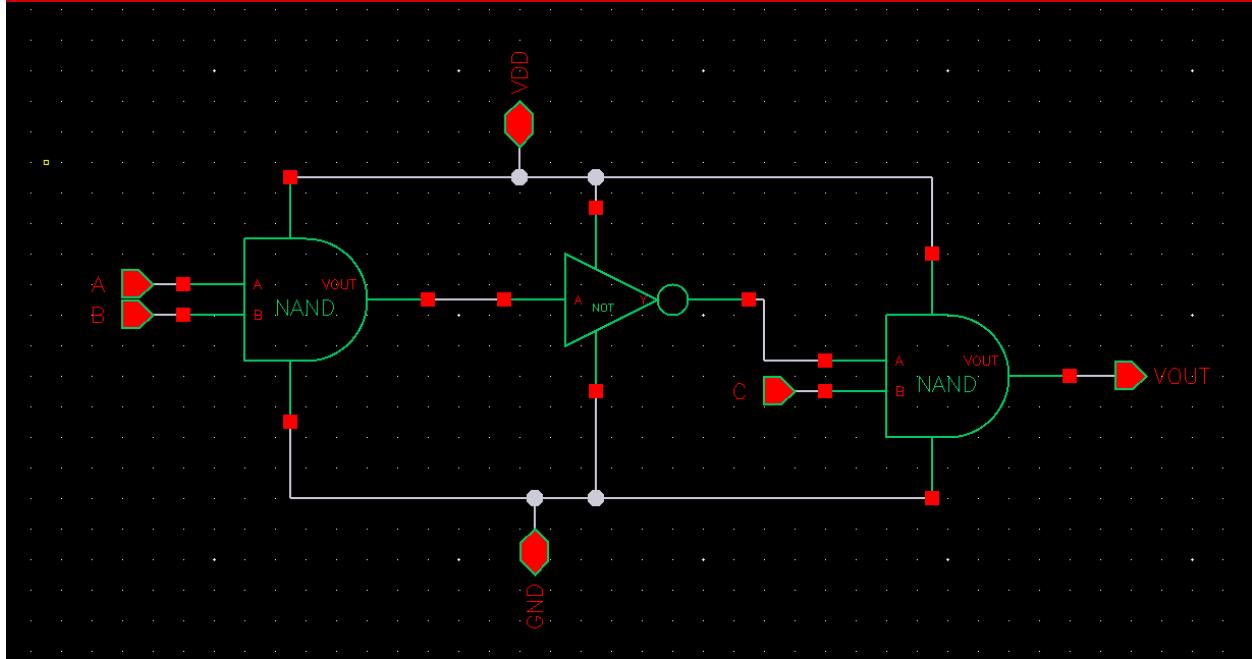
Schematics of whole 5-bit Adder-

[https://drive.google.com/file/d/14SG1m5vXd7a-13WUEyOXn0UXAnZYW9YI/view?usp=share\\_link](https://drive.google.com/file/d/14SG1m5vXd7a-13WUEyOXn0UXAnZYW9YI/view?usp=share_link)

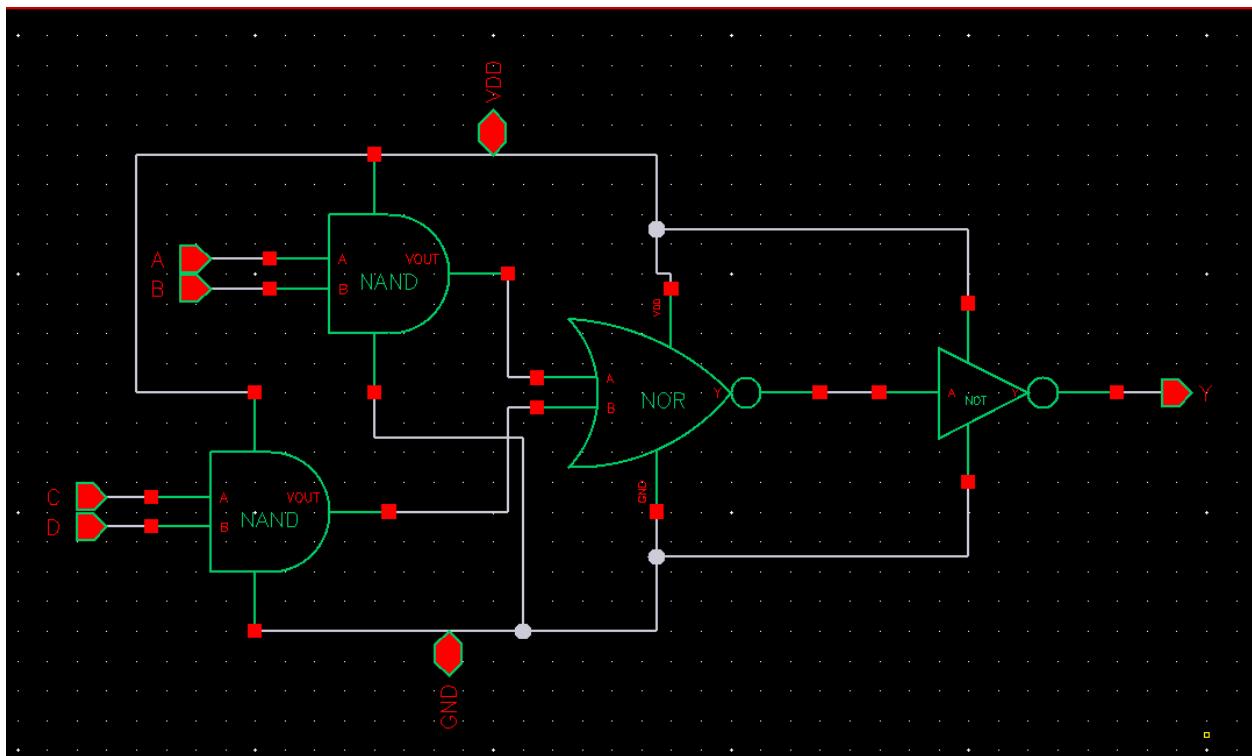
## NAND



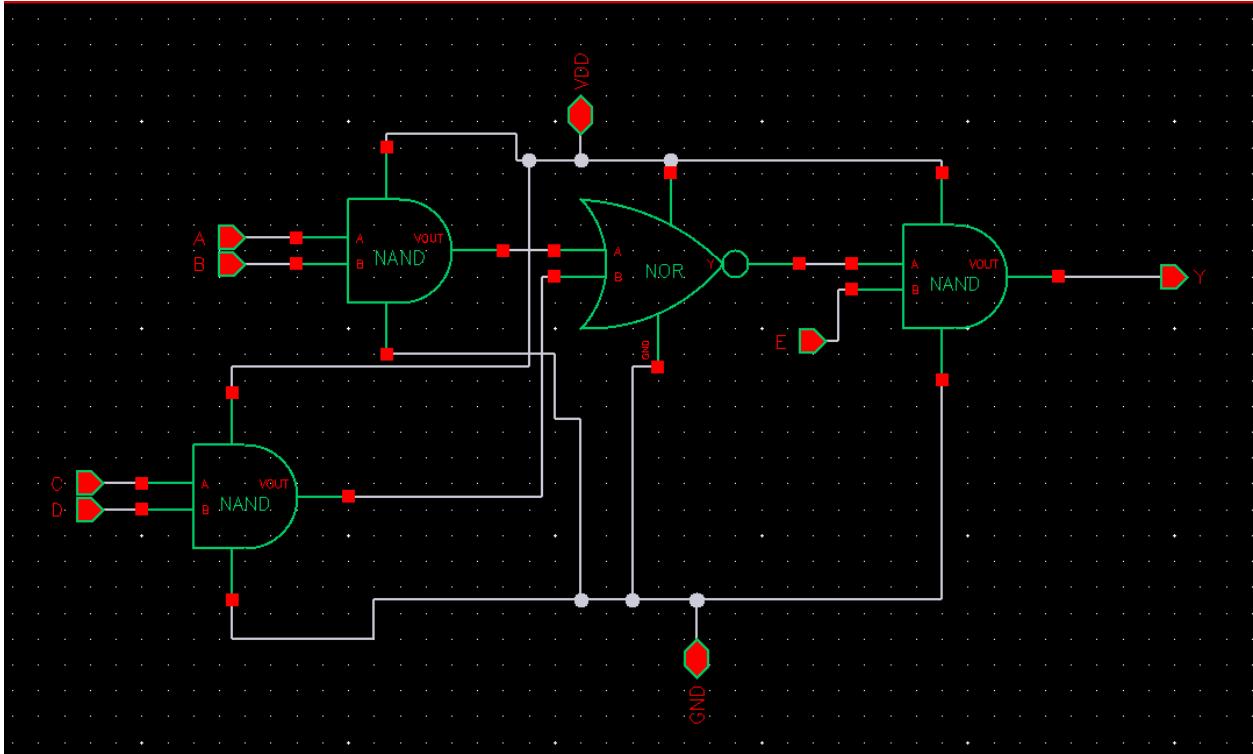
## NAND3



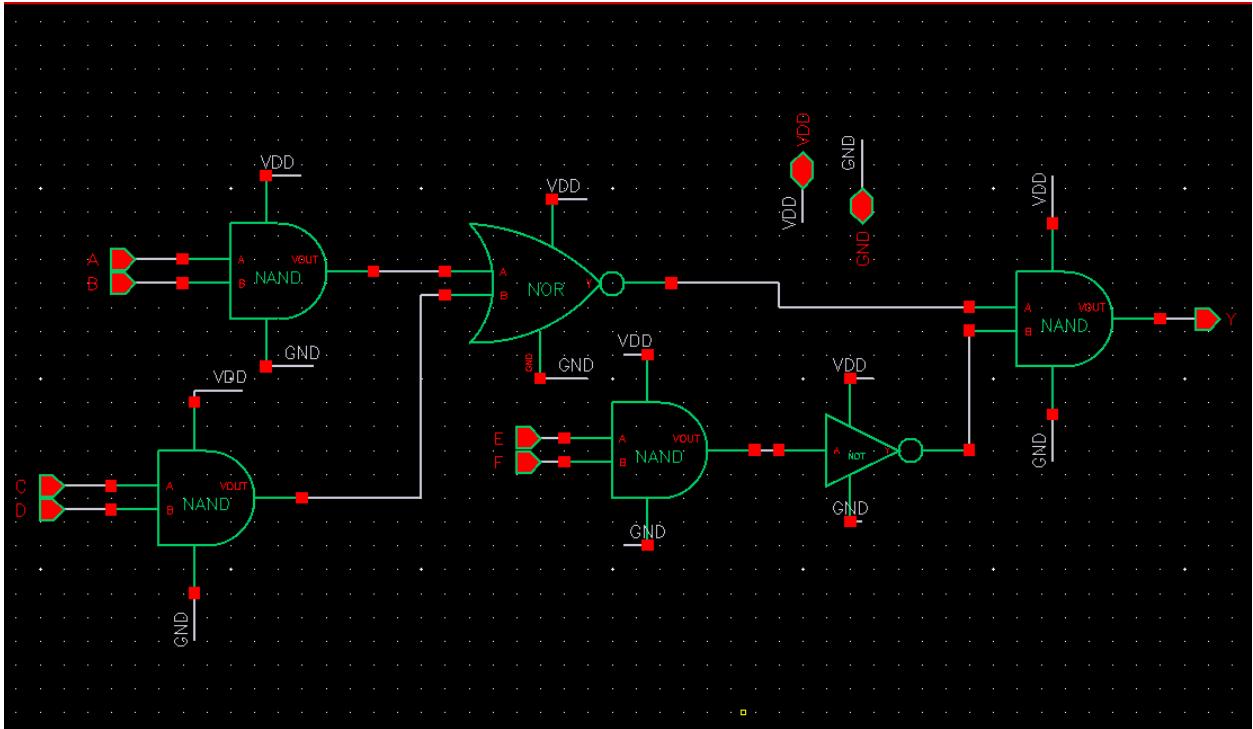
## NAND4



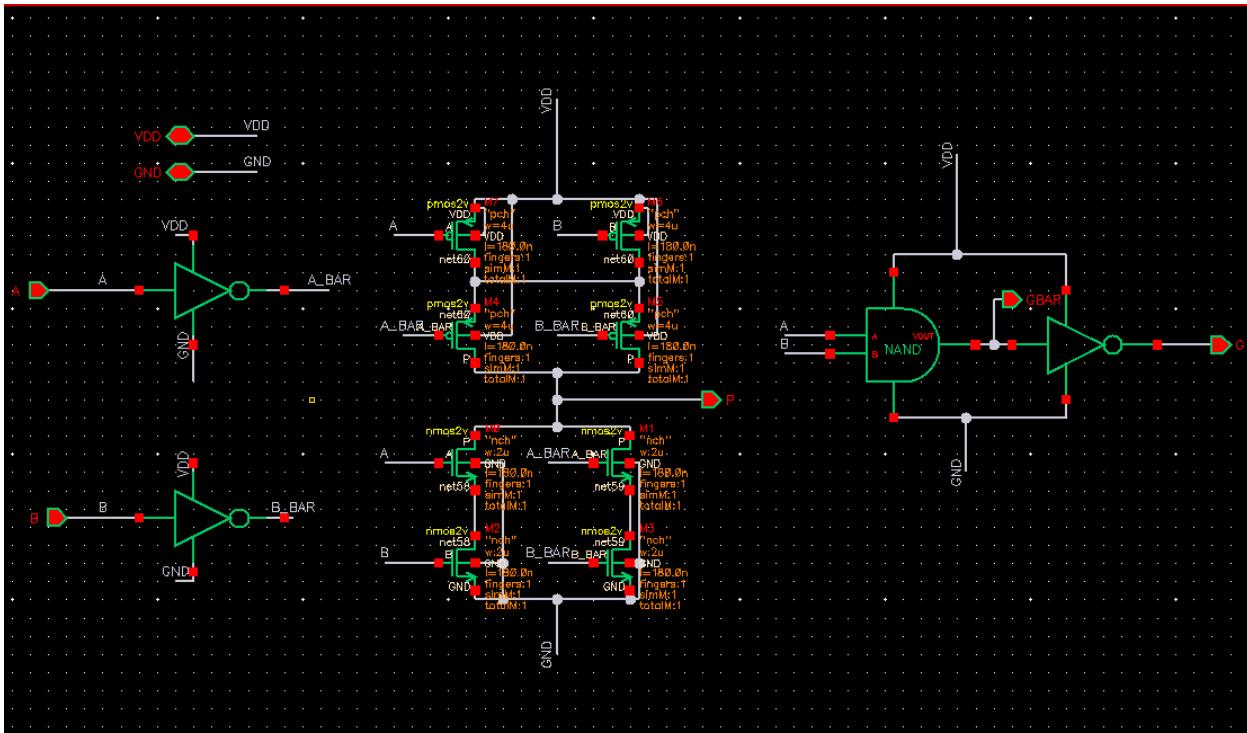
## NAND5



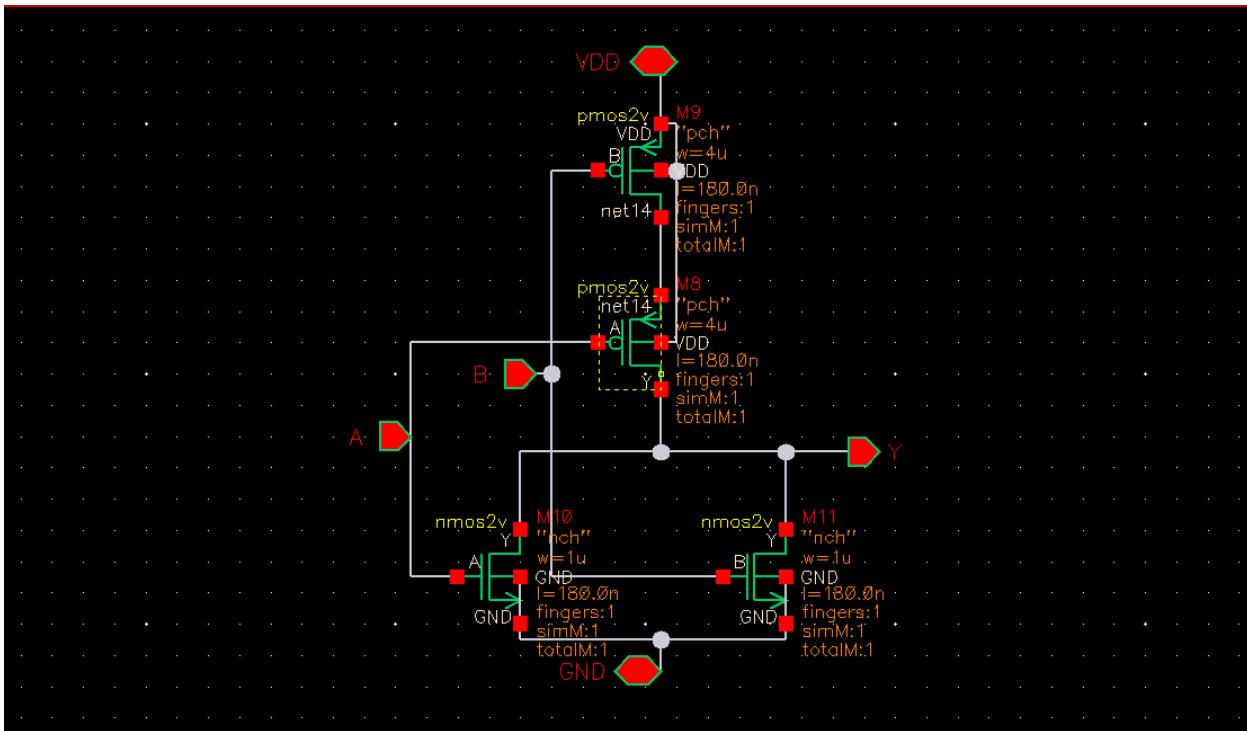
## NAND6



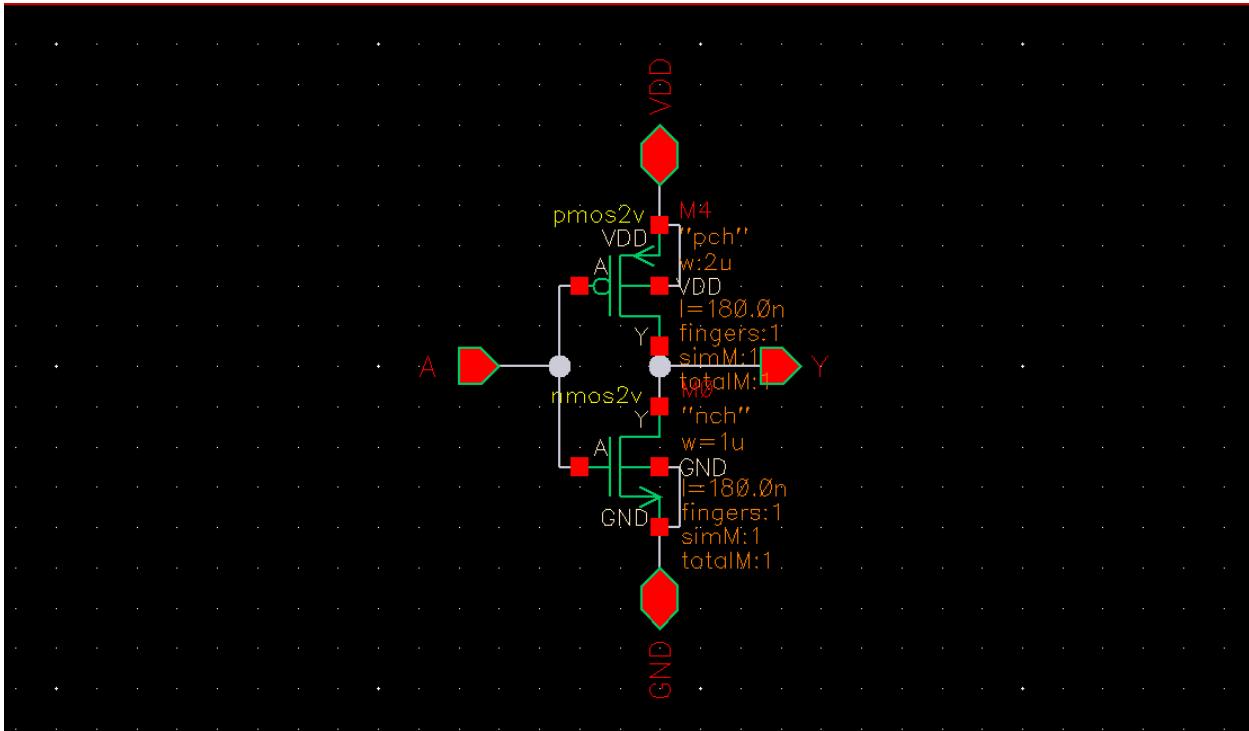
## HALF ADDER



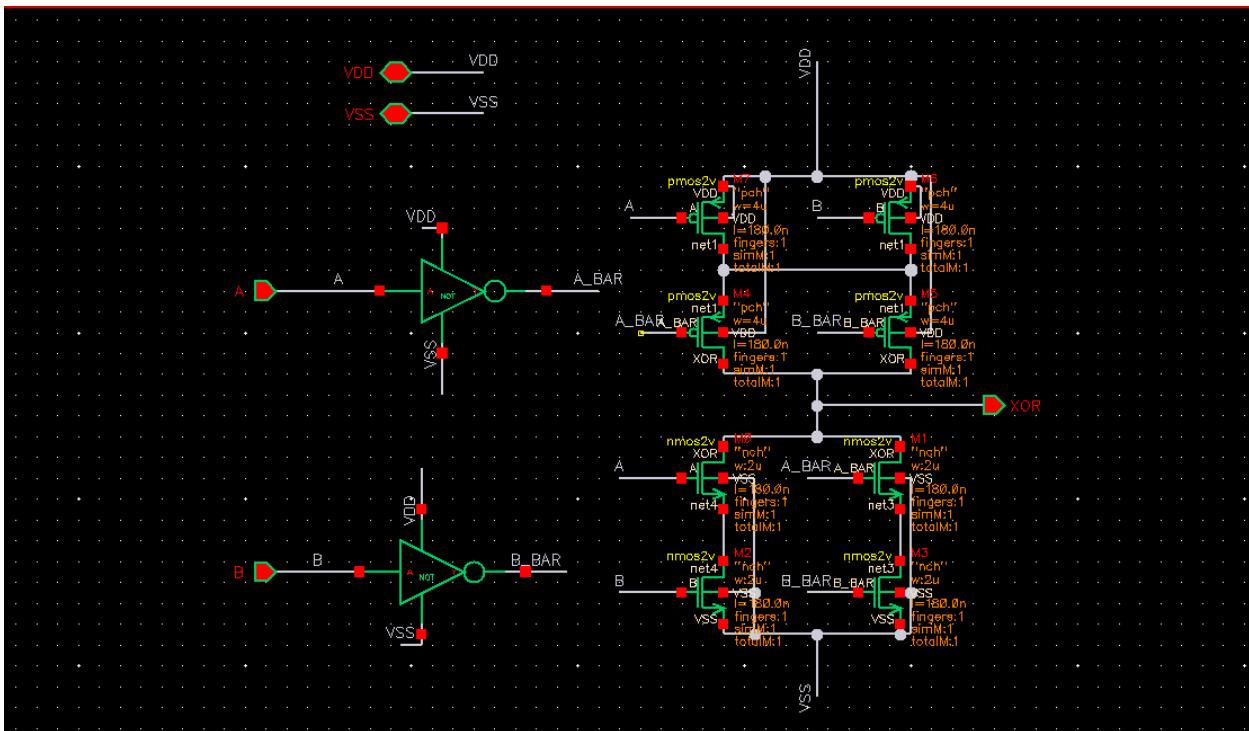
## NOR

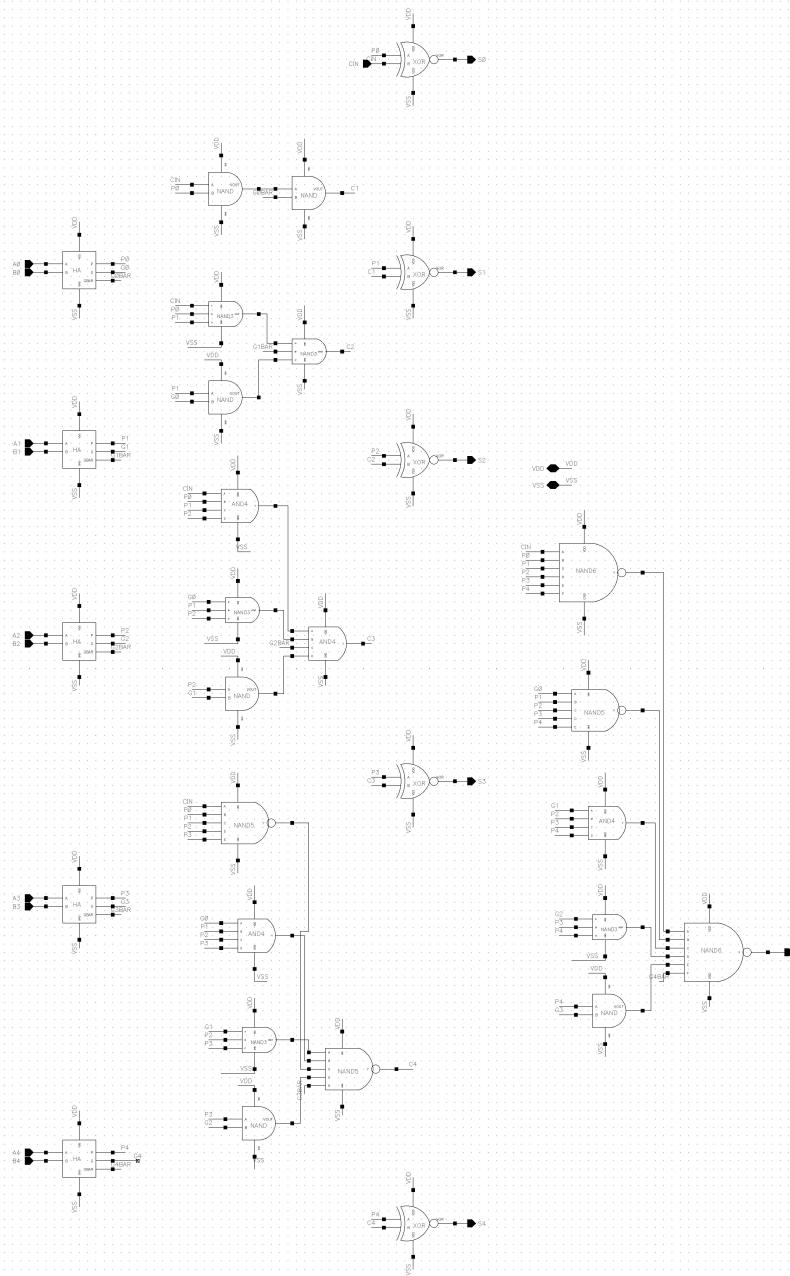


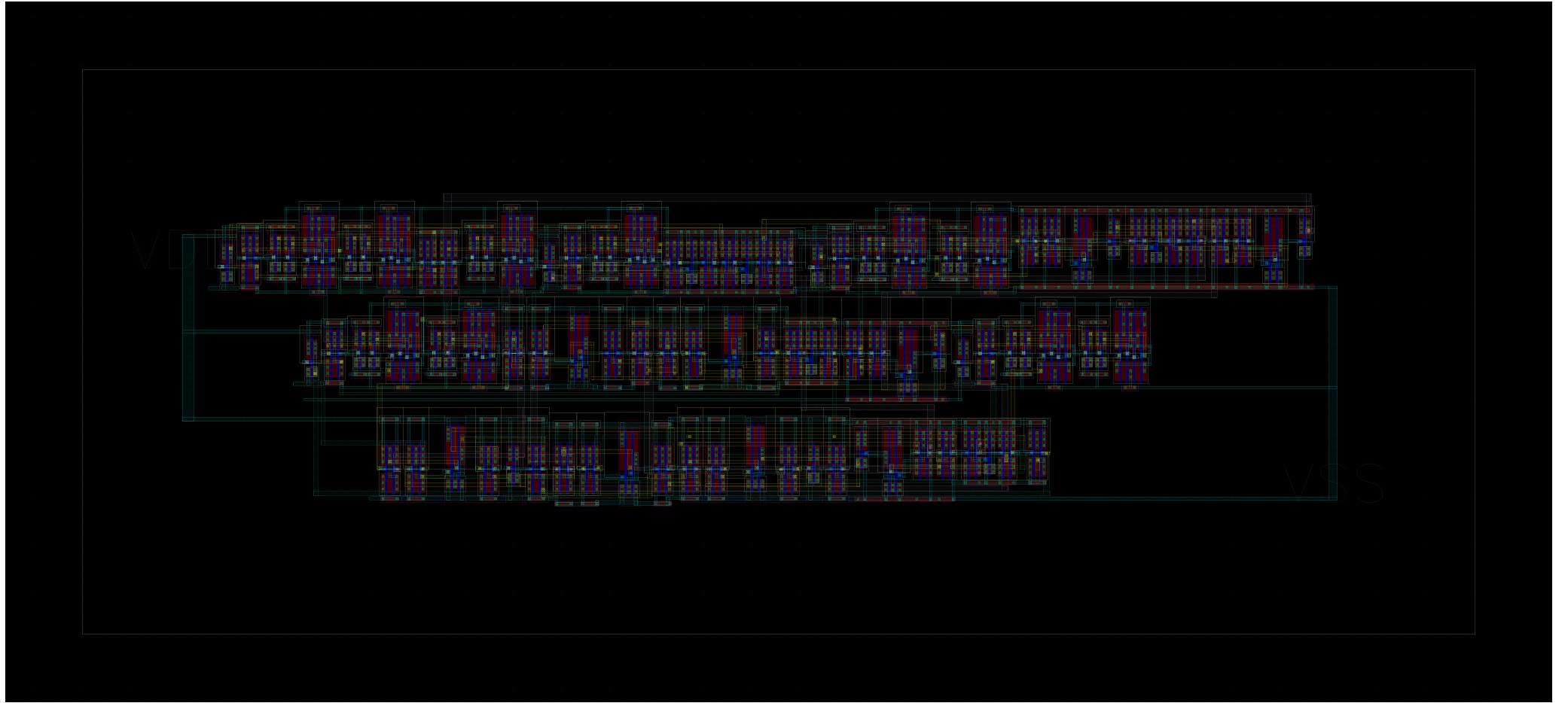
## NOT



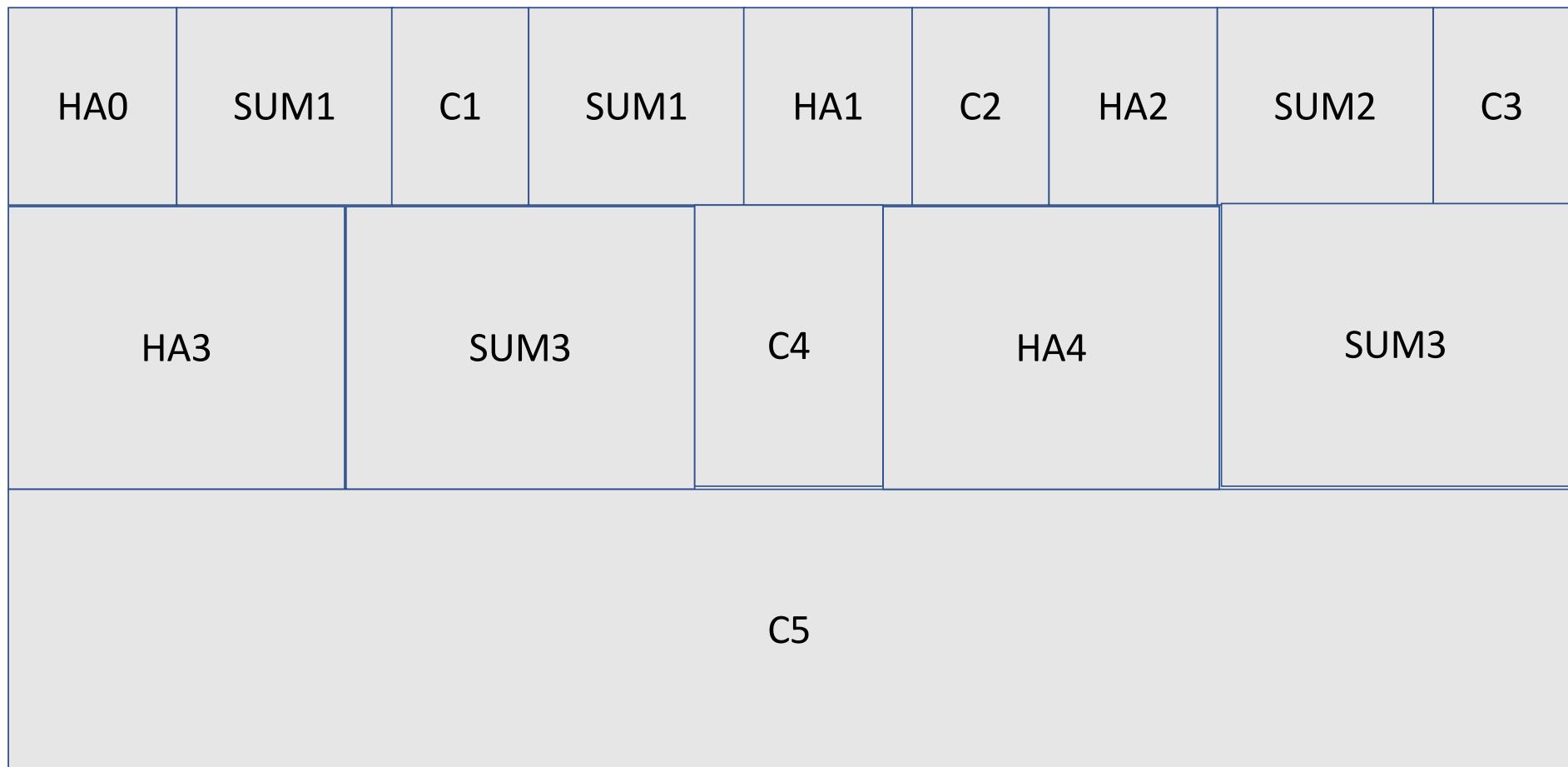
## XOR







# FLOOR PLAN



**HA**

NOT

NAND

NOT

NOT

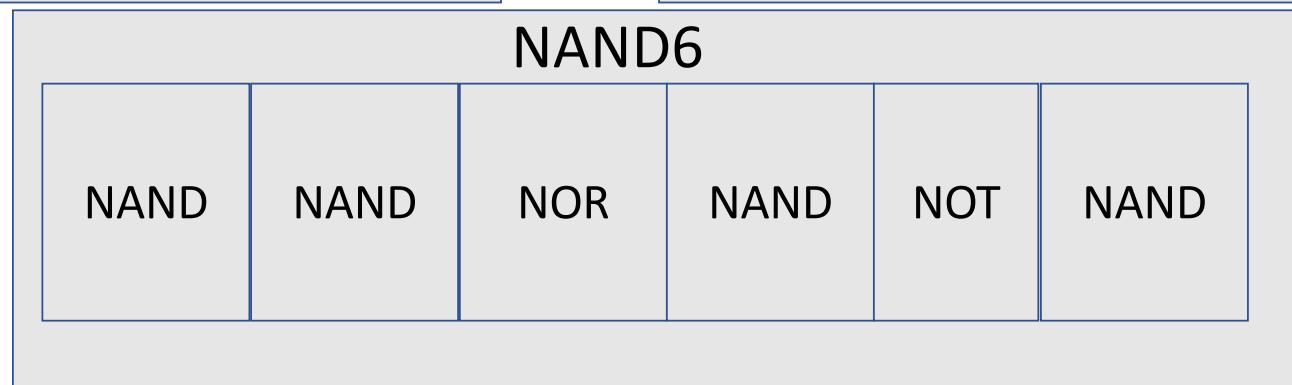
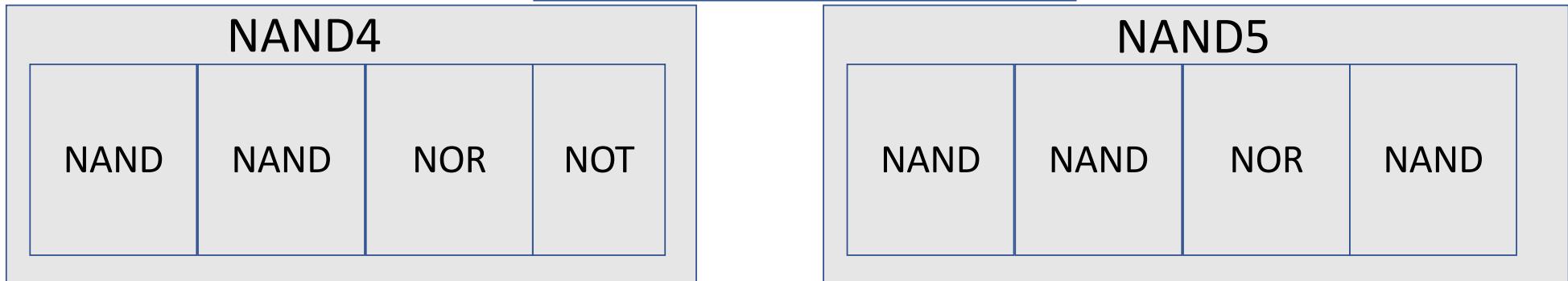
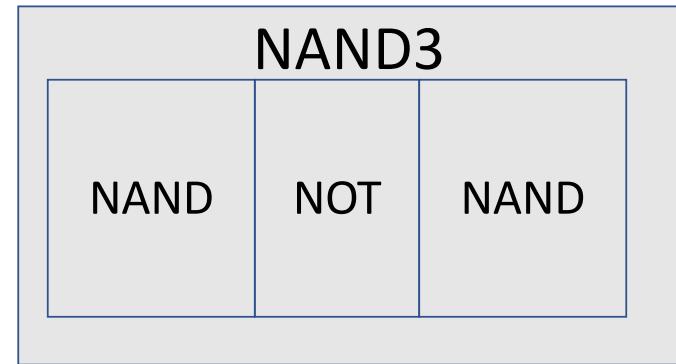
XOR

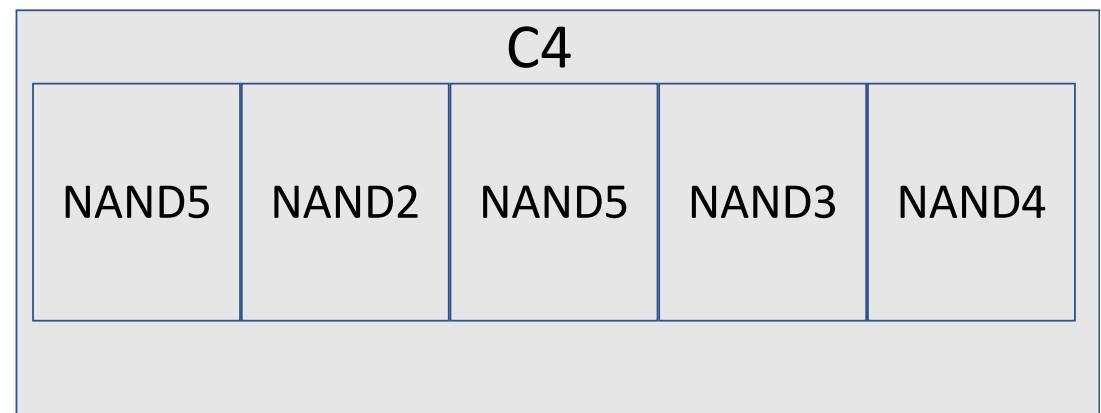
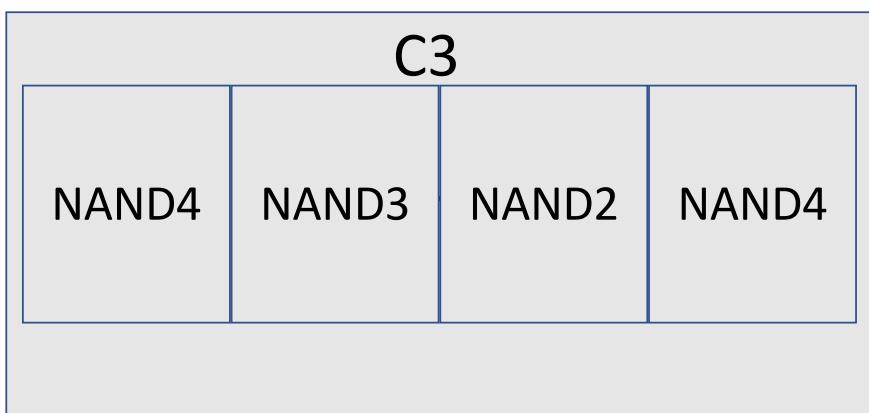
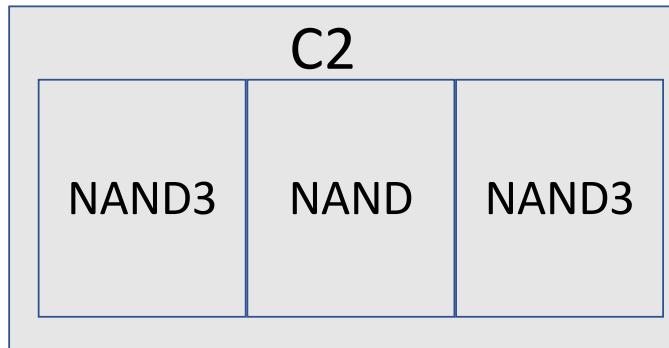
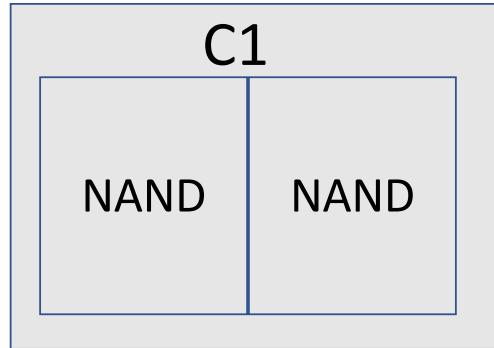
**SUM**

NOT

NOT

XOR





C5

NAND6

NAND5

NAND6

NAND4

NAND3

NAND2