Lab – 8

ECN – 252

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Part 1: 4-bit Multiplier

Design

```
module four_bit_multiplier(a,b,result);
  input [3:0] a, b;
  output [7:0] result;

  assign result = a*b;

endmodule
```

Testbench

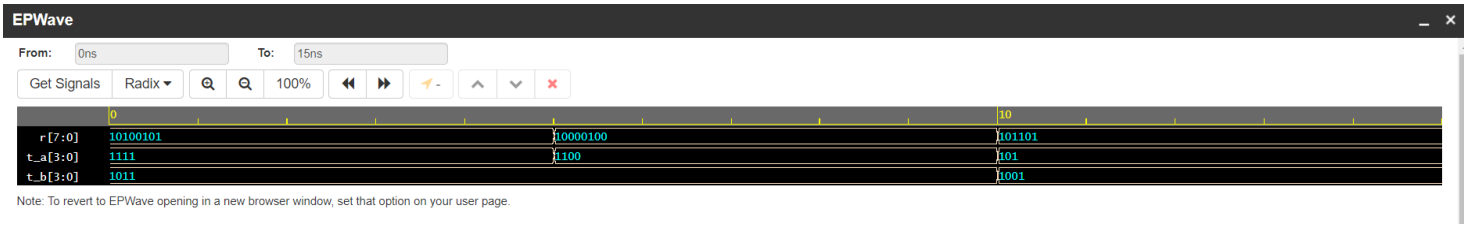
```
module testbench();
  reg [3:0] t_a,t_b;
  wire [7:0] r;

  four_bit_multiplier dut(.a(t_a) , .b(t_b) , .result(r));

  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end

  initial begin
    t_a= 4'b 1111;
    t_b= 4'b 1011;
    #5
    t_a= 4'b 1100;
    t_b= 4'b 1011;
    #5
    t_a= 4'b 0101;
    t_b= 4'b 1001;
    #5
    $finish();
  end
endmodule
```

Input - output waveforms



Part 2 : Positive edge triggered Toggle(T) flip-flop with an asynchronous set and an asynchronous reset

Design

```
module T_Flip_Flop( clk, set, reset, t, q, qb);

  input clk;
  input set;
  input t;
  input reset;

  output reg q;
  output qb;

  assign qb = ~q;

  always @(posedge clk or posedge reset or posedge set)
    begin
      if(reset) begin
        q <= 0;
      end else if(set) begin
        q <= 1;
      end else begin
        if(t) begin
          q = ~q;
        end
      end
    end
endmodule
```

Testbench

```
module testbench();
  reg clk;
  reg set;
  reg t;
  reg reset;

  wire q;
  wire qb;

  T_Flip_Flop dut(.clk(clk), .set(set), .reset(reset),
.t(t), .q(q), .qb(qb));

  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end

  always #5 clk = ~clk;

  initial begin
    clk <= 0;
    t <= 0;
    reset <= 0;
    set <= 1;
     #3
    reset = 0;
    set = 0;
     t = 1;
    #3
    reset = 0;
    set = 0;
     t = 1;
    #3
    reset = 0;
    set = 0;
    t = 0;
    #3
    reset = 0;
    set = 0;
    t = 1;
    #3
```

```
    reset = 0;
    set = 0;
    t = 1;
    #3
    reset = 0;
    set = 0;
    t = 0;

    $finish();
  end

endmodule
```

Input - output waveforms