ECN-252 Lab 10

You need to submit the codes for the design/module as well as the testbench, along with a snapshot of the input-output waveforms. Please put these three things in **a single .pdf file.**
You can also add text-files for the codes if you want, but it is not necessary. If you do so, submit a zip including the pdf and the text files.

The submission should be named as your roll no., following the same custom as all previous labs.

NOTE:

1. Do not paste snapshots of code. Please copy the code in text mode. This will allow us to easily copy your code into our testbench for checking. Any submission with snapshots of code (i.e., where the code text cannot be directly copied) will incur a **penalty of 1 mark for each of the Parts independently.**
2. Any error in the report is an error, even if the implementation is correct. Such cases will incur **penalties based on the number and severity of errors.**

Part-1:

Design an ALU using Verilog. The ALU takes two inputs A and B. Each of these are 4 bit numbers. A third input called SEL determines the operation to be performed on A and B. The output OUT gives the results (including carry, if any)

SEL	**Operation**
000	OUT=0
001	Addition (A+B)
010	Multiplication (A*B)
011	Rotate left (only A)
100	Rotate right (only A)
101	Greater than comparison (Returns 1 if A>B, else 0)
110	Equal comparison (Returns 1 if A==B, else 0)
111	OUT=1

For the testbench, use A=1100, B=1011. Show the output for all SEL inputs.

Deadline: 12 May 11:59 pm.

Hints:

You can use “case()” statement to make things easier.

```
begin
    case (SEL)
        3’b000: <statement>
        3’b001: <statement>
        --
        default: <statement>
 end case
```

For rotations: 1011 rotated left once becomes 0111. Rotated a second time it becomes 1110 and so on. The opposite happens when rotated right i.e, 1011 roated right once becomes 1101. For these rotations, note that {A[0],A[3:1]} is a four bit number with the digit order as A[0]A[3]A[2]A[1].

For greater than and equal comparisons, you can use ternary operators written as

<Query>?[if true]:[if false]

For example, OUT=(A<B)?4’b0110:4’b0011 means OUT=0110 if A<B, else OUT=0011. You can also use if-else conditions.

For test-bench design you can use a for loop for SEL, like

```
for (k=0;k<=7;k=k+1)  begin
     SEL = SEL + 3'b001;
     #10;
 end
```

NOTE that “k” needs to be defined as an integer. Syntax: integer k;