ECN-252 Lab 8

You need to submit the codes for the design/module as well as the testbench, along with a snapshot of the input-output waveforms. Please put these three things in **a single .pdf file.**

The pdf file should be named as your roll no., following the same custom as all previous labs.

NOTE:

1. Do not submit zipped folders with multiple files. *Only submit one .pdf file with the codes and waveform.*
2. Do not paste snapshots of code. Please copy the code in text mode. This will allow us to easily copy your code into our testbench for checking. Any submission with snapshots of code (i.e., where the code text cannot be directly copied) will incur a **penalty of 1 mark for each of the Parts independently.**
3. Any error in the report is an error, even if the implementation is correct. Such cases will incur **penalties based on the number and severity of errors.**

Part-1:

Use Verilog to design a four-bit multiplier at the behavioral level. Design a testbench to show the output for

(a) 1111 x 1011

(b) 1100 x 1011

(c) 0101x 1001

Part-2:

Use Verilog to design a positive edge triggered Toggle(T) flip-flop with an asynchronous set and an asynchronous reset. Design a testbench to show successful operation.

Deadline: 18 April 11:59 pm.