ECN-252 Lab 9 Design using VHDL

This assignment is based on VHDL programming. Use the same browser-based simulator available at www.edaplayground.com. But use VHDL option for this assignment (will be explained during tutorial).

Submit one zip file that includes the following – (1) testbench and design copied into separate text files for each problem below. (2) Report - should include your explanation, waveform screenshots and any other notes that you want to include.

During tutorial, basic design process will be explained. Then you'll design two circuits below.

Part 1:
Design a 4-bit full adder using structural description of the architecture, using 1-bit full adders as the building block. The 1-bit full adder should be designed with only NAND-gates using structural description. The NAND gates should be designed with behavioral description. Demonstrate 4-bit full adder operation using suitable test bench (no need to show all combinations). Assume unsigned integer for all cases. ~~What would be the worst-case delay in the 4-bit full adder for the carry out bit and the sum if a delay of 1 ns is included in the NAND gate? Write down your explanation. Demonstrate/verify this worst-case delay calculation by setting the testbench accordingly. [Marks: 2(full adder design) +1(explain worst case delay) +3(demonstrate worst case delay)]~~

Now assume 1 ns delay implemented in the NAND gate. What would be the delay for the sum and carry-out bits to settle *for the 1 bit full adder*, given the input transition from $a = 0, b = 0, cin = 0$ to $a = 1, b = 0, cin = 1$. Explain your observation using a test bench. [Marks: 2(full adder design) +4(explain and demonstrate the scenario with gate delay)]

(Check out this link – slides 7 and 9 - https://nptel.ac.in/content/storage2/courses/117106114/Week9%20Slides/9.3Adder.pdf to learn the delay calculation if you are not familiar with this kind of calculation)

Part 2: (adapted from Digital Design book by Mano.)
Design, construct, and test a two-bit counter that counts up or down. **ECE: design and demonstrate the UP counter. CSE: design and demonstrate the down counter.** An enable input E determines whether the counter is on or off. If E = 0, the counter is disabled and remains at its present count even though clock pulses are applied. If E = 1, the counter is enabled. For the UP counter, the circuit counts upward with the sequence 00, 01, 10, 11, and the count repeats, at the rising edge of the clock signal. For the down counter, the circuit counts downward with the sequence 11, 10, 01, 00, and the count repeats, at the rising edge of the clock signal. Do not use E to disable the clock. Design the sequential circuit for the counter using behavioral description in VHDL with E and the clock as inputs, count value as the output. Be sure to design a testbench that captures the function of input E. (Marks 4)