Lab – 10

ECN – 252

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Part 1 :

Design

```
module Four_Bit_ALU(A, B, Select, Output, Flag_carry);

input [3:0] A,B;
input [2:0] Select;
output [7:0] Output;
output Flag_carry;
reg [7:0] Result;
assign Output = Result;
assign Flag_carry = Result[4];

always @(*)

begin
case(Select)
    // Zero OUT
    3'b0000:
        Result = 4'd0 ;
    // Addition
    3'b0001:
        Result = A + B ;
    // Multiplication
    3'b0010:
        Result = A * B;
    // Rotate left
    3'b0011:
        Result = {A[2:0],A[3]};
    // Rotate Right
    3'b0100:
        Result = {A[0],A[3:1]};
    // Greater Than
```

```verilog
        3'b0101:
            Result = (A>B)?4'd1:4'd0 ;
        // Equal To
        3'b0110:
            Result = (A==B)?4'd1:4'd0 ;
        // Rotate right
        3'b0111:
            Result = 4'd1 ;

default:
    Result = 4'd0 ;
endcase

end
endmodule
```

Testbench

```verilog
`timescale 1ns / 1ps
module Four_Bit_ALU_TB;

reg[3:0] A_TB,B_TB;
reg[3:0] Select_TB;

wire[7:0] OUT_TB;
wire Flag_carry_TB;

integer i;
Four_Bit_ALU uut(
    .A(A_TB),
    .B(B_TB),
    .Select(Select_TB),
    .Output(OUT_TB),
    .Flag_carry(Flag_carry_TB)
);

initial begin
    $dumpfile("dump.vcd");
    $dumpvars;
```

```
        end

        initial begin
            A_TB = 4'b1100;
            B_TB = 4'b1011;
            Select_TB = 4'b0;
            #20;
            for (i=0;i<=6;i=i+1)
                    begin
                    Select_TB = Select_TB + 1'b1;
                    #20;
            end;
        end

        endmodule
```

WaveForm

A = 1100 , B = 1011