Implementing MMD algorithm for Reversible Logic Synthesis on Parallel Machine

Abhinav Tallapally
Columbia University
Department of Electrical Engineering
at2769@columbia.edu

Adil Sadik
Columbia University
Department of Electrical Engineering
ams2378@columbia.edu

1.INTRODUCTION:

Reversible circuit has same number of input and output and, it can generate a unique output vector from each input vector and vice versa. The traditional logic gates (AND, OR, XOR) are irreversible as it is not possible to recover the input bits from the output bit. In other words, irreversible circuit lose information bits. With each bit of lost information, $K_T$log2 joules of hear is generated regardless of underlying technology [1]. This energy dissipation would not occur if the computation is carried out in a reversible way[2]. When a logic operation is performed with irreversible logic gates, the computer erase information and it give rise of heat dissipation which can reduce the life of the circuit.

Moore's law assets that processing power doubles every 18 months. Reversible logic doesn't erase information and thus it dissipate much less hear. So there are compelling reasons to consider circuits designed in reversible way as it has the potential to offer greater benefit over irreversible circuits especially in case of high speed power aware devices. Reversible circuits are of high interest in low-power CMOS design, optical circuits along with applications in digital signal processing, communication, computer graphics and cryptography, and more importantly in quantum computing [4]. With promising developments in realization of quantum computing and projections of it being the future of computing, doing work on synthesis tools for it can make us prepared for rapid adaptation of it into everyday computing.

2.REVERSIBLE LOGIC SYNTHESIS

Developing efficient Logic synthesis algorithms is the first step toward synthesis reversible circuits. The synthesis process of reversible circuits differ significantly than the irreversible gates. Therefore logic design of irreversible circuits is a new and challenging task. Several ideas and algorithms have been proposed [5][6][7] for reversible logic synthesis. From the nature of these algorithms, these are heuristic type in nature and tremendously computation intensive and the improvement of the quality of the solution can be seen with increase in the execution time of the algorithm.

Hence, attempts are currently being made to implement the algorithm on multi-cores, gpu units so as to gain execution time and invest it in improving the results further. One such attempt is [8], where the algorithm has been implemented on a GPU and multi-core processor and results of both are evaluated and compared against standard benchmarks.

We propose to implement the MMD algorithm [9] using MPI/Pthreads in C++ for multi-core processor environment. It is planned to evaluate the results of our implementation with that reported by the paper [9] in quality and runtime being the evaluation parameters. We expect to achieve similar if not better results than the Cell implementation in the same paper.

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