

A Special Section on Multicore Parallel CAD: Algorithm Design and Programming

KURT KEUTZER, University of California, Berkeley

PENG LI, Texas A&M University

LI SHANG, University of Colorado, Boulder

HAI ZHOU, Northwestern University

ACM Reference Format:

Keutzer, K., Li, P., Shang, L., and Zhou H. 2011. A special section on multicore parallel CAD: Algorithm design and programming. *ACM Trans. Des. Autom. Electron. Syst.* 16, 3, Article 21 (June 2011), 2 pages. DOI = 10.1145/1970353.1970354 <http://doi.acm.org/10.1145/1970353.1970354>.

High-performance parallel computer architecture and systems have improved at a phenomenal rate. Meanwhile, VLSI Computer-Aided Design (CAD) software for multibillion-transistor IC design has become increasingly complex and requires prohibitively high computational resources. Recent studies have shown that numerous CAD problems with their high computational complexity can greatly benefit from the increasing parallel computation capabilities. However, parallel programming imposes big challenges for CAD applications. A full exploration of the computational power of emerging general-purpose and domain-specific multicore/many-core processor systems calls for fundamental research and engineering practice across every stage of parallel CAD design, from algorithm exploration, programming models, design-time and runtime environment, to CAD applications, such as verification, optimization, and simulation.

Included in this journal special section is some recent progress on parallel CAD research, including algorithm foundations, programming models, and parallel architectural-specific optimization. Specifically, we have selected nine articles among all the submissions. They can be categorized into four groups based on the problems they solve and the parallel architectures they employ. Problems they attack include design optimization and simulation/analysis; employed architectures are either general multicore processors or Graphics Processing Units (GPUs).

The first article, “Efficient and Deterministic Parallel Placement for FPGAs”, is on design optimization on general multicore processors. The second and the third

Authors’ address: K. Keutzer, EECS Department, University of California, Berkeley, 566 Soda Hall, Berkeley, CA 94720; email: keutzer@eecs.berkeley.edu; P. Li, Department of Electrical and Computer Engineering, Texas A&M University, 333M WERC, 3259 TAMU, College Station, TX 77843; L. Shang, EECE Department, University of Colorado, Boulder, CO; H. Zhou, Department of Electrical Engineering and Computer Science, Northwestern University, 2145 Sheridan Road, Evanston, IL 60208-3118.

Permission to make digital or hard copies of part or all of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies show this notice on the first page or initial screen of a display along with the full citation. Copyrights for components of this work owned by others than ACM must be honored. Abstracting with credit is permitted. To copy otherwise, to republish, to post on servers, to redistribute to lists, or to use any component of this work in other works requires prior specific permission and/or a fee. Permissions may be requested from the Publications Dept., ACM, Inc., 2 Penn Plaza, Suite 701, New York, NY 10121-0701 USA, fax +1 (212) 869-0481, or permissions@acm.org.

© 2011 ACM 1084-4309/2011/06-ART21 \$10.00

DOI 10.1145/1970353.1970354 <http://doi.acm.org/10.1145/1970353.1970354>

articles, “Design and Implementation of a Throughput Optimized GPU Floorplanning Algorithm” and “GPU-Based Parallelization for Fast Circuit Optimization”, are on design optimization on GPU platforms. The next four articles, “Multithreaded Simulation for Synchronous Dataflow Graphs”, “Accelerating UNISIM-Based Cycle-Level Microarchitectural Simulations on Multicore Platforms”, “A New Algorithm for VHDL Parallel Simulation”, and “Locality-Driven Parallel Static Analysis for Power Delivery Networks”, deal with simulation and analysis on multicore processors. Finally, the last two articles, “Massively Parallel Logic Simulation with GPUs” and “Gate-Level Simulation with GPU Computing”, discuss how to speed up simulation on GPU platforms.