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Hardware Design of Approximate Matrix Multiplier based on FPGA in Verilog

Ankit Gupta
Dept. of Electronics and Communication Engineering
Delhi Technological University
New Delhi, India
ayangupta137@gmail.com

Kriti Suneja
Dept. of Electronics and Communication Engineering
Delhi Technological University
New Delhi, India
kritisuneja@dtu.ac.in

***Abstract*— Approximate computing has emerged as a new paradigm for the energy-efficient design of circuits and systems. It enables highly efficient hardware and software implementations by exploiting the inherent resilience of applications to in-exactness in their computations. In this work, hardware implementation of Matrix Multiplier based on approximate computing is modeled in VERILOG Hardware Description Language (HDL). The target device used for synthesis is xc7a100t-3csg324 in Xilinx. Simulations were performed in ISIM simulator and device utilization has been presented below.**

Keywords— approximate computing, matrix multiplier, Verilog, Field Programmable Array (FPGA), Look Up Tables (LUTs)

I. INTRODUCTION

Approximate computing has been emerging as a new revolution in the digital circuit world. It plays with the trade-off between the requirement of exact computing to improved area requirement, speed and power performance. Many important applications like computer vision, machine learning, big data analytics, web search, etc. can inherently tolerate a loss in accuracy and require the results faster. In applications involving signal/image processing and multimedia, exact computations are not always necessary and are often very heavy, and these applications are error-tolerant and produce results that are good enough for perception by the human eye. Hence, approximate computing can be used in such error-tolerant applications by reducing accuracy, but still providing meaningful results faster and/or with lower power consumption. In any system design, arithmetic units lie at the base and govern the Area and Time Consumption for the design. Thus they are one of the most ideal parts to implement approximate computing. Many papers in the past few years have shown the implementation of approximation in adders and multipliers

Exact computing is quite expensive in terms of energy and thus approximate adders and multipliers can prove to be efficient [1]. Following Moore's law, approximate computing has the potential to be the next step for VLSI [2] [3] [4]. In paper [5] they explained how approximating the carry output for a full adder can bring down the area and time consumption by including a minimal amount of error. Some papers also reveal the improvement in time consumption with breaking the carry propagation chain for the LSB part of the calculation [6] [7]. Approximate multipliers are more complicated and generally designed by using an approximation in the summation process of partial products [8] [9] [10].

Approximate matrix computing has been discussed in some previous studies but lacked hardware implementation which is the crux of this paper. Also using adders and multipliers together for approximation provides better control of error percentage

In this paper, a novel approximate matrix multiplier is presented with improved area and time requirements. The paper is structured as follows, II presents the architecture of the proposed design, III accommodates the results generated for the proposed design and IV comprises of the conclusion inferred from the experiment

II. PROPOSED ARCHITECTURE

A. Lower-Part OR-based Approximate Adder

One of the more common techniques for designing an approximate adder involves breaking the chain by segmenting the adder into 2 parts, the accurate part and the inaccurate part. The accurate part employs exact adders to calculate the MSBs while the inaccurate part is used to calculate the LSBs. In the proposed adder, the operands are divided into 2 equal halves. The upper part addition is carried out by a simple Ripple Carry Adder (RCA) while the lower part addition is carried out bit by bit using OR gates. Length of the inaccurate part depends on the requirements of the application. In this case, have taken the accurate and inaccurate block equal

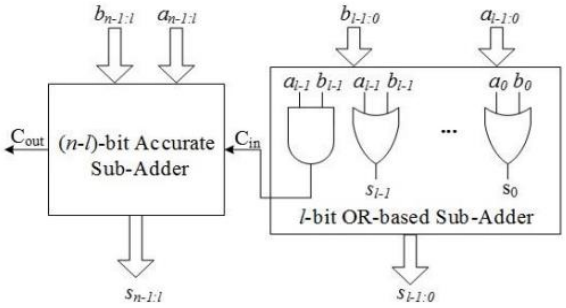


Fig 1 Lower-part OR Adder [11]

B. *Lower-Part OR-based Approximate Multiplier*

Multiplication is a complex process and is majorly responsible for the time consumption during any operation thus employing approximate computing in Multipliers can prove to be majorly fruitful in large scale operations. Multiplication can be divided into 2 procedural steps

- Partial Product Generation by employing bit by bit multiplication
- Summation of the partial products and generating the final result

Approximate Multipliers are generally designed by approximating the summation of partial products. In the proposed multiplier the summation process has been carried out by dividing the partial products into 2 blocks, accurate block for the MSBs and inaccurate block for the LSBs. The accurate block employs the famous Wallace Tree Multiplier Technique as shown in the figure below, for carrying out the summation process with speed and efficiency. The Inaccurate block employs OR gates to generate the final product for the lower part. The dividing strategy is based on numerous factors like Power consumption, delay and accuracy and can vary depending upon its application

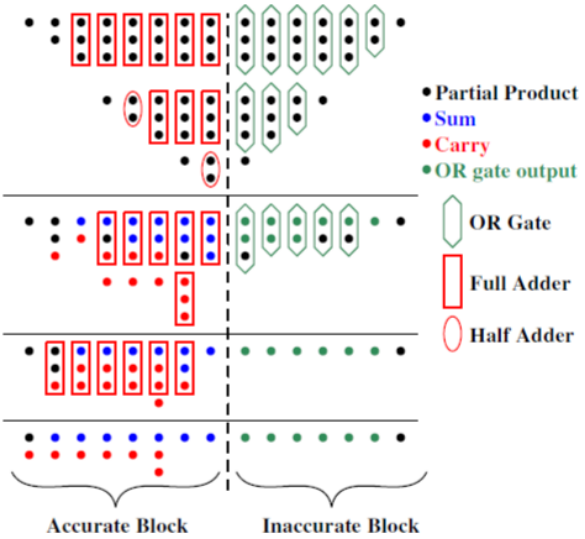


Fig 2 Lower-Part OR Wallace Tree Multiplier [12]

C. *Proposed Approximate Matrix Multiplier*

Finally, the proposed Approximate Adder and Approximate Multiplier are brought together to carry out the matrix multiplication and is compared with traditional Matrix Multiplier in terms of delay and Area used

III. TEST RESULT AND ANALYSIS

The unsigned matrix multiplication is implemented for a 3x3 8-bit matrix and compared the device utilization summary of the exact matrix multiplier comprising of Wallace Tree Multiplier and Ripple Carry Adder with our proposed design to verify the reduction in Time and Area consumption. The changes are also recorded in device utilization by varying the bit size of the matrix terms and the matrix size using Verilog HDL, logic and simulation is verified using Xilinx ISE 14.7.

Table 1 below shows the decrease in area and delay for the matrix multiplication by introducing a negligible amount of error in calculations by approximate computing. There is a fall of about 45% in requirement of slice LUTs and a decrease of about 25% in the delay.

Table 2 below shows the parabolic nature of the curve for the no. of LUTs with increasing bit size and the variations in the curve with increasing matrix size whereas Table 3 below shows the changes the amount of delay in the circuit with changing bit size and matrix size.

TABLE 1

Matrix Multipliers	Area (LUTs)	Delay (ns)	Error (%)
Exact Matrix Multiplier	3177	10.783	0
Proposed Matrix Multiplier	1809	8.377	0-1%

TABLE 2

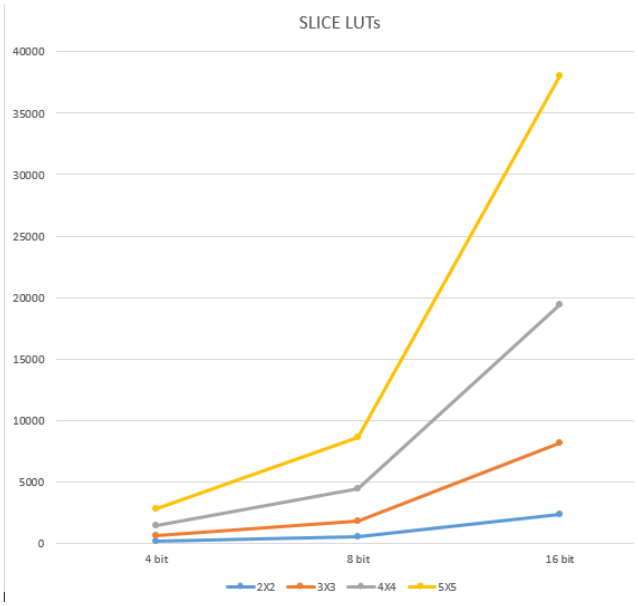
DATA BIT SIZE →

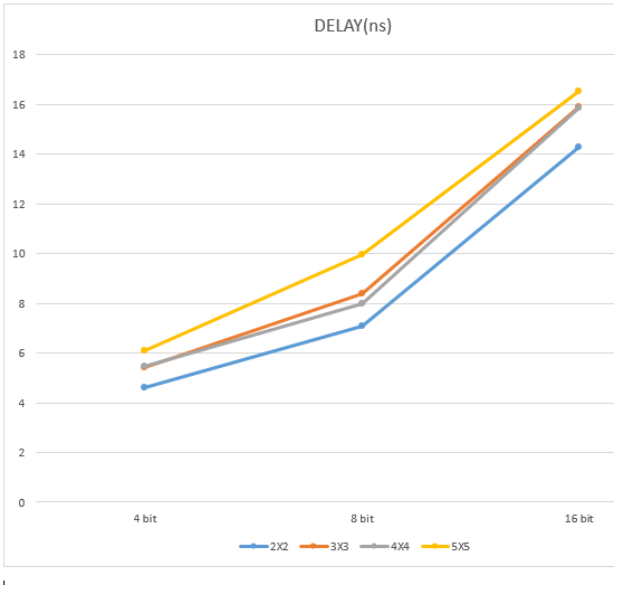
DELAY (ns)	4 Bit	8 Bit	16 Bit
2X2	4.612	7.099	14.282
3X3	5.438	8.377	15.902
4X4	5.449	7.987	15.85
5X5	6.101	9.963	16.517

TABLE 3

DATA BIT SIZE →

SLICE LUTs	4 Bit	8 Bit	16 Bit
2X2	176	524	2371
3X3	588	1809	8153
4X4	1469	4400	19391
5X5	2828	8650	37999





IV. CONCLUSION

The paper presents a novel approximate matrix multiplier structure employing the trade-off between precision and performance. It presents how to approximate computing can bring a significant improvement in the process of matrix multiplication by introducing a negligible amount of error. As per requirement degree of approximation can be changed thus it can have a huge amount of applications. Further studies can include ways of predicting the errors which can help approximate computing find its way to various fields like Signal Transmission and Data Encryption in the coming future.

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