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Implementation of Approximate Multiplier using Inexact Compressors

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Abstract- Nanoscale ICs required components with increased speed and less consumption of power. The trade-off between speed, area, and power is an important task. For the optimization of these parameters, approximate computing is used. In this paper, the approximate high-order compressor is implemented which is further used in partial product reduction of the multiplier. It is important to increase the computational parameters of the multiplication process. The performance of the multiplier increases by using compressors. In this paper, the authors proposed 9:2 compressor which helps in the reduction of the complexity of the circuit and increases the performance of the multiplication block. By applying compressors in the multiplication block, an energy-efficient multiplier is implemented. An energy-efficient multiplier can be further used in error-tolerant applications. The proposed approximated multiplier consumes 43.93% low power and area utilization 49.52 % less as compared to the exact multiplier. All the simulation is carried out in VIVADO 2018.3 using Verilog HDL coding.

Keyword- Approximate Computing, ***Compressor***, ***Multiplier***, ***Error-tolerant application***, ***Approximation.***

I. INTRODUCTION

Approximate computing is an approximation technique that reduced the computational time of the circuit with a small loss of output accuracy [1] [2]. This technique is used in those applications which tolerate some error and in these applications; arithmetic circuits play an important role [3]. In the literature, different types of techniques have been proposed to overcome the challenges faced by digital circuits [4] such as power consumption, latency, and so on [5]. Researchers are applying approximation techniques in digital circuits for a better trade-off between performance parameters [6]. The traditional partial product reduction method of multiplication block uses an exact computational method which increases the complexity of the circuit. But the approximate computing gives such relaxation, which helps in reducing the complexity and improving the performance of the digital circuits [7]. The multiplier is used as a fundamental block in error-tolerant applications [8]. The compressors are used for designing energy-efficient multiplier blocks [9]. By using compressors in the reduction step the performance of the multiplier is improved and an approximate multiplier is implemented. By applying approximation in multiplier, the performance parameter such as delay, area, and speed is improved [10]. In error-tolerant applications, the approximate multiplier plays a major role [11]. In different papers, different algorithms are proposed for the reduction of power consumption.

The authors in [3] proposed an approximate compressor to reduce the complexity of the circuit and error. The circuit is synthesized in 40nm CMOS technology. Reddy *et al*. [10] implemented a novel 4-2 compressor which was further used in the modified Dadda multiplier. The novel 4-2 compressor shows less error rate and error distance but the latency of the circuit increases. Guo *et al*. [12] designed an approximate multiplier using an inexact compressor. The inexact compressor is implemented with no-XOR gates for reducing the complexity of the circuits but errors also increase at the output. Authors in [13] proposed an 8×8 multiplier by using an exact 4:2 compressor at the reduction stage of partial products. The proposed design shows the low-power dissipation and high accuracy at the output but an increase in the latency. By using adders such as Kogge-stone at the reduction stage multiplier increases the power consumption of the multiplier block [14]. By using an exact compressor in the reduction stage of the multiplier, the hardware complexity of the overall circuit increases [15] [16].

For the reduction of partial products in multiplier the complexity increases in the conventional method. To reduce this complexity, the approximate circuits are proposed in this research paper, which helps in further designing the energy-efficient multiplier. Approximate computing probably has a great future

ahead of it. There's been some impressive work on using analog for approximate computing resulting 100× better power consumption and 10× price reduction.

Organization of paper: The proposed methodology of the paper is shown in Section II. After those results and discussion of approximate compressor and multiplier are shown in Section III and conclusion in Section IV.

II. PROPOSED METHODOLOGY

Approximate computing helps in improving the performance of circuits by sacrificing some accuracy [17]. Accuracy is the sacrifice for those applications which can tolerate some error and improve the overall performance of the circuits. In such types of applications, multiplication is an important operation [18]. Improving the computational performance of the multiplication block is a major task. Figure 1 shows the proposed methodology of the proposed approximated multiplier. For the implementation of the approximate multiplier, the compressor plays a crucial role. Compressors help in the reduction stage of the multiplications process. All the simulation for the implementation of approximate compressor and multiplier is done in VIVADO 2018.3.

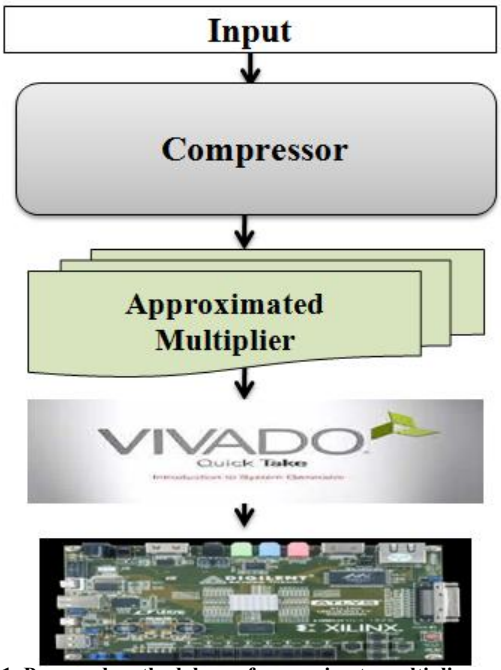


Fig. 1. Proposed methodology of approximate multiplier

A. Compressor

The compressor plays a crucial role in the multiplication process. So, it is important to boost the performance of the compressor. In this paper, an approximate 9:2 compressor is implemented using two approximated 4:2 compressors and one approximated 3:2 compressor. In comparison to the exact 9:2 circuit as shown in Fig. 2, the proposed 9:2 circuit shows less circuit complexity and low power consumption. The proposed 9:2 compressor is shown in Fig 3 consisting of nine inputs and four outputs. The carry outputs $Cout_1$ and $Cout_2$ of Fig 3 are evaluated using Eq. (1) and Eq. (2). The final *Sum* and *Carry* are expressed by Eq. (3), Eq. (4) respectively.

$$Cout_1 = ((x_4 + x_3).(x_2 + x_1)) + (x_4.x_3) + (x_2.x_1) \quad (1)$$

$$Cout_2 = ((x_7 + x_6).(x_5 + ((x_1 + x_2 + x_3) \oplus x_4))) + (x_7.x_6) + (x_5.((x_1 + x_2 + x_3) \oplus x_4)) \quad (2)$$

$$Sum = ((x_9 + ((((x_1 + x_2 + x_3) \oplus x_4) + x_5 + x_6) \oplus x_7)) \oplus x_8) \quad (3)$$

$$Carry = ((x_9 + ((((x_1 + x_2 + x_3) \oplus x_4) + x_5 + x_6) \oplus x_7)).x_8) \quad (4)$$

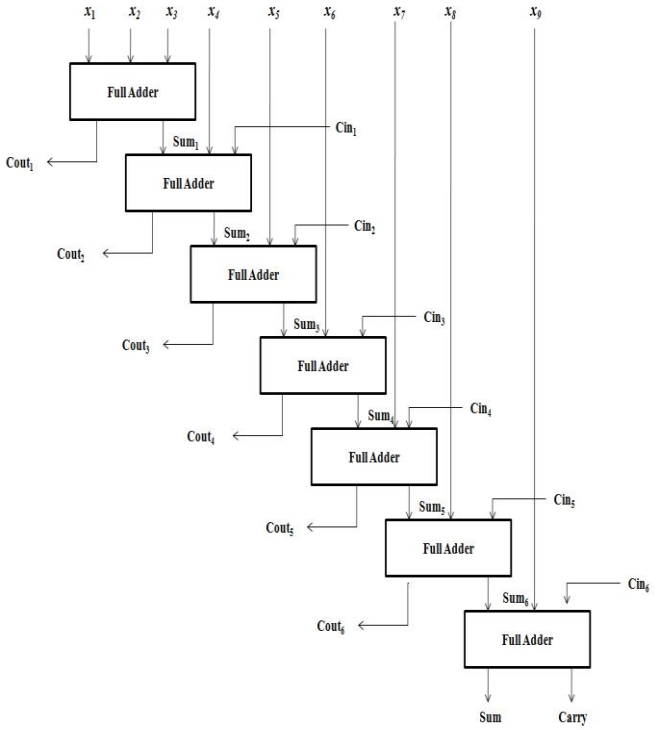
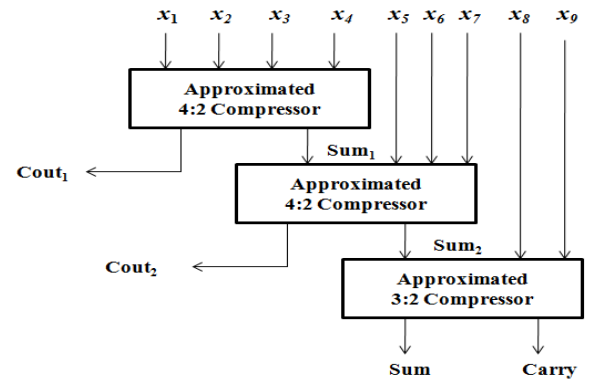
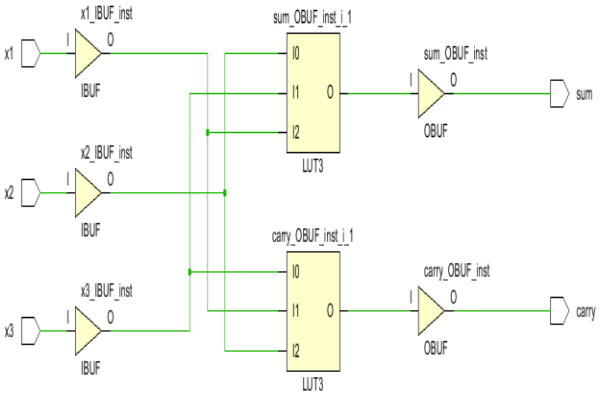


Fig. 2. Exact 9:2 Compressor



(a)



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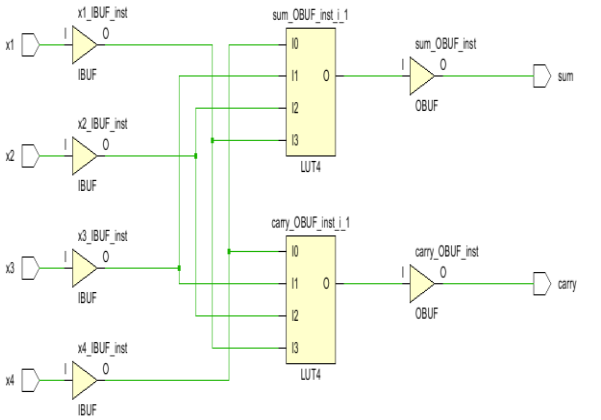


(c)

Fig. 3. (a) Block diagram of proposed 9:2 compressor (b) Circuit diagram of approximated 3:2 compressor (c) Circuit diagram of approximated 4:2 compressor

Figure 3 (a) consist block diagram of proposed approximate 9:2 compressor. In this block diagram approximated 3:2 compressor and approximated 4:2 compressor is used. The circuit diagram of approximated 3:2 compressor and approximated 4:2 compressor is shown in Fig. 3 (b) and Fig. 3 (c). The proposed approximated 9:2 compressor shows a less complex structure and reduces latency in comparison to the exact 9:2 compressor.

B. Multiplier

The multiplier consists of three modules for its fast multiplication process.

- Generation of partial product
- Reduction of partial products
- For the final computation Carry propagation adder

The second module that is the reduction of partial product in the most important module for designing the efficient multiplier. So, it is important to increase the performance of the second module. In this paper, the performance of the second module is increased by using compressors. The proposed and exact compressors are used for the implementation of the approximate multiplier. Figure 4 shows the generation of the partial product by multiplying two 9-bit inputs. After multiplying two 9-bit inputs, partial products are generated. Different *n*-bit compressors are used as shown in Fig. 5 for the reduction. By applying approximate compressors in the multiplication process an energy-efficient block is implemented.

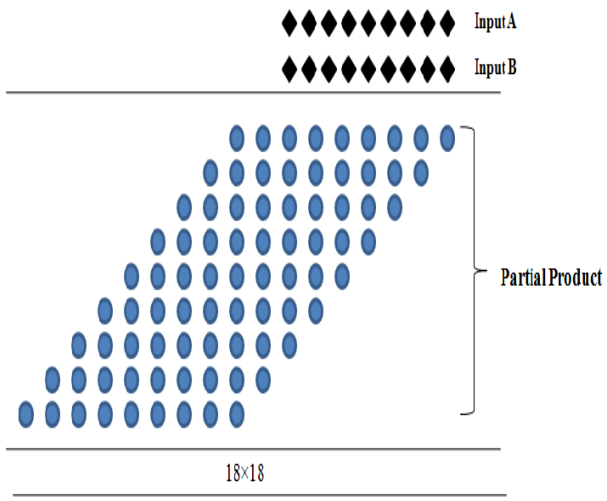


Fig. 4. Generation of partial products (9×9 multiplier)

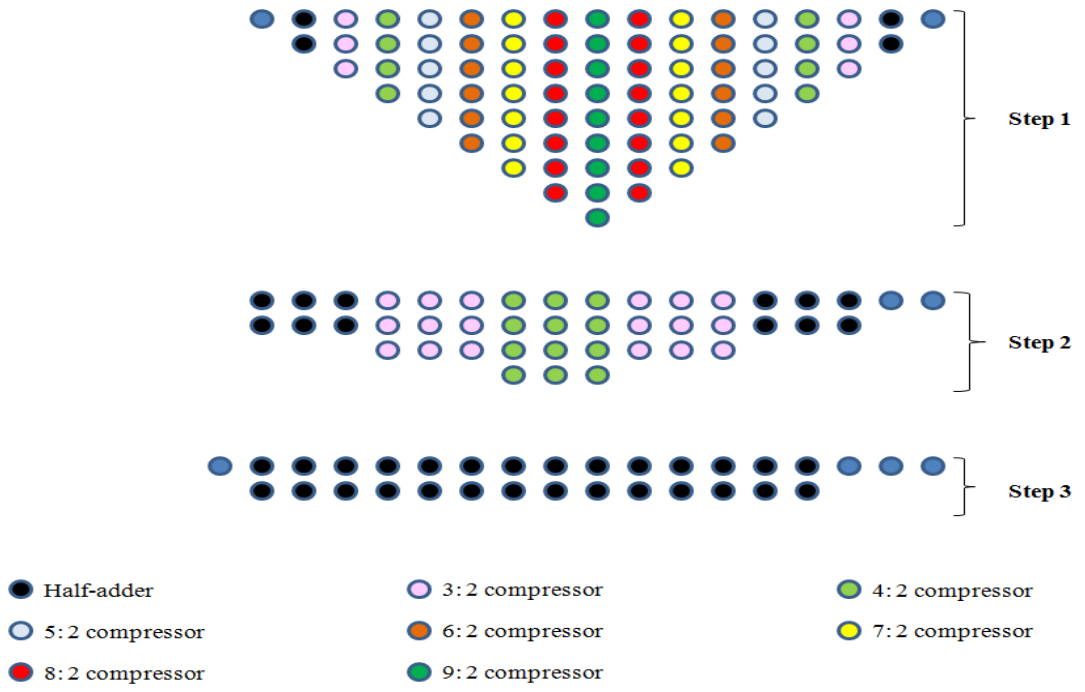


Fig. 5. Reduction of partial products using compressors

In this paper, the reduction of partial products using the exact compressor and proposed approximated compressor is done. In comparison to exact compressors, the approximated compressors show remarkable results and decrease the circuit complexity. The approximated compressors help in designing energy-efficient multiplication block.

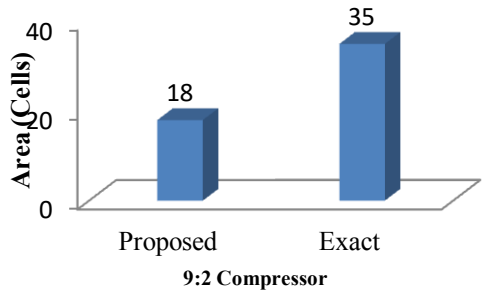
III. RESULTS AND DISCUSSIONS

Approximate multiplier plays a crucial role in those applications where inexactness in energy computing is tolerable. To increase the performance of the multiplier block, the approximate compressor is proposed and implemented in the multiplication block. All the implementation is done on VIVADO 2018.3 using Verilog HDL coding. Table 1 shows the result of the proposed and exact 9:2 compressor.

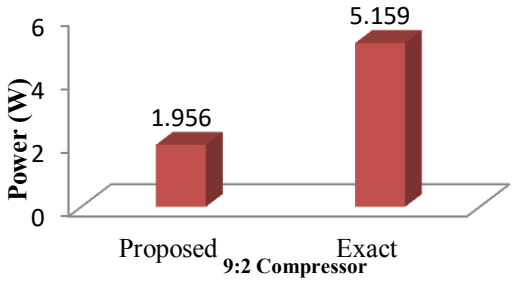
TABLE 1
RESULTS OF PROPOSED AND EXACT 9:2 COMPRESSOR

	Cell usage			Area	Memory (MB)		Power(W)			Junction Temperature (°C)	Thermal Margin (°C)
	LUT	IBUF	OBUF	Cells	Peak	Gain	Dynamic	Static	Total On-chip Power		
Proposed 9:2 Compressor	5	9	4	18	596.844	315.004	1.813	0.143	1.956	47.6	37.4 (3.1 W)
Exact 9:2 Compressor	12	15	8	35	597.520	315.426	4.832	0.326	5.159	84.5	0.5 (0.1 W)

Table 1 illustrated that the proposed 9:2 compressor consumes 62.08% low power and area utilization 48.57 % less regarding the exact 9:2 compressor. Figure 6 shows the area (cells) and power (W) graph of the 9:2 compressor. The compressor increases the performance of the multiplication block.



(a)



(b)

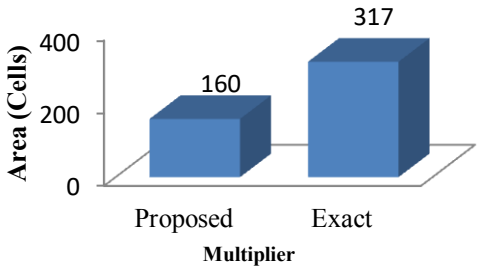
Fig. 6. 9:2 compressor (a) Area (Cells) (b) Power (W)

Figure 6 (a) shows the 9:2 compressor graph of area (cells). The area graph shows the comparison of the proposed and exact 9:2 compressor. The proposed 9:2 compressor takes less area (18 cells) for its computation in comparison to the exact 9:2 compressor area (35 cells). Figure 6 (b) shows the 9:2 compressor graph of power (W). The power graph shows the comparison of the proposed and exact 9:2 compressor. The proposed 9:2 compressor consumes less power (1.956 W) for its computation in comparison to exact 9:2 compressor power (5.159 W). Table 2 tabulates the result of the proposed and exact 9-bit multiplier. This table shows the results of different parameters that include cells usage, area utilization, memory, power consumption, temperature, and thermal margin.

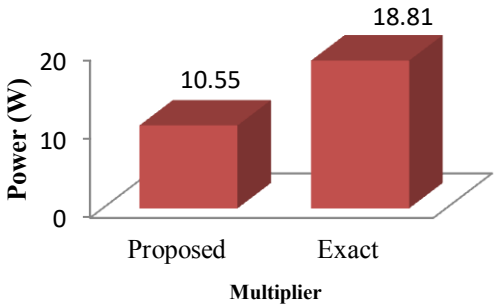
TABLE 2
RESULTS OF PROPOSED AND EXACT MULTIPLIER

9-Bit	Cell usage			Area	Memory (MB)		Power(W)			Junction Temperature (°C)	Thermal Margin (°C)
	LUT	IBUF	OBUF	Cells	Peak	Gain	Dynamic	Static	Total On-chip Power		
Multiplier using proposed compressor	133	9	18	160	617,809	335.715	9.511	1.039	10.55	125.0	-61.7 (-4.6 W)
Multiplier using exact compressor	280	17	20	317	671.387	389.223	17.778	1.039	18.81	125.0	-157.0 (-12.9)

Table 2 illustrated that the proposed multiplier consumes 43.93% low power and area utilization 49.52 % less, regarding the exact multiplier. Figure 7 shows the area (cells) and power (W) graph of the multiplier.



(a)



(b)

Fig. 7. 9-Bit multiplier (a) Area (Cells) (b) Power (W)

Figure 7 (a) shows the 9-bit multiplier graph of area (cells). The area graph shows the comparison of the proposed and exact 9-bit multiplier. The proposed 9-bit multiplier takes less area (160 cells) for its computation in comparison to the exact 9-bit multiplier area (317 cells). Figure 7 (b) shows 9-bit multiplier graph of power (W). The power graph shows the comparison of the proposed and exact 9-bit multiplier. The proposed 9-bit multiplier consumes less power (10.55 W) for its computation in comparison to the exact 9-bit multiplier power (18.81

W). The proposed multiplier shows remarkable results and can be further used in error-tolerant applications.

IV. CONCLUSION

In this paper, a novel design of approximated 9:2 compressor is presented. The proposed 9:2 compressor consumes 62.08% low power and area utilization 48.57 % less regarding the exact 9:2 compressor. Further, the approximated compressors are implemented in the multiplication process for designing of energy-efficient multiplication block. The reduction of partial products using the exact computational method increases power dissipation and the complexity of the circuit. So, the approximated multiplier is implemented using different types of approximated compressors. All the simulation is done in VIVADO using Verilog HDL coding. The energy-efficient multiplier is implemented in this paper and consumes 43.93% less power, 49.52 % less area utilization. In comparison to the exact multiplier, the multiplier using approximate computing shows advantageous results. In the future, an approximate multiplier further implements in applications that tolerate some errors.

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