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Energy Efficient Approximate Multiplier Design for Image/Video Processing Applications

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***Abstract*—An energy-efficient approximate multiplier is designed by using an approximate compressor for image and video processing applications. This paper proposes an approximate 4:2 compressor design with an 18.75% error rate that consumes on an average 15% less energy compared with the existing designs from the literature. This paper proposes two variants of the multiplier, one with only approximate compressors and another one with approximate and accurate compressors.**

***Index Terms*—Energy Efficient Multiplier, Approximate Computing, Approximate 4:2 Compressor, Image/Video Processing applications.**

I. Introduction

APROXIMATE hardware-based computing is an emerging area for energy-efficient hardware design. Many real-life applications can be implemented using these approximate hardware. The applications that can tolerate errors in their output are the best suited for this kind of implementation. Signal processing, Image processing, and Video processing applications are best suited for approximate computing, and thereby one can reduce significant energy, delay, power, and area. The majority of the hardware will commonly use data path elements like adders and multipliers, etc.,. An efficient approximate multiplier will significantly reduce the energy of the system [1] [2].

In general approximate multiplier is designed by introducing approximate compressors in the partial product reduction stage as the partial product reduction stage consumes more area, power, and delay. Introducing approximation in this stage will significantly reduce the energy. There is a significant contribution has done by many researchers in designing a new compressor with different error rates at the output level [1] [2] [3].

The compressors produce two output bits from the n-input bits. Hence, it is popularly used in the partial product reduction stage of the multiplier [4]. The primary function of the compressor is to give the number of 1's present in the given input and produces the binary output. For example, let us consider the input to the compressor as 1111; the compressor produces the output as 100. The number of ones present in this input is 4; this can be read in the output as the most significant two bits 10 are Cout and Carry will have the same weight as 2^1 and the least significant bit is Sum and its weight is 2^0 as shown in equation (1).

$$A + B + C + D = (Cout + Carry).2^1 + Sum.2^0 \quad (1)$$

The accurate 4:2 compressor without Cin is designed using one full adder and one-half adder. Its corresponding circuit diagram is shown in Fig. 1, and Table I is the truth table of the circuit.

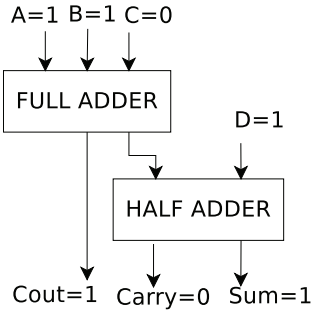

Fig. 1: Conventional Accurate 4:2 Compressor without Cin

TABLE I: Truth Table for Conventional 4:2 Compressor without Cin

A	B	C	D	Cout	Carry	Sum
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	1
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	0
1	1	0	1	1	0	1
1	1	1	0	1	0	1
1	1	1	1	1	1	0

The objective of the approximate compressor is to reduce the power and delay. Hence, the simple circuit can be designed only using primitive gates with slight variation from

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the original output (which leads to error in the output for certain combinations); in such case, the use of XOR gates can be eliminated; as a result, power consumption reduces. The presence of error in the output will not change the visual information in image/video processing applications.

This paper proposes an approximate 4:2 compressor design, which uses primarily primitive gates. The proposed approximate 4:2 compressor design is used in the design of the multiplier to reduce the partial products. The proposed multiplier is delivering superior performance than the existing approximate multipliers.

The rest of the paper is organized as follows. Section II presents a detailed literature review about approximate multiplier. Section III proposes novel approximate 4:2 compressor design and approximate multiplier designs. Section IV detailed the results and discussion and followed by Section V Conclusion.

II. Literature Review

Approximate computing can be implemented at various levels, such as algorithmic level, module-level design, gate-level design, and transistor-level design. Many of the approximate computing works that are available in the literature are at gate-level implementations. In this paper, we are implementing approximate computing for the arithmetic circuit. This paper targets to design an approximate multiplier by designing approximate compressors for the Dadda multiplier.

The generic block diagram of the approximate 4:2 compressor is shown in Fig. 2, and the truth table is shown in Table II. Its equation is shown in 2.

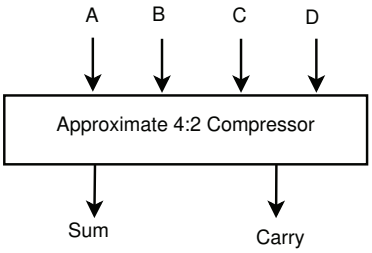


Fig. 2: Generalized Approximate 4:2 Compressor

$$A + B + C + D = Carry.2^1 + Sum.2^0 \quad (2)$$

[3] has proposed hardware-level approximate compressor at gate-level design. [3] has proposed two designs in his work, design2 uses 2 XNOR gates, 3 NOR gates, and one OR gate in his design with an error rate of 25%. He proved that his proposed design would have a lesser delay than the convention accurate 4:2 compressor.

[5] has proposed a approximate 4:2 compressor design as shown in Fig. 3 and Fig. 4 with 12.5% and 25% error rate respectively. In order to reduce the error rate, the author has used XOR, OR, AND, AOI, and OAI standard cells from the design library. The area, power, and delay of [5] are higher than the [3].

TABLE II: Truth Table for Approximate 4:2 Compressor

A	B	C	D	Carry	Sum
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

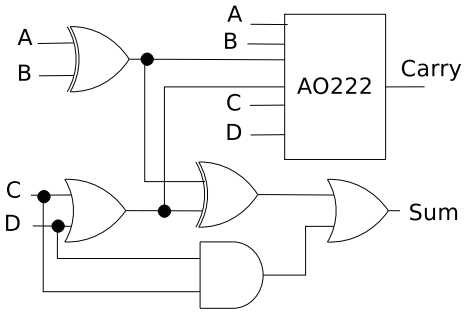


Fig. 3: Approximate 4:2 Compressor Design2 [5]

[6] has proposed three designs, where the hardware circuit for all the three designs remains the same as shown in Fig. 5, except the ordering of the given inputs. The input reorder is achieved using a 2:1 multiplexer, XOR, two OR gates, and one AND gate. All the design has same error rate, i.e., 25% with various delay characteristics. The author has mainly focused on reducing the delay and error rate. The approximate compressor with a different error rate is also present in [7] [8] [9].

A. Contribution of this paper

The objective of this paper is to reduce the power delay product with an acceptable output visual quality of the image.

- This paper uses an input reordering mechanism to reduce the number of inputs to a small number, thereby reducing the complexity of the circuit.
- Proposes a novel approximate 4:2 compressor with an 18.75% error rate.
- The proposed compressor design uses only primitive gates.
- To demonstrate the proposed compressor's effectiveness, this paper uses two multiplier designs.
- Estimated area, power, delay, and Energy (Power delay product) for existing and proposed compressor design and multiplier designs.
- Image processing application is chosen to prove the multiplier's effectiveness, and its metrics are presented.

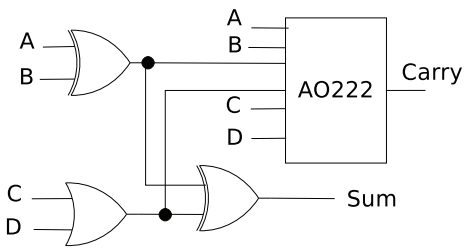


Fig. 4: Approximate 4:2 Compressor Design3 [5]

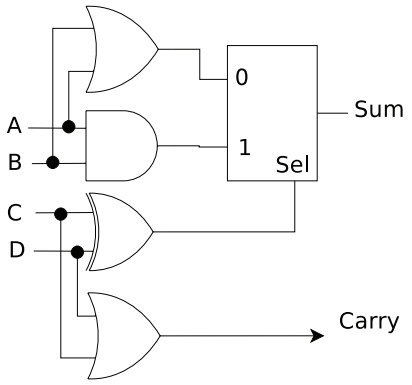


Fig. 5: Approximate 4:2 Compressor Design [6]

III. Proposed Energy-Efficient Approximate Multiplier

This section proposes a novel approximate 4:2 compressor, which is used for reducing the partial products efficiently. This section is organized into two parts. The first part will explain the proposed approximate 4:2 compressors and followed by the second part is an approximate multiplier.

A. A Novel Proposed Approximate 4:2 Compressor

The objective of this section is to design an approximate 4:2 compressor with reduced power, circuit area, delay, and energy. This section proposes a novel approximate 4:2 compressors. The compressor design is designed using only primitive gates, and as a result, delay and power are significantly reduced than the existing approximate 4:2 compressors from the literature.

The truth table of the conventional accurate 4:2 compressor without Cin is shown in Table I, and its circuit diagram is shown in Fig. 1. Based on the truth table I of the accurate 4:2 compressor without Cin, the approximation in the circuit is made by eliminating Cout in the output of the accurate 4:2 compressor design to make it as approximate 4:2 compressor as shown in Fig. 2 and the truth Table II. As accurate 4:2 compressor without Cin has four inputs and three outputs named Cout, Carry, and Sum. As it has four inputs, only one possible combination, i.e., $ABCD = 1111$, will give counted number of 1's like four and rest of the case it is only maximum three and this maximum number of 1's, three can be represented using two output bits, i.e., Carry and Sum.

TABLE III: Truth Table of Input Pairing Alignment Circuit

A	B	C	D	1's Count	Y0	Y1	Y2	Y3
0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	1	0
0	0	1	0	1	0	0	1	0
0	0	1	1	2	0	0	1	1
0	1	0	0	1	1	0	0	0
0	1	0	1	2	1	0	1	0
0	1	1	0	2	1	0	1	0
0	1	1	1	3	1	0	1	1
1	0	0	0	1	1	0	0	0
1	0	0	1	2	1	0	1	0
1	0	1	0	2	1	0	1	0
1	0	1	1	3	1	0	1	1
1	1	0	0	2	1	1	0	0
1	1	0	1	3	1	1	1	0
1	1	1	0	3	1	1	1	0
1	1	1	1	4	1	1	1	1

The maximum count value counted for all the four input 1's is Sum=1 and Carry=1 with an error. The compressor count value depends on the number of 1's present in the input combination rather than the decimal value. Hence, this paper aligns all the 1's presents in the input towards to most significant bit (MSB) side using the input pairing alignment circuit as shown in Fig. 6. In Fig. 6 the inputs A and B are one pair and C and D are another pair. These two pairs align the 1's presents in the inputs towards the MSB side as shown in truth Table III. As a result number of 16 input combinations is reduced to 9 output combinations, as shown in Table III. As a result, compressor design with this logic will have lesser complexity, and circuit switching activity reduces than the existing design. The proposed approximate 4:2 compressor is designed using a truth table of the reduced number of combinations as shown in Table III.

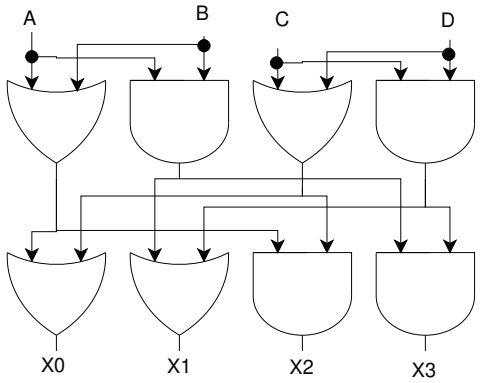


Fig. 6: Input Reordering Circuit

The proposed compressor will have three output combinations that have deviated from the accurate 4:2 compressor with an error rate of 18.75% as shown in Truth Table IV, and its equivalent circuit diagram is shown in Figure 7. The proposed compressor is designed with only primitive gates and one multiplexer.

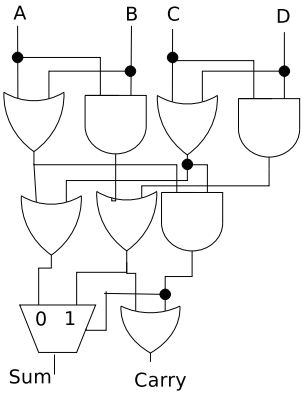


Fig. 7: Proposed Approximate 4:2 Compressor Design.

TABLE IV: Truth Table for Proposed Approximate 4:2 Compressor Design

A	B	C	D	Carry	Sum	Difference
0	0	0	0	0	1	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	1	1	+1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	1	0	0
0	1	1	1	1	1	0
1	0	0	0	0	1	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	1	0
1	1	0	0	1	1	+1
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	-1

B. Approximate Multiplier Design

This section proposes two 8×8 multiplier designs [3] [5], where approximate multiplier design1 as shown in Figure 8 uses the only proposed approximate 4:2 compressors in the partial product reduction stage and adders. The approximate multiplier design2 is shown in Figure 9 uses lower half significant bits is added using the proposed approximate 4:2 compressors, and higher half significant bits of the multiplier is designed using accurate 4:2 compressor in order to reduce the overall error distance.

IV. Results and Discussions

All the existing and proposed designs are modeled using Verilog HDL and implemented in 45nm technology library using Cadence 6.1 EDA tools. The area, power, delay, and power delay product (PDP) of all the designs are estimated. The comparison results of area, power, delay, and power delay product (PDP) of all the existing and proposed approximate compressors are shown in Table V. From Table V, one can summarize that the proposed designs save significant energy (PDP) compared to the existing designs. The percentage of reduction in energy or power delay product is shown in Table VI.

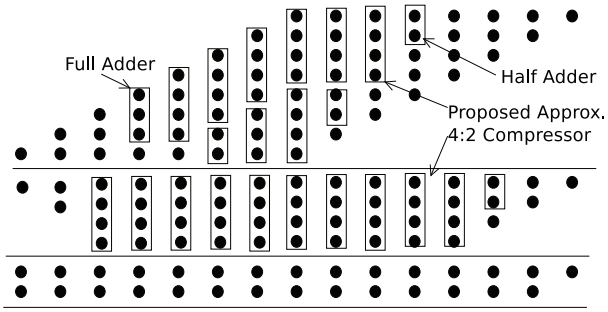


Fig. 8: Proposed Approximate 4:2 Compressors Mapping on Multiplier Design1

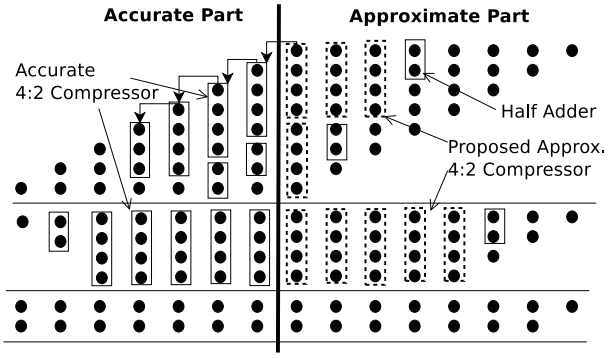


Fig. 9: Proposed Approximate and Accurate 4:2 Compressors Mapping on Multiplier Design2

TABLE V: Results Comparison for Existing and Proposed Approximate 4:2 Compressor Designs

Approximate 4:2 Compressor	**Area** um^2	**Power** nW	**Delay** ps	**PDP** aJ	**% of Error**
Existing Design2 [5]	7	613	70	42.97	12.50
Existing Design3 [5]	7	550	69	37.95	25
Existing Design [6]	7	634	53	33.60	25
Proposed Design	7	556	57	31.69	18.75

TABLE VI: % improvement of PDP of proposed Compressor designs compare with all the existing 4:2 compressors

Approximate 4:2 Compressor From Literature	**Proposed Design**
Existing Design2 [5]	26.24%
Existing Design3 [5]	16.49%
Existing Design [6]	5.68%

The proposed approximate 4:2 compressors are used in the design of the approximate multiplier. The area, power, delay, and power delay product (PDP) of the approximate multiplier design1 implemented using the existing and proposed compressors results are shown in Table VII. Implementation results of the multiplier design2 are shown in Table VIII. The percentage of improvement in multiplier design1 and design2 designed using 25% error based compressors comparison with the proposed compressor is shown in Table VII and Table VIII respectively. The proposed compressor-based multiplier de-

sign2 is compared with all the existing designs from the literature, and its percentage of improvement in power delay product is shown in Table IX.

TABLE VII: Results Comparison for Existing and Proposed Approximate 8-bit Multiplier Design1

Approximate 4:2 Compressor	**Area** um^2	**Power** nW	**Delay** ps	**PDP** fJ
Existing Design2 [5]	276	29835	477	14.23
Existing Design3 [5]	261	28489	558	15.89
Existing Design [6]	264	28430	642	18.25
Proposed Design	273	28016	579	16.22

TABLE VIII: Results Comparison for Existing and Proposed Approximate 8-bit Multiplier Design2

Approximate 4:2 Compressor	**Area** um^2	**Power** nW	**Delay** ps	**PDP** aJ
Existing Design2 [5]	286	34926	559	19.52
Existing Design3 [5]	278	34293	580	19.88
Existing Design [6]	279	34074	580	19.76
Proposed Design	296	34286	517	17.72

TABLE IX: % improvement of PDP of proposed multiplier design-2 compare with existence 4:2 compressor

Approximate 4:2 Compressor From Literature	**Proposed Design4**
Existing Design2 [5]	10%
Existing Design3 [5]	11%
Existing Design [6]	11%

TABLE X: Results Comparison for Existing and Proposed Approximate 8-bit Multiplier Design1

Approximate 4:2 Compressor Design Type	**PSNR dB**	**Mean Error Distance**	**Normalized Error Distance**
Existing Design2 [5]	35	83.28	0.32
Existing Design3 [5]	35.8	138.41	0.5
Existing Design [6]	28	$1.93x10^3$	7.59
Proposed Design	32.82	850	3.33

TABLE XI: Results Comparison for Existing and Proposed Approximate 8-bit Multiplier Design2

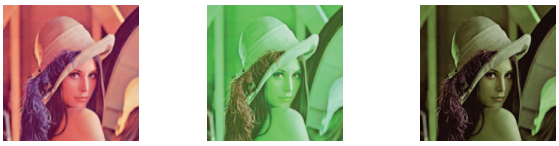
Approximate 4:2 Compressor Design Type	**PSNR dB**	**Mean Error Distance**	**Normalized Error Distance**
Existing Design2 [5]	63.31	11.22	0.04
Existing Design3 [5]	63.31	11.22	0.04
Existing Design [6]	61.45	18.46	0.07
Proposed Design	56.68	80.88	0.23

A. Application: Image Processing

The effectiveness of the approximate multiplication results can be proved by applying on the images and estimating the PSNR of the resultant images. The input for all the approximate multipliers is shown in Figure 10a and Figure 10b. The accurate multiplier resultant output image is shown in Figure 10c. The existing compressor-based approximate multiplier design1 resultant images are shown in Figure 11. The proposed approximate multiplier design1 resultant images are shown in Figure 13a.

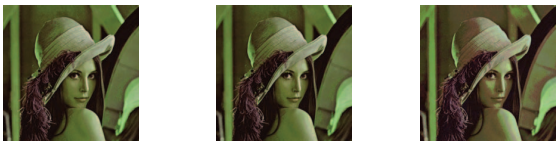
The existing compressor-based approximate multiplier design2 resultant images are shown in Figure 12. The proposed approximate multiplier design2 resultant images are shown in Figure 13b.

The peak signal-noise ratio (PSNR), mean error distance (MED) [1], and normalized error distance (NED) [10] of the existing and proposed compressor-based multiplier design1 and design2 are compared in the Table X and Table XI. The proposed compressor-based multiplier is shown a significant improvement than the existing techniques from the literature. Multiplication is one of the basic operation in many image/video processing applications such as DCT (Discrete Cosine Transform) and DWT (Discrete Wavelet Transform) and etc.,.



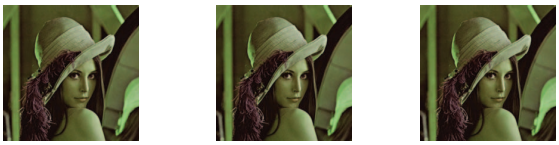
(a) Input Image1 (b) Input Image2 (c) Output Image

Fig. 10: Input and Output Images of the Exact Multiplication



(a) Output [5] (b) Output [5] (c) Output [6]

Fig. 11: Output Images of the Approximate Multiplier Design1



(a) Output [5] (b) Output [5] (c) Output [6]

Fig. 12: Output Images of the Approximate Multiplier Design2

V. Conclusion

This paper proposed an approximate 4:2 compressor design with an 18.75% error rate. The proposed approximate compressor is compared with the existing designs in terms of area, power, and power delay product. The proposed approximate 4:2 compressors design delivers impressive energy savings

(a) Using Multiplier Design1 (b) Using Multiplier Design2

Fig. 13: Output Images of the Proposed Approximate Multiplier

with a low error rate, i.e., 18.75%. The proposed approximate compressors are used in the design of multiplier design1 and design2. The approximate multiplier design2 saves energy on an average of 10.8%, compared with all the existing designs. The PSNR values of the approximate multiplier design2 are better than the existing designs.

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