



EE224 PROJECT REPORT

TEAM ID- 12

OUR TEAM

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22B1219

22B3958

22B0305

22B3966

WORK DISTRIBUTION

DOCUMENTATION

- Mrunali and Mitul worked on the initial framework we needed to get started.
- Garima made the diagrams, and Abhineet wrote the documentation.
- We all worked together to figure out the logic necessary for implementation.

CODE

- We distributed the coding implementation fairly uniformly.
- The components were made mostly by Mitul, Garima and Mrunali.
- The main entity and the integration of all components was taken care of by Abhineet.
- The de-bugging and the final testing was done by all of us together.



WORK FLOW

- To begin with, we used the project statement and our notes as reference, and made pen-paper designs and flowcharts for the entire cpu, all the parts.
- This included grouping equivalent states, and figuring out where to use decoders and muxes along with their relevant control signals.
- We then started coding to implement the design in VHDL.



WORK FLOW

- We made the components first. These include the ALU, the sign-extenders, the MUXes, the register file, the memory unit and the other components used by these components internally.
- We, then made the top-level entity, iitb_cpu. This included coding the state transition logic and the output logic.
- After this, we started debugging which took a really long time. Once, the syntax errors were removed and we could finally compile, we ran into another problem: our output was oscillating between the same two values.

WORK FLOW

- We figured out that there was an error in our 16-bit adder-subtractor. This fixed the oscillation issue and gave us the correct outputs.
- Another challenge that came up was that some of the signal values didn't get updated. We fixed this issue by splitting some of the states into two.
- This made sure that the signals, which get updated only after a clock pulse had a separate state.
- Then to test whether all the operations were working correctly, we initialized the register array according to the operation codes and checked the RTL simulation.