WORK REPORT

EE224/309

IITB-CPU

TEAM ID- 12

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CHANGES MADE TO THE PREVIOUS CODE:

→ Added and removed a few states.
→ Changed to structural modeling from behavioral modeling to reduce the number of registers created by the Xen10 board while execution, and to make the code more easily synthesizable.
→ Introduced a MUX for RF_write to specify which register we are writing into.
→ Did the pin planning of respective input and output signals.
→ Initially had a separate register for IP, but now integrated it to the R7 of register file, taking care that R7 can also be used as an operand as well as updated after an operation.

OUTPUTS:

PB1 - RST
PB2 - shows lower order 8 bits when LOW; and higher order 8 bits when high.
PB3 - LED1 shows the z flag when high.
PB4 - LEDs show registers when low and memory data when high.

SW 1-3 : gives the input for register number when PB4 is low.
SW 1-8 : gives the memory address when PB4 is high.

LED 1-8 : shows lower or higher order 8 bits of the output corresponding to the input given to PB-2.

WORK DISTRIBUTION:

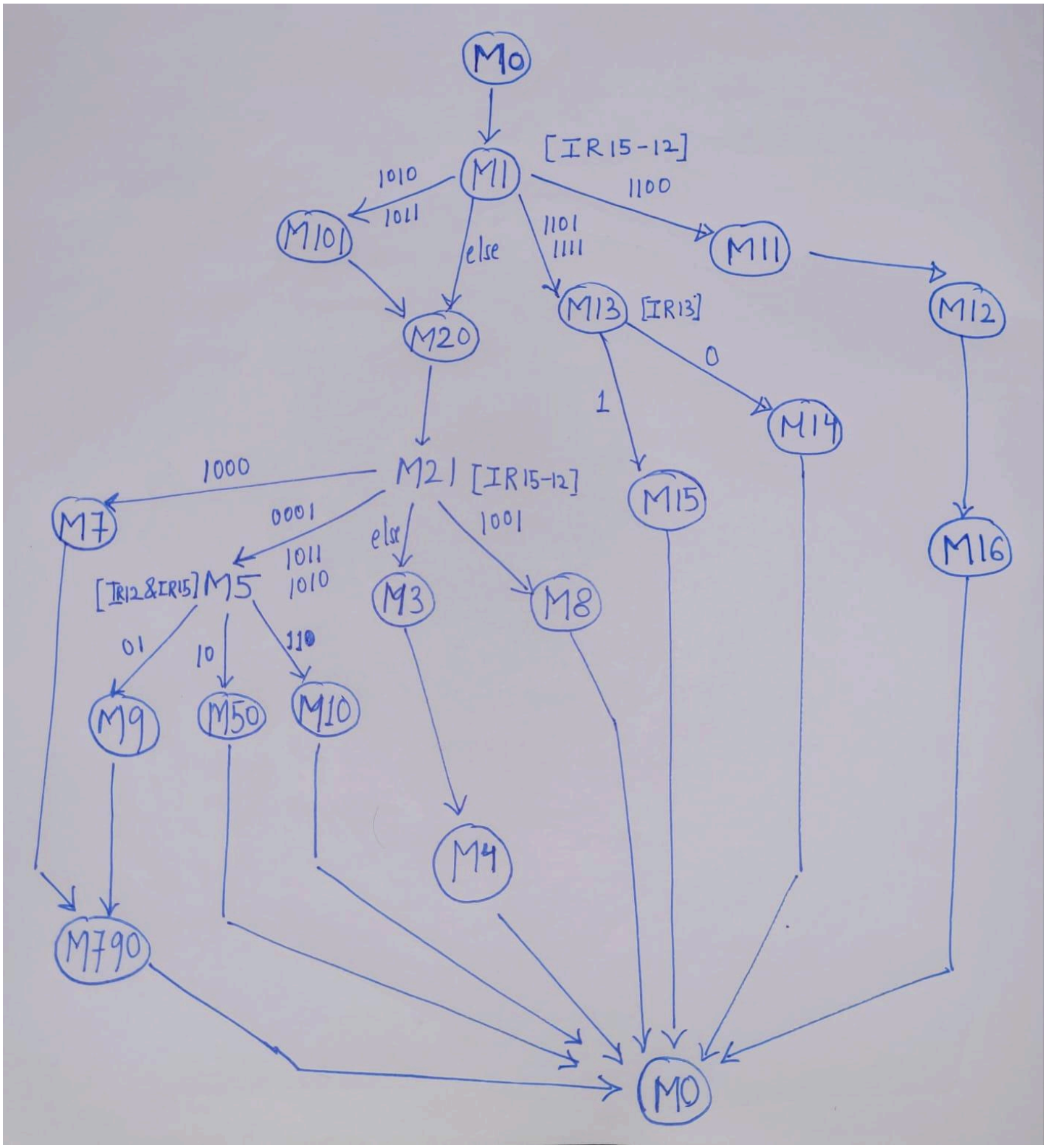
Mrunali: design of the CPU based on structural modeling; re-writing RF file and memory ; testing and debugging.

Mitul: design of the CPU based on structural modeling; re-writing RF file and memory ; testing and debugging.

Abhineet: Re-writing the main entity and integrating the code; pin-planning; debugging.

Garima: design of the CPU based on structural modeling; pin-planning.

New FSM


M0
M1
[IR15-12]
1010
1011
1100
M101
else
1101
1111
M11
M12
M13
[IR13]
M20
0
1
M14
M15
M16
M21
[IR15-12]
1000
0001
1001
else
M7
1011
1010
[IR12&IR15]
M5
M3
M8
01
10
11
M9
M50
M10
M4
M790
M0