EE224 Course Project

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ADD

1. Fetch instruction and IP update. (S_1)
2. Understand and operand fetch. (S_2)
3. Add. (S_3)
4. Update result onto Register (S_4)

1. Fetch instruction and IP update. (S_1)

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Understand and operand fetch. (S_2)

Fetch	Controls
IR_{9-11}—>RF-A_1	T_1-W
IR_{6-8} —> RF-A_2	T_2-W
RF-D_1 —> T_1	
RF-D_2 —> T_2	

3. Add. (S_3)

Fetch	Controls
T_1—>ALU-A	ADD 00_00
T_2—> ALU-B	T_3-W
ALU-C —> T_3	

4. Update result onto Register. (S_4)

Fetch	Controls
T_3—>RF-D_3	RF-W
IR_{3-5}—> RF-A_3	

SUB

1. Fetch instruction and IP update. (S_5)
2. Understand and operand fetch. (S_6)
3. Subtract. (S_7)
4. Update result onto Register (S_8)

1. Fetch instruction and IP update. (S_5)

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Understand and operand fetch. (S_6)

Fetch	Controls
$IR_{9\text{-}11}$—>RF-A_1	T_1-W
$IR_{6\text{-}8}$ —> RF-A_2	T_2-W
RF-D_1 —> T_1	
RF-D_2 —> T_2	

3. Subtract. (S_7)

Fetch	Controls
T_1—>ALU-A	SUB 00_10
T_2—> ALU-B	T_3-W
ALU-C —> T_3	

4. Update result onto Register. (S_8)

Fetch	Controls
T_3—>RF-D_3	RF-W
$IR_{3\text{-}5}$—> RF-A_3	

MUL

1. Fetch instruction and IP update. (S_9)
2. Understand and operand fetch. (S_{10})
3. Multiply. (S_{11})
4. Update result onto Register (S_{12})

1. Fetch instruction and IP update. (S_9)

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Understand and operand fetch. (S_{10})

Fetch	Controls
IR_{9-11}—>RF-A_1	T_1-W
IR_{6-8} —> RF-A_2	T_2-W
RF-D_1 —> T_1	
RF-D_2 —> T_2	

3. Multiply. (S_{11})

Fetch	Controls
T_1—>ALU-A	MUL 00_11
T_2—> ALU-B	T_3-W
ALU-C —> T_3	

4. Update result onto Register. (S_{12})

Fetch	Controls
T_3—>RF-D_3	RF-W
IR_{3-5}—> RF-A_3	

ADI

1. Fetch instruction and IP update. (S_{13})
2. Understand and operand fetch. (S_{14})
3. Execute.. (S_{15})
4. Update result onto Register (S_{16})

1. Fetch instruction and IP update. (S_{13})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Understand and operand fetch. (S_{14})

Fetch	Controls
IR_{9-11}—>RF-A_1	T_1-W
RF-D_1 —> T_1	

3. Execute. (S_{15})

Fetch	Controls
T_1 —> ALU-A	ADD 00_00
IR_{0-5} —> SE[6] —> ALU-B	T_3-W
ALU-C —> T_3	

4. Update result onto Register. (S_{16})

Fetch	Controls
T_3 —> RF-D_3	RF-W
IR_{6-8} —> RF-A_3	

AND

1. Fetch instruction and IP update. (S_{17})
2. Understand and operand fetch. (S_{18})
3. Execute logical AND. (S_{19})
4. Update result onto Register (S_{20})

1. Fetch instruction and IP update. (S_{17})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Understand and operand fetch. (S_{18})

Fetch	Controls
IR_{9-11}—>RF-A_1	T_1-W
IR_{6-8} —> RF-A_2	T_2-W
RF-D_1 —> T_1	
RF-D_2 —> T_2	

3. Execute logical AND. (S_{19})

Fetch	Controls
T_1—>ALU-A	AND 01_00
T_2—> ALU-B	T_3-W
ALU-C —> T_3	

4. Update result onto Register. (S_{20})

Fetch	Controls
T_3—>RF-D_3	RF-W
IR_{3-5}—> RF-A_3	

ORA

1. Fetch instruction and IP update. (S_{21})
2. Understand and operand fetch. (S_{22})
3. Execute logical OR. (S_{23})
4. Update result onto Register (S_{24})

1. Fetch instruction and IP update. (S_{21})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Understand and operand fetch. (S_{22})

Fetch	Controls
IR_{9-11}—>RF-A_1	T_1-W
IR_{6-8} —> RF-A_2	T_2-W
RF-D_1 —> T_1	
RF-D_2 —> T_2	

3. Execute. (S_{23})

Fetch	Controls
T_1—>ALU-A	ORA 01_01
T_2—> ALU-B	T_3-W
ALU-C —> T_3	

4. Update result onto Register. (S_{24})

Fetch	Controls
T_3—>RF-D_3	RF-W
IR_{3-5}—> RF-A_3	

IMP

1. Fetch instruction and IP update. (S_{25})
2. Understand and operand fetch. (S_{26})
3. Execute logical implication. (S_{27})
4. Update result onto Register (S_{28})

1. Fetch instruction and IP update. (S_{25})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Understand and operand fetch. (S_{26})

Fetch	Controls
IR_{9-11}—>RF-A_1	T_1-W
IR_{6-8} —> RF-A_2	T_2-W
RF-D_1 —> T_1	
RF-D_2 —> T_2	

3. Execute logical implication. (S_{27})

Fetch	Controls
T_1—>ALU-A	IMP 01_10
T_2—> ALU-B	T_3-W
ALU-C —> T_3	

4. Update result onto Register. (S_{28})

Fetch	Controls
T_3—>RF-D_3	RF-W
IR_{3-5}—> RF-A_3	

LHI

1. Fetch instruction and IP update. (S_{29})
2. Empty State. (S_{30})
3. Executing left shift operation. (S_{31})
4. Update result onto Register. (S_{32})

1. Fetch instruction and IP update. (S_{29})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Empty State. (S_{30})

Fetch	Controls

3. Execute. (S_{31})

Fetch	Controls
IR_{0-7} —> SE[8] —> ALU-A	LEFT SHIFT (8 bits)
ALU-C —> T_3	T_3-W

4. Update result onto Register. (S_{32})

Fetch	Controls
T_3—>RF-D_3	RF-W
IR_{9-11}—> RF-A_3	

LLI

1. Fetch instruction and IP update. (S_{33})
2. Empty state. (S_{34})
3. Update result onto Register (S_{35})

1. Fetch instruction and IP update. (S_{33})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Empty state. (S_{34})

Fetch	Controls

3. Update result onto Register. (S_{35})

Fetch	Controls
IR_{0-7} —> SE[8] —> RF-D3	RF-W
IR_{9-11} —> RF-A_3	

LW

1. Fetch instruction and IP update. (S_{36})
2. Understand and operand fetch. (S_{37})
3. Compute address. (S_{38})
4. Read Memory. (S_{39})
5. Update Register. (S_{40})

1. Fetch instruction and IP update. (S_{36})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Understand and operand fetch. (S_{37})

Fetch	Controls
IR_{9-11}—>RF-A_1	T_1-W
RF-D_1 —> T_1	

3. Compute Address [R_2 + IMM*2] (S_{38})

Fetch	Controls
T_1 —> ALU-A	ADD 00_00
IR_{0-5} —> SE[6] —> ALU-B	T_3-W
ALU-C —> T_3	

4. Read Memory M[R_2 + IMM*2] (S_{39})

Fetch	Controls
T_3—> Memory Address	Mem-Read
Memory Data —> T_3	T_3-W

5. Update Register (R_1) (S_{40})

T_3—> RF-D_3	RF-W
IR_{6-8}—> RF-A_3	

SW

1. Fetch instruction and IP update. (S_{41})
2. Understand and operand fetch. (S_{42})
3. Compute address. (S_{43})
4. Write Memory. (S_{44})

1. Fetch instruction and IP update. (S_{41})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	ADD 00_00
IP —> ALU-A	IR-W
+2 —> ALU-B	IP-W
ALU-C —> IP	

2. Understand and operand fetch. (S_{42})

Fetch	Controls
IR_{9-11} —> RF-A_1	T_1-W
IR_{6-8} —> RF-A_2	T_2-W
RF-D_1 —> T_1	
RF-D_2 —> T_2	

3. Compute Address [R_2 + IMM*2] (S_{43})

Fetch	Controls
T_1 —> ALU-A	ADD 00_00
IR_{0-5} —> SE[6] —> ALU-B	T_3-W
ALU-C —> T_3	

4. Write Memory. (S_{44})

Fetch	Controls
T_3 —> Memory Address	Mem-Write
T_2 —> Memory Data	

BEQ

1. Fetch instruction (S_{45})
2. Understand and operand fetch (S_{46})
3. Compute if (R_1-R_2) = 0 (S_{47})
4. Update Instruction pointer 1 (S_{48})
5. Update Instruction pointer 2 (S_{57})

1. Fetch instruction.(S_{45})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	IR-W

2. Understand and operand fetch. (S_{46})

Fetch	Controls
IR_{9-11}—>RF-A_1	T_1-W
IR_{6-8} —> RF-A_2	T_2-W
RF-D_1 —> T_1	
RF-D_2 —> T_2	

3.Compute if (R_1-R_2) = 0 (S_{47})

Fetch	Controls
T_1—>ALU-A	SUB 00_01
T_2—> ALU-B	Z-W
ALU-Z—> Z	

4.Update Instruction pointer 1. (S_{48})

Fetch	Controls
IP—>ALU-A	ADD 00_00
IR_{0-5} —> SE6 —> ALU-B	T3_W
ALU-C —> T3	

5. Update Instruction pointer 2. (S_{57})

IP—>ALU-A	ADD 00_00
+2 —> ALU-B ALU-C —> T1 If (Z==1) T3 —> IP	IP_W T1_W

Else T1 —> IP	

JAL

1. Fetch instruction. (S_{49})
2. Empty state (S_{50})
3. Update current Instruction pointer onto Register. (S_{51})
4. Compute Instruction pointer. (S_{52})

1. Fetch instruction (S_{49})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	IR-W

2. Empty state (S_{50})

Fetch	Controls

3. Update current Instruction pointer onto Register(S_{51})

Fetch	Controls
IP —> RF-D_3	RF-W
$IR_{9\text{-}11}$ —> RF-A_3	

4. Compute Instruction pointer (S_{52})

Fetch	Controls
IP —> ALU-A	ADD 00_00
$IR_{0\text{-}8}$ —> SE[9] —> SHIFT LEFT —--> ALU-B	IP-W
ALU-C —> IP	

JLR

1. Fetch instruction. (S_{53})
2. Empty state. (S_{54})
3. Update current Instruction pointer onto Register. (S_{55})
4. Update Instruction pointer. (S_{56})

1. Fetch instruction. (S_{53})

Fetch	Controls
IP —> Memory Address	Mem-Read
Memory Data —> IR	IR-W

2. Empty state. (S_{54})

Fetch	Controls

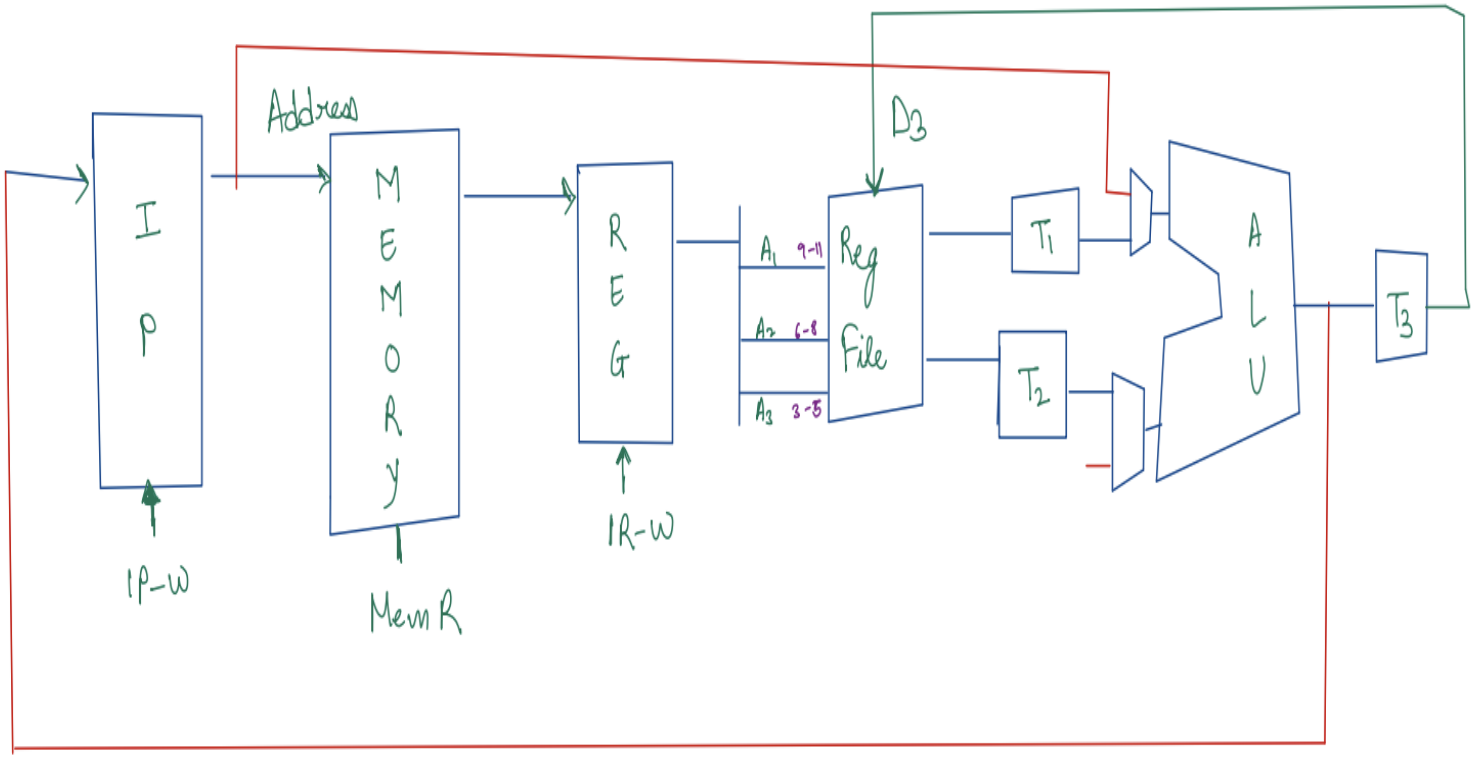
3. Update current Instruction pointer onto Register(S_{55})

Fetch	Controls
IP —> $RF\text{-}D_3$	RF-W
$IR_{9\text{-}11}$ —> $RF\text{-}A_3$	

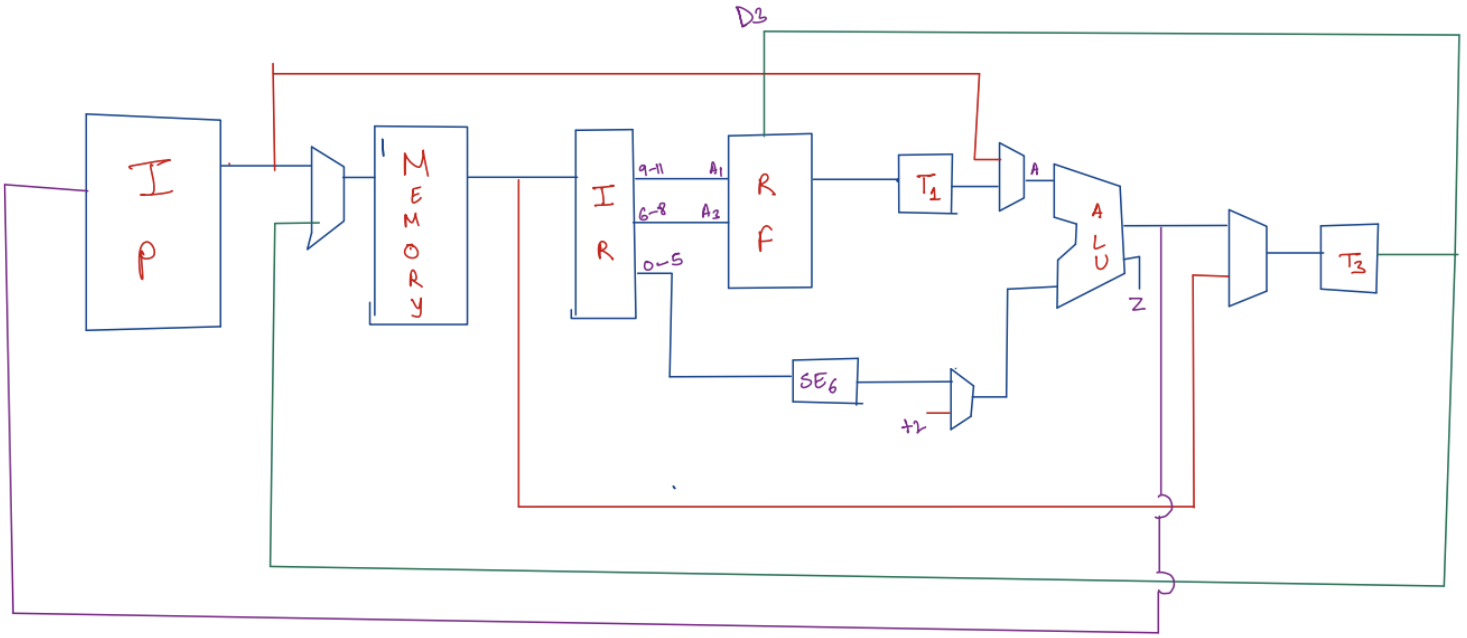
4. Update Instruction pointer (S_{56})

Fetch	Controls
$IR_{6\text{-}8}$ —> RF-A2	IP-W
$RF\text{-}D_2$ —-> IP	

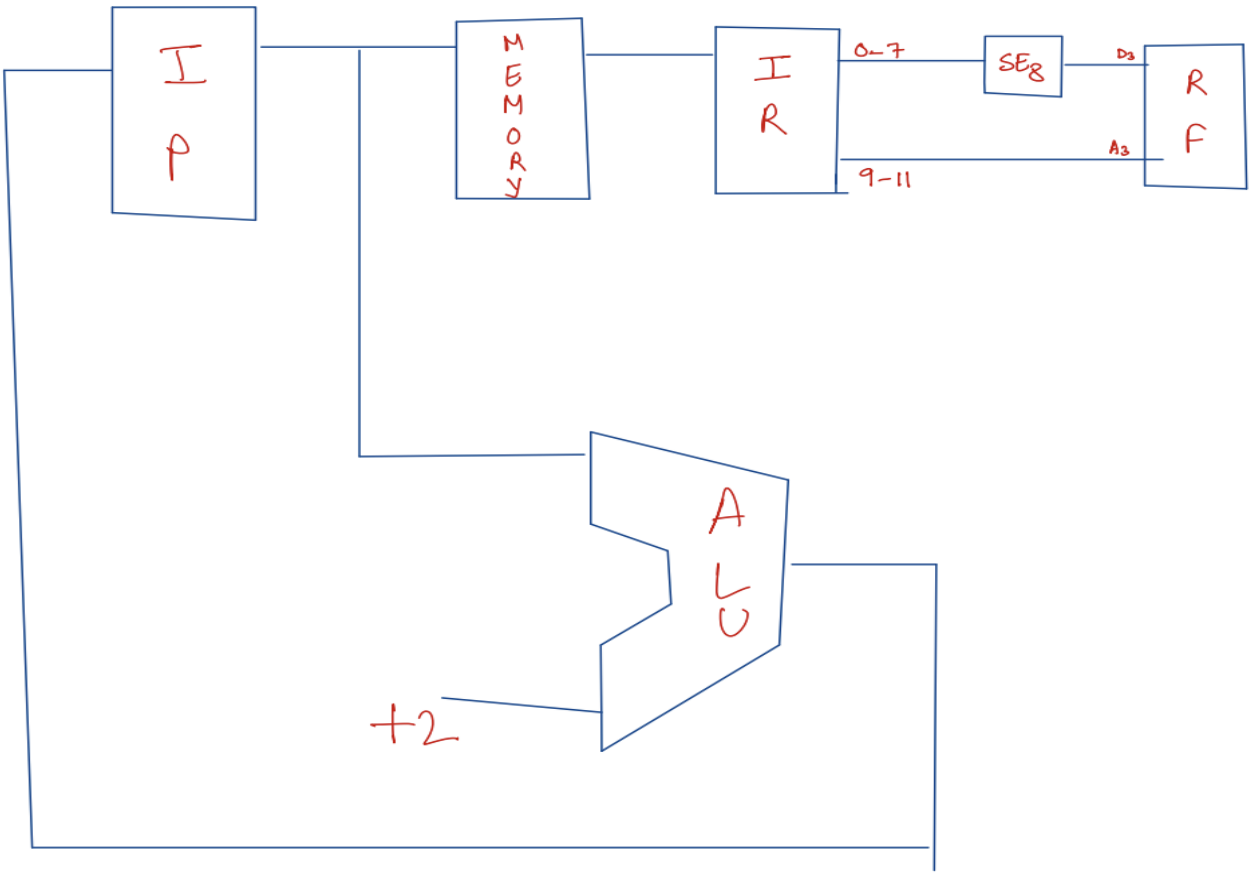
ADD / SUB / MUL / LOGICAL_AND / LOGICAL_OR / LOGICAL_IMP



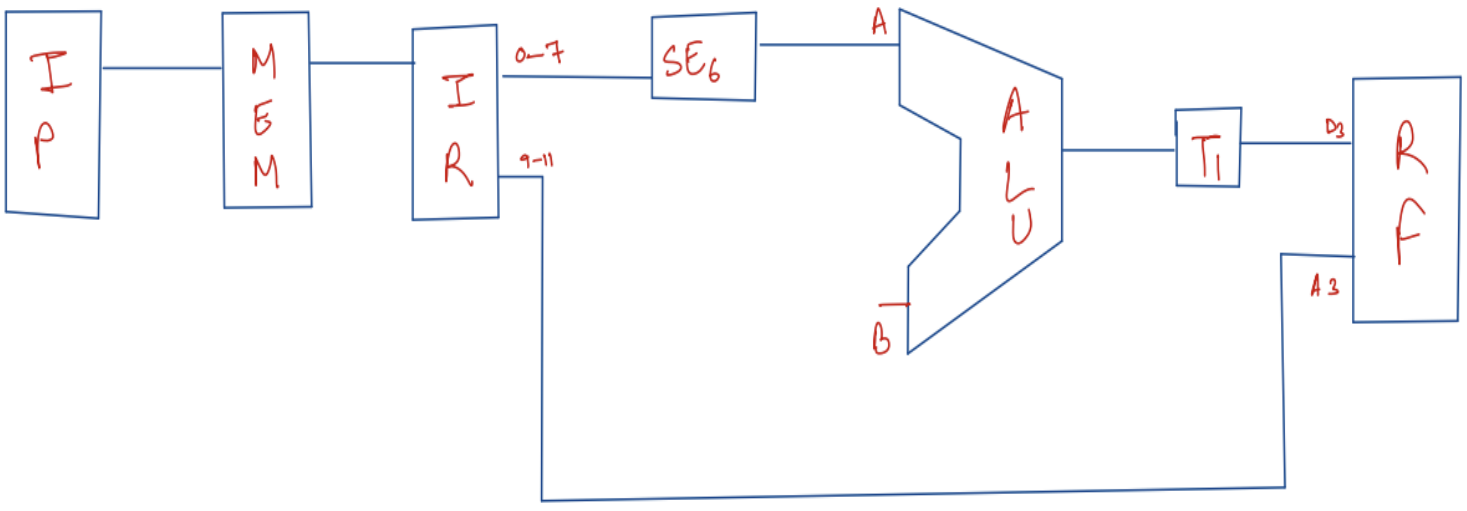
ADD_IMM / LOAD / STORE / BEQ



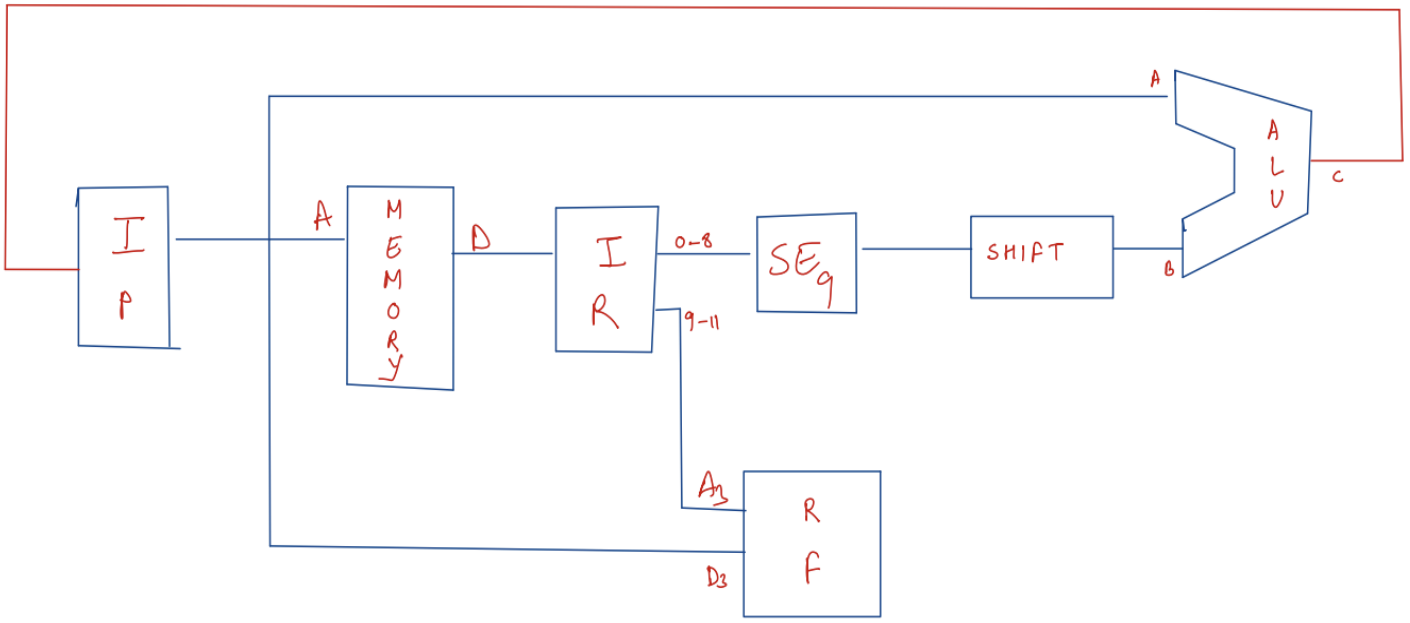
LLI


I
p
MEMORY
I
R
0-7
SE8
D3
R
F
A3
9-11
A
L
U
+2

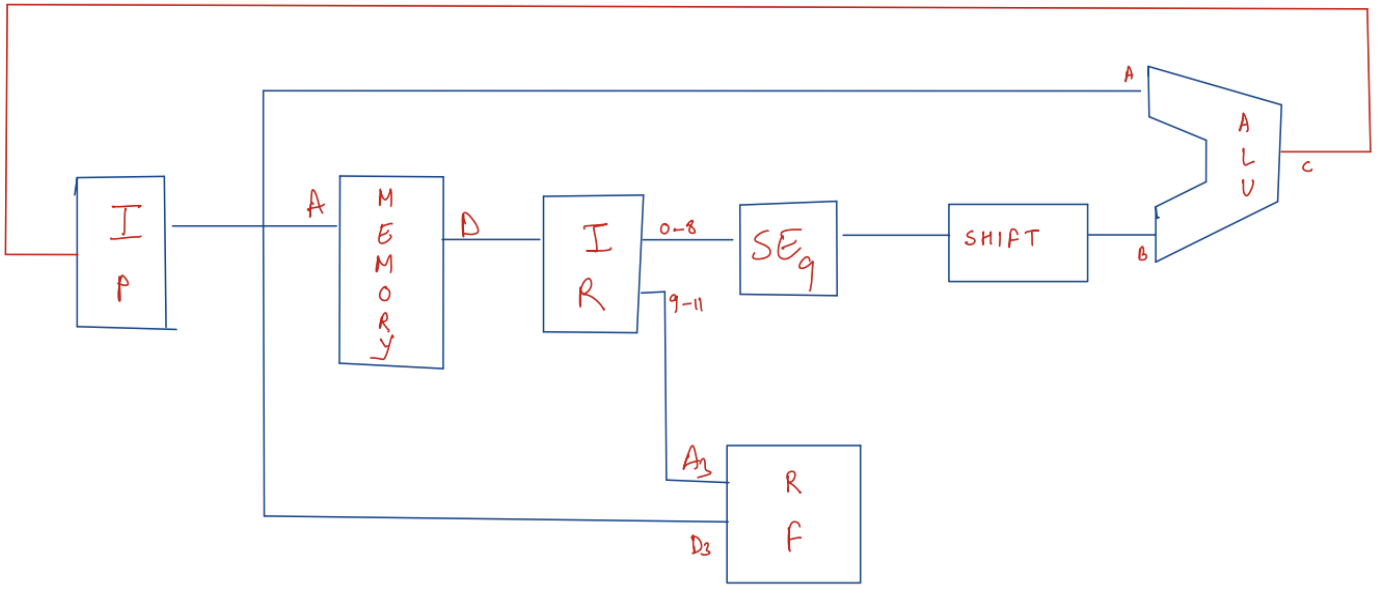
LHI


I
p
MEM
I
R
0-7
9-11
SE6
A
A
L
U
B
T1
D3
R
F
A3

JUMP AND LINK

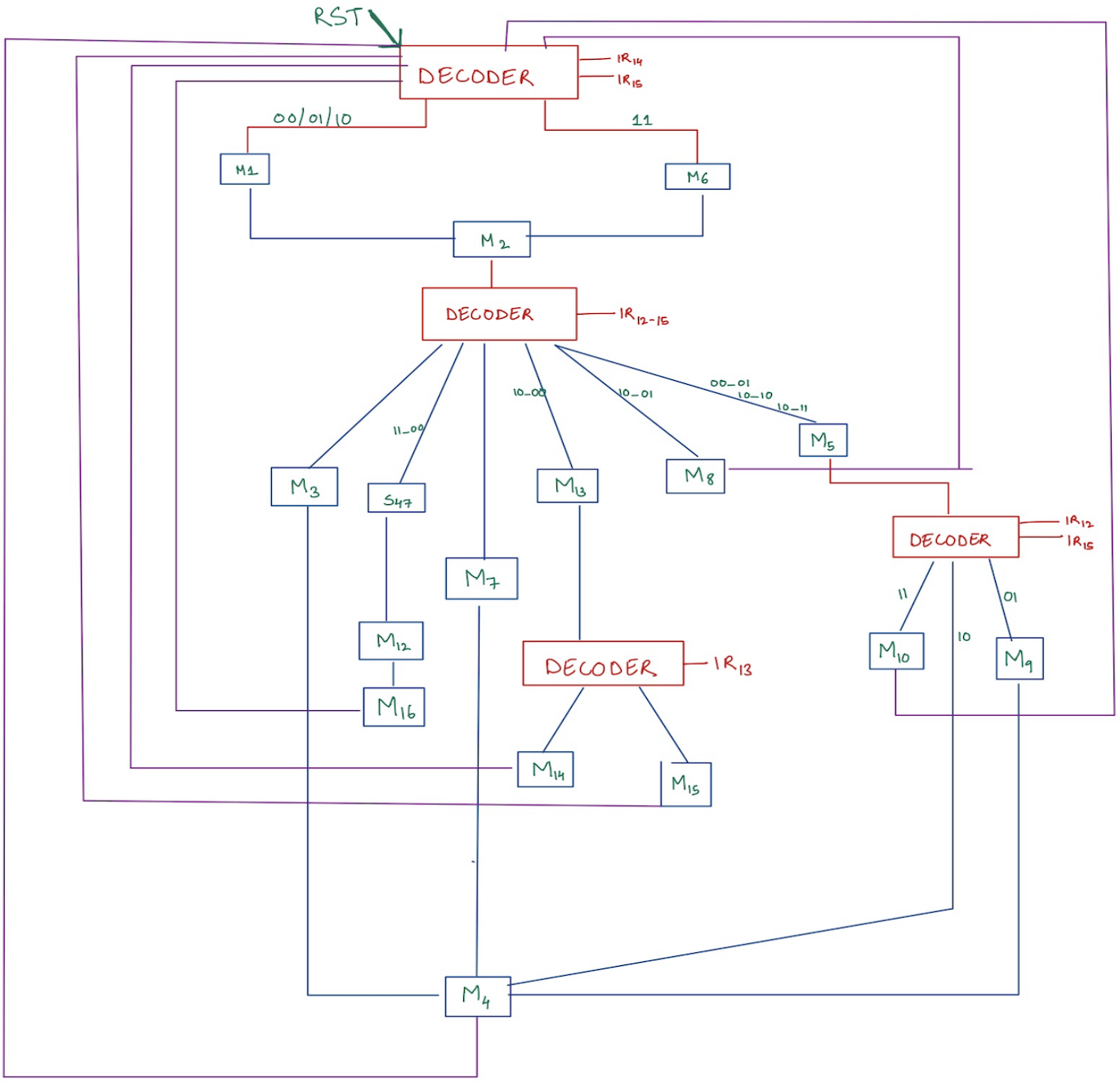


JUMP AND LINK TO REG

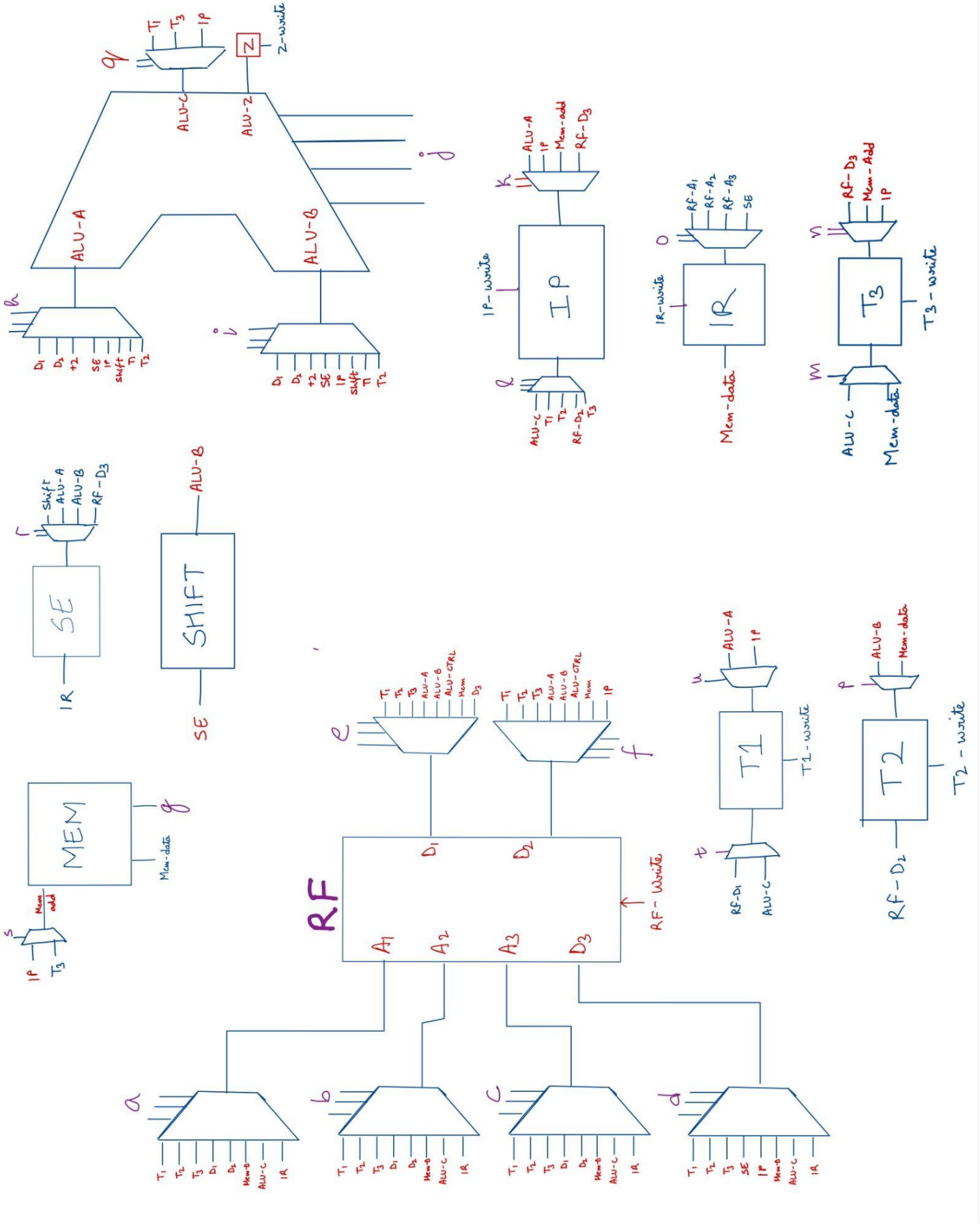


Grouping of equivalent states

M_1: S_1, S_5, S_9, S_{13}, S_{17}, S_{21}, S_{25}, S_{29}, S_{33}, S_{36}, S_{41}.
M_2 : S_2, S_6, S_{10}, S_{14}, S_{18}, S_{22}, S_{26}, S_{30}, S_{34}, S_{37}, S_{42}, S_{46}, S_{50}, S_{54}.
M_3: S_3, S_7, S_{11}, S_{19}, S_{23}, S_{27}.
M_4: S_4, S_8, S_{12}, S_{16}, S_{20}, S_{24}, S_{28}, S_{32}, S_{40}.
M_5: S_{15}, S_{38}, S_{42}.
M_6: S_{45}, S_{49}, S_{53}.
M_7: S_{31}.
M_8: S_{35}.
M_9: S_{39}.
M_{10}: S_{44}.
M_{11}: S_{47}.
M_{12}: S_{48}.
M_{13}: S_{51}, S_{55}.
M_{14}: S_{52}.
M_{15}: S_{56}.
M_{16}=S_{57}



Final Circuit



MUX mappings

ADD:
S_1
s=0
g=0
k=10
j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010
l=00
q=10

S_2
T_1_W=1
T_2_W=1
IR_{9-11}=RF_A_1
IR_{6-8}=RF_A_2
a=111
b=111
e=000
f=001

S_3
p=0
m=0
j=0000
T_3_W=1
q=01

S_4
RF_W=1
d=010
n=00
IR_{3-5}=RF_A_3

SUB:

S_5
g=0
k=10
j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010

l=00
q=10
s=0

S_6
T_1_W=1
T_2_W=1
IR_{9-11}=RF_A_1
IR_{6-8}=RF_A_2
a=111
b=111
e=000
f=001

S_7
p=0
m=0
j=0010
T_3_W=1
q=01

S_8
RF_W=1
d=010
n=00
IR_{3-5}=RF_A_3

MUL
S_9
g=0
k=10
j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010
l=00
q=10
s=0

S_{10}
T_1_W=1
T_2_W=1
IR_{9-11}=RF_A_1
IR_{6-8}=RF_A_2
a=111
b=111
e=000
f=001

S_{11}

p=0
m=0
j=0011
T_3_W=1
q=01

S_{12}
RF_W=1
d=010
n=00
IR_{3-5}=RF_A_3

ADI

S_{13}
g=0
k=10
j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010
l=00
q=10
s=0

S_{14}
T_1_W=1
IR_{9-11}=RF_A_1

S_{15}
h=110
IR_{0-5}=SE
i=100
q=01
j=0000
T_3_W=1
r=10

S_{16}
n=00
d=011
RF_W=1
IR_{6-8}=RF_A_3
c=111

AND

S_{17}
g=0
k=10

j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010
l=00
q=10
s=0

S_{18}
T_1_W=1
T_2_W=1
IR_{9-11}=RF_A_1
IR_{6-8}=RF_A_2
a=111
b=111
e=000
f=001

S_{19}
p=0
m=0
j=0100
T_3_W=1
q=01

S_{20}
RF_W=1
d=010
n=00
IR_{3-5}=RF_A_3

ORA

S_{21}
g=0
k=10
j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010
l=00
q=10
s=0

S_{22}
T_1_W=1
T_2_W=1
IR_{9-11}=RF_A_1

$IR_{6\text{-}8}$=RF_A_2
a=111
b=111
e=000
f=001

S_{23}
p=0
m=0
j=0101
T_3_W=1
q=01

S_{24}
RF_W=1
d=010
n=00
$IR_{3\text{-}5}$=RF_A_3

IMP

S_{25}
g=0
k=10
j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010
l=00
q=10
s=0

S_{26}
T_1_W=1
T_2_W=1
$IR_{9\text{-}11}$=RF_A_1
$IR_{6\text{-}8}$=RF_A_2
a=111
b=111

S_{27}
p=0
m=0
j=0110
T_3_W=1
q=01

S_{28}
RF_W=1
d=010

n=00
IR_{3-5}=RF_A_3

LHI

S_{29}
g=0
k=10
j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010
l=00
q=10
s=0

S_{30}

S_{31}
IR_{0-7}=SE
h=100 when j=1111, ALU executes a LEFT_SHIFT (8 bits) operation
q=01
m=0
T_3_W=1
r=01

S_{32}
n=00
RF_W=1
d=011
IR_{9-11}=RF_A_3
c=111

LLI

S_{33}
g=0
k=10
j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010
l=00
q=10
s=0

S_{34}

S_{35}
IR_{0-7}=SE
r=11 when j=1111, ALU executes a LEFT_SHIFT (8 bits) operation
RF_W=1
IR_{9-11}=RF_A_3
c=111

LW

S_{36}
g=0
k=10
j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010
l=00
q=10
s=0

S_{37}
S_{14}
T_1_W=1
IR_{9-11}=RF_A_1

S_{38}
h=110
T_3_W=1
j=0000
IR_{0-5}=SE
i=110
r=10
q=01
m=0
S_{39}
T_3_W=1
n=01
g=0
m=1

S_{40}
n=00
RF_W=1
d=011
IR_{9-11}=RF_A_3
c=111

SW

S_{41}
g=0
k=10
j=0000
IR_W=1
IP_W=1
h=101
k=00
i=010
l=00
q=10
s=0

S_{42}
T_1_W=1
T_2_W=1
$IR_{9\text{-}11}$=RF_A_1
$IR_{6\text{-}8}$=RF_A_2
a=111
b=111
e=000
f=001

S_{43}
h=110
j=0000
T_3_W=1
$IR_{0\text{-}5}$=SE
i=100
r=10
q=01
m=0

S_{44}
g=1
n=01
p=1
s=1

BEQ

S_{45}
s=0
g=0
IR_W=1

S_{46}
T_1_W=1
T_2_W=1
$IR_{9\text{-}11}$=RF_A_1

$IR_{6\text{-}8}$=RF_A_2
a=111
b=111

S_{47}
h=110
i=111
p=0
Z_W=1
j=0001
e=000
f=001

S_{48}
h=101
k=00
$IR_{0\text{-}5}$=SE
i=100
r=10
q=01
m=0
j=0000
T_3_W=1

S_{57}
k=00
h=101
i=011
q=00
t=1
IP_W=1
T_1_W=1
j=0000
if(Z==1)
n=10
l=100
else
u=1
l=001

JLA
S_{49}
s=0
g=0
IR_W=1

S_{50}

S_{51}
k=11
d=100
RF_W=1

$IR_{9\text{-}11}$=RF_A_3
c=111

S_{52}

k=00
h=100
j=0000
IP_W=1
$IR_{0\text{-}8}$=SE
r=00
i=101
q=10
l=000

JLR

S_{53}
s=0
g=0
IR_W=1
S_{54}

S_{55}
k=11
d=100
RF_W=1
$IR_{9\text{-}11}$=RF_A_3
c=111

S_{56}
$IR_{6\text{-}8}$=RF_A_2
b=111
IP_W=1
f=111