EE230: Analog Circuits Lab
Lab No.6

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March 13, 2024

1 MOSFET Characterization

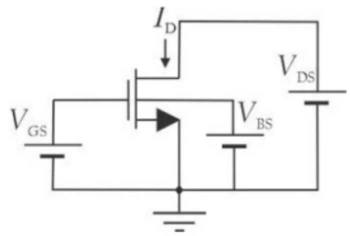
1.1 Aim of the experiment

The aim of this analysis is to investigate the relationship between I_d and V_{gs}, and to validate the theoretical expression for I_d using experimental data. In this section, experimental data for I_d values corresponding to various V_{gs} values (ranging from 0 to 5 V) is provided. The experiments were conducted with a constant drain-source voltage (V_{ds}) of 5 V and a gate-source voltage (V_{bs}) of 0 V.

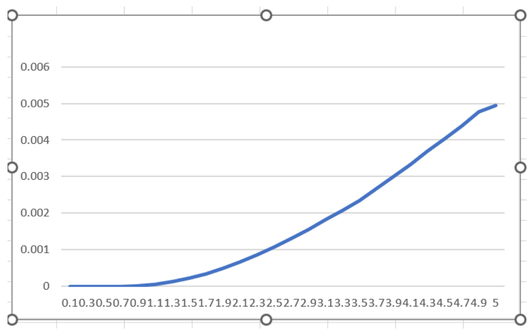
1.2 Design

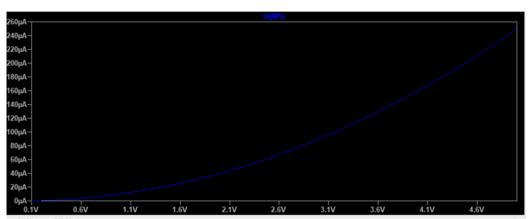
1.2.1 Extract Kn and Vth

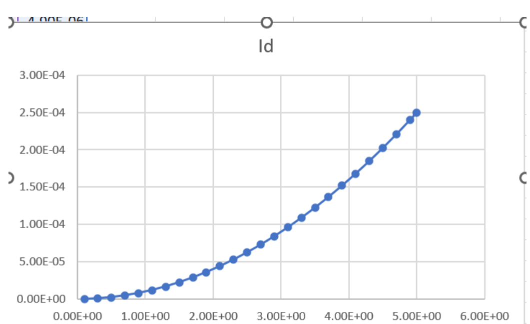
In the design phase, we utilize $I_d = \frac{k_n}{2} \cdot (V_{gs} - V_{th})^2$ to calculate drain current (I_d). This expression, with k_n as transconductance and V_{th} as threshold voltage, facilitates I_d determination for varied V_{gs} values, aiding biasing decisions. Component values are chosen based on I_d calculations and circuit needs, ensuring desired functionality. This approach integrates theory with practical considerations for efficient circuit implementation.



1.2.2 Section 1: Id v/s Vgs







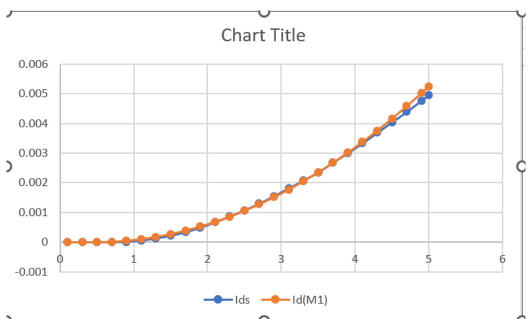
1.2.3 Section 2: Extract Kn and Vth

Given the expression for drain current (I_d) as $I_d = \frac{k_n}{2} \cdot (V_{gs} - V_{th})^2$, and considering experimental data, we extract $V_{th} = 0.45\,\mathrm{V}$ and $k_n = 495 \times 10^{-6}\,\mathrm{A/V^2}$.

1.2.4 Section 3: Simulation and Analysis

In this section, we include the parameters k_n and V_{th} into the model file and simulate the schematic in Ltspice as shown in Fig[1]. The simulation involves a DC sweep on V_{gs} from 0 to 5 V, with $V_{ds} = 5$ V and $V_{bs} = 0$ V. We then plot I_d versus V_{gs}.

After simulating the circuit, we extract the simulation data (Id and Vgs values) from LtSpice. This data is then plotted in Excel along with the experimental data.



2 Common Source (CS) Amplifier with Resistive Load

2.1 Aim :

The aim of the experiment is to investigate, observe, or test a hypothesis, theory, or phenomenon through procedures or measurements, aiming to gather data and analyze results to draw conclusions or validate hypotheses.

2.2 Hand Calculations for Design

1. **Calculate Drain Current (I_D):**

- Use the expression for drain current in saturation region:

$$I_D = \frac{k_n}{2}(V_{in} - V_{th})^2$$

- We also know that $V_{out} = V_{DD} - I_D \cdot R_D$.

2. **Determine DC Bias Voltage (V_{bias}):**

   - Apply the constraint for transistor saturation:

$$V_{DD} - V_m = \frac{1}{2}A_v(V_{in} - V_{th})^2 + V_{th}$$

   - Solve for V_{in}, which represents the DC bias voltage.

3. **Choose Drain Resistance (R_D):**

   - R_D can be chosen based on desired DC operating point and AC small signal gain. You may use load line analysis to determine an appropriate value.

4. **Calculate DC Output Voltage (Aim):**

   - Once R_D is chosen, use the equation for V_{out} to calculate the DC output voltage.

2.3 Hand Calculations for Gain Specifications

In this section, we perform hand calculations to meet the gain specifications using the extracted parameter values for k_n and V_{th}.

To determine the voltage gain (A_v), we utilize the equation:

$$20 = 20\log(A_v)$$

which yields $A_v = 10$.

Subsequently, we calculate the input voltage (V_{in}):

$$V_{in} = \frac{V_{DD} - V_m}{1 + \frac{A_v}{2}} + V_{th}$$

$$V_{in} = \frac{4.5\,\text{V}}{1+5} + 0.46 = \frac{4.5\,\text{V}}{6} + 0.46 = 0.75\,\text{V} + 0.46 = 1.24\,\text{V}$$

Given that $g_m = k_n(V_{in} - V_{th})$, and $g_m = 371.25 \times 10^{-6}$, we find $g_m R_D = A_v$.

Thus, the value of R_D is calculated as:

$$R_D = \frac{A_v}{g_m} = \frac{10}{371.25 \times 10^{-6}} = 27\,\mathrm{k\Omega}$$

.

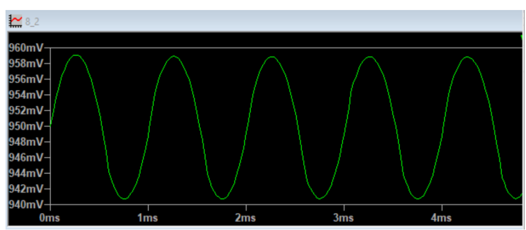
Starting with the expression for drain current (I_d):

$$I_d = \frac{k_n}{2}(V_{in} - V_{th})^2$$

Finding $I_d = 139.21 \times 10^{-6}$, we calculate the output voltage (V_{out}):

$$V_{out} = V_{DD} - I_d \cdot R_D = 1.28\,\mathrm{V}$$

2.4 LtSpice Simulation



2.5 Determination of Gain (A_v)

In this subsection, we determine the gain (A_v) of the amplifier.

Observed gain:

$$A_v = \frac{1}{0.1} = 10$$

The observed gain (A_v) is calculated to be 10.

2.6 DC Operating Point

In this section, we tabulate the DC operating point values for V_{gs}, V_{ds}, I_d, and g_m.

Parameter	Value
V_{gs}	1.24 V
V_{ds}	3.74 V
I_d	139.21 A
g_m	371.25 S

Table 1: DC Operating Point Values

3 Common Source (CS) Amplifier with Diode Connected Load

3.1 Aim

In this section, we discuss the design of a common-source amplifier with a diode-connected load.

3.2 Design

3.2.1 Explanation of Drain and Gate Connection of M2

The drain and gate of M2 are connected to each other. Therefore, if M2 is on, it will always be biased in the saturation region. This is because when the drain and gate of M2 are connected, the gate-source voltage (V_{gs}) of M2 is always equal to the drain-source voltage (V_{ds}), ensuring that M2 remains in saturation.

3.2.2 Condition for M1 Saturation

M1 will remain in saturation as long as $V_{out} > V_{in} - V_{th1}$. Thus, $V_{out} = V_{in} - V_{th1} + V_m$, where V_m is the margin voltage by which V_{out} is greater than $V_{in} - V_{th1}$.

3.2.3 Equation for Input Voltage

The current from M2 and M1 are the same. Therefore, $K_n(V_{in} - V_{th1})^2 = K_p(V_{DD} - V_{out} - V_{th2})^2$. The input voltage ($V_{in}$) can be expressed as:

$$V_{in} = \frac{qK_p}{K_n}(V_{DD} - V_{out} - V_{th2}) + V_{th1}$$

3.2.4 Calculation of Bias Voltage (V_{bias})

Let V_m be the margin voltage by which V_{out} is greater than $V_{in} - V_{th1}$. Substituting this in the equation for V_{in}, we can solve for V_{in}. This value will be the bias voltage (V_{bias}) of M1.

This completes the aim and design of the common-source amplifier with a diode-connected load.

3.3 Calculation

3.3.1 Voltage Gain (A_v)

$$A_v = \sqrt{\frac{K_p}{K_n}} = \sqrt{\frac{495}{200}} = \sqrt{2.475} = 1.407$$

3.3.2 Input Voltage (V_{in})

$$V_{in} = \sqrt{\frac{K_p}{K_n}}(V_{DD} - V_{out} - V_{th2}) + V_{th1}$$

$$V_{in} = \sqrt{\frac{K_p}{K_n}}(5\,\mathrm{V} - V_{out} - 1\,\mathrm{V}) + 1\,\mathrm{V}$$

$V_{in} = 2.013$

3.3.3 Output Voltage (V_{out})

$$V_{out} = V_{in} - V_{th1} + V_m$$

Given $V_m = 0.5$ and $V_{in} = 2.246$, we find $V_{out} = 2,28$.

3.4 LtSpice Simulation

3.5 Determination of Observed Gain ($A_{\mathbf{observed}}$)

In this subsection, we determine the observed gain (A_{observed}) of the amplifier.

The observed gain:

$$A_{\text{observed}} = 1$$

The observed gain (A_{observed}) is calculated to be 1.

3.6 Voltage and Gain Table

In this subsection, we tabulate the values of V_{in}, V_{out}, and A_v.

V_{in} **(V)**	V_{out} **(V)**	A_v
2.246	2.28	1.407

Table 2: Voltage and Gain Table

4 Current Mirror (CM) Design

4.1 Aim

The current mirror circuit aims to accurately replicate a reference current and distribute it reliably to the load.Its pivotal role lies in maintaining consistent current sourcing or sinking across the circuit, ensuring dependable and stable operation in diverse analog systems.

4.2 Design Concept

The basic idea is to generate a reference voltage (V_{GS1}) by pushing current (I_{REF}) into the diode-connected MOSFET (M1). This voltage is then used to bias another MOSFET (M2) such that it acts as a current source, providing the same current (I_{copy}) as the reference current (I_{REF}). Let's derive the equation for I_{COPY} in terms of I_{REF} and device parameters.

The current equation of a MOSFET, ignoring channel length modulation and biased in the saturation region, is given by:

$$I_{DS} = \frac{1}{2}\mu_{COX}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad (1)$$

Rearranging Equation (1), we obtain:

$$V_{GS} = \sqrt{\frac{2I_{DS}}{\mu_{COX}\frac{W}{L}}} + V_{TH} \quad (2)$$

Referring to Equation (2), we can write V_{GS1} as:

$$V_{GS1} - V_{TH1} = \sqrt{\frac{2I_{REF}}{\mu_{COX}\frac{W_1}{L_1}}} \quad (3)$$

Since $V_{GS1} = V_{GS2}$ and assuming $V_{TH1} = V_{TH2}$, we can write I_{COPY} as:

$$I_{COPY} = \frac{1}{2}\mu_{COX}\frac{W_2}{L_2}(V_{GS1} - V_{TH1})^2 \quad (4)$$

$$I_{COPY} = \frac{W_2}{L_2} I_{REF} \frac{W_1}{L_1}$$

4.3 Calculation

4.3.1 Calculation of V_{GS1}

$$\begin{aligned} V_{GS1} &= \sqrt{\frac{2 \cdot 2 \cdot 10^{-3}}{495 \times 10^{-6}}} \\ &= \sqrt{\frac{4}{495}} \\ &= 2.82\,\mathrm{V} \end{aligned}$$

4.3.2 Calculation of R_D

Given that $V_{DS1} = 2.82\,\mathrm{V}$, $I_D = 2 \times 10^{-3}\,\mathrm{A}$, $V_{DD} = 8\,\mathrm{V}$, and $R_D = 2.59\,\mathrm{k\Omega}$, we substitute these values:

$$\begin{aligned} \frac{V_{DD} - V_{DS1}}{I_D} &= R_D \\ \frac{8 - 2.82}{2 \times 10^{-3}} &= 2.59 \times 10^3 \\ \frac{5.18}{2 \times 10^{-3}} &= 2.59 \times 10^3 \end{aligned}$$

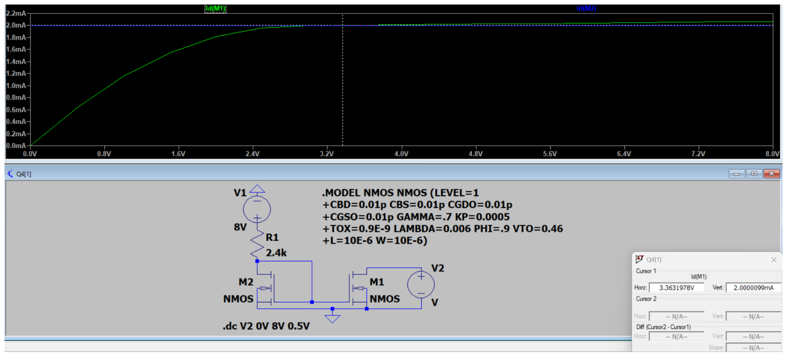
4.3.3 Calculation of V_{GS1} with V_{TH}

$$V_{GS1} = V_{DS1} + V_{TH} = 2.82 + 0.46 = 3.28\,\mathrm{V}$$

4.4 LtSpice Schematic

4.4.1 Observed V_{DS2}

The observed value of V_{DS2} is approximately $3.3631978\,\mathrm{V}$.



4.4.2 Relationship between V_{DS2} and V_{DS1}

In this circuit, V_{DS2} and V_{DS1} are equal due to the symmetry and design of the circuit.

Conclusion

In conclusion, I have successfully completed all parts of the assignment. Each section, including the design concepts, calculations, and observations, has been addressed comprehensively.