EE230: Analog LAB WEEK 4
Log and Antilog amplifier

Report by
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1 Square-root amplifier

1.1 Aim of the experiment

The experiment aims to design and analyze a square-root amplifier in analog electronics. Objectives include understanding theoretical principles like log and antilog, implementing a circuit, and evaluating performance through simulations or measurements.

1.2 Design

The basic principle idea behind designing a square root amplifier is to take the logarithm of the input, $\ln(V_{\text{in}})$, then scale it by half, $\frac{1}{2}\ln(V_{\text{in}})$, and finally take its anti-log to obtain $e^{\frac{1}{2}\ln(V_{\text{in}})} = \sqrt{V_{\text{in}}}$. The equation for the terminal characteristics of a pn junction diode in forward bias is given by:

$$I_D = I_S \cdot \left(e^{\frac{V_D}{nV_T}} - 1 \right)$$

We may approximate equation (1) as

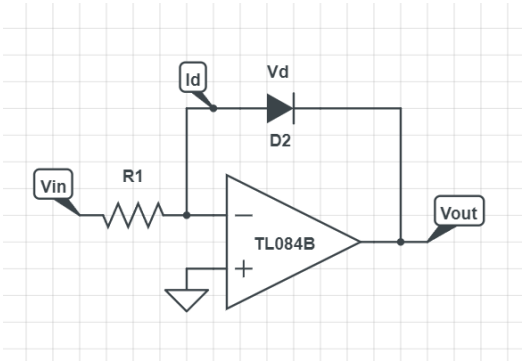
$$I_D = I_S \cdot e^{\frac{V_D}{nV_T}}$$

$$V_D = nV_T \cdot (\ln(I_D) - \ln(I_S))$$

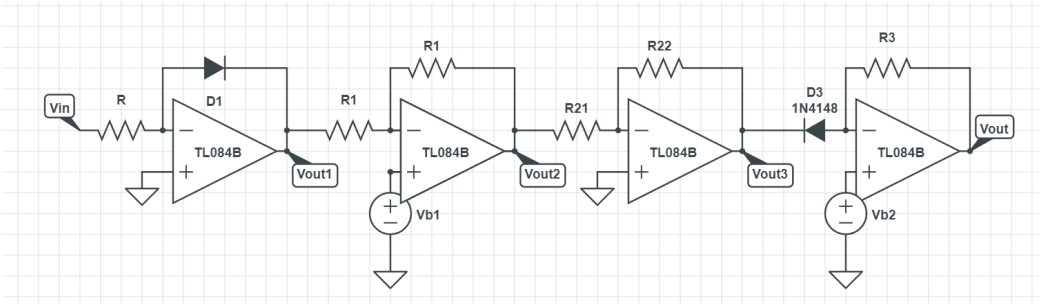
Equation (3) can be rewritten as

$$\ln(I_D) = \frac{V_D}{nV_T} + \ln(I_S)$$

A voltage can be easily converted to a current using the inverting amplifier configuration. The circuit is as follows:



The basic design of the square-root amplifier circuit involves taking the logarithm of the input voltage, scaling it by half, and then applying the anti-logarithm. The circuit can be represented as follows:



$$V_{\text{out1}} = -V_D \quad (1)$$

Substituting equation and rearranging,

$$V_{\text{out1}} = nV_T \cdot (\ln(ISR) - \ln(V_{\text{in}})) \quad (2)$$

Equation (2) can be written in the following form:

$$V_{\text{out1}} = -a_1 \ln(V_{\text{in}}) + a_2 \quad (3)$$

where,

$$a_1 = nV_T \quad (4)$$
$$a_2 = nV_T \ln(ISR)$$

The Block-2 is used for removing the offset from V_{out1} as shown in Figure 2.

$$V_{\text{out2}} = -V_{\text{out1}} + 2V_{b1} \quad (5)$$
$$0 = a_1 \ln(V_{\text{in}}) - a_2 + 2V_{b1} \quad (6)$$

Set $V_{b1} = \frac{a_2}{2}$ in equation (6). So the input to Block-3 would be $a_1 \ln(V_{\text{in}})$.

$$V_{\text{out3}} = -a_1\beta \ln(V_{\text{in}}) = \ln(V_{\text{in}})_1^a\beta$$

In the equation above, β is the magnitude of the gain for Block-3, which is given by $\frac{R_{22}}{R_{21}}$. The current I_{D2} flowing through diode $D2$ will also flow through resistor $R3$, then V_{out} will be

$$V_{\text{out}} = R3I_{D2} + V_{b2} \quad (8)$$
$$V_{\text{out}} = R3IS_2 e^{\frac{V_{b2}-V_{\text{out3}}}{n_2 V_T}} + V_{b2} \quad (9)$$

If you substitute V_{out3} and a_1 in equation (9), then the final V_{out} will be

$$V_{\text{out}} = R3IS_2 e^{\frac{V_{b2}}{n_2 V_T}} \left(\frac{V_{\text{in}}}{n_1 n_2 \beta} + V_{b2}\right) \quad (10)$$

The voltage across resistor $R3$ would be

$$V_{R3} = V_{\text{out}} - V_x = R3IS_2 e^{\frac{V_{b2}}{n_2 V_T}} \left(\frac{V_{\text{in}}}{n_1 n_2 \beta}\right) \quad (11)$$
$$V_{R3} = b_1 V_{b2}^{b_2 \text{in}} \quad (12)$$

where,

$$b_1 = R3IS_2 e^{\frac{V_{b2}}{n_2 V_T}} \quad (13)$$
$$b_2 = \frac{n_1}{n_2 \beta} \quad (14)$$

Choosing $b_1 = 1$, $b_2 = \frac{1}{2}$, and substituting ,then V_{R3} would be

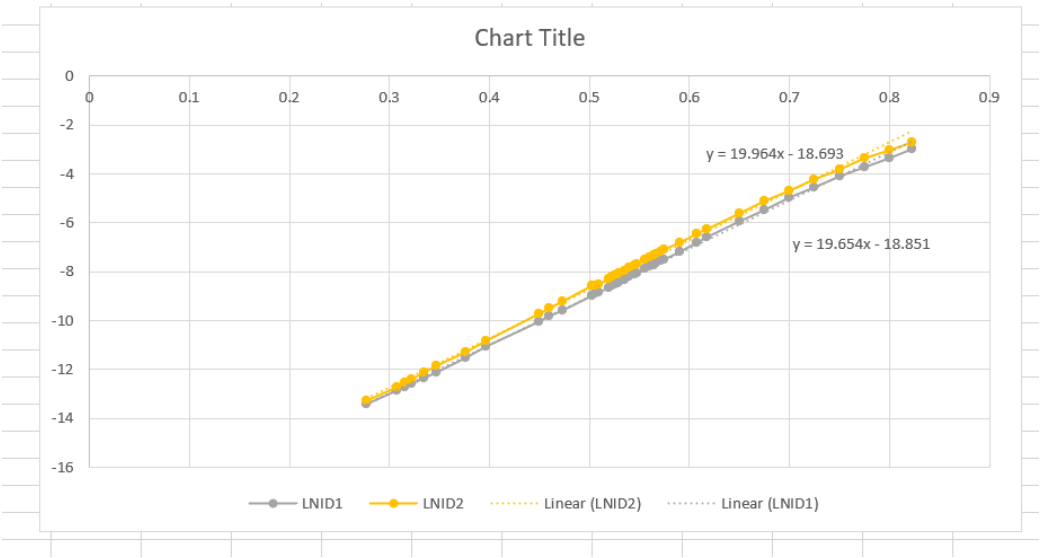
$$V_{R3} = \sqrt{\frac{1}{2} V_{\text{in}}} \quad (15)$$

The voltage across resistor $R3$ is our final output, which is the square root of the input voltage.

1.3 Experimental results

1.3.1 Part i. Voltage characteristics of two diodes

Plot $\ln(I_D)$ versus V_D as shown below for plotting the experimental data.



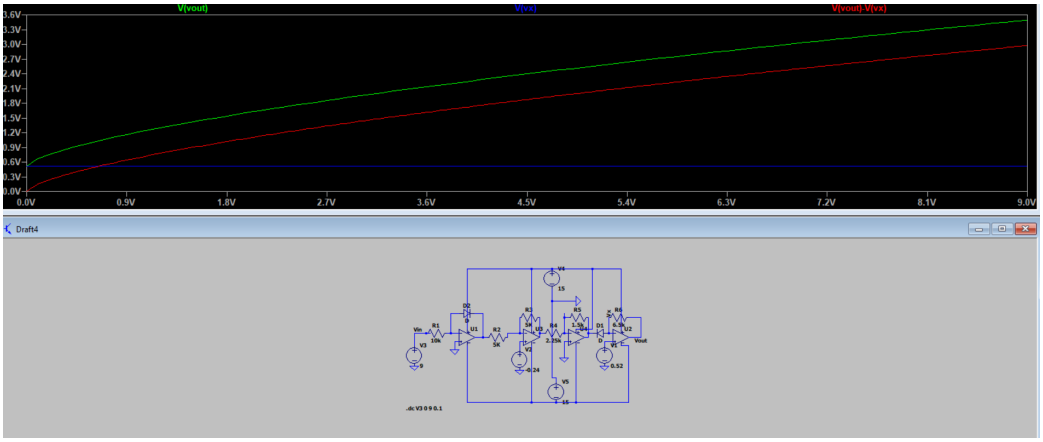
By comparing $D1$ and $D3$, for the current range over which $\ln(I_D)$ versus V_D is linear, note that the slopes $\left(\frac{1}{nV_T}\right)$. Since V_T is a constant at a given temperature, we may conclude that the ideality factor, The value of V_T at 27°C or 300 K, as you may verify, is 0.026 V, and $\frac{1}{nV_T}$=1.926, so n=1.956.Similarly, for the second equation, $\frac{1}{nV_T} = 19.964$, leading to n=1.926.

The y-intercept of $\ln(I_D)$ versus V_D is $\ln(IS)$. Hence, the saturation current can be estimated from the y-intercept. $\ln(IS) = -18.851$, so IS=6.5030 $\times$ 10^{-9}.Additionally, $IS_2 = 7.61 \times 10^{-9}$.

1.3.2 Part ii.SPICE model file for both the diodes.

1.3.3 Part iii.Range of diode currents and R

The relationship between $\ln(ID)$ and VD is linear. For instance, $ID1 = 0.0000155$ and $ID2 = 0.0011359$. The linearity indicates the validity of the diode model for this range of currents.
Given $r = \frac{15}{ID2}$, when evaluating, we find that $r \approx 11037.527$.



1.3.4 Part iv Expression for Vout1

$$V_{\text{out1}} = nV_T \cdot (\ln(ISR)) - \ln(V_{\text{in}})$$

1.3.5 Part v Expression for Vb1

$$a_2 = n_1 V_T \ln(ISR)$$

$$V_{\text{out2}} = a_1 \ln(V_{\text{in}}) - a_2 + 2V_{b1}$$

Set $V_{b1} = \frac{a_2}{2}$. $a_2 = 1.957 \times 0.026 \times \ln(6.503 \times 11037 \times 10^{-9})$, we get $a_2 \approx -0.48551$. Therefore, $Vb1 \approx 0.24$.

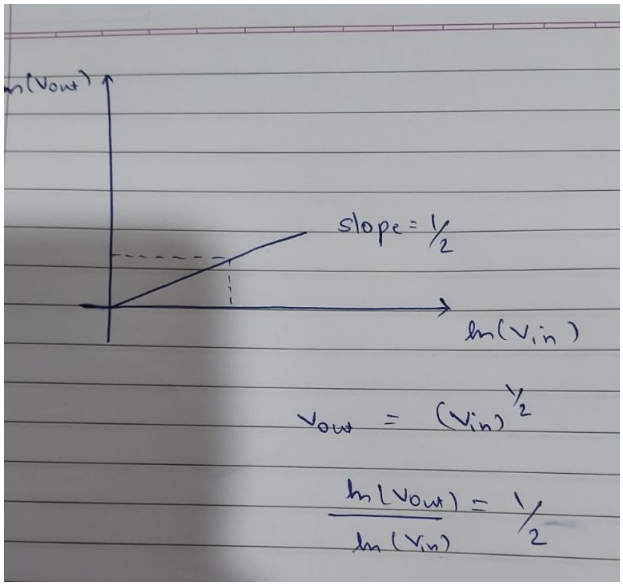
1.3.6 Part vi Expression for R3

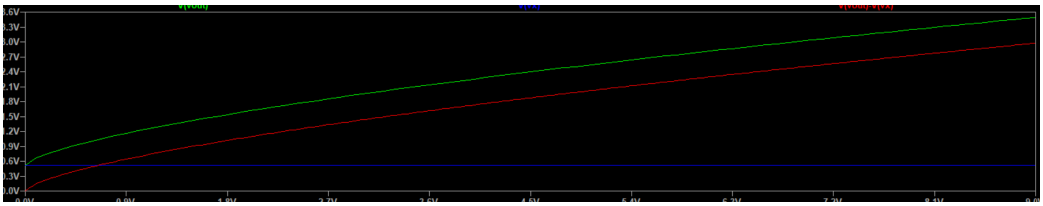
$$R_3 \cdot I_{S2} \cdot e^{\frac{V_{B2}}{N_2 V_T}} = 1$$

Given that $V_{B2} = 0.52$, $V_T = 0.026$, and $I_{S2} = 6.503 \times 10^{-9}$, we find that $R_3 \approx 4063.5$.

1.3.7 Part vii. Ideal plot of ln(Vout) vs ln(Vin)

The graph obtained in LTspice is as follows:





1.4 Conclusion and Inference

In conclusion, the square-root amplifier circuit demonstrated linearity, validated through $\ln(ID)$ versus VD. Diode model comparisons revealed variations in ideality factors and saturation currents. Circuit equations, validated by experimental data, emphasized its functionality. Overall, the circuit successfully converted input voltage to the square root of the output.

1.5 Experiment completion status

Completed all sections of this Question.