EE230: Analog Circuits Lab
Lab No. 10-11

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1 Differential Amplifier with Resistive Load

1.1 Aim of the experiment

Simulating and experimenting with a differential amplifier circuit with a resistive load, amplifying the small signal AC component of the input Voltage.

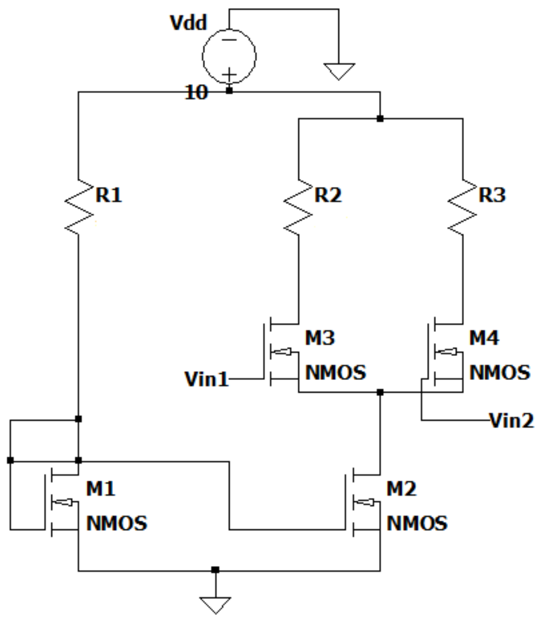
1.2 Design

For the circuit, the differential gain, A_v is given by:

$$A_v = R_2 * \sqrt{I_{tail} K_{n1}} \tag{1}$$

and the output common mode voltage is:

$$V_{outcm} = V_{DD} - \frac{I_{tail} R_2}{2} \tag{2}$$



1.3 Simulation

For the specifications:
Gain > 12dB
, $V_{incmmin}$ = 3.5V
and 5V < $V_{outcmmin}$ < 7V
and keeping $Kn = 0.53mA/V^2$, $Kp = 0.16mA/V^2$, V_{thn} = 0.45V, V_{thp} = -0.5 V.

Choosing the following values:

$A_v = 5$
$R_2 = R_3 = 7.47\text{k}\Omega$
$V_{outCM} = 6.84\text{V}$
$I_{tail} = 0.846\text{mA}$
$R_1 = 9.17\text{k}\Omega$

$V_{GS1} = V_{DS1} = V_{GS2}$	2.23V
V_{DS2}	2.8V
V_{out1}	6.83V
V_{out2}	6.83V
I_{ref}	0.846mA

1.4 Simulation Results

1.4.1 Large signal(DC) response

1.4.2 Vin1 sweep

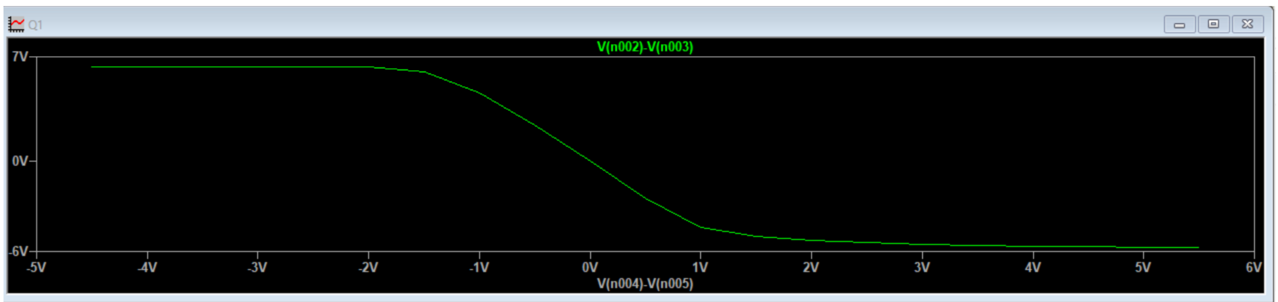


Figure 1: (Vout1 - Vout2) vs (Vin1 - Vin2)

1.4.3 Small signal(AC) response

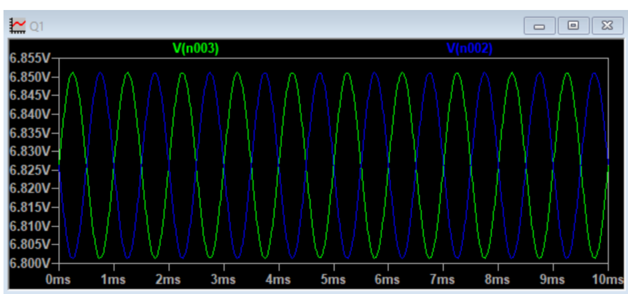


Figure 2: Vout1 and Vout2

So the small signal gain comes out to be:

$$A_v = 5 \tag{3}$$

1.5 Experiment Results

1.5.1 Large signal analysis

$V_{in1} = V_{in2} = 4.5$V
The following values were observed: $V_{out1} = 6.36$V
$V_{out2} = 6.75$V

All MOSFETS were observed to be in saturation.

1.5.2 Small Signal Analysis

$V_{in1} = 20$ mVpp, 1kHz sinusoid with 4.5 DC offset
$V_{in2} = 20$ mVpp, 1kHz sinusoid with 4.5 DC offset, out of phase with V_{in1}
The following values were observed:
$V_{out1} = 112$ mVpp, 1kHz sinusoid
$V_{out2} = 112$ mVpp, 1kHz sinusoid out of phase with V_{out1}
We observed a 180 degree phase shift as well. So the small signal gain comes out to be:

$$A_v = \frac{112}{20} = 5.6 \tag{4}$$

1.6 Conclusion and Inference

This experiment demonstrated the method to bias a MOSFET in the correct region (saturation), and also demonstrated the construction of a differential amplifier with a resistive load.

1.7 Experiment completion status

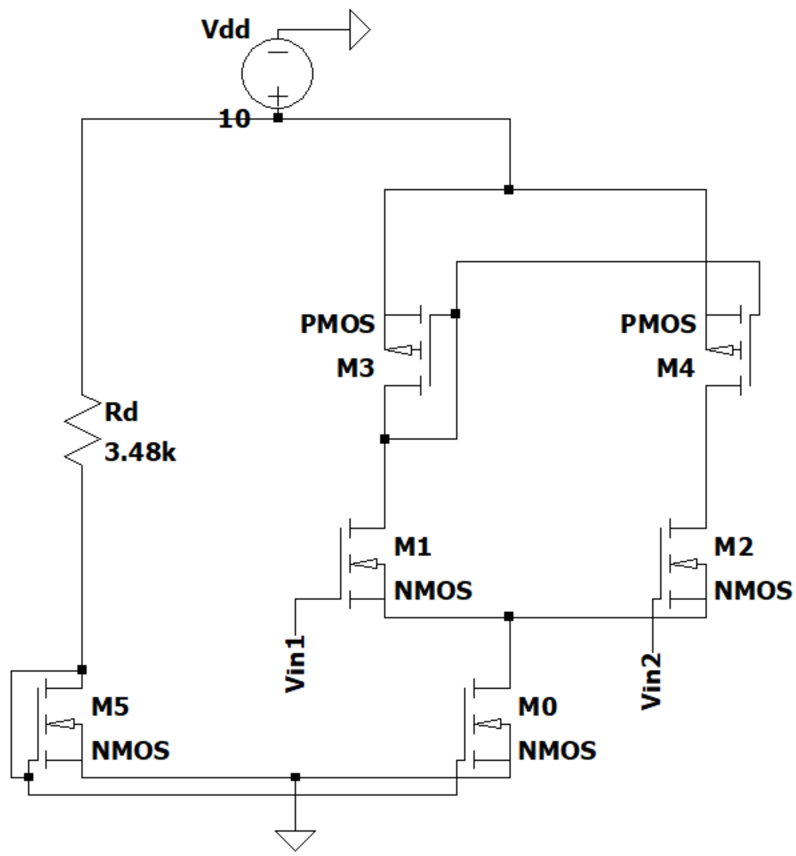
Completed.

2 Differential Amplifier with Diode connected Load

2.1 Aim of the experiment

Simulating and experimenting with a differential amplifier circuit with a diode connected load, amplifying the small signal AC component of the input Voltage.

2.2 Design



For the circuit, the differential gain, A_v is given by:

$$A_v = -g_{m1}(r_{o2}||r_{o4}) \tag{5}$$

where

$$r_o = \frac{1}{\lambda I_D} \tag{6}$$

and the output DC mode voltage is:

$$V_{outDC} = V_{DD} - \sqrt{\frac{I_o}{K_n}} - V_{th} \tag{7}$$

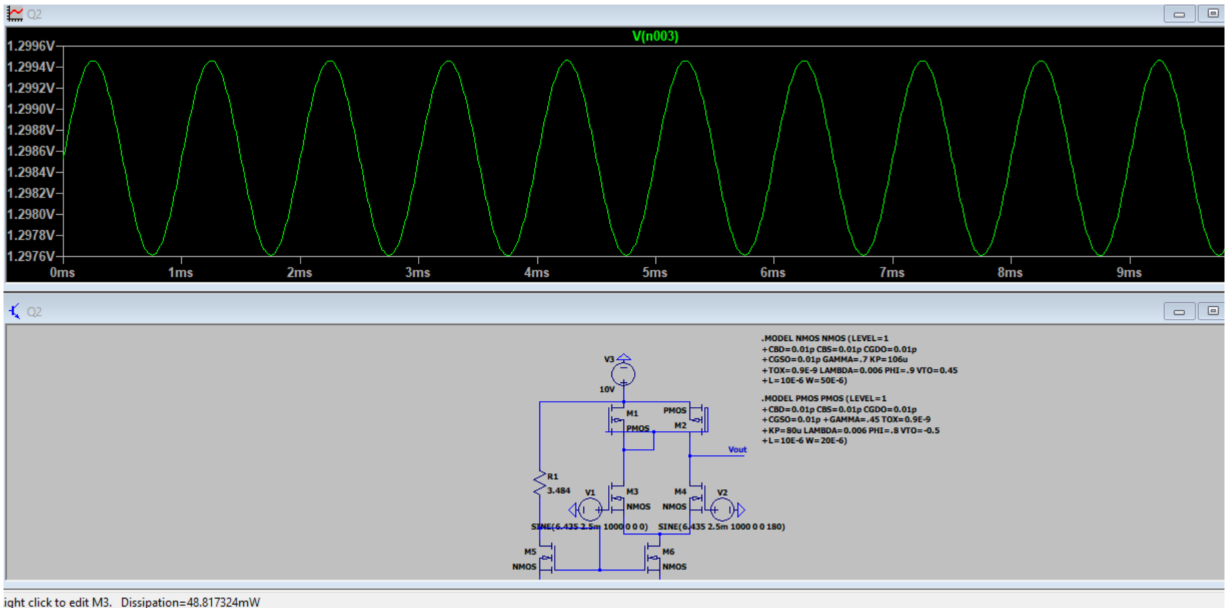
2.3 Simulation

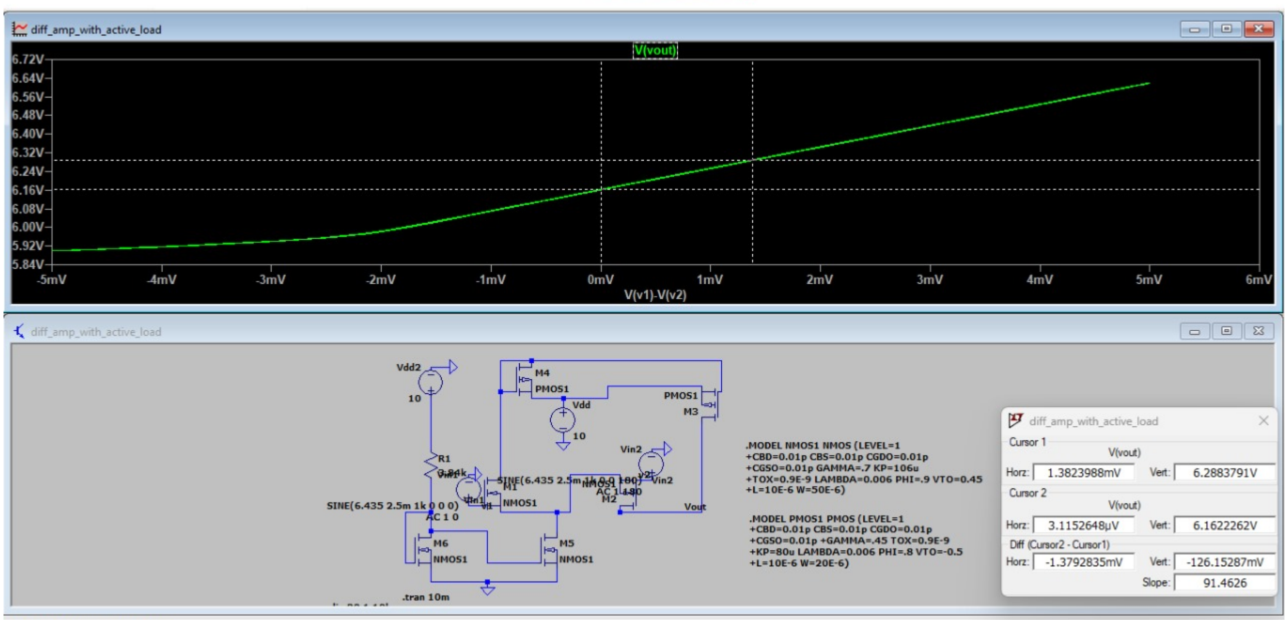
For the specifications:
V_{outDC} = 6V
V_{DD} = 10V
we get
5.1V < V_{incm} < 6.45V
and keeping $Kn = 0.53mA/V^2$, $Kp = 0.16mA/V^2$, V_{thn} = 0.45V, V_{thp} = -0.5 V.
I_o = 1.96mA
R_D = 3.48kΩ
V_{D05} = 3.63V
V_{incm} = 5.7V

2.4 Simulation Results

2.4.1 Large signal(DC) response

$V_{in1} = V_{in2}$	5.7V
V_{DS5}	3.15V
V_{GS0}	3.15V
V_{DS0}	3.337V
V_{out}	6.03V
V_{g3}	6.03V


V(n003)
1.2996V
1.2994V
1.2992V
1.2990V
1.2988V
1.2986V
1.2984V
1.2982V
1.2980V
1.2978V
1.2976V
0ms
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
.MODEL NMOS NMOS (LEVEL=1
+CBD=0.01p CBS=0.01p CGDO=0.01p
+CGSO=0.01p GAMMA=.7 KP=106u
+TOX=0.9E-9 LAMBDA=0.006 PHI=.9 VTO=0.45
+L=10E-6 W=50E-6)
.MODEL PMOS PMOS (LEVEL=1
+CBD=0.01p CBS=0.01p CGDO=0.01p
+CGSO=0.01p +GAMMA=.45 TOX=0.9E-9
+KP=80u LAMBDA=0.006 PHI=.8 VTO=-0.5
+L=10E-6 W=20E-6)
Vout
SINE(6.435 2.5m 1000 0 0 0)
SINE(6.435 2.5m 1000 0 0 180)
ight click to edit M3. Dissipation=48.817324mW


diff_amp_with_active_load
V(vout)
6.72V
6.64V
6.56V
6.48V
6.40V
6.32V
6.24V
6.16V
6.08V
6.00V
5.92V
5.84V
-5mV
-4mV
-3mV
-2mV
-1mV
0mV
1mV
2mV
3mV
4mV
5mV
6mV
V(v1)-V(v2)
Cursor 1
Horz: 1.3823988mV
Vert: 6.2883791V
Cursor 2
Horz: 3.1152648µV
Vert: 6.1622262V
Diff (Cursor2 - Cursor1)
Horz: -1.3792835mV
Vert: -126.15287mV
Slope: 91.4626
.MODEL NMOS1 NMOS (LEVEL=1
+CBD=0.01p CBS=0.01p CGDO=0.01p
+CGSO=0.01p GAMMA=.7 KP=106u
+TOX=0.9E-9 LAMBDA=0.006 PHI=.9 VTO=0.45
+L=10E-6 W=50E-6)
.MODEL PMOS1 PMOS (LEVEL=1
+CBD=0.01p CBS=0.01p CGDO=0.01p
+CGSO=0.01p +GAMMA=.45 TOX=0.9E-9
+KP=80u LAMBDA=0.006 PHI=.8 VTO=-0.5
+L=10E-6 W=20E-6)
.tran 10m

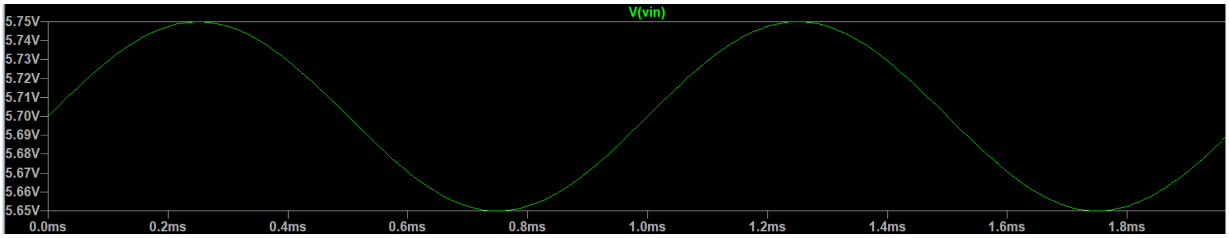
2.4.2 Small signal(AC) response

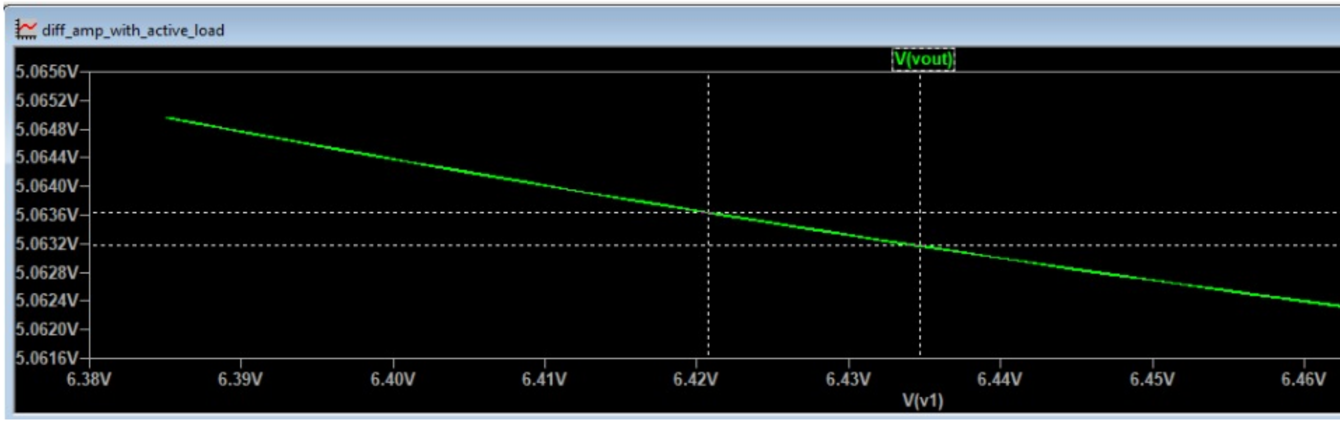
So the small signal gain comes out to be:

$$A_v = 86.80 \tag{8}$$

While the hand calculated value is 86.67, which is pretty close to this value.

2.4.3 Common mode gain





Which gives the common mode gain = 0.01.

2.5 Experiment Results

2.5.1 Large signal analysis

$V_{in1} = V_{in2} = V_{inCM} = 5.5$V
$V_{out} = 6.4$V
$V_{gs} = 2$V
$V_{ds} = 4.1$V
$I_{ref} = 1.27$mA
All MOSFETs observed to be in saturation.

2.5.2 Small Signal Analysis

$V_{in1} = 20$ mVpp, 1kHz sinusoid with 5.5V DC offset
$V_{in2} = 20$ mVpp, 1kHz sinusoid with 5.5V DC offset, out of phase with V_{in1}
The following values were observed:
$V_{out} = 3.3$Vpp, 1kHz sinusoid, with an offset of 5.9 V. So the small signal gain comes out to be:

$$A_v = \frac{3.3}{0.04} = 85 \tag{9}$$

All MOSFETS were observed to be in saturation.

2.6 Conclusion and Inference

This experiment demonstrated the method to bias a MOSFET in the correct region, and also demonstrated how to build a differential amplifier with diode connected load.

2.7 Experiment completion status

Completed.

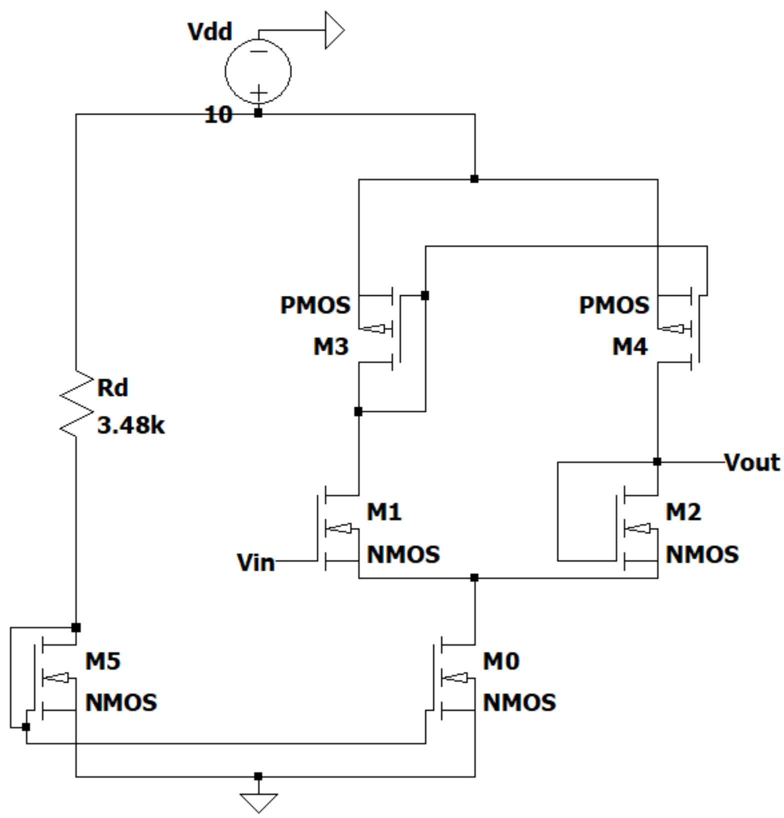
3 Five Transistor OTA Design

3.1 Aim of the experiment

Simulating and experimenting with different applications of the 5T-OTA circuit, including an inverting amplifier, a unity gain amplifier and a differentiator.

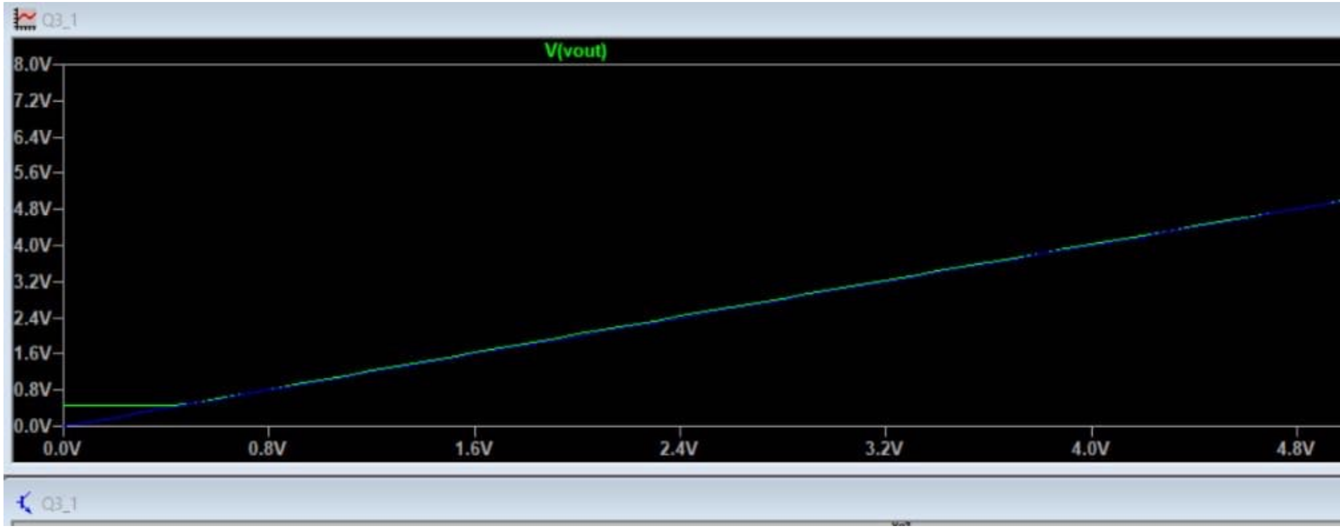
3.2 Unity Gain Amplifier

3.2.1 Design

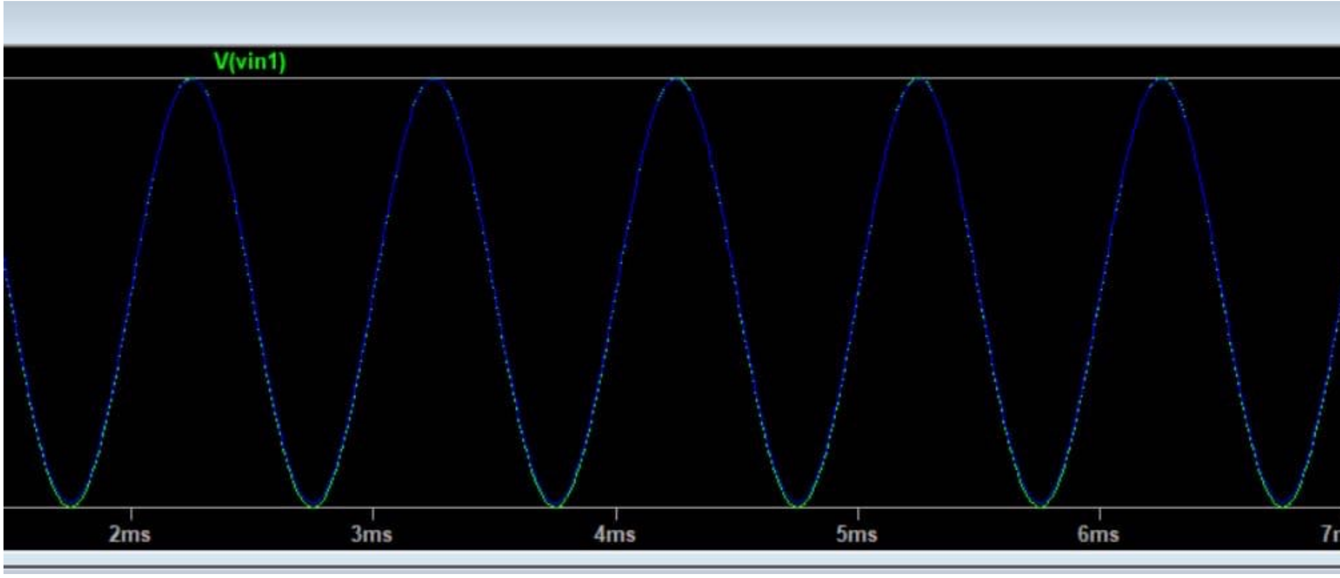


3.2.2 Simulation

Vin DC SWEEP



SINUSOIDAL INPUT

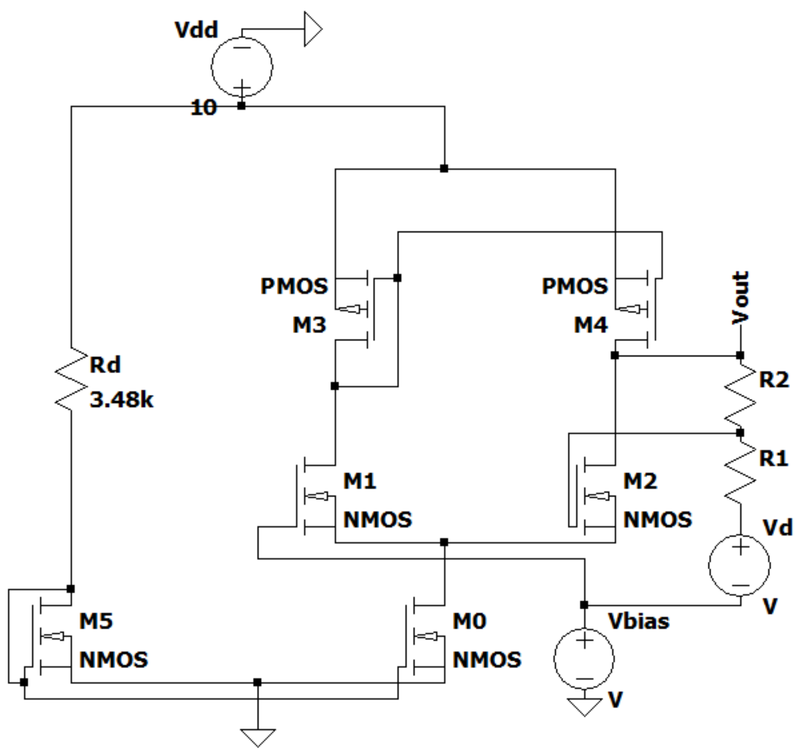


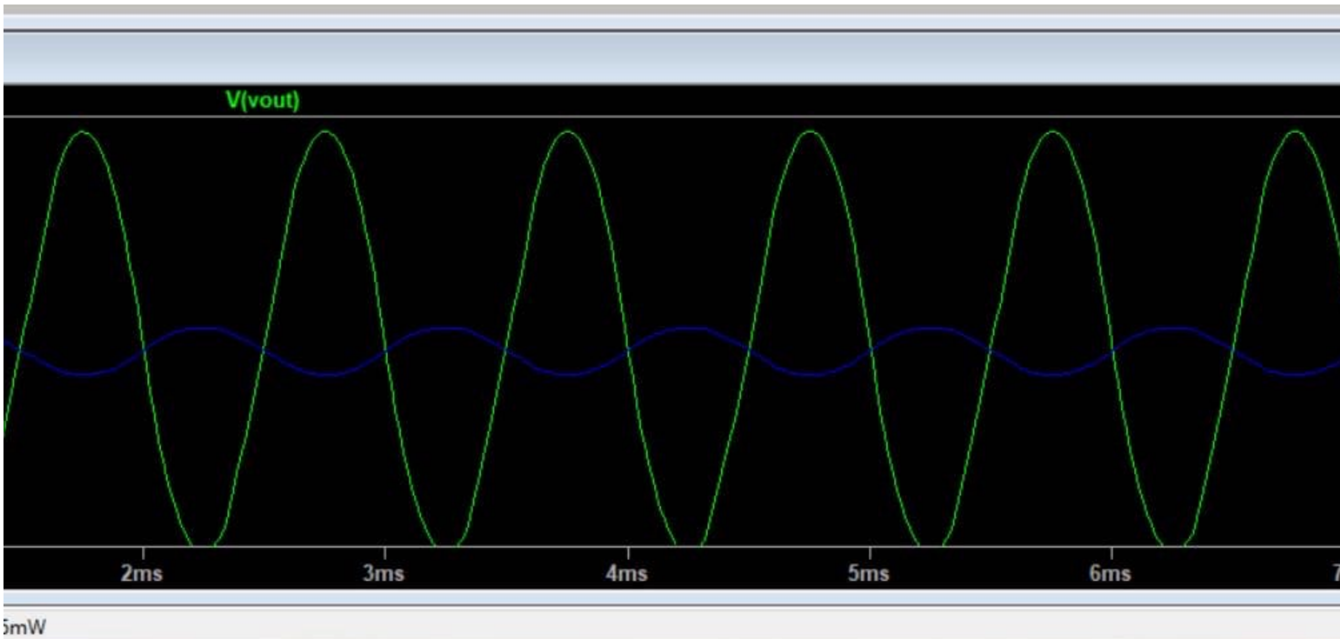
3.2.3 Experimental Results

$R_D = 3.4\text{k}\Omega$
V_in = sinusoid of 1V peak to peak amplitude, 1kHz frequency and an offset of 5.5V
V_{outAC} = sinusoid with 1V peak to peak, from 5.53 to 6.53 V.

3.3 Inverting Amplifier

3.3.1 Design





3.3.2 Simulation

3.3.3 Experimental Results

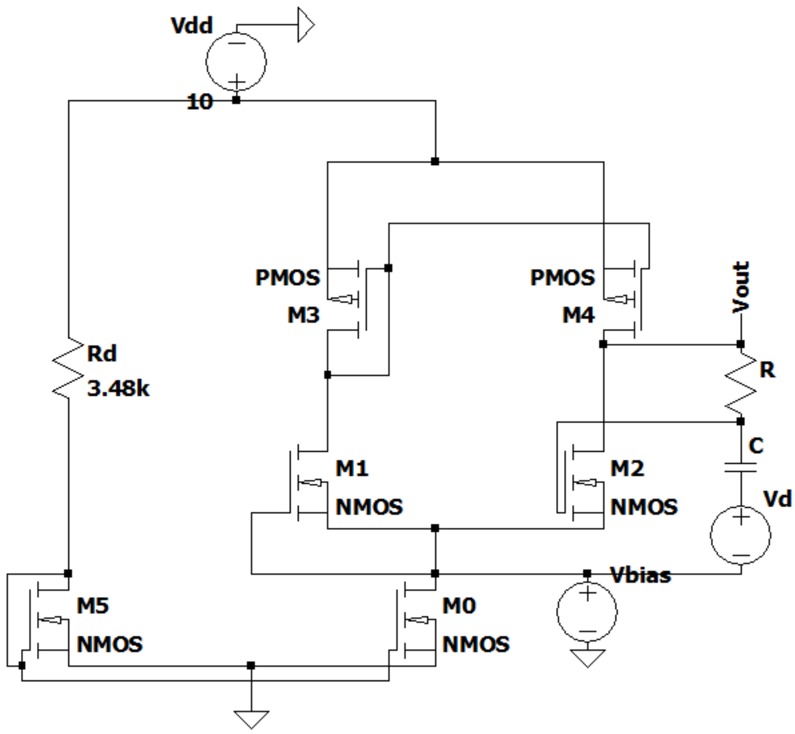
V_{bias} = 5.5V
R_2 = 10 MΩ
R_1 = 1 MΩ
V_d = 50 mVpp, 1kHz sinusoid
The output observed was a 499.2 mVpp, 1kHz sinusoid
So the gain is A_v = -167 degrees

3.4 Differentiator

3.4.1 Design

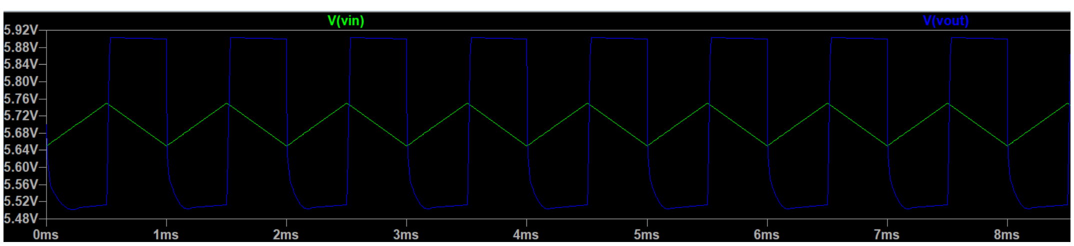
for this circuit:

$V_{outpp} = \frac{f * V_{inpp}}{250}$ where f = frequency (Hz) of the input waveform



3.4.2 Simulation

Keeping Vin as triangular waveform of 100 mVpp, 1 KHz frequency, with C = 100pF, R = 10MΩ



3.4.3 Experimental Results

For V_{in} = 100mVpp, 1kHz sinusoid, V_{out} = 400mVpp, we observed a triangular waveform from 5.97 V to 6.10 V.

3.5 Conclusion and Inference

This experiment demonstrated the method to bias a MOSFET in the correct region, and also demonstrated a unity gain amplifier, an inverting amplifier and a differentiator circuit, using a 5T-OTA circuit.

3.6 Experiment completion status

Completed.