EE230: Analog Circuits Lab
Lab No.5

Abhineet Agarwal, 22B1219

February 7, 2024

1 Hardware Implementation of an Analog Square-root Circuit

1.1 Aim of the experiment

To understand the Log and Antilog amplifier to make a square root amplifier.

1.2 Design

The circuit is interconnected block by block, as depicted in the figure. The voltages V_{b1} and V_{b2} are generated using potentiometers connected between $V_{CC} = +15V$ and ground.

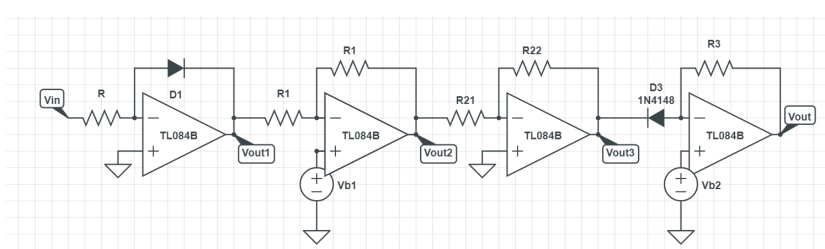

Figure 1: Analog square-root circuit

1.2.1 Section 1

A connection is established between the ground and V_{CC} through a potentiometer, with its central pin linked to the non-inverting terminal of the LM-741 Op-Amp IC. The inverting terminal and output of the 741-IC are interconnected and directed to R in Block 1.

1.2.2 Section 2

The inverting terminal of the Op-Amp is linked to R, while the non-inverting terminal is grounded. The positive side of diode $D1$ is connected to the inverting terminal of the Op-Amp, and the negative side is connected to the Op-Amp's output. The output of the Op-Amp is then connected to R_1.

$$R = 2.23\ k\Omega \tag{1}$$

1.2.3 Section 3

The inverting terminal of the Op-Amp is connected to R_1, and the non-inverting terminal is set to V_{b1}. The output of the Op-Amp is connected to R_{21}.

$$R_1 = 2\ k\Omega \tag{2}$$

$$R_{21} = 3\ k\Omega \tag{3}$$

Set V_{in} as 1V and change V_{b1} till $V_{out2} = 0V$.

1.2.4 Section 4

The inverting terminal of the Op-Amp is connected to R_{21}, and the non-inverting terminal is grounded, as shown in Fig. R_{22} is connected between the inverting terminal and the output of the Op-Amp. The output is also linked to the cathode of diode $D2$.

$$\begin{aligned} R_{22} &= R_{21}\beta \\ &= R_{21} b_2 \frac{n_2}{n_1} \end{aligned} \tag{4}$$

For square root amplifier $b_2 = \frac{1}{2}$ and $n_1 \approx n_2$

$$\begin{aligned} R_{22} &= \frac{R_{21}}{2} \\ &= 2.013k\ k\Omega \end{aligned} \tag{5}$$

R_{22} can varied to get different powers of V_{in} at the output.

1.2.5 Section 5

The Op-Amp's inverting terminal is linked to the anode of diode $D2$, while the non-inverting terminal is set to V_{b2}. R_3 is positioned between the inverting terminal and the Op-Amp's output. The output of the square-root amplifier is obtained across resistor R_3. The resistor's resistance is adjusted to ensure diode $D2$ operates in the linear region. V_{b2} is varied until $V_{out} = 1V$ for $V_{in} = 1V$.

$$R_3 = 0.827\ k\Omega \tag{6}$$

1.3 Simulation Results

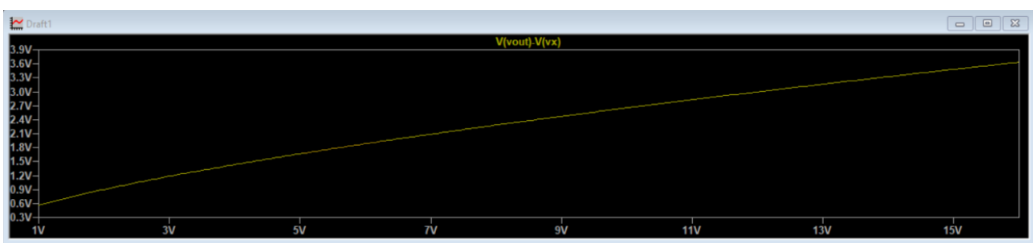

Figure 2: V_{out}

1.4 Experimental Results

Q1. Block 0 is used to implement the potentiometer which is used to give a large range of DC voltage from 0 to $+V_{CC} = 15V$.

Q2. If V_{in} is directly connected to V_{in1} then current will flow from resistor R which changes the input voltage, changing the output - input relation.

Q3.

$$Input\ Current = \frac{V_{in}}{R} \tag{7}$$

$$Input\ Voltage = V_{in} \tag{8}$$

$$\begin{aligned} Input\ Impedance &= \frac{V_{in}}{I_{in}} \\ &= R \end{aligned} \tag{9}$$

Q6.

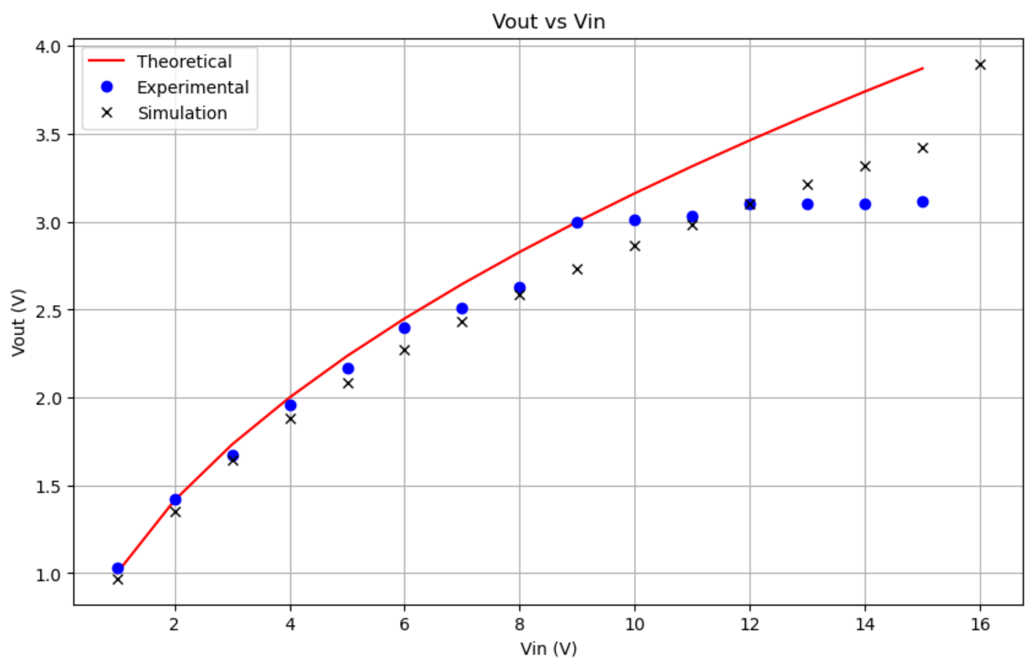

Figure 3: Simulated, Observed and Theoretical V_{out}s plotted against V_{in}

$$V_{b1} = -0.28V \tag{10}$$

$$V_{b2} = 0.6V \tag{11}$$

Q7. $V_{R_3} = V_{out4} - V_{out3}$ but since $V_x = V_{b2}$ due to virtual ground between inverting and non-inverting terminal of the Op-Amp.

$$V_{R_3} = I_{S_2} R_3 e^{V_{b2}/n_2 V_T} (V_{in})^{n_1 \beta / n_2} \tag{12}$$

V_{b2} is important to ensure correct biasing of diode. R_3 is for fine adjustment as $V_{R_3} \propto R_3 \propto \sqrt{V_{in}}$. Thus the potentiometer at the non-inverting terminal acts as a coarse adjustment, whereas the feedback resistor(R3) acts as a fine adjustment.

Q8.

Table 1: Observed Values fro V_{out}

V_{in}	V_{out}
1 V	1.03 V
2 V	1.42 V
3 V	1.67 V
4 V	1.96 V
5 V	2.17 V
6 V	2.40 V
7 V	2.51 V
8 V	2.63 V
9 V	3 V
10 V	3.01 V
11 V	3.03 V
12 V	3.10 V
13 V	3.10 V
14 V	3.10 V
15 V	3.12 V

Q9. Refer figure 8

Q10. Refer figure 9

Q11.

$$V_{out} = (V_{in})^{\frac{1}{2}} \tag{13}$$

$$ln(V_{out}) = \frac{ln(V_{in})}{2} \tag{14}$$

Therefore expected slope of $ln(V_{out})$ vs $ln(V_{in})$ graph $= \frac{1}{2}$

Q12. If the polarity of the diode D2 is reversed then V_{out} would not be proportional to positive power of V_{in}. The graph would be similar to $\frac{1}{\sqrt{V_{in}}}$

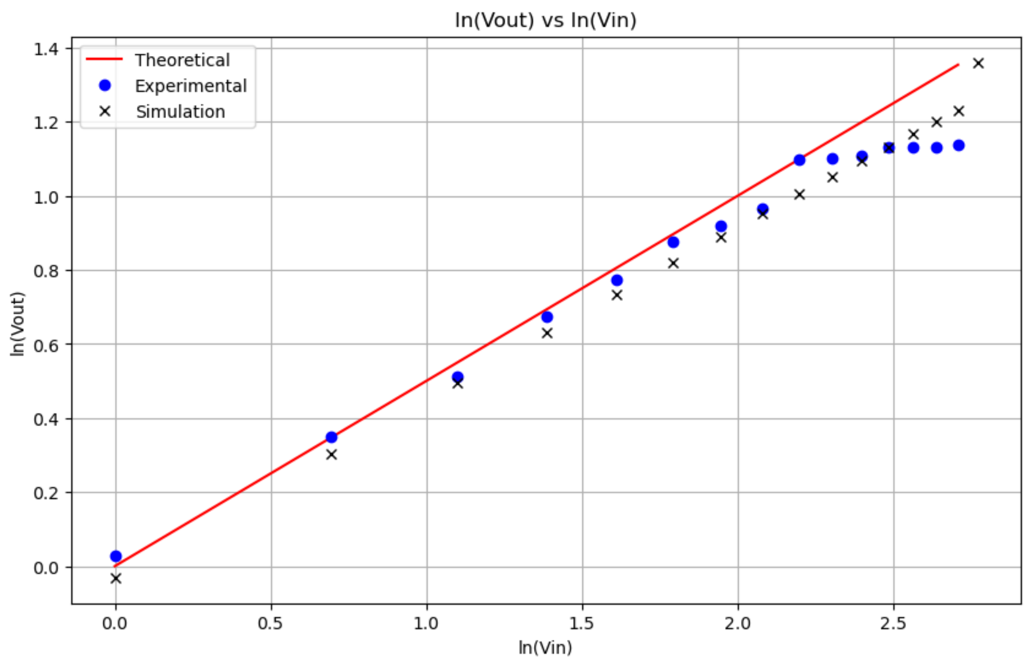

Figure 4: Simulated, Observed and Theoretical $ln(V_{out})$s plotted vs $ln(V_{in})$

1.5 Conclusion and Inference

- Potentiometers can be used to implement variable voltage source and variable resistors.
- The current conducted through a diode depends on voltage across it exponentially when it is not in saturation.
- OpAmps can be used as a Logarithmic amplifier with a non-ideal diode.

- OpAmps can be used as an Anti-logarithmic amplifier with a non-ideal diode..

1.6 Experiment completion status

Completed the experiment in its entirety in lab. Competed all sections and found answers to all the questions in the lab sheet.