Band-To-Band Tunneling in SOI MOSFET Modeling

EE724 Project Report - Stage 1
Abhineet Agarwal, Harsh Pujare, Kushagra Gehlot
Mentor - Jay Sonawane
Instructor - Prof. Udayan Ganguly
IIT Bombay, Powai, Mumbai, India - 400076

I. INTRODUCTION

Band-to-band tunneling (BTBT) is a quantum mechanical phenomenon that plays a significant role in the operation of semiconductor devices, particularly in Silicon-on-Insulator (SOI) MOSFETs. In SOI MOSFETs, where the channel is formed in a thin silicon layer over a buried insulator, BTBT can occur through direct tunneling through the silicon layer, trap-assisted tunneling via localized states in the energy band gap, or tunneling near the drain region. Understanding and accurately modeling BTBT is essential for optimizing device performance. Several models like the Hurkx, Schenk and non-local path model have been developed to describe BTBT in MOSFETS. These models offer insights into the mechanisms and parameters influencing BTBT, aiding in designing and analysing advanced semiconductor devices.

This project focuses on investigating BTBT effects in SOI MOSFETs utilizing TCAD simulations. In Stage 1, we focus on replicating the results of the reference paper [4] concerning the reduction of BTBT current in a 32nm PD-SOI MOSFET. In Stage 2, we will shift to a 22nm FDX-SOI MOSFET, and focus on device design for higher BTBT current.

II. MOTIVATION

Spiking Neural Networks (SNNs) are a type of artificial neural network that closely mimics the behaviour of biological neural networks. If implemented in silicon, these can lead to highly energy-efficient Artificial Intelligence (AI) computing solutions. Large SNNs require ultra-low power and low variability hardware for neuromorphic computing applications. In a quest to find the area and energy-efficient technology to realize SNNs, a band-to-band tunnelling (BTBT) regime-based neuron was proposed using Partially Depleted Silicon-on-Insulator (PD-SOI) technology. To ensure that these neurons remain energy efficient, a low BTBT current is required. The objective of this phase of the project was to recreate the device parameter optimisation results from the reference paper [4].

III. LITERATURE SURVEY

In band-to-band tunneling charge carriers tunnel through the forbidden energy band gap from one band to another [5]. Several models have been proposed to describe band-to-band tunneling.

- **Hurkx Model**: It describes BTBT as a result of the coupling of electronic states across the tunnel barrier. The model considers both the direct and indirect tunneling processes. Direct tunneling involves the transfer of carriers through the energy barrier, while indirect tunneling occurs via trap-assisted tunneling mechanisms. It provides a description of tunneling in terms of carrier energies, tunneling distance, and the effective mass of carriers [2].
- **Schenk Model**: This model focuses on the impact of the electric field on band-to-band tunneling. It considers the electric field dependence of tunneling probabilities and incorporates the effects of band non-parabolicity. It provides insights into the role of electric fields in enhancing or suppressing tunneling currents [3].
- **Nonlocal Path Model**: This model takes into account the nonlocal nature of tunneling paths in the device structure. It considers the contributions from multiple tunneling paths, accounting for their varying lengths and associated probabilities. It offers a more accurate representation of tunneling behavior in realistic device geometries compared to simpler models. In our simulations, we use the NLP model. [1].

  The primary reference paper [4] focuses on developing ultra-low power hardware for large spiking neural networks (SNNs). The researchers aim to minimize BTBT current in SOI-MOSFETs to achieve energy-efficient neuron implementation with low variability, essential for large-scale SNN performance. They conduct a comprehensive design space and variability analysis using TCAD simulations calibrated with experimental data from GlobalFoundries' 32nm PD-SOI MOSFET.
  The study also delves into the physics of tunnelling mechanisms and explores the impact of device design parameters on SOI MOSFET performance. The results of the study show a significant reduction in BTBT current by about 20x through device parameter optimization. They also find a high sensitivity of the BTBT regime from variability factors like random dopant fluctuations (RDF) and oxide thickness variability (OTV) while showing minimal sensitivity to channel-oxide interface traps (DIT).

IV. METHODOLOGY

The 32nm PD-SOI MOSFET fabricated at GF with gate length (LG)/width (W) of 40/450 nm was used. The electrical measurements were performed using an Agilent B1500 Semiconductor parameter analyzer. A well-calibrated Sentaurus TCAD deck was used. For design space analysis, variation in channel height (H_{CH}), buried oxide thickness (H_{BOX}), substrate height (H_{SUB}), drain-gate (D-G) and source-gate (S-

G) overlap length (L_{OV}), equivalent oxide thickness (T_{OX}), channel (N_{CH}) and source/drain doping (N_{SD}) were considered, and the simulation results were analysed to find ways to reduce the BTBT current.

V. RESULTS

- H_{BOX} and H_{CH} scaling has little effect on the BTBT current. This is primarily because BTBT predominantly occurs in the D-G overlap region.
- A slight increase in the BTBT current is observed as the D-G overlap (L_{OV}) increases. This maybe because of enhanced electric field at the junction.
- BTBT current increases with an increase in the channel doping (N_{CH}).
- Increase in the S-D doping (N_{SD}) leads to a large increase in the BTBT current.

Higher N_{CH} and N_{SD} values lead to a reduction in the depletion width at the drain-channel junction. This results in a steeper energy band profile, shorter tunnel lengths, and a higher electric field in the overlap region.

In all the graphs, I_D is the y axis and V_{GS} is the x axis.

VI. STAGE 2 PLAN

In stage 2, we will study band-to-band tunneling in a 22nm FDX-SOI MOSFET using simulations and design a MOSFET for higher BTBT current. As we have seen in the case of a PDSOI MOSFET, varying the parameters of a MOSFET which affect the D-G region affect the BTBT current. These are L_{OV}, N_{SD} and N_{CH}. Optimizing them for maximum BTBT current and at the same time, getting minimum variability in the BTBT as well as the ON and SS regions is our goal. Also, we will be studying the effects of temperature on the BTBT current and the effect of L_G scaling as we move from the 32nm PDSOI MOSFET to 22nm FDX.

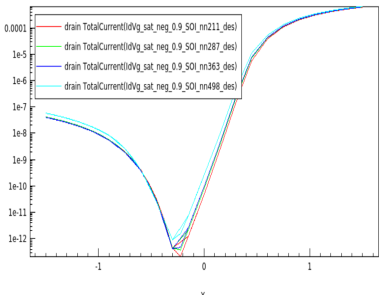

Fig. 1: Variation with H_{BOX}

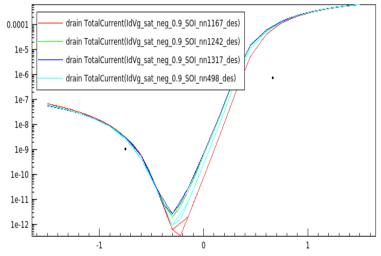

Fig. 2: Variation with H_{CH}

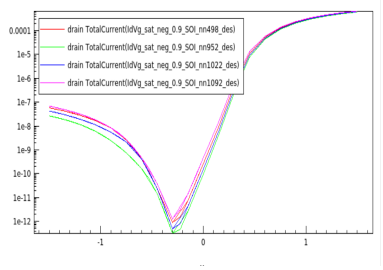

Fig. 3: Variation with L_{OV}

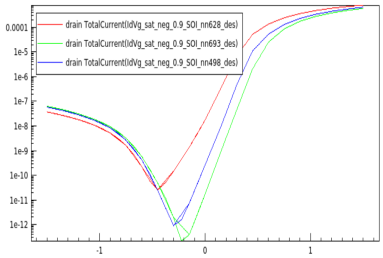

Fig. 4: Variation with N_{CH}

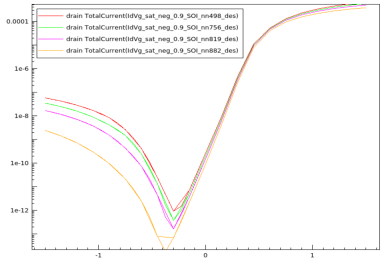

Fig. 5: Variation with N_{SD}

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