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# Developing the Guidelines for the Power MOSFET doping Profiles

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#### Abstract

The doping profile, which characterizes the spatial distribution of dopant atoms in the semiconductor material, plays a pivotal role in shaping the electrical characteristics of power MOSFETs. Our investigation involves a comprehensive study of various doping profiles and their effects on key parameters such as threshold voltage, on-state resistance, and switching speed.

Through detailed simulations and experimental analyses, we explore the trade-offs associated with different doping profiles, considering factors such as channel mobility, gate capacitance, and overall device reliability. The study aims to provide insights into optimizing the doping profile for enhanced power MOSFET performance under diverse operating conditions.

Furthermore, the report discusses the implications of doping variations on power MOSFET thermal behavior. Heat dissipation is a critical concern in power electronics, and understanding how doping profiles influence thermal resistance and junction temperature is imperative for designing efficient cooling solutions.

Our main aim of the project is to find the best suitable structure and a rough estimate of the doping profiles which can be implemented. The main structure which we have chosen is the tri-RESURF structure.

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#### Introduction

In this project, we have simulated the tri-RESURF structure for different doping profiles mainly for the p-n dilute region near the source for better breakdown voltage.

We have observed that the tri-RESURF structure reduces both the channel resistance and the major drift resistance and maintains the channel width for the proper functioning of the MOSFET. The Fin-Fet concept of minimizing the on-resistance is becoming popular.

The simulation for the project involves the software of tead which we have taken of 14 test cases for the simulation. In which there were 5 test cases of which the break down voltage of the MOSFET was more than 120V.

This project is made for the development of the doping profile levels at which the MOSFET can give the greater performance which can be used for many application. The main aim of the project to design and simulate a MOSFET structure which can handle of 100V and its efficiency should be more.

## Literature Review or Background

This project is made with the LDMOS RESURF structure. This structure is taken because the On resistance is minimal.

$$R_{\rm on} \approx R_{\rm channel} + R_{\rm drift}$$

This is because when the MOSFET is switched on there is creation of the depletion region near the sandwiched p region between the n substrate which reduces the drift resistance.

They have two electric field which reduces the bulk electric field. But they have the an interference electric field which creates a uniformly distributed over the base layer which increases the bulk electric field leading to higher breakdown voltage.

We consider the maximum doping level to be 1e+20 for the Base, Drain and Source. The On resistance was mainly was due to drift resistance which we reduced by sandwiching a p region between them now the other factor was the channel resistance we imporve the structure by a 3D Tri gate in the LDMOS power device.

We then find the optimum doping levels which the MOSFET can be working at higher voltages.

### Methodology or Approach

We are analyzing the structure for the Single-RESURF MOSFET with the doping profiles of:

$$N_{\rm sub} = 1 \times 10^{15} \tag{3.1}$$

$$N_{\rm ch} = 1 \times 10^{17} \tag{3.2}$$

$$N_{\rm nw} = 1 \times 10^{17} \tag{3.3}$$

$$V_{\rm g} = 12V \tag{3.4}$$

$$V_{\text{drain}} = 200V \text{ for the upper limit}$$
 (3.5)

We only change the values for the p substrate doping levels. We then analysis the structure at different doping levels of the by looking at the cross section of the structure. In the structure we take care of the channel width and the channel on resistance and the on resistance. However T resurf has two lower electric field peaks  $E_1$  and  $E_2$  which results in the reduced bulk the electric field concentration effect disappears.

The main part to modify was the On resistance which was the sum of the drift resistance and the channel resistance. For the drift resistance we used the RESURF structure which is having a pregion sandwiched between the n substrate. The sandwiched pregion provides the diffused region which reduces the drift resistance. For the channel resistance we use the 3-D structure of fin FET.

#### Results

We are plotting the graphs for  $V_{\text{drain}}$  Vs  $I_{\text{drain}}$  for the breakdown voltage. This will help to find the breakdown voltage.

Here we keep the  $N_{\rm sub}$  substrate doping to be  $1 \times 10^{15}$  constant,  $N_{\rm channel}$  channel doping to be  $1 \times 10^{17}$ ,  $N_{\rm nw}$  source and drain of the n region to be  $1 \times 10^{17}$ .

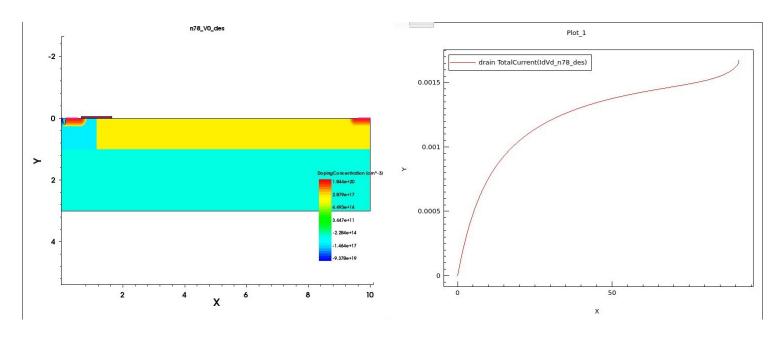


Figure 4.1:  $V_{\text{drain}}$  Vs  $I_{\text{drain}}$  MOSFET structure

With this MOSFET there is the break down at the 78V. With the p substrate doping level as  $5 \times 10^{15}$ .

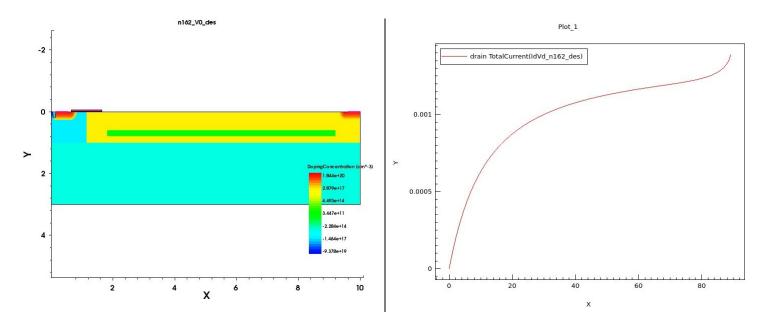


Figure 4.2:  $V_{\text{drain}}$  Vs  $I_{\text{drain}}$  MOSFET structure

With this MOSFET the breakdown occurs at the 90V which is better than the previous structure. This is because the doping of the p substrate to be  $1 \times 10^{17}$ .

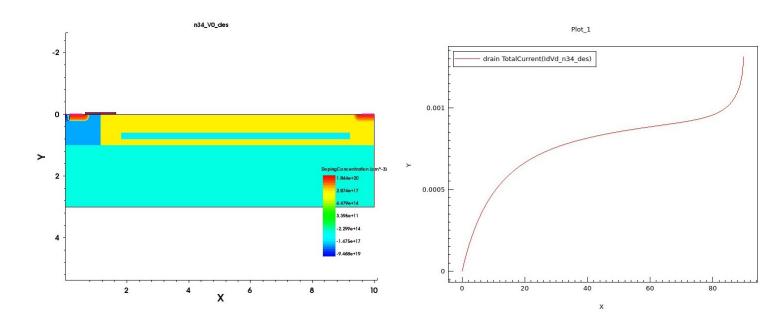


Figure 4.3:  $V_{\text{drain}}$  Vs  $I_{\text{drain}}$  MOSFET structure

With this MOSFET the breakdown occurs at the 85V because the p substrate doping level was made greater then the n source and drain which affects the breakdown voltage. The doping level was

 $2 \times 10^{17}$ .

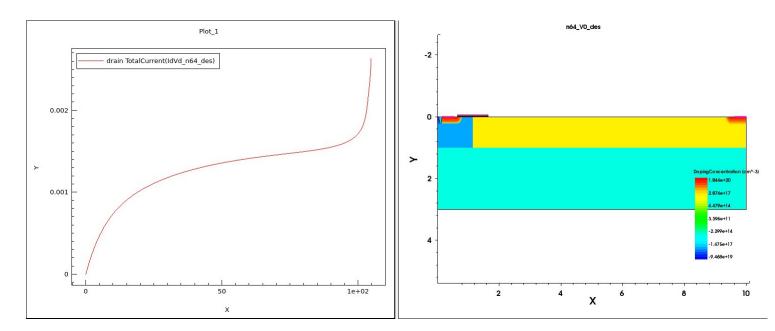


Figure 4.4:  $V_{\text{drain}}$  Vs  $I_{\text{drain}}$  MOSFET structure

With this structure we get the break down voltage at 120V which is much better than the others here the doping for the substrate changes from  $1 \times 10^{15}$  to  $5 \times 10^{16}$  with the substrate doping level to be  $1 \times 10^{15}$ , channel doping to be  $1 \times 10^{18}$  and the source and drain of the n region to be  $1 \times 10^{17}$ .

Here we observe that when doping level of the channel and the p substrate are  $\approx$  equal then the break down occur at the lower voltages.

When the p substrate and the source and the drain doping levels are also same then then break down Voltage starts to reduce.

#### Conclusion

Table 5.1: Structure of the designed Tri-RESURF MOSFET

Region	Peak Doping Concentratio	$\frac{0}{\text{depth}}$	Position	concentration type
P+bulk	1e+20	0.25	0-0.025	Gaussian
n+source	1e+20	0.25	0.125 - 0.62	Gaussian
n+drain	1+e20	-	9.5-10.0	Gaussian
p well	1e+20	1.0	0-1.145	constant
n well	1e+20	7.0	1.145-10	constant
p sub	1e+15	2.0	0-10	constant

After getting the graphs for the  $V_{\text{drain}}$  Vs  $I_{\text{drain}}$  the most MOSFET which can withstand the maximum voltage was the doping profiles of :

$$N_{\rm sub} = 1e + 15$$

$$N_{\rm ch} = 1e + 18$$

$$N_{\rm nw} = 1e + 17$$

$$N_{\rm pb} = 1e + 15to5e + 16$$

We observe the early breakdown when the doping profiles of the p substrate sandwiched and the channel doping profiles are the same.

This is for MOSFET with the substrate and the channel doping profiles being same  $N_{\text{sub}} = 1e + 15, N_{\text{ch}} = 1e + 18, N_{\text{nw}} = 1e + 17$  and  $N_{\text{pb}} = 1e + 18$ . Where the substrate and the channel have

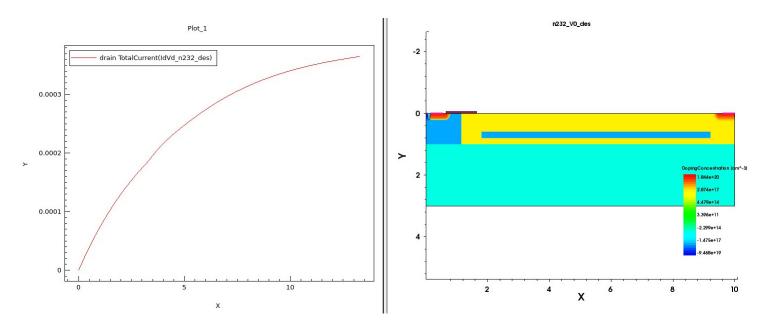


Figure 5.1:  $N_{\text{sub}} = 1e + 15, N_{\text{ch}} = 1e + 18, N_{\text{nw}} = 1e + 17$  and  $N_{\text{pb}} = 1e + 18$ 

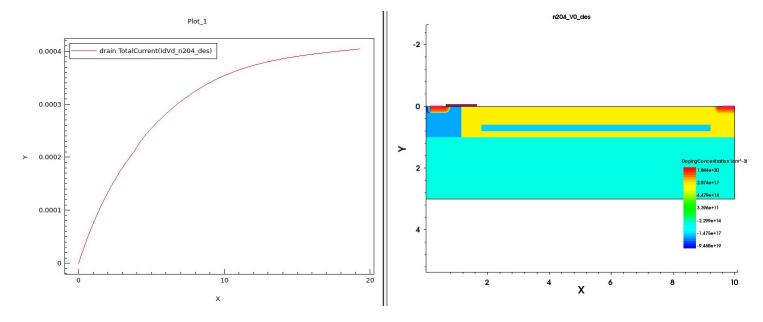


Figure 5.2:  $N_{\rm sub} = 1e + 15, N_{\rm ch} = 1e + 18, N_{\rm nw} = 1e + 17$  and  $N_{\rm pb} = 5e + 17$ 

the same doping levels which creates a greater on resistance because of the stringer depletion and the stronger electric field which leads to early breakdown. This structure breaks down at 20V.

### Acknowledgments

I would like to express my sincere gratitude to Prof. Nikhil K S for his invaluable guidance and support throughout the MOSFET doping levels project.

His expertise and insights have been instrumental in the successful completion of this work.

We were motivated to do the project and learn new concepts and get the knowledge of the reduced surface MOSFET and the LDMOS(linear diffusion Metal oxide semiconductor). We learnt the tead software for the simulation.

I am truly thankful for his time, patience, and encouragement.

## **Bibliography**

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