Digital System Design
(Credits: Theory-04, Practicals-02)

Total Lectures 60

Unit-1 (15 lectures)

Number System and Codes: Decimal, Binary, Hexadecimal, Octal, BCD, Conversions, Complements (1's and 2's), Signed and unsigned numbers, addition and subtraction, multiplication and subtraction, Gray Codes

Boolean algebra and Logic gates: Boolean algebra- Positive and negative logic. Boolean laws. De Morgan's theorems, simplification of Boolean expressions-SOP and POS. Logic gates- basic logic gates-AND, OR, NOT, logic symbol and truth table. Derived logic gates (NAND, NOR, XOR & XNOR). Universal property of NOR and NAND gates. K-map-3 and 4 variable expressions. Characteristics of logic families: Fan In and Fan out, power dissipation and noise Immunity, propagation delay, comparison of TTL and CMOS families.

Unit-2 (11 lectures)

Combinational logic analysis and design: Multiplexers and Demultiplexers, Adder (half and full) and their use as subtractor, Encoder and Decoder, Code Converter (Binary to BCD and vice versa)

Unit-3 (16 lectures)

Sequential logic design: Latch, Flip flop, S-R FF , J-K FF, T and D type FFs, clocked FFs, registers, Counters (ripple, synchronous and asynchronous, ring, modulus)

Unit-4 (18 Lectures)

VHDL: A Brief History of HDL, Structure of HDL Module, Comparison of VHDL and Verilog, Introduction to Simulation and Synthesis Tools, Test Benches.

VHDL: Module, Delays, brief description - data flow style, behavioral style, structural style, mixed design style, simulating design.

Language Elements, Introduction, Keywords, Identifiers, White Space Characters, Comments, format, Integers, reals and strings. Logic Values, Data Types-net types, undeclared nets, scalars and vector nets, Register type, Parameters. Operands, Operators, types of Expressions

Gate level modeling, built in Primitive Gates, multiple input gates, Tri-state gates, pull gates, MOS switches, bidirectional switches, gate delay, array instances, implicit nets, Illustrative Examples (both combinational and sequential logic circuits).

Digital System Design Lab (Hardware and Circuit Simulation Software)
60 lectures

1. To verify and design AND, OR, NOT and XOR gates using NAND gates.
2. To convert a Boolean expression into logic gate circuit and assemble it using logic gate IC's.
3. Design a Half and Full Adder.
4. Design a Half and Full Subtractor.
5. Design a seven segment display driver.
6. Design a 4 X 1 Multiplexer using gates.
7. To build a Flip- Flop Circuits using elementary gates. (RS, Clocked RS, D-type).
8. Design a counter using D/T/JK Flip-Flop.
9. Design a shift register and study Serial and parallel shifting of data.

VHDL

1. Write code to realize basic and derived logic gates.
2. Half adder, Full Adder using basic and derived gates.
3. Half subtractor and Full Subtractor using basic and derived gates.
4. Clocked D FF, T FF and JK FF (with Reset inputs).
5. Multiplexer (4x1, 8x1) and Demultiplexer using logic gates.
6. Decoder (2x4, 3x8), Encoders and Priority Encoders.
7. Design and simulation of a 4 bit Adder.
8. Code converters (Binary to Gray and vice versa).
9. 2 bit Magnitude comparator.
10. 3 bit Ripple counter.