TECHNISCHE UNIVERSITÄT DRESDEN

Prof. Dr.-Ing. Thomas Mikolajick, Prof. Dr. rer. nat. Stefan Mannsfeld

Microtechnologies
Chapter 1 - Introduction

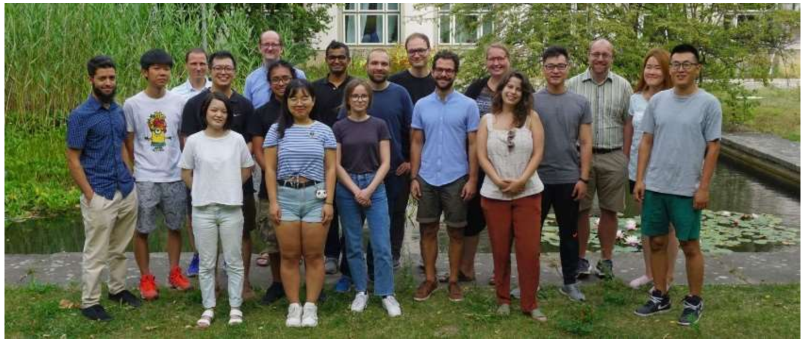
Dresden, 15.10.2024

Administrative Details

Chair of Organic Devices

Prof. Dr. rer. nat. Stefan Mannsfeld
Technische Universität Dresden,
Center for Advancing Electronics Dresden (cfaed),
Department of Electrical Enginering and Information Technology
BAR Barkhausen-Bau II.55
01069 Dresden

Tel: +49(0)351-463-43706
Fax: +49(0)351-463-39923
stefan.mannsfeld@tu-dresden.de



Administrative Details

Lecture Dates:

Tuesday	1:00pm - 2:30 pm	TOE/0317/H
Thursday	9:20am - 10:50am	SCH/A118/H

No lectures/tutorials on the following days: Thu., Nov. 21 2024, Thu. Nov. 28 2024, Thu. Dec. 19 2024

The slides will be uploaded to OPAL soon (typically in stride with the lecture). Note that throughout this semester, we will also have 4 tutorials. These will take place at the lecture time slots/locations.

The course will finish with a written exam – at the end of the summer semester – that combines both this and next semesters lectures and tutorials.

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1 Introduction

- Overview
- History of semiconductor technology
- Trends in semiconductor technology
- Typical process sequence

2 Wafer Fabrication

- Basics
- Crystal growing
- From crystal to wafer

3 Lithography

- Basics
- Optical lithography processes
- Non-optical lithographic processes

4 Layer fabrication

- Thermal layer generation
- Physical layer deposition
- Chemical film deposition
- Electrochemical layer deposition
- Other layer generation processes

5 Cleaning and Structuring

- Cleaning
- Wet chemical etching process
- Dry chemical etching process

6 Planarization

- Chemical-mechanical polishing

7 Doping

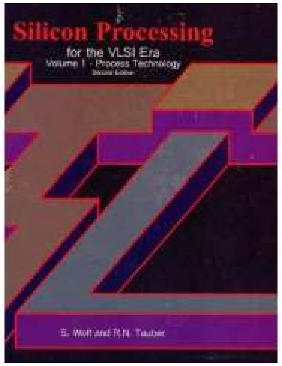
- Diffusion
- Ion implantation

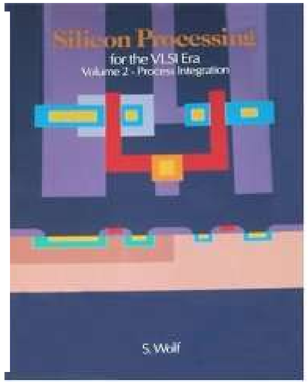
8 Complete CMOS process

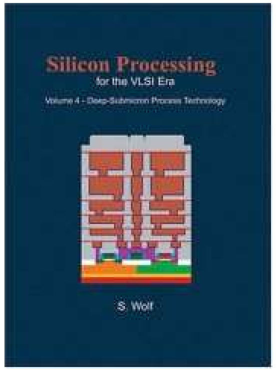
9 Process Control

- Optical measuring methods
- Electrical measurement methods
- Yield analysis

10 Outlook







Silicon Processing for the VLSI Era:

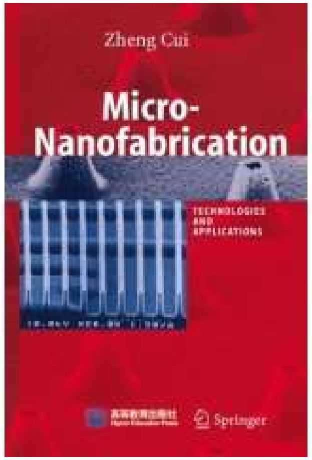
Volume 1 – Process Technology

Volume 2 – Process Integration

Volume 4 – Deep-Submicron Process Technology

S. Wolf

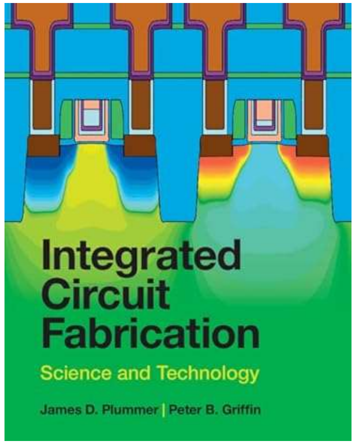
Lattice Press



Micro-Nanofabrication. Technologies and Applications

Zheng Cui

Springer, Berlin (2005)



Integrated Circuit Fabrication : Science and Technology

Plummer & Griffin

Cambridge University Press (2024)

Free download https://plummergriffinbook.stanford.edu/book

Content

1.2 History of semiconductor technology - from silicon to IC -

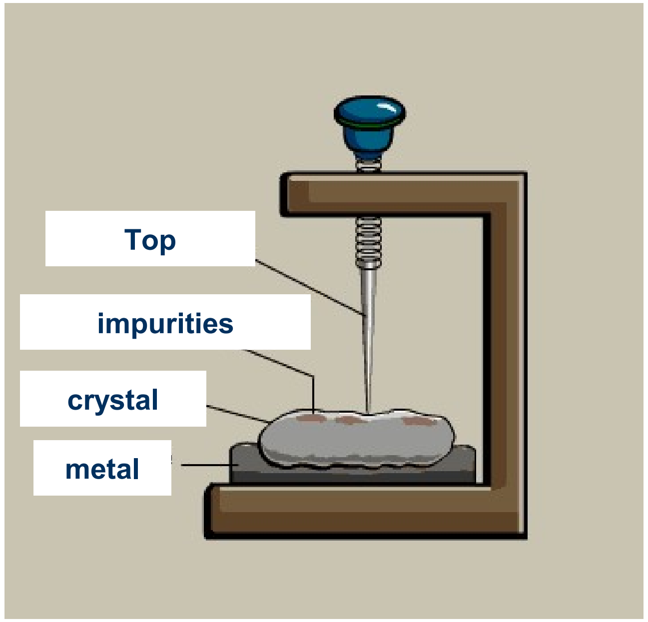
1823	Discovery of silicon
1874	Discovery of the rectifier effect ▶
1886	Discovery of germanium
1925	*Formation of Bell Labs*
1928	selenium rectifier
1938	silicon crystal diode
1941	germanium diode ▶
1947	First transistor (Germanium) ▶
1952	First monocrystalline germanium ▶
1954	First monocrystalline silicon ➔ silicon transistor ▶
1954	Piezoresistive effect in silicon and germanium
1955	*Foundation of Shockley Semiconductor Laboratories (start of Silicon Valley)*
1957	*Fairchild Semiconductors founded*
1958/59	Integrated circuit ▶

1959	Feynman's lecture: " There's plenty of Room at the Bottom " ▶
1959	MOS transistor
1963	Complementary MOS Technology (CMOS) ▶
1965	Moore's law ▶
1967	Surface Micromechanics (FET Accelerometer) ▶
	Anisotropic silicon etch
1968	*Foundation of Integrated Electronics (INTEL)*
1971	Intel 4004 microprocessor; First DRAM memory 1103 ▶
1982	The term "micromechanics" is generated
1983	Surface micromechanics with polysilicon and SiO_2 - sacrificial layer technology
1985	LIGA (Lithography Galvanic "Abformung" (molding)) technique
1985	First 3-dimensional DRAM trench and stack capacitors in production ▶
1987	First manufacture of moving parts in silicon
	Introduction of the term "microsystems technology" (MEMS = Micro Electromechanical systems)
1995	First silicon germanium hetero-bipolar transistors in production ▶
1997	First Cu-interconnect technology in production ▶

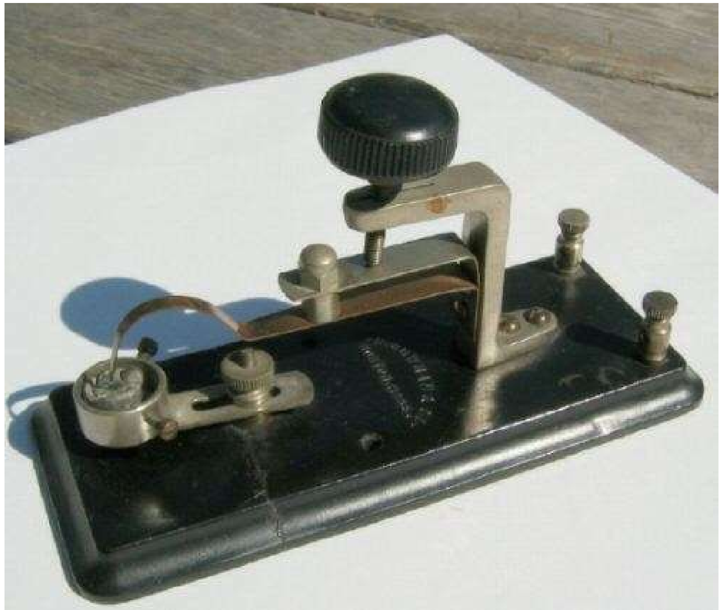
2003/4	Beginning of the age of nanoelectronics (90nm technology)
2011	First 22nm technology with FinFET transistors ▶
2013	First 3D integrated NAND flash memory in production ▶
2015	First 3D memory with conventional stacking technology (3D x-point) ▶

The **rectifier** effect is the property of an electronic component (diode) to only conduct the current in one direction (valve). This is fundamental to all electronic circuits. The effect was discovered by **Ferdinand Braun in 1874** in sulfur-metal compounds, but was not understood at the time. Later other materials were used. Contact points had to be "tried out" until a stable operating point was found.

Schematic of a crystal detector



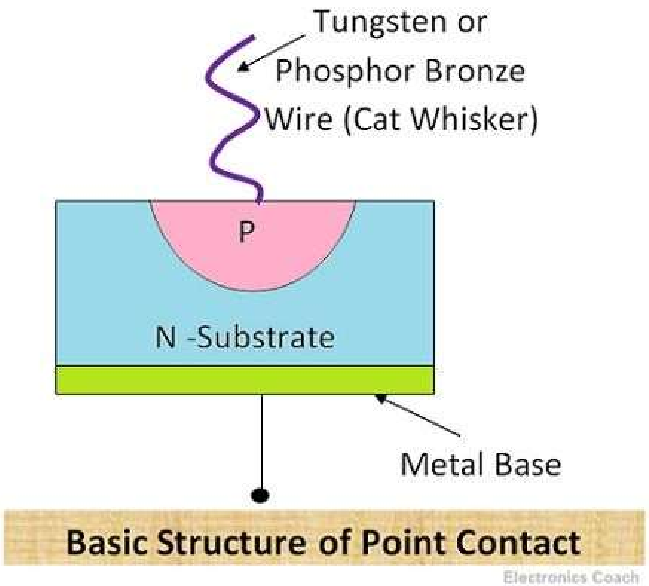
crystal detector



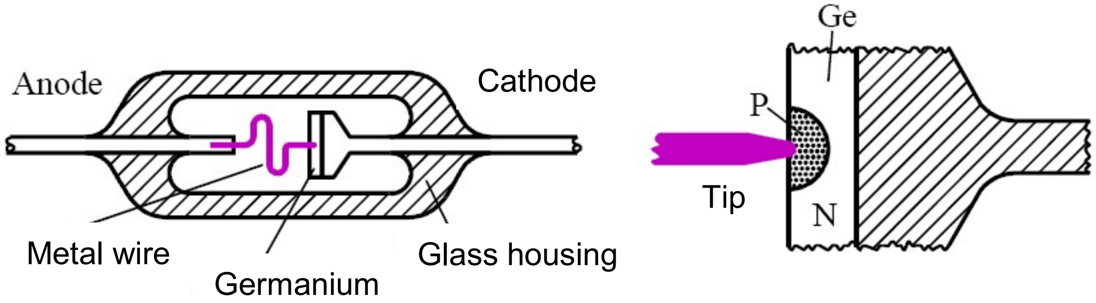
Ferdinand Brown

The Ge point contact diode was the first reproducible semiconductor component.

Principle of the point-contact diode



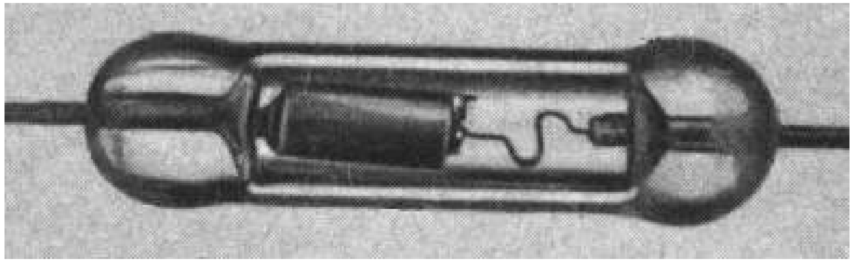
Structure of a germanium point-contact diode



Top diode on average

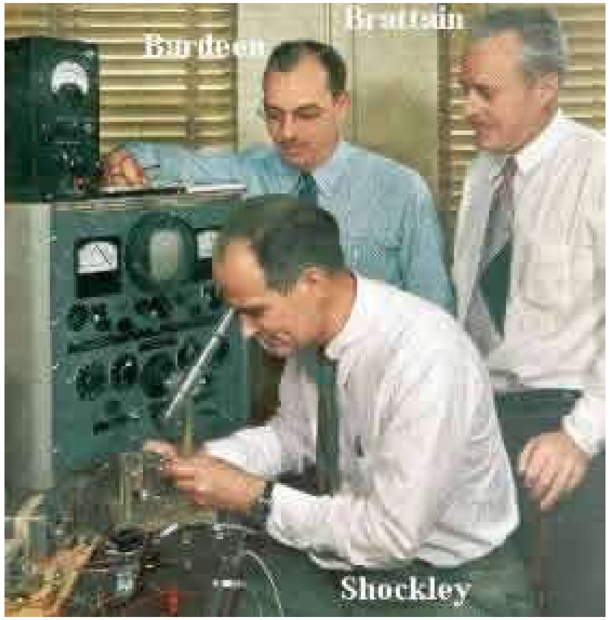
crystal cutout

Real germanium point contact diode

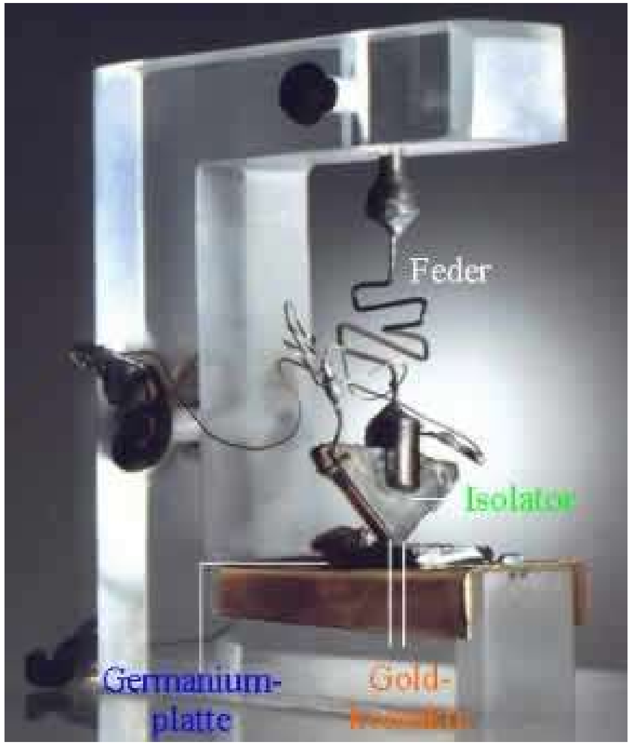


The first transistor was developed by Shockley, Bardeen and Brattain at Bell Labs in 1947. Already in the 1920s there were patents for (field effect!) transistors.

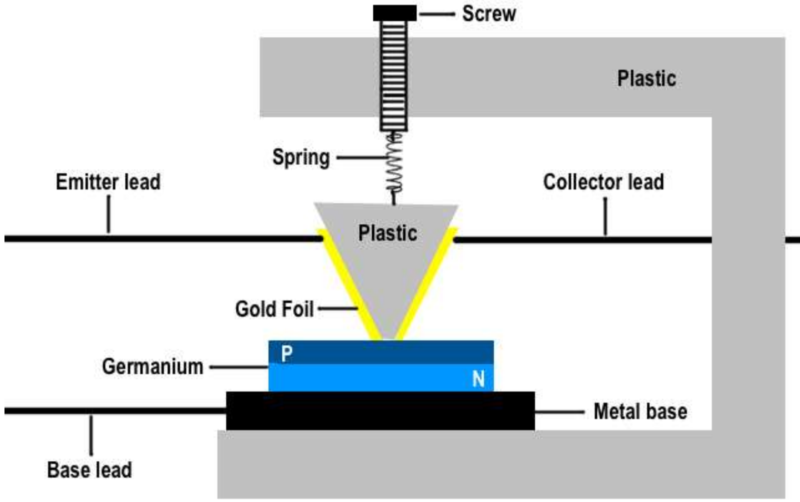
The developers of first transistor



replica of first transistor

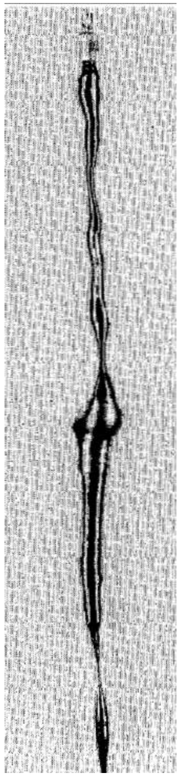


construction of first transistor

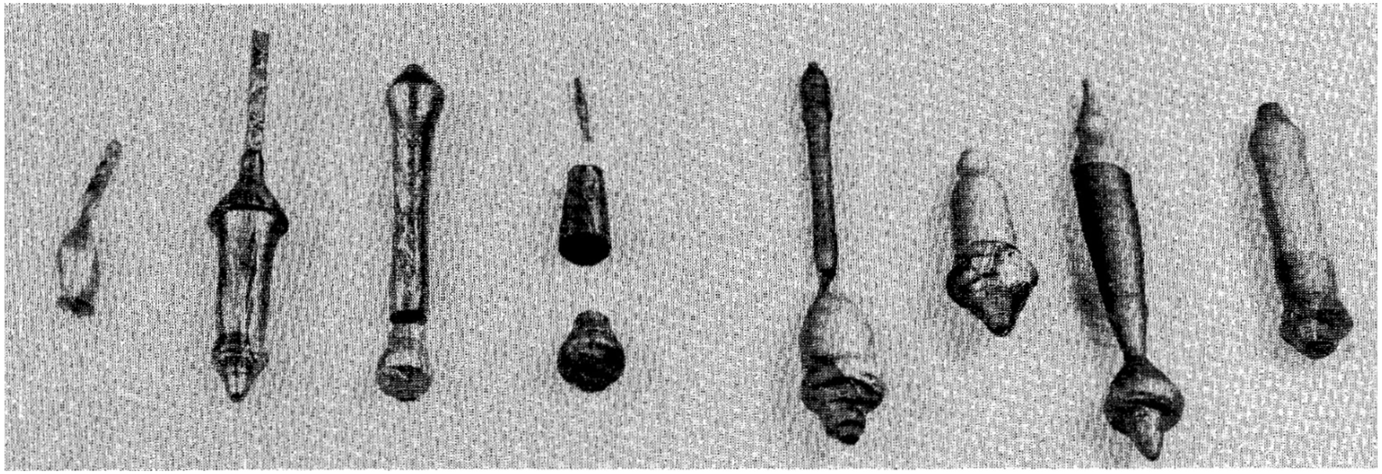


At the end of the 1940s, the importance of **high-purity single crystals** for semiconductor devices became apparent. **Gordon Teal** developed, first at Bell Labs and later at Texas Instruments, the **technique of growing single crystals** and doping from the melt. The production of (doped) germanium single crystals led to the development of the bipolar pn transistor

Formerly germanium single crystal

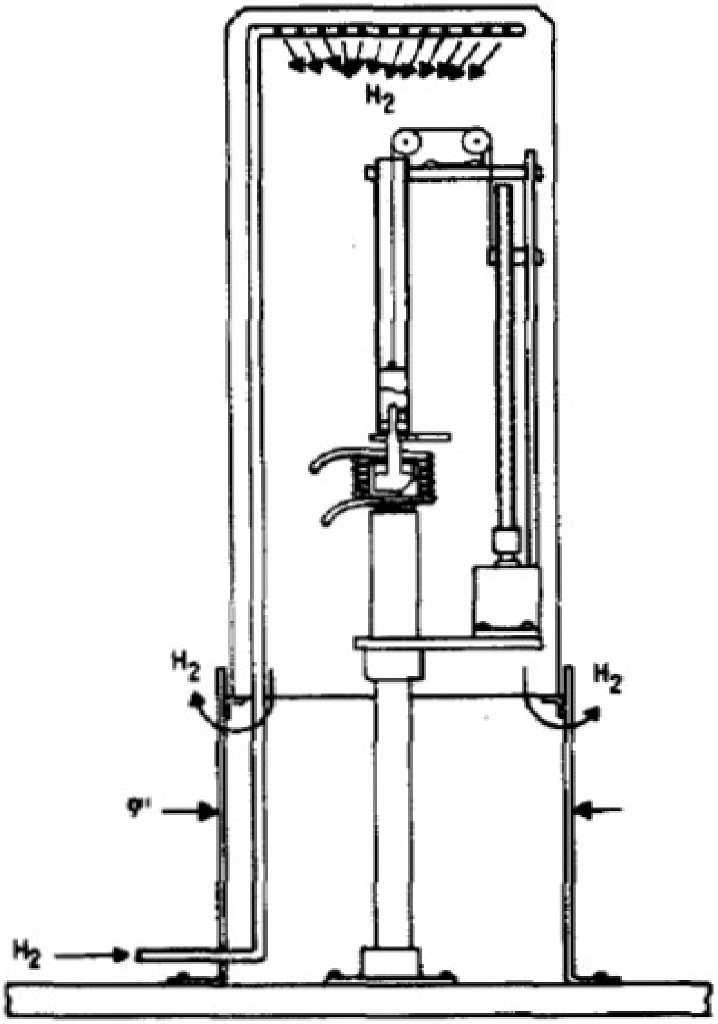


Former silicon single crystals



G.Teal

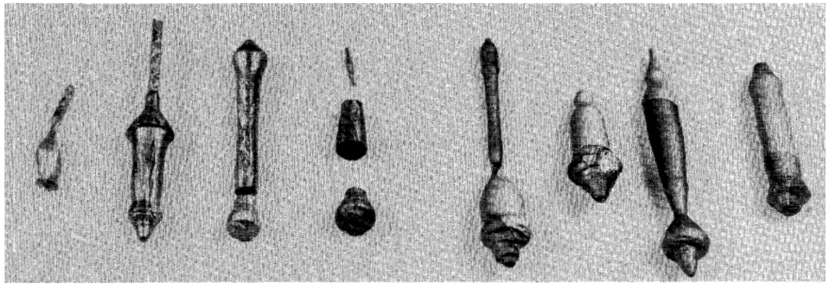
First facility for growing single crystals by Teal and Little



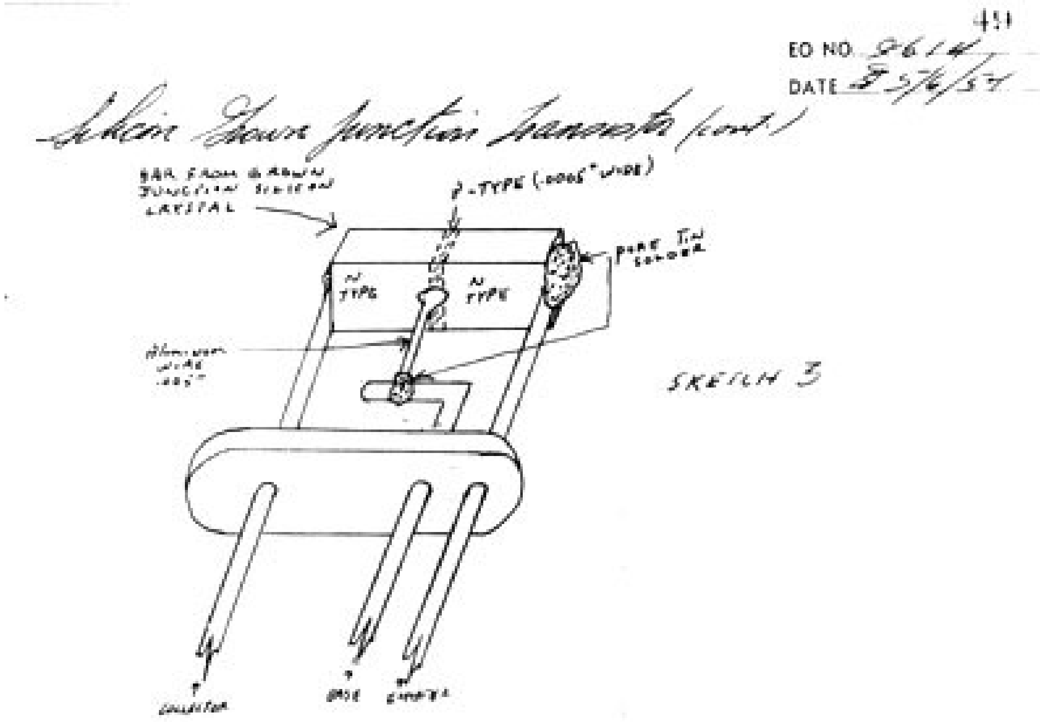
First bipolar pn transistor

Gordon Teal joined Texas Instruments in 1952. There he also began to pull silicon monocrystals . In 1954 Texas Instruments introduced the first silicon transistor and the first transistor radio . The silicon transistor was a sensation at the time, since germanium was technologically much easier to master.

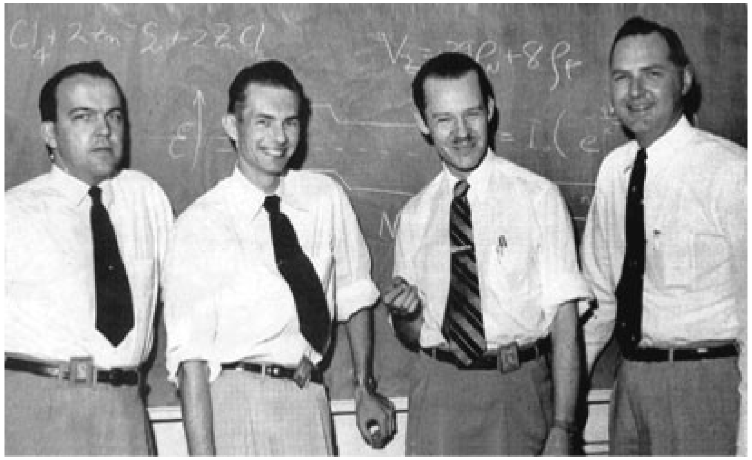
Former silicon single crystals



Sketch of the first silicon transistor

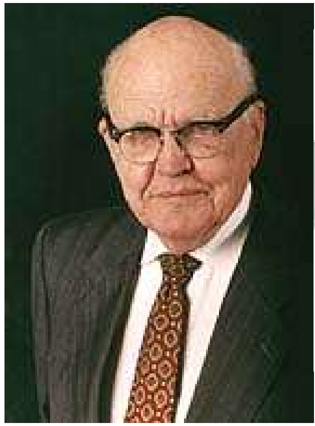


Willis AdcockMort Jones
Ed Jackson and Jay Thornhill



At almost the same time, J. Kilby (TI) and B. Noyce (Fairchild) developed the integrated circuit . J. Hörni (Fairchild) developed planar technology in the same period .

J Kilby

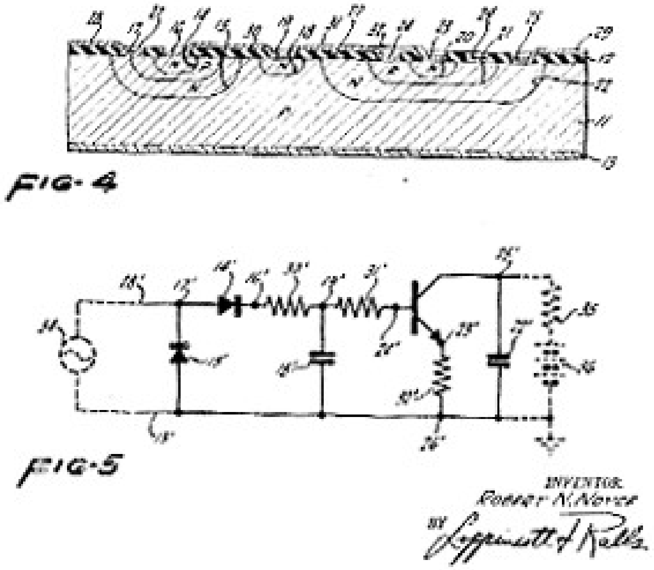


B. Noyce

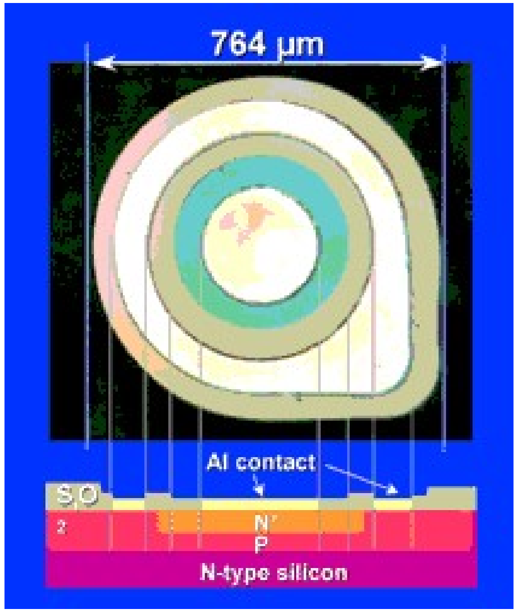
J. Horni

Kilby's first IC

Noyce's first IC



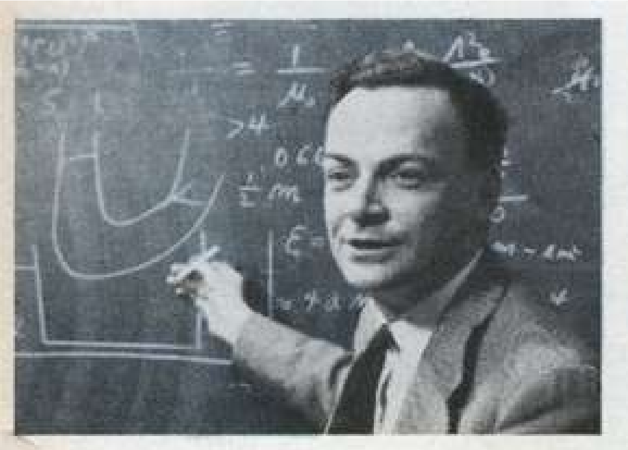
First planar transistor

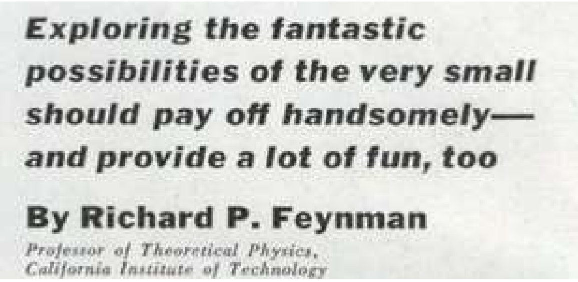


for entry into a new field of physics, the field of **microstructures**, with the sentence **"There's Plenty of Room at the Bottom"**.

micro and nanotechnology are **worth it (economically)** and **lots of fun !**

Richard Feynman





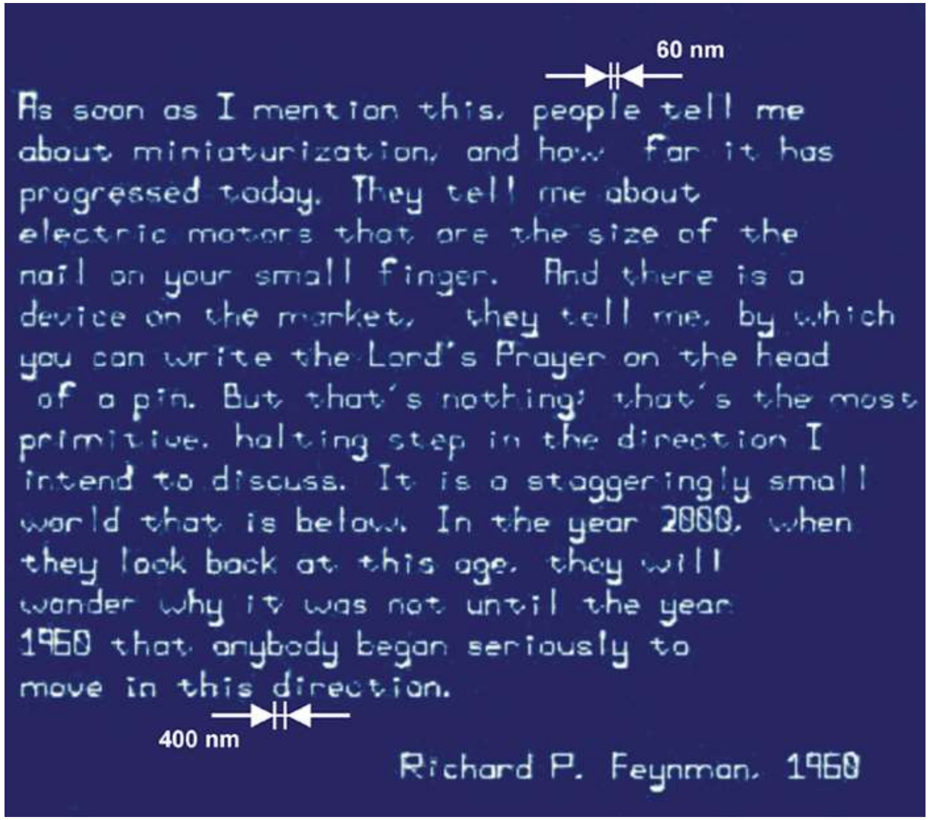
Exploring the fantastic possibilities of the very small should pay off handsomely— and provide a lot of fun, too

By Richard P. Feynman

Professor of Theoretical Physics, California Institute of Technology

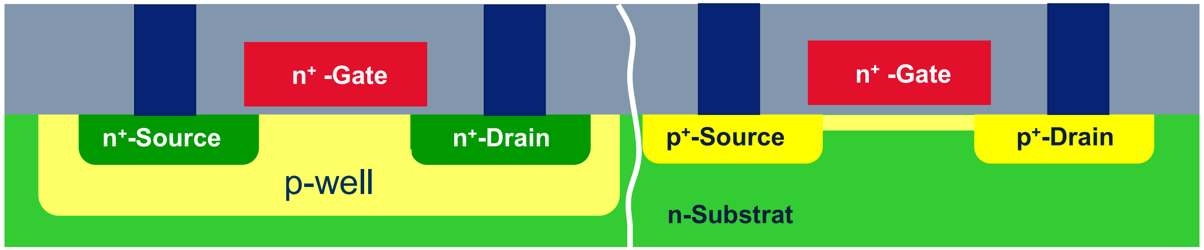
http://www.zyvex.com/nanotech/feynman.html

From Feynman's lecture



By combining n-channel and p-channel components (complementary metal-oxide-silicon = CMOS) the power loss of digital circuits can be drastically reduced . The complementary principle was proposed by Frank Wanlass (then Fairchild) in 1963 .

CMOS Technology



F. Wanlass

In 1965 Gordon Moore (then Fairchild, later one of the three INTEL founders) published a paper in which he predicted that the number of transistors on an integrated circuit would double every 12 months . Back then, integrated circuits had fewer than 100 transistors.

Title and summary of Gordon Moore's original publication in Electronics, Vol. 8, dated April 19, 1965

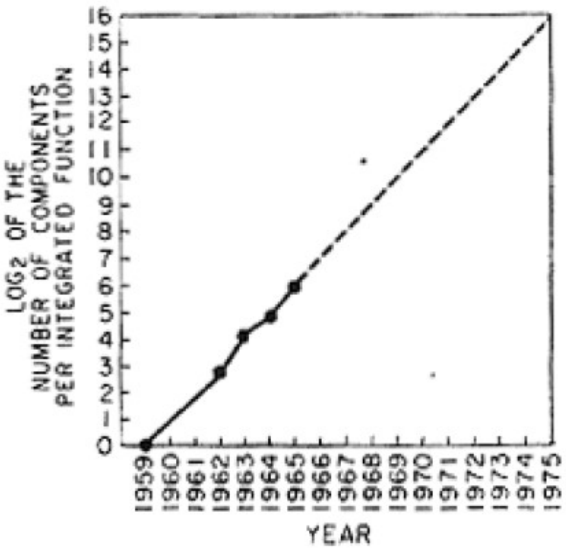
Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

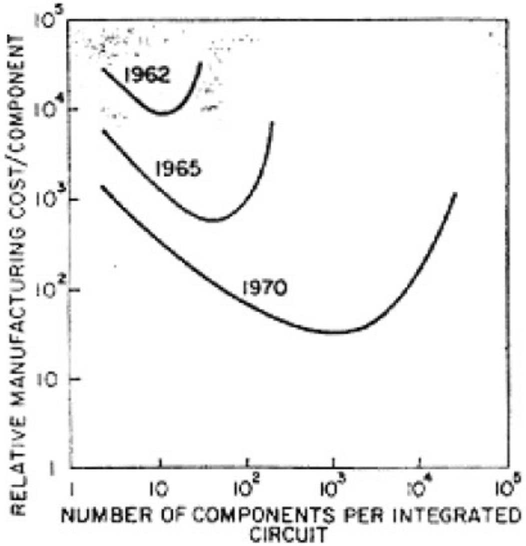
By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

Moore's extrapolation



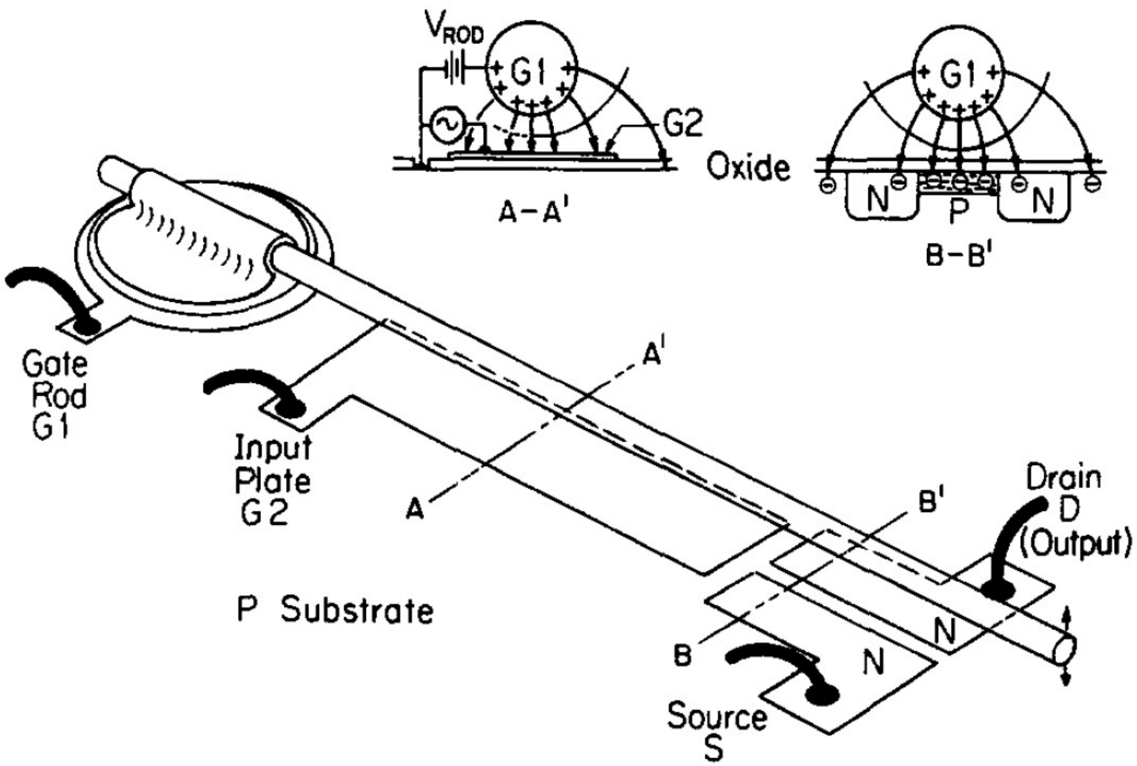
Moore's cost forecast



G Moore

In **1967** , **Nathanson and Wickstrom** at **Westinghouse** developed a field effect transistor with a **vibrating beam as the gate electrode** . This device is considered to be the **beginning of surface** micromechanics. In **1983 Howe and Muller** were the first to fabricate this device using a **sacrificial polysilicon layer technique** .

Transistor with swinging bar as gate



First resonance bar in sacrificial layer technology

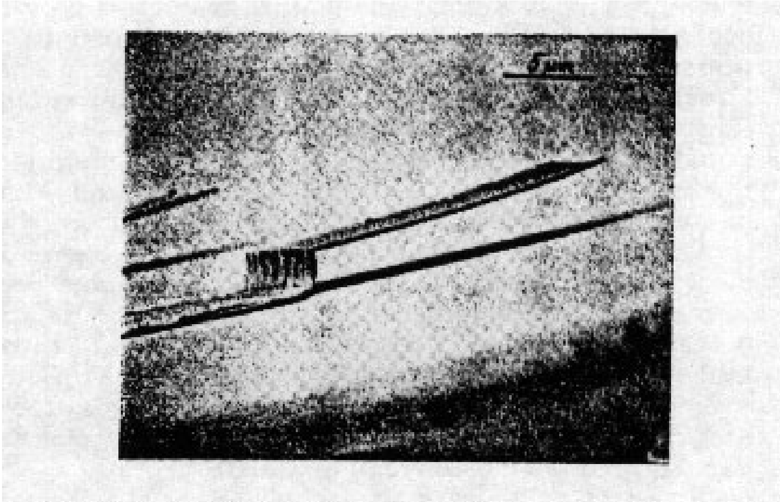


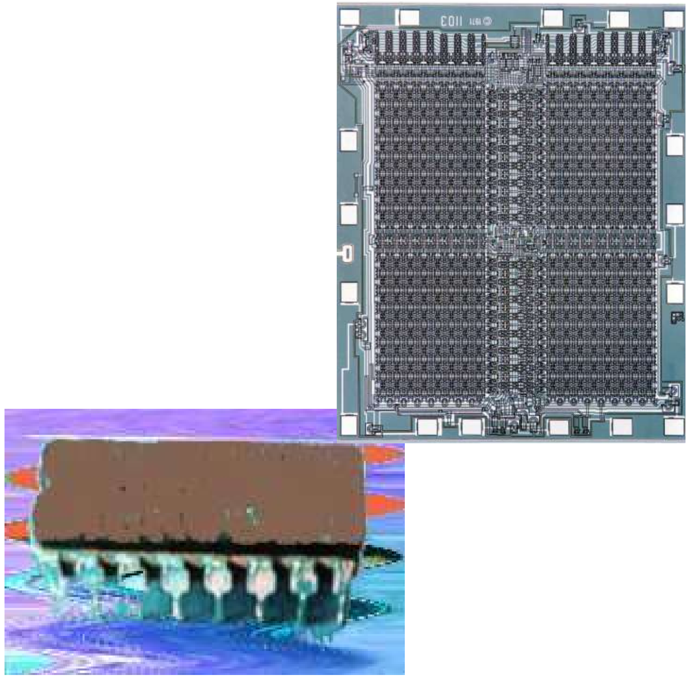
Fig. 6. Thin poly-Si cantilever: 25 μm long, 230 nm thick, with a 3.5 μm beam-substrate separation.

1.2 History of Semiconductor Technology

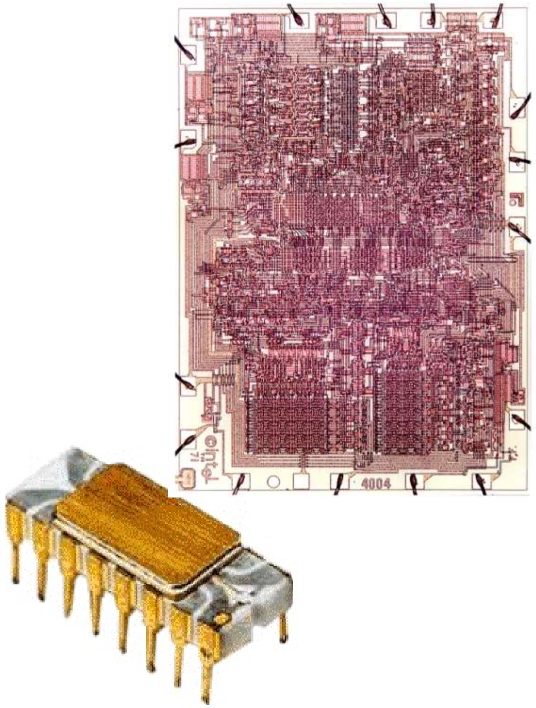
- First DRAM and first microprocessor (1971) -

In **1971**, INTEL launched the first **dynamic** memory chip (dynamic random access memory = **DRAM INTEL 1103**). In the same year, INTEL also released the **4004 microprocessor** developed by **Ted Hoff.**

First DRAM 1103



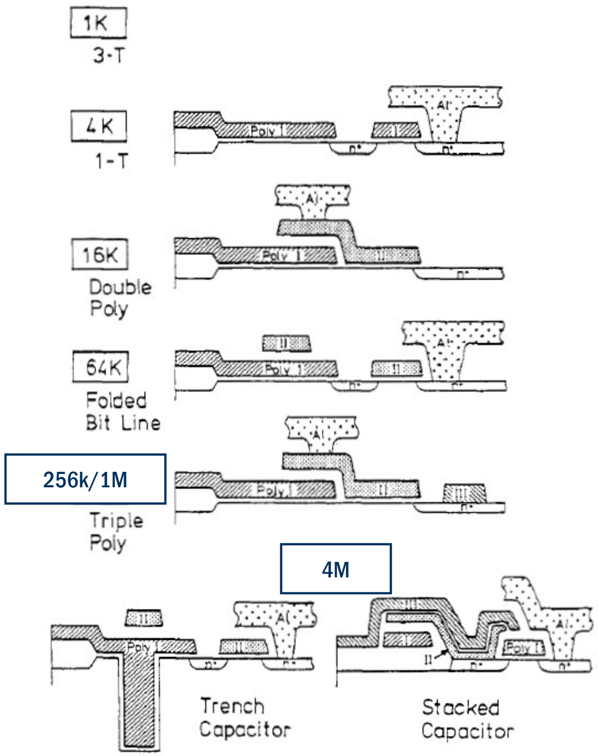
Microprocessor 4004



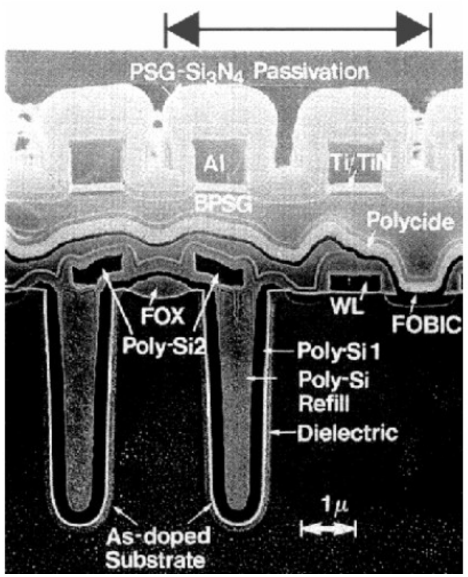
Ted Hoff

In the mid-1980s, the line width in the field of DRAMs was reached at which a minimally sized planar ONO capacitor could no longer store enough charge to be reliably used as a memory. Integrated circuits had to go into the third dimension.

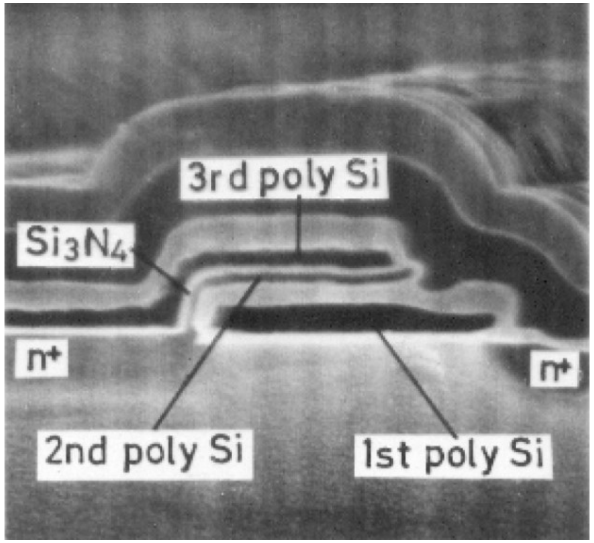
DRAM memory cells 1971 – 1985



trench capacitor

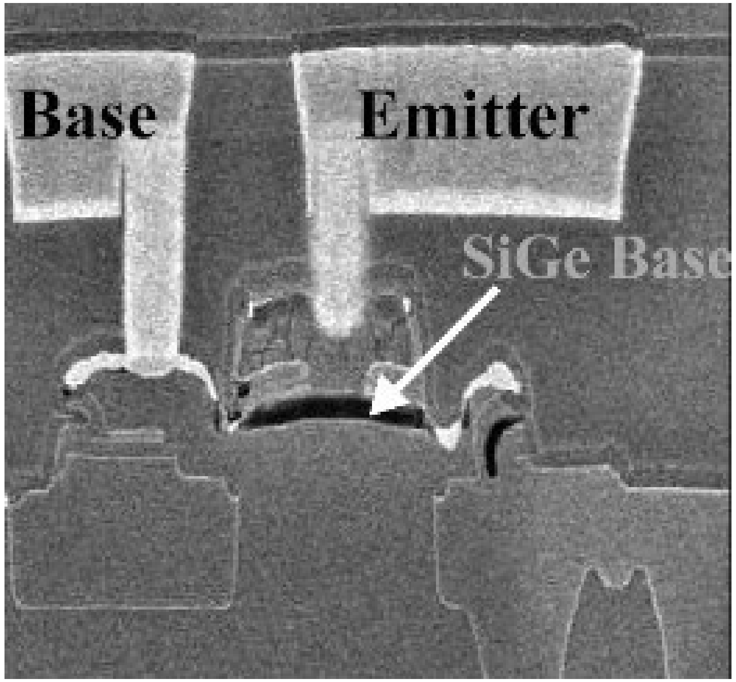


stacked capacitor

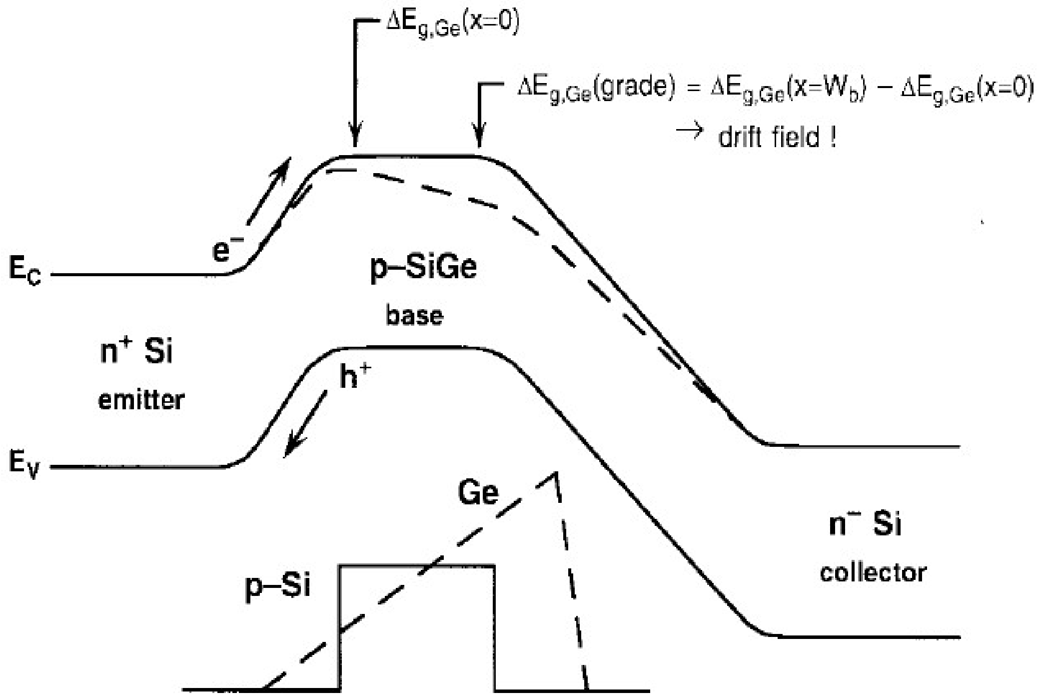


In 1995 IBM brought out a **BiCMOS** (**Bipolar CMOS**) technology with bipolar transistors with a **SiGe base** on the market. The SiGe base makes the transistor faster, which is why this technology is used for high-frequency applications (e.g. mobile phones).

SiGe hetero bipolar transistor



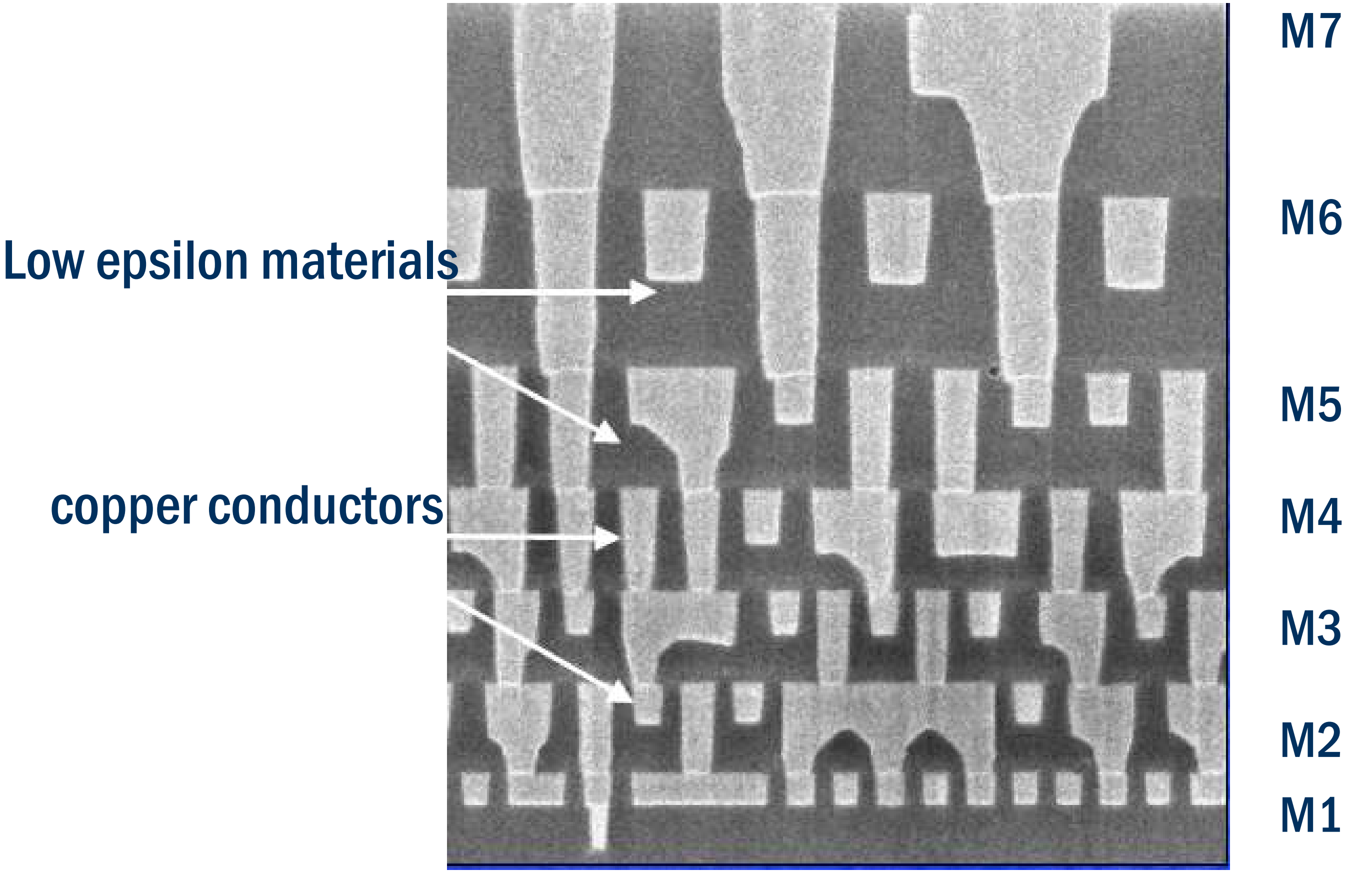
SiGe base in the ribbon model



1.2 History of Semiconductor Technology - Cu Technology (1999) -

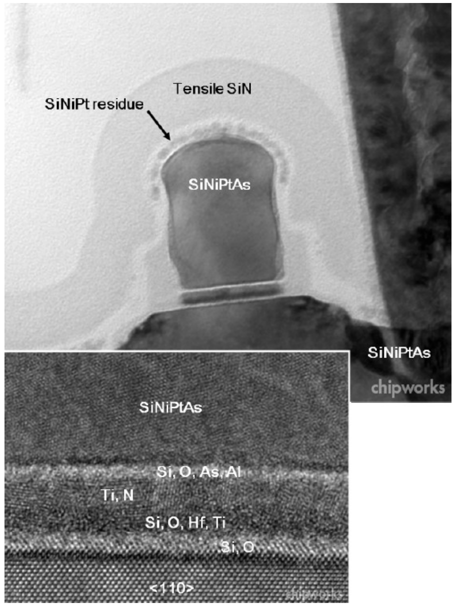
In **1995**, IBM introduced the **copper technology** . This was one of the greatest material innovations in the history of semiconductor technology to date. Cu forms deep traps in silicon and was therefore avoided until then. This innovation opened the way for further developments.

Metallization of an INTEL 130nm process

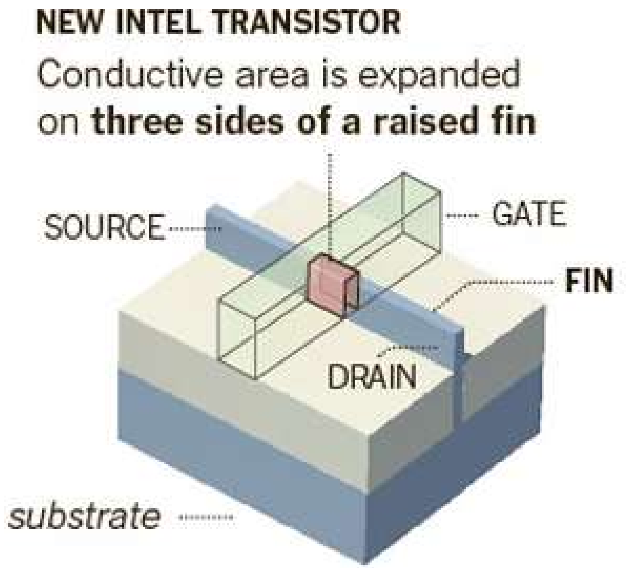


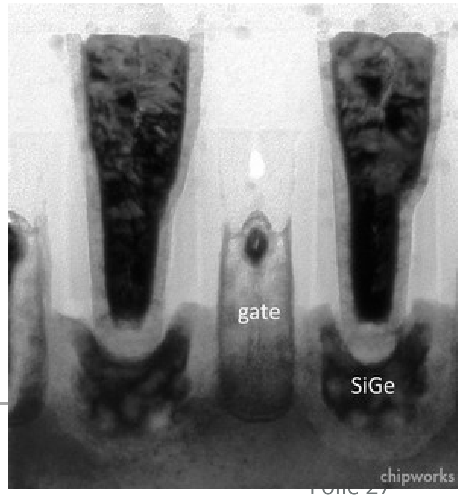
1.2 History of Semiconductor Technology - FinFET (2011) -

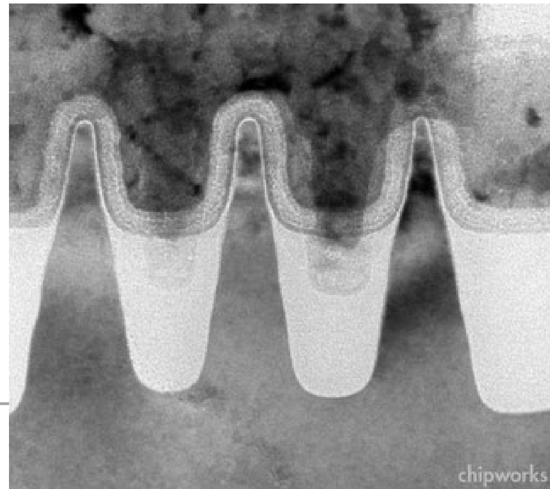
32nm NMOS with HfO2 (Global Foundries)



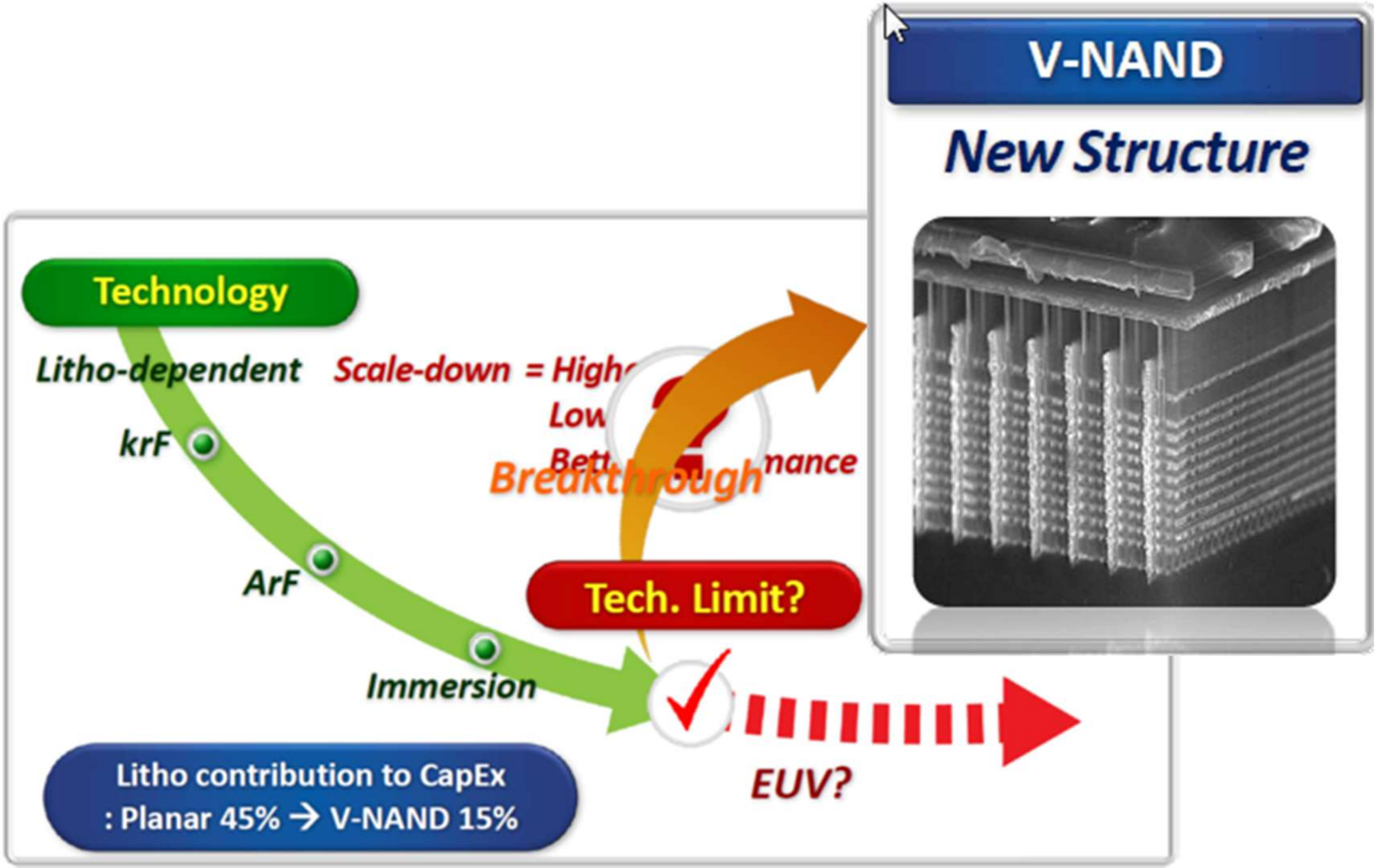
FINFET



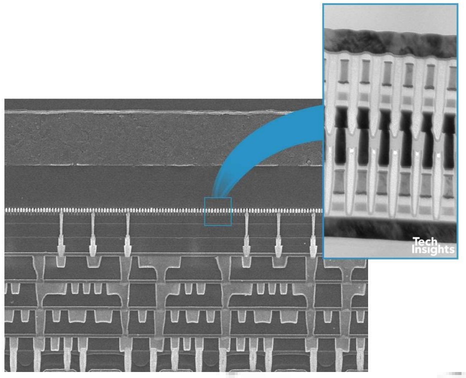


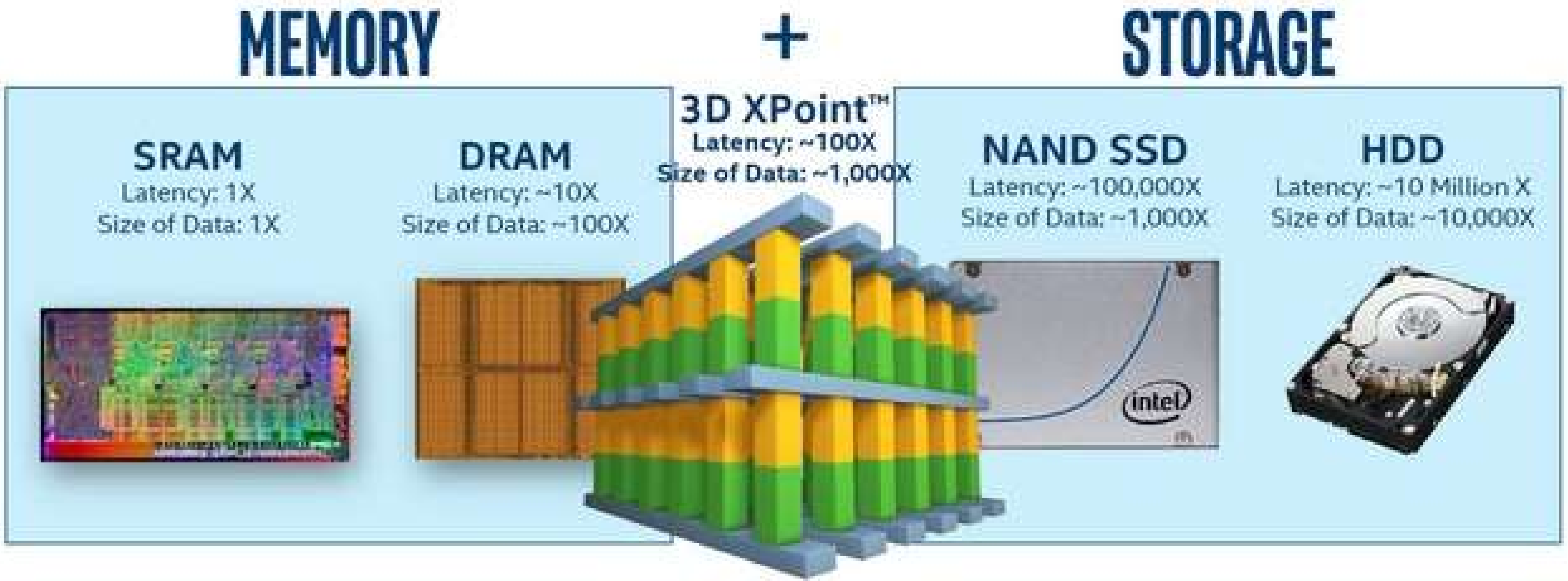


3D-NAND


V-NAND
New Structure
Technology
Litho-dependent
Scale-down = High
Low
Bett
mance
Breakthrough
krF
ArF
Immersion
Tech. Limit?
EUV?
Litho contribution to CapEx
: Planar 45% → V-NAND 15%

3D - XPoint

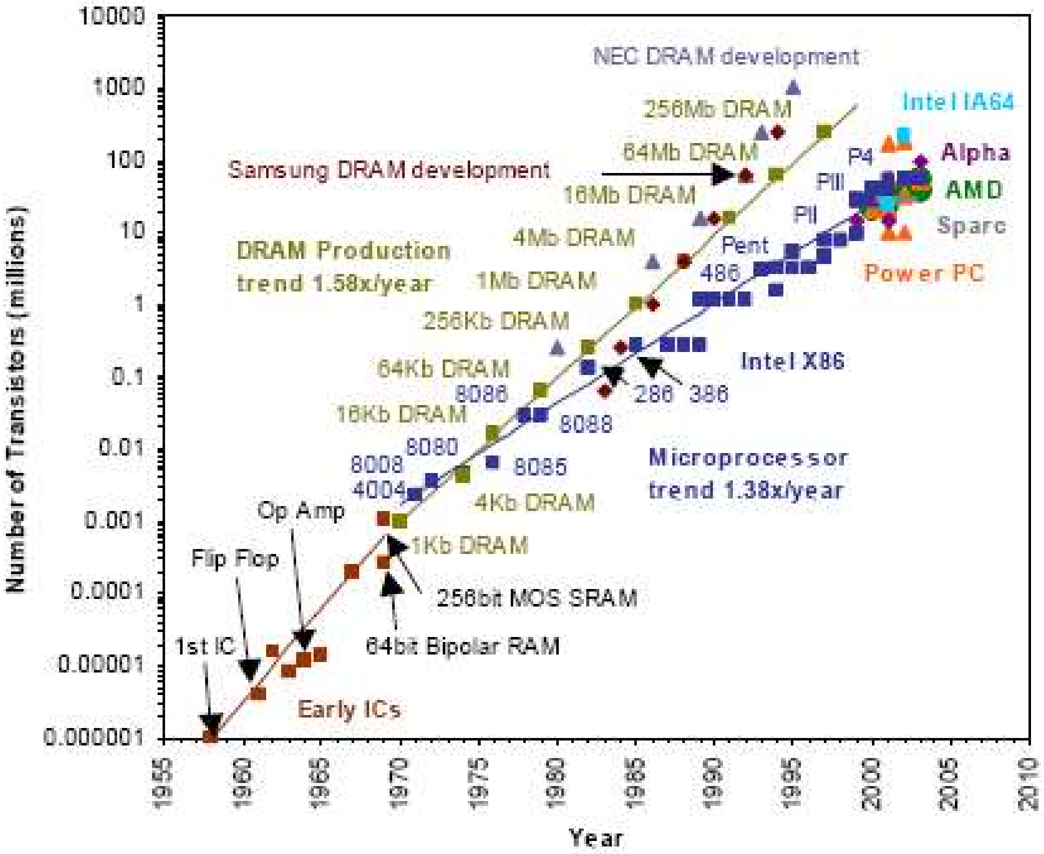

Tech Insights


MEMORY
+
STORAGE
SRAM
Latency: 1X
Size of Data: 1X
DRAM
Latency: ~10X
Size of Data: ~100X
3D XPoint™
Latency: ~100X
Size of Data: ~1,000X
NAND SSD
Latency: ~100,000X
Size of Data: ~1,000X
HDD
Latency: ~10 Million X
Size of Data: ~10,000X
intel

contents

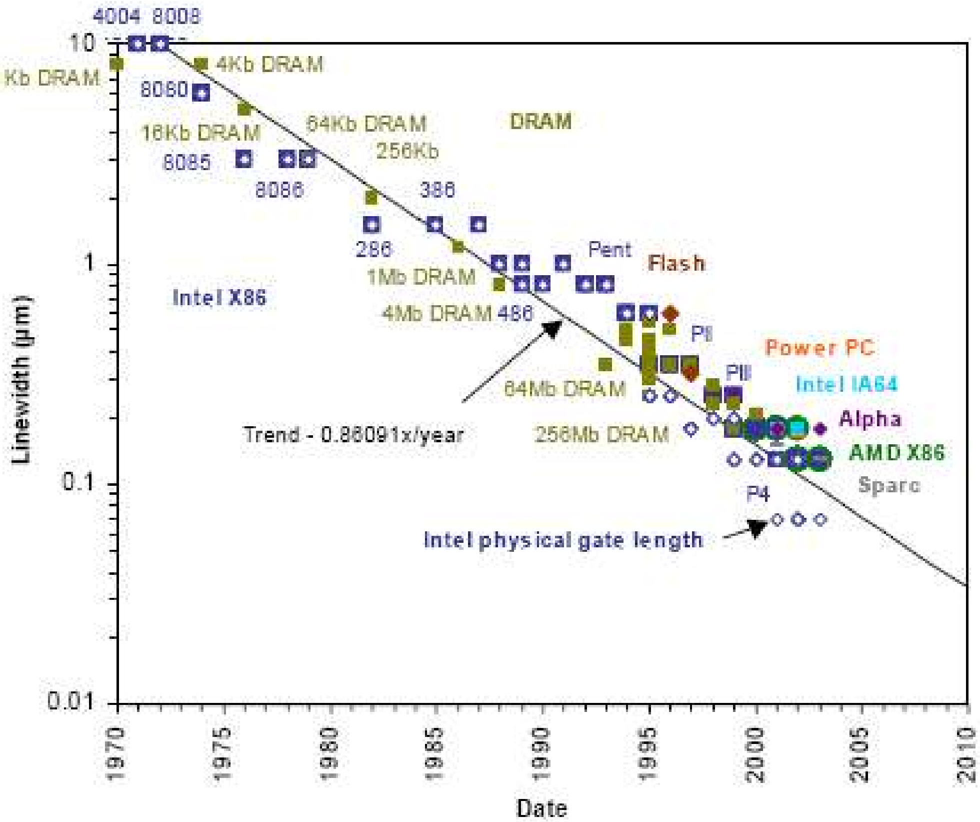
The trend of an exponential increase in the number of transistors per chip predicted by Gordon Moore in 1965 has now lasted for 40 years . However, the number of transistors will “only” double every 18 months and not every 12 months, as predicted by Gordon Moore.

Exponential increase in the number of transistors per chip



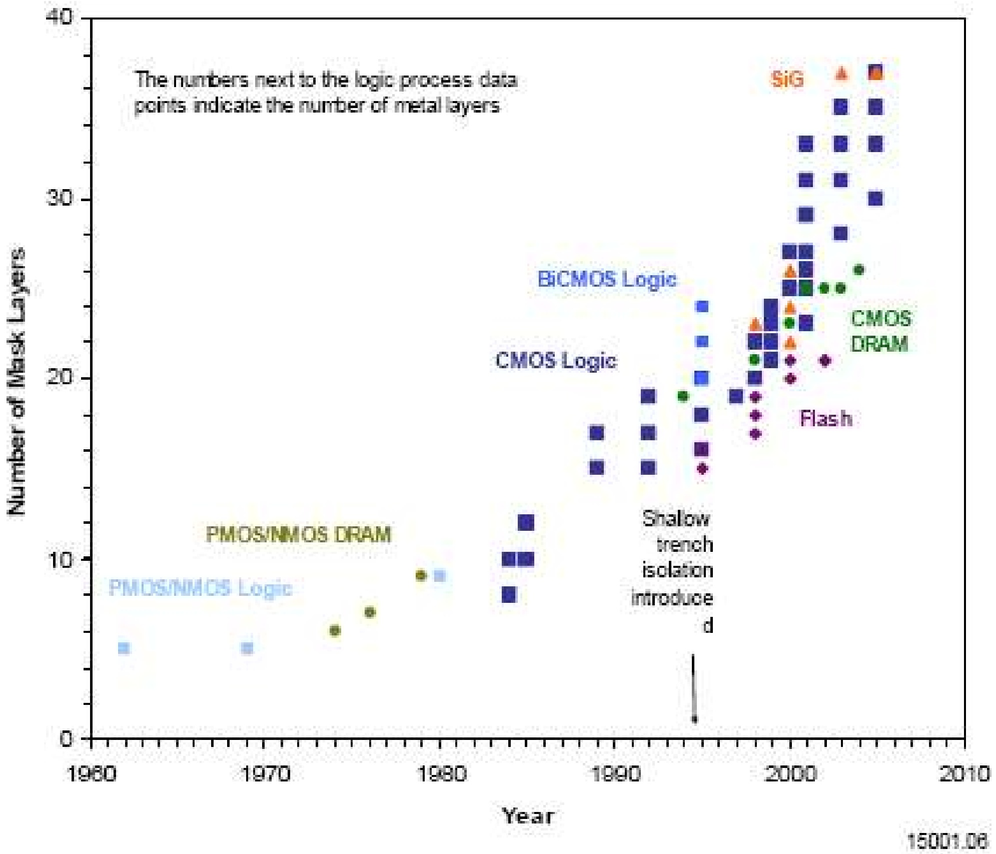
The increase in chip complexity is primarily achieved by **reducing the minimum line width**. For line widths below 100nm, one no longer speaks of microelectronics, but of nanoelectronics. This limit was reached around 2003/4 .

Reduction of the minimum line width in integrated circuits



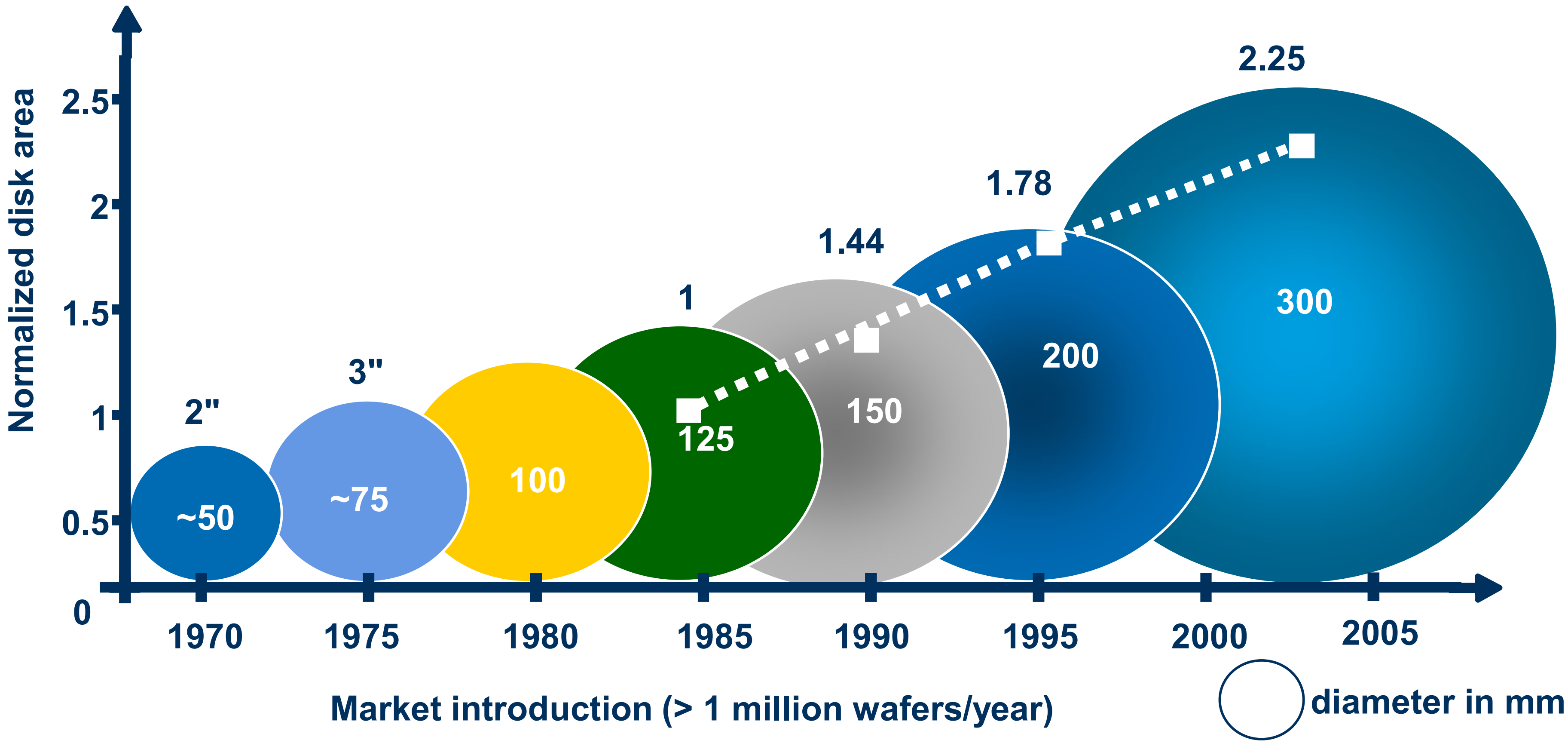
The reduction in line width goes hand in hand with increased complexity of the processes. The number of mask levels/layers per process can be understood as a simple measure of the complexity.

Increasing the complexity in integrated circuits



In order to increase the number of chips per disc and thus reduce costs, the disc diameter of the substrates is being continuously increased .

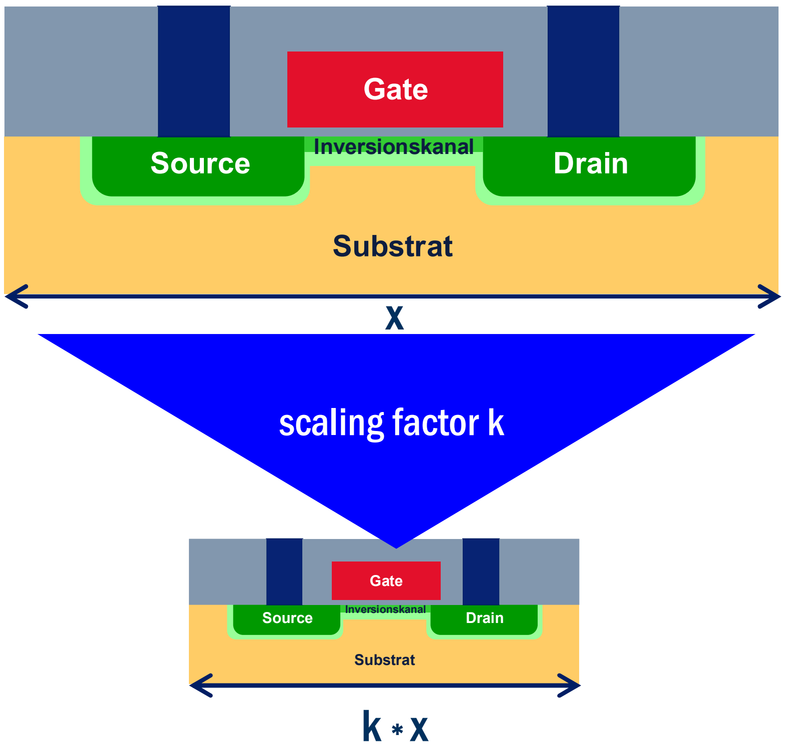
Increasing the silicon substrate diameter



The structure reduction brings about a **reduction in area and an increase in speed.**

Structure reduction can be performed either at **constant voltage or constant field.**

Scaling of a MOS transistor



Up to approx. 0.7 µm was scaled at a constant voltage of 5V.

Below 0.7 microns, the voltage was successively from

5V → 3.3V → 2.5V → 1.8V → 1.5V → 1.2V → ....
reduced

Table 1.1. Scaling of MOS transistors

parameter	constant field	constant voltage	
supply voltage	k	1	scaled parameters
length	k	k	
width	k	k	
gate oxide thickness	k	k	
depth of the pn junction	k	k	
substrate doping	1/k	1/k	
elec. field over the gate oxide	1	1/k	Components Consequences
width of the space charge zone	k	k	
gate area	k^2	k^2	
gate capacity	k	k	
drain current	k	1/k	
transconductance	1	1/k	
gate delay	k	k^2	circuit consequences
current density	1/k	$1/k^3$	
power loss (static and dynamic)	k^2	1/k	
power density	1	$1/k^3$	
power Delay Time Product	k^3	k	

Not all components show improved properties in the micro or nano world! For example, friction in the micro-world increases or magnetic fields become less efficient. In the case of microsystems, the benefit must therefore be assessed against the effort in each individual case and the suitable physical effect for the micro or nano world must be selected.

Scaling laws for important quantities

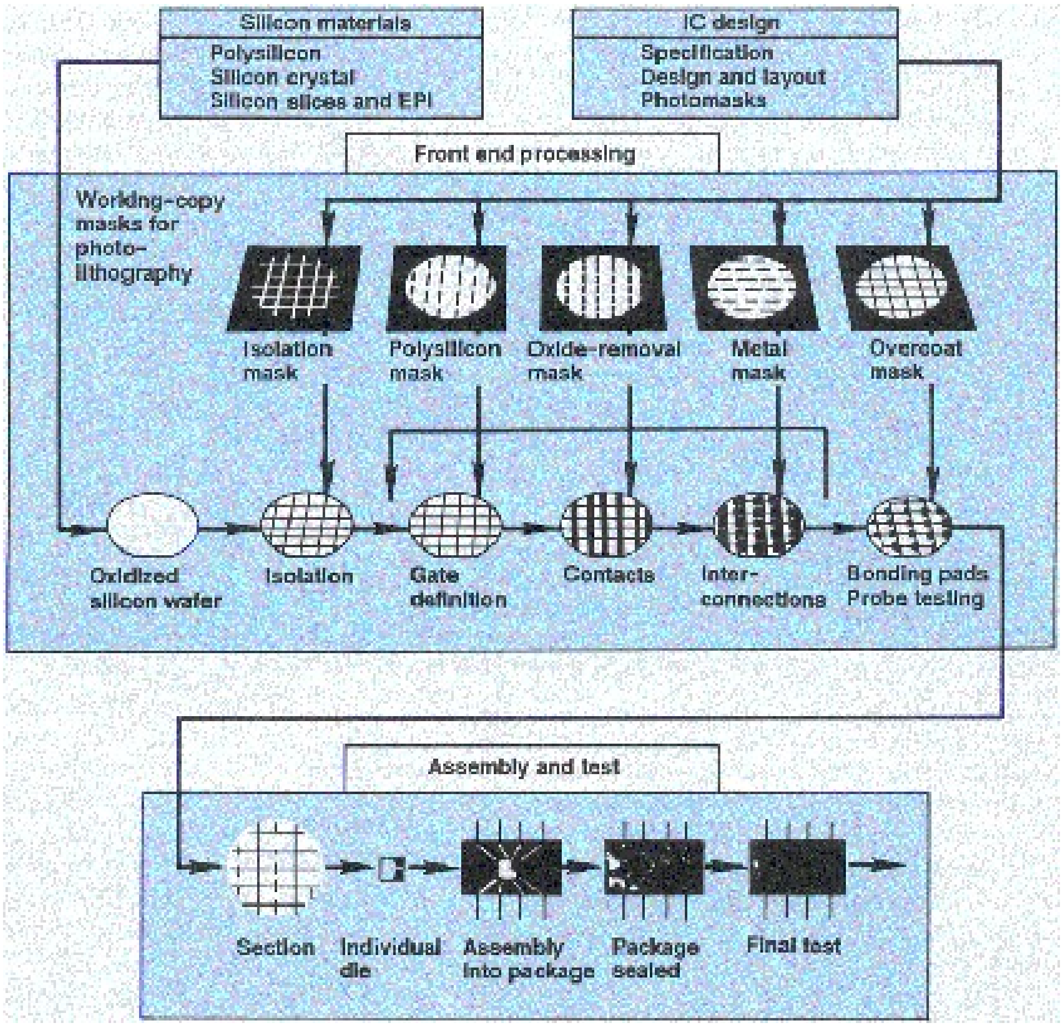
time	k^0
van der Waals force	$k^{1/4}$
diffusion	$k^{½}$
distance	k
speed	k
surface tension	k
electrostatic force	k^2
muscular strength	k^2
friction	k^2
thermal losses	k^2
piezoelectricity	k^2
dimensions	k^3
gravity	k^3
magnetic force	k^3
angular momentum	k^3
perfomance	k^3

A long chain of individual steps is necessary to produce an integrated circuit. First the **circuit to be manufactured must be designed on the computer** . The structure data generated in this way are then transferred to **masks** .

The masks are then converted into actual **components** on the wafer in the actual **wafer manufacturing process.** Manufacturing the circuitry on the wafer is commonly referred to as " **front-end** " **manufacturing** .

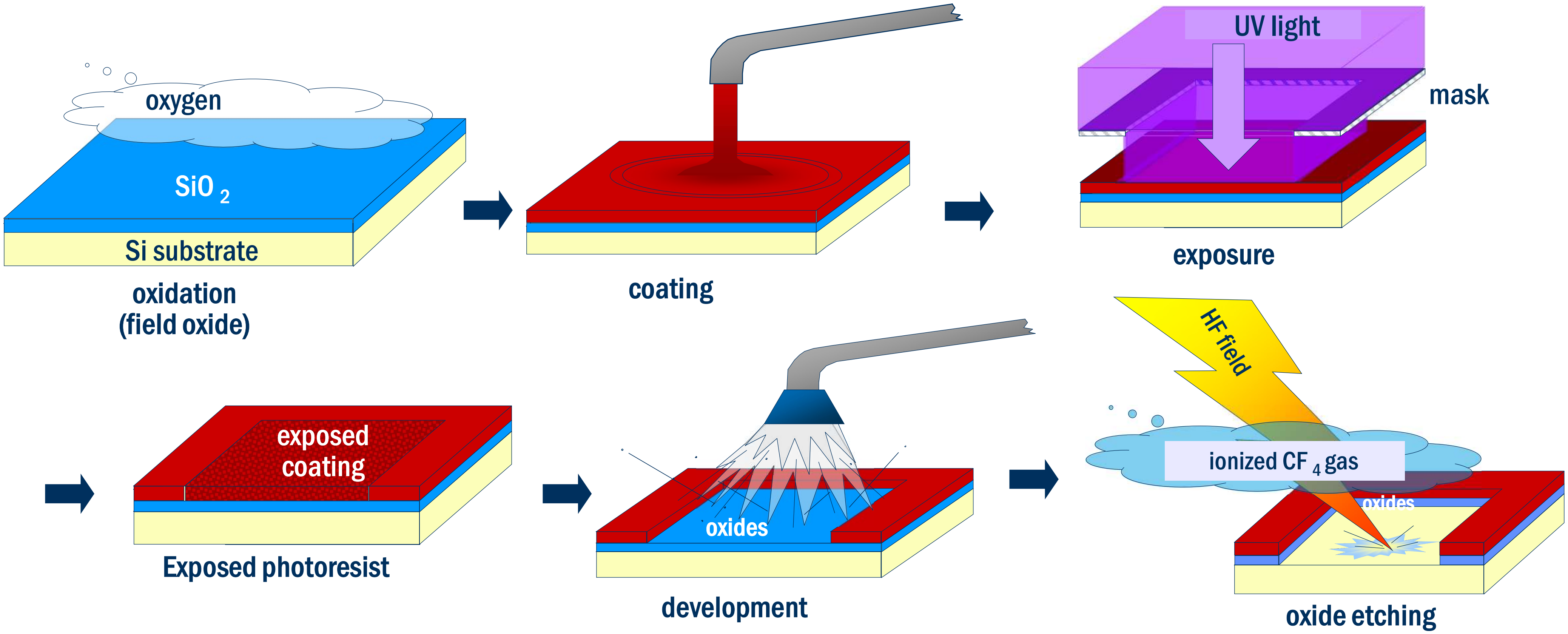
Finally, the circuits must be **isolated, installed in housings and tested** . This process sequence is often referred to as " **back-end** " **manufacturing** .

Process chain in the manufacture of an integrated circuit

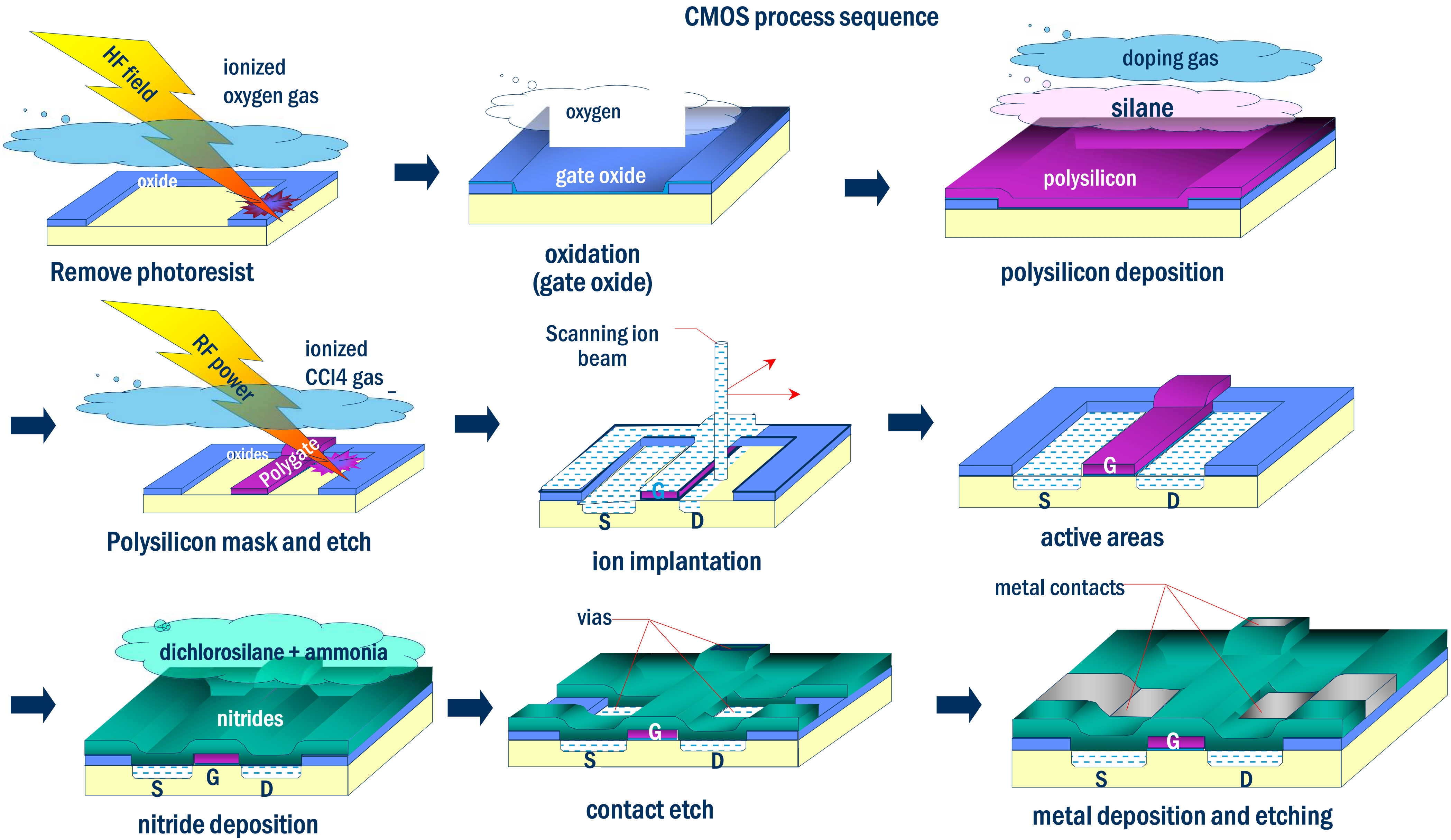


The focus of the repetitive process steps is lithography , which transfers the desired structures to the substrate with the help of photomasks. These are then etched into the surface or doped at the appropriate locations. The CMOS process suite forms the basis of most modern semiconductor processes.

CMOS process sequence



1.4 Typical Process Sequence - MOS Process Sequence -



In contrast to most manufacturing processes (e.g. automobile production), a semiconductor line is not a linear sequence of process stations , but a station can be required several times at different points in the process . This requires a very complex process control.

Complexity of a semiconductor production line