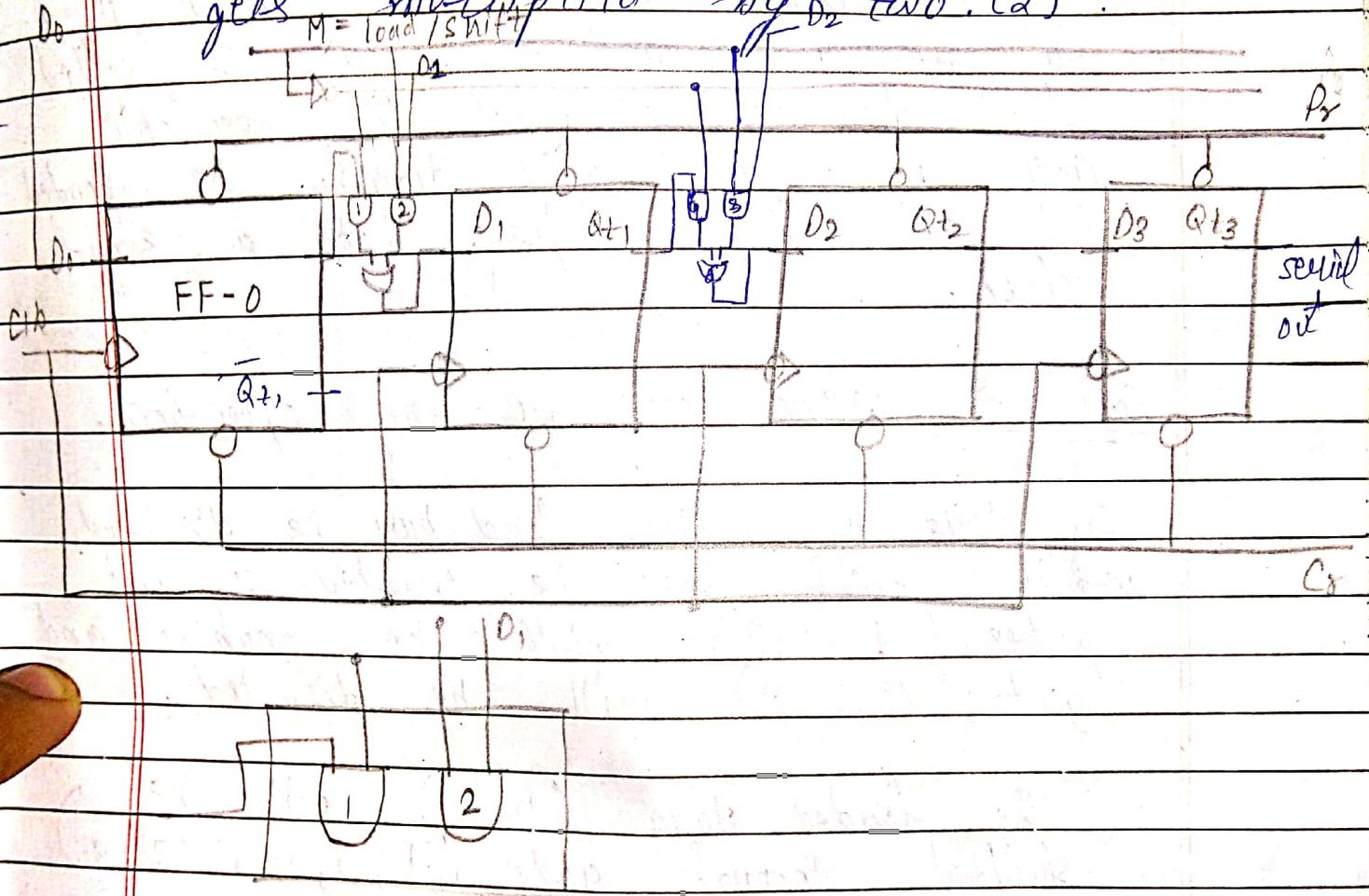


3) PISO : \rightarrow (4 bit) Parallel in serial out.

If we do left shift then value gets divided by two

and if we do right shift then it gets multiplied by 2^2 two. (2)



In parallel and serial out register, an additional set is req. b/w two flip flops that can provide the selection of load and shift operations. This ch. acts as a multiplexer.

Case I : \rightarrow When $M=1$ i.e. Load operation

In this case, the load bar is enabled while shift bar is disabled. Due to that gate no. 2, 5 and 8 (all are and gates).

PTPO :-

are also enabled b/c they are connected to the load bar and at the same time gate no -1, 4 and 7 are disabled as they are connected to shift bars.

i.e. or gate (3, 6 and 9) proceed the output coming from input D₀, D₁, D₂, D₃ via gate (2, 5 and 8). Drie is called Prod operation as all the available data to D₃ will directly be loaded into all flip flops with a single clock.

Case 2 :- When m=0 i.e. shift operation.

In this case, the load bar ie. disabled while shift bar is enabled. and gates (1, 4, 7) will be enabled and gate (2, 5, 8) will be disabled.

i.e. the loaded data (1010) will be shifted through gate (1, 3, 4, 6, 2, 9) in a serial manner.

This is the working of parallel in serial convt.

$$N_{CH} = 1 (\text{load}) + 4$$

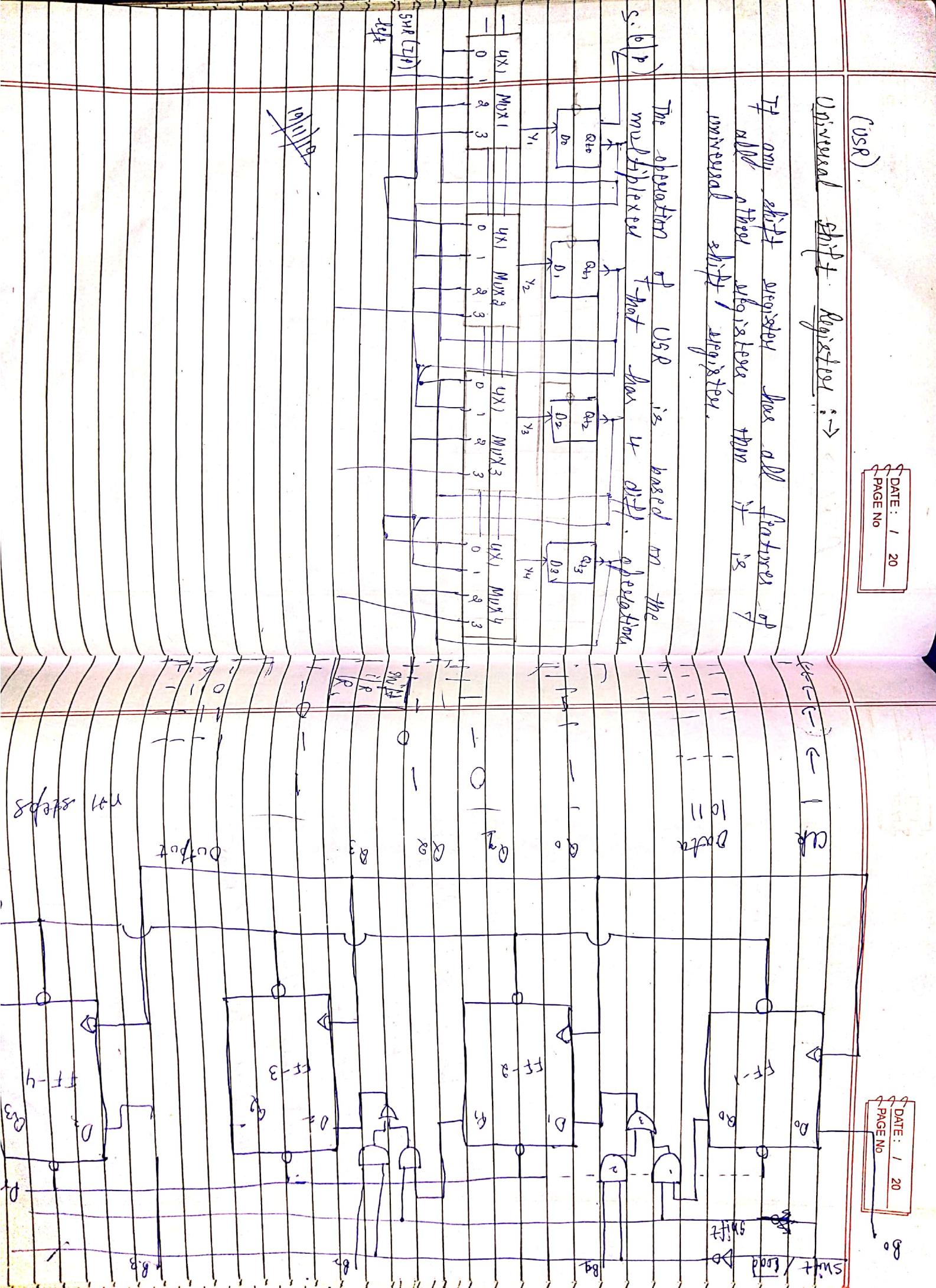
$$\boxed{N_{CH} = 1+n}$$

(USR)

Universal Shift Register :-

If only shift register has all features of other register then it is universal shift register.

The operation of USR is based on the multiplexer that has 4 diff. selection



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1010

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Assignment

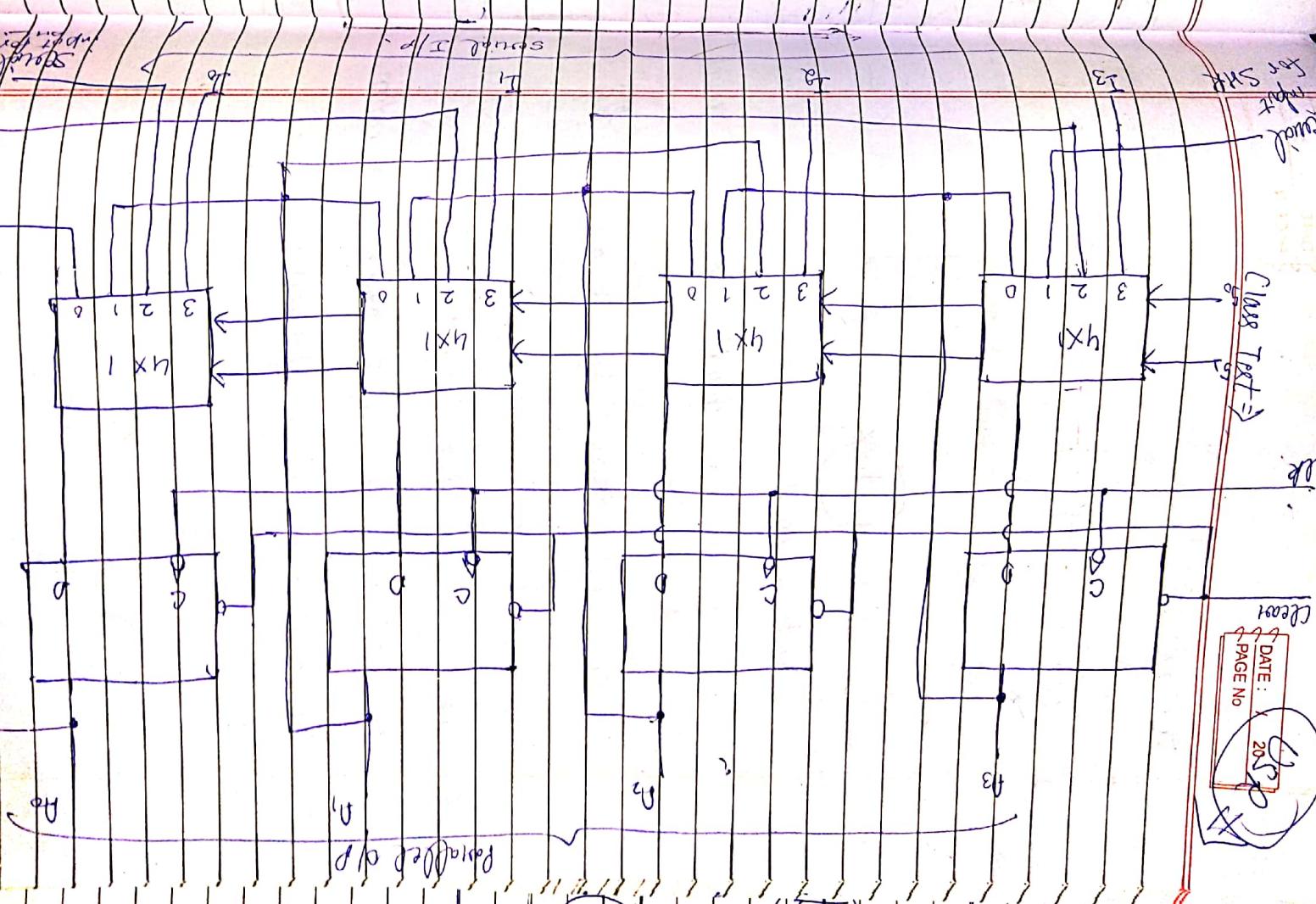
Q1. Define following for flip flops

a) Set up time (t_{su})

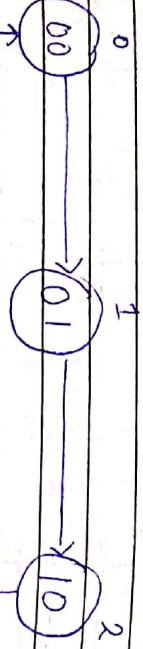
b) Hold time (t_{hp})

c) Clock skew (Clk_s)

d) Max. clock frequency (fmax). (fmax)



COUNTERS :-



- On basis of clock input & config. the numbers may be of two types :-
- (i) Synchronous counter.
- (ii) Asynchronous counter. (Ripple counter).

State Diagram

A kind of sequential circuit that can count the input pulses.

Counters can be designed by JK and T flip-flops.

Types of counters :-

↳ Based on following things :-

- o) When clock is applied simultaneously across all the flip-flops called synchronous counter.
- o) When clock is applied to first flip-flop only and output of first flip-flop can be used as a clock for the next flip-flop ie called asynchronous counter.

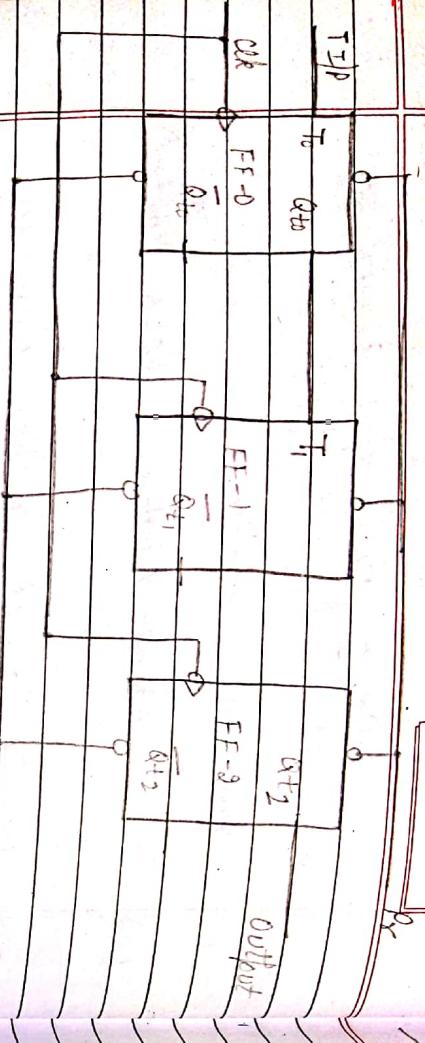
- On basis of counting operation
- (i) Up-down counter - (Bidirectional counter)
- (ii) Down counter

Synchronous Counter

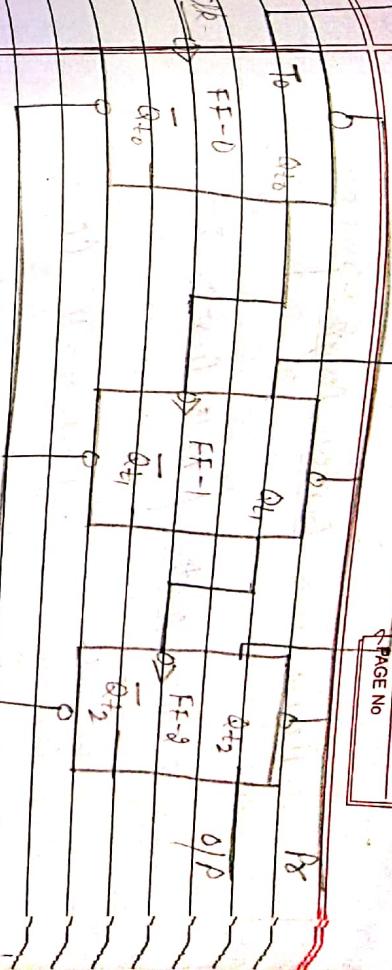
Asynchronous Counter

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b) Search counter means the synchronization means operation is synchronized clock dependent.

by common clock pulse circuit. but the input and

will be important to divide the change in a

flip-flop i.e. synchronous counter means input

dependent

c) Design is simple and 1). Designing is little easy to maintain. bit complex.

d) Operation is fast. d) Operation is slow.

Due to propagation delay of flip-flop there will be a subtle unwanted state between two

stages and the operation of counting of slow. they are also called in the counters.

Synchronous Counter Design :-

Modulus = 9 -

We can form mod-8 or mod-3 by modifying mod-4 counter.

Modulus of Counter / Modulo Counter :-

0 0

0 1 No. of states = 4. (2^2)

1 0 Modulus Counter = 4.

1

Mod = 8

0 0 0

0 0 1

0 1 0

0 1 1

1 0 0

1 0 1

1 1 0

1 1 1

0 0 0

0 0 1

0 1 0

4 - MOD 5 - 8

$2^3 \rightarrow$ no. of flip-flops required to design the counter.

Decade counter - Mod 10.

The modulus of a counter can represent the no. of states to be counted by a counter.

In simple language, modulus of a counter means number of states that can be counted by a counter during counting operation.

Mathematically, if modulus counter is MOD = N, where $n =$ no. of flip-flops required to design the counter.

Modulus of Counter means count capability of a Counter.

The max. count capability = 2^n ($n=7$)

Mod = 3 (Counter)

0 0 1

0 1 0

1 0 1

1 1 0

1 1 1

Mod = N

= 2^n

\rightarrow J

No. of bits (no. of flip-flops) \rightarrow JK

State Diagram (Most Imp). — Counting State

— Used State

— Unused State

— Up/Down bidirectional counter.

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⇒ Counter can also be used as frequency divider

Clock or timing control clock.

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Downcounter (DCL) : →

$\rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 0 \rightarrow$

If we use the \bar{Q}_2 instead of Q_1 as the input of clk of FF-2.

Clk Q_n

$Q_1 \Rightarrow \text{Clk} \rightarrow D_1 \text{ with initial } 1$

(condn) 11

①

$\bar{Q}_2 \Rightarrow \text{Clk} \rightarrow D_2 \text{ with init.}$

(condn) 00

1

②

$Q_2 \Rightarrow \text{Clk} \rightarrow D_2 \text{ with init.}$

(condn) 00

0

③

$\bar{Q}_1 \Rightarrow \text{Clk} \rightarrow D_1 \text{ with init.}$

(condn) 11

1

④

$T = 1$
Mod-5 div by 5

Mod-8 div by 8.

Q_0

Q_1

Q_2

Q_3

Clk

$Q_0 = 11$

00

01

00

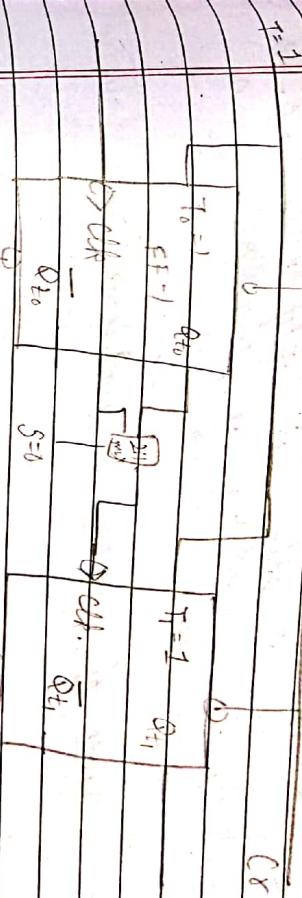
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BIDIRECTIONAL COUNTER : →

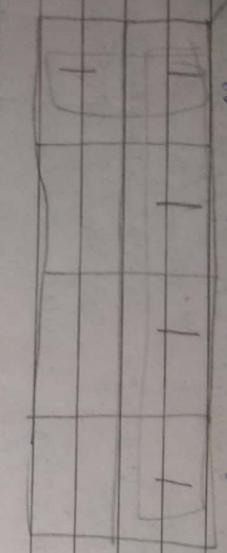
Mod Control

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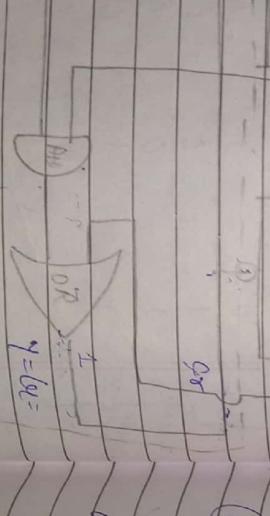
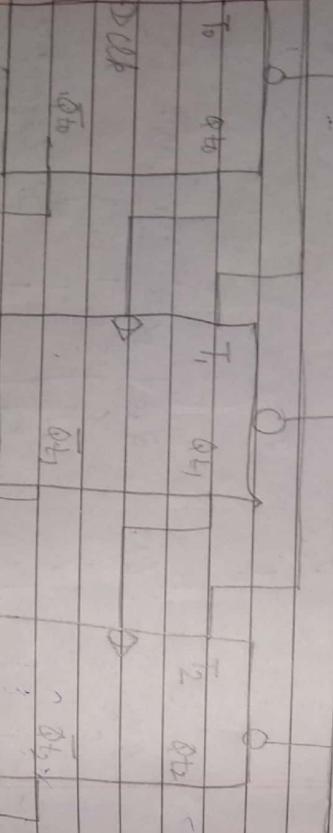
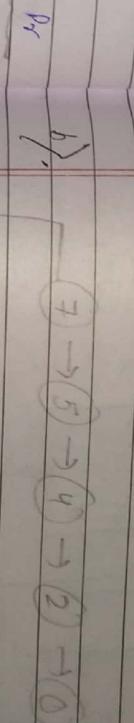
Programmable Counter



Design ripple counter for full state diagrams.



$$y = \beta_{t_2} + \beta_{t_3} \cdot \beta_{t_4}$$



$\rho_s > \text{Active High}$ $y=0 \quad v.s.$
 $\rho_u < \text{Active High}$ $y=1 \quad v.s.$

$\Rightarrow Clk \rightarrow \neg v_p$

b). Design a dead ripple counter. Mod 10.

Reset logic.

b) $C_{lk} \rightarrow \text{time}$

$Q_t \rightarrow \text{Clk} - DC$

$\bar{Q}_t \rightarrow \text{clk - vpc.}$

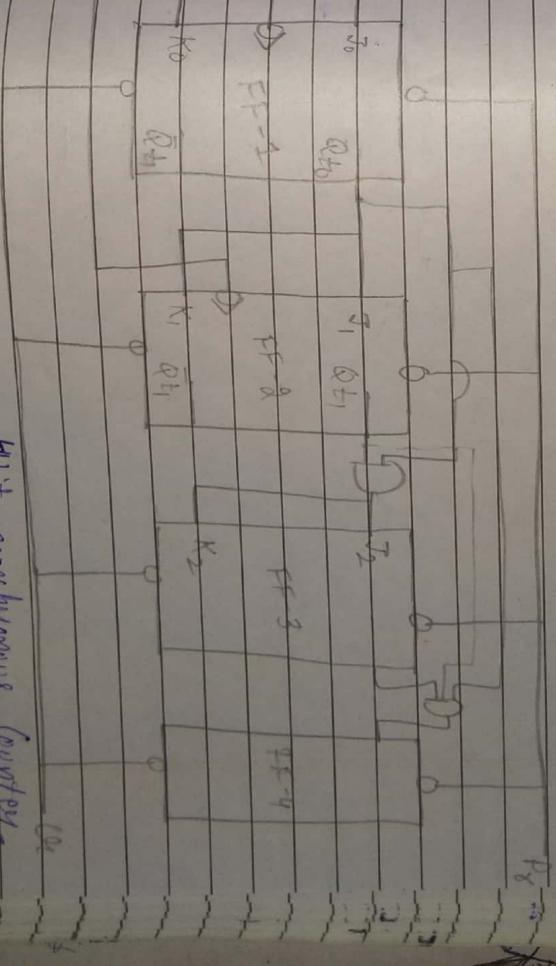
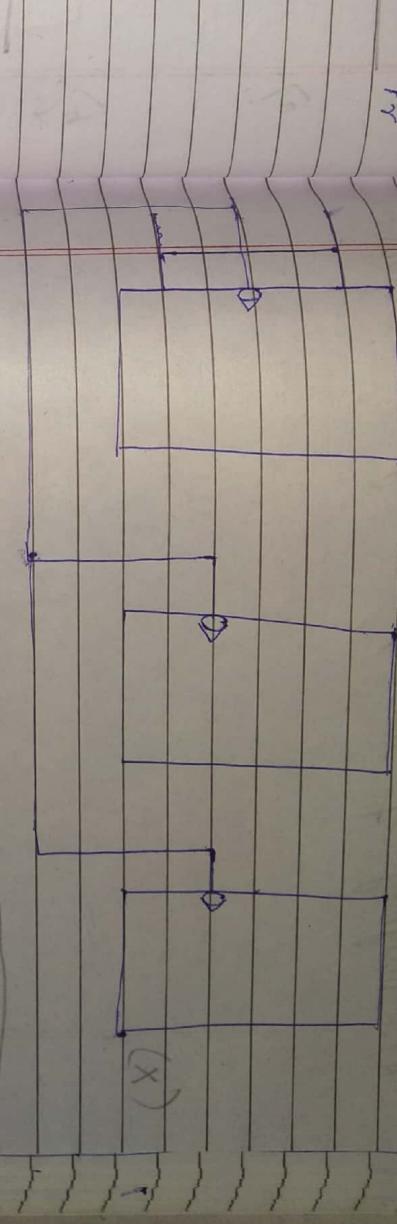
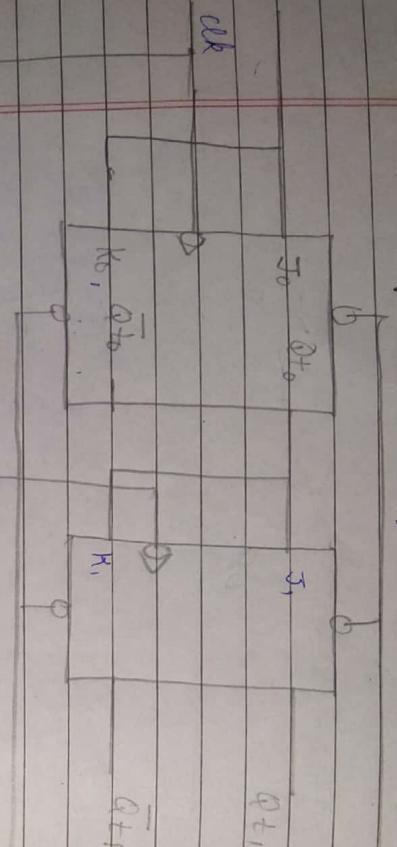
$0 \rightarrow 1 \rightarrow 2 \rightarrow 3$
 $1 \rightarrow 0 \rightarrow 1 \rightarrow 0$
 $y = f(x)$
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2-bit synchronous up Counter :-

P.T.



4-bit synchronous counter

(a)

Applications of Counter:

- 1) Frequency divider circuit.
- 2) As a clocked seq. ckt that can be used for timing control in digital processor.
- 3) In state machines (finite state machine).

$Q_1=0$

0

$Q_2=0$

01

on 10

00

UNIT - V

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LOGIC FAMILY

Logic families is relevant to design the IC's. ∵ designing process is standardised as per the requirement & design rules. and these design rules are common for all kinds of circuits based on technology.

As a whole the designing of such circuit for a common technology is referred as a logic family.

Types of logic families : → (BJT) :

Saturated LF \swarrow Bipolar or (CCIT) : TTL, DTL.

(2)

Unsaturated LF.

\searrow ECL

~~BJT~~ T²L. (Int. injection logic).

~~BJT~~ BJT : \rightarrow Bipolar junction Transistor.

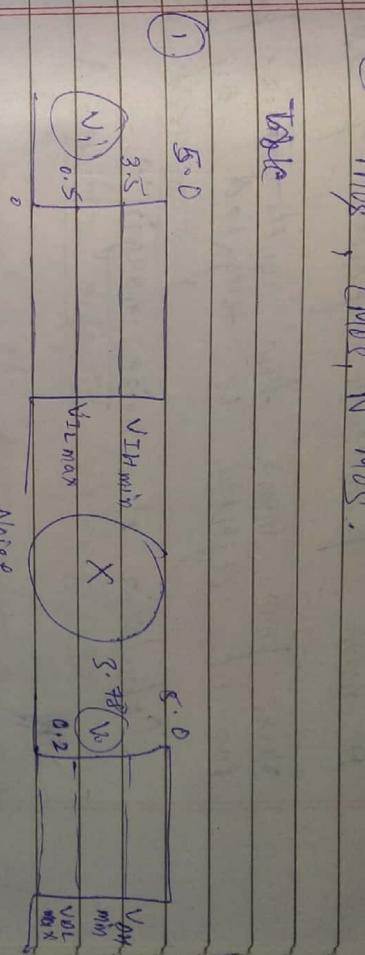
Bipolar :

Bipolar TTL \neq C

Unipolar means (\neq mos, nmos & pmos) designing.

Standard Parameters :

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$V_{IH\ min}$: The max. input voltage that can be considered as logic low.

$V_{IH\ max}$: This is the minimum input voltage that can be considered as logic high.

$V_{IL\ min}$: This is the max. output voltage that can be considered as logic low.

$V_{IL\ max}$: The min. output voltage that can be considered as logic high.

Noise margin: \Rightarrow A quantitative measure of noise immunity is k/a noise margin.

A noise tolerance power of chip -

Noise imm. means how much noise source can be rejected by tolerated by chip.

Calculation of noise margin :-

'N'

1). Low noise margin: \rightarrow LNM :-

$$V_{I\max} - V_{I\min} = 0.5 - 0.2 = 0.3.$$

$$\Delta V_{I\max} = V_{I\max} - V_{I\min} = 3.78 - 3.5 \\ = 0.28.$$

For a high speed device the value of propagation delay is less.

3). Fan-in : \Rightarrow No. of inputs that can be driven by logic standard logic fan-in is the max no. of inputs in a given word

$$\text{Speed} = 1/t_p$$

4). Fan-out: Max no. of -o/p that

can be driven by a logic gate w/o. the degradation logic standards fan-out.

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In order to design power dissipation is to be reduced to improve the power backup of system.

Operating temp is typical parameter of IC designing that can restrict the opp. of a part. In I_C

: range of temp. of an IC can permit its using the application.

(speed power product) (figure of merit)

SPP

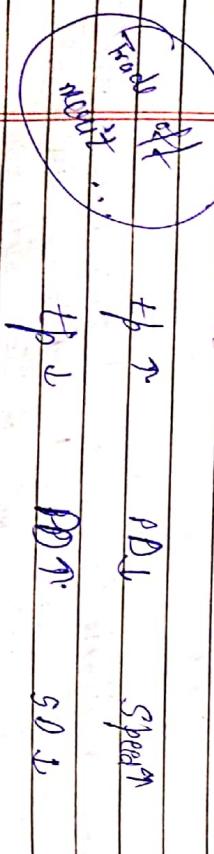
I_C decides the degree of performance.

$$(SPP = t_p \times P.D)$$

SPP means product of pro. delay and power dissipation.

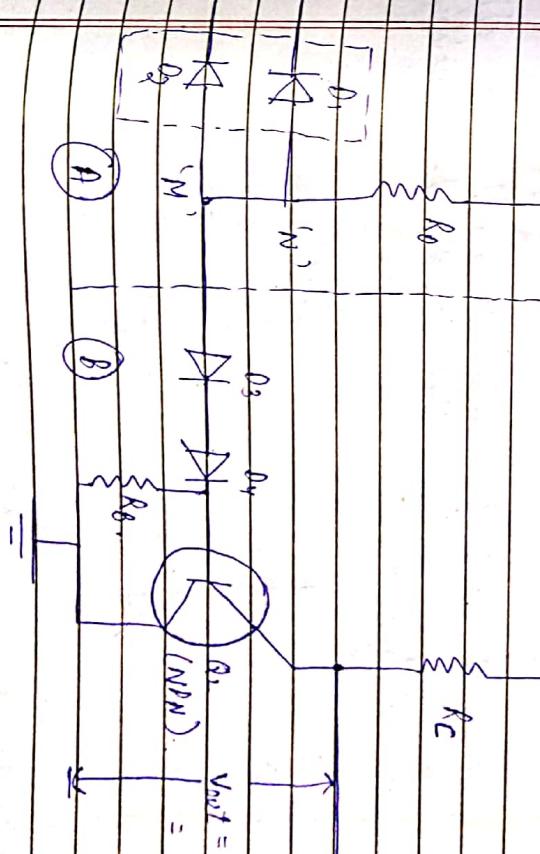
$$SPP = t_p (P.D) = 10^{-9} \times 10^{-6} = 10^{-15} \text{ pJ.}$$

This SPP has constant value of a device.



A

B



Unipolar logic families :-

P MOS
NMOS

C MOS

Saturated

↓

: DTL

↓

: TTL

↓

: ECL

↓

: TAL X

↓

: Unijunction Transistor Logic

↓

: Bi polar logic Families :-

↓

: NPN

↓

: PNP

↓

: Bipolar logic Families :-

↓

: CMOS

Note :- NPN is better than PNP b/c emitter is of n type : large no. of e⁻ and mobility of e⁻ is higher than that of PNP. i.e. more speed.

Operation:

1)

when $A = B = 0$. i.e. A and B are connected to ground.

A

B

- * that means voltage at node 'N' will be approximately +5V.
- * that makes diode D₁ and D₂ in forward bias condition.

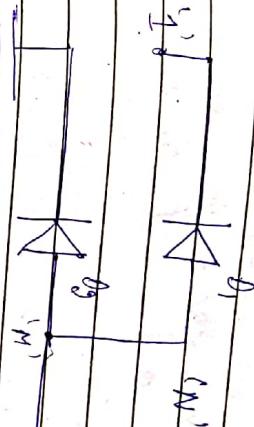
In this condition, diodes D₃ and D₄ will remain off.

To this emitter-base junction of a npn transistor will be off.

Hence, the output which will get approximately 5V. and that is to be considered as logic 1.

A B X = $(A \cdot B)$

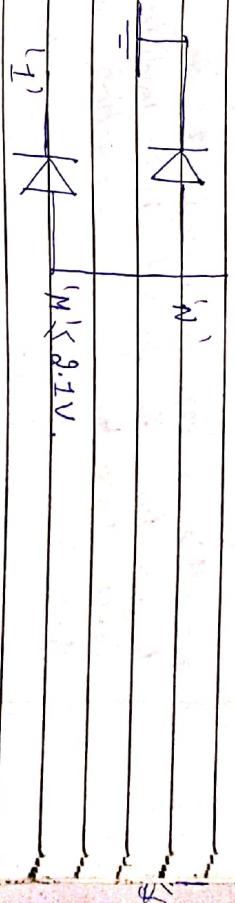
| | | |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |



To this

because of D₃, the node voltage at 'N' is not sufficient to drive the transistor D₄ into saturation. It remains off. Hence the output of the circuit remains same as in the previous case.

When $A=0$ $B=1$



When $A=0$ $B=1$

In this case, diode D₁ is in forward bias condition which diode D₂ is in reverse bias condition.

Q)

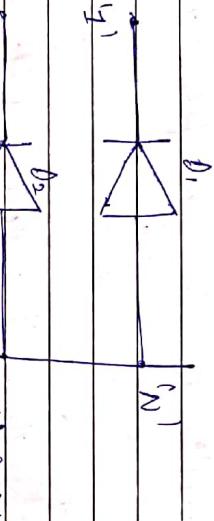
When $A=1$ $B=0$ then.

A

So because of diode D_1 , the node voltage at point 'N' is not sufficient to drive the transistor Q into saturation and it remains off. Hence, the output of circuit is approx. equal to $+V_{CC}$

$$i.e. +5V = \text{logic '1'}$$

Case 4: when $A=1$ and $B=1$.



In this case, both diodes D_1 and D_2 are in reverse bias condition i.e. the voltage at node 'N' is approx. $5V$.

and this voltage is sufficient to make diode D_2 in forward bias condition that makes transistor Q in saturation mode i.e. transistor will be on

Hence the output of circuit is approximately on i.e. logic 0.

Now, according to above said description the following table can show the working of

logical circuit.

Now, according to the table we can say that the circuit is working as a NAND Gate.

Advantages:

- Higher fan out is possible.
- It has greater noise immunity.
- Little bit economical.

TTL \Rightarrow stands for Transistor Transistor Logic.

It uses the transistor only that's why called TTL.

Most popular bipolar logic family that was developed in 1965 with the name of standard TTL.

It has two configurations (for more impedance)

- First with TTL with transistor output stage.
- Second is open collector output stage.
- (for less impedance)

TTL Nand gate with internal output stage :-

Trans-paleo

$$+V_{CC} = +5V$$

✓✓✓

4

10

T₃X

1

1

4

1

1

1

1

1

10

11

1

100

3

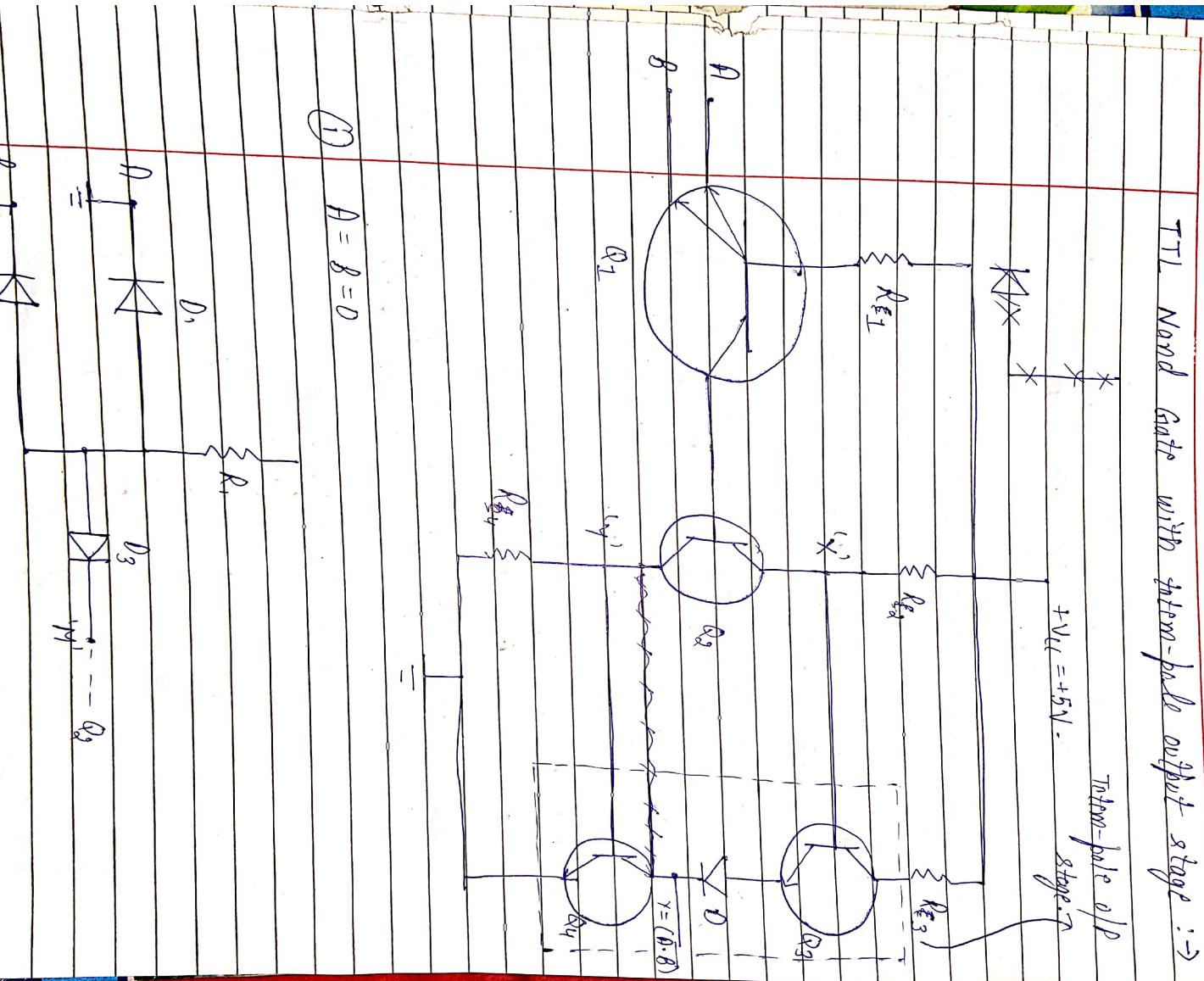
10

1

1

•

2



when $\beta=0$

* In this case diode D_1 is in forward bias condition while D_2 and D_3 are in reverse bias condition.

* In this case diodes D_1 and D_2 are in forward bias condition while diode D_3 is in reverse bias condition.

* The reverse bias condition of D_3 does not make Q_2 into saturation mode and it remains off.

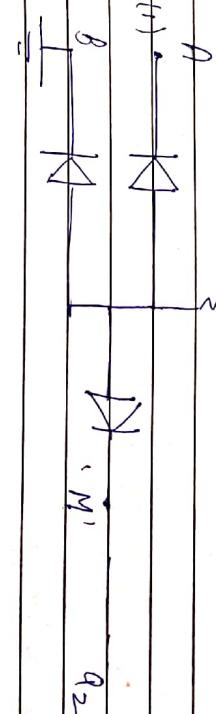
* As a result of this, the transistor Q_3 also remains off.

* At the same time, the transistor Q_3 is in saturation mode as the voltage at node 'X' is quite sufficient to drive the transistor Q_3 into saturation.

* If Q_3 is in saturation mode (i.e. on), it makes diode D in forward bias condition.

Hence, the output of circuit is approximately true i.e. near about 5V considered as logic 1.

Case 2: when $\beta=0$ and $\alpha=1$



Similar to case 2 where diode D_1 is in forward bias and D_2 , D_3 in reverse bias condn.

$b_{(1)} \rightarrow D_2$



Now, in this case diode D_1 is in forward bias and D_2 , D_3 in reverse bias condn.

Unipolar better than Dipolar.

Case 4: When $A = B = 1$

$D_1 \quad R_1$

$+5V$



In this case, diode D_1 and R_1 both add in reverse bias condition that makes diode D_3 in forward bias condition.

Now, because of forward bias cond. of D_3 , the voltage at node 'M' is quite sufficient ($0.7V$) to drive the transistor Q_3 into saturation and that force on transistor Q_4 into saturation.

\therefore in trim-pole off stage both transistors Q_3 and Q_4 go into saturation with forward bias condition of diode D_3 ($0.7V$).

Hence current of Q_4 is approximately

Advantages:

1) Reduces power dissipation.
2) Better fan in and fan out ratio.

3) It has accurate value of g_m . that makes the circuit family the most convenient and suitable in case of higher gain.

classfellow

Disadvantages:

1) Improve capacitive nature of off. at off stage.

2) Desynchronization b/w Q_3 and Q_4 .

MOSFET \rightarrow Metal oxide semiconductor field effect

NMOS channel is of p-type

NMOS is of n-type.

NMOS is better than PMOS

CMOS comb. of PMOS and NMOS.

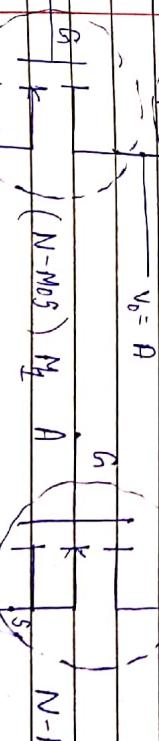
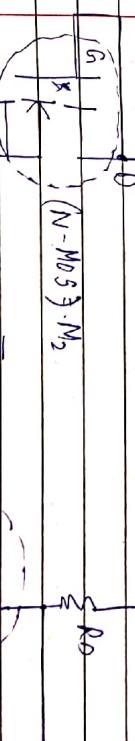
Two types of Mosfet:

1) Depletion type 2) Enhancement type.

N-Mos Inverter (NOT):

$$+V_{DD} = +5V$$

$$+V_{DD} = +5V$$



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G - Gate

D - Drain

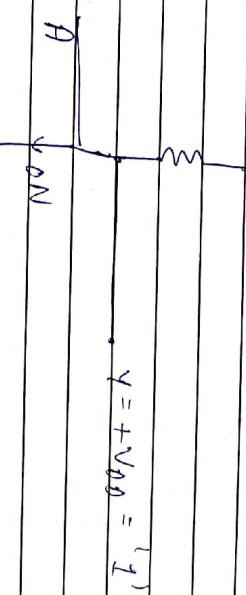
S - Source

Q1) When $A = 0$ that means voltage across gate source terminal is 0V. i.e. $V_{GS} = 0V$.

g) This V_{GS} voltage is not sufficient to turn on the transistor N_2 (N-MOS).

$$i_g = k(V_{GS} - V_{TH})^2$$

$$\begin{aligned} V_{GS} &> V_{TH} \\ V_{GS} &\geq 0.7V \end{aligned}$$



Case g) \rightarrow When $A = 1$ i.e. $V_{GS} = +V_{DD} = +5V$.

i.e. Transistor N_2 turns on \therefore output of ckt.

and op of ckt = logic 0.

$$\begin{array}{c} A \\ \text{---} \\ 0 \\ | \\ 1 \end{array} \quad Y = \bar{A}$$

Q1) Design a input NAND gate using NMOS logic.
Design 2 input NOR gate using NMOS logic.
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V.Imp.

3). CMOS Inverter :>

$$V_{DD} = +5V$$

P-MOS

N-MOS

$$V_D = V_{IN}(R_2)$$

Case 1 :> When $V_{IN} = 0V$ ('0')

In this case, transistor P-MOS i.e. Q_2 will be off. N-MOS Q_1 will be on. $+V_{DD} = +5V$

Q_2 ON

$$V_D = +5V = '1'$$

$$Q_1 = 0 \neq \rho$$

Case 1 :>

When $V_{IN} = +5V$ the pmos Q_2 will be off while NMOS i.e. Q_1 will be

on. ρ of Q_2 = logic 0.

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Advantages of CMOS logic :-

- 1) Much faster than other logic families whether bipolar or unipolar.
- 2) It consumes extremely low power as compared to other MOS families.
- 3) It has greater fan-in & fan-out as compared to other families.
- 4) Design & exp. working of full-gates using CMOS logic.
- 5) 2-input NOR gate
- 6) 2-input NAND gate.

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