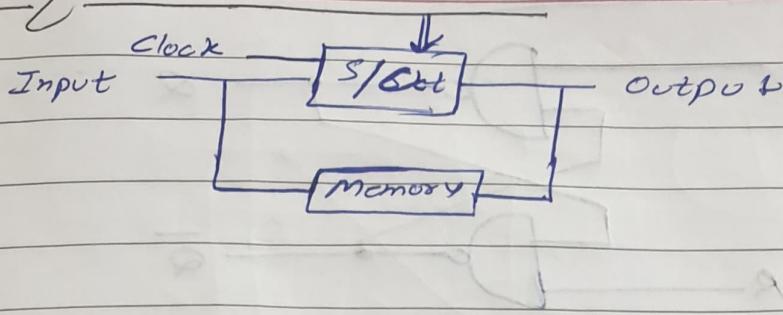


## A) Sequential Ckt.



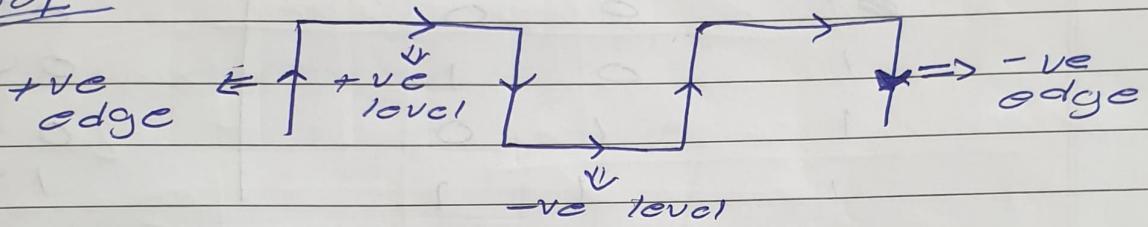
input changes  
% to output  
(A)  
output  
also changes  
% to  
new input

## A) Flip-Flop =>

sequential ckt. used to store 1 bit data

1-Bit logic-1 — +5V  
logic 0 — 0V  
FF Bi-stable multivibrator

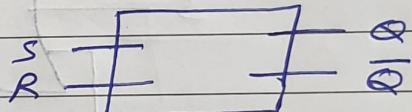
### Graph



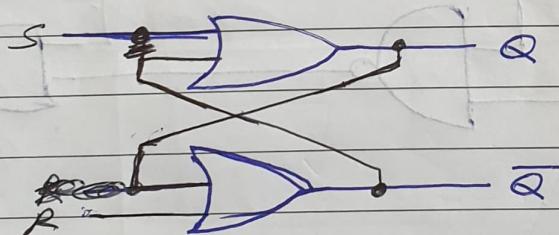
## Types of Flip-Flop =>

SR / JK / D / T

## A) SR - Flip-Flop =>

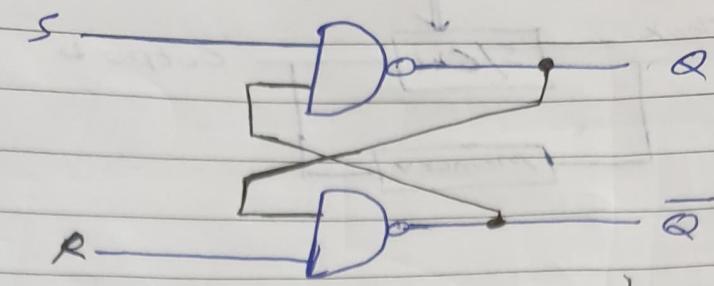


= NOR SR latch



S	R	$Q(t)$	$Q(t+1)$
0	0	0	0 ] $Q(t)$
0	0	1	1 ]
0	1	0	0 ] $\text{reset}$
0	1	1	0 ]
1	0	0	1 ] $\text{set}$
1	0	1	1 ]
1	1	0	0 ] $\text{invalid}$

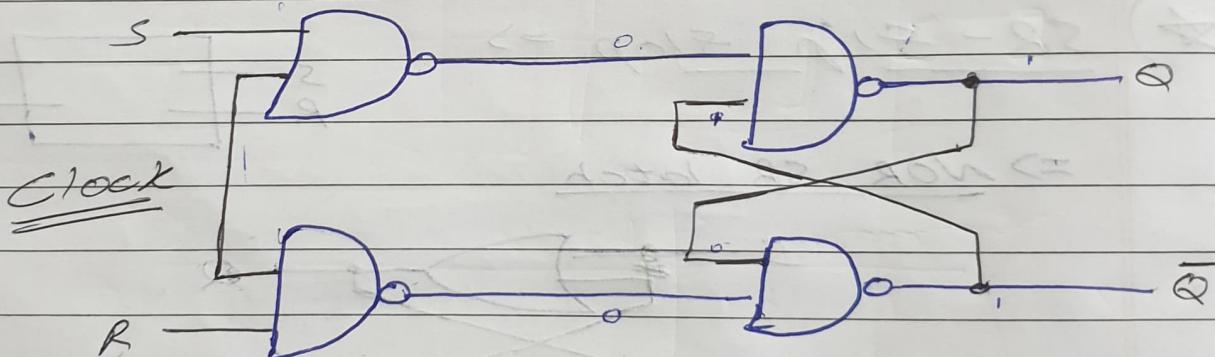
$\Rightarrow$  SR NAND Latch



S	R	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	1	0
1	0	0	0
1	1	0	1
1	1	1	1

0 X ] invalid  
X X ] set  
0, 1 ] reset  
0, 0 ] 0 (0)  
0, 1 ] Q(t+1)

(\*) SR Sip - Slop



## A) Characteristic Table

	S	R	$Q(t)$	$Q(t+1)$
1	0	0	0	0 ] Q(t)
2	0	0	1	1 ] No change
3	0	1	0	0 ] Reset.
4	0	1	1	0 ] (S=0)
5	1	0	0	1 ] Set (S=1)
6 <del>Character</del>	0	-	1	-
7	1	1	0	X ] Don't care
8	-	1	1	X ] (S=R=1) (Invalid)

$\Rightarrow$  characteristic eq'

S	$\bar{R}Q(t)$			
	00	01	11	10
0	.	1	.	.
1	1	1	X	X

$$Q(t+1) = S + \bar{R}Q(t)$$

$$\Delta [SR=0]$$

to remove  
Don't care / Invalid

## B) Excitation table

(reverse of ch-table)

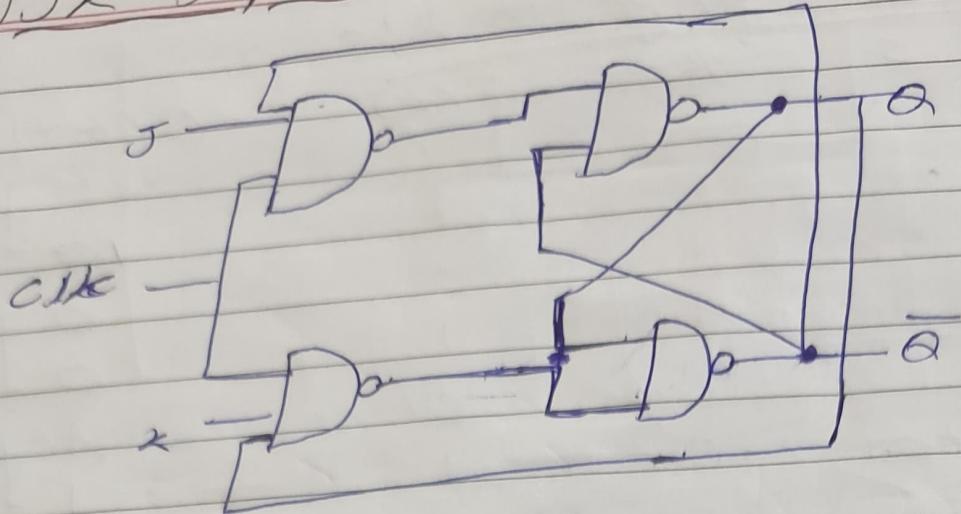
$Q(t)$	$Q(t+1)$	S	R	
0	0	0	X	(1, 3)
0	1	1	0	(5)
1	0	0	1	(4)
1	1	X	0	(6, 2)

## C) Disadvantage of SR Slip-Slop $\Rightarrow$

In SR Slip-Slop a invalid state is present when  $SR = 1$

To avoid invalid state JK Slip-Slop is used

~~A) JK~~ JK ~~slip - stop~~  $\Rightarrow$



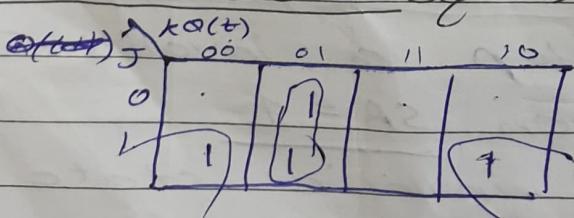
To To

J	K	$Q(t)$	$Q(t+1)$
0	0	0	0 ] no change $(J=K=0)$ [ $Q(t)$ ]
-0	0	1	1 ] Reset $(J=0)$
0	1	0	0 ] Set $(J=1)$
0	1	1-	
-1	0	0	1 ] Set $(J=1)$
-1	0	1	1 ] $Q(t)$
-1	1	0	0 ] Toggle
1	1	1-	

xx

J	K	$Q(t)$	$Q(t+1)$
0	0		$Q(t)$
0	1		0
1	0		1
1	1		$Q(t)$

$\Rightarrow$  characteristic eqn  $\Rightarrow$



$$Q(t+1) = J \bar{Q}(t) + \bar{K}Q(t)$$

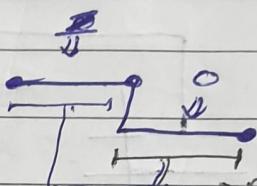
$\Rightarrow$  excitation table

$Q(t)$	$Q(t+1)$	$J$	$K$
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Note: { Is  $J=K=1$   
 A clock is applied for long time  
 then output will be fluctuating  
 e.g.  $\Rightarrow 01010101$   
 race around condition } as at time  $t$   $Q(t) = 1 \Rightarrow Q(t+1) = 0$   
 for next state in time  
 $t = t+1$   $Q(t) = 0 \Rightarrow Q(t+1) = 1$

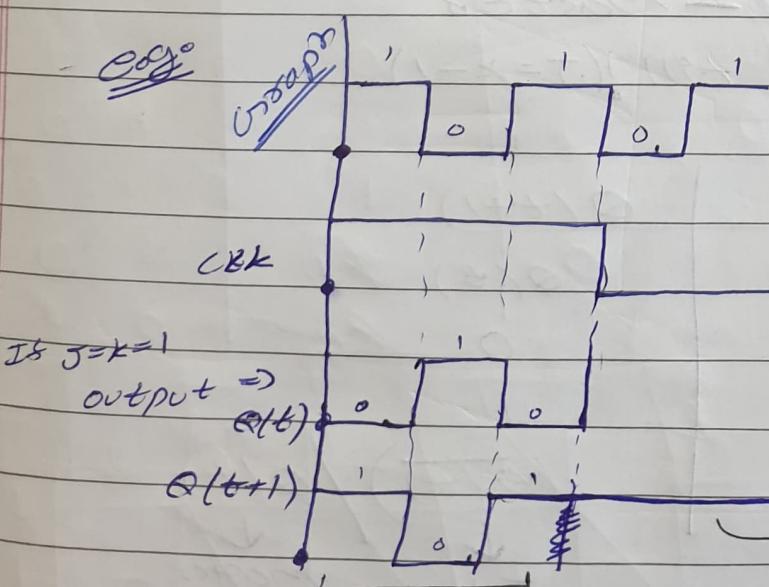
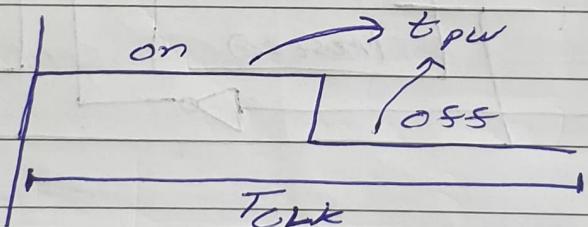
### \* Propagation Delay

$$t_{pdFF} \Rightarrow$$



( $t_{pdFF} \rightarrow$  propagation delay of flip flop)

Clock pulse  
 $(t_{pw})$   
 $pw \rightarrow$  pulse width



Is  $J=K=1$

output  $\Rightarrow$

$$Q(t)$$

$$Q(t+1)$$

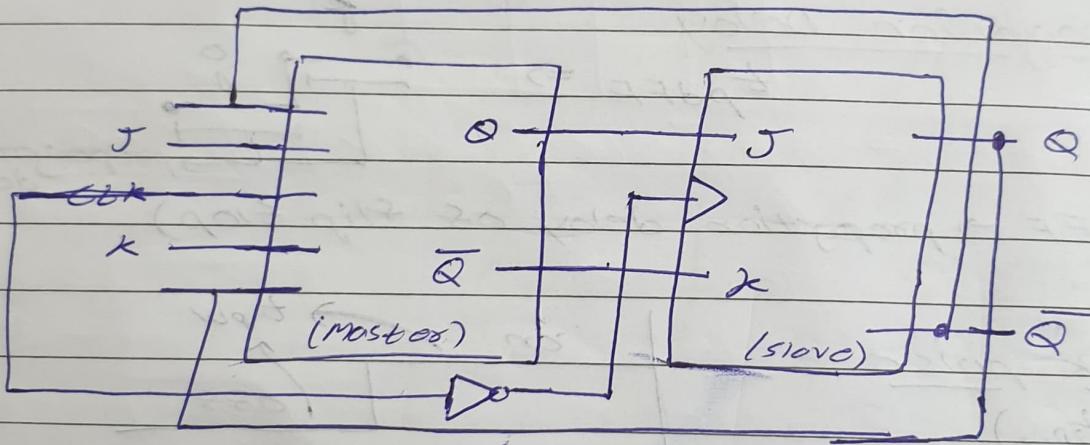
race around condition

{ To overcome race around time of CLK on should be less than  $t_{pdFF}$  }

## ~~A) Disadvantages of JK flip-flop~~

- If  $t_{PDFF} < t_{pw}$  &  $J = K = 1$   
 $\Rightarrow$  race around will occur & output will change more than once in a single clock ( $clk$ )
- To avoid race around  
 $T_{clk} > t_{PDFF} > t_{pw}$   
 ↪ (Tough) ↪ (use this)
- To avoid race around condition  
 Master Slave JK flip-flop is used

## ~~B) Master Slave JKFF~~



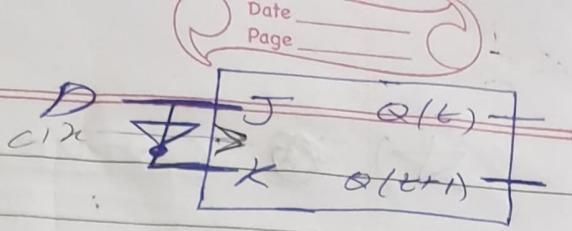
~~Master = Slave~~

~~if  $J = K = 1$~~

$J$	$K$	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$(\overline{Q(t)}) / Q(t)$

↓                      ↓  
 JK                      master slave

\* Data Slip-Slop  $\Rightarrow$   
 (D: slip-slop)  
Truth table



D	$Q(t)$	$Q(t+1)$
0	0	0
0	1	0
1	0	1
1	1	1

Characteristic eq =

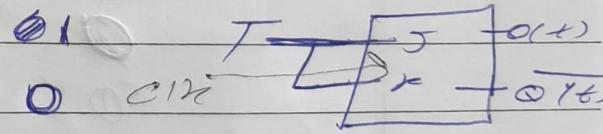
$$Q(t+1) = D$$

excitation table

$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

\* Toggle Slip-Slop  $\Rightarrow$

T	$Q(t)$	$Q(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0



Characteristic eq =

$$Q(t+1) = T \oplus Q(t)$$

excitation table

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

★) ~~Conversion of~~ Conversion of SR - flip-flop

$\Rightarrow$  JK to D  
 ↓ same      ↓ Target

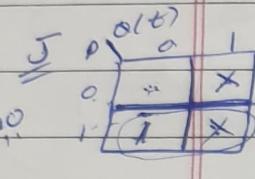
~~Table~~ Excitation of source  
 Truth of target +

D	Input (excitation)		J K
	$Q(t)$	$Q(t+1)$	
0	0	0	0 X
0	1	0	X 1
1	0	1	1 X
1	1	1	X 0

$\downarrow$

Output (Truth)

$\left\{ \begin{array}{l} J = D \\ K = \bar{D} \end{array} \right. \quad \text{eqn}$



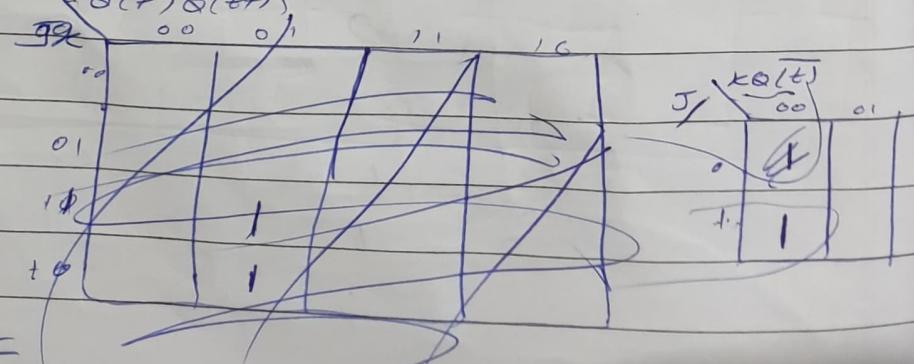
~~JKSR~~  $\Rightarrow$  SR to JK

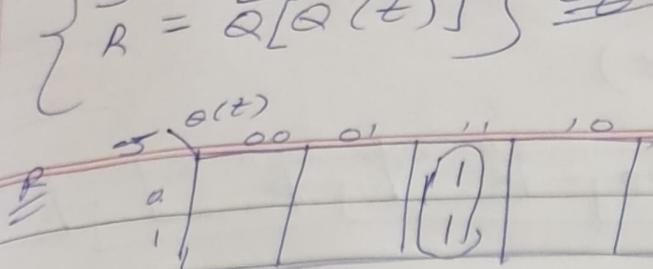
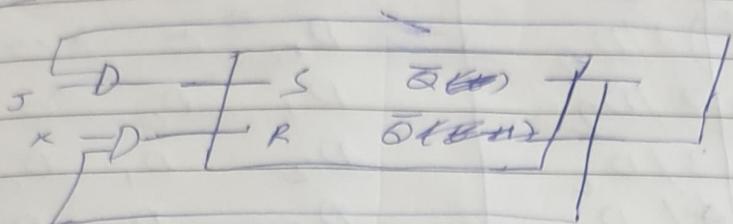
J	K	$Q(t)$	$Q(t+1)$	S R
0	0	0	0	0 X
0	0	1	1	X 0
0	1	0	0	0 X
0	1	1	0	0 1
1	0	0	1	! 0
1	0	1	1	X 0
1	1	0	1	! 0
1	1	1	0	0 1

$Q(t)$   
 000  
 001  
 010  
 011  
 100  
 101  
 110  
 111

$J \neq S$

$S =$



ConversionConversion

To convert various flip-flops into each other

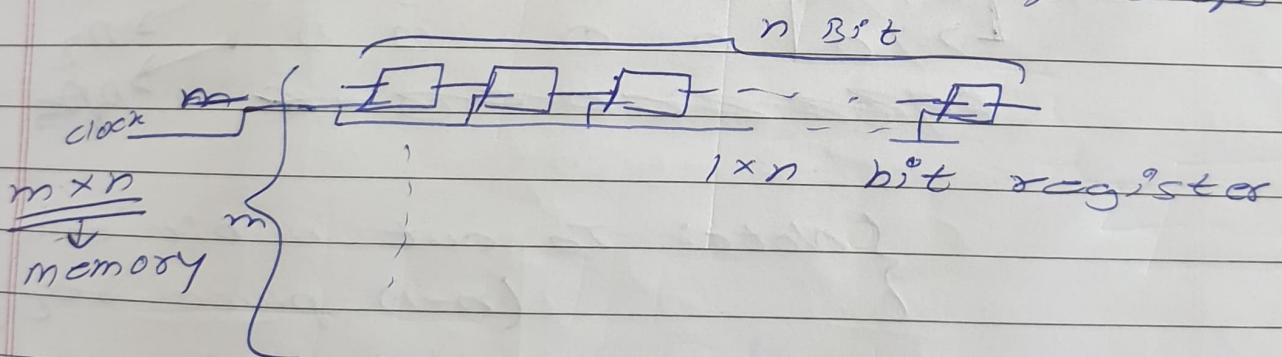
\* Registers  $\Rightarrow$

Flip-Flop used  $\Rightarrow$  D, JK, T

To store  $n$ -bit data

$\Rightarrow$  'n' flip-flops are used  
in ~~register~~ register

$\Rightarrow$  It is combination of flip-flops

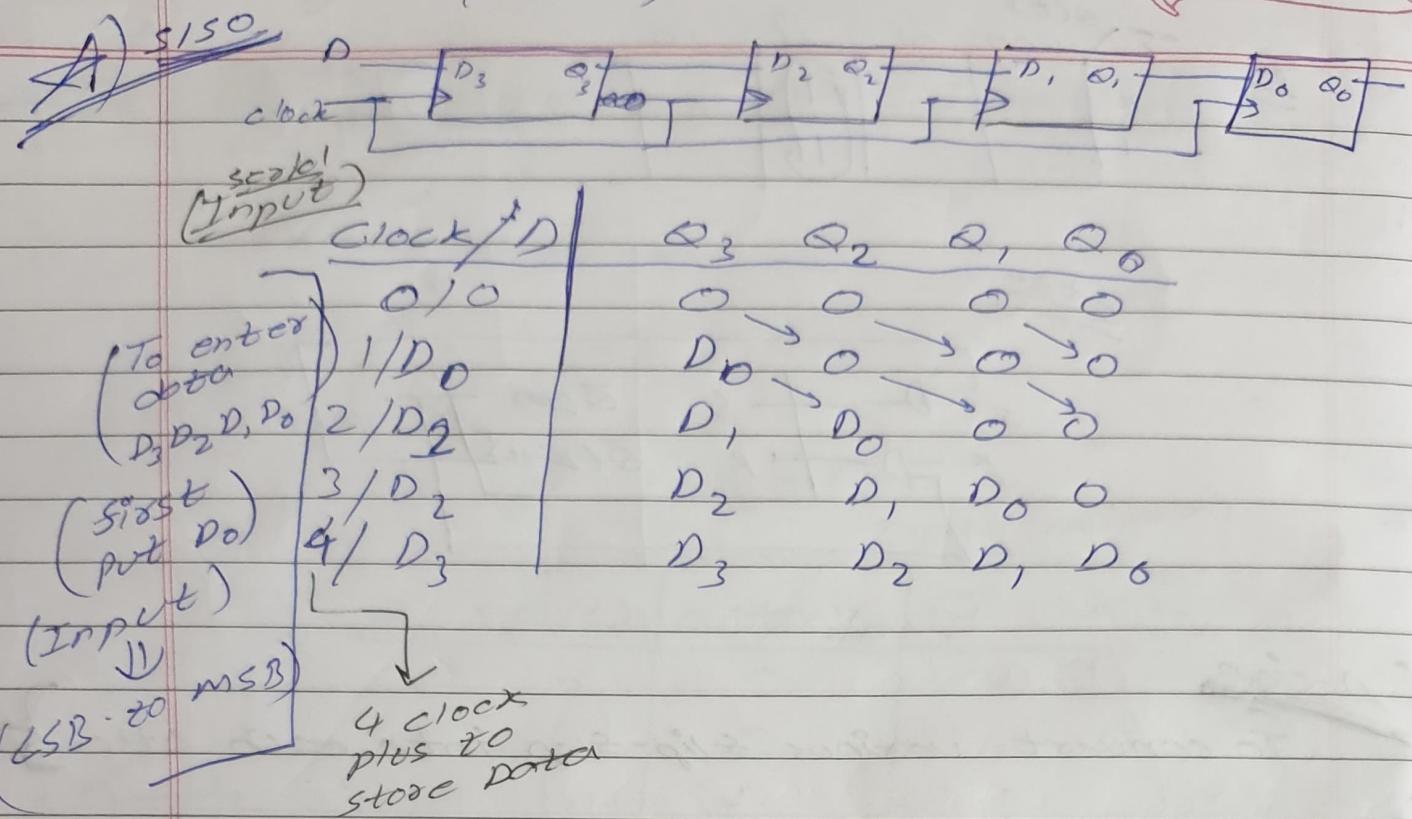


$\Rightarrow$  Based on application registers are divided in 2 parts

i) storage      ii) shift

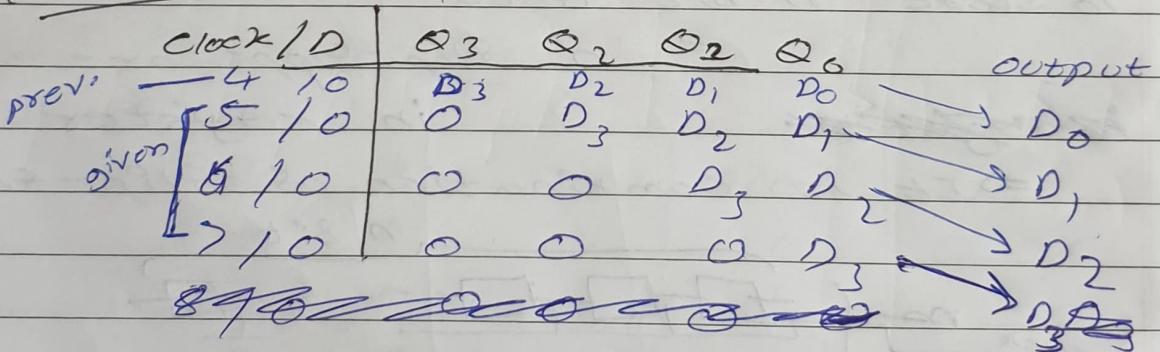
\* Shift register  $\Rightarrow$

- |                   |                         |         |
|-------------------|-------------------------|---------|
| Based<br>on input | 1) Serial in serial out | (SISI)  |
|                   | 2) " " Parallel "       | (SIPSI) |
|                   | 3) Parallel in serial " | (PISI)  |
|                   | 4) " " Parallel "       | (PIPO)  |

(4 bit<sup>st</sup>)

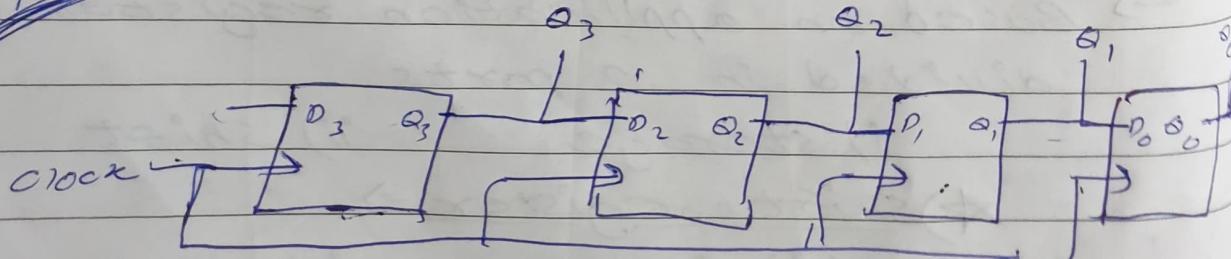
{ Note: To store n bit data }  
n pulse seq.

serial  
(output)



{ Note: To out n bit data }  
(n-1) pulse seq

~~A) SIPO~~



Control  
Signal

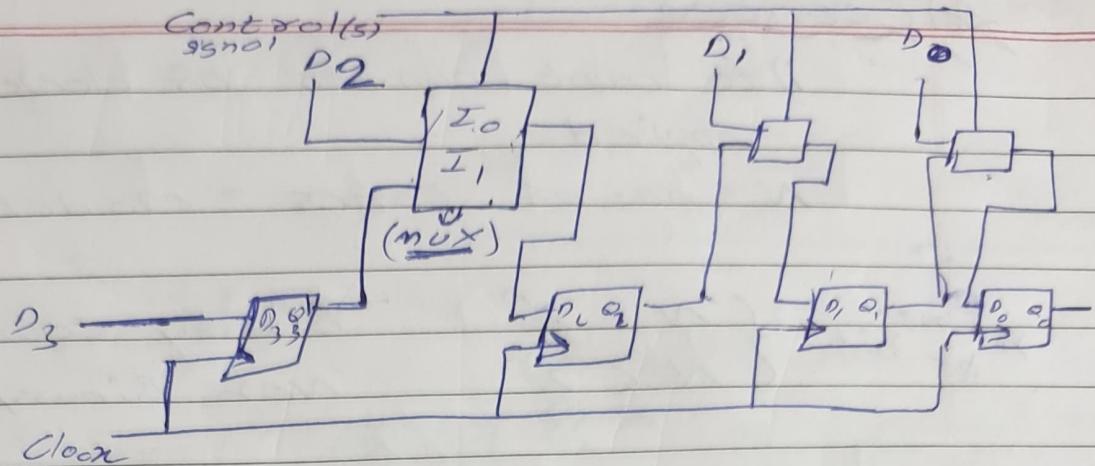
0 → Data // In

1 → Data Serial Out

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★) PISO



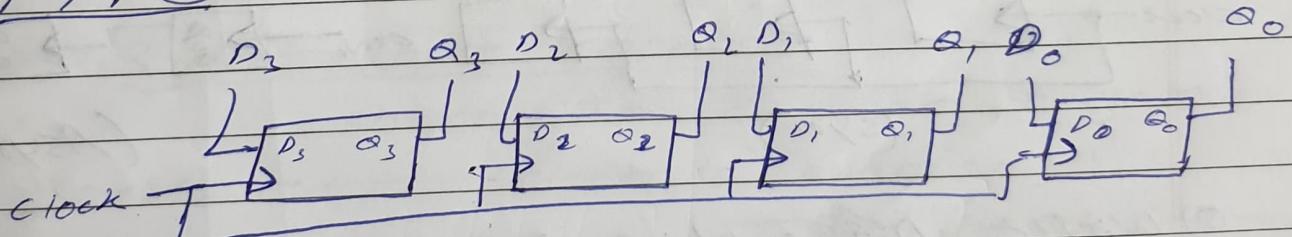
Control / Clock 10  
Signal

1/0/03  
0/1/10  
0/2/10  
0/3/0

$Q_3$	$Q_2$	$Q_1$	$Q_0$
$D_3$	$D_2$	$D_1$	$D_0$
0	$D_3$	$D_2$	$D_1$
0	0	$D_3$	$D_2$
0	0	0	$D_3$

(Rog = 3 pulses)

★) PIPO



## A) Counted

- i) to count number of clock pulses applied

$$N = \text{no. of states} = \text{modulus}$$

$$n = \begin{cases} \text{no. of bits} & N = 2^n \\ & N < 2^n \end{cases}$$

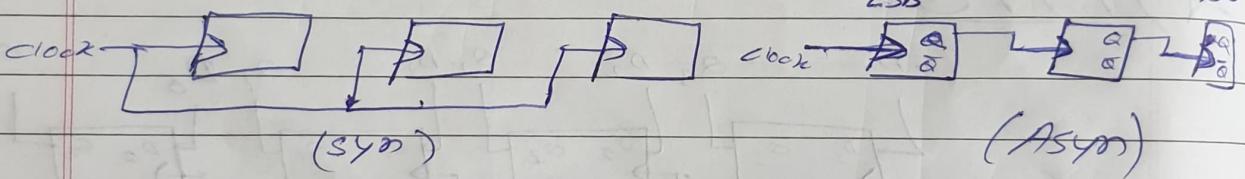
Binary Counters  
Non Binary "

### Asynchronous

- used JK ~~AT~~
- outputs =  $Q$  &  $\bar{Q}$
- $Q$  is used as clock for next bit on which clock is applied is LSB
- (slow) Bit on which clock is applied is next
- ↳ as wait for prev. output

### Synchronous

- used D
- same clock is applied

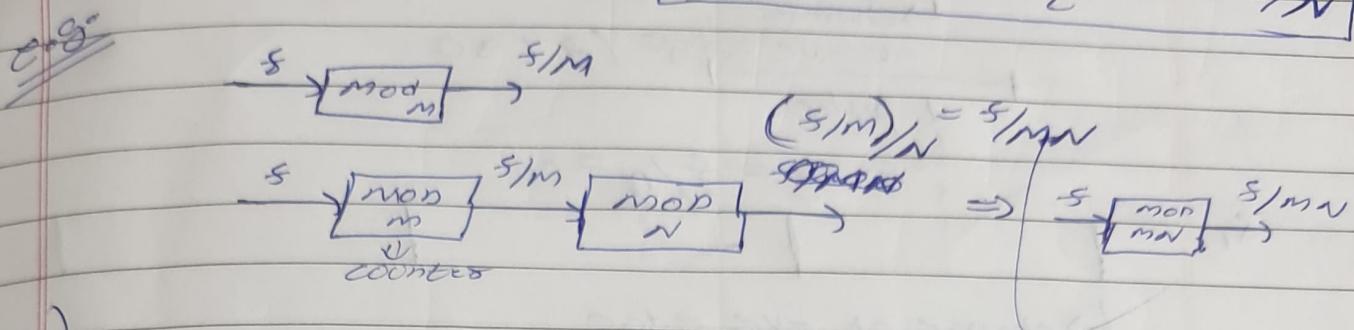


- Q) Write differences b/w synchronous & asynchronous counters

- | <u>Syn</u>                                    | <u>Asyn</u>                                   |
|---|---|
| i) All flip flops are applied with same clock | Diffs. flip flops have diff. clocks           |
| ii) Faster                                    | slower  |
| iii) can be designed for any count sequence   | Only fixed count seq. is possible (up & down) |
| iv) No decoding error                         | Decoding error due to propagation delay       |

L → unused states  
Q8 for  $N=5$   
 USC 3 bit  $2^3$   
 unused (0000)  
 ↓  
 000  
 001  
 010  
 011  
 100  
 101  
 110  
 111  
 ↓  
 3 for 5 it should  
 reset to 2020  
 aster 65

Clock frequency of mod-N counters  
 is ' $s$ ' then, [output freq] =  $s/N$



~~Q8~~ Counters  $\Rightarrow$  Frequency divider circ.

$\Rightarrow$  Frequency measurement  
 $\Rightarrow$  Pulse width "  
 $\Rightarrow$  Time "

## \* Ripple Counter (Asynchronous Counter)

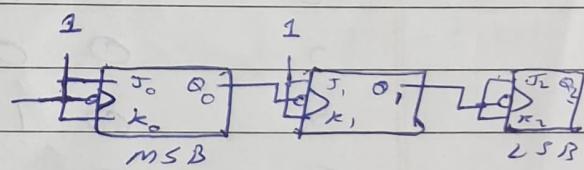
$\Rightarrow$  3 bit Ripple counter

short JK  $\Rightarrow$  make toggle

-Vc edge (clock is bubbled)

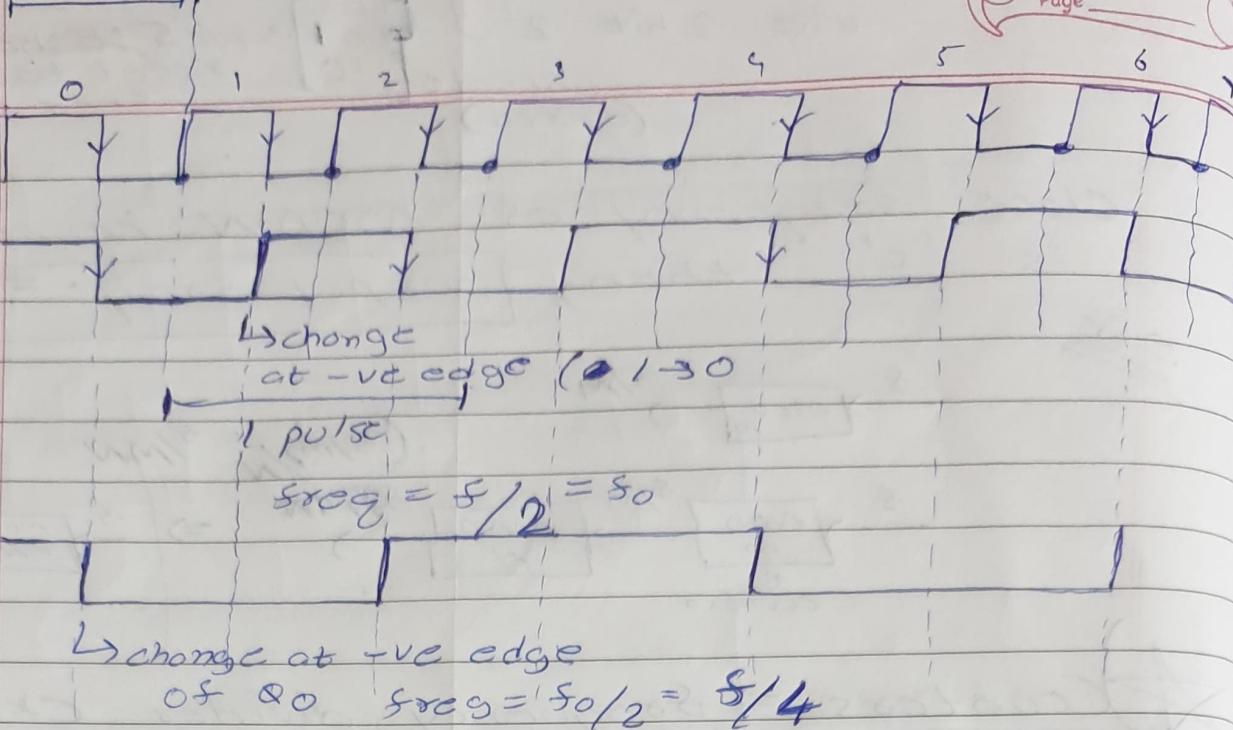
(will change in -Vc edge)  $\rightarrow$  (no ~~edge~~  $\Rightarrow$  change state)

Clock	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

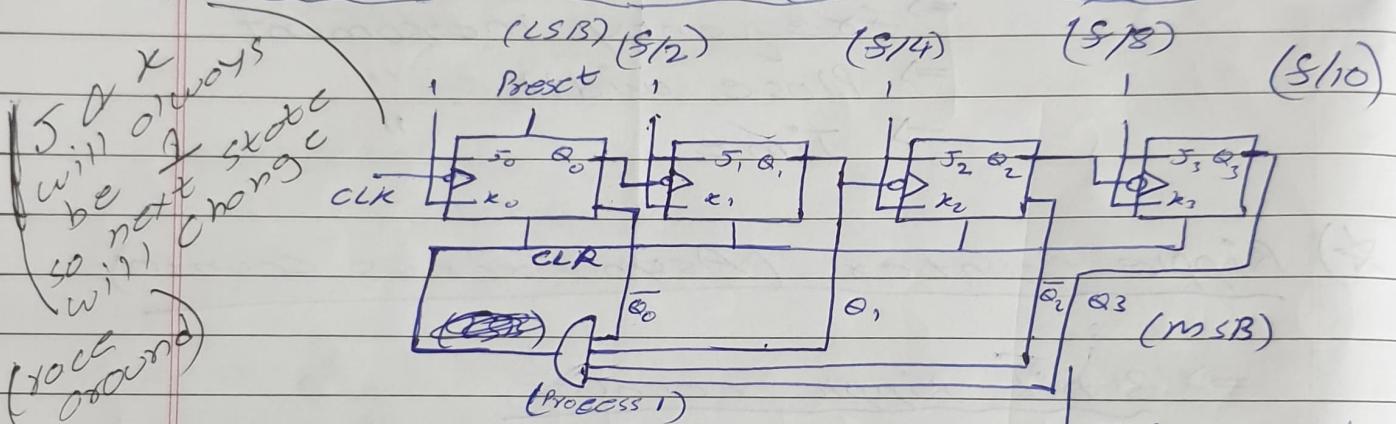


MSB will  
change  
in every  
run

$$1 \text{ pulse} \Rightarrow S_{seq} = 5$$



### ★) Decade Counter (Mod-10) (BCD counter)



CLK	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0

IS previous state  
 $\rightarrow 0$

change next

$Q_0$  will change every time  
(race around)  
but initially all are zero

$\Rightarrow (\text{max}) \text{ Resetz at } 10$   
(Process 1)  
 $Q_0 Q_1 Q_2 Q_3$   
 $S_{seq}$

expected using  $\text{resetz}$ )

Process!

to reset 1010 ( $'010$  to  $0000$ )  
 using ckt.

$$Q_3 \bar{Q}_2 Q_1 \bar{Q}_0$$

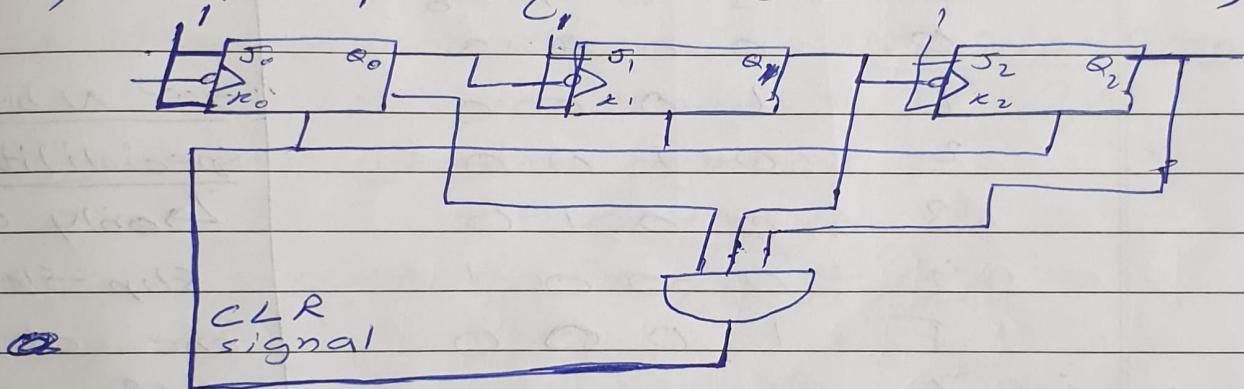
↓

1111

~~connected step~~ This will give  
~~and~~ sum of all 4 bits  
 $0000 = 1$   
 (seq. to activate  
 CLR signal to reset)  
 $011$  slip stop

\* ) (MOD-6) Asynchronous Counter

• 3 slip-stop seq. (reset at 6)



CLK	$Q_2$	$Q_1$	$Q_0$	Change next at $1 \rightarrow 0$
0	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	$\Rightarrow$ max
6	1	1	0	

Fit clk  
 0 result  
 should  
 be zero

Ckt. will be

$$\text{at } 6 \Rightarrow \begin{matrix} Q_2 & Q_1 & Q_0 \\ 1 & 1 & 0 \end{matrix}$$

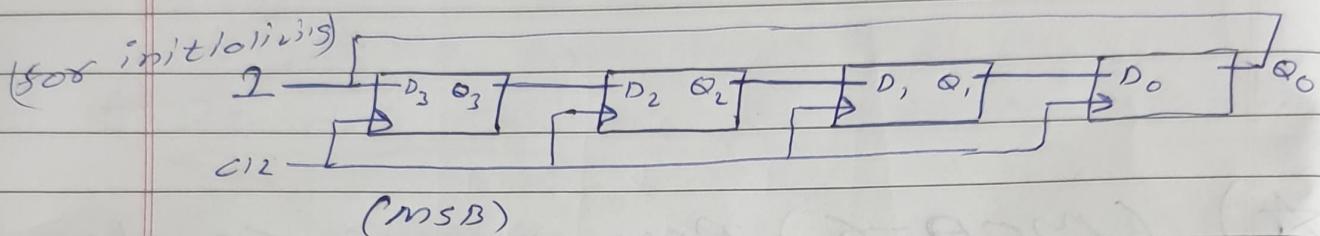
$$\text{ckt.} = Q_2 Q_1 \bar{Q}_0$$

## ★) Synchronous Counter

### i) Ring Counter

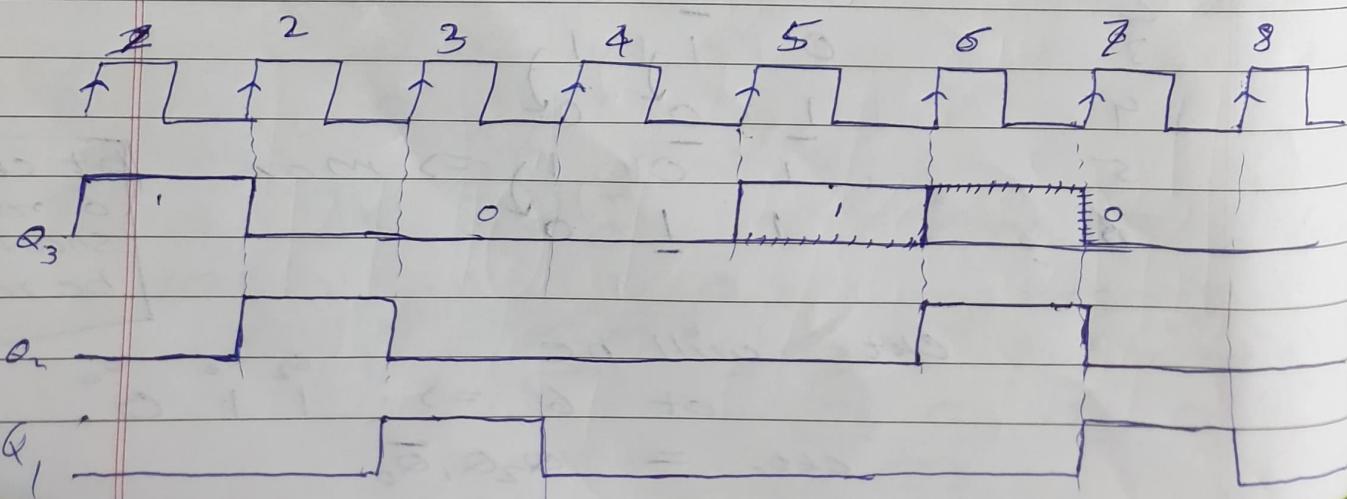
a) 4-bit

⇒ using SISO shift register  
⇒ 4 slip-slop



CLK	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0
7	0	0	1	0
8	0	0	0	1
9	0	0	0	0

for n bits  
speciality  
↳ only one  
slip-slop is  
one at a  
time



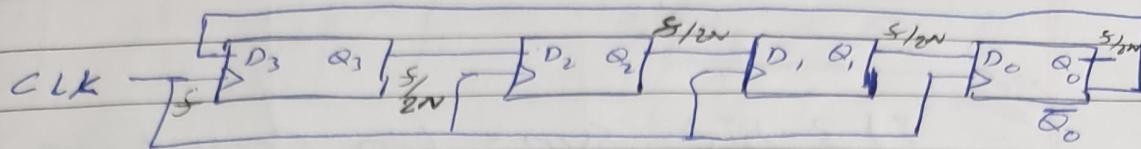
(max. used state =  $2^N$   
used state =  $2^N - 2^N$ )

classmate

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### A) Johnson Counter



CLK       $Q_3 \quad Q_2 \quad Q_1 \quad Q_0$

0            0    0    0    0

1            1    0    0    0

$$\bar{Q}_0 = 1$$

2            1    1    0    0

"

3            1    1    1    0

"

4            1    1    1    1

"

$$Q_0 = 1$$

5            0    1    1    1

$$\bar{Q}_0 = 0$$

6            0    0    1    1

7            0    0    1    1

8            0    0    0    0

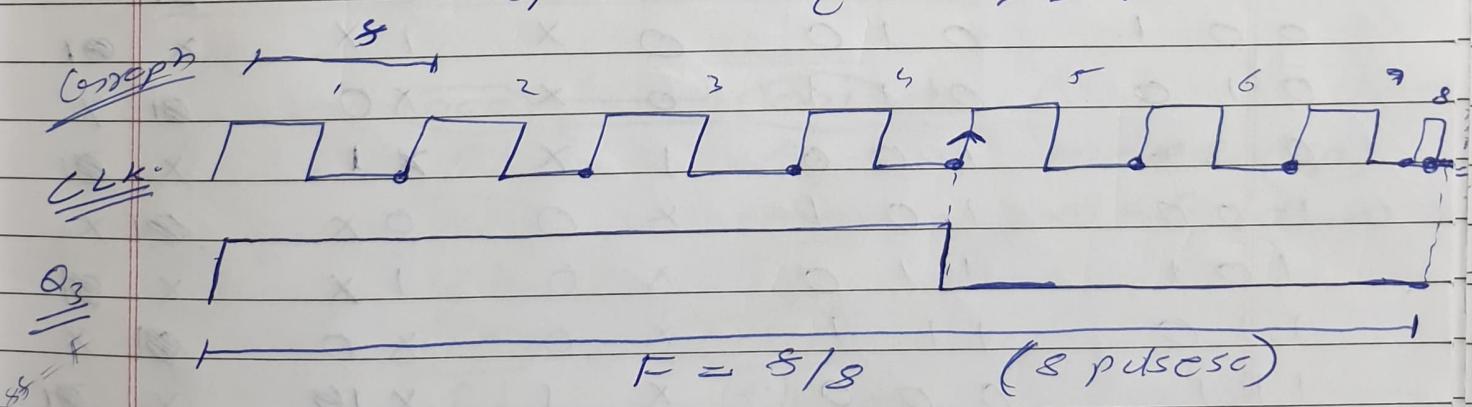
$\Rightarrow$  (reset)

$\Rightarrow$  In Johnson counter with N slip-slop  
max. possible state = ~~2~~  $2^N$

$\Rightarrow$  In normal Johnson counter

is  $S = \text{CLK } \text{S} \text{eq}$

output  $S \text{eq} = S/2^N$



up  $\rightarrow$  000  $\rightarrow$  001  $\rightarrow$  010  $\dots$   
 down  $\rightarrow$  000  $\rightarrow$  111  $\rightarrow$  110  $\dots$  001

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## A) Designing of syn. Counter

Q. 9

### i) 3-bit syn. Up Counter

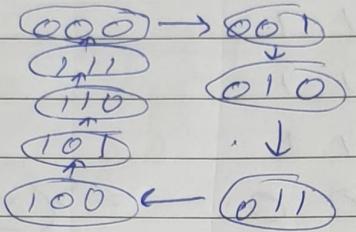
B) in up-counting

000  $\rightarrow$  001  $\rightarrow$  010  $\rightarrow$  011  $\rightarrow \dots \rightarrow$  111



(cycle)  $\dots \rightarrow 010 \leftarrow 001 \leftarrow 000$

state  
dig



excitation table of given FF

Prev State	Next State	J <sub>2</sub>	J <sub>1</sub>	J <sub>0</sub>	K <sub>2</sub>	K <sub>1</sub>	K <sub>0</sub>
Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>						
0 0 0	0 0 1	0	X	0 X	0 1 X		
0 0 1	0 1 0	0	X	1 X	X 0 1		
0 1 0	0 1 1	0	X	X 0	0 1 X		
0 1 1	1 0 0	1	X	X 1	X 0 1		
1 0 0	1 0 1	X 0	0 X	0 1 X	0 0 1 X		
1 0 1	1 1 0	X 0	1 X	X 0 1	X 0 0 1		
1 1 0	1 1 1	X 0	X 0	X 0	0 1 X		
1 1 1	0 0 0	X 1	X 1 0	X 1 0	X 0 1		

~~J<sub>2</sub>~~

Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	J <sub>2</sub>	J <sub>1</sub>	J <sub>0</sub>
0	0	0	0	0	0
1	X	X	X	X	X

PIC to  
prev.  
state

$$J_2 = Q_1 Q_0$$

0 1 0  
1 1 0  
0 1

$Q_2$	00	01	11	10
*	X	(X)	X	X

$$\boxed{J_2 = Q_1 Q_0}$$

classmate

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$Q_2$	00	01	11	10
0	1	X	X	X
1	1	X	X	X

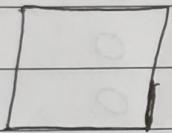
$$\boxed{J_1 = Q_0}$$

$Q_2$	00	01	11	10
X	X	X	X	X
X	X	X	X	X

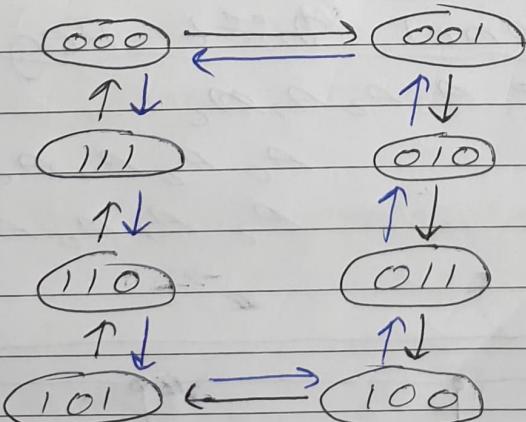
$$\boxed{J_0 = Q_0}$$

$Q_2$	00	01	11	10
0	1	X	X	1
1	1	X	X	1

100s bit 2's complement down count



\* 3 bit up & down counter



$m = 1$  (up)

$m = 0$  (down)

$Q_2 Q_1 Q_0$	$D_1$	$Q_2 Q_1 Q_0$	$J_2 J_1 J_0$
0 0 0	0	1 1 1	1 X
0 0 0	1	0 0 1	0 X
0 0 1	0	0 0 0	0 X
0 0 1	1	0 1 0	0 X
0 1 0	0	0 0 1	0 X
0 1 0	1	0 1 1	0 X
0 1 1	0	0 1 0	1 X
0 1 1	1	1 0 0	X 1
1 0 0	0	0 1 1	X 0
1 0 0	1	1 0 1	X 0
1 0 1	0	1 0 0	X 0
1 0 1	1	1 1 0	X 0
1 1 0	0	1 0 1	X 0
1 1 0	1	1 1 1	X 0
1 1 1	0	1 1 0	
1 1 1	1	0 0 0	

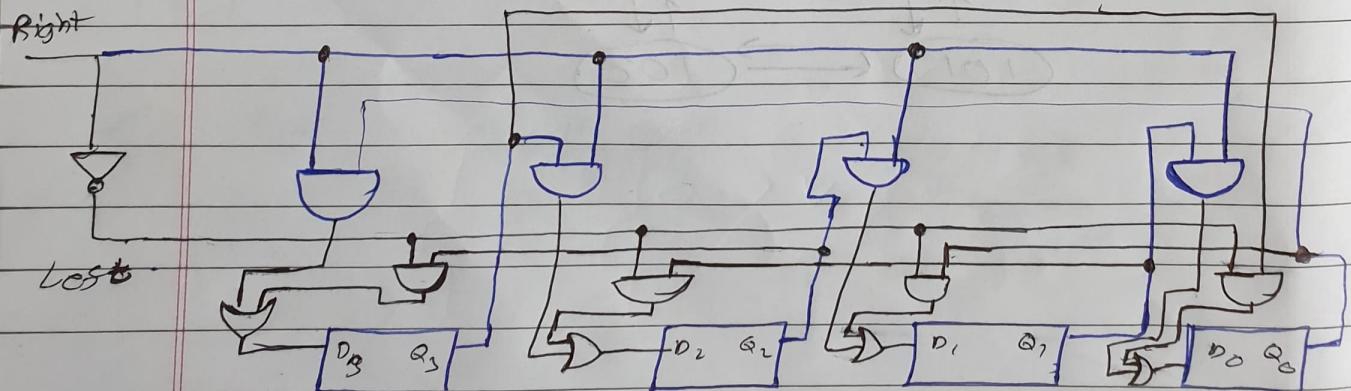
A) Bi-Directional Shift Register  $\Rightarrow$

$$D = D_3 D_2 D_1 D_0$$

Shift Right  
" Lost

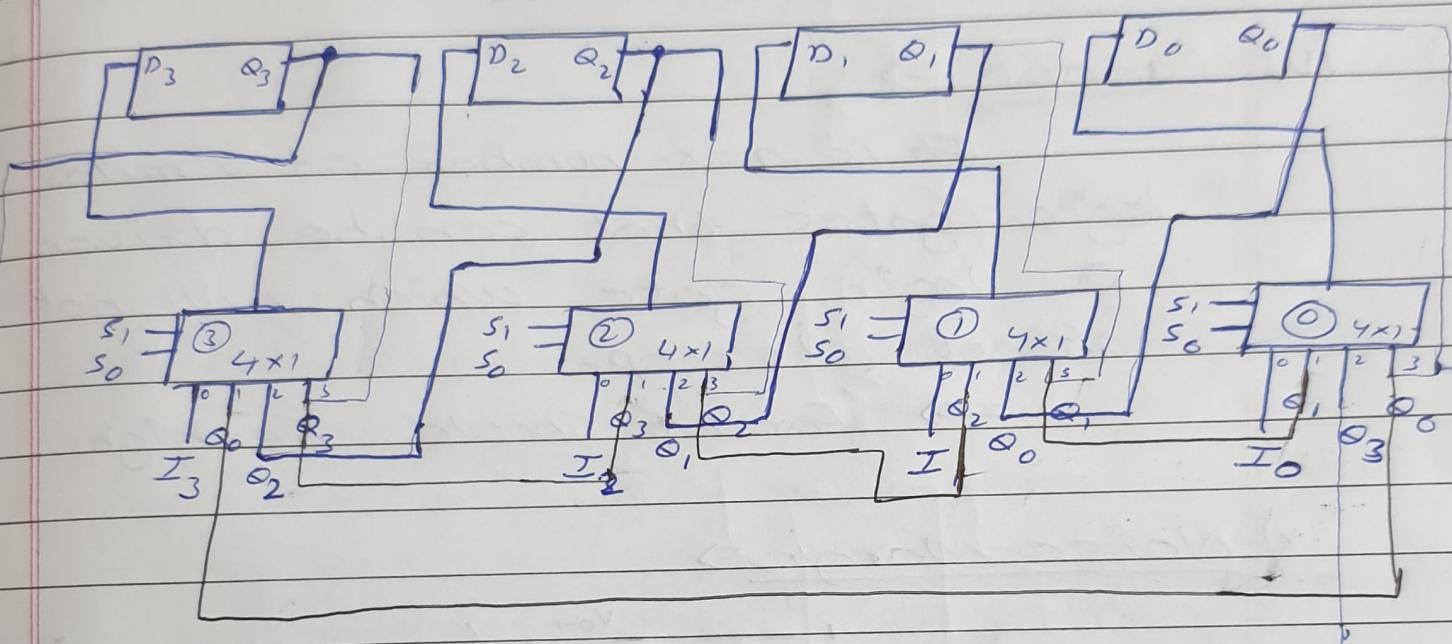
$D_0 D_2 D_1 D_0$   
 $D_2 D_1 D_0 D_3$

(Circular shift right)



### i) 4-bit Universal Shift register

	$S_1$	$S_0$	OP
0	0	0	no change
1	0	1	right shift
2	1	0	left shift
3	1	1	parallel load

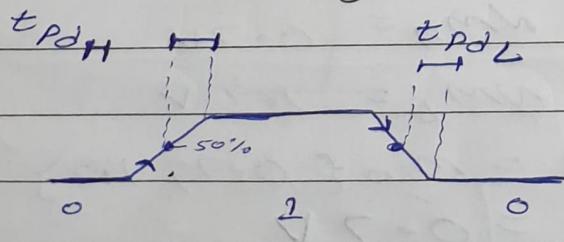


### A) Logic Families

i) ~~Characteristics of logic families~~

i) Propagation delay :- (speed of)

measured  
in  
nanosec



delay was  
started  
to be  
counted  
at 50%

$t_{PDH}$  = Propagation delay for high

$t_{PDL}$  = " " " low

$$t_{PDH} > t_{PDL} \quad (\text{they are not equal})$$

$$t_{PD} = \frac{t_{PDH} + t_{PDL}}{2}$$

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ii) Power dissipation per logic gate  $\Rightarrow$

$$P_{diss} = V_{CC} \times I_{C_{avg}}$$

[measured in milliwatt (mW)]

iii) Figure of merit :

(Speed product power product)

$$F = t_{PD} \times P_{diss}$$

PicoJoule (PJ)

iv) Fan-out  $\Rightarrow$

$F_b$  is max. number of similar logic gates that can be driven by a logic gate which will not affect its op.

$\Rightarrow$  Fanout should be high

v) Noise Margin  $\Rightarrow$

$$\begin{array}{c} V_{OH} \\ \hline V_{IL} - I \\ \hline V_{OL} \end{array} = V_{IH} \Rightarrow (NM_H = V_{OH} - V_{IH})$$

$$(NM_L = V_{IL} - V_{OL})$$

$$\text{Noise Margin} = \min \{ NM_H \text{ and } NM_L \}$$

eg:

$$V_{OH} = 3.8V$$

$$V_{IL} = 2V$$

$$V_{IH} = 3.1V$$

$$V_{OL} = 0.7V$$

$$NM_H = 0.7V$$

$$NM_L = 1.3V$$

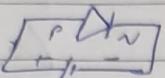
$$\begin{aligned} NM &= \min \{ 0.7, 1.3 \} \\ &= 0.7V \end{aligned}$$

## Note: PN Junction Diode

$S_i = 0.07V$  } x KNEE Voltage  
 $V_{OC} = 0.2V$  } threshold "

classmate  
Date \_\_\_\_\_  
Page \_\_\_\_\_

### Forward Biased

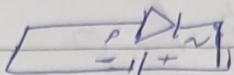


$$\frac{dV_{DS}}{dI_{DS}} \Rightarrow (P > N)$$

$$R = 0$$

(closed circuit)

### Reverse Biased



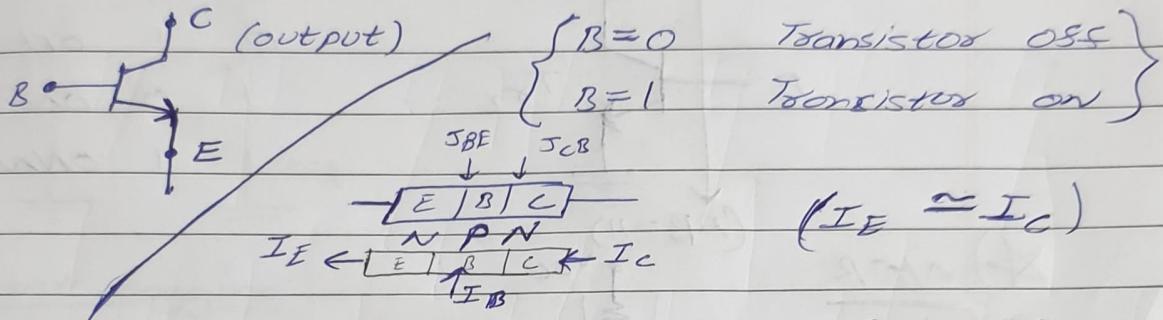
$$(P < N)$$

$$R = \infty$$

$$I_R = 0$$

(open circuit)

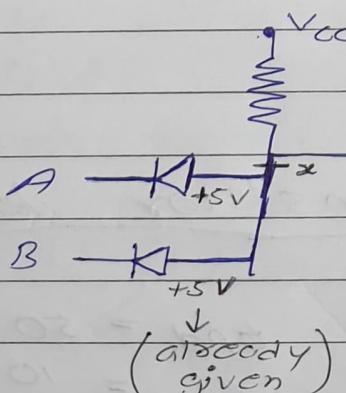
## Note: collector-emitter



## Implementation of AND gate using Diode

$JEB$	$JCB$	<u>Operation</u>
$F_B$	$R_B$	Active mode ) ON
$F_B$	$F_B$	Saturation ) OFF
$R_B$	$R_B$	Cut off ) OFF
$R_B$	$F_B$	Rev. active mode ) ON

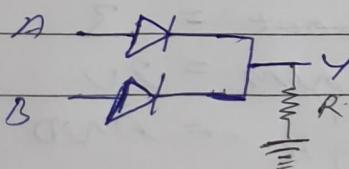
## \* Implementation of AND gate using Diode



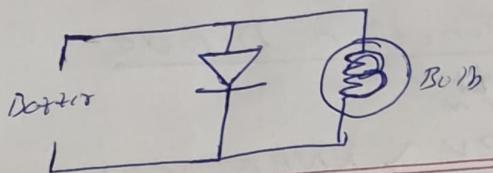
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

will go to output to A and B  
any one is active  
will

## \* AND



A	B	Y
0	0	0 → no current
0	1	[any one will be active]
1	0	[any one will be active]
1	1	1

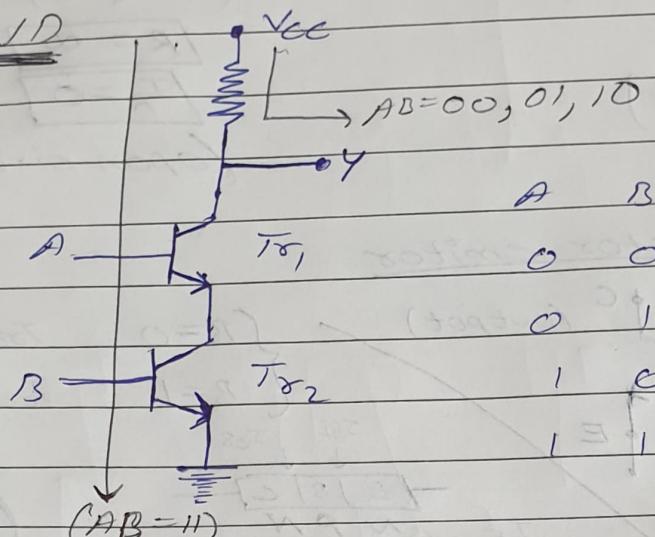


(4)

Date \_\_\_\_\_  
Page \_\_\_\_\_\*) NOT  $\Rightarrow$ 

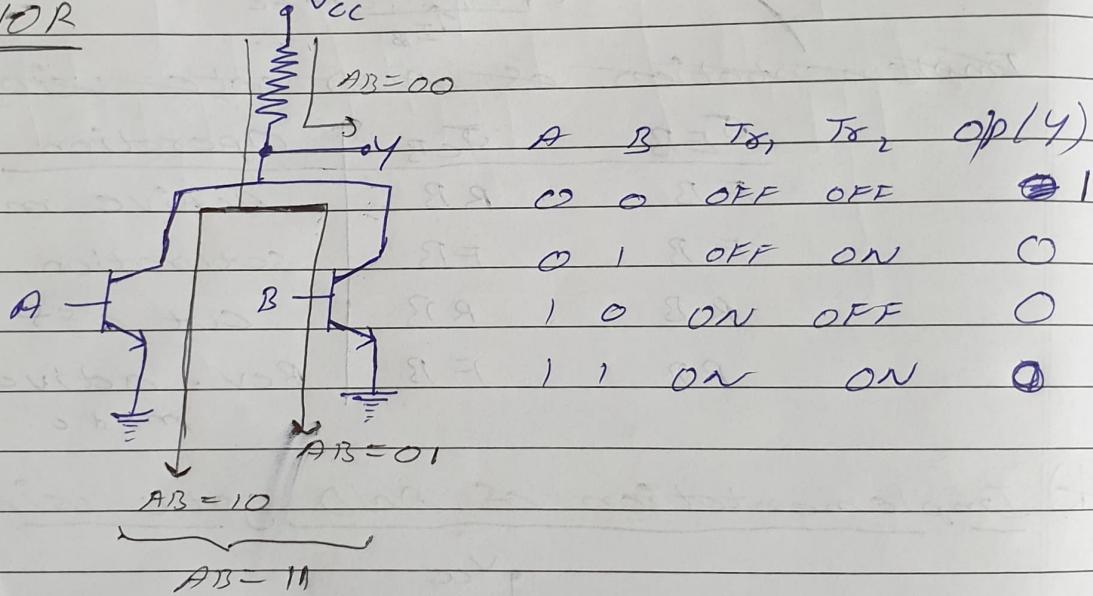
Battery	A	Diode	-Y
on	0	0	1
off	1	1	0
			(short) (open)

\*) NAND

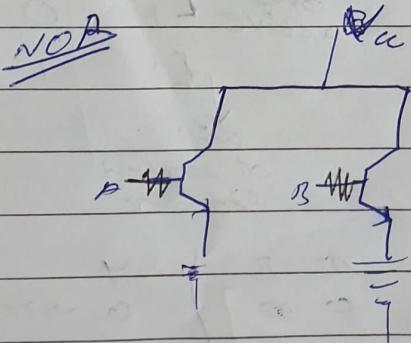


A	B	Tr <sub>1</sub> , Tr <sub>2</sub>	Y
0	0	OFF OFF	1
0	1	OFF ON	1
1	0	ON OFF	1
1	1	ON ON	0

\*) NOR



A	B	Tr <sub>1</sub> , Tr <sub>2</sub>	Op(Y)
0	0	OFF OFF	1
0	1	OFF ON	0
1	0	ON OFF	0
1	1	ON ON	0

\*) Registered transistor logic  $\Rightarrow$ 

$$t_{PD} = 50 \text{ nscc}$$

$$P_{diss} = 10 \text{ mW}$$

$$FOM = 500 \text{ pJ}$$

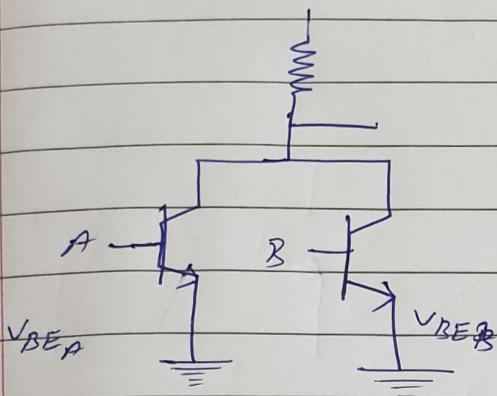
$$Fan-out = 3$$

$$V_{DM} = 2V$$

$$\text{word log ic} = \text{AND}$$

~~Disadvantage~~

- i) lower field of operation
- ii) lower fan-out
- iii) lower noise margin

~~DCTL (Direct couple transistor logic)~~

$$t_{PD} = 40 \text{ nsec}$$

Current hogging

is ( $V_{BEA} = V_{BE_B}$ )

Both on at same

if ( $V_{BE_A} > V_{BE_B}$ )

(A gets on)  
first

(current will go  
through A to Gnd)

is ( $V_{BE_B} > V_{BE_A}$ )

(some for B)

Disadvantage=> current hogging

Both transistors not exactly

same the which have lower  $V_{BE}$  get

on first & does not allow other

transistor to get on