① 08/04/2022 , 9:30 AM

② Exam Roll No. 21234757061

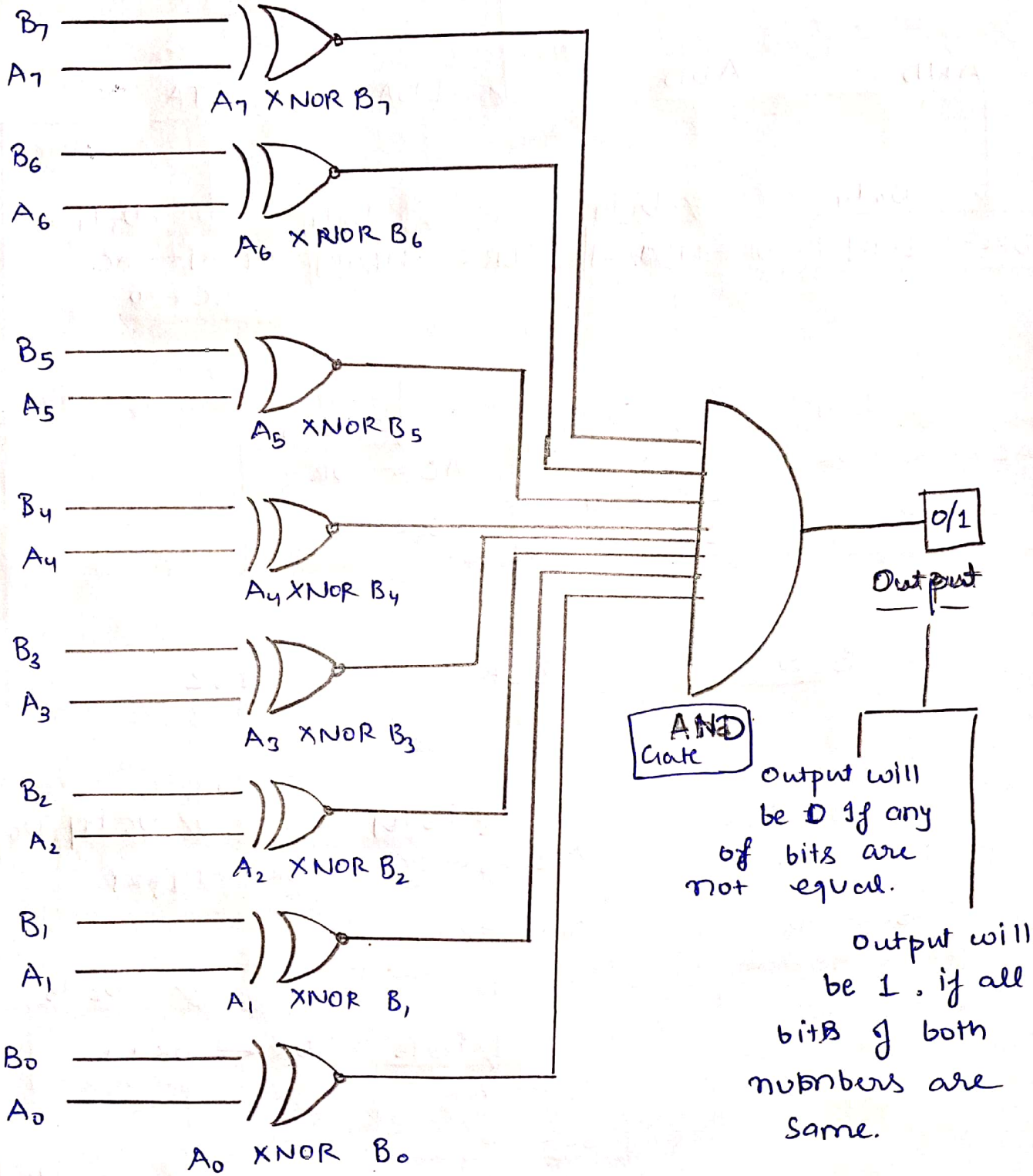
③ MCA

④ Sem-I/ Year-I

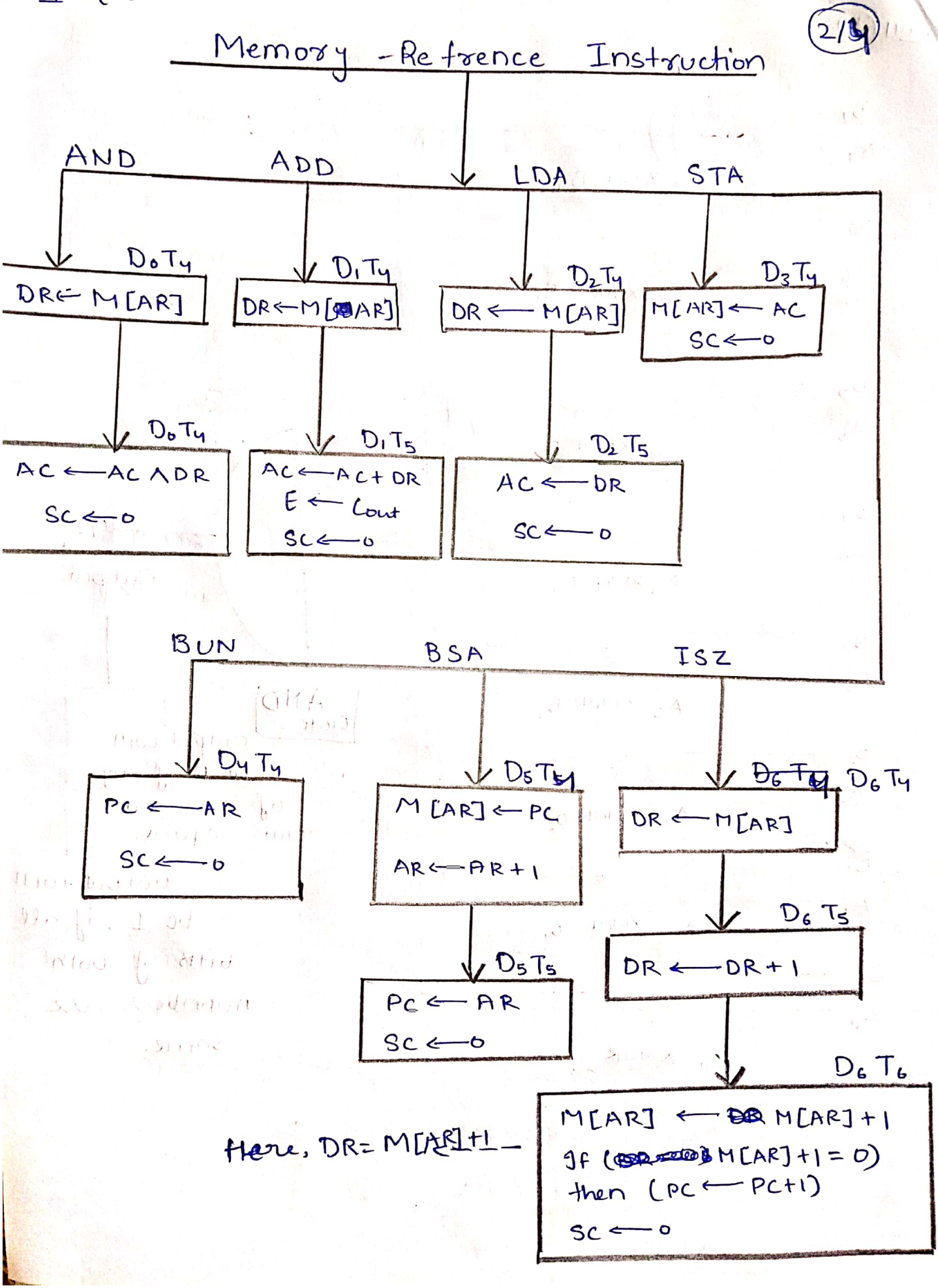
⑤ UPC: 223401104

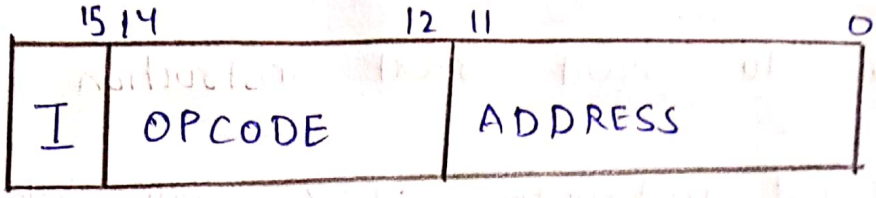
⑥ Computer System Architecture

Ans 1 (b)



Ans 1(A) Flow Chart for Memory Reference Inst.





(Opcode = 000 through 110)

Memory reference instruction.

In above flow chart of memory refrence instruction, control functions are indicated on top of each box.

The microoperation that are performed during time T_4, T_5, T_6 depends on opcode value.

After decoding the instruction, there will be seven (D_i where $i = 0, 1, 2, \ldots, 6$) decoded output from the operation decoder.

Two microoperations that are performed during time signal T_4, T_5, T_6

All the microoperations are indicated by six different paths in the flowchart.

The sequence counter SC is cleared to 0 with the last timing signal in each care.

This cause a transfer of control to timing signal T_0 to start next instruction cycle.

The longest instruction ISZ will take seven timing signals whereas smallest instruction STA will only take 5 timing signal.

The effective address of instruction is in AR and was placed during timing signal T_2 when I=0 or during T_3 when I=1.

Execution of instruction starts with timing signal T_4.

Symbol	Operation Decoder	Symbolic Description
AND	D_0	AC ← AC ∧ M[AR]
ADD	D_1	AC ← AC + M[AR], E ← Cout
LDA	D_2	AC ← M[AR]
STA	D_3	M[AR] ← AC
BUN	D_4	PC ← AR
BSA	D_5	M[AR] ← PC, PC ← AR + 1
ISZ	D_6	M[AR] ← M[AR] + 1, If M[AR] + 1 = 0 then PC ← PC + 1