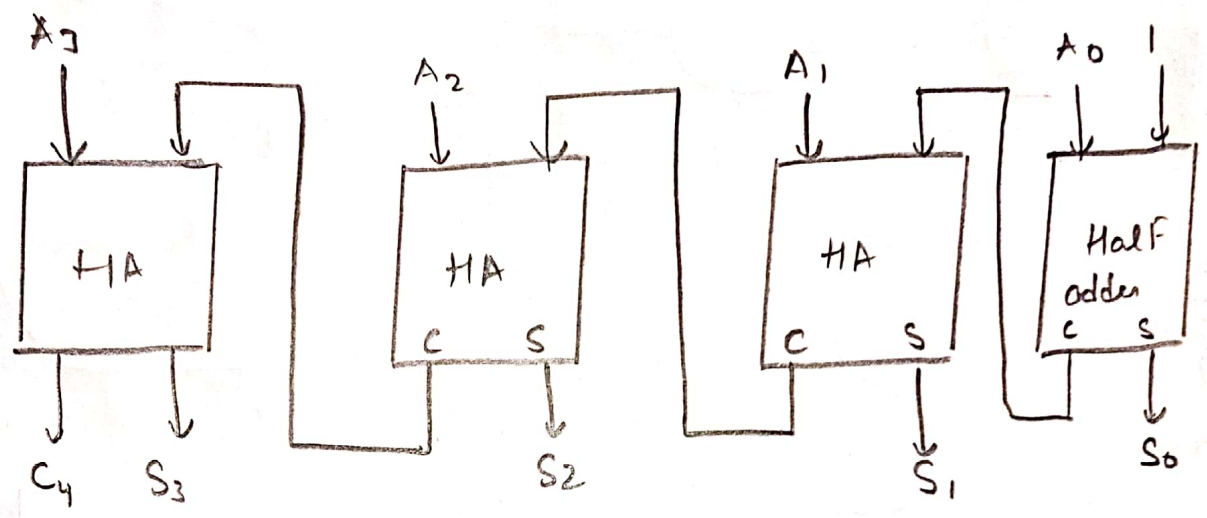


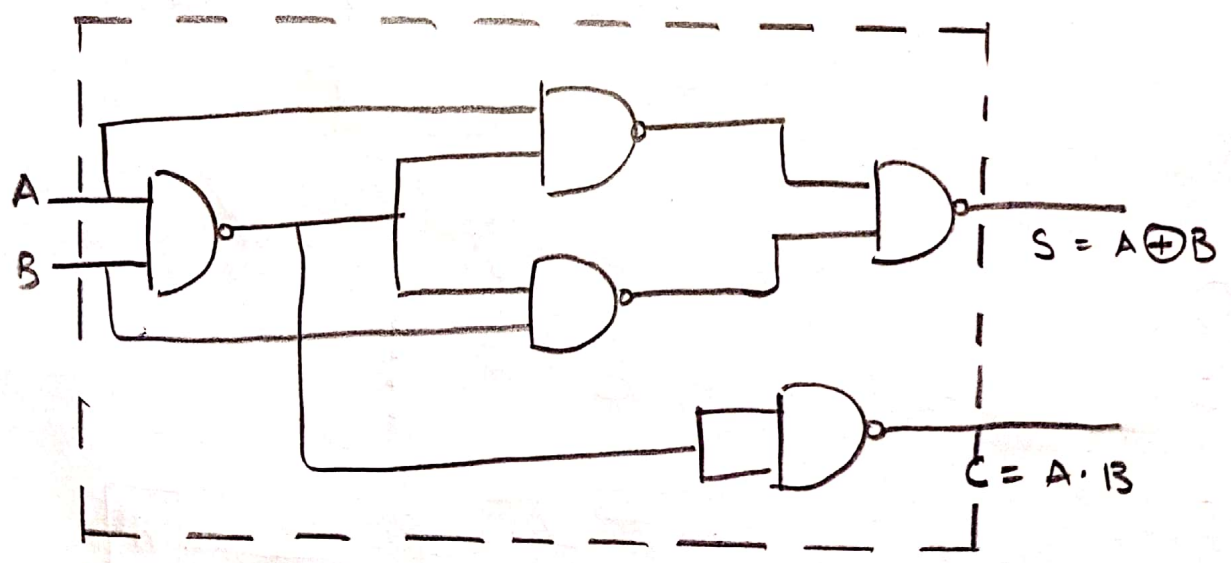
- ① 08/04/2022 , 9:30 AM
- ② Exam Roll No. 21234757061
- ③ MCA
- ④ Sem-I / Year-I
- ⑤ UPC : 223401104
- ⑥ Computer System Architecture

Q 5(B) 4-Bit combinational circuit incrementer using NAND gates.

Binary Incrementer can be made with half adder like this

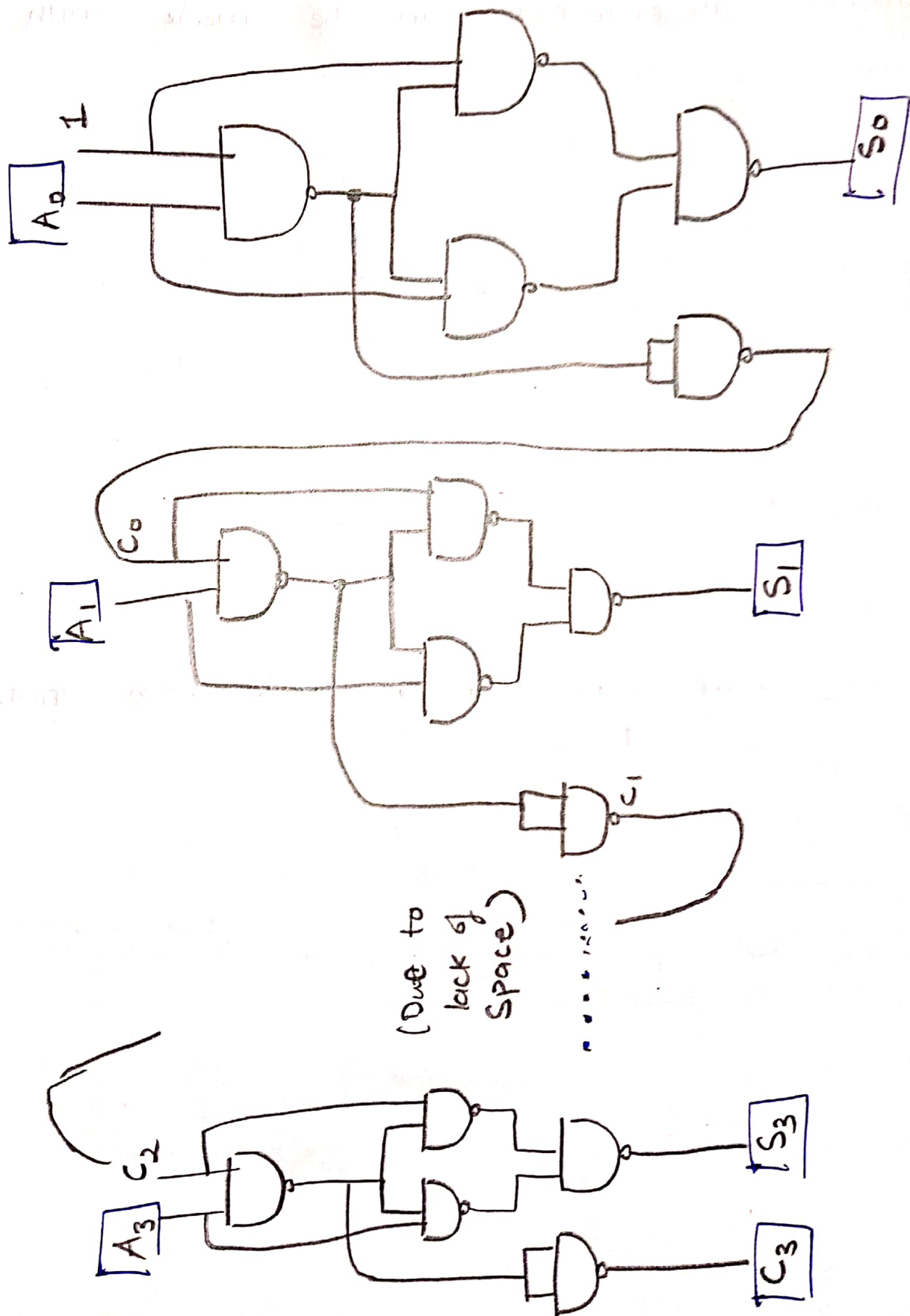


And Half adder can be made with NAND gate



Due to lack of space, I skipped HA-3 and cont. with (...)

118 4-bit binary shifter with nand gate is. (2/3)



Ans 5(a)

(i) 0 1 1 1 0 0 0 1 1 1

Worst case: 01 1100 0111

Best case: 01 11 00 01 11

In other case

~~In these case~~
This is the ~~worst~~^{best} case of booth' multi-
plication as the chunk of consecutive 1's &
0's are present in multipliers.

(ii) oiiiii

This is the worst case of Booth's multipliers as there is consecutive pair of 01 present in multiplier.

Worst case: 01 01 01 01 01

Worst case: 01 01 01 01 01

Beet case: Not possible.

0110011000

Worst ~~Best~~ case: 01 10 01 10 00

Best case : 0 11 00 11 00 0

(iv) 1111 00 1111

Worst case: 111 10 01 111

Best case: 1111 00 1111