MCA
MCAC-104: Computer Systems Architecture
Unique Paper Code: 223401104
Semester I
March-2022
Year of admission: 2021

Time: Three Hours **Max. Marks: 70**

Note: Answer any 4 questions. All questions carry equal marks.

1 (A) Design and Describe the flowchart for the memory reference instruction with timing signal.

1 (B) Design an 8-bit combinational circuit that compares two 8-bit numbers. The circuit produces output 1 if the numbers are equal and 0 otherwise.

2.(A) Design the overlapped register windows and also find out the total number of registers needed in overlapped RISC architecture where we have four windows with 30 registers in each. And we have 12 registers that are common to all procedures. The number of shared registers is twice than the local registers in each window.

2.(B) Match the following

i)	DMA	(A)	ALU
ii)	Cache	(B)	Printer
iii)	Interrupt I/O	(C)	Disk
		(D)	High Speed RAM

3.(A) Design a complete circuit for Accumulator Logic. Also show the circuit for load, increment and clear logic for Accumulator.

3 (B) Match the following

i)	Micro-programmed control unit	(A)	RISC Processor
ii)	Memory mapped I/O	(B)	More flexible I/O program
iii)	TRAP	(C)	Both edge & level triggered
		(D)	CISC Processor

4 (A) Evaluate the arithmetic statement in assembly language instruction

$$X = A + B[C * D + E(F + G)]$$

(A) Using three address instructions.
(B) Using two address instructions.
(C) Using one address instructions.
(D) Using zero address operation instructions.

Use the symbols *ADD* and *MUL* for arithmetic operations; *MOV* for the transfer-type operation; and *LOAD* and *STORE* for transfers to and from *AC* register and memory. Assume that memory operands are stored at memory addresses *A, B, C, D, E, F, G* and the result must be stored in memory at address *X*.

4 (B) Design an 8-bit combinational circuit shifter.

5.(A) Explain the best and worst case performance for Both's multiplication in respect to the given multiplier:

i) 0111000111 ii) 0101010101

iii) 0110011000 iv) 1111001111

5.(B) Design an 4-bit combinational circuit incrementer using NAND gates.

6.(A) Why are the read and write control lines in a DMA controller bidirectional? Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose are they used as outputs?

6.(B) Give a Boolean function for the match logic of one word in an associative memory taking into consideration a tag bit that indicates whether the word is active or inactive.

6.(C) Match the following

iv) SRAM	(E) Virtual memory
v) DRAM	(F) Matching logic
vi) DISK	(G) Record
vii) Associate Memory	(H) Refreshing
	(I) High Speed RAM