① 08/04/2022 , 9:30 AM

② Exam Roll No. 21234757061

③ MCA

④ Sem-I/ Year-I

⑤ UPC: 223401104

⑥ Computer System Architecture

Ans 3 (A) Completer circuit for accumulator logic

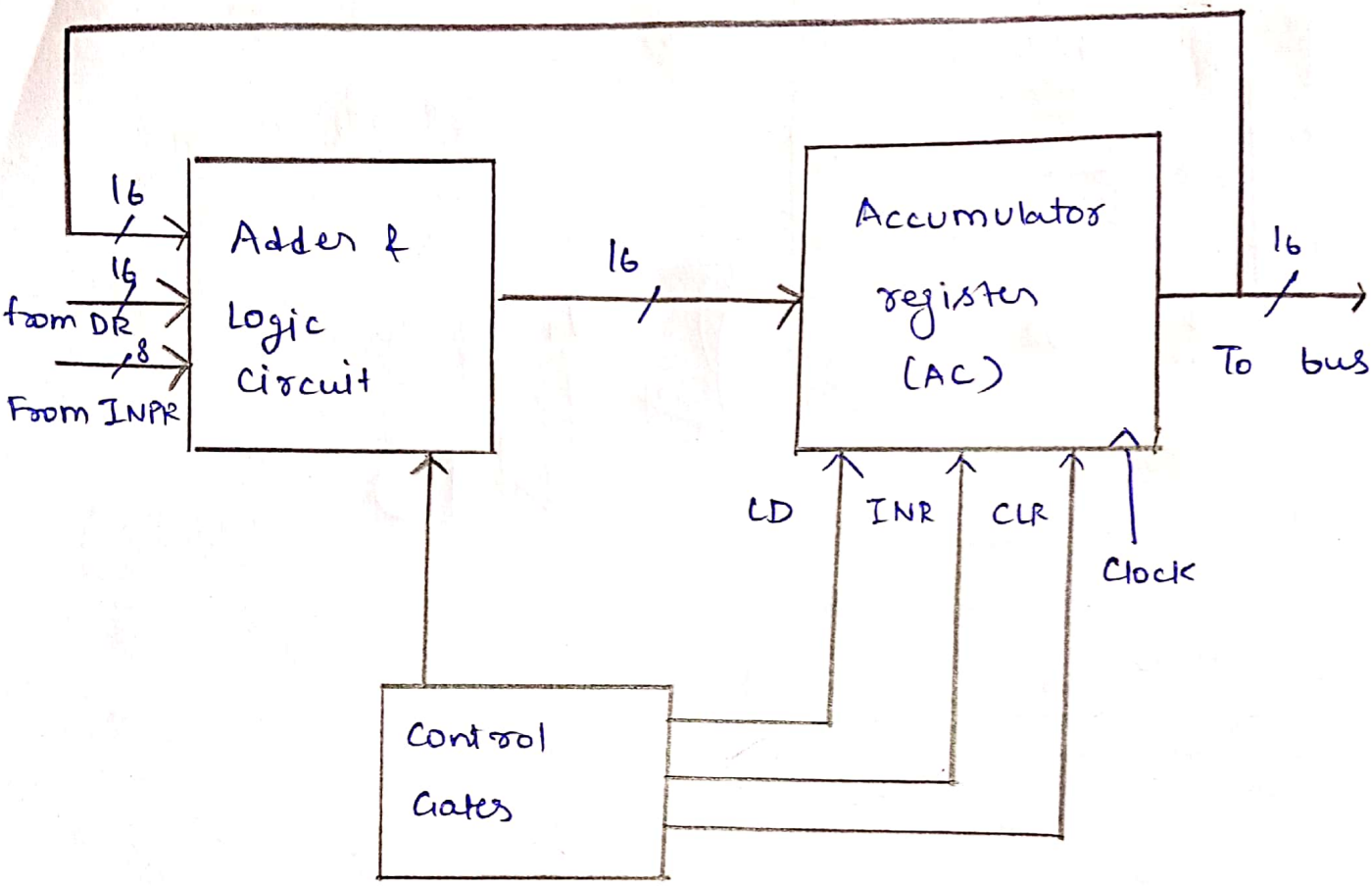
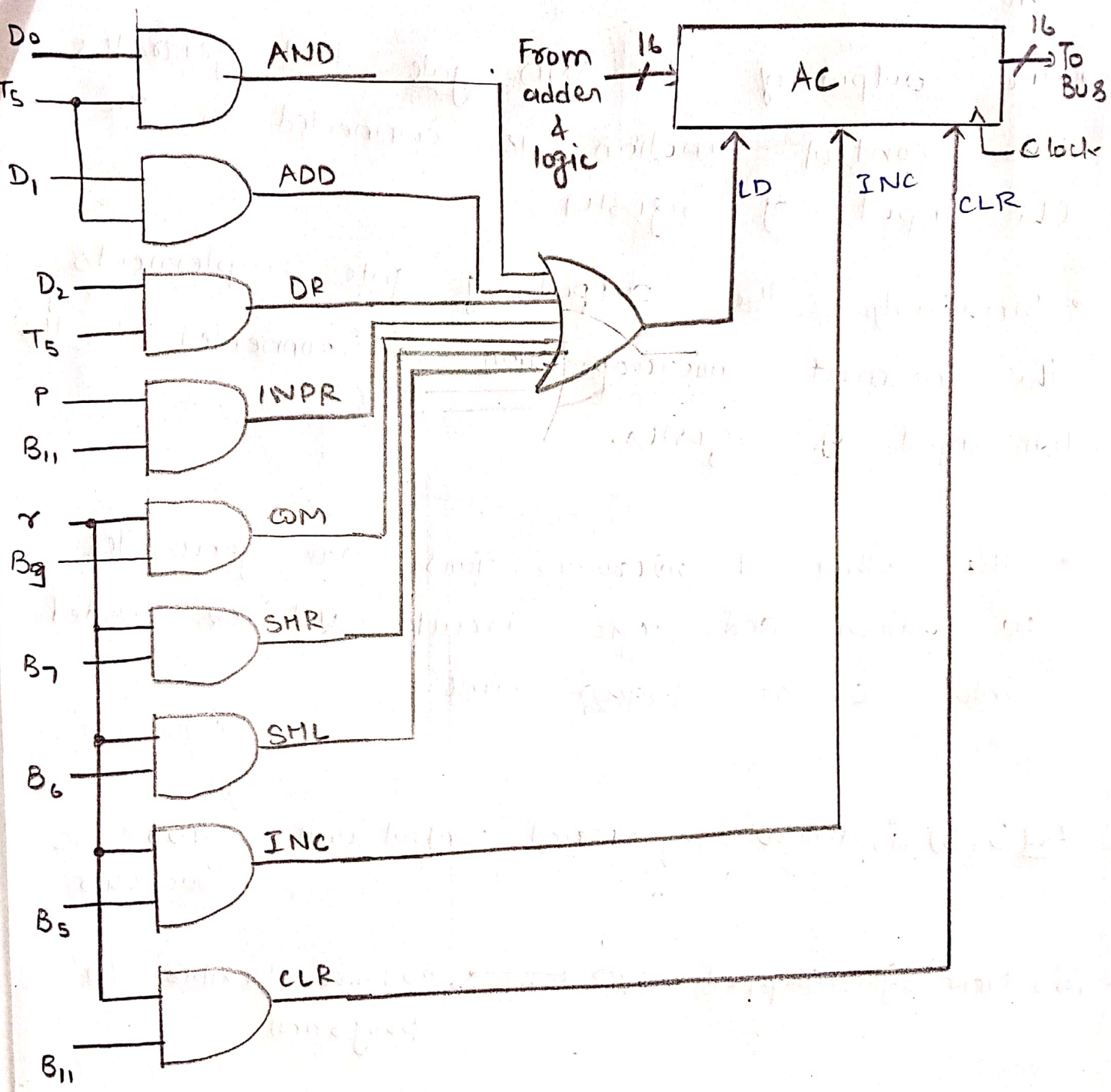


Fig. Circuits associate with AC

In above circuit, adder & logic circuit has three sets of inputs. One set of 16 input comes from output of AC. Another 16-input set comes from DR (data register). A third set comes from INPR (input register) of 8 inputs. Output of A & L circuit provide data input for register. It is necessary to include logic gates for controlling LD, ~~IRR~~ INR, and CLR in register & for controlling the operation of the adder and logic circuit.

circuit for load, increment and clear logic :-



- The control function for the clear micro-operation is rB_{11}, where $r = D7I'T3$ and $B_{11} = IR(11)$.
- The output of the AND gate that generates this control function is connected to the CLR input of register.
- Similiarly, the output of gate implements the increment microoperation is connected to the INP input of register.
- The other 7 microoperations are generated in adder and logic circuit and are loaded into AC at proper time.

Any 3 (B) (i) Micro-programmed control unit ⟷ (D) CISC Processor

(ii) Memory Mapped I/O ⟷ (B) More flexible I/O program

(iii) TRAP ⟷ (C) ~~TRAP~~ Both edge & level triggered.