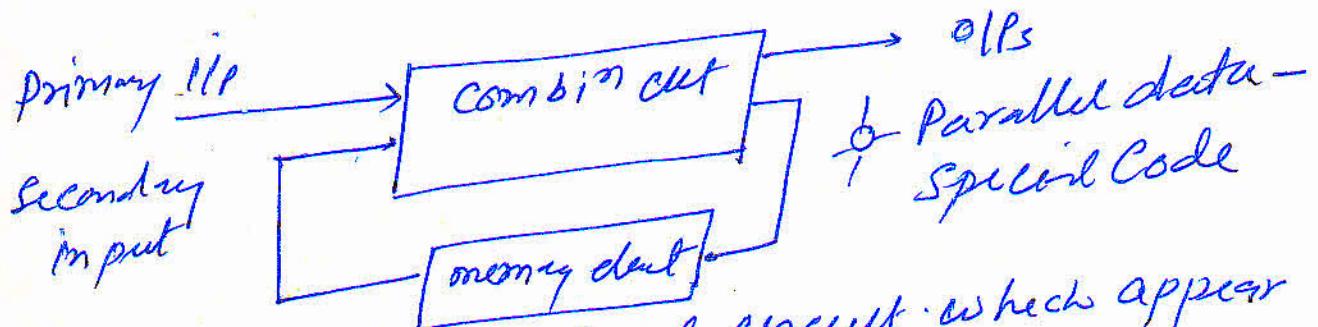


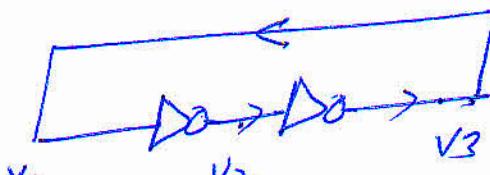
Sequential Circuit \Rightarrow in combinational ckt the O/P at any time depend only up on the present input at that time O/P don't depend up on past I/Ps. The past refer to time period greater than the propagation delay of the ckt. \Rightarrow serial data - temporal data



If some O/Ps of the Combinational circuit which appear after some time delay are fed back as input to combn ckt then it is called combn Sequential ckt. In fact a sequential ckt consist of combn ckt to which memory element are connected to form feedback path.

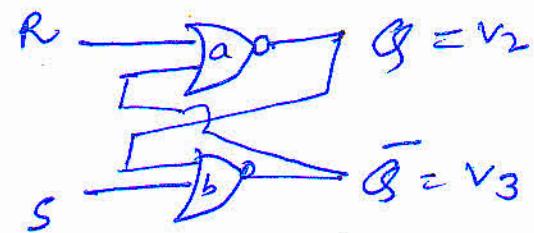
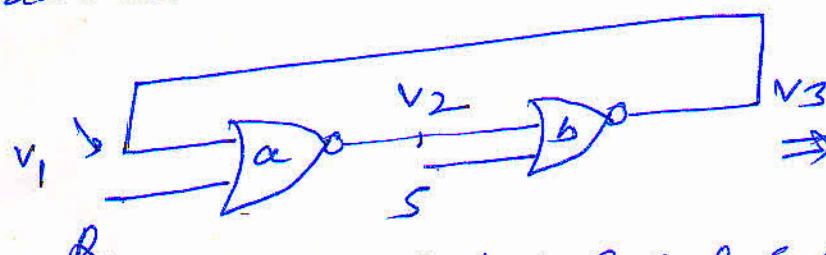
- * The memory element store binary information.
- * The information stored in memory element defines the state of the sequential circuit.
- * External Input (primary) together with the present state of memory element determines the output.
- \Rightarrow Sequential Circuit $\begin{cases} \rightarrow \text{Synchronous} \\ \rightarrow \text{Asynchronous} \end{cases}$
- * In Asynchronous ckt. Inputs and outputs do not change at preassigned times. Since the inherent delays are not rigidly controlled. This might lead to Instability (races). That's why these ckt are not common.

- ⇒ In Synchronous CLK - The behaviour can be defined from the knowledge of its signals at discrete instant of time. The synchronization is obtained by clock pulses.
- ⇒ The memory element used is clocked sequential CLK is called flip-flop (a binary cell capable of storing 1 bit of information). A flip flop has two output. one for normal values and one for complement of the bit stored in it
- ⇒ F/Fs are called latches, bistable MV or bimoris. Any device that has two stable state is said to be bistable i.e. Toggle switch has (two) stable state (open/closed). The switch said to have memory since it will remain as such until the position is changed.
- In fact any bistable device can be used to store 1 bit of information
- ⇒ one of the easiest way to construct flip flop is



- ⇒ If feedback is open $V_1 \rightarrow 0V$ (GND), V_3 is also at 0. Now if feedback is reconnected and ground removed from V_1 , both V_1 and V_3 will remain at 0V
- ⇒ Conversely if V_1 is set at +5V V_3 is also at +5V then feedback line is used to hold V_1 at +5V
- ⇒ This basic F/Fs can be improved by replacing inverts with either NAND or NOR gate.

The additional inputs on these gates provide convenient means for application of input signal to switch the flip flop from one stable state to another.



If two input labels R and S are ignored from the previous case we have the present case

R	S	\bar{Q}	last value
0	0	1	No change
0	1	0	Set
1	0	?	Reset
1	1	?	forbidden. violates compatibility

action. \Rightarrow logic at Any Input of NOR the O/P is

x	y	f
0	0	1
0	1	0
1	0	0
1	1	0

O/P

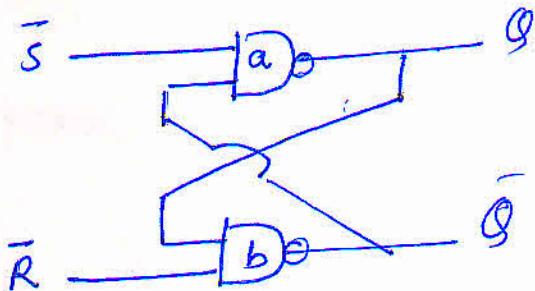
\Rightarrow If $R=S=0 \rightarrow Q$ remains unchanged (half previous state)

$\Rightarrow R=0, S=1, S=1$, force NOR_b to get low(0) then both inputs of NOR_a is low the O/P is high $\rightarrow Q=1$. when $S=1$ is said to be set the F.F. I.e $Q=1$

\Rightarrow for $R=1, S=0$, force NOR_a to get low(0) both inputs of NOR_b are 0 the out put is high. when $S=0$ is said to be reset the F/F I.e $Q=0, \bar{Q}=1$

$\Rightarrow R=S=1$, is forbidden, it force both NOR gate to go low. This violates the basic definition of F/F which require the O/P of NOR_a and NOR_b be complemented. Hence given to impose this condition. The RS flip-flop is also called a Latch

⇒ Latch may also be constructed using NAND logic. (If Any input of NAND logic is 0 the output is high).



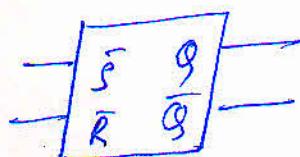
\bar{R} \bar{S} Q

1 1 Last stable

1 0 1 → set

0 1 0 → Reset/clear

0 0 ? → forbidden.



* for $\bar{S} = 0, \bar{R} = 1$ forces the output of NANDa to go high and F/F is set

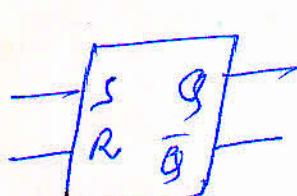
* for $\bar{S} = 1, \bar{R} = 0$ " " " " F/F is Reset

* for $\bar{R} = \bar{S} = 1$ F/F is Remains in previous state

* for $\bar{S} = \bar{R} = 0$ is forbidden because both Q and \bar{Q} are high

We call this latch is $\bar{R}\bar{S}$ flip flop

⇒ $\bar{R}\bar{S}$ latch can be modified to behave exactly as RS latch with NOR logic.



S $\rightarrow D_o \rightarrow D_o \rightarrow Q$

R $\rightarrow D_o \rightarrow D_o \rightarrow \bar{Q}$

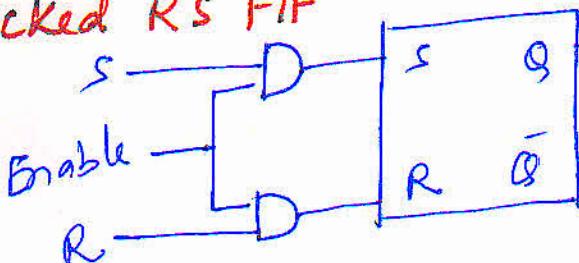
R S Q State
0 0 previous

0 1 1 → set

1 0 0 → Reset

1 1 ? → forbidden

Clocked RS F/F

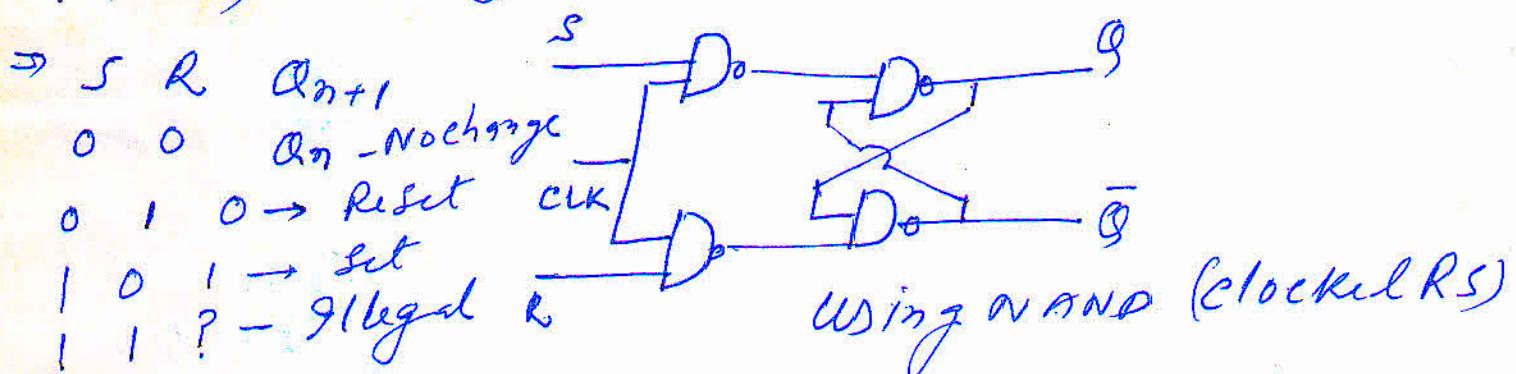


If Enable is low the output of ANDs gate is low

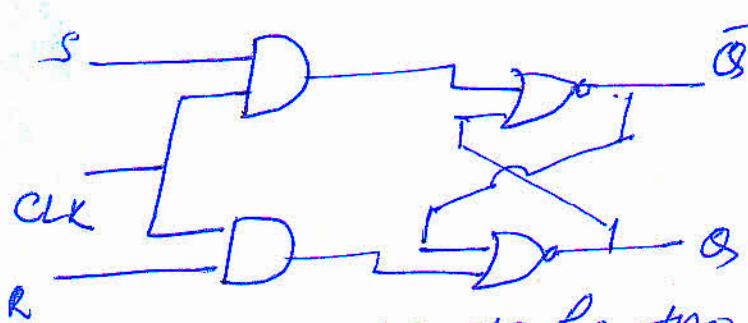
Neithow S nor R will have any effect on F/F

The F/F is said to be disabled.

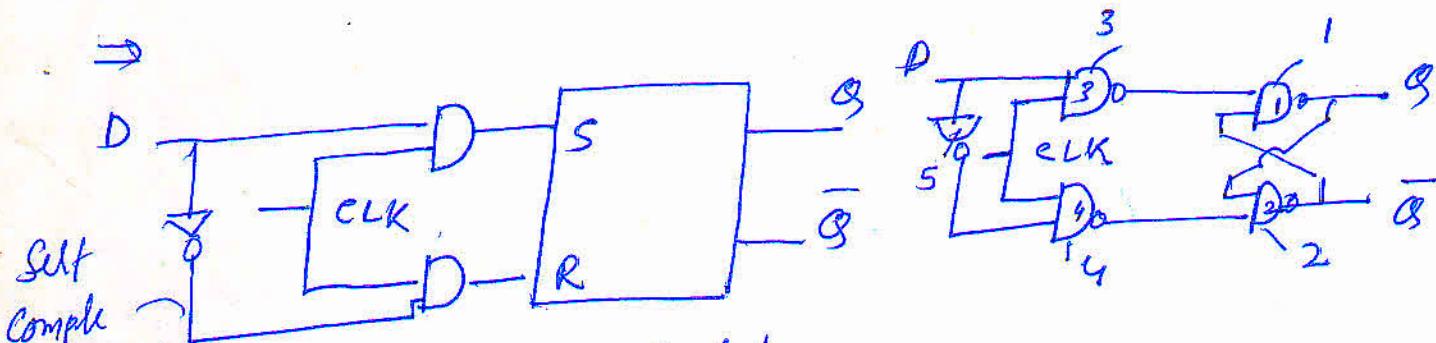
- ⇒ for high enable the information at R and S inputs will be transmitted directly to the output. The latch is said to be enabled.
- ⇒ The O/P will change in response to the input as long as enable is high, when enable goes low the O/P will retain the information that was present on input when high to low transition of enable take place
- ⇒ In this way it is possible to strobe or clock the F/F to store the information (Set/Reset) at any time and then hold the information (Stored) for any desired period of time



⇒ Using NOR



D FLIP FLOP: — RS F/F has two input R and S. Storing high bit requires high S, storing low bit (0) requires high R. The generation of two signals to derive a sup flop is disadvantageous in certain application. also when $R=S=1$, forbidden condition may occur. This has led to D-F/F which has single input and condition $R=S=1$ is also avoided.



Self
Complementary
memory.

Delay/FIFO or D latch

⇒ low CLK will provide high at 3, 4 and

Q, \bar{Q} Has previous state

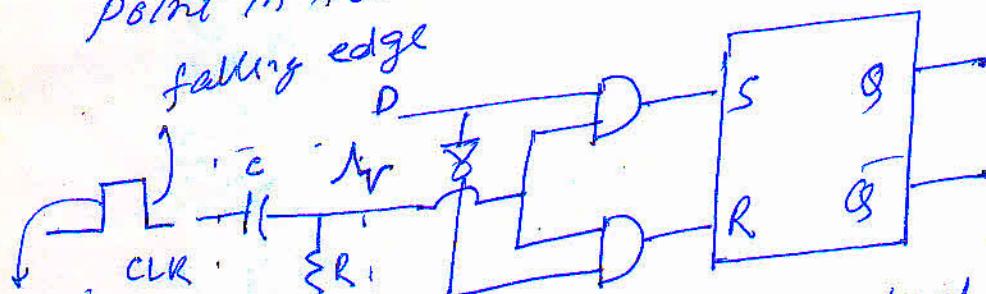
⇒ high CLK, $D=1$ forces gate 3 goes to 0 and hence

$Q=1 \leftarrow \text{Set}$

⇒ High CLK $D=0$, forces gate 4 " 0 and hence

$\bar{Q}=1 \leftarrow \text{Reset} \rightarrow Q=0$

EDGE Triggered D FIFs : D latch is used for temporary storage in electronic instruments. More popular D FIF used to in digital computers is of kind that sample the data bit at a unique point in time.



Leading edge - RC CC Tclk at the o/p of differentiator

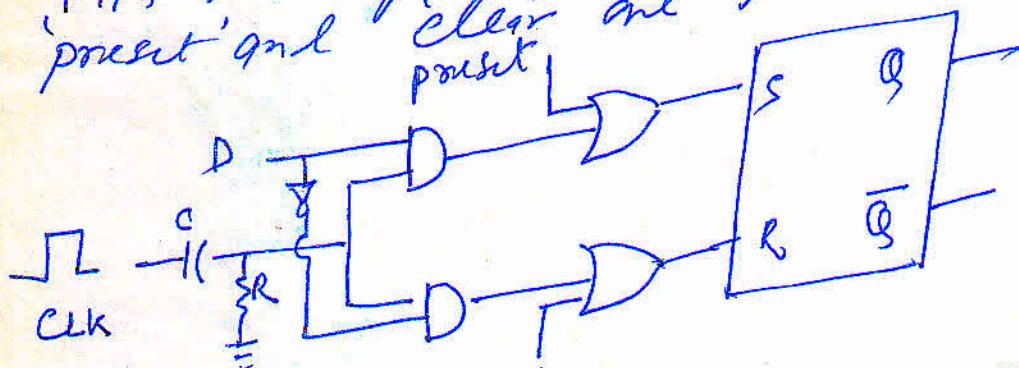
RC differentiator leading edge generates +ve voltage spike whereas trailing edge generates -ve voltage spike

Narrow +ve voltage spike enables AND gates and negative voltage spike does nothing. During +ve voltage spike, the value of D is sampled for an instant. This forcing the FIF is either set or reset. This is referred to as the edge triggering.

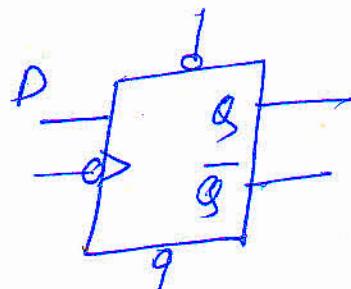
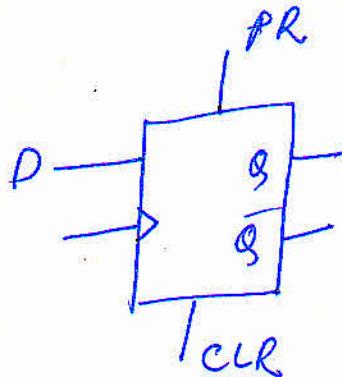
⇒ FIF Circuits don't use RC - Circuit to obtain spikes. Because it is difficult to fabricate capacitor on chip. other don't coupled designs (Master-slave) are used in IC's.

	CLK	D	Q_{n+1}
(+ve edge leading)	0	x	Q_n
	↑	1	1
(-ve edge trailing)	↑	0	0
	↓	x	Q_n

preset and clear function in FIF: When power is first switched on FIFs assume Random state; it could be necessary to Set or Reset all the FIFs initially, to do so, two asynchronously input 'preset' and 'clear' are included as follows



- ⇒ High preset forces Q to set $Q=1$ and high clear forces Q to Reset independent of CLK.
- ⇒ Since preset and clear activate FIF independent of CLK, they are called asynchronous/ outside inputs.
- ⇒ D input is synchronous, because it has an effect on Q and \bar{Q} only when CLK edge occurs.
- ⇒ Negative edge triggering is preferred in certain applications. An inverter may complement CLK pulse before it reaches AND gates



+ve edge triggered D/F/F
with active high PR and CLR

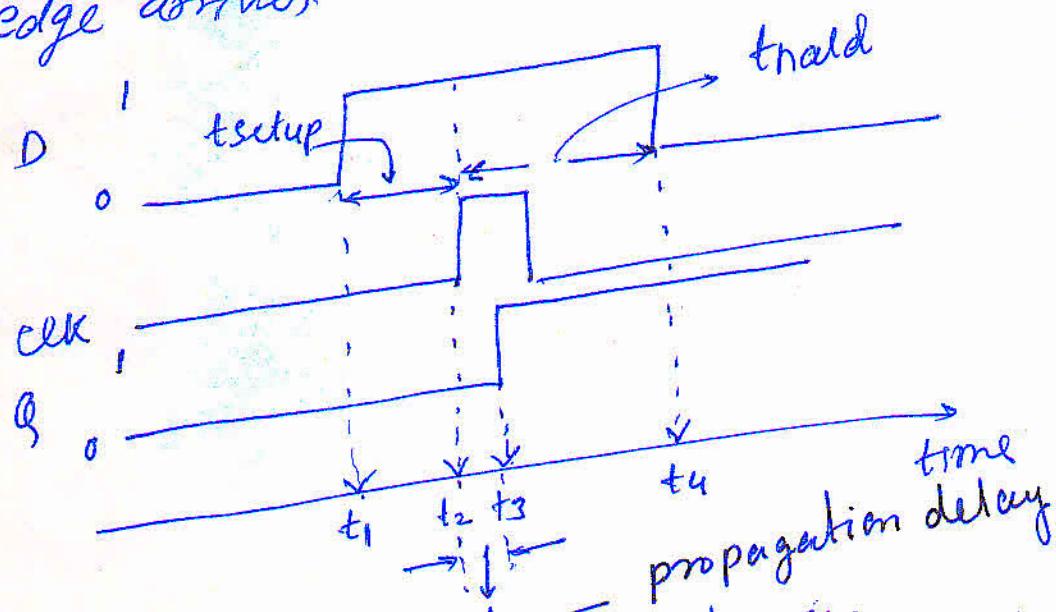
-ve edge triggered F/F
with active low PR and CLR

FLIP FLOP switching time :-

⇒ propagation delay:- The propagation delay t_p is the amount of time taken by off of a F/F to change states after input changes.

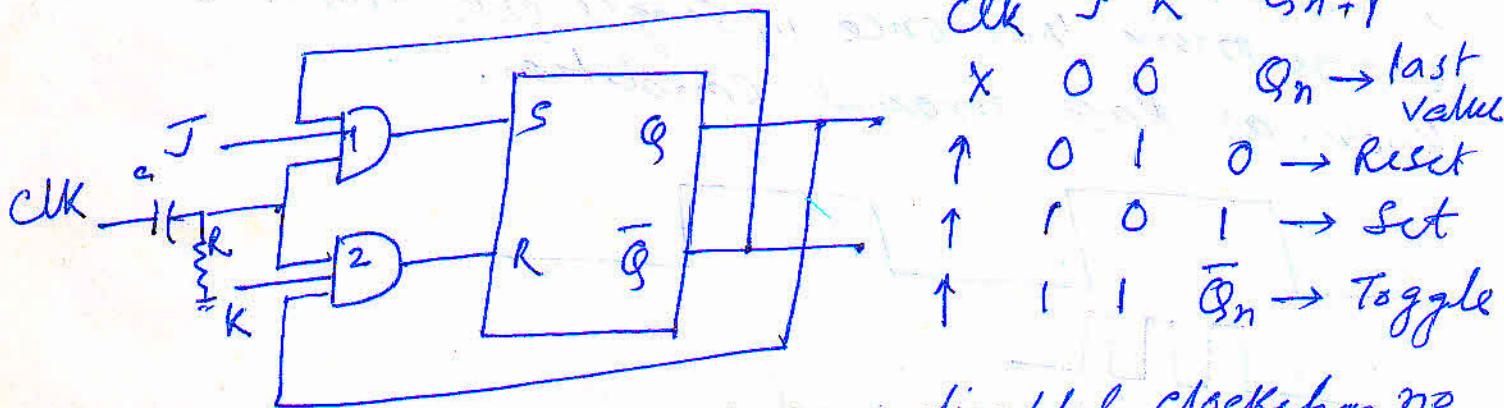
⇒ Set up time ⇒ t_{setup} is the minimum amount of time that the data bit must be present before CLK edge hits.

⇒ Hold time:- t_{hold} is the minimum amount of time that data bit D must be present after the CLK edge arrives.



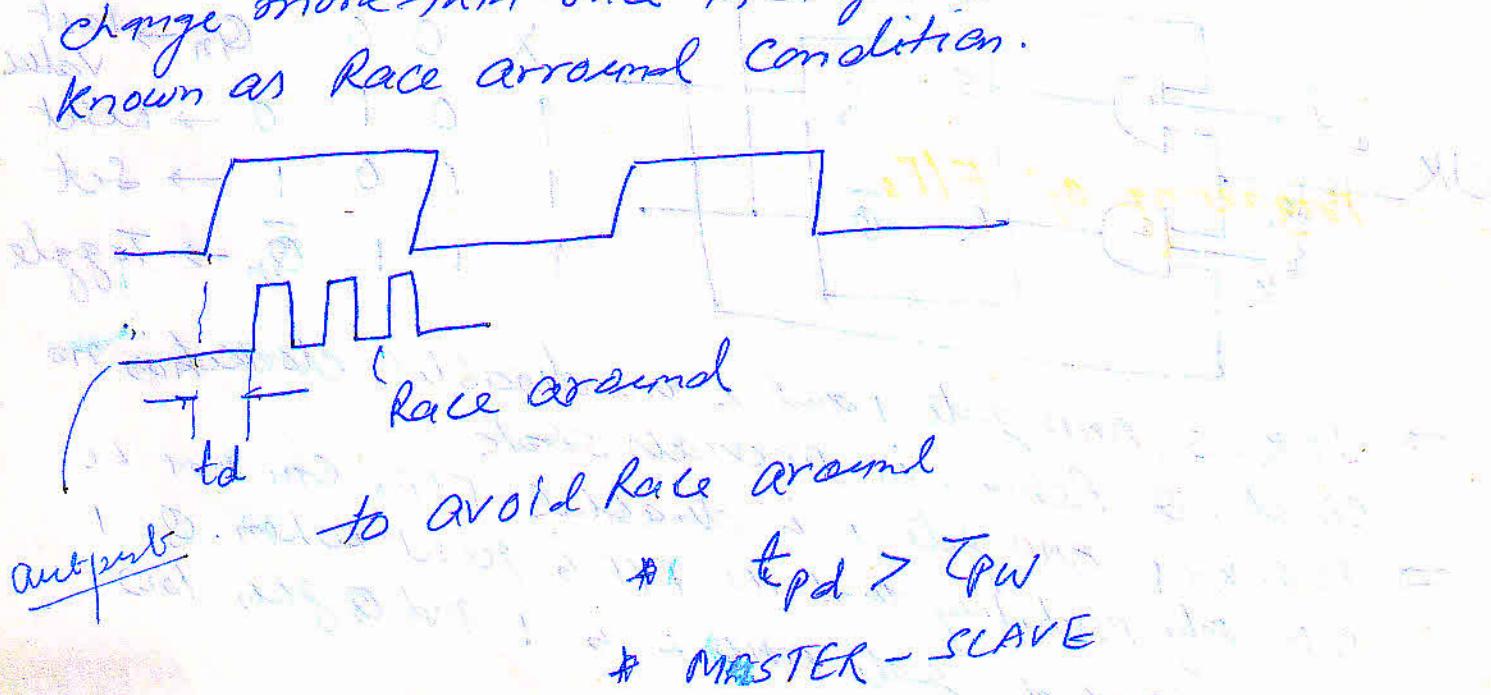
- ⇒ for $t < t_1$ D can be 0/1 or changing steadily
- ⇒ for $t_1 \leq t < t_2$ D must be held
- ⇒ Data D is shifted in to F/Fs. at $t = t_2$ (CLK edge) but does not appear at Q until time $t_3 \Rightarrow t_p = t_3 - t_2$
- ⇒ for proper operation D must be held steadily for $t_2 \leq t \leq t_4$
- ⇒ for $t > t_4$ D is forced to change.

JK FLIP FLOP:- JK flip flop is an ideal element for counter. Counter is a circuit that counts no. of +ve/-ve clk edges during its clk input.



- ⇒ $J=K=0$, AND gate 1 and 2 are disabled. Clock has no effect. Q remains in previous state.
- ⇒ $J=0, K=1$, AND gate 1 is disabled. F/F can not be set. Only possibility that the F/F is reset when $Q=1$ and output of gate AND 2 is 1 and Q goes low (unless the Q is already low).
- ⇒ $J=1, K=0$ AND gate 2 is disabled. F/F can't be reset if $Q=0 \Rightarrow \bar{Q}=1$ the AND gate 1 is enabled and F/F is set (unless Q is already high).
- ⇒ $J=K=1$ If $Q=1$ F/F is Reset (AND gate 2), If $Q=0$ F/F is set (AND gate 1). Eight way Q changes to complete the last stage (toggling).
- ⇒ If clock pulse remain high with $J=K=1$. After Q/Ps has been complemented once, it will cause repeated and continuous transitions of Q/Ps. To avoid this $t_{clk} < t_{pd}$, which can be eliminated with master slave or edge triggered construction.
- ⇒ The propagation delay prevents JK F/F from racing (toggling more pr. than once during +ve clk edge)
 - +ve edge triggered active high pr and CLK
 - ve edge triggered

Race around condition \rightarrow in level triggered JK FF if Both (Set to pre duration) JK F/F of Both
 $J = S, K = 1$ and $t_{pd} < T_{pw}$ then O/P will change more than once in single clk this is known as Race around condition.

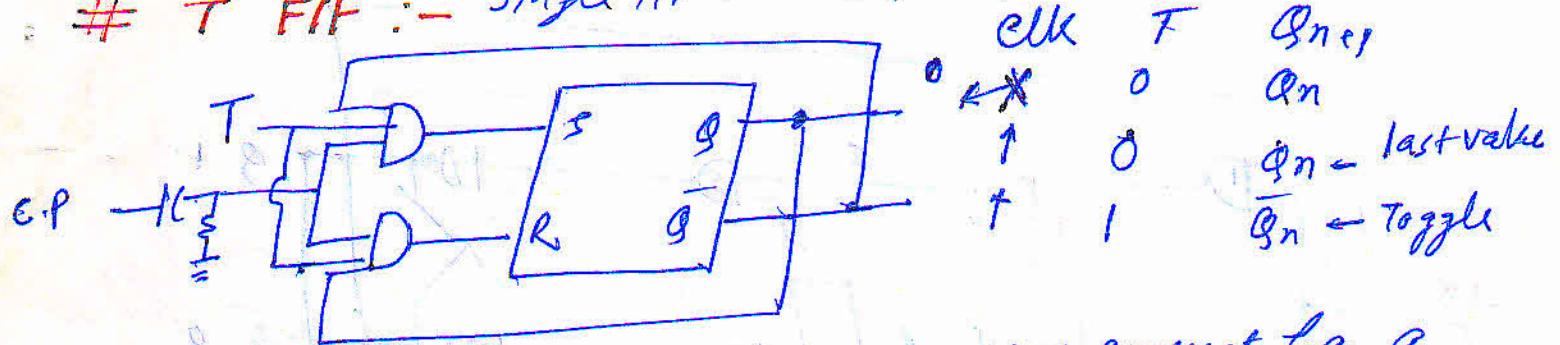


outputs \rightarrow to avoid race around

$$t_{pd} > T_{pw}$$

* MASTER - SLAVE

T F/F :- single IIP version of JK



Triggering of F/Fs :- A sequential circuit has a feedback path betn combinational ckt and memory elements. This feedback path may produce Instability if the o/p's of memory elements (F/Fs) are changing while o/p's of Combinational ckt that go to flip-flop input are being sampled by the clk pulse.

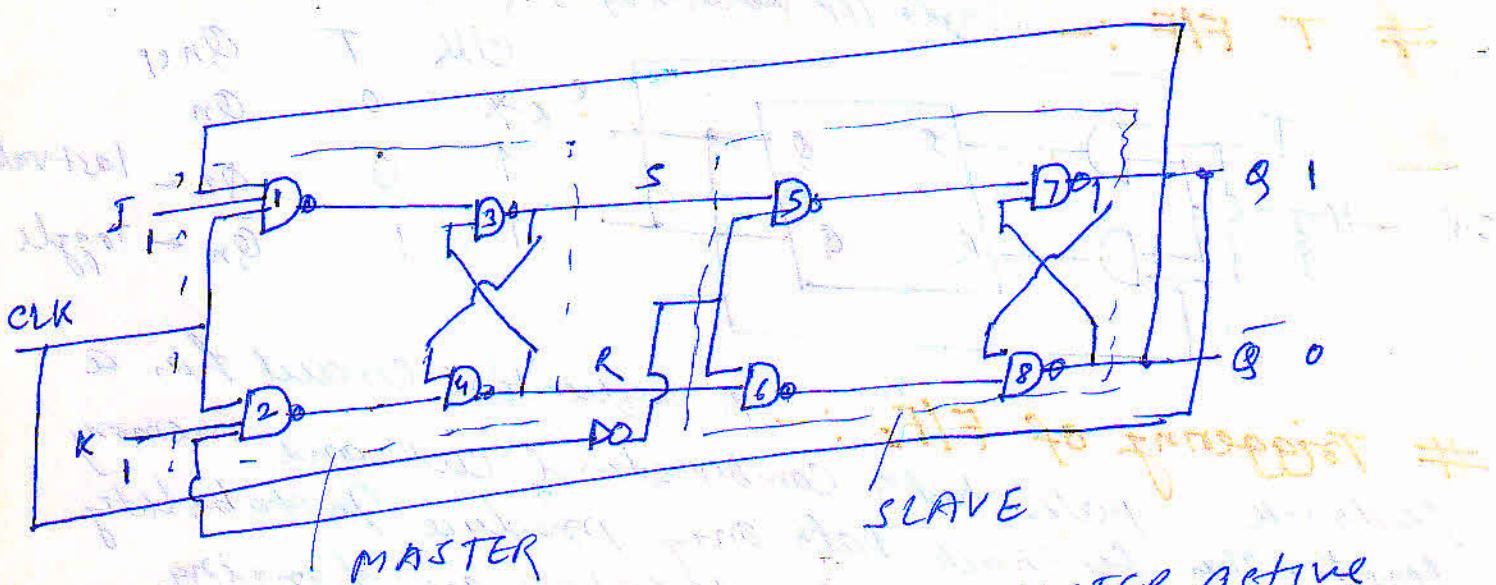
The timing problem may be eliminated if output of F/Fs do not start changing until pulse input has returned to zero. To ensure this F/F must have propagation delay in excess of clk pulse duration. ($t_{pd} > t_{cp}$).

Designers can not exercise on t_{pd} . Then the option is to make F/Fs sensitive to pulse transition rather than pulse duration.

The possible method are

- ⇒ * Insertion of RC ckt
- ⇒ * Master Slave Configuration
- ⇒ * edge triggered F/F

MASTER-SLAVE F/F:- The clk F/Fs are triggered when clk transition from 0 to 1 and state transition begins. As soon as clk pulse reaches 1 level, The new state of F/Fs may appear at the o/p terminal while 1P clk is still 1. New states are feedback and if when inputs also change while $clk=1$, F/Fs begins to respond to new values and new o/p state may occur.



\Rightarrow If $J=K=1$, $Q=1$, $\bar{Q}=0 \rightarrow \text{clk}=1$ MASTER active
 Slave Inactive $\rightarrow S=0, R=1$
 $\rightarrow \text{clk}=0$ MASTER inactive, slave
 active $\rightarrow Q=0, \bar{Q}=1$

- \Rightarrow The information at J and K inputs is transmitted to the Master on +ve edge of clk and is held until neg. edge of the clock occurs, after which it is allowed to pass through to the Slave F/F.
- \Rightarrow Slave copies master on negative edge clk
- \Rightarrow Slave copies master on negative edge clk
- \Rightarrow The new state appear at o/p terminal only after clk pulse has returned to zero.

