Date: 11/08/2020

Experiment No. 1

Aim: To design and verify Full Adder using basic gates.

Tool & Apparatus Used: LTspice, ICs Number

Theory: The Full Adder is an arithmetic circuits….

Fig.1.1 Circuit diagram of Full Adder

Table 1.1 Truth Table of Full Adde**r**

Design and Simulation:

Figure 1.2 Schematic of Full Adder

Observation:

Figure 1.3 Transient result of Full Adder output

Result: The Full Adder has been designed using basic gates and output and truth table are verified.

Applications: In ALUs, Computers, Microprocessors

Table of Contains

Exp. No.	Experiment	Exp. Date	Sub. Date	Remarks