

signed Binary NO. \rightarrow in signed binary NO. we require one extra bit to represent a +ve or -ve NO. Signed binary NO. is represented in the following ways.

1. Sign - Magnitude
2. Sign - 1's complement
3. Sign - 2's complement

- * A positive NO. in any representation has a 0 as the left most bit for +, followed by positive binary number.
- * A negative NO. Always has a '1' as the leftmost bit for negative followed by Magnitude bits as.
 - \rightarrow +ve NO. in Sign Magnitude form.
 - \rightarrow 1's complement of binary NO. in 1's comp. form
 - \rightarrow 2's complement of binary NO. in 2's comp. form

\Rightarrow Table for +ve and -ve four bit pattern (one bit for sign).

	Sign Mag.	1's Complement	2's Complement
0 \rightarrow	0,000		
1 \rightarrow	0,001		
2 \rightarrow	0,010		
3 \rightarrow	0,011		
4 \rightarrow	0,100		
5 \rightarrow	0,101		
6 \rightarrow	0,110		
7 \rightarrow	0,111		
-8 \rightarrow	Impossible	Impossible	1000
-7 \rightarrow	1,111	1,000	1,001
-6 \rightarrow	1,110	1,001	1,010
-5 \rightarrow	1,101	1,010	1,011
-4 \rightarrow	1,100	1,011	1,100
-3 \rightarrow	1,011	1,100	1,101
-2 \rightarrow	1,010	1,101	1,110
-1 \rightarrow	1,001	1,110	1,111
-0 \rightarrow	1,000	1,111	Impossible

⇒ using 7 bit representation.

$$\begin{array}{rcl}
 \text{Sign Mag.} & +11 & 0, 001011 \longrightarrow 1, 001011 \quad \text{Comp only sign bit} \\
 \text{Sign-1's Comp.} & 0, 001011 \longrightarrow 1, 110100 & \text{comp. each bit including sign bit} \\
 \text{Sign 2's Comp.} & 0, 001011 \longrightarrow 1, 110101 & \text{(taking 2's Comp. of +ve No. including sign bit).}
 \end{array}$$

Addition of Signed No. →

* Addition of two signed binary numbers in 2's Complement form is performed by adding two No. including their sign bit. A carry in MSB (sign bit) is ignored.

* If -ve No. in 1's complement form the carry out of MSB (sign bit) is added to the LSB of Sum and then ignored.

⇒ 7 bit representation. (in 2's Comp. form).

$$+11 \longrightarrow 0, 001011$$

$$+6 \longrightarrow 0, 000110$$

$$+17 \longrightarrow 0 \quad 010001$$

$$+11 = 0001011$$

$$-6 = 1111010$$

$$\begin{array}{r}
 \text{ignore EAC} \longrightarrow \textcircled{1} 0000101 \\
 \downarrow +5
 \end{array}$$

$$-11 \longrightarrow 1110101$$

$$+6 \longrightarrow 0000110$$

$$\begin{array}{r}
 \text{NO EAC} \longrightarrow 111011 \longrightarrow -5 \text{ in 2's Comp. form.}
 \end{array}$$

$$-11 \longrightarrow 1110101$$

$$-6 \longrightarrow 1111010$$

$$\begin{array}{r}
 \text{ignore EAC} \longrightarrow \textcircled{1} 1101111 \\
 \downarrow -17 \text{ in 2's Comp. form.}
 \end{array}$$

⇒ Addition using (1's Comp. form).

$$+11 \quad 0001011$$

$$+6 \quad 0000110$$

$$+17 \quad 0010001$$

$$-11 \longrightarrow 1110100$$

$$-6 \longrightarrow 1111001$$

$$\text{EAC} \longrightarrow \textcircled{1} 1101101$$

$$-17 \longleftarrow 1101110 \longrightarrow \text{in 1's Comp. form}$$

⇒ Note: * A zero with sign bit in different rep.

8-bit Pattern	Sign Mag	+0	-0
		0 0000000	1 0000000
	Sign 1's Comp.	0 0000000	1 1111111
	Sign 2's Comp	0 0000000	

* The Range of Binary Integer NO. that can be stored in n bit register.

- 1 bit is reserved for sign
- k bits are used to binary NO.

$$k = n - 1$$

⇒ In Sign Magnitude and 1's Comp the Range of NO. is

$$-(2^k - 1) \text{ to } +(2^k - 1)$$

⇒ In 2's Complement the range is

$$-2^k \text{ to } +(2^k - 1)$$

for example — 8 bit register can store.

	Sign-Mag	1's Comp	2's Comp
+127	0 1111111	0 1111111	0 1111111
-127	1 1111111	1 0000000	1 0000001
-128	Impossible	Impossible	1 0000000

Arithmetic Subtraction — using 2's Complement.

(Using 7 bit pattern). DO: $(+9) - (+6) = +3$

$$\begin{array}{r}
 +9 \rightarrow 0001001 \\
 +6 \rightarrow 0000110 \\
 -9 \rightarrow 1000111 \\
 -6 \rightarrow 1111010 \\
 \hline
 0001001 \\
 0000110 \\
 \hline
 0001111 \rightarrow +3
 \end{array}$$

DO: $(+9) - (-6) = +9 + 6$

$$\begin{array}{r}
 0001001 \\
 0000110 \\
 \hline
 0001111 \rightarrow +3
 \end{array}$$

DO: $(-9) - (+6)$

$$\begin{array}{r}
 1110111 \\
 1111010 \\
 \hline
 1110001 \leftarrow -15 \text{ in 2's complement}
 \end{array}$$

Encoding and Conversion \rightarrow Encoding requires more bits compared to conversion. on the Average $\log_2 10 = 3.32$ bits are required when decimal number are converted into binary while 4 bits per digit are required in encoding. The ratio $\frac{4}{3.32} = 1.2$ is measure of extra bits required this consequently requires extra storage as well.

* Conversion from decimal to binary is a slow process. An algorithm involving successive division is needed for conversion while encoding is straight forward table look up.

* There are (3×10^{10}) ways of developing codes. only few of them are chosen from viewpoint of

- i) ease in Arithmetic
- ii) error detection property
- iii) ease in coding.

Classification of codes \rightarrow

* weighted codes - $d = \sum w_i b_i$ w_i = weight of i th bit
 $b_i = 0/1$

* Self Complementary code - on Replacing 0 by 1 and 1 by 0 in a code for decimal digit d , one obtains the code for decimal digit $9-d$. It is called Self Complementary Code

* Cyclic / Reflected / Gray Code - A code in which each code differs from its Neighbour by only one bit

* Error detecting codes. The error detecting codes are ~~used~~ constructed by using redundant bits in the codes. one such Method is:

→ Introduce fifth bit such that total No. of 1's in 5 bit group is odd. This is called parity bit. If in a code total No. of 1's is not odd, one can conclude there exist a single error

* Error detecting codes :-

Transmitted Row Parity

Information bits: 0 0 0 1 1
 0 0 0 1 0
 0 0 1 0 0
 0 0 1 1 0
 0 1 0 0 0
 → 1 0 1 1

Receive

0 0 0 0 1
 0 0 0 1 0 ← Parity failure
 0 0 1 0 0
 0 0 1 1 1
 0 1 0 0 0
 1 0 1 1 → Parity failure

Column

Parity → single error detecting / correcting code failure

1	2	3	4	5	6	7
P ₁	P ₂	I ₃	P ₄	I ₅	I ₆	I ₇
0	0	0	1	0	0	0
0	1	0	1	0	0	1
0	1	0	1	0	1	0
1	0	0	0	0	1	1
0	0	0	1	0	0	0
1	0	0	0	1	1	0
0	0	0	1	0	0	1
1	0	0	1	0	0	1

← bit Position.
 1, 2, 4 → Parity bit
 3, 5, 6, 7 → Information bit
bit at position 1 - Even Parity for 1, 3, 5, 7
bit at position 2 - Even Parity for 2, 3, 6, 7.
bit at position 4 - Even Parity For 4, 5, 6, 7.

⇒ The following procedure are used to detect and correct the error.

* The position 1,3,5,7 passes even parity test → $c_1 = 0$

* The " 2,3,6,7 " " " " → c_2 is 0 or else $c_2 = 1$

* The position 4,5,6,7 " " " " → $c_4 = 0$ else else $c_4 = 1$

→ The decimal equivalent of $c_4 c_2 c_1$ gives position of incorrect bit. If $c_4 c_2 c_1 = 0$ it indicates no error

→ example : Received code is 0110110 that means.

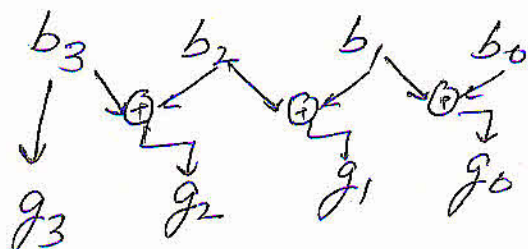
$c_1 = 0, c_2 = 1, c_4 = 0$, decimal $[c_4 c_2 c_1] = \text{dec}[010] = 2$

correct code is 0010110

# Codes	→	weights	^{8 4 -2 -1} 8421	→	2421	→	X-3
d		8421					
0	→	0000	→	0000	→	0011	
1	→	0001	→	0111	→	0100	
2	→	0010	→	0110	→	0101	
3	→	0011	→	0101	→	0110	
4	→	0100	→	0100	→	0111	
5	→	0101	→	0100	→	1000	
6	→	0110	→	1000	→	1001	
7	→	0111	→	1001	→	1010	
8	→	1000	→	1001	→	1011	
9	→	1001	→	1111	→	1100	

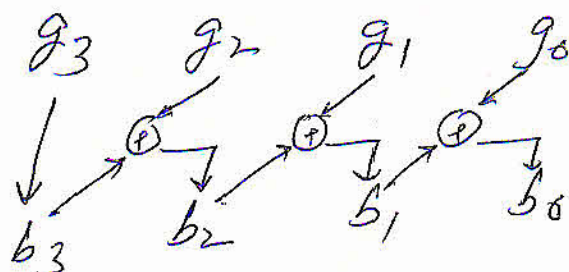
* A necessary condition for Self Complementary weighted code is that the sum of its weights be one Nine (9)

* A Self Complementary code need not necessarily be weighted e.g. X-3 non weighted Self Complementary

Conversion from binary to gray \rightarrow 

Rule
 * Retain MSB
 * Ex-OR every bit with next bit and place the Result or add two bits and ignore carry

dec	Binary	Gray
0 \rightarrow	0000	0000
1 \rightarrow	0001	0001
2 \rightarrow	0010	0011
3 \rightarrow	0011	0010
4 \rightarrow	0100	0110
5 \rightarrow	0101	0111
6 \rightarrow	0110	0101
7 \rightarrow	0111	0100

 \Rightarrow Gray to Binary

Rule
 * Retain MSB
 * Ex-OR this bit with next bit from gray code
 * The Result is then ex-ORed with next bit from gray code and so on.

Gray code is used in A/D Converter.

BCD - Binary Coded decimal - 0-9 with four

binary bit $25 \rightarrow 0010, 0101$

BCD Addition \rightarrow If Binary sum of pair of digits ≥ 10 , get correct BCD code by adding 0110 (6) to sum else leave it alone.

⇒ Add 65 and 85

$$\begin{array}{r}
 65 \rightarrow 0110 \quad 0101 \\
 85 \rightarrow 1000 \quad 0101 \\
 \hline
 1110 \quad 1010 \\
 \text{Correction} \rightarrow 0110 + 0110 \leftarrow \text{correction.} \\
 \hline
 1 \quad 010010000 \\
 \downarrow \quad \downarrow \quad \downarrow \\
 0101 \quad 0000 \\
 \downarrow \quad \downarrow \\
 \text{Result}
 \end{array}$$

Result 0000 0101 0000 ← 150

* In BCD addition, correction is also required when sum yields a carry.

Add → 19, 28

$$\begin{array}{r}
 19 \rightarrow 0001 \quad 1001 \\
 28 \rightarrow 0010 \quad 1000 \\
 \hline
 0100 \quad 10001 \\
 \downarrow \quad \downarrow \\
 0100 \quad 0110 \leftarrow \text{correction.} \\
 \hline
 0100 \quad 0111 \\
 \downarrow \quad \downarrow \\
 0100 \quad 0111 \leftarrow \text{Result}
 \end{array}$$

* Subtract 18 from 25 using 10's complement (in BCD).

$$\begin{array}{r}
 \text{Minuend} \rightarrow 0010 \quad 0101 \\
 \text{10's Complement of Subtrahend} \rightarrow 1000 \quad 0010 \\
 (100 - 18 = 82) \\
 \hline
 1010 \quad 0111 \\
 \downarrow \\
 \text{Correction} \rightarrow 0110 \\
 \hline
 \text{Ignore EAC} \leftarrow 1 \quad 0000 \\
 \hline
 \text{Result} \rightarrow 0000 \quad 0111 \leftarrow 07
 \end{array}$$

* Subtract 25 from 18

$$\begin{array}{r}
 \rightarrow 0001 \ 1000 \\
 \rightarrow 0111 \ 0101 \\
 \hline
 1001 \quad 1101 \\
 \hline
 9 \quad 10011 \\
 \downarrow 3
 \end{array}$$

← correction.

NO EAC Result = - (10's comp of 93) = -07

Addition of Xs-3 Code →

* If a carry is generated add 0011 (3) to the sum and if no carry is generated subtract 0011 (3) from sum.

⇒ Add 525 and 639 (in Xs-3 code)

$$\begin{array}{r}
 \text{Augend} \rightarrow 1000 \ 0101 \ 1000 \\
 \text{Addend} \rightarrow 1001 \ 0110 \ 1100 \\
 \hline
 1 \ 0001 \ 1100 \ 10100
 \end{array}$$

$$\begin{array}{r}
 +11 \quad +11 \quad -11 \quad +11 \\
 \hline
 0100 \ 0100 \ 1001 \ 0111
 \end{array}$$

[0110 + BEP] → Xs-3.

Result = 1 1 6 4
 ⇒ Subtract 863 - 425 (using 10's complement) (in Xs-3 code)

Mineend $\xrightarrow{863}$
 10's comp of Subtrahend (575)

$$\begin{array}{r}
 1011 \ 1001 \ 0110 \\
 1000 \ 1010 \ 1000 \\
 \hline
 10011 \ 1110
 \end{array}$$

$$\begin{array}{r}
 \text{ignore EAC} \leftarrow \textcircled{1} \ 0100 \ 10011 \ 1110 \\
 +11 \quad +11 \quad -11 \quad \leftarrow \text{correction.} \\
 \hline
 0111 \ 0110 \ 1011
 \end{array}$$

Result = 4 3 8