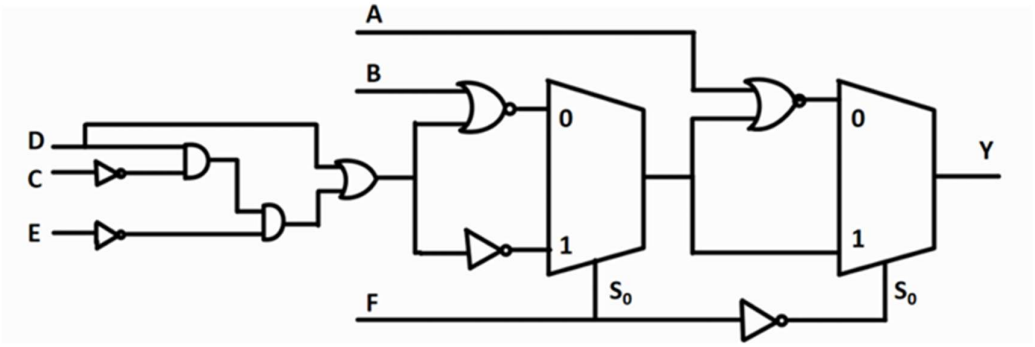
VLSI Physical Design with Timing Analysis

Assignment -2

Qns 1 to 2: Question Label: Comprehension

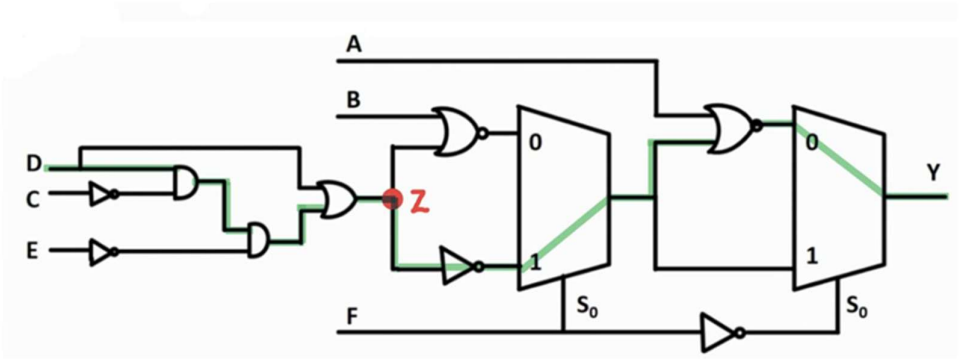
Consider the following logic circuit. Delays of logic gates are t_{NOR} = 1.5ns, t_{NOT} = 1ns, t_{OR} = 2ns, t_{AND}= 1.5ns and t_{MUX} = 2.5ns.



The critical path delay in the logic circuit given above is _____

a. 14 ns
b. 13.5 ns
c. 13 ns
d. 12.5 ns

Ans: **(d) 12.5**



$Z = D + \overline{C}.D.\overline{E} = D\ (1 + \overline{C}.\overline{E}) = D$

The value at point Z in the circuit does not depend on C and E, So the inverters doesn't need to be considered in the critical path delay.

$T_{critical} = t_{and} + t_{and} + t_{or} + t_{not} + t_{mux} + t_{nor} + t_{mux}$

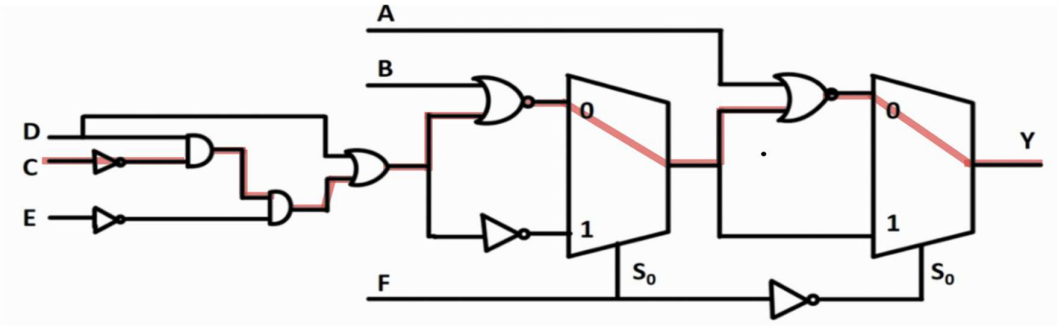
$T_{critical} = 1.5+1.5+2+1+2.5+1.5+2.5$

$T_{critical} = 12.5$ ns

Qns 2: Find the delay of the false path in the logic circuit given in question 1.

a. 11 ns
b. 12 ns
c. 13 ns
d. 14 ns

Ans: (d) 14ns



$T_{false} = t_{NOT} + t_{AND} + t_{AND} + t_{OR} + t_{NOR} + t_{MUX} + t_{NOR} + t_{MUX}$

$T_{false} = 1+1.5+1.5+2+1.5+2.5+1.5+2.5$

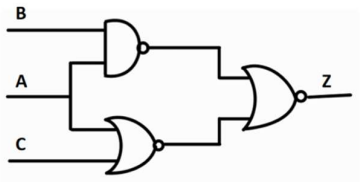
$T_{false} = 14$ ns

Qns 3: Which of the following is/are true?

a. If setup time increases, then speed will decrease.
b. For fixing hold violation, we may increase delay of combination path.
c. Negative skew improves speed of design.
d. Positive skew degrades hold requirement.

Ans: (a, b, d) refer lecture slide

Qns 4: Consider the following logic circuit.



What is the Unateness of output pin Z with respect to the input pin A?

a. Negative unate
b. Positive unate
c. Non-unate
d. Can't determined

Ans: (b)

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Case – 1: keep B = 0, C = 0 and A is changing from 0 → 1. You see no change in the output Z from truth table.

Case – 2: keep B = 0, C = 0 and A is changing from 1 → 0. You see no change in the output Z from truth table.

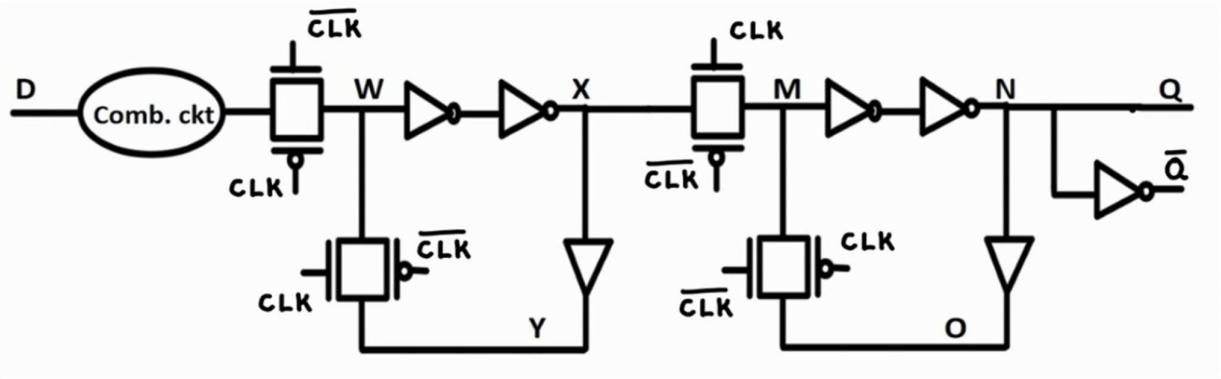
Case – 3: keep B = 1, C = 1 and A is changing from 0 → 1. You see 0 → 1 in the output Z from truth table.

Case – 4: keep B = 1, C = 1 and A is changing from 1 → 0. You see 1 → 0 in the output Z from truth table.

Similarly, you can check for four other cases and find that output pin Z is of positive unate with respect to pin A.

Qns 5 to 7: Question Label: Comprehension

Consider the master-slave flipflop circuit given below.

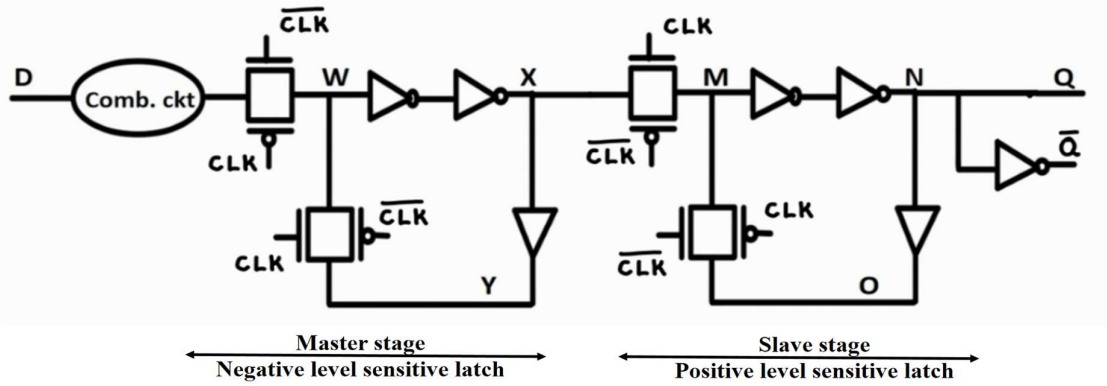


Delays of gates are: t_{INV} = 0.5ns, t_{BUF} = 0.8ns, t_{TX} = 1ns , t_{comb} = 1ns

Given master-slave flipflop is _____ triggered.

a. Positive edge
b. Negative edge
c. Level
d. Can't determined

Ans: (a)

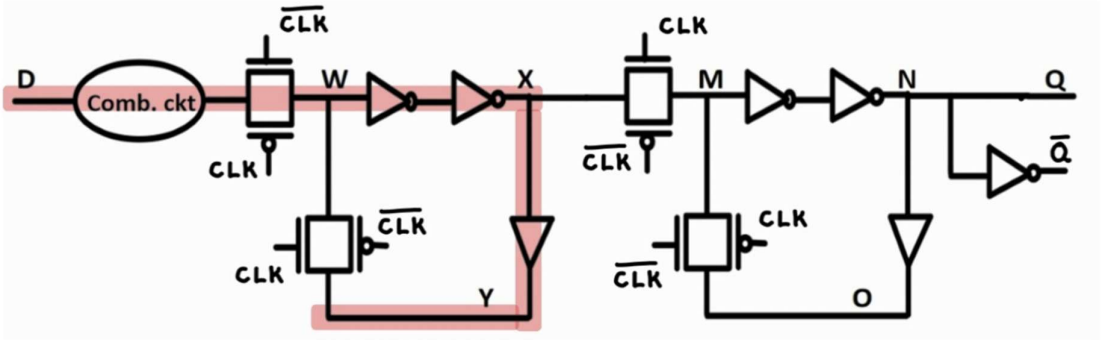


Data is captured by master during negative clock cycle and slave becomes transparent during positive cycle. So, it is a Positive edge triggered flipflop.

Qns 6: The setup time of the master-slave flipflop in given main question is _____ns.

a. 3.5 ns
b. 3.8 ns
c. 2.8 ns
d. 2.5 ns

Ans: (b) 3.8 ns



$T_{setup} = t_{comb} + t_{TX} + 2*t_{INV} + t_{BUF}$

$T_{setup} = 1+1+2*0.5+0.8$

$T_{setup} = 3.8ns$

Qns 7: The hold time of the master-slave flipflop in given main question is

a. Negative
b. Positive
c. Zero
d. Can't determined

Ans: (c)

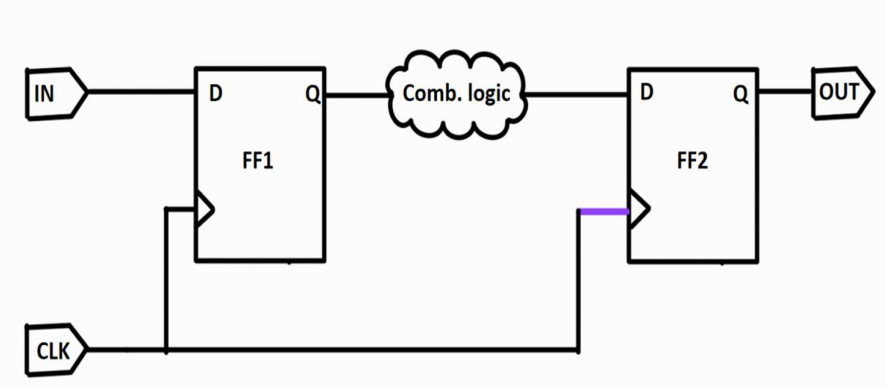
t_{comb} = 1ns, t_{TX} =1ns

$t_{comb} = t_{TX}$

Hold time is Zero. (refer lecture slide)

Qns 8 to 9: Question Label: Comprehension

Consider the following diagram



Delay values of Flipflop and Combinational circuit are: $\mathbf{t_{setup}}$ = 2.5 ns and $\mathbf{t_{hold}}$ = 3 ns

Delay	**T_{clk-q} (ns)**	**T_{comb} (ns)**
Max.	7	10.5
Min.	4.5	3

The maximum frequency at which the given circuit can operate without failure is ____(MHz) (roundup to the nearest integer)

Ans: 50MHz

$T_{CLK} \geq t_{clk-q}$ (max) + t_{comb} (max) + t_{setup}

$T_{CLK} \geq 7 + 10.5 + 2.5$

$T_{CLK} \geq 20ns$

$F_{MAX} = 1 / T_{CLK}$ (min)

$F_{MAX} = \frac{1}{20ns}$ = 50 MHz

Qns 9: Choose the correct hold constraint equation for the circuit given in main question.

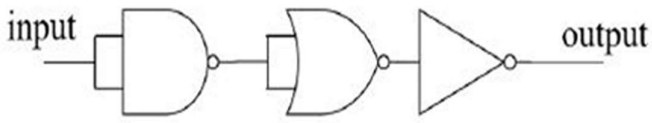
a. 3ns ≤ 10.5ns + 7ns
b. 3ns ≤ 4.5ns + 3ns
c. 3ns ≤ 4.5ns + 7ns
d. 3ns ≤ 7ns + 3ns

Ans: (b)

$t_{HOLD} \leq t_{clk\text{-}q}$ (min) + t_{comb} (min)

3ns ≤ 4.5ns + 3ns

Qns 10: Consider the given logic circuit. Find the rise and fall delay of timing path from input to output.



The rise and fall delay of the gates are as follow

Gate	Not(ns)	Nor(ns)	Nand(ns)
Rise delay	3	5	3
Fall delay	2	4	4

a. t_{rise}=14ns, t_{fall}=16ns

b. t_{rise}=11ns, t_{fall}=10ns

c. t_{rise}=10ns, t_{fall}=11ns

d. t_{rise}=16ns, t_{fall}=14ns

Ans: (c)

t_{rise}= t_{rise}(nand)+t_{fall}(nor)+ t_{rise}(inv)

t_{rise}=3+4+3

t_{rise}=10ns

t_{fall}= t_{fall}(nand)+t_{rise}(nor)+ t_{fall}(inv)

t_{fall}=4+5+2

t_{fall}=11ns