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# VLSI Physical Design with Timing Analysis

## Lecture – 9: Delay Parameters of Combinational Circuits

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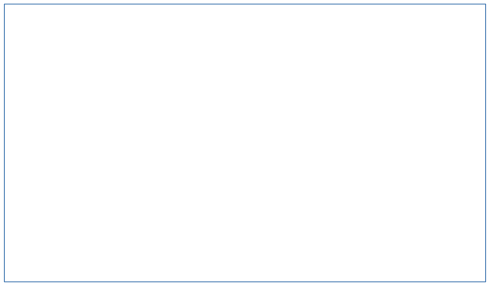
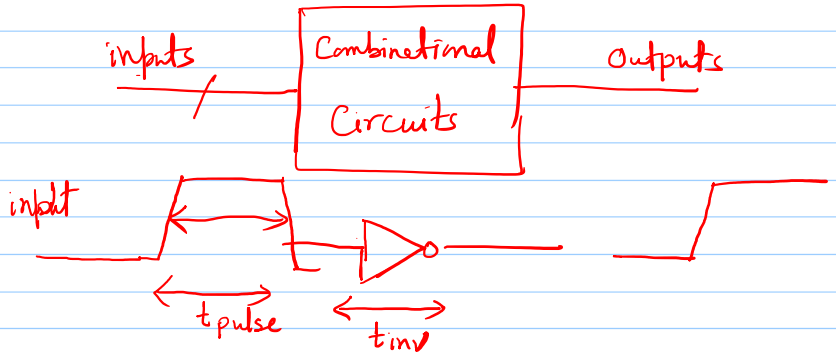
- Delay Parameters of Logic gate

  (1) Propagation Delay and (2) Transition time
- Delay of Timing path



Combinational Circuits




Case I $t_{pulse} > t_{inv}$, then the pulse will appear at the output of the gate

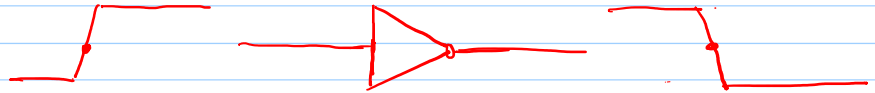
Case II $t_{pulse} < t_{inv}$, then the pulse will not appear at the output

This property of the logic gate is called inertial delay property

## Propagation Delay of Combinational Circuits :

of logic gate

- It is measured between the 50% transition points of the input and output waveforms.



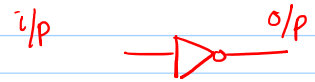
Types of Propagation Delay

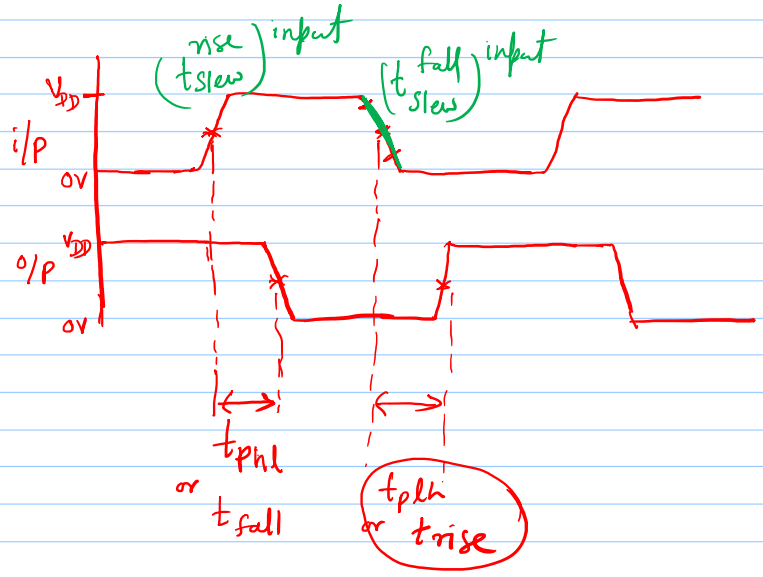
- **Rise Propagation Delay (Tplh)** = The signal-delay time between 50% of the input and 50% of the output when the output changes from low to high level.


- **Fall Propagation Delay (Tphl)** = The signal-delay time between 50% of the input and 50% of the output when the output changes from high to low level.

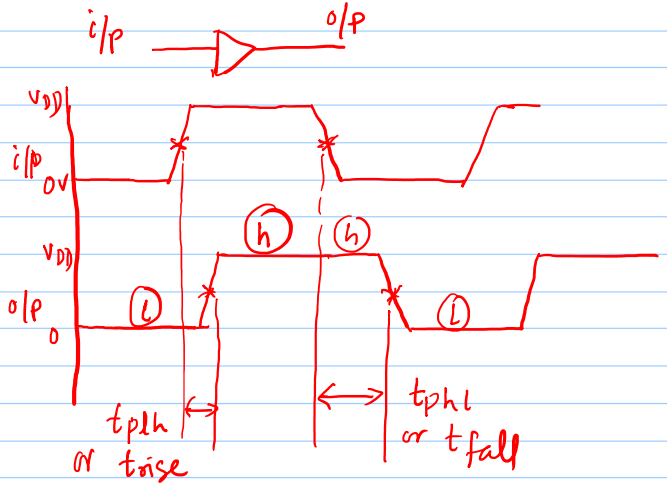

- **Average propagation delay** tp =(Tphl + Tplh)/2

## Inverting gate




## Non-inverting gate

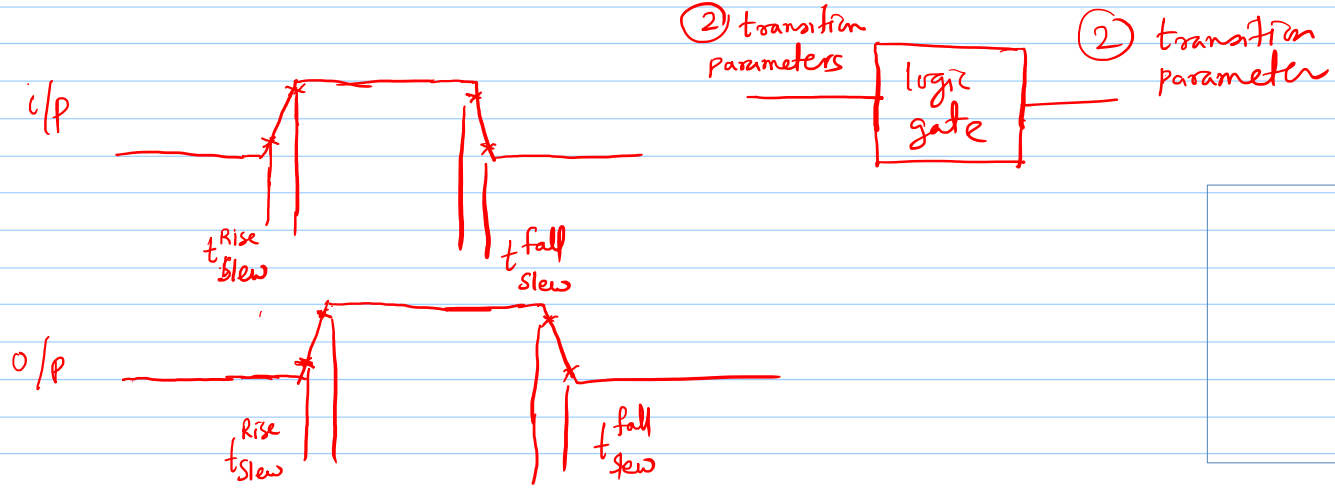


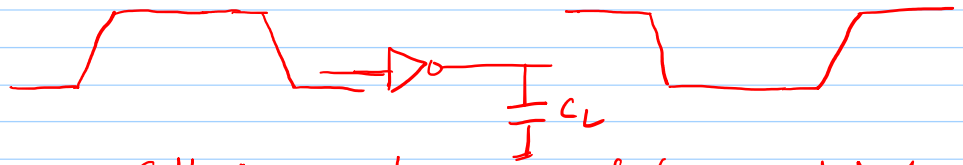
**Rise transition delay**

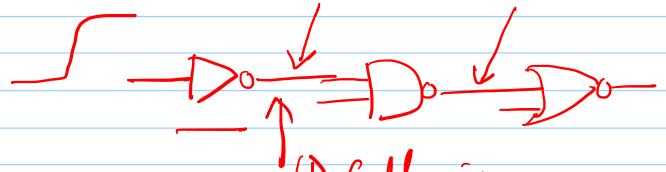
- The time taken by the signal to rise from 10% (20%) to 90% (80%) of its maximum value.

**Fall transition delay**

- The time taken by the signal to fall from 90% (80%) to 10% (20%) of its maximum value.





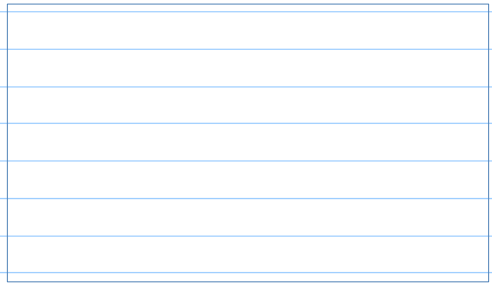
① Cell rise
② Cell fall
③ Output transition time (Rise)
④ Output " time (fall)

Cell rise or $t_{plh}$ = f ($C_L$, input transition time)
= f ($C_L$, input fall transition time)

Cell fall or $t_{phl}$ = f ($C_L$, input rise transition time)

Output transition time (Rise) = f ($C_L$, input fall transition time)

" " " (fall) = f ($C_L$, input rise transition time)



```
pin (OUT) {
  max_transition : 1.0;
  timing() {
    related_pin : "INP1";
    timing_sense : negative_unate;
    cell_rise(delay_template_3x3) {
      index_1 ("0.1, 0.3, 0.7"); /* Input transition */
      index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
      values (  /*   0.16      0.35      1.43 */ \
        /* 0.1 */   "0.0513,  0.1537,  0.5280", \
        /* 0.3 */   "0.1018,  0.2327,  0.6476", \
        /* 0.7 */   "0.1334,  0.2973,  0.7252");
      }
    cell_fall(delay_template_3x3) {
      index_1 ("0.1, 0.3, 0.7"); /* Input transition */
      index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
      values (  /*   0.16      0.35      1.43 */ \
        /* 0.1 */   "0.0617,  0.1537,   0.5280", \
        /* 0.3 */   "0.0918,  0.2027,   0.5676", \
        /* 0.7 */   "0.1034,  0.2273,   0.6452");
    }
```

1) $t_{plh}$ or $t_{rise}$

2) $t_{phl}$ or $t_{fall}$

.lib → used extensively in STA

Source : Static Timing Analysis For Nanometer Designs: A Practical Approach by J. Bhasker and Rakesh Chadha

```
pin (OUT) {
  max_transition : 1.0;
  timing() {
    related_pin : "INP";
    timing_sense : negative_unate;
    rise_transition(delay_template_3x3) {
      index_1 ("0.1, 0.3, 0.7"); /* Input transition */
      index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
      values ( /*   0.16      0.35     1.43 */ \
        /* 0.1 */  "0.0417,  0.1337,  0.4680", \
        /* 0.3 */  "0.0718,  0.1827,  0.5676", \
        /* 0.7 */  "0.1034,  0.2173,  0.6452");
    }
    fall_transition(delay_template_3x3) {
      index_1 ("0.1, 0.3, 0.7"); /* Input transition */
      index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
      values ( /*    0.16      0.35     1.43 */ \
        /* 0.1 */   "0.0817,  0.1937,  0.7280", \
        /* 0.3 */   "0.1018,  0.2327,  0.7676", \
        /* 0.7 */   "0.1334,  0.2973,  0.8452");
    }
```

3) Output signal Rise transition

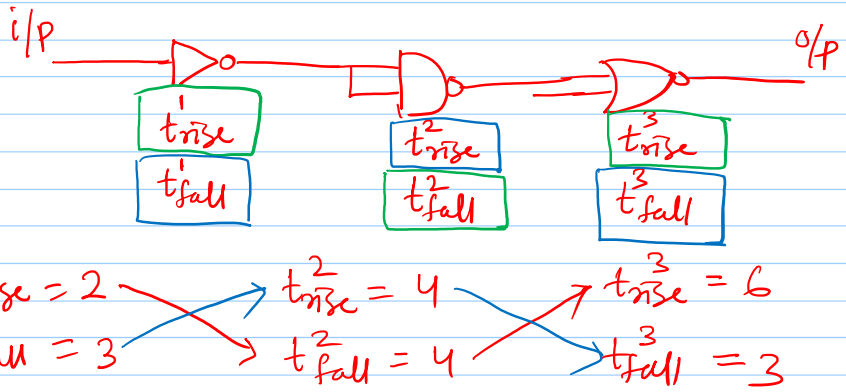
4) Output signal fall transition.

Source : Static Timing Analysis For Nanometer Designs: A Practical Approach by J. Bhasker and Rakesh Chadha

# Delay of a timing Path

$$T_{rise} = (t_{plh})^{path} = t^1_{rise} + t^2_{fall} + t^3_{rise}$$

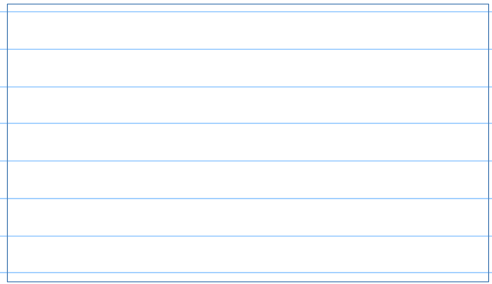
$$T_{fall} = (t_{phl})^{path} = t^1_{fall} + t^2_{rise} + t^3_{fall}$$

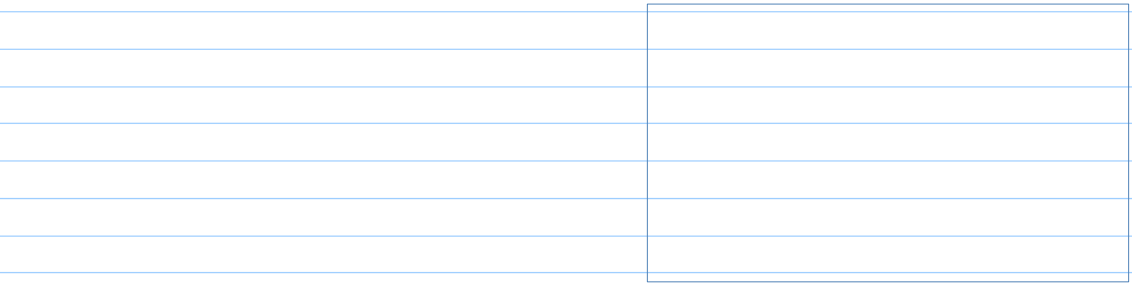


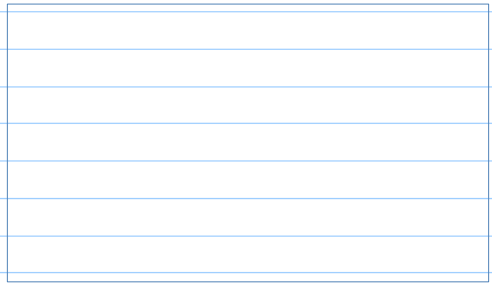

$T_{rise} = 2 + 4 + 6 = 12$

$T_{fall} = 3 + 4 + 3 = 10$

$T_{rise} > T_{fall}$







# Thank You