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NPTEL ONLINE CERTIFICATION COURSE

VLSI Physical Design with Timing Analysis

Lecture – 2: Introduction to VLSI Physical Design

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- Physical Design Flow
- Physical Verification
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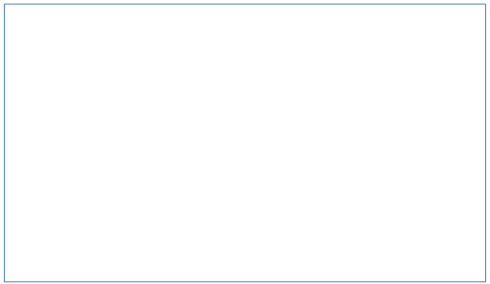
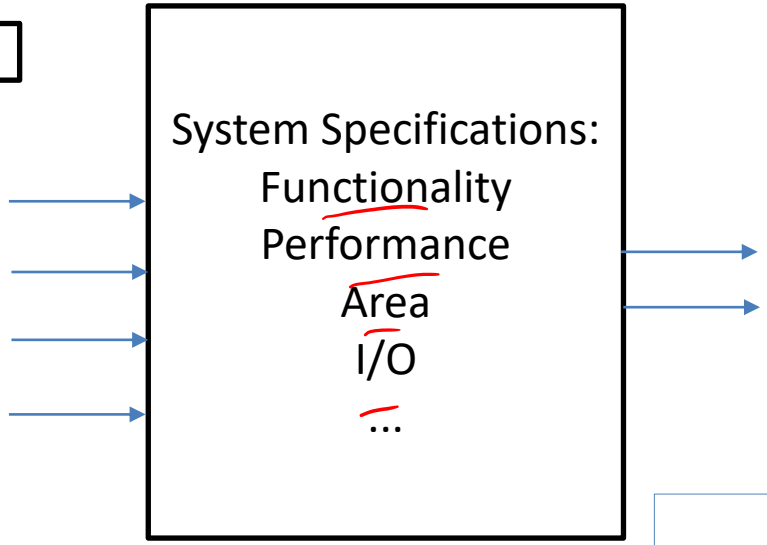


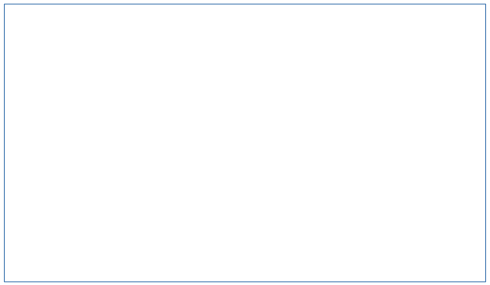
VLSI Design Flow

System Specification



System Specification

- Define overall goals and high-level requirements.
- Specify functionality, performance targets, physical dimensions, and production technology constraints.
- Involve chip architects, circuit designers, product marketers, operation managers, and layout and library designers.



VLSI Design Flow

System Specification

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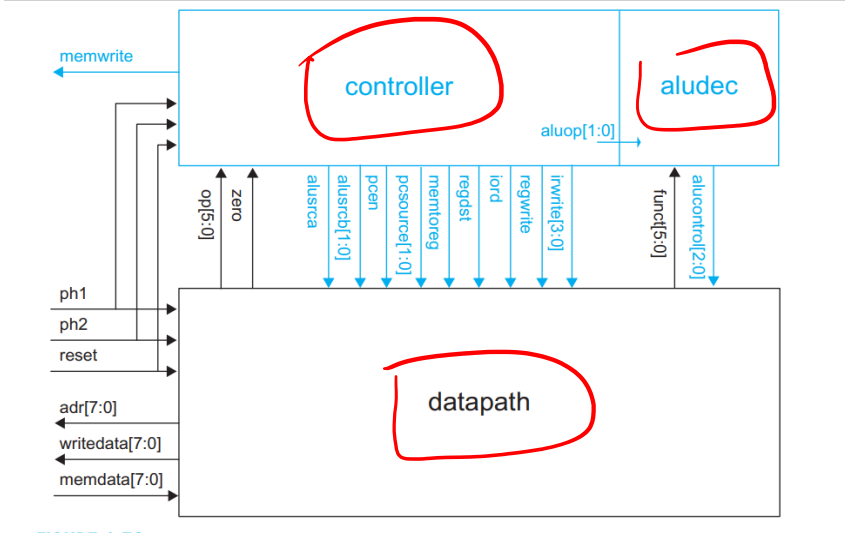
Architectural Design

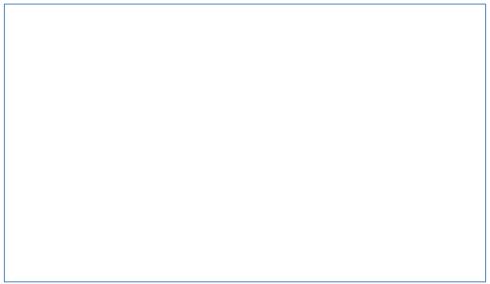
Top-level MIPS block diagram



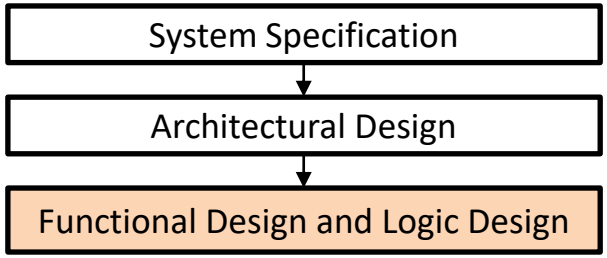
Picture Source: Weste, Neil and Harris, David: CMOS VLSI Design: A Circuits and Systems Perspective

Architectural Design

- Decide on the integration of analog and digital blocks.
- Establish memory management strategies.
  - serial/parallel, addressing scheme
- Determine the number and types of computational cores
  - processors, DSP units
- Choose communication protocols and support for standard interfaces.
- Consider using hard and soft intellectual property (IP) blocks.



VLSI Design Flow



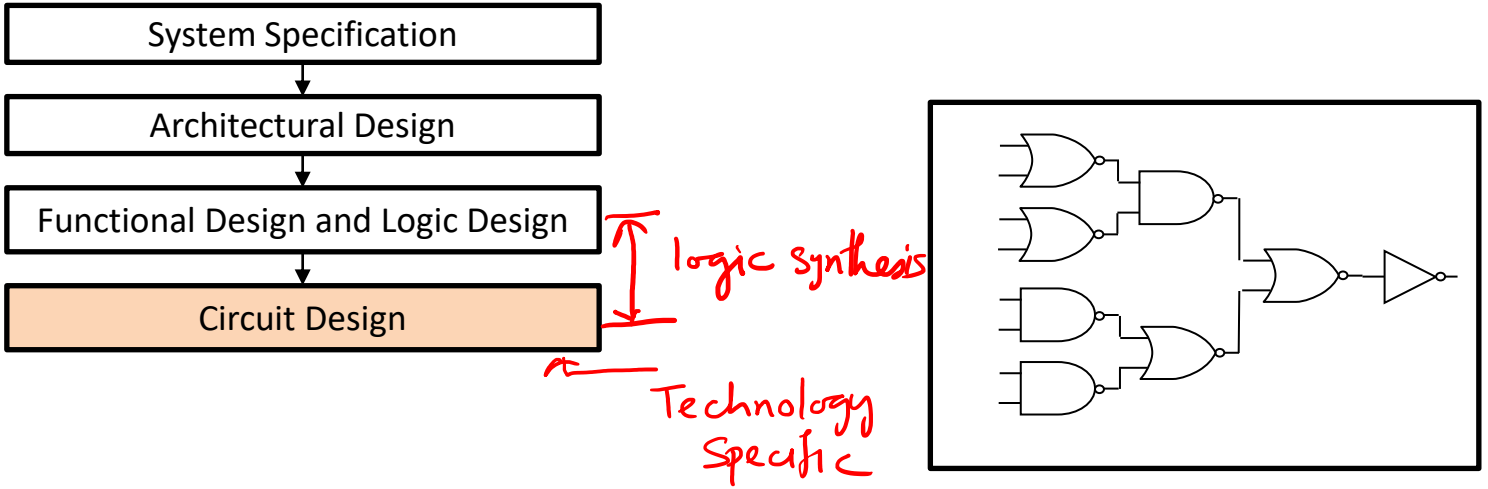

```
module Verilog_mod(out1, out2,…,in1, in2… )
   input in1, in2;
   output out1, out2;
   always@(posedge clk) begin
      out1 = in1 + in2;
        ⋮
   end
endmodule
```

RTL: Verilog Code

Functional and Logic Design

- Define the functionality and connectivity of each module.
- Perform functional design to specify high-level behavior.
- Logic design is done at the register-transfer level (RTL) using HDLs.
- Simulate and verify module behavior thoroughly.
- Utilize logic synthesis tools to convert HDL into low-level circuits.

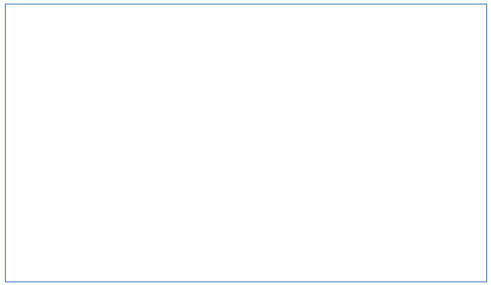
VLSI Design Flow



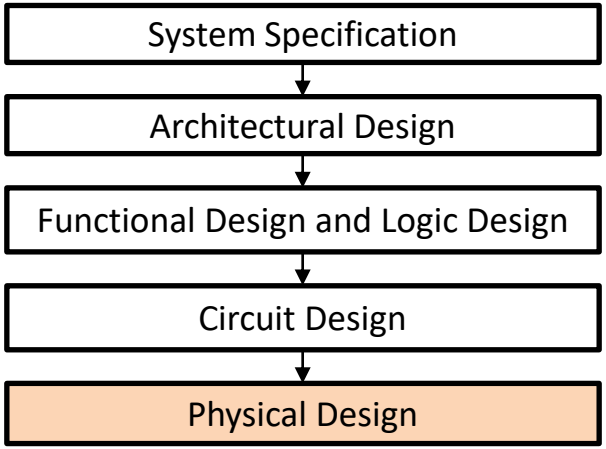
Circuit Design

- Identify critical elements designed at the transistor level.
- Examples include static RAM blocks, analog circuits, and high-speed functions.
- Use circuit simulation tools like SPICE to verify correctness.
- Consider factors like transistor size, power, and manufacturing variability.

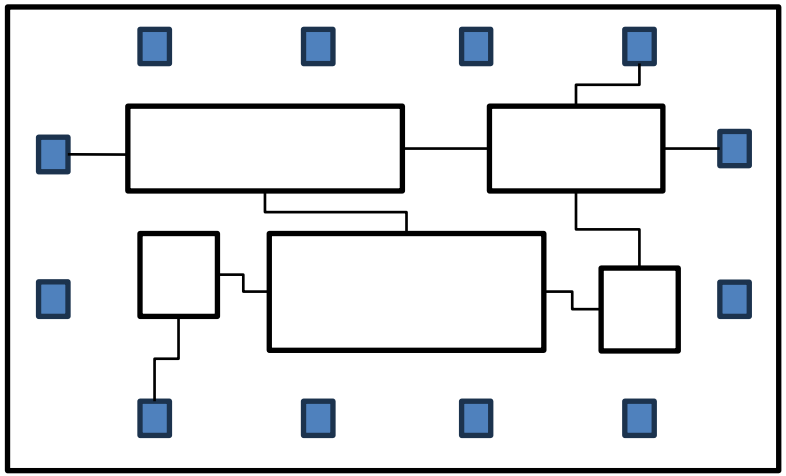
LTspice



VLSI Design Flow



Physical synthesis

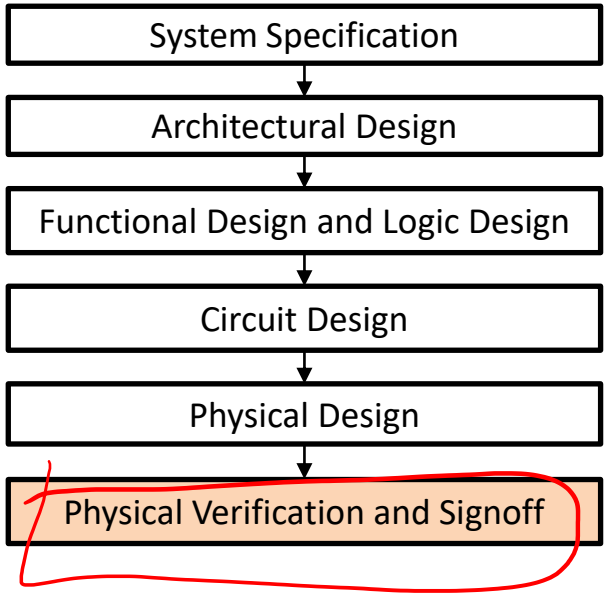


Layout

Physical Design

- Instantiate design components with geometric representations.
- Assign spatial locations (placement) and routing connections (routing) to components.
- Adhere to design rules representing fabrication constraints.
- Consider the impact on performance, area, reliability, power, and yield.

VLSI Design Flow

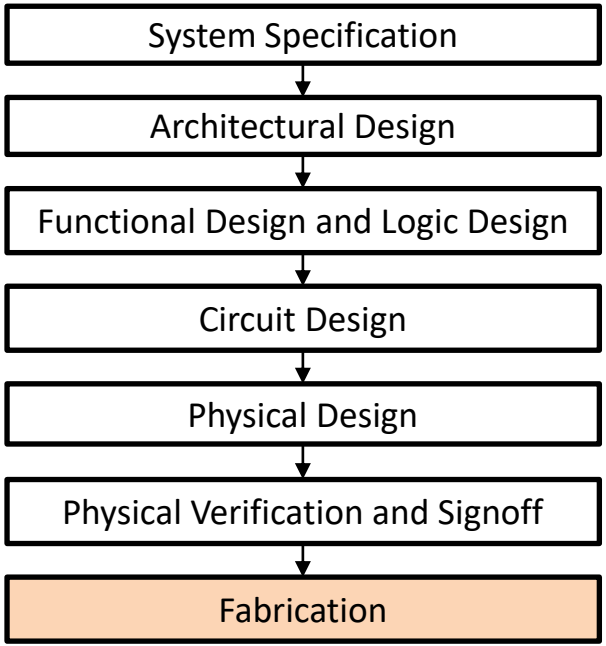


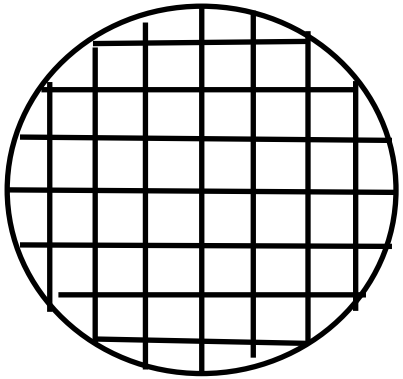
DRC
LVS
ERC
ARC

Physical Verification and Signoff

- Perform **design rule checking** (DRC) to ensure technology constraints are met.
- Conduct **layout vs. schematic** (LVS) checking to verify functionality.
- Extract **parasitic parameters** and verify electrical characteristics.
- Check for potential **antenna effects** and proper power/ground connections.
- Ensure minimal layout changes at this stage.

VLSI Design Flow

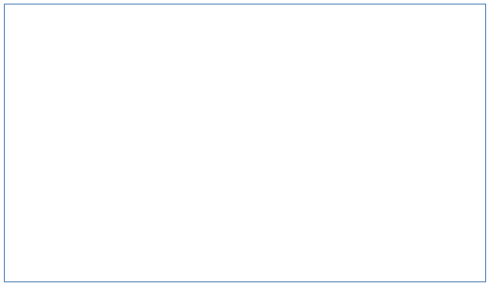




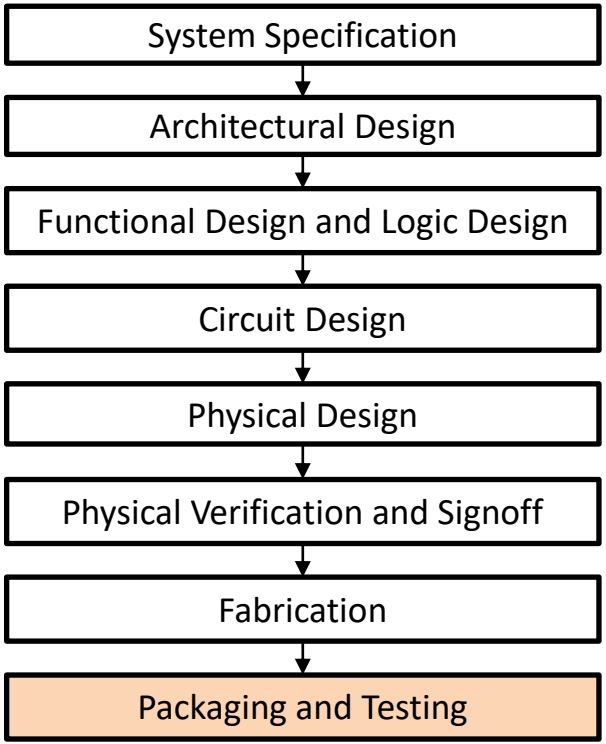
Silicon Wafer

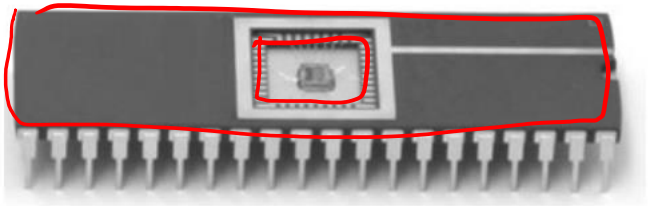
Fabrication

- DRC-clean layout is sent to a silicon foundry for manufacturing (tape out).
- Use photomasks to define patterns on silicon wafers.
- Commonly used wafer sizes (e.g., 200mm to 300mm).



VLSI Design Flow



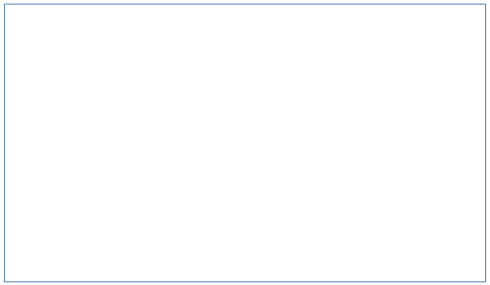


Chip in a 40-pin dual-inline package

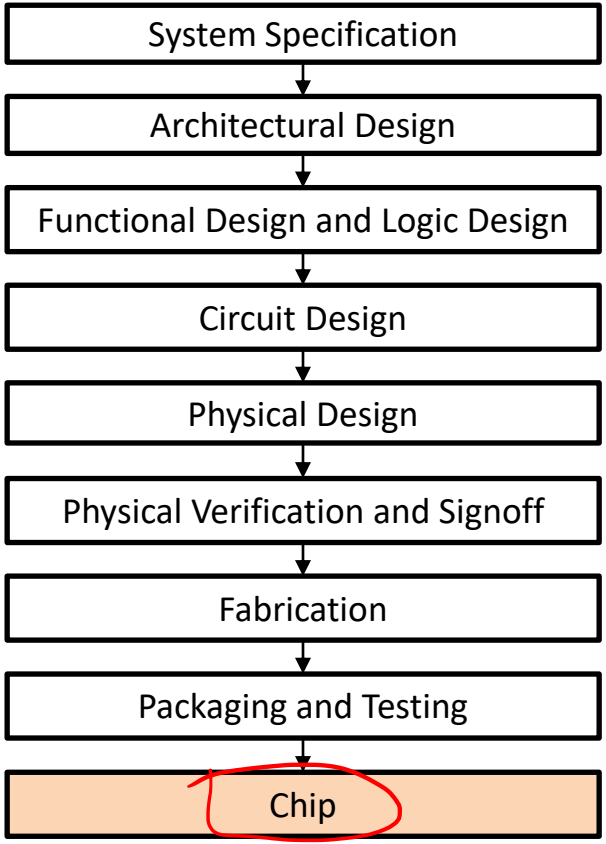
Picture Source: Weste, Neil and Harris, David: CMOS VLSI Design: A Circuits and Systems Perspective

Packaging and Testing

- Choose packaging types such as DIPs, PGAs, or BGAs based on application and cost requirements.
- Describe packaging methods like wire bonding or solder bumps.
- Sequencing of manufacturing, assembly, and testing.
- Testing for functionality, timing, and power.



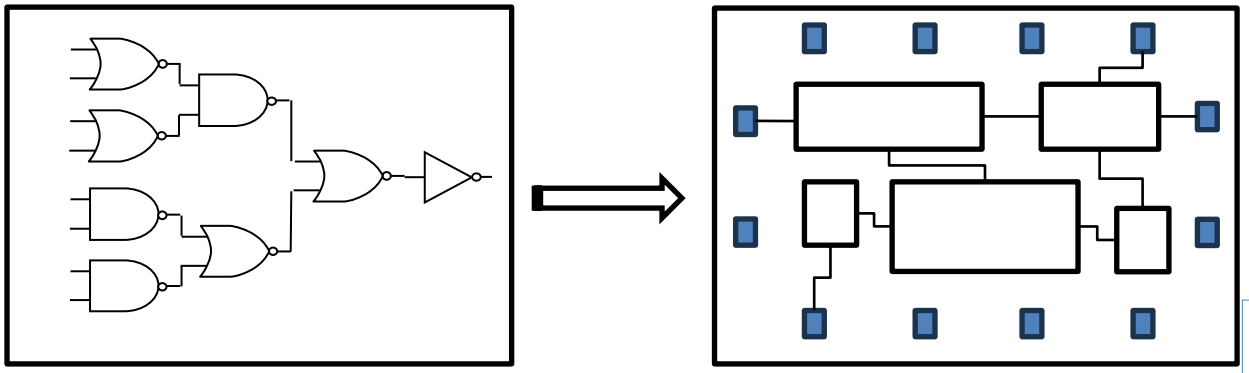
VLSI Design Flow



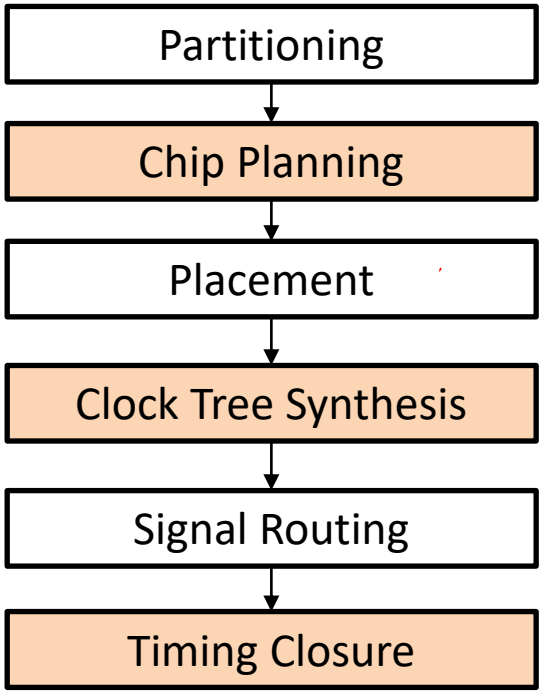
Physical Design Cycle

VLSI Physical Synthesis

- Physical design cycle transforms a circuit diagram into a layout.

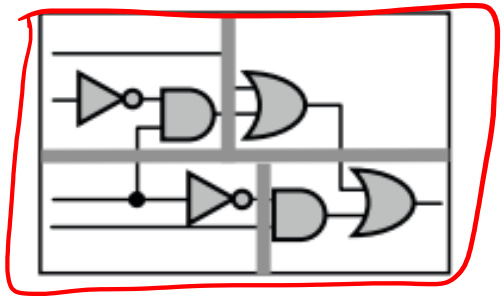


Physical Design Flow



Physical design Flow

- **Partitioning** breaks the circuit into smaller modules.

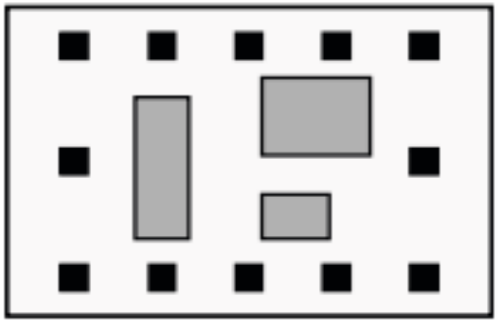


- **Floor planning** determines module shapes and arrangements.

Source: A. B. Kahng et al., VLSI Physical Design: From Graph Partitioning to Timing Closure

Physical design Flow

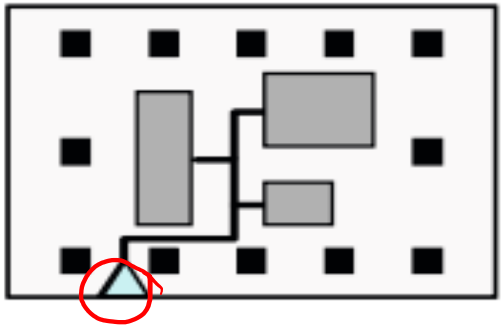
- **Placement** finds spatial locations for cells within each module.



Source: A. B. Kahng et al., VLSI Physical Design: From Graph Partitioning to Timing Closure

Physical design Flow

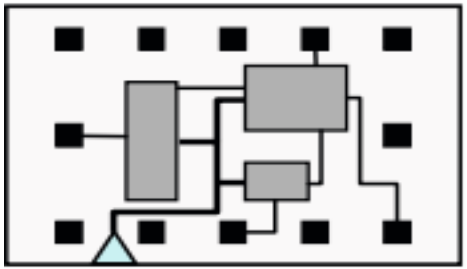
- **Clock Tree Synthesis**:
  - Determines buffering, gating, and routing of the clock signal.
  - Meets prescribed skew and delay requirements.



Source: A. B. Kahng et al., VLSI Physical Design: From Graph Partitioning to Timing Closure

Physical design Flow

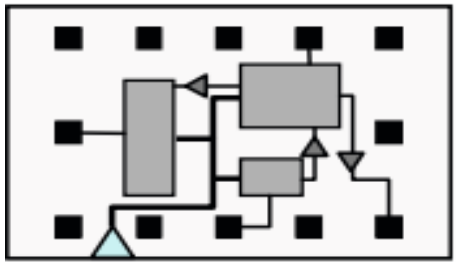
- **Signal Routing**:
  - Power and ground routing distributes power and ground nets.
  - Global routing allocates resources for connections.
    - Example resources include routing tracks in channels and in switch boxes.



Source: A. B. Kahng et al., VLSI Physical Design: From Graph Partitioning to Timing Closure

Physical design Flow

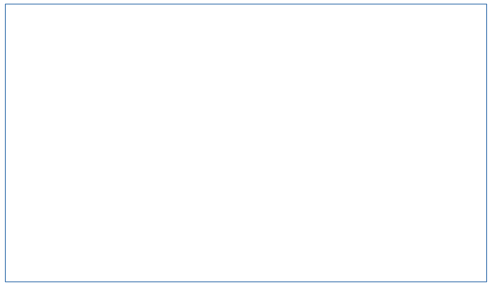
- Detailed routing assigns routes to specific metal layers and routing tracks.
- **Timing Closure:**
  - Optimizes circuit performance through placement and routing.



Source: A. B. Kahng et al., VLSI Physical Design: From Graph Partitioning to Timing Closure

Physical Verification

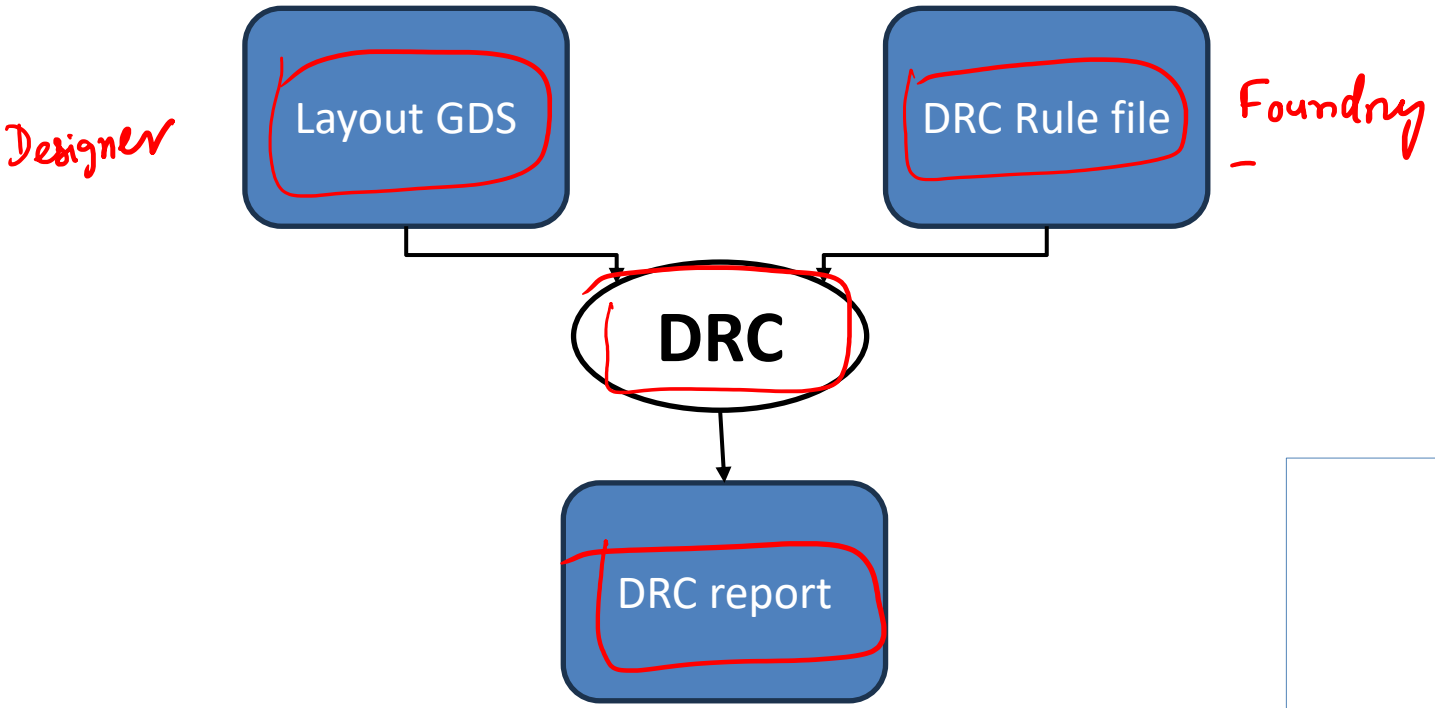
- To ensure correct electrical and logical functionality, the layout must be fully verified after Physical Design.
  - Design Rule Check(DRC)
  - Layout vs Schematic Check(LVS)
  - Electrical Rule Check(ERC)
  - Antenna Rule Check(ARC)



Design Rule Check(DRC)

- **Design Rules**:
  - Geometric constraints on layout to ensure successful fabrication.
  - Must be followed to avoid any manufacturing defects.
  - Minimum allowable drawing dimensions.
- DRC ensures layout data complies with fabrication rules.

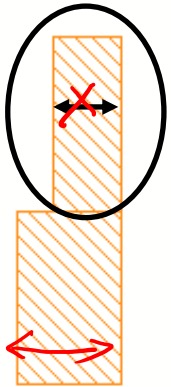
Design Rule Check(DRC)



Design Rule Check

- Design Rule Examples:

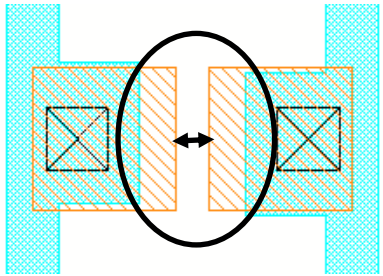
1. Minimum Width



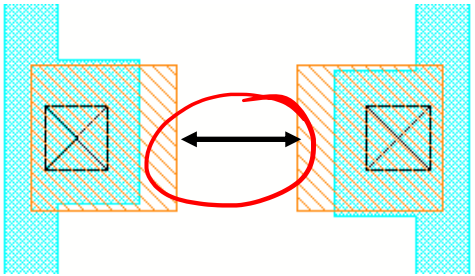
Violation

Fixed

2. Minimum Spacing

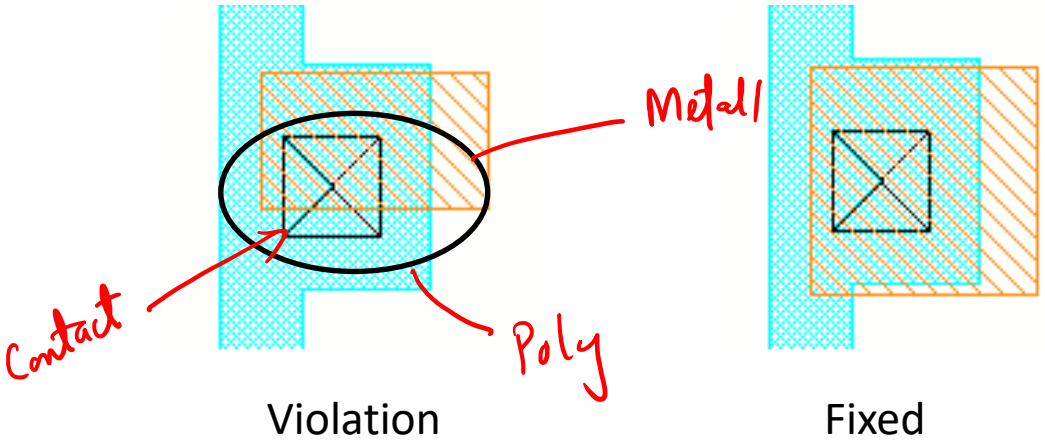


Violation



Fixed

3. Minimum Enclosure/Overlap

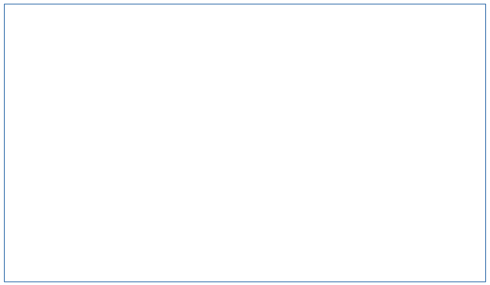


Violation

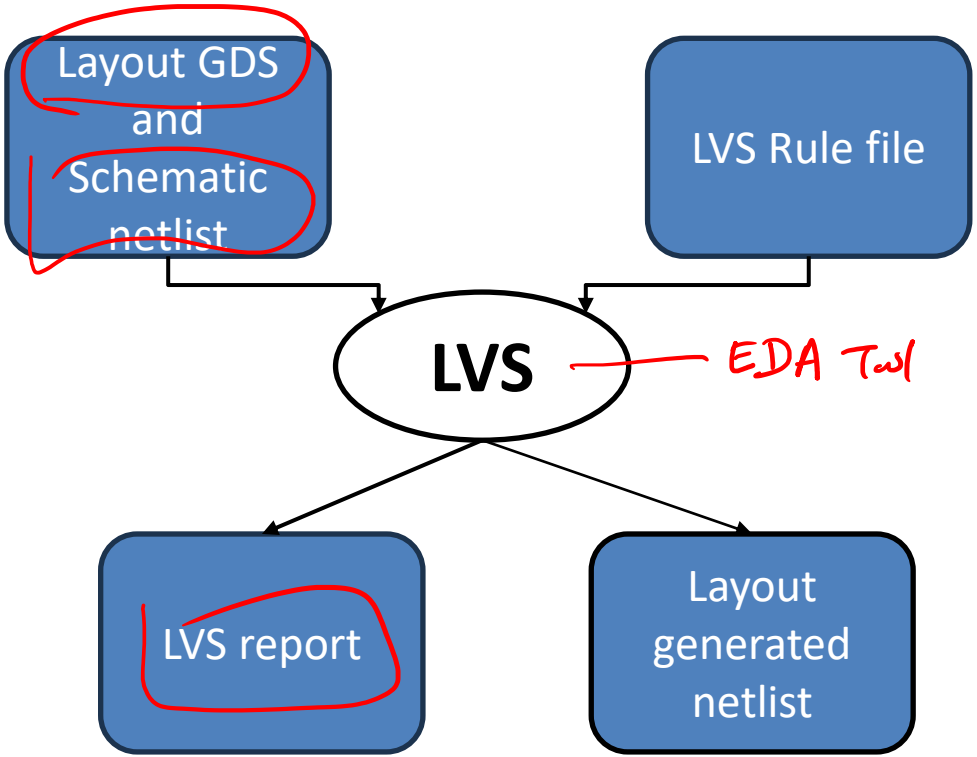
Fixed

Layout vs Schematic (LVS)

- LVS checks that transistors in a layout are connected in the same way as in the circuit schematic.
- Compares extracted netlist from the layout to the original schematic netlist.



Layout vs Schematic (LVS)



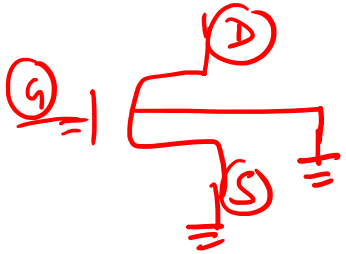
Layout vs Schematic (LVS)

- LVS Errors are classified into two main categories:
  - Compare errors
    - Device mismatch
    - Net mismatch
    - Property errors
    - Port swap errors

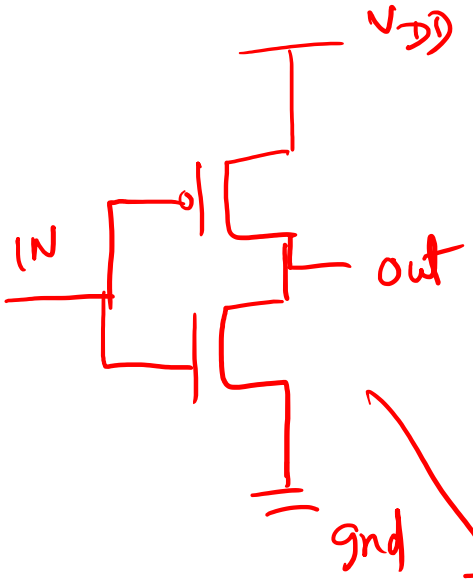
Layout vs Schematic (LVS)

– Extraction errors

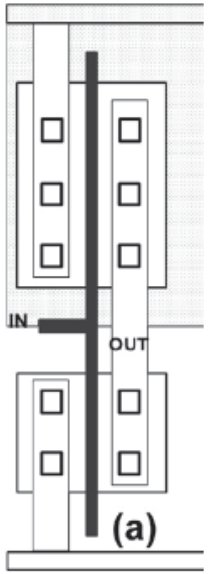
- Missing device terminal
- Extra device terminal
- Device extraction error
- Text short and open



Layout vs Schematic (LVS)



Schematic netlist

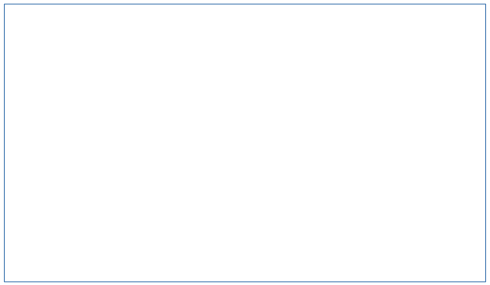


Layout netlist

① Schematic is golden reference

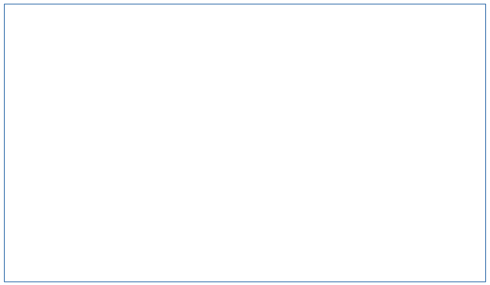
Electrical Rule Check(ERC)

- Verifies the correctness of power and ground connections
- Verifies that signal transition times (slew), capacitive loads, and fanouts are appropriately bounded.



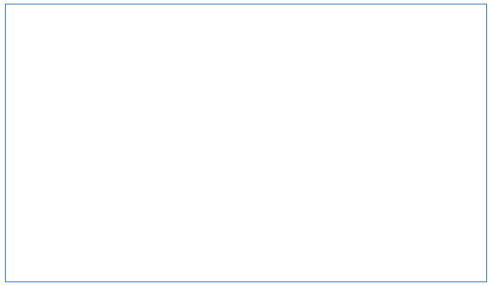
Antenna Rule Check(ARC)

- **Antenna Effect**:
  - Plasma etching of a metal wire connected to a transistor gate can lead to the accumulation of charge, which may damage the gate oxide.
  - This is also called **plasma-induced gate-oxide damage**.



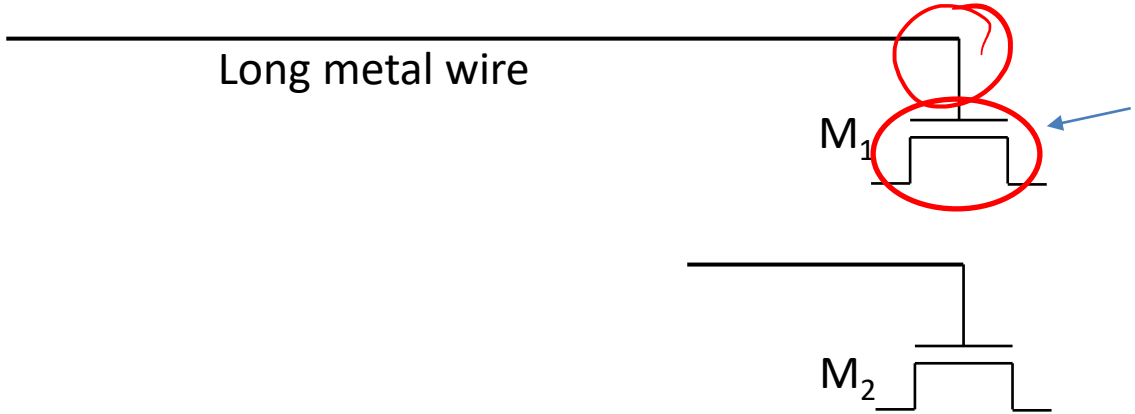
Antenna Rule Check(ARC)

- **Consequences of Antenna Effect:**
  - Increases gate leakage.
  - Changes the threshold voltage.
  - Reduces the life expectancy of the transistor.



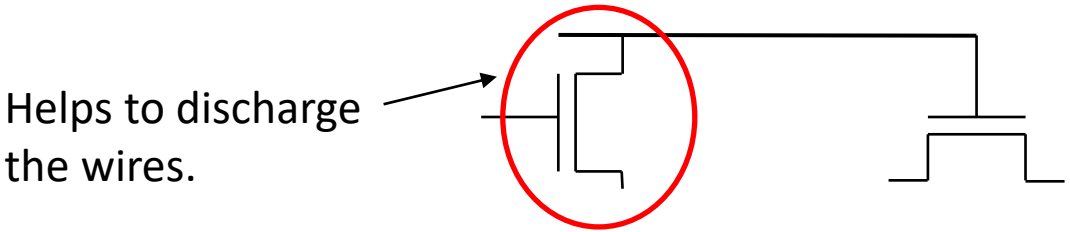
Antenna Rule Check(ARC)

- Longer wires accumulate more charge and are more likely to damage the gates.



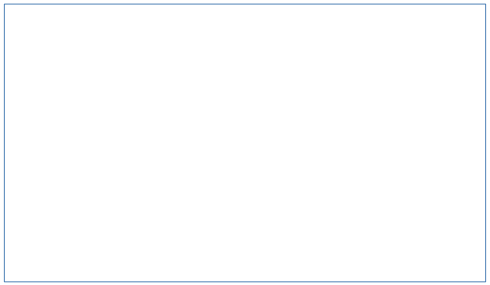
Antenna Rule Check(ARC)

- Diodes formed by **source and drain diffusions** can conduct significant current during the high-temperature plasma etch.
- These diodes help bleed off the charge from wires, preventing gate oxide damage.



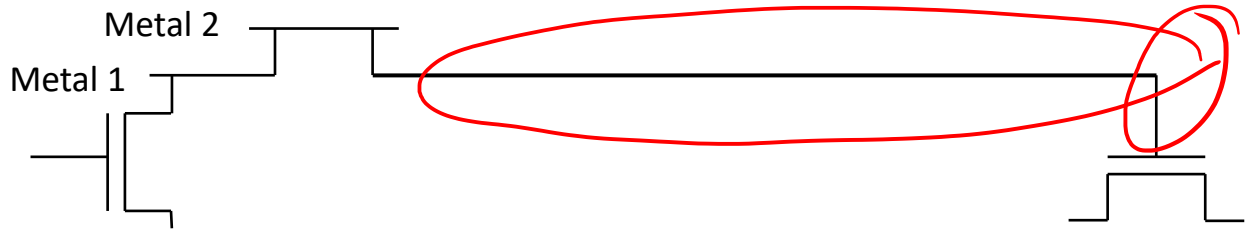
Antenna Rule Check(ARC)

- **Antenna Rules**:
  - Antenna rules specify the maximum metal area connected to a gate without a source or drain connection to act as a discharge element.



Antenna Rule Check(ARC)

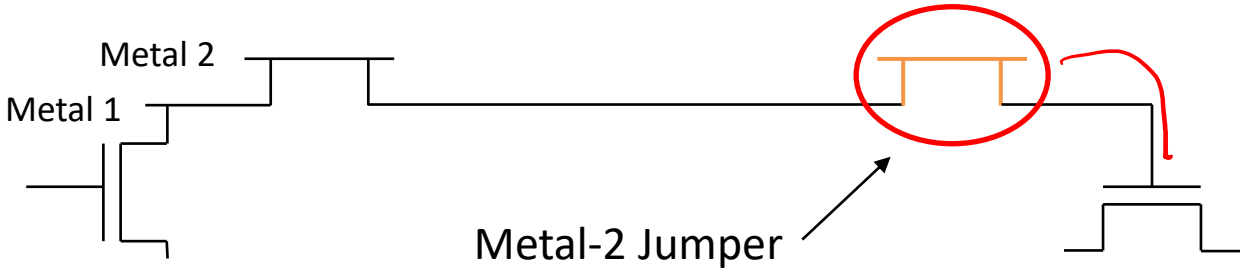
- **Antenna Rule Violations**:



- Long metal 1 connected to the gate of MOSFET can cause damage.

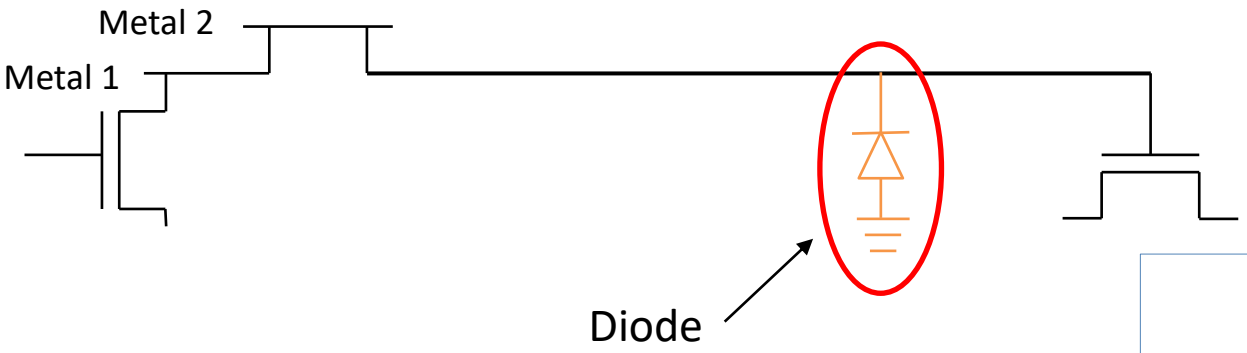
Antenna Rule Check(ARC)

- **Fixing Violation**:
  1. By adding a metal-2 jumper.



Antenna Rule Check(ARC)

- **Fixing Violation**:
  2. By adding a diode.



Thank You