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NPTEL ONLINE CERTIFICATION COURSE

VLSI Physical Design with Timing Analysis

Lecture – 17: STA for Combinational Circuits – I

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Contents

- Types of Path
- Arrival time and Required time
- Output Arrival time for (1) Inverting gate and (2) Non-inverting gate
- Input Required time for (1) Inverting gate and (2) Non-inverting gate

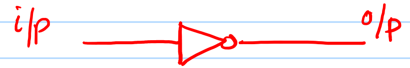
Types of Paths in Combinational Circuits

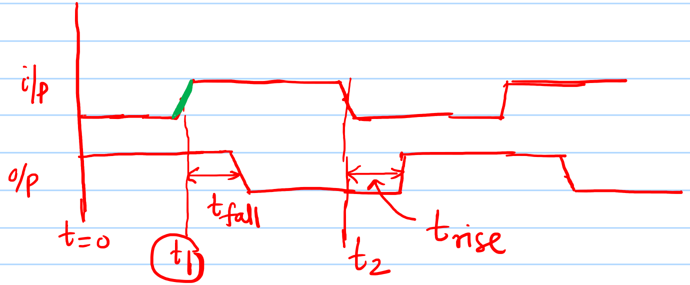
1. Critical Path or longest path in a design (setup check)
2. Short Path or Min data path in a design/circuit (Hold check)
3. False Path

- Arrival time: Actual rise and fall times at different nodes due to the rise and fall delay of the logic gates
- Required time: Rise and fall arrival time required or needed due to the time constraint specified by the circuit designer

Inverting-type of gates:

① Single-input gates:



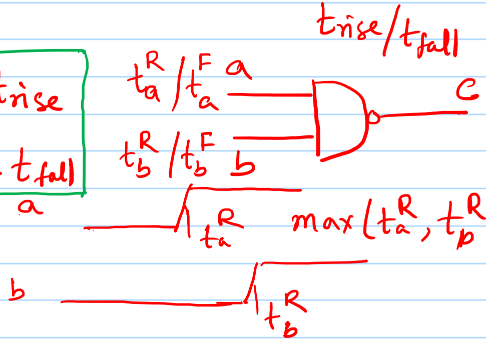


$$o/p\ A.T(rise) = t_2 + t_{rise}$$
$$= i/p\ fall\ A.T. + t_{rise}$$

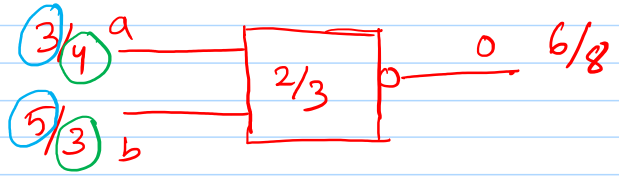
$$o/p\ A.T.(fall) = t_1 + t_{fall}$$
$$= i/p\ rise\ A.T. + t_{fall}$$

② multiple-input gates:

$$o/p\ A.T(rise) = max(input\ fall\ A.T.) + t_{rise}$$
$$o/p\ A.T.(fall) = max(input\ rise\ A.T.) + t_{fall}$$



$$max(t_a^R, t_b^R) = t_b^R$$

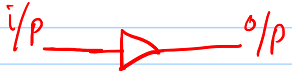


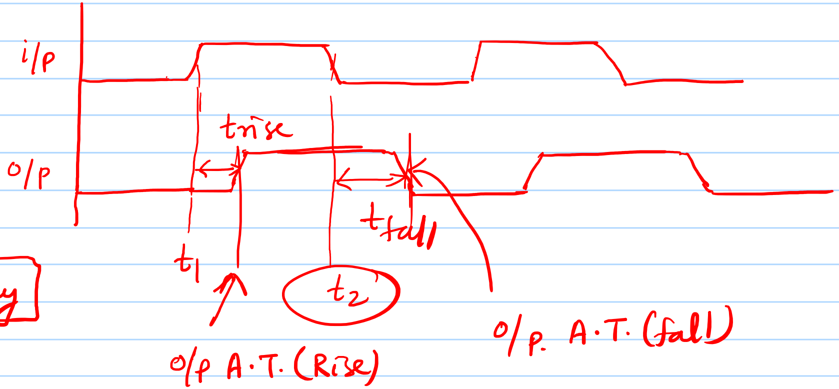
O/P. A.T. (Rise) $= \max(4, 3) + 2 = 4 + 2 = 6$

O/P A.T. (fall) $= \max(3, 5) + 3 = 5 + 3 = 8$

Non-Inverting type of gates

(1) Single-input gate





o/p A.T. (Rise) $= t_1 + t_{rise}$

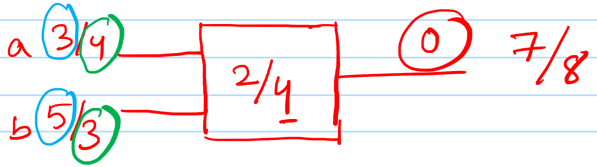
$\boxed{\text{o/p. Rise A.T.} = \text{input Rise A.T.} + \text{Rise delay}}$

o/p A.T. (fall) $= t_2 + t_{fall}$

$\boxed{\text{o/p. fall. A.T.} = \text{input fall A.T.} + \text{fall delay}}$

(2) multiple-input gate

$$\boxed{\begin{aligned} \text{o/p A.T. (rise)} &= \max(\text{input rise A.T.}) + \text{Rise delay} \\ \text{o/p A.T. (fall)} &= \max(\text{input fall A.T.}) + \text{fall delay} \end{aligned}}$$



o/p rise A.T. $= \max(3,5) + 2 = 5 + 2 = 7$

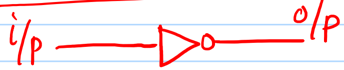
o/p fall A.T. $= \max(4,3) + 4 = 4 + 4 = 8$

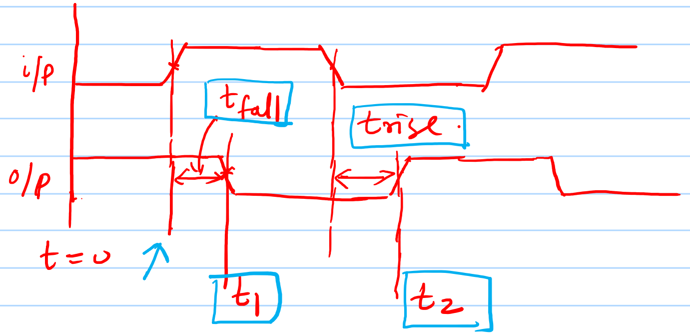
Input A.T. (Rise/fall)

Given Parameters (1) Output A.T (Rise/Fall) (2) Rise delay / Fall delay

(1) Inverting-type gates

(i) Single-input and Single-output





input rise A.T. = $\boxed{t_1}$ − $\boxed{t_{fall}}$

$\boxed{\text{input rise A.T. = output fall A.T. − fall delay}}$

input fall A.T. = $\boxed{t_2}$ − $\boxed{t_{rise}}$

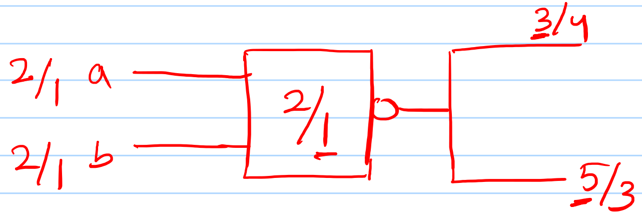
$\boxed{\text{input fall A.T. = Output rise A.T. − Rise delay}}$

(ii) Multiple-Fan-out connected to o/p pin of the gates

input Rise A.T. = Min(output fall A.T.) − fall delay

input fall A.T. = Min(Output rise A.T.) − Rise delay

Ex:-)

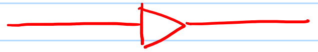


input Rise A.T. (a or b) = min(4, 3) − 1 = 3 − 1 = 2

input fall A.T. (a or b) = min(3, 5) − 2 = 3 − 2 = 1

Non-Inverting gates :

(1) Single-input and Single-output :

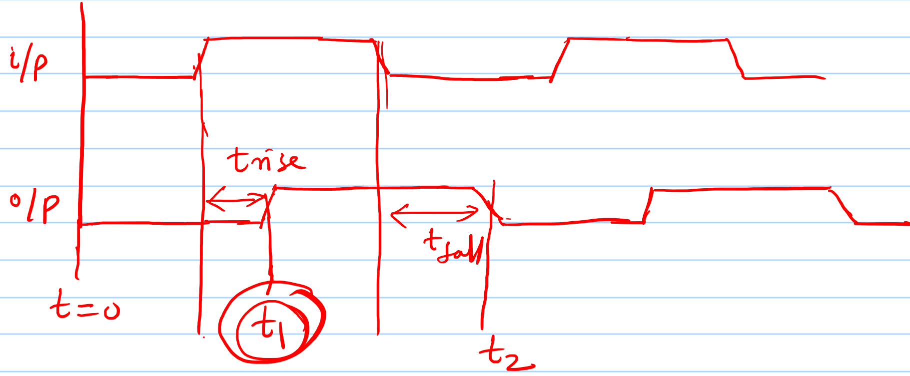


i/p rise A.T. = t_1 − t_{rise}

$\boxed{\text{i/p rise A.T. = o/p. Rise A.T. − Rise delay}}$

i/p fall A.T. = t_2 − t_{fall}

$\boxed{\text{i/p fall A.T. = o/p fall A.T. − fall delay}}$

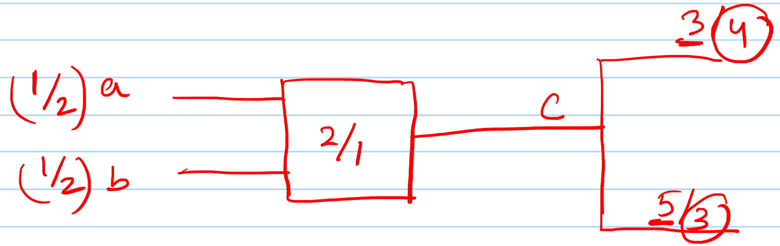


(2) Multiple-Fan-Out

$\boxed{\text{i/p. rise A.T. = min (o/p. Rise A.T.) − Rise delay}}$

$\boxed{\text{i/p fall A.T. = min (o/p fall A.T.) − fall delay}}$

Ex



i/p Rise A.T. = Min (o/p. Rise A.T.) − Rise delay

$= \text{Min}(3, 5) - 2 = 3 - 2 = 1$

i/p. fall A.T. = Min (o/p. fall A.T.) − fall delay

$= \text{Min}(4, 3) - 1 = 3 - 1 = 2$

i/p (Rise / fall) A.T. $= (1/2)$

Thank You