Week 1

1. What is the current generated from an PMOS transistor of Width 400 nm, for a 65 nm technology node (channel length = 50nm) considering mobility of 40 cm^2/V-sec. Consider the PMOS is biased to Vds of -1V, and Vgs of -1V. The current for a PMOS of 200 nm Width is 128.9 µA.

a) 257.8 µA

b) 128.9 µA

c) 112.8 µA

d) 688.9 µA

e) 128.9 mA

f) 112.8 mA

g) 688.9 mA

h) 257.8 mA

2. What is the Vds-saturation voltage for an NMOS transistor of 400 nm width, and biased with Vds of 0.5V, and Vgs of 1V, for 65 nm technology short channel current model ?

a) 0.55 V

b) 0.85 V

c) 0.418 V

d) 0.35 V

e) 0.87 V

f) 0.57 V

g) 0.7 V

h) 0.2 V

3. As Vgs varies from Vgs<0 to Vgs>Vt, what is the correct sequence of the mode of operation?

a) Depletion → Inversion → Accumulation

b) Accumulation → Inversion → Depletion

c) Accumulation → Depletion → Inversion

d) Inversion → Accumulation → Depletion

4. What are the non-ideal effects seen in a MOS due to short channel?

a) Velocity saturation leading to higher Ids for higher Vds

b) Velocity saturation leading to lower Ids for higher Vds

c) Mobility degradation of charge carriers leading to lower Ids for higher Vgs

d) Mobility degradation of charge carriers leading to higher Ids for higher Vgs

5. For Vds>>0, Vd>> Vs, which of the following is true

a) For Vgs<Vt, there is a current through the channel

b) For Vgs>Vt, there is no current through the channel

c) For Vgs>Vt, there is a constant current through the channel, when Vds>=Vgs-Vth

d) For Vgs>Vt, there is a constant current through the channel, when Vds<Vgs-Vth

6. Calculate the effective mobility of a pMOS transistor for 65nm technology node. Vgs=0.9 V, Vt=0.3 V, tox= 1.05 nm

a. 36.37 cm^2/V-sec

b. 95.7 cm^2/V-sec

c. 38.51 cm^2/V-sec

d. 34.65 cm^2/V-sec

7. Which of the following is/are true?

a) Leff vaies with Vds, hence current varies(increases) post saturation in short channel

b) If Vgs-Vt>>Vc, Vds sat is achieved due to pinch-off effect

c) Slope of Ids post saturation is dependent on ro(output resistance)

d) None of the above

8. Calculate values for Vc-p for 65 nm technology node (saturation velocity = 10^7 cm/sec, Vgs= 0.9 V, Vt= 0.3 V, tox= 1.05 nm, L= 50 nm)

a) 2.456 V
b) 2.1996 V
c) 2.077 V
d) 2.354 V

9. Mobility degradation observed in short channel mos devices is due to

a) decrease in channel length

b) decrease in oxide thickness

c) velocity saturation

d) Pinch off at drain region

e) increase in oxide thickness

f) Threshold voltage decreases

g) Threshold voltage increases

h) increase in channel length

10. Which of the following is true?

a. Vth increases with increase in source-body potential

b. Vth decreases with increase in source-body potential

c. Vth increases with decrease in source-body potential

d. Vth decreases with decrease in source-body potential

Solutions:

1) a. 257.8 uA
   Considering all the other parameters for both the mosfet to be same, current is directly proportional to the width.
   I = 2 * 128.9 = 257.8 uA

2) c. 0.418 V
   $V_{ds,sat} = \frac{V_c(V_{gs}-V_t)}{V_c+V_{gs}-V_t} = 0.418$

3) c
   When Vgs<0, the opposite charge carriers are accumulated at the gate , hence MOS is in accumulation mode.
   When Vt>Vgs>0, the positive supply at the gate repels the charge carriers leaving the immobile ions at the gate, which is the depletion mode
   When Vgs>Vt, the minority charge carriers move towards the gate forming a inducting path for current, which is the inversion mode

4) b,c
   At high Vds, Eds increases and the velocity of charge carriers ceases to increase with Eds, hence we see lower Ids than expected for higher Vds.
   Due to carrier scattering at oxide interface, majority carriers slow down in speed and hence lower Ids than expected for higher Vds.

5) C
When the mosfet is in saturation , Vds>Vgs-Vth and Vgs>Vth, there is a constant current flow

6) C. 38.51 cm^2/ V-sec

$$\mu_{effp} = 185/(1 + \frac{Vgs+1.5Vt}{0.338*tox}) \quad \text{cm}^2/\text{V-sec}$$

7) a,c
In short channel MOS, in saturation region, when Vds is very high, the depletion region near drain increases and shortens the effective channel length, because of which current increases. This increase in current, has a slope which is dependent on output resistance.

8) C
Vcp = Ec-p * L
Ecp = $2 * Vsat / \mu_{effp}$

9) b
As the oxide thickness decreases, the vertical electric field due to the gate voltage increases, causing collision of charge carriers at Si-SiO2 interface. This causes mobility degradation.

10) a
Vth increases with increase in source-body potential
As we apply more Vsb, it creates more depletion region near source and hence requires for Vgs to create channel between source and drain, hence Vth increases.