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NPTEL ONLINE CERTIFICATION COURSE

# VLSI Physical Design with Timing Analysis

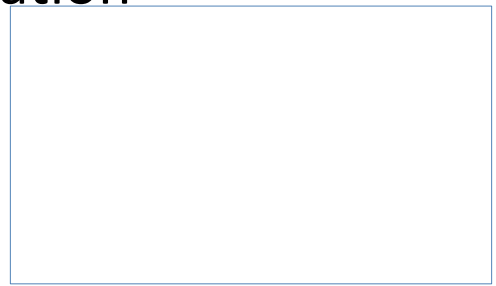
## Lecture – 11: Timing Analysis in Sequential Circuit

**Bishnu Prasad Das**

**Department of Electronics and Communication Engineering**

# Contents

- Setup time and hold time
- Maximum timing analysis ( Setup check)
- Minimum timing analysis ( Hold Check)
- Impact of Process corner on setup and hold Violation
- Solve the issues of setup and hold violation in a manufactured chip

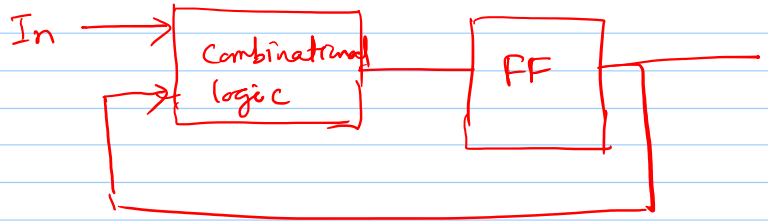


FF delay Parameters

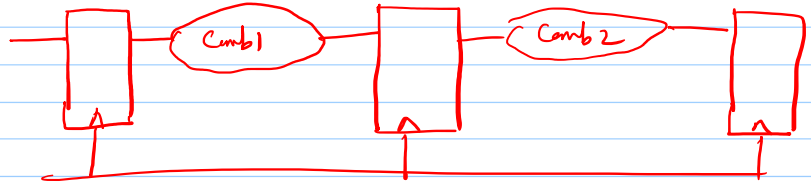
1. $t_{setup}$ = setup time
2. $t_{hold}$ = hold time
3. $t_{ccq} = t_{cq}^{min}$ = Contamination delay bet$^n$ clk and q (Min)
4. $t_{pcq} = t_{cq}^{max}$ = propagation delay bet$^n$ clk and q (Max)
5. $t_{cd} = t_{comb}^{min}$ = Contamination delay of the combinational circuit (Min)
6. $t_{pd} = t_{comb}^{max}$ = Propagation delay of the " " (Max.)

# Sequential Circuits

① Finite state machines (FSM)




② Pipelined Design




③ Shift registers

④ Counters

$t_{pd}$ - Logic Propagation Delay
$t_{cd}$ - Logic Contamination Delay
$t_{pcq}$ - Latch/Flop Clock-to-*Q* Propagation Delay
$t_{ccq}$ - Latch/Flop Clock-to-*Q* Contamination Delay
$t_{pdq}$ - Latch *D*-to-*Q* Propagation Delay
$t_{setup}$ - Latch/Flop Setup Time
$t_{hold}$ - Latch/Flop Hold Time

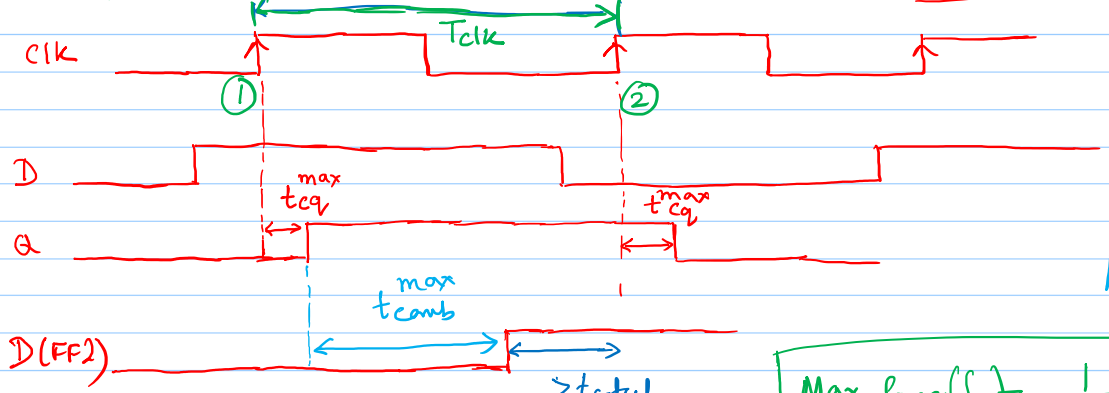
# Max. Timing Analysis

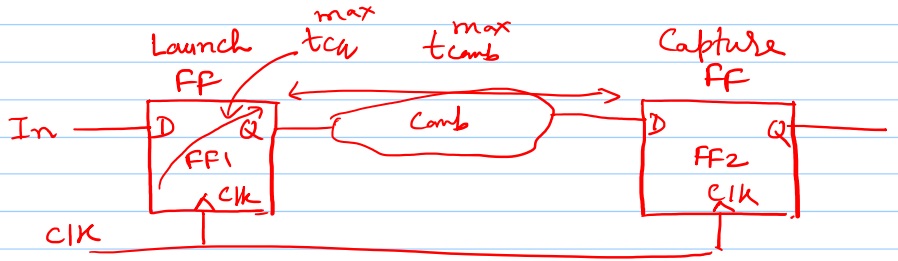
① 1- FF — ① setup time ② hold time ③ clk2q delay

② 2- FFs —

$$T_{clk} \geq t_{cq}^{max} + t_{comb}^{max} + t_{setup}$$

$$T_{clk} \geq t_{pcq} + t_{pd} + t_{setup}$$




① Manufactured chip has setup violation.
→ Slow down the clock speed.

$$\text{Max freq.}\left(f_{max}\right) = \frac{1}{T_{clk}}$$

① NMOS – (S, T, F)
② PMOS – (S, T, F)

Types of corners are ① SS (Slow Slow) ② TT ③ FF ④ FS ⑤ SF

③ Temperature

④ voltage

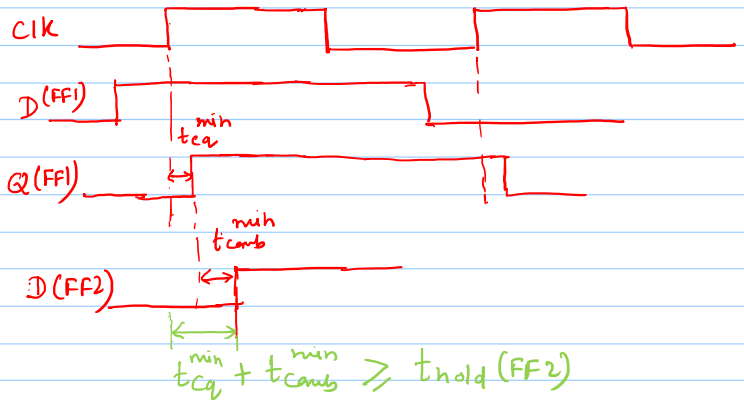
Max timing analysis → SS corner

# Minimum Timing Analysis (Hold check)

① Hold time

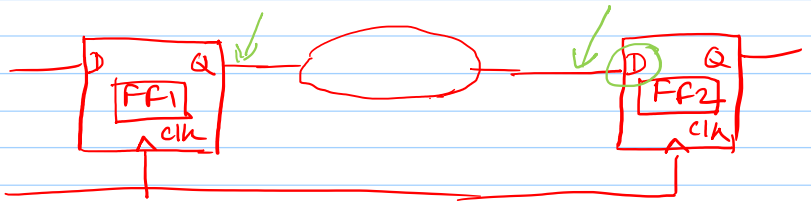
② $t_{ccq} = t_{cq}^{min}$

③ $t_{cd} = t_{comb}^{min}$




① setup time check → 2 clock edges

② hold time check → 1 clock edges




③ hold check → FF corner

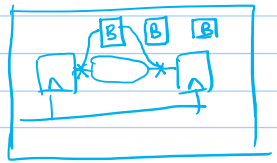
④ Fixing hold violation –

Increase the delay of combinational path

⇓

Buffer insertion.

⑤ Manufactured chip has hold violation



# Thank You