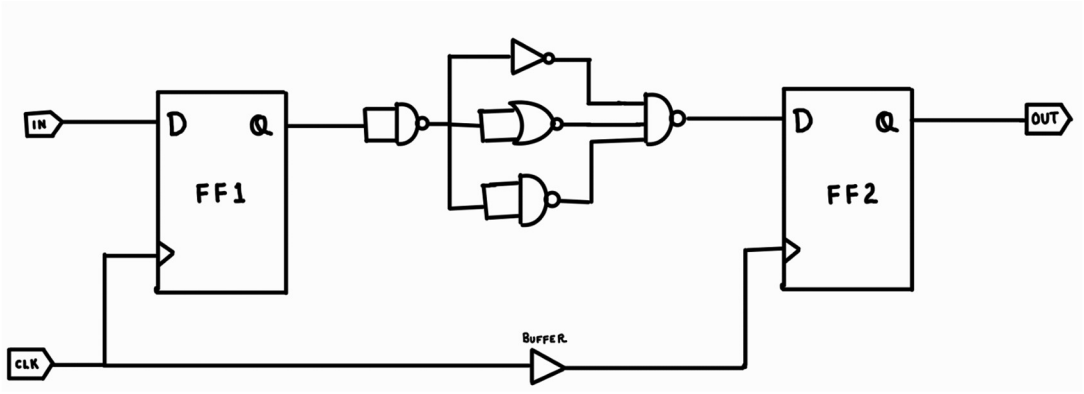
VLSI Physical Design with Timing Analysis

Assignment - 3

Qns 1: Consider the following circuit.



Delay values of Flipflop and Combinational circuit are: t_{setup} = 3ns and t_{hold} = 2ns. The delay of the buffer is t_{buf} = 2ns.

Delay	t_{clk-q}	t_{NAND3}	t_{NOT}	t_{NOR}	t_{NAND2}
Max	3 ns	2.5 ns	1 ns	2.5 ns	2 ns
Min	2 ns	1.5 ns	0.3 ns	1.5ns	1.2 ns

The maximum frequency at which the given circuit can operate without failure is __ (MHz) (Rounded to 2 decimal points)

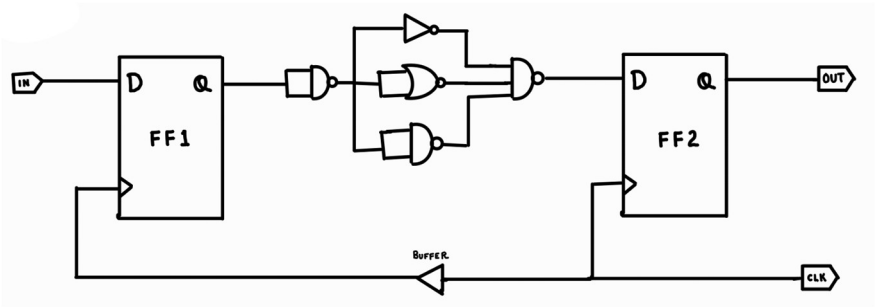
Ans: **90.90 MHz**

Qns 2: Choose the correct hold constraint equation for the circuit given in question 1.

- **a.** 4ns – 2ns $\leq$ 2ns + 3ns
- **b.** 4ns $\leq$ 2ns + 3ns
- **c.** 4ns $\leq$ 3ns + 5.5ns
- **d.** 4ns – 2ns $\leq$ 3ns + 5.5ns

Ans: **(b)**

Qns 3 : Consider the following circuit.



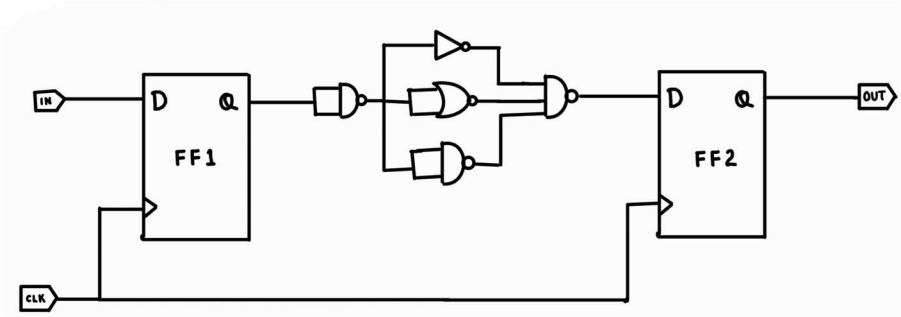
Delay values of Flipflop and Combinational circuit are: t_{setup} = 3ns and t_{hold} = 2ns. The delay of the buffer is t_{buf} = 2ns.

Delay	t_{clk-q}	t_{NAND3}	t_{NOT}	t_{NOR}	t_{NAND2}
Max	3 ns	2.5 ns	1 ns	2.5 ns	2 ns
Min	2 ns	1.5 ns	0.3 ns	1.5 ns	1.2 ns

The maximum frequency at which the given circuit can operate without failure is___(MHz) (Rounded to 2 decimal points)

Ans: 66.67 MHz

Qns 4: Consider the following circuit.



Delay values of Flipflop and Combinational circuit are: t_{setup} = 3ns and t_{hold} = 2ns. The clock period is T_{CLK} = 20ns.

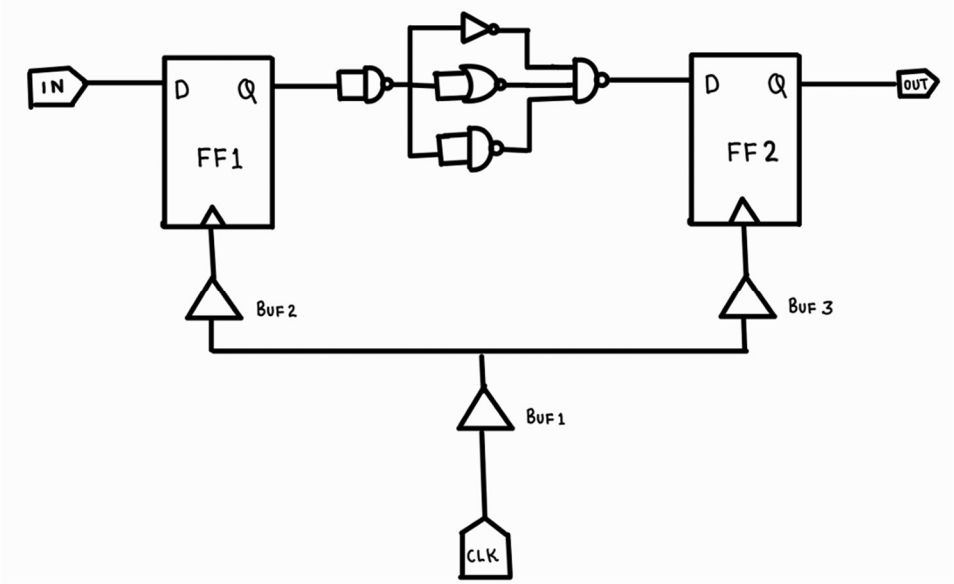
Delay	t_{clk-q}	t_{NAND3}	t_{NOT}	t_{NOR}	t_{NAND2}
Max	3 ns	2.5 ns	1 ns	2.5 ns	2 ns
Min	2 ns	1.5 ns	0.3 ns	1.5 ns	1.2 ns

What is the maximum allowable jitter (t_{jitter}) in the clock signal so that the given circuit works at the given frequency without failure?

a. 0.5 ns
b. 1.5 ns
c. 2.5 ns
d. 3.5 ns

Ans: (b)

Qns 5 : Consider the following circuit.



Delay	$t_{clk\text{-}q}(FF_1)$	$t_{clk\text{-}q}(FF_2)$	t_{NAND3}	t_{NOT}	t_{NOR}	t_{NAND2}
Max	3.8 ns	5 ns	2.5 ns	1 ns	2.5 ns	2 ns
Min	2 ns	2.8 ns	1.5 ns	0.3 ns	1.5 ns	1.2 ns

The delays of buffers t_{buf1} = 1.2ns, t_{buf2} = 0.9ns, and t_{buf3} = 0.7ns. The setup and hold time of both flipflops is t_{setup} = 2ns and t_{hold} = 1ns respectively.

The On-chip variation is modeled as

set_timing_derate -early 0.9

set_timing_derate -late 1.12

set_timing_derate -late 1.08 -cell_check

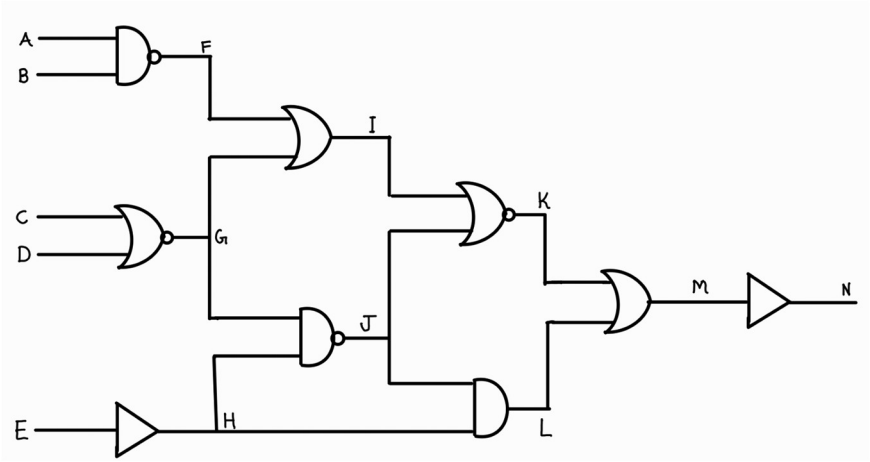
With On-chip variation, the maximum frequency at which the given circuit can operate without failure is ____(MHz) (Rounded to 2 decimal points)

Ans: 67.12 MHz

Qns 6 : The value of common path pessimism (CPP) in the circuit given in question 5 is ___ps

Ans: 264 ps

Qns 7 to 9: Question Label: Comprehension
Consider the following logic circuit.



Logic gate	Rise delay(ns)	Fall delay(ns)
NAND	4	3
NOR	3	5
AND	2	3
OR	5	4
Buffer	1	2

Arrival Time at all primary inputs A, B, C, D and E is 0/0.
Required Time at node 'N' is 16/13
Qns 7: The fall output arrival time at node 'J' is ___(ns)

Ans: 6 ns

Qns 8: The rise input required time at node 'G' in the given circuit is ____ (ns)

Ans: -3 ns

Qns 9: The slack(rise/fall) at node 'H' in the given circuit is _____
- **a.** 7/2
- **b.** 7/-4
- **c.** 0/-4
- **d.** 7/-4

Ans: (c)

Qns 10: Choose the incorrect option(s) about clock skew and clock jitter.
- **a.** Excessive skew can cause timing violations (setup or hold violations) leading to functional errors.
- **b.** Clock skew is non-deterministic in nature while Clock Jitter is deterministic in nature.
- **c.** Clock skew occurs due to noise & instability in clock while clock jitter occurs due to physical layout & propagation delay.
- **d.** Clock jitter can lead to data corruption in high-speed designs.

Ans: (b, c)

SOLUTION

Sol 1.

The max. timing constraint for positive skew is

$$T_{CLK} \geq t_{clk\text{-}q}^{max} + t_{comb.}^{max.} + t_{setup} - t_{buf}$$

$$t_{comb}^{max} = t_{critical} = t_{NAND2}^{max} + t_{NOR}^{max} + t_{NAND3}^{max}$$

$$t_{comb.}^{max} = 2 + 2.5 + 2.5 = 7\,ns$$

$$T_{CLK} \geq 3 + 7 + 3 - 2$$

$$T_{CLK} \geq 11\,ns$$

max. frequency $f_{max} = \frac{1}{T_{CLK}^{min.}}$

$$f_{max} = \frac{1}{11 \times 10^{-9}}$$

$$f_{max} = 90.9\ MHz$$

Sol 2.

Hold timing constraint (min. timing constraint) equation for positive skew:

$$t_{hold} + t_{buf} \leq t_{CLK\text{-}q}^{min.} + t_{comb}^{min.}$$

$$t_{comb}^{min.} = t_{NAND2}^{min.} + t_{NOT}^{min} + t_{NAND3}^{min}$$

$$t_{comb}^{min} = 1.2 + 0.3 + 1.5$$

$$t_{comb}^{min} = 3\,ns$$

now, $2ns + 2ns \leq 2ns + 3ns$

or $4ns \leq 2ns + 3ns$

Sol 3.

In this case, max. timing constraint equation:

$$T_{CLK} \geq t_{CLK\text{-}q}^{max.} + t_{comb.}^{max} + t_{setup} + t_{buf}$$

$t_{comb}^{max} = 7\,ns$ (calculated in solution of Q.1)

$$T_{CLK} \geq 3 + 7 + 3 + 2$$

$$T_{CLK} \geq 15\,ns$$

$$f_{max.} = \frac{1}{T_{CLK}^{min.}} = \frac{1}{15\,n}$$

$f_{max} = 66.67\ MHz$

Sol 4.

Case I: Max. timing analysis considering clock jitter:

$$T_{CLK} \geq t_{CLK\text{-}q}^{max.} + t_{comb}^{max.} + t_{setup} + 2\,t_{jitter}$$

↳ calculated in solution of Q.1

$$20 \geq 3 + 7 + 3 + 2\,t_{jitter}$$

$$t_{jitter} \leq 3.5\,ns$$

Case II: Min. timing analysis considering clock jitter:

$$t_{hold} \leq t_{CLK\text{-}q}^{min.} + t_{comb}^{min.} - 2\,t_{jitter}$$

↳ calculated in solution of Q.2

$$2 \leq 2 + 3 - 2\,t_{jitter}$$

$$t_{jitter} \geq 1.5\,ns$$

Now. max. allowable jitter, $t_{jitter} = \min.(3.5\,ns, 1.5\,ns)$

$t_{jitter} = 1.5\ ns$

Sol 5.

Capture clock path = 1.2 + 0.7 = 1.9 ns

Launch clock path = 1.2 + 0.9 = 2.1 ns

max. data path = $t_{CLK\text{-}Q}^{max} + t_{comb}^{max}$ → calculated in solution of Q.1

max. data path = 3.8 + 7 = 10.8 ns

With OCV:

T_{CLH} + [capture clock path] * (0.9) − t_{setup} * (1.08) ≥ (Launch clock path + max. data path) * (1.12)

$T_{CLH} + 1.9 * 0.9 - 2 * 1.08 \geq (2.1 + 10.8) * 1.12$

$T_{CLH} + 1.71 - 2.16 \geq 14.448$

$T_{CLH} \geq 14.898$ ns

$$f_{max} = \frac{1}{14.898\,n}$$

f_{max} = 67.12 MHz

Sol 6.

CPP = Latest AT @ common point − earliest AT @ common point

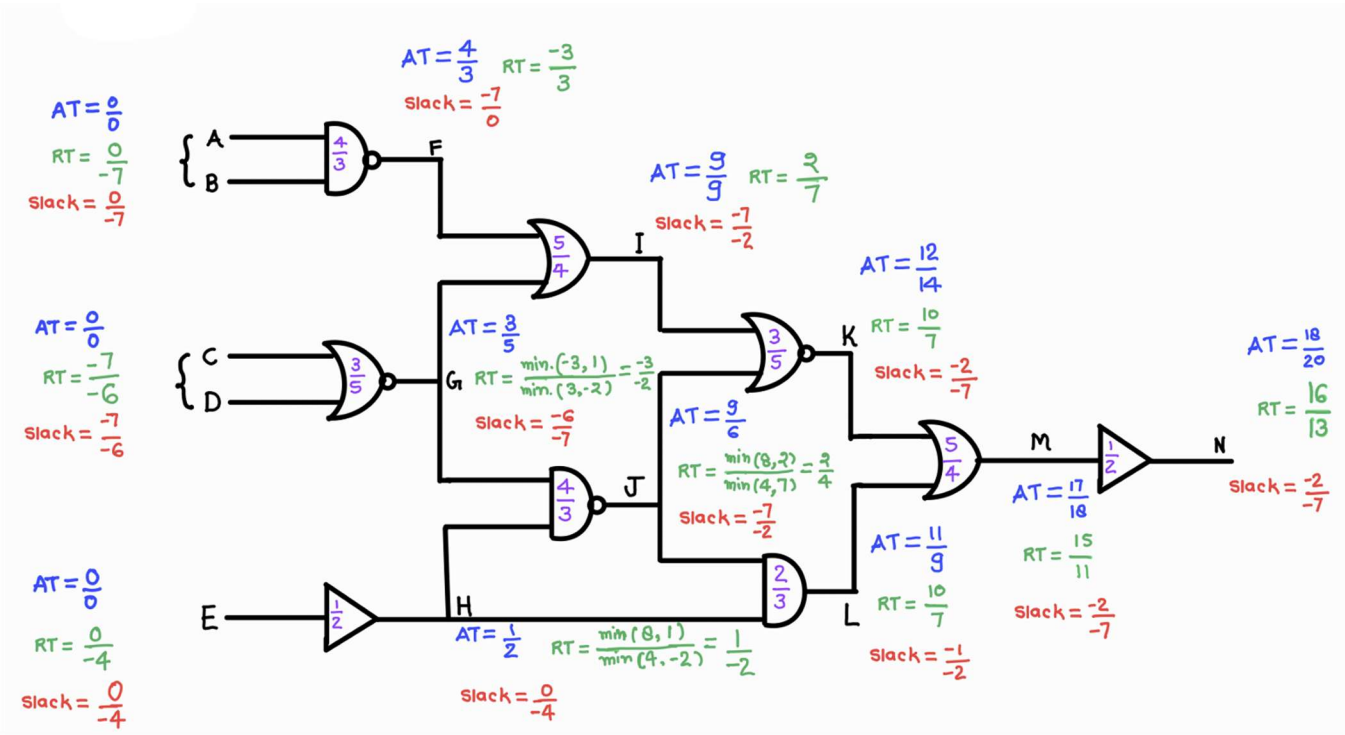
CPP = 1.2 * 1.12 − 1.2 * 0.9

CPP = 0.264 ns

CPP = 264 PS

Sol 7-9.
Equations used in the solution:

For inverting gates:	For non inverting gates:
output rise AT = max(input fall AT) + trise	output rise AT = max(input rise AT) + trise
output fall AT = max(input rise AT) + tfall	output fall AT = max(input fall AT) + tfall
input rise RT = min(output fall RT) – tfall	input rise RT = min(output rise RT) – trise
input fall RT = min(output rise RT) – trise	input fall RT = min(output fall RT) – tfall



Sol 10. Refer lecture notes