IIT ROORKEE

FREE ONLINE EDUCATION swayam शिक्षित भारत, उन्नत भारत

NPTEL ONLINE CERTIFICATION COURSE

VLSI Physical Design with Timing Analysis

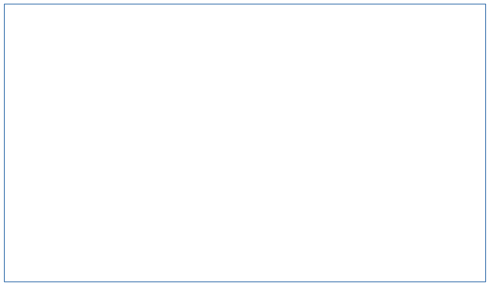
Lecture – 14: Timing Constraints in Sequential Circuit with Clock jitter

Bishnu Prasad Das

Department of Electronics and Communication Engineering

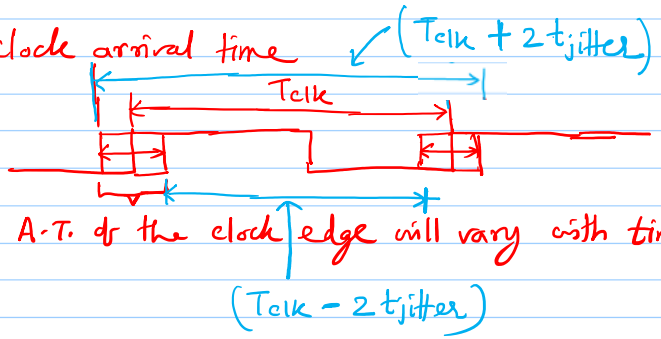
Contents

- What is clock Jitter?
- Max. timing analysis (Setup check) with Clock Jitter
- Min. timing analysis (Hold Check) with Clock Jitter
- Sources of Clock skew and Jitter



What is clock jitter?

① Clock jitter is basically a temporal variation of clock arrival time
↓
w.r.t. to time

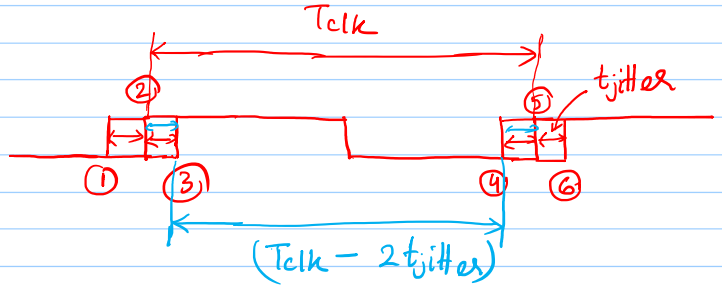


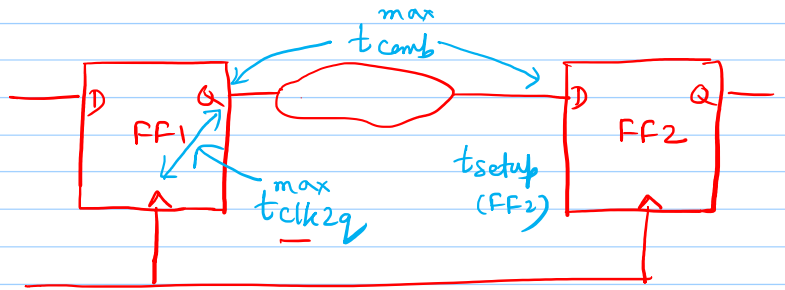
② Clock period will increase or decrease with time
↑ ↑
(Tclk + 2tjitter) (Tclk - 2tjitter)

③ Cycle-to-cycle jitter ⇒ Timing varying deviation of a single clock period.

④ It can be modelled using a zero mean random variable.

Max timing Analysis with jitter





Tclk will be increase by 2tjitter

Tclk ↑ ⇒ fclk ↓

Case I (without jitter) → FF1 samples at edge ② / FF2 " at edge ⑤ } → Tclk

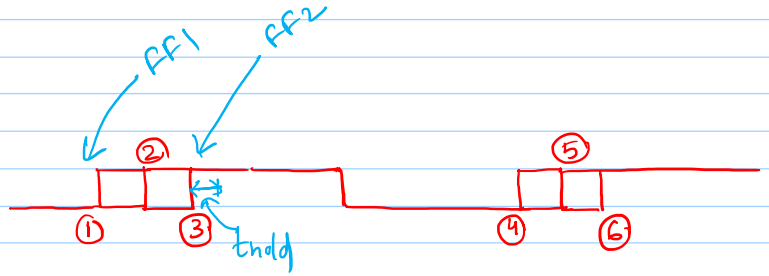
$$T_{clk} \geq t_{clk2q}^{max} + t_{comb}^{max} + t_{setup}$$

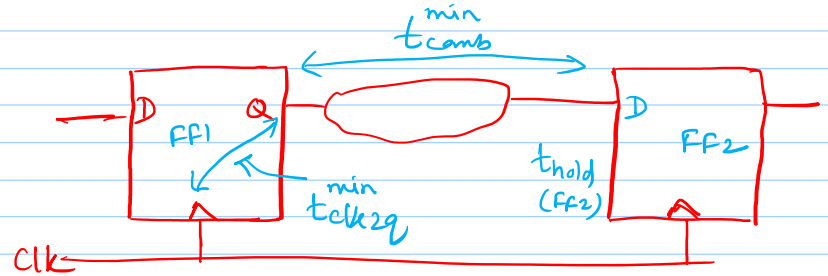
Case II (with jitter) → FF1 samples at edge ③ ← late / FF2 " " " ④ ← early } $T_{clk} - 2t_{jitter}$

$$T_{clk} - 2t_{jitter} \geq t_{clk2q}^{max} + t_{comb}^{max} + t_{setup}$$

$$T_{clk} \geq t_{clk2q}^{max} + t_{comb}^{max} + t_{setup} + 2t_{jitter}$$

Min. Timing analysis with jitter





Case I (without jitter) : Edge ② is considered by FF1 and FF2

$$t_{hold} \leq t_{clk2q}^{min} + t_{comb}^{min}$$

Case II (with jitter) : FF1 should sample at edge ① } Worst case
FF2 " " " " ③ } condition

$$t_{hold} \longrightarrow (t_{hold} + 2t_{jitter})$$

$$t_{hold} + 2t_{jitter} \leq t_{cq}^{min} + t_{comb}^{min}$$

degrade the hold requirement

$$\boxed{t_{hold} \leq t_{clk2q}^{min} + t_{comb}^{min} - 2t_{jitter}}$$

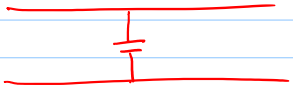
Sources of skew and jitter:

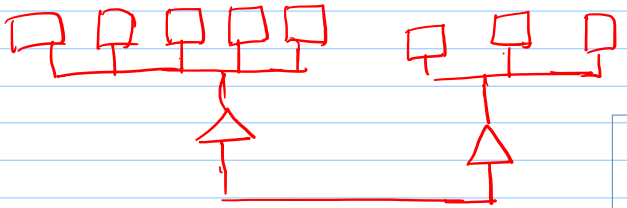
Clock jitter

① Clock generation → PLL → VCO → clock jitter
→ crystal

② Power supply variation → Clock generation circuit → clock jitter

③ Coupling to Adjacent lines — Clock jitter.





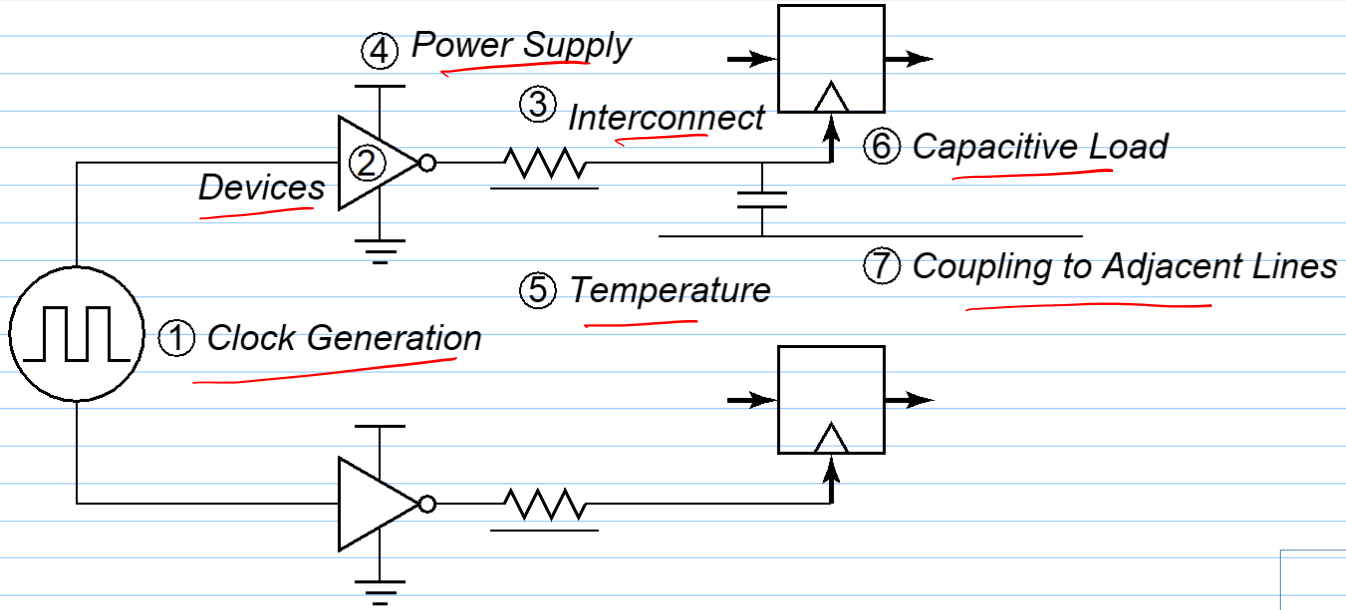
Clock skew

① Interconnect variation.

② Device or Process Variation (Within die) — (i) RDF (ii) LER (iii) OTV

③ Capacitive load variation.

④ Temperature variation (Clock jitter and skew)



Sources of clock uncertainty

Source : Digital Integrated Circuits: A Design Perspective by Jan Rabaey, Anantha Chandrakasan, Borivoje Nikolic

Thank You