PMOS Transistor

Instructor – Dr. Madhav Rao

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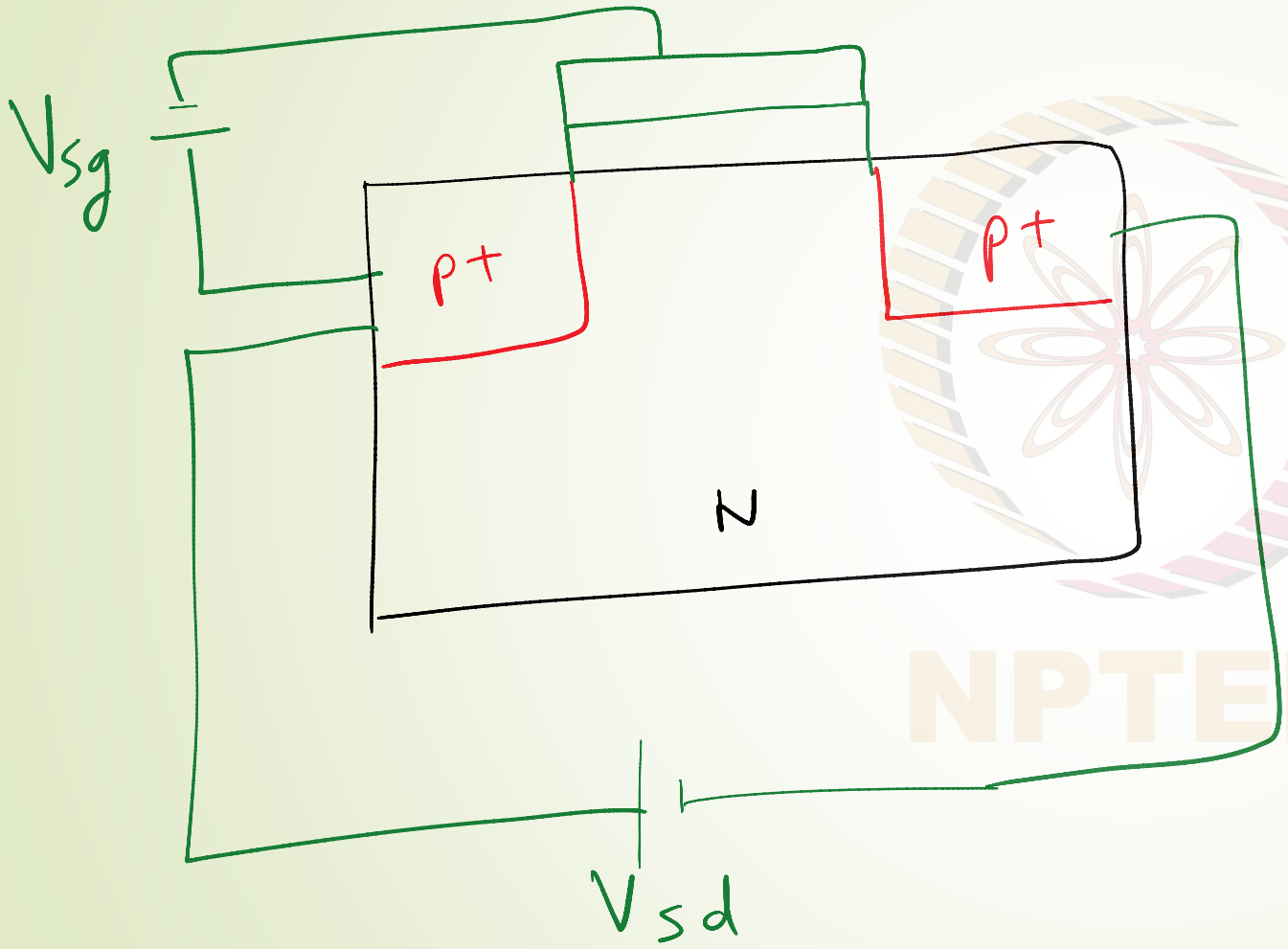
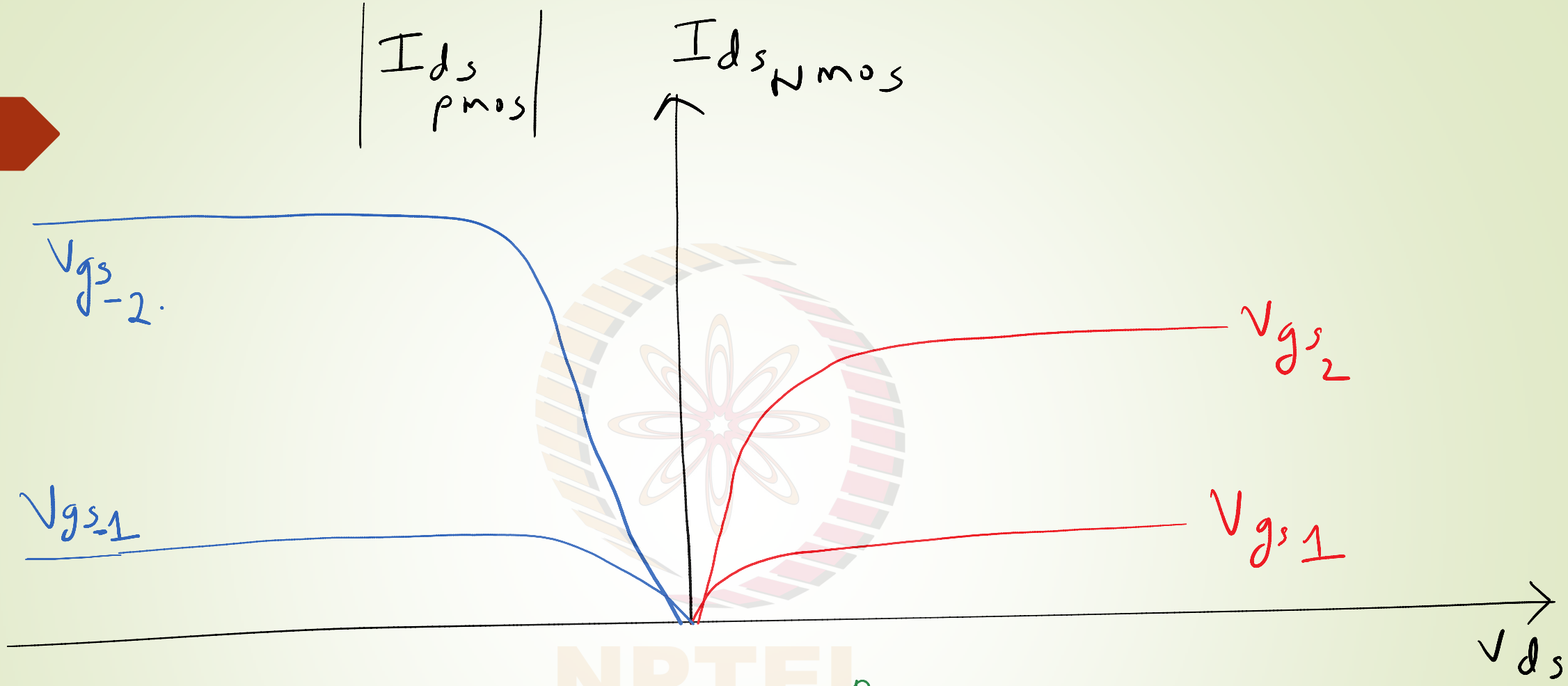


$$I_{sd}\ \text{Linear} = \beta\left(V_{sg} - |V_t| - \frac{V_{sd}}{2}\right)V_{sd}$$

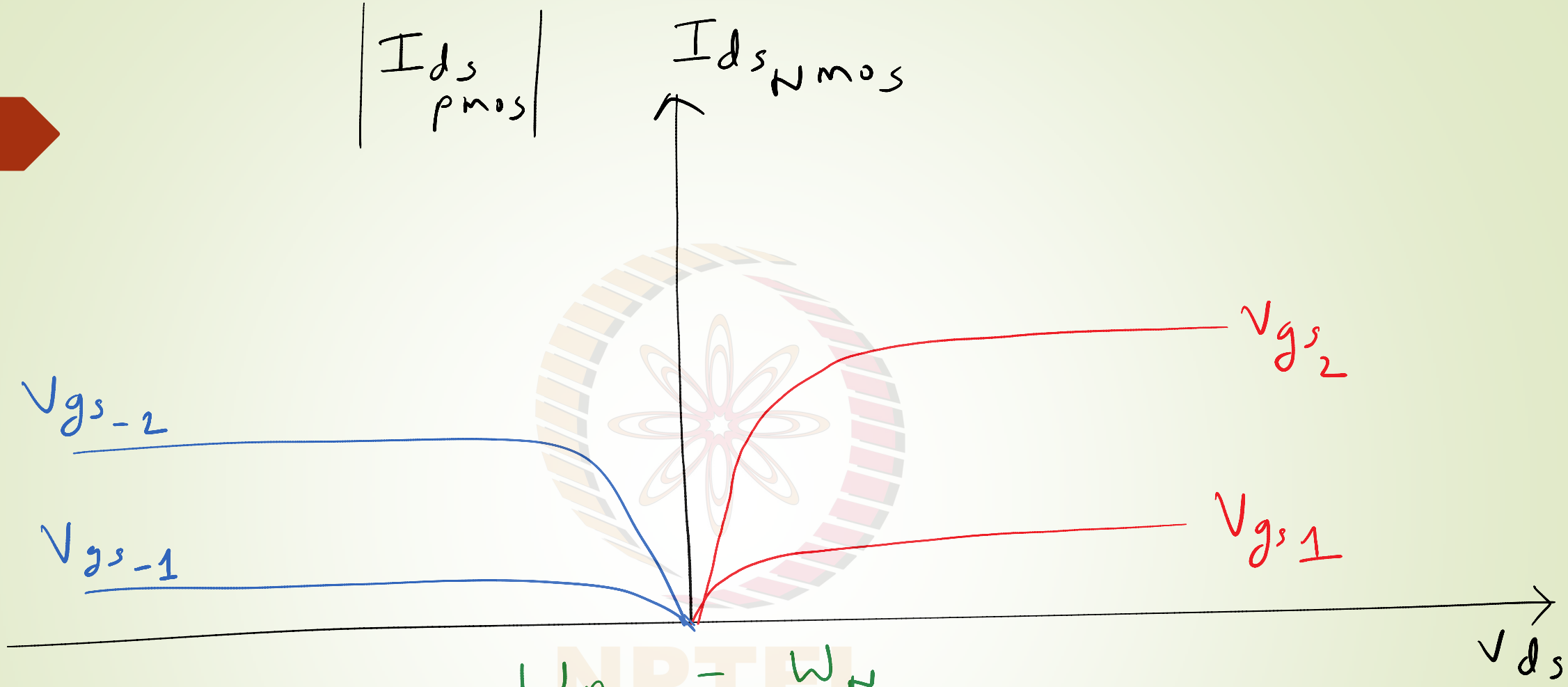
$$I_{sd}\ \text{Saturation} = \frac{\beta}{2}\left(V_{sg} - |V_t|\right)^2$$

$$\boxed{V_{t\,pmos} = -0.3\ V}$$



$$\beta_P > \beta_N$$

$$\mu_p C_{ox} \frac{W}{L} > \mu_N C_{ox} \frac{W}{L}$$



$$W_p = W_N$$

$$L_p = L_N$$

$$C_{ox_p} = C_{ox_N}$$

$$\boxed{\mu_p < \mu_N}$$

Long Channel (Ideal) Model parameters for 65 nm Technology node

Long Channel Model for **65 nm Technology Node: NMOS Transistor**

Mobility = μ = 80 cm^2/v-sec

Vt = 0.3V

t_{ox} = 1.05 nm

W/L = 4/2, unless any other Width is given are asked to be estimated.

Lamda = 2λ = 50 nm

Long Channel Model for **65 nm Technology Node: PMOS Transistor**

Mobility = μ = 40 cm^2/v-sec

Vt = 0.3V

t_{ox} = 1.05 nm

W/L = 4/2, unless any other Width is given are asked to be estimated.

Lamda = 2λ = 50 nm