



IIT ROORKEE



NPTEL ONLINE
CERTIFICATION COURSE

VLSI Physical Design with Timing Analysis

Lecture – 12: Timing Constraints in Sequential Circuit with Clock Skew

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- What is clock skew?
- Types : Positive Skew and Negative Skew
- Max. timing constraint (Setup check) with Clock Skew
- Min. timing constraint (Hold Check) with Clock Skew



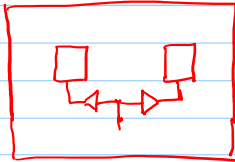
What is Clock Skew?

① The difference of the arrival time of the clock signal at the input of two consecutive FFs in a design \rightarrow Clock skew

② Reasons of clock skew (i) interconnect delay

(ii) Buffer delay

③ The clock skew occurs due to spatial variation:
Space

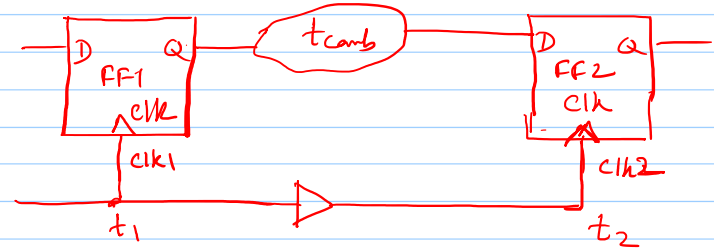
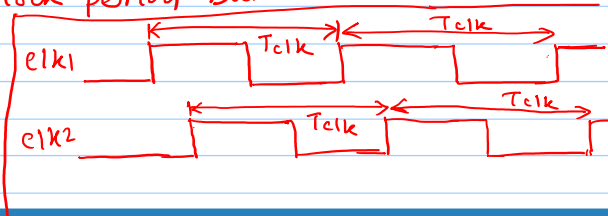


④ The clk skew \rightarrow Static variation in the path length.

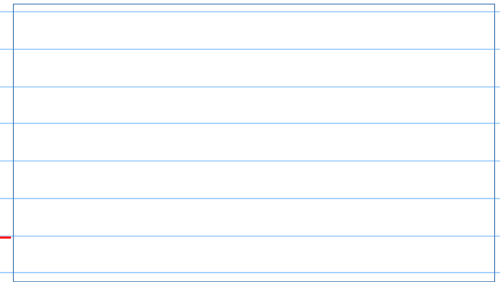
⑤ The clock skew does not change the clock period but

it will shift the phase of the clock

⑥ skew is constant from cycle to cycle

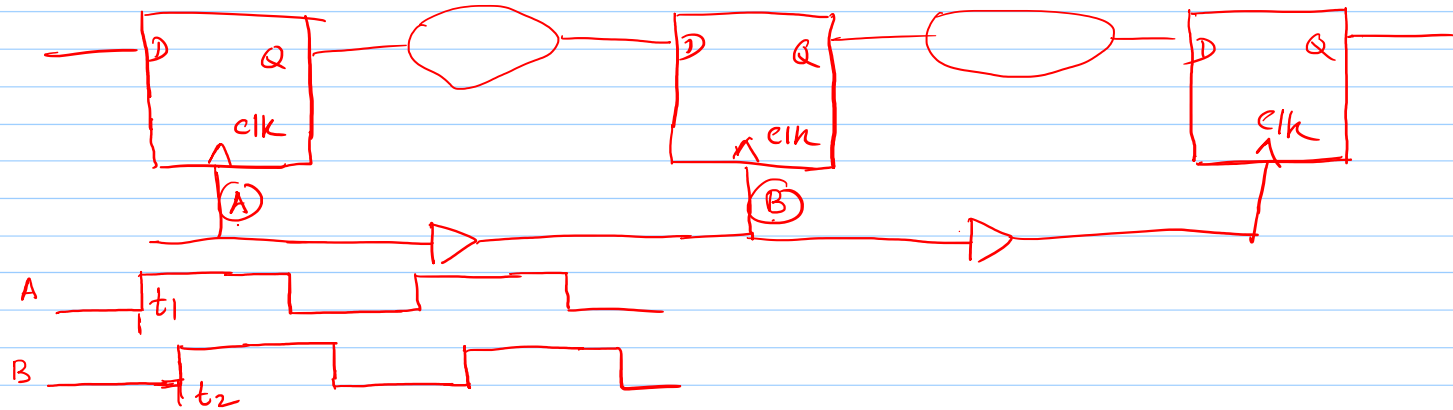


$$\begin{aligned}\text{Clock skew} &= (t_2 - t_1) \\ &= (\text{Capture clock A.T} - \text{Launch clock A.T})\end{aligned}$$

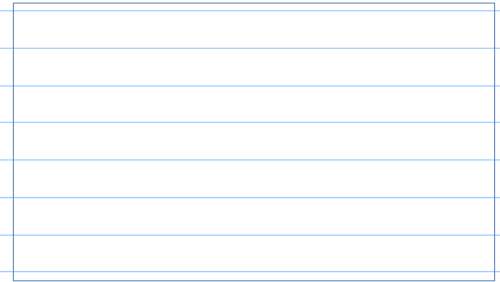


Types of Clock skew :

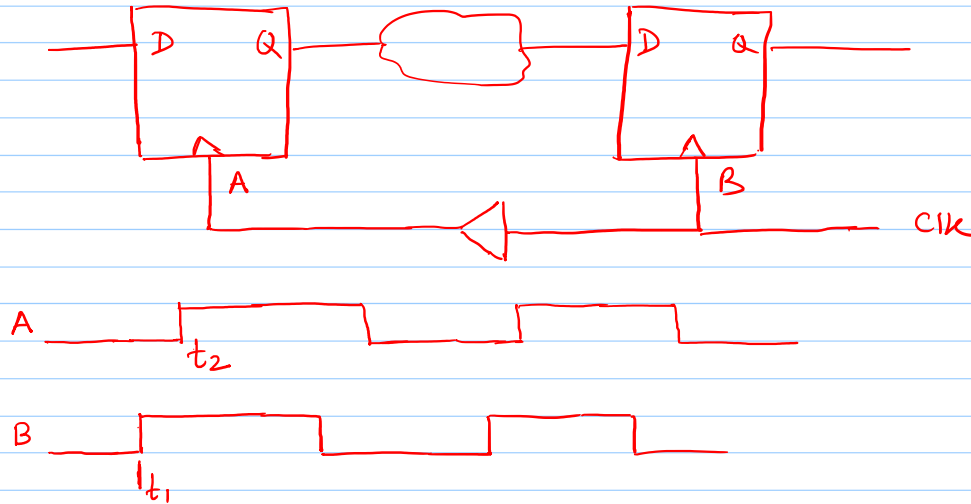
① Positive Skew : The clock and data signals are moving in same direction



$$\begin{aligned} \text{skew} &= \text{Capture clk A-T.} - \text{launch clk A-T} \\ &= (t_2 - t_1) \end{aligned}$$



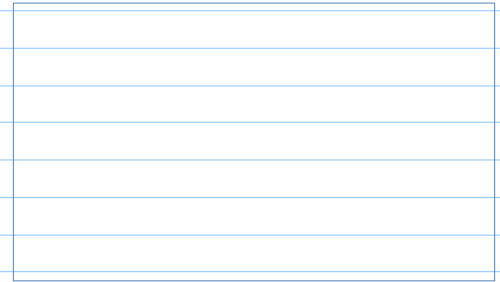
② Negative Skew: Data and clock signal is moving in "opposite" direction.



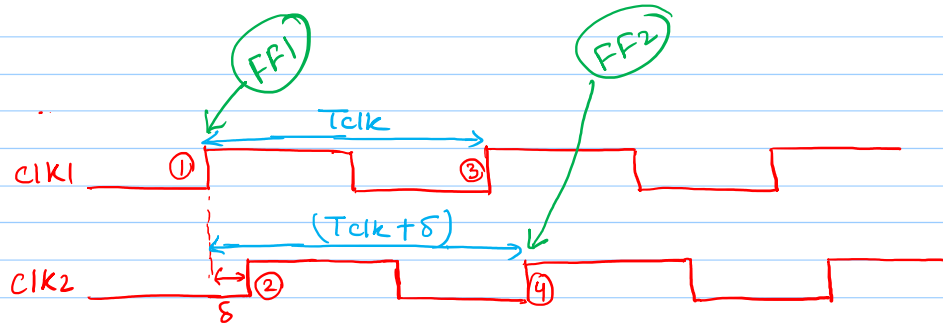
$$\text{Skew} = \text{Capture clk A.T.} - \text{Launch clk A.T.}$$

$$= (t_1 - t_2)$$

Skew is -ve



Max. Timing analysis considering skew (δ is +ve)



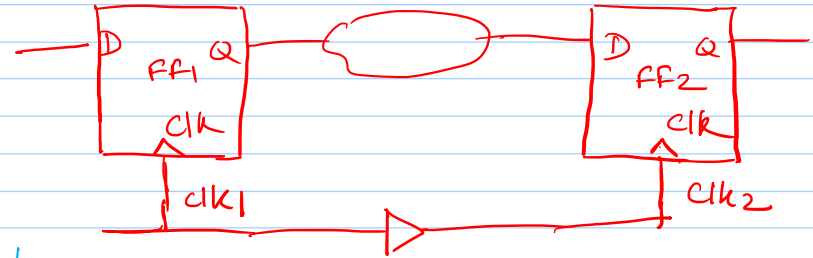
FF1 samples the data at edge 1

FF2 samples the data at edge 4

Positive skew improves the speed of the design

$$\Rightarrow t_{cq}^{\max} + t_{comb}^{\max} + t_{setup} - \delta \leq T_{clk}$$

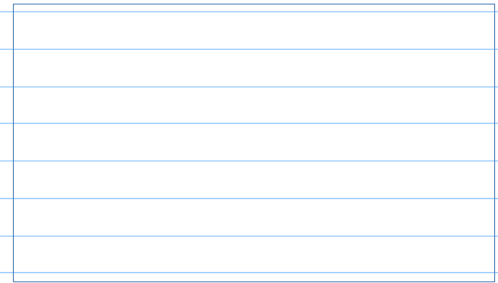
$T_{clk} \downarrow \Rightarrow f_{clk} \uparrow$



Case I (without skew): $t_{cq}^{\max} + t_{comb}^{\max} + t_{setup} \leq T_{clk}$

Case II (with skew): $t_{cq}^{\max} + t_{comb}^{\max} + t_{setup} \leq (T_{clk} + \delta)$

\Rightarrow



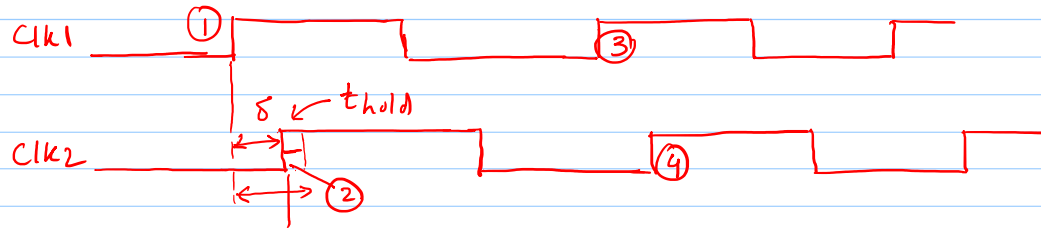
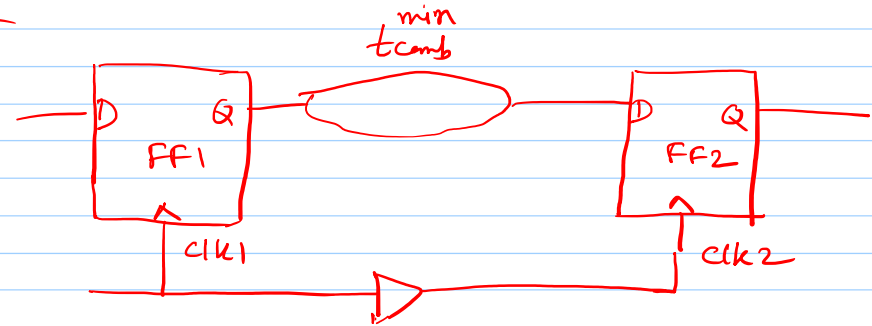
Minimum timing Analysis Consider +ve skew

① Case I (without clock skew)

The hold time of FF2 is t_{hold}

$$t_{hold} \leq t_{cq}^{min} + t_{comb}^{min}$$

② Case II (with clock skew)



hold check \Rightarrow clk1 - ①
clk2 - ②

The hold time of the FF2 is $(t_{hold} + \delta)$

$$(t_{hold} + \delta) \leq t_{cq}^{min} + t_{comb}^{min}$$

\Rightarrow +ve skew degrades the hold requirements

Thank You

