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NPTEL ONLINE CERTIFICATION COURSE

VLSI Physical Design with Timing Analysis

Lecture – 15: STA considering OCV and CRPR (Setup check)

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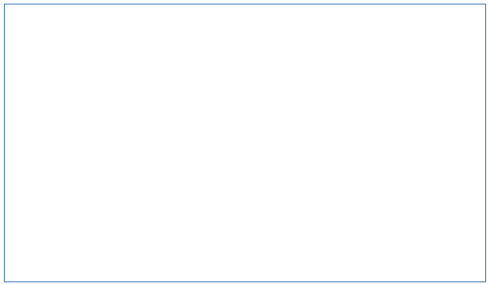
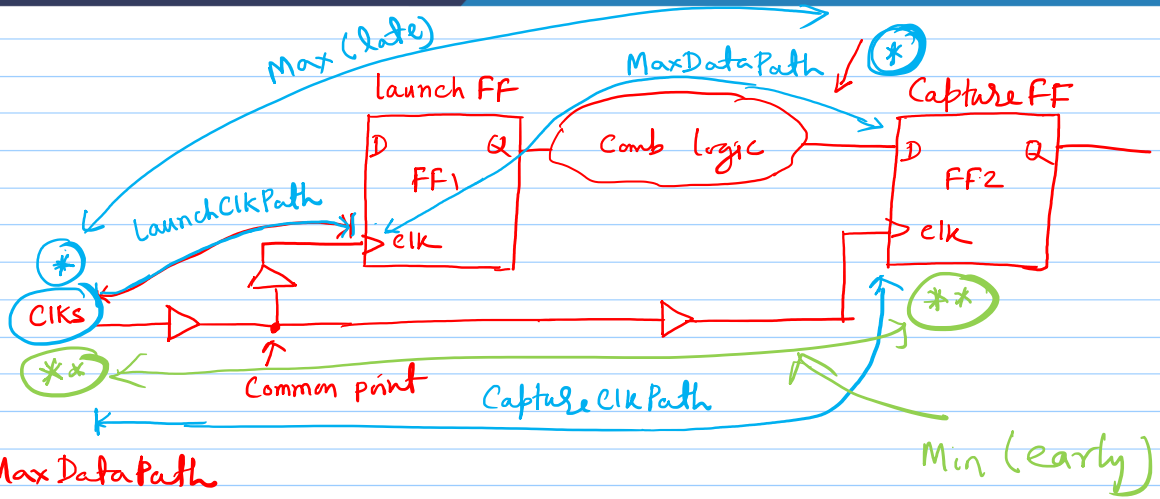
- Launch FF and Capture FF
- Max. timing analysis (Setup check) without variation
- Max. timing analysis (Setup check) with on-chip variation (OCV)
- Max. timing analysis (Setup check) with OCV + CRPR



FF1 – launch FF

FF2 – Capture FF



Data Arrival time = LaunchClkPath + MaxDataPath

Data Required time = Clock Period + Capture Clock Path – t_{setup} (FF2)

For Setup time check

Data arrival time ≤ Data Required time

In general case (with clock buffer in clock tree)

$DAT \leq DRT$

$$\text{LaunchClkPath} + \text{MaxDataPath} \leq \text{ClockPeriod} + \text{CaptureClockPath} - t_{setup} \quad \text{——(1)}$$

Special case (No buffer in clock tree) ← Ideal cond^n

$\text{LaunchClkPath} = 0$

$\text{CaptureClkPath} = 0$

$$\text{MaxDataPath} \leq \text{ClockPeriod} - t_{setup}$$

$$\Rightarrow t_{clk2q}^{max} + t_{comb}^{max} \leq T_{clk} - t_{setup}$$

$$\Rightarrow \boxed{t_{clk2q}^{max} + t_{comb}^{max} + t_{setup} \leq T_{clk}} \quad \text{——(2)}$$

Slack = How much delay margin we have?

Slack = DRT − DAT

Case I

If Slack = 0, ⇒ DRT = DAT

We have Min clock period / Max clock frequency

Case II

If slack is +ve,

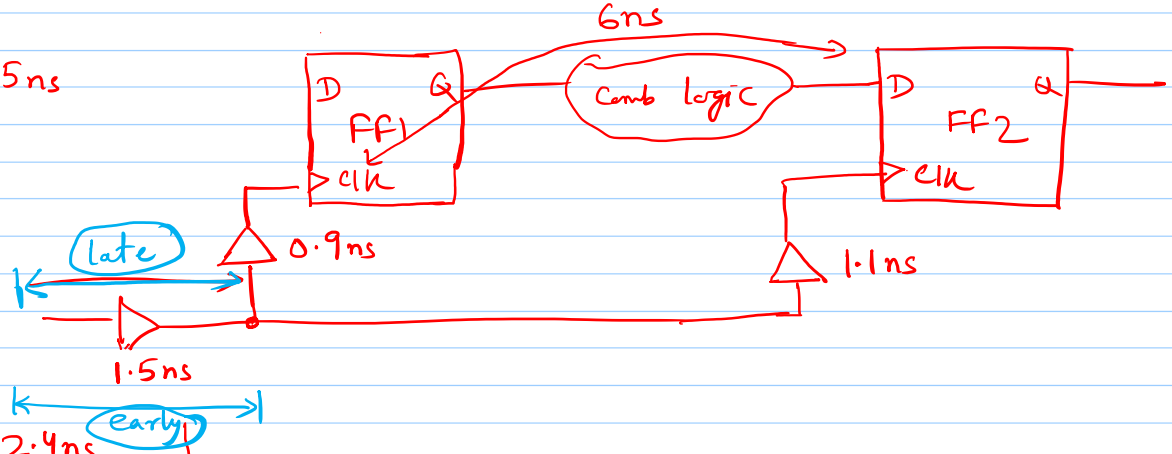
We have extra Margin

Case III

If Slack is −ve, ⇒ setup violation.

Ex-1

$T_{clk} = 7.2\ ns$; $t_{setup} = 0.5\ ns$



Case I (without variation)

Launch Clock Path = 1.5 ns + 0.9 ns = 2.4 ns

Max Data Path = 6 ns

Capture Clk Path = 1.5 ns + 1.1 ns = 2.6 ns

t_{setup} = 0.5 ns

DAT = 2.4 + 6 = 8.4 ns

$DRT = \frac{7.2}{T_{clk}} + 2.6 - 0.5 = 9.3\ ns$

Slack = DRT − DAT

= 9.3 − 8.4 = 0.9 ns

Slack is +ve and setup requirement is satisfied

Case II (with OCV) – On-chip Variation — local variation (inside the same die)

set_timing_derate -early 0.85

set_timing_derate -late 1.1

set_timing_derate -late 1.05 -cell_check ← tsetup and thold

Launch Clk Path = 2.4 ns × 1.1 = 2.64 ns

Max Datapath = 6 ns × 1.1 = 6.6 ns

Capture Clock Path = 2.6 ns × 0.85 = 2.21 ns

tsetup = 0.5 ns × 1.05 = 0.525 ns

DAT = 2.64 + 6.6 = 9.24 ns

DRT = 2.21 ns − 0.525 ns + 7.2 ns = 8.885 ns

Slack = DRT − DAT = −0.355 ns ← Setup violation.

Case III (with OCV + CRPR)

CRPR – Clock Reconvergent Pessimism Removal.

CPP – is the delay difference along this common portion of the clock tree due to the different derating for launch and capture clock paths

CPP = latest A.T @ commonpoint – Earliest A.T @ CommonPoint

$= (1.5_{ns} \times 1.1 - 1.5ns \times 0.85) = 0.375ns$

Slack = $-0.355ns + 0.375ns = 0.02ns = 20ps$

Now Slack is +ve. ⇒ No setup violation

Slack = DRT – DAT

Slack (ocv + CRPR)

= Slack (ocv) + CPP

Thank You