Week 2

Q1. For an Inverter of 2:1 size, evaluate the current when an input voltage of 2 V is applied for a 5V rail voltage. Consider Vt for NMOS, and PMOS as 0.3 V, and -0.3 V respectively, and Widths of 100 nm, and 200 nm for NMOS and PMOS transistors, with channel length of 50 nm, tox=1.05 nm and mobility of 80 cm2/v-sec, and 40 cm2/v-sec for NMOS and PMOS transistors.

a) 128 µA
b) 256 µA
c) 512 µA
d) 760 mA
e) 128 mA
f) 760 µA
g) 1.28 mA
h) 7.60 mA

Q2. For a skewing ratio of 0.30 for a 65 nm technology node with a rail voltage of 1V as per the long-channel model, which is the more appropriate statement ?

a) Threshold-voltage of inverter is 0.5 V.
b) Threshold-voltage of inverter is 1 V.
c) Threshold-voltage of inverter is 0 V.
d) Threshold-voltage of inverter falls in between 0.5 and 1 V
e) Threshold-voltage of inverter falls in between 0.5 and 0 V
f) Threshold-voltage of inverter is above 1 V
g) Threshold-voltage of inverter is below 0 V
h) Threshold-voltage of inverter is 0.3 V

Q3. For an inverter designed to have a threshold voltage of 0.636 V for a rail voltage of 1 V in a 65 nm technology node, which of the following is the most appropriate statement related to the designed inverter ?

a) The inverter is unskewed

b) The inverter is asymmetric

c) The inverter is low skewed

d) The inverter is continuously switching

e) The inverter noise margin remains similar to the unskewed inverter's.

f) The inverter shows ZERO short-circuit power.

g) The inverter shows ZERO dynamic power.

h) The inverter is high skewed.

Q4. For an N-cascaded NMOS pass transistors where all the gates are tied to 1V, and 0.9V is applied as an input, what is the output of the cascaded N-Pass transistors?

a) (0.9N) V.

b) (N) V

c) 0.7 V

d) 0.3 V

e) -.0.7 V

f) -0.3 V

g) 1.3 V

h) 1.7 V

Q5. For an N-cascaded PMOS pass transistors where all the gates are tied to 0V, and 0.9V is applied as an input, what is the output of the cascaded N-Pass transistors?

a) 0.9N.

b) N

c) 0.7V

d) 0.3V

e) -.0.7V

f) -0.3V

g) 1.3V

h) 0.9V

Q6.

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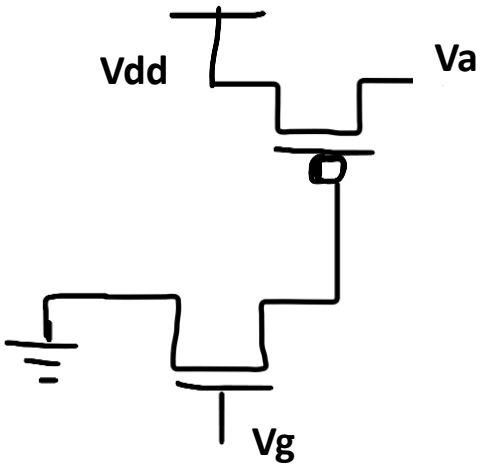
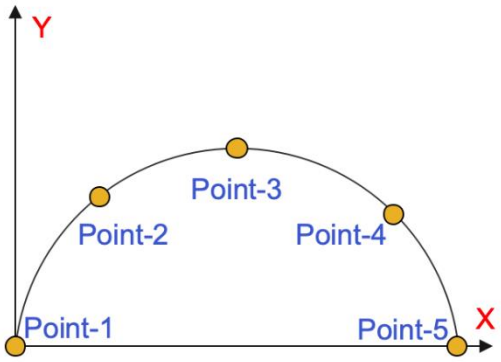


What is Va for Vg>0.3? Assume Vt=0.3 for both nMOS and pMOS

a) Va = Vdd – Vtp
b) Va = Vtp
c) Va = Vdd
d) Va is floating

Q7) In the provided inverter characteristics figure, which parameters should be plotted on the X and Y axes to represent the observed characteristics, and identify the operating regions of PMOS and NMOS transistors at Point-4?



a) Y: Vout, X: Vin, At Point-4: PMOS: Saturation, NMOS: Linear
b) Y: Vin, X: Vout, At Point-4: PMOS: Saturation, NMOS: Saturation
c) Y: Ids, X: Vin, At Point-4: PMOS: Linear, NMOS: Saturation
d) Y: Vin, X: Ids, At Point-4: PMOS: Cut-off, NMOS: Linear
e) Y: Vout, X: Ids, At Point-4: PMOS: Saturation, NMOS: Linear
f) Y: Ids, X: Vin, At Point-4: PMOS: Saturation, NMOS: Linear

g)	Y: Ids,	X: Vout,	At Point-4: PMOS: Linear,	NMOS: Saturation
h)	Y: Ids,	X: Vout,	At Point-4: PMOS: Saturation,	NMOS: Linear

Q8. Employing the short-channel current model, calculate the threshold voltage of an inverter functioning at a nominal voltage of 1 volt. The system exhibits a PMOS width to NMOS width ratio of 2:5, a NMOS velocity saturation ratio to PMOS velocity saturation ratio of 2:4, and possesses threshold voltages of 0.3 volts for both the PMOS and NMOS transistors.

a) 0.585
b) 0.325
c) 0.174
d) 0.744
e) 0.779
f) 0.4
g) 0.625
h) 0.8

Q9. N stacked series nMOS transistors with each dimension (w,L) can be equivalently be represented by

a) w,NL

b) w/N, L

c) w/N,NL

d) Nw,L/N

Q10. In a transmission gate, when the supply is ramped from 0 to Vdd, which of the following is true?

a) From 0 → Vdd-Vt, nMOS ON, Vdd-Vt → Vdd , pMOS ON

b) From 0 → Vdd-Vt, pMOS ON, Vdd-Vt → Vdd, nMOS OFF

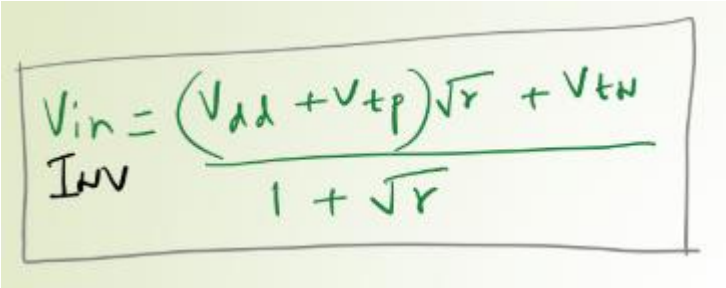
c) From 0 → Vdd-Vt, pMOS ON, Vdd-Vt → Vt, nMOS ON

d) From Vdd-Vt → Vdd, nMOS OFF, pMOS OFF

Solutions:

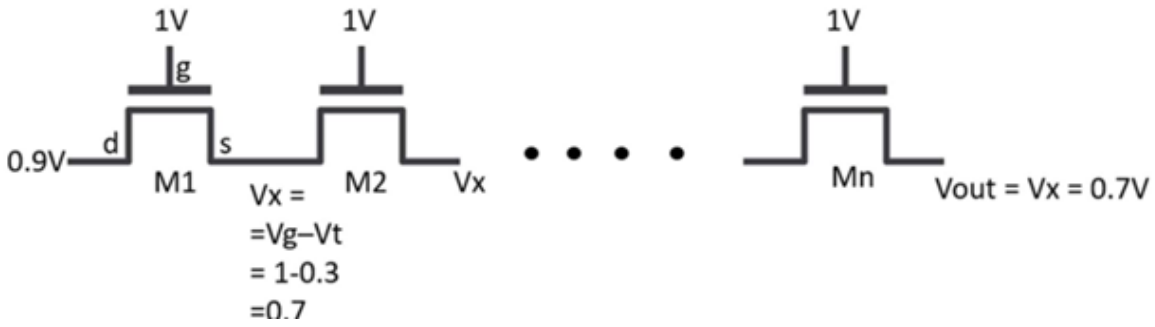
1. f
   For the given values, nMOS is in saturation and pMOS is in linear
   Using the nMOS saturation current equation, ids sat= un*Cox(w/2*L)(Vgs-Vth)^2, Id in inverter is 760 uA

2. e

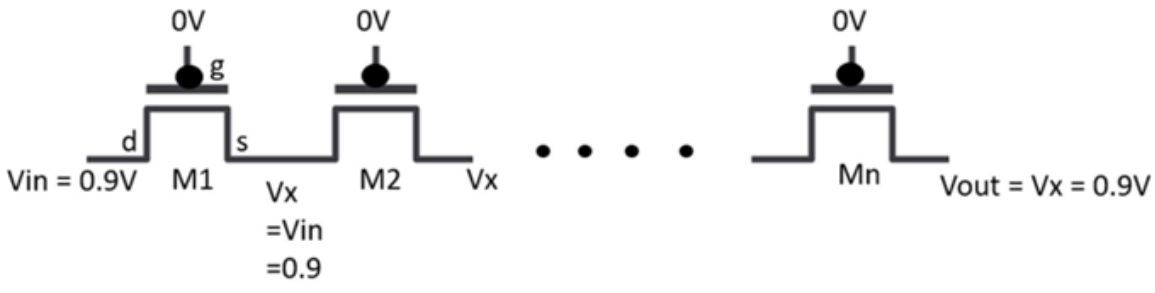


3. h

4. c. 0.7 V nmos passes weak 1



5. h. 0.9 V



6. C
   For Vg>0.3 , nMOS is ON, nMOS passes strong 0, so gate of pMOS is at 0
   Then for the pMOS, pMOS passes strong 1, so Va= Vdd

7. G
   The plot represents Ids vs Vds characteristics of an inverter
   point 4 is the point where input is close to 0 and output is close to Vdd, with nMOS in saturation and pMOS in linear

8. D

$$r = \frac{W_p v_{sat-p}}{W_N v_{sat-N}}$$

Wp/Wn= 2/5=0.4

Vsat-n/Vsat-p=2/4=> Vsat-p/Vsat-n=4/2=2

r=0.4*2=0.8

$$V_{inv} = \frac{r(V_{dd} + V_{tp}) + V_{tN}}{1 + r}$$

Vinv th=(0.8x[1+0.3]+0.3)/(1+0.8)=0.744

9. A,b

10. A,b
pMOS conducts from 0 to Vdd whereas nMOS conducts only from 0 to Vdd-Vt