





VLSI Physical Design with Timing Analysis

Lecture - 18: STA for Combinational Circuits - II

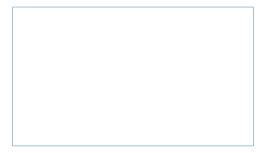
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Contents

Critical Path finding









Investing type of gates



- 1 Output rise A.T. = max (input fall A.T.) + Rise delay
- 2) Output fall A.T. = max(input rise A.T.) + fall delay
- 3 input rise A.T. = min (output fall R.T.) fall delay
- (y) input fall A.T. = min(output rise A.T.) rise delay





Given (Rise delay) for each gate

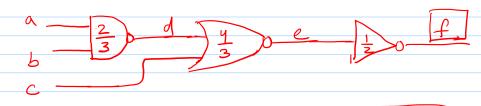
rise A.T. node "a" = $\frac{0}{0}$

$$''$$
 $''$ $''$ $''$ $b'' = \frac{0}{0}$

$$c'' = \frac{0}{0}$$

R.T. at node "
$$f$$
" = $\frac{5}{11}$

- (i) Find the R.T. at each node
- is Find the slack at each node
- (iii) Critical path in the circuit



Node a
$$A \cdot T = \frac{0}{0} \times Rise A \cdot T$$

$$7 \text{ R.T.} = \frac{2}{-1}$$
 Slack = $\frac{2}{-1}$

Node b A.T. =
$$\frac{0}{0}$$
 Slack = $\frac{2}{-1}$

$$R \cdot T \cdot = \frac{5-3}{1-2} = \frac{2}{-1}$$

$$=3$$
 of P. R.T. γ is $z=1$, γ is a deby (NAND)



Slack =
$$\frac{1-0}{5-0} = \frac{1}{5}$$

$$R \cdot T = \frac{4-3}{9-4} = \frac{1}{5}$$

$$=\frac{3+9}{2+2}=\frac{7}{5}$$

$$R \cdot 7 \cdot = \frac{11 - 2}{5 - 1} = \frac{9}{9}$$

$$=\frac{9-7}{4-5}=\frac{2}{-1}$$



A.T. =
$$\frac{2}{3}$$
 full A.T. = 0; Rise delay = 2
 $\frac{1}{7}$ rise A.T. = 0; fall delay = 3

$$\frac{\partial}{\partial r} = \frac{\partial}{\partial r} + \frac{\partial}{\partial r} = \frac{\partial}{\partial r} + \frac{\partial}$$



Node
$$f$$

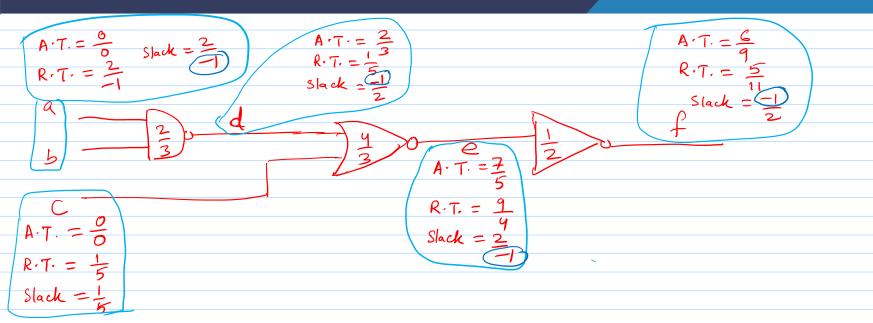
A·T. $=\frac{5+1}{7+2}=\frac{6}{9}$
 $\begin{cases} i/p. \text{ A·T. fall } =5; \text{ Rise delay } =1\\ i/p. \text{ A·T. rise } =7 \text{ fall delay } =2 \end{cases}$

Given
$$R \cdot T = \frac{5}{11}$$

Slack = $R \cdot T - A \cdot T = \frac{R \cdot T \cdot (Rise) - A \cdot T \cdot (Rise)}{R \cdot T \cdot (full) - A \cdot T \cdot (full)} = \frac{5 - 6}{2} = \frac{-1}{2}$







'(f' rising > 'e' falling > 'd' rising > "a/b" falling







Thank You





