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VLSI Physical Design with Timing Analysis

Lecture – 13: STA in Sequential Circuit with Clock Skew

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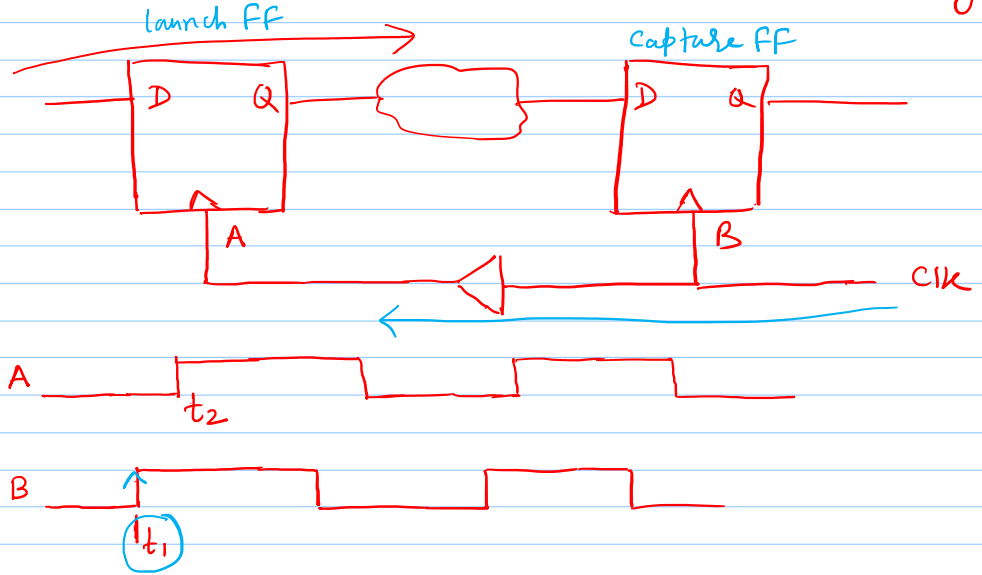
Contents

- What is negative clock skew?
- Max. timing constraint (Setup check) with negative Clock Skew
- Min. timing constraint (Hold Check) with negative Clock Skew
- Some examples

② **Negative Skew**: Data and clock signal is moving in "opposite" direction.



Skew = Capture clk A.T. − launch clk A.T.

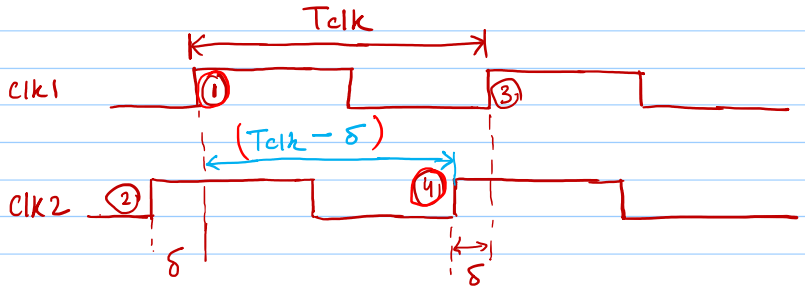
= $(t_1 - t_2)$

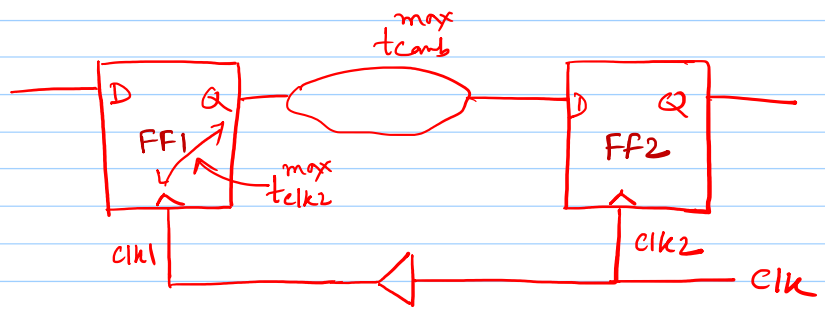
Skew is −ve

Max timing Analysis considering -ve skew

① FF1 will sample at edge ①

② FF2 will sample at edge ④





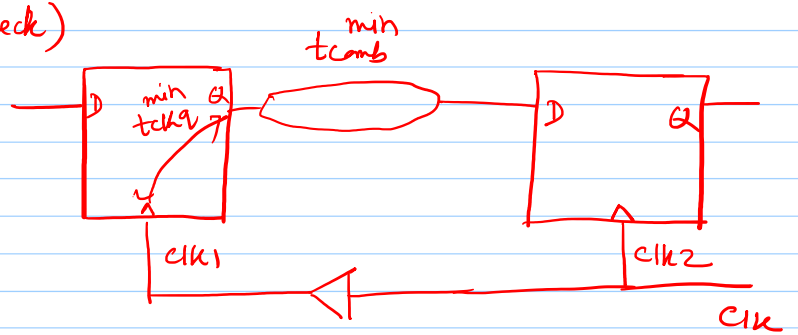
Case I (without clock skew) : $t_{clk2q}^{max} + t_{comb}^{max} + t_{setup} \leq T_{clk}$

Case II (with clock skew) : $t_{clk_{2q}}^{max} + t_{comb}^{max} + t_{setup} \leq (T_{clk} - \delta)$

$\Rightarrow \left(t_{clk2q}^{max} + t_{comb}^{max} + t_{setup} + \delta\right) \leq T_{clk}$

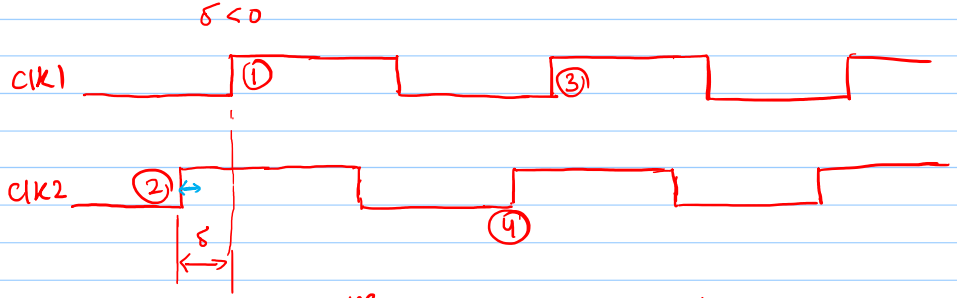
$\because T_{clk} \uparrow \Rightarrow f_{clk} \downarrow$ (Max speed of operation will decrease)

Min. timing Analysis considering -ve skew (Hold check)



We are checking edge ① and ②

with -ve skew, $t_{hold} \rightarrow (t_{hold} - \delta)$



① Case I (without -ve clock skew) : $t_{hold} \leq t^{min}_{clk2q} + t^{min}_{comb}$

② Case II (with -ve clock skew : $(t_{hold} - \delta) \leq t^{min}_{clk2q} + t^{min}_{comb}$

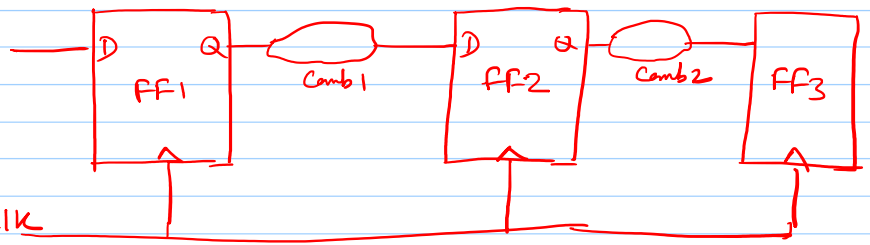
$$t_{hold} \leq t^{min}_{clk2q} + t^{min}_{comb} + \delta$$

Ex1

$t_{setup} = 2ns$, $t_{hold} = 1ns$, $t_{clk2q} = 10ns$

$t_{comb1} = 5ns\ (max)$ | $t_{comb2} = 6ns\ (max)$

$= 2ns\ (min)$ | $= 1ns\ (min)$



Find the max. frequency of operation.

Ans:

Case I: Path bet^n FF1 and FF2

$$T_{clk_1} \geq t_{clk2q}^{max} + t_{comb1}^{max} + t_{setup}\ (FF2)$$

$$\geq 10ns + 5ns + 2ns$$

$$T_{clk} \geq 17ns$$

Case II: Path bet^n FF2 and FF3

$$T_{clk_2} \geq 10ns + 6ns^{(t_{comb2}\ max)} + 2$$

$$T_{clk} \geq 18ns$$

$$T_{clk} = \max(T_{clk1}, T_{clk2})$$

$$= 18ns$$

$$f_{clk} = \frac{1}{T_{clk}} = \frac{1}{18ns} = 55.56MHz$$

$f_{clk} = 55.56MHz$

Min. Timing analysis in the circuit. (Hold check)

Case I (FF1 and FF2)

$$t_{hold} \leq t_{clk2q}^{min} + t_{comb}^{min}$$

$$1ns \leq 10ns + 2ns$$

$$1ns \leq 12ns$$

No hold violation.

Case II (FF2 and FF3)

$$t_{hold} \leq t_{clk2q}^{min} + t_{comb}^{min}$$

$$1ns \leq 10ns + 1ns$$

$$\boxed{1ns \leq 11ns.}$$

No hold violation.

Assume: $t_{clk2q}^{min} = 0.5ns$ and $t_{comb}^{min} = 0.2ns$

$t_{hold} = 1ns$

$$t_{hold} \leq t_{clk2q}^{min} + t_{comb}^{min}$$

$$1ns \leq 0.5ns + 0.2ns$$

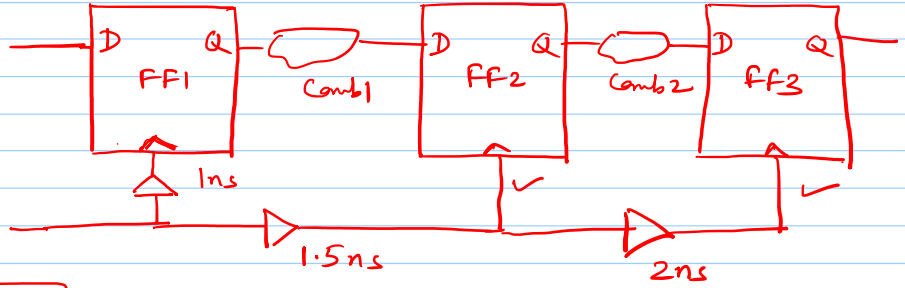
$$\boxed{1ns \leq 0.7ns} \quad \times$$

hold violation.

Ex-2

(i) Max freq. of operation

(ii) hold check



Case I (FF1 and FF2)

$\delta = (1.5\text{ns} - 1\text{ns}) = 0.5\text{ns}$

$(T_{clk1} + \delta) \geq t_{clk2q} + t_{comb1}^{(max)} + t_{setup}$

$\geq 10\text{ns} + 5\text{ns} + 2\text{ns}$

$T_{clk1} \geq 17 - 0.5 = 16.5\text{ns} \Rightarrow T_{clk1} = 16.5\text{ns}$

Case II (FF2 and FF3)

$\delta = 2\text{ns}$

$T_{clk2} = 18\text{ns}$ (without clock skew)

$T_{clk2} = 18\text{ns} - 2\text{ns}$

$T_{clk2} = 16\text{ns}$ (with clock skew)

$T_{clk} = \max(T_{clk1}, T_{clk2}) = \max(16.5\text{ns}, 16\text{ns})$

$= 16.5\text{ns}$

$f_{clk} = \frac{1}{16.5\text{ns}} = 60.61\text{MHz}$

① with +ve skew, speed of operation increases

Hold check

Case I (betn FF1 and FF2) $\Rightarrow \delta = 0.5ns$

$$t_{hold} + \delta \leq t_{clk2q}^{min} + t_{comb_1}^{min}$$

$$1ns + 0.5ns \leq 10ns + 2ns$$

$$1.5ns \leq 12ns \quad \text{(No hold violation)}$$

Case II (betn FF2 and FF3) $\Rightarrow \delta = 2ns$

$$t_{hold} + \delta \leq t_{clk2q}^{min} + t_{comb_2}^{min}$$

$$1ns + 2ns \leq 10ns + 1ns$$

$$\boxed{3ns \leq 11ns} \quad \text{(No hold violation)}$$

Assume:

$t_{clk2q}^{min} = 0.5ns$ and $t_{comb_1}^{min} = 0.5ns$

$t_{hold} = 1ns$ and $\delta = 0.5ns$

$$\Rightarrow t_{hold} + \delta \leq t_{clk2q}^{min} + t_{comb_1}^{min}$$

$$\Rightarrow 1ns + 0.5ns \leq 0.5ns + 0.5ns$$

$$\Rightarrow \boxed{1.5ns \leq 1ns} \quad \times$$

hold violation.

Thank You