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NPTEL ONLINE CERTIFICATION COURSE

# VLSI Physical Design with Timing Analysis

## Lecture – 1: Introduction to VLSI Design

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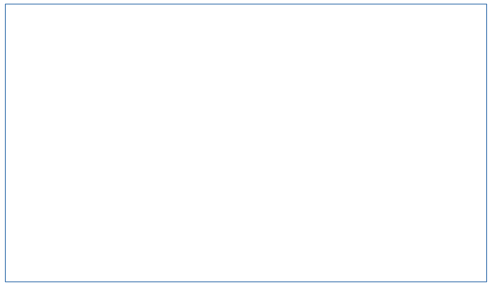
**Department of Electronics and Communication Engineering**

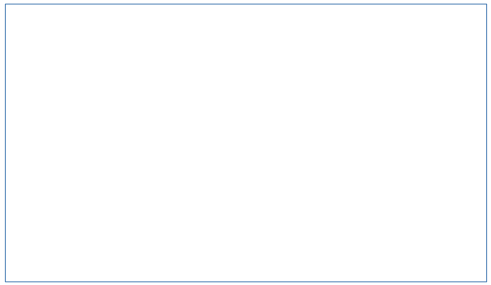
# Objectives of the course

1. Understanding VLSI Design and Physical Design Flow.
2. Learn the fundamentals of graph theory and algorithms used in VLSI physical design.
3. Explore the principles of STA and learn to apply them in practice.



# Objectives of the course

4. Learn about various steps in VLSI Physical Design like Partitioning, Chip planning, Placement, CTS, and Routing etc.
5. Learn to use some open-source tools for VLSI Physical Design.
6. Introduce advanced topics like SSTA.

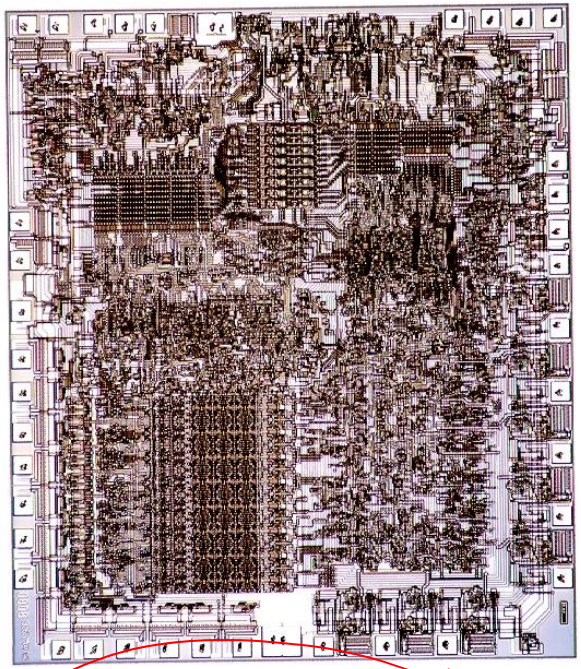


# Significance of Physical Design

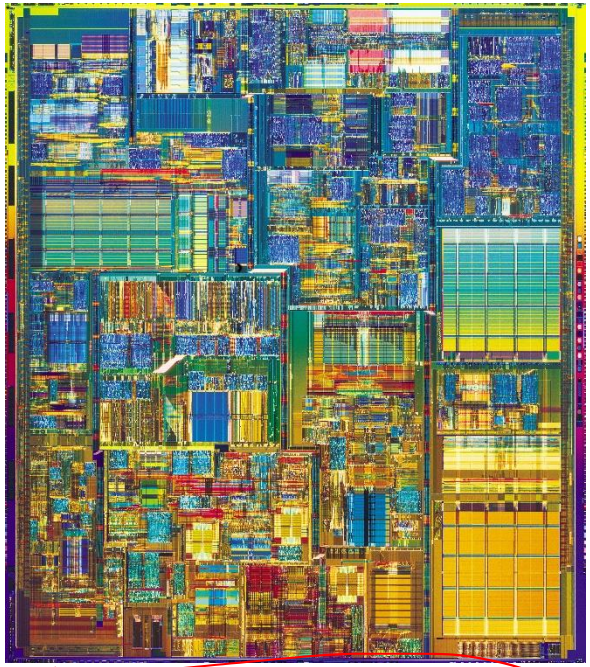
| Year | Processor | Transistor count |
|---|---|---|
| 2000 | Pentium 4 from Intel | 42 million |
| 2003 | AMD K8 Barton | 54.3 million |
| 2018 | Xeon Platinum 8180 from intel | 8 billion |
| 2022 | Qualcomm Snapdragon 8 Gen 2 | 16 billion |
| 2023 | Apple M2 ultra | 134 billion |
| 2023 | AMD Instinct MI300A | 146 billion |

Source: https://en.wikipedia.org/wiki/Transistor_count

# Significance of Physical Design



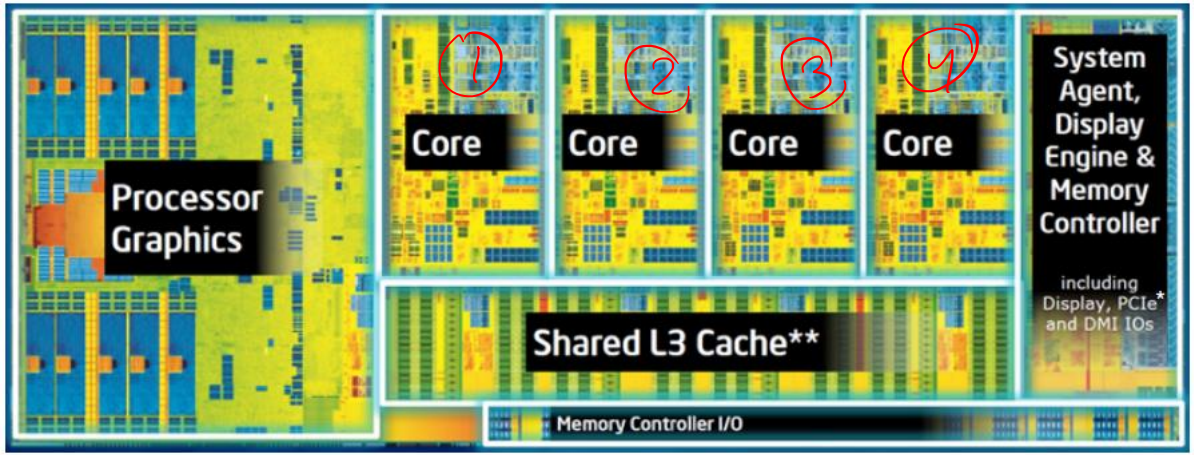
1974: Intel 8080



2000: Intel Pentium 4

Source: https://www.tayloredge.com/museum/processor/processorhistory.html

# Significance of Physical Design

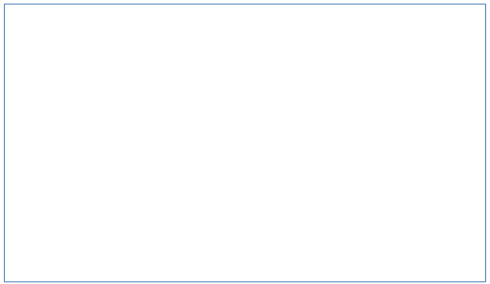



Intel® Core™ i7 processor internal die photograph

Source: https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/ia-introduction-basics-paper.pdf

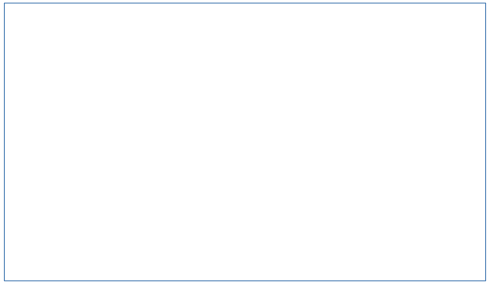
# Contents

- VLSI Design Styles
- Design Abstraction
- Synthesis

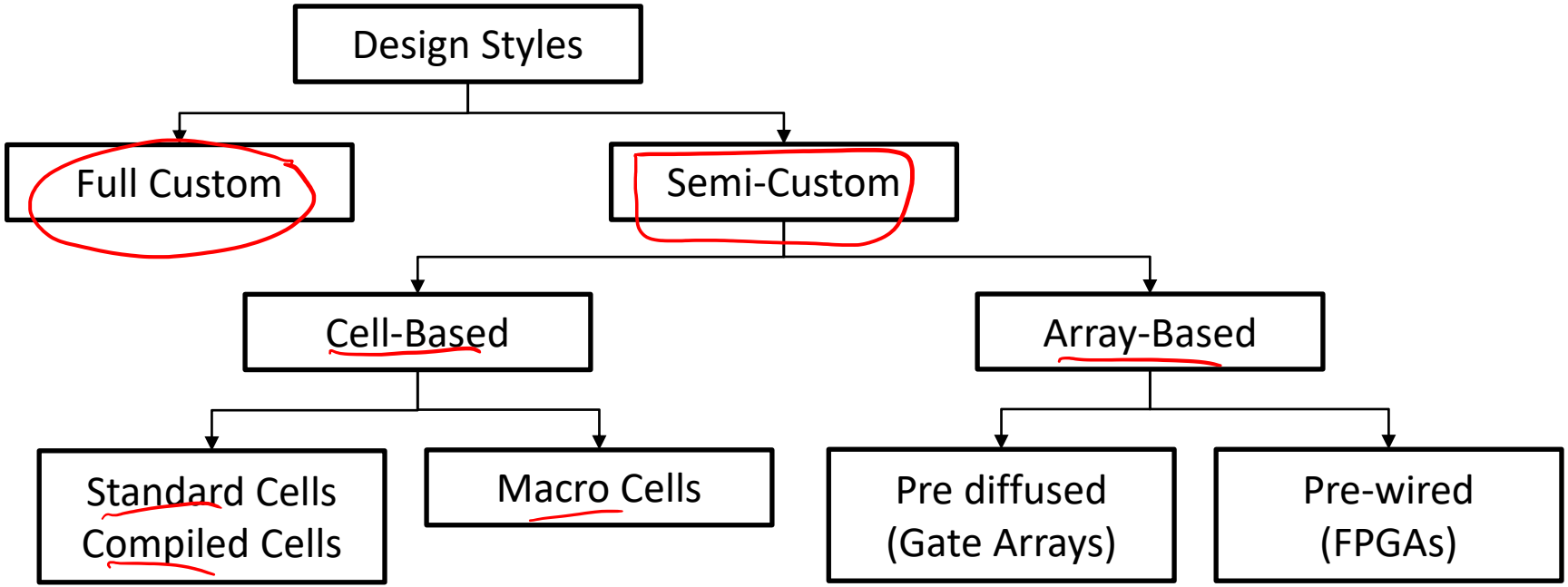


# VLSI Design Styles

- Design styles can be broadly categorized as
  1. Full custom
  2. Semi-custom
- The choice of layout style depends on factors like
  - chip type
  - cost
  - time-to-market



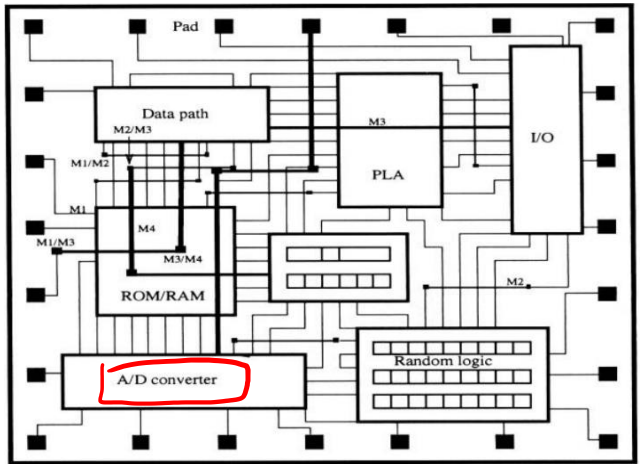
# VLSI design styles



# Full Custom Design Style

- Fewest Constraints during layout generation.
  - Blocks can be placed anywhere on the chip.

① Layout are drawn manually
② No constraints in size of the design
③ No placement constraints




Picture source: Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation

# Full Custom Design Style

- Yields a very compact chip with highly optimized electrical properties.
- Laborious, time-consuming, and error-prone.
- Useful for microprocessors, FPGAs, and Analog Blocks.

Critical paths or data path

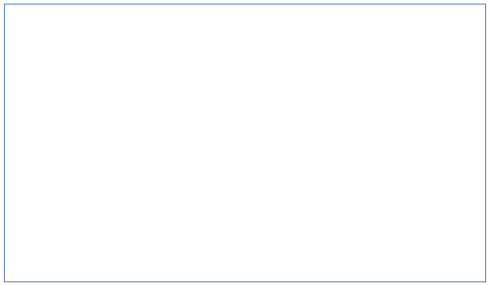
① Switch matric
② LUT
③ CLB

① ADC
② PLL

# Semi-Custom Design Style

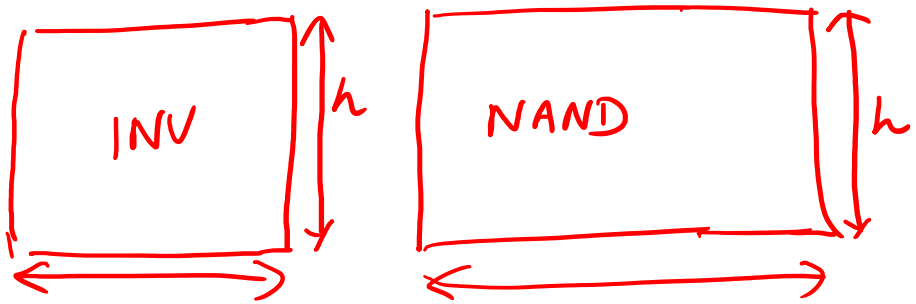
- In **semi-custom** layouts
  - Certain circuit portions are pre-designed by third part company
- It can be categorized as
  1. Cell-based
  2. Array based

1. ARM
2. Synopsys
3. Faraday



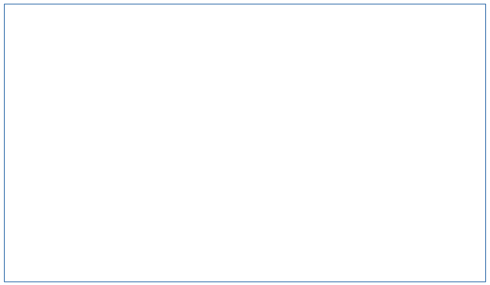
# Cell-Based Style

- **Standard Cell Design:**
  - Uses predefined **rectangular cells of the same height**.
  - These cells are part of a rigorously tested and characterized library.

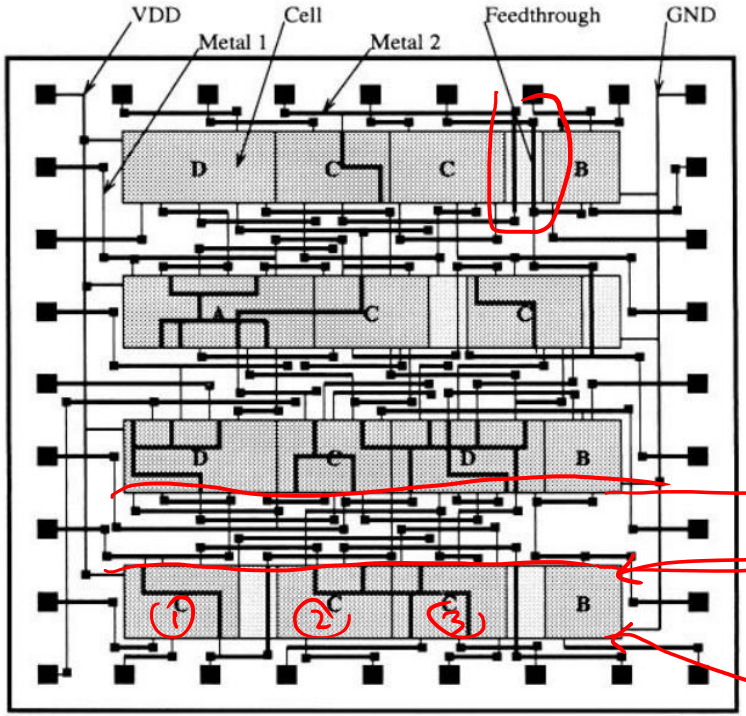


# Standard Cell Design

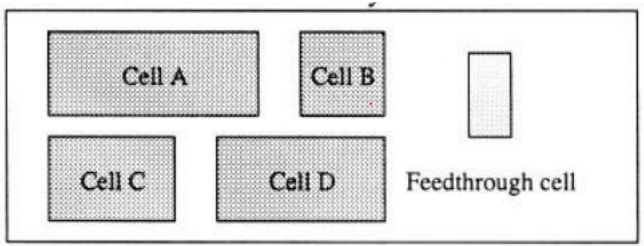
- Cells are arranged in rows, with interconnections in the **channels** between rows.
- Connections between cells can go through channels or over cells (feedthroughs) if they're not in adjacent rows.



# Standard Cell Design




**Standard cell library**



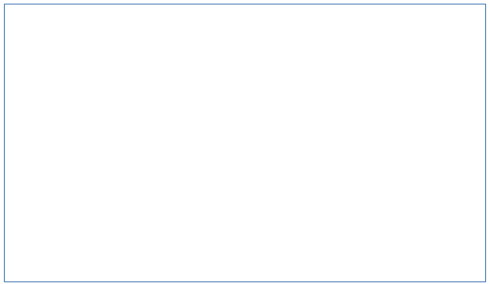




Picture source: Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation

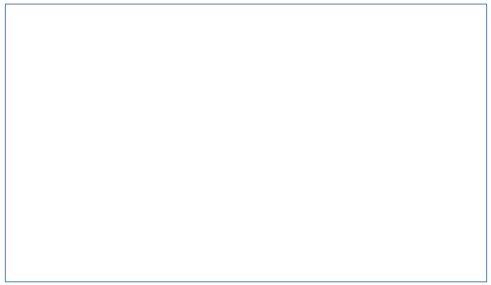
# Standard Cell Design

- Simpler than full-custom design and works well with modern design tools.
- Occupies more chip area than full-custom designs but is getting closer with advancements in technology.

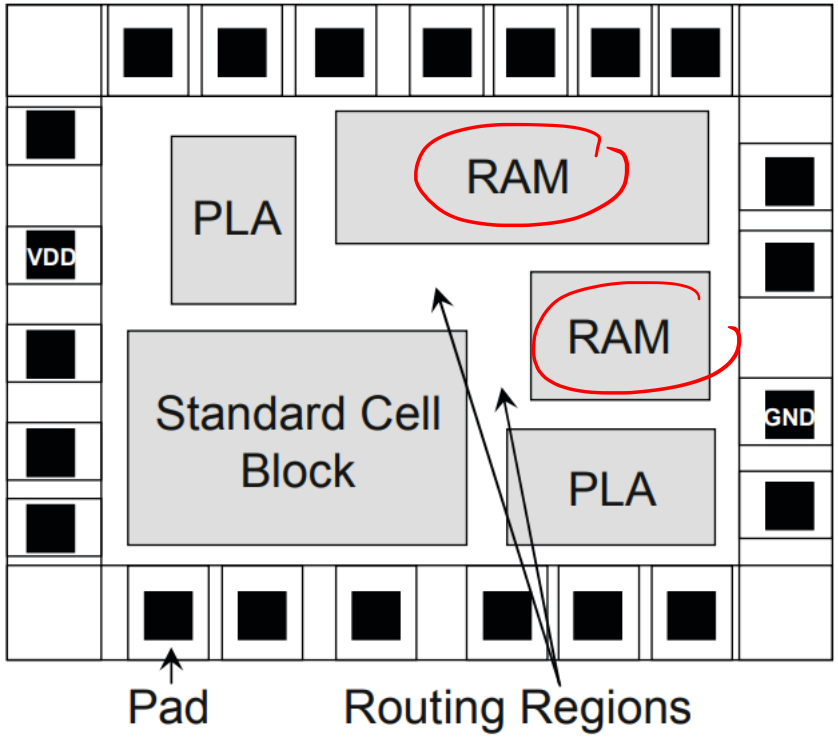


# Cell-Based Style

- **Macro Cells:**
  - Larger logic components with
    - reusable functionalities,
    - ranging from simple to highly complex,
    - even reaching the scale of embedded processors or memory blocks.



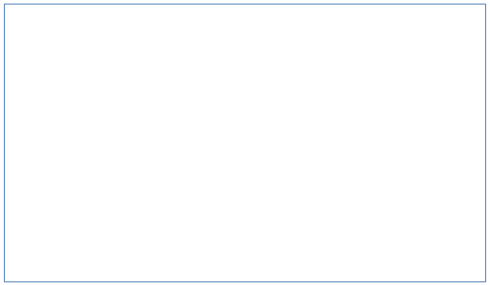
# Macro Cells




Source: A. B. Kahng et al., VLSI Physical Design: From Graph Partitioning to Timing Closure

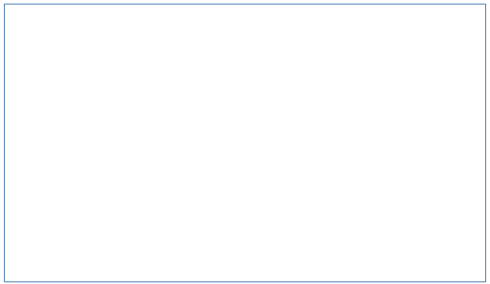
# Macro Cells

- Can be placed anywhere in the layout area to optimize routing distance or electrical properties.
- In some cases, a design can be mostly assembled from **pre-existing macros**, necessitating top-level assembly.



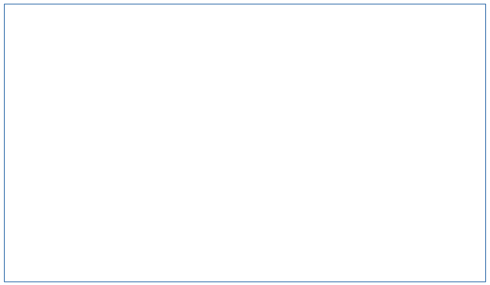
# Array-Based Design Style

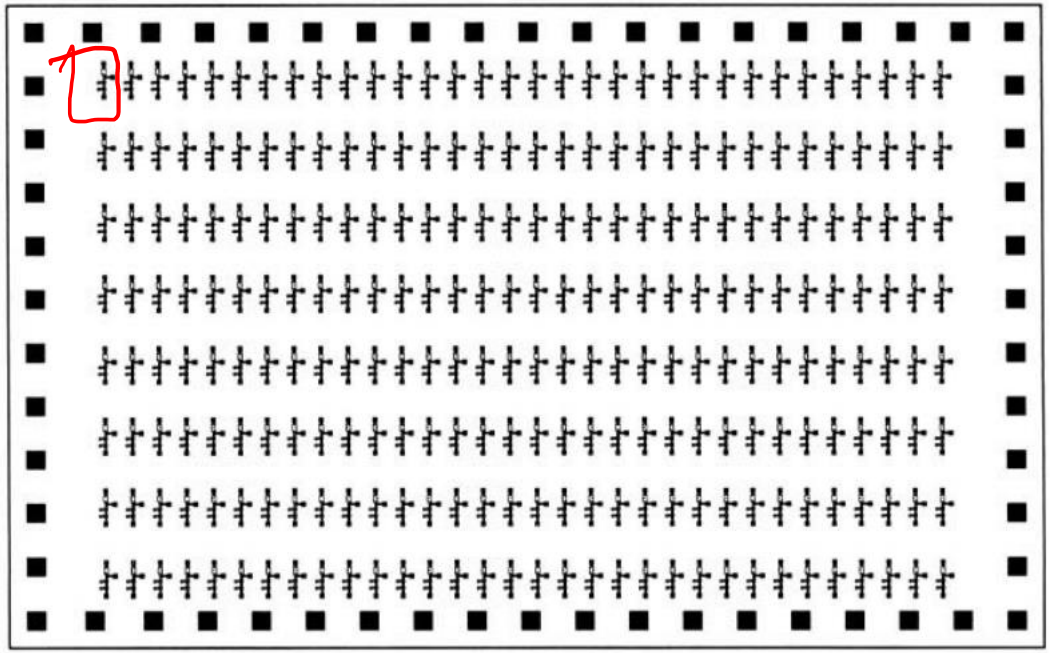
- **Gate Array:**
  - Simplifies chip design by using identical cells or gates throughout the chip.
  - The circuit is divided into identical blocks, each equivalent to a cell on the gate array.
  - Blocks are mapped or placed onto prefabricated cells during partitioning.



# Gate Array

- Interconnections are established using horizontal and vertical channels.
- **Uncommitted Gate Array:**
  - A prefabricated chip where routing layers are added on top in a fabrication facility.
- **Committed Gate Array:**
  - A gate array design with fully customized routing layers.

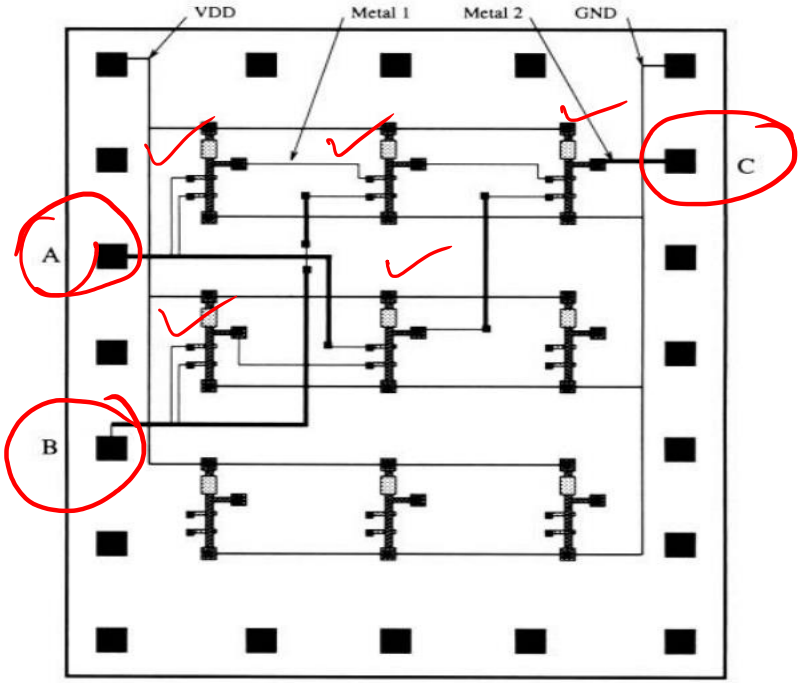


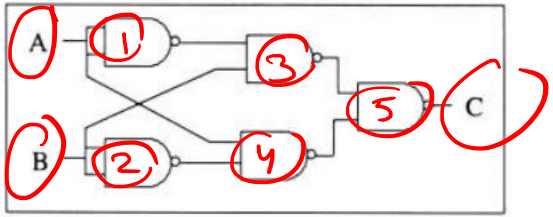


A conceptual uncommitted gate array

Picture source: Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation

# A conceptual Gate Array



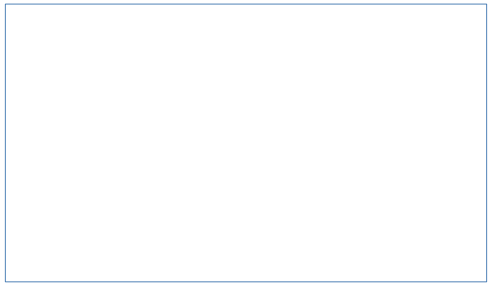

Picture source: Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation

# Gate Array

- Cost-effective
- Easier to produce than full-custom or standard cell designs but **less flexible**.
- Routing in gate array design is simpler,
  - focusing on routability rather than optimizing area.

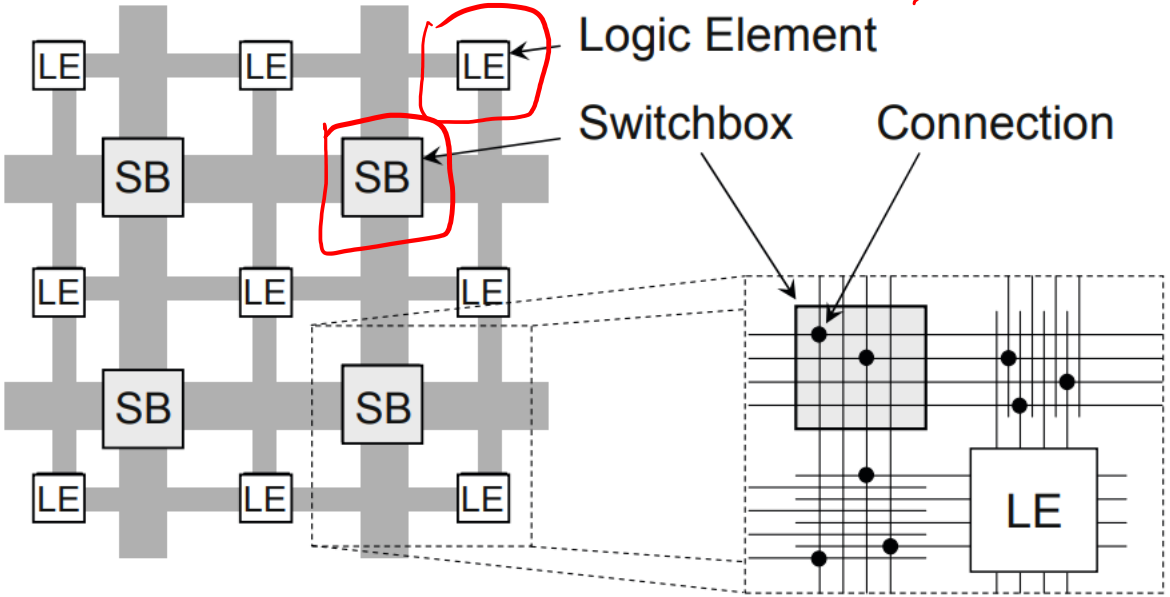
# Field Programmable Gate Arrays(FPGAs)

- In FPGAs, cells and interconnects are pre-made, and users program the interconnect.
- Offers large-scale integration and user programmability.
- Logic blocks in FPGAs are like memory blocks that can store logic tables for functions with small inputs – **LUT**s.
- Consists of rows of logic blocks separated by routing channels.



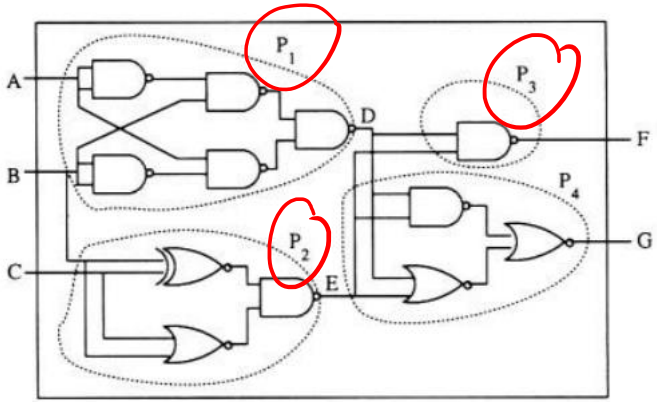
# FPGAs

CLB → Slices → LUT




Source: A. B. Kahng et al., VLSI Physical Design: From Graph Partitioning to Timing Closure

# FPGAs




$P_1$

| A | B | D |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$P_2$

| B | C | E |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

$P_3$

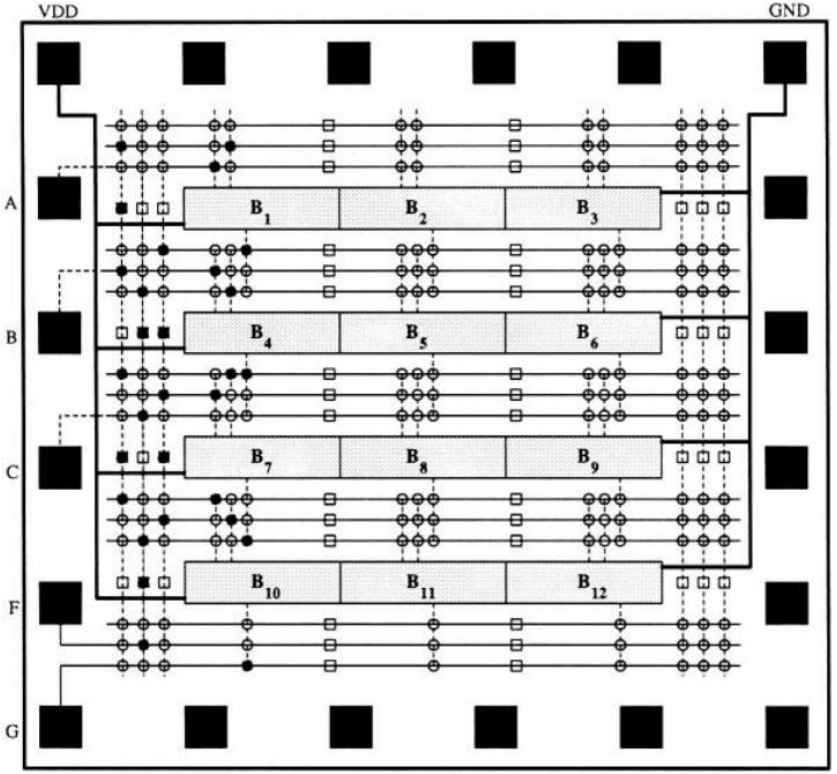
| D | E | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$P_4$

| D | E | G |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

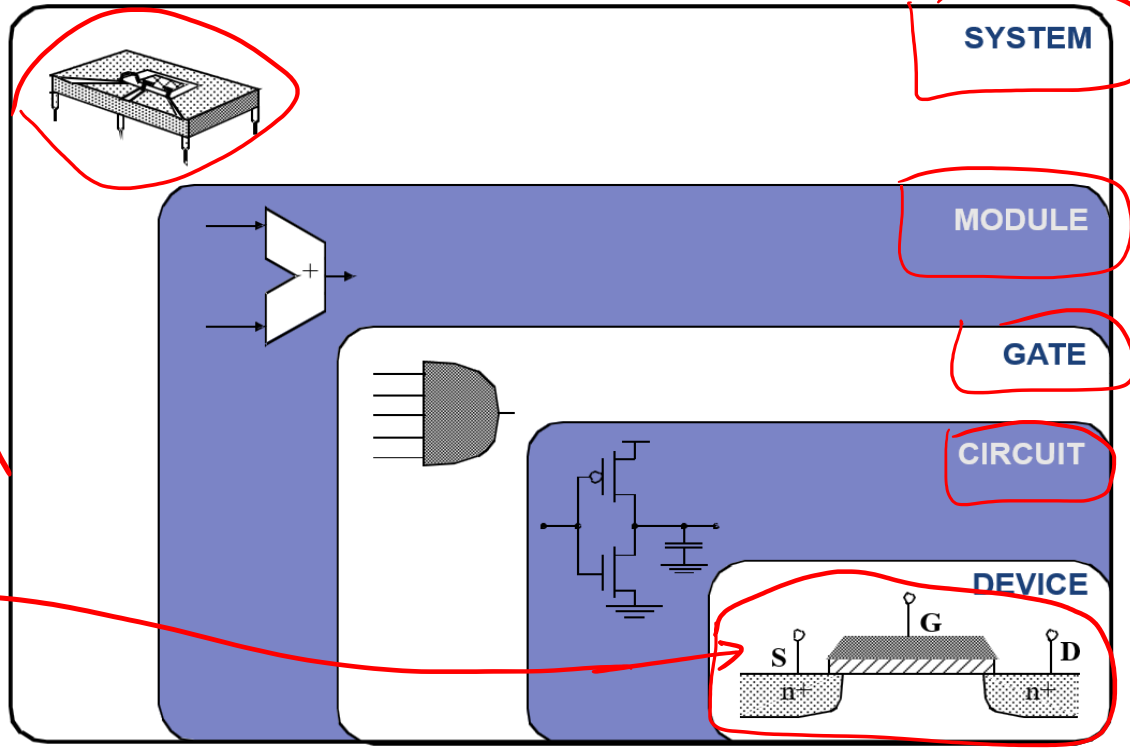
Picture source: Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation

# FPGAs




Picture source: Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation

# Design Abstraction Levels




Top-level view

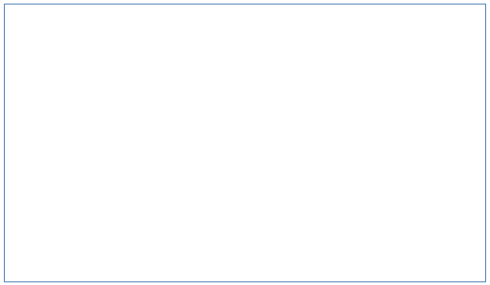
1. Speed
2. Area
3. Power

Bottom-level view

Source: Digital Integrated Circuits: A design perspective by Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic

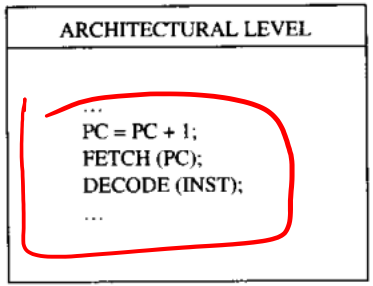
# Abstraction

- A representation that shows relevant features without associated details.
- Three main abstractions are considered: Architectural, Logic, and Geometrical.
- Design involves refining the **architectural model** into a detailed **geometrical model** suitable for manufacturing.



# Architectural Level

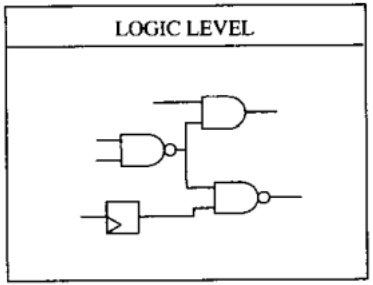
- Focuses on circuit operations.
- Represented as HDL models or flow diagrams.
- Example:
  - Processor described by HDL model.




Picture Source: Giovanni De Micheli “Synthesis and Optimization of Digital Circuits”

# Logic Level

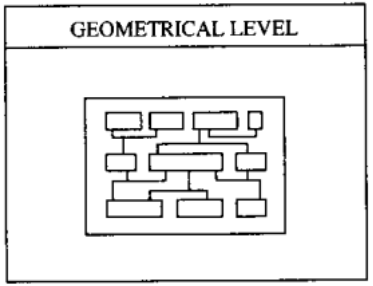
- Deals with logic functions.
- Represented as state transition diagrams or schematics.
- Example:
  - A gate-level schematic




Picture Source: Giovanni De Micheli “Synthesis and Optimization of Digital Circuits”

# Geometrical level

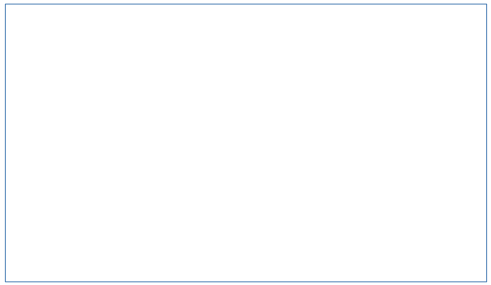
- Represents circuits as geometrical entities like Floor plans or layouts.
- Example:
  - Two-dimensional geometric picture represents mask layout.



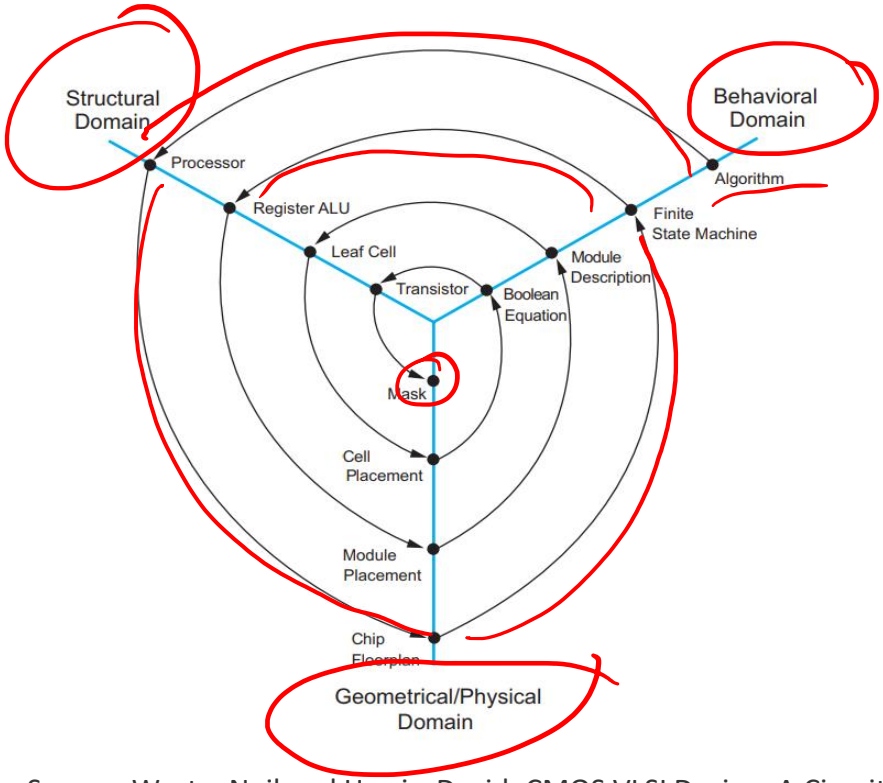

Picture Source: Giovanni De Micheli “Synthesis and Optimization of Digital Circuits”

# Views of a Model

- Views are classified as behavioral, structural, and physical.
  - **Behavioral views** describe circuit function regardless of implementation.
  - **Structural views** depict the model as an interconnection of components.
  - **Physical views** relate to the design's physical objects (e.g., transistors).



# Y-chart Representation

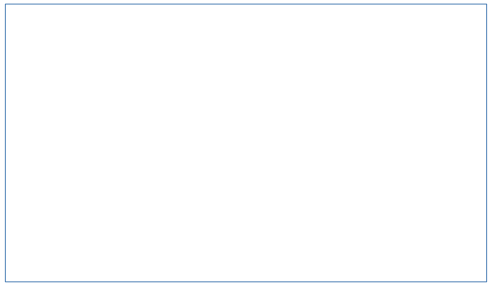



Views and abstraction levels are represented as segments of the letter Y, known as Gajski and Kuhn's Y-chart.

Picture Source: Weste, Neil and Harris, David: CMOS VLSI Design: A Circuits and Systems Perspective

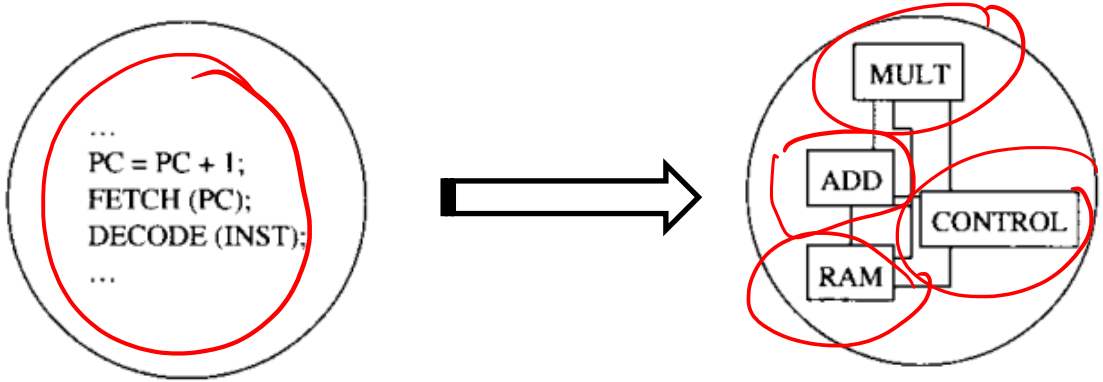
# Synthesis

- Synthesis involves transformations between different views.
- Classification of synthesis tasks based on modeling levels:
  - Architectural-level synthesis
  - Logic-level synthesis
  - Geometrical-level synthesis



# Architectural-level synthesis

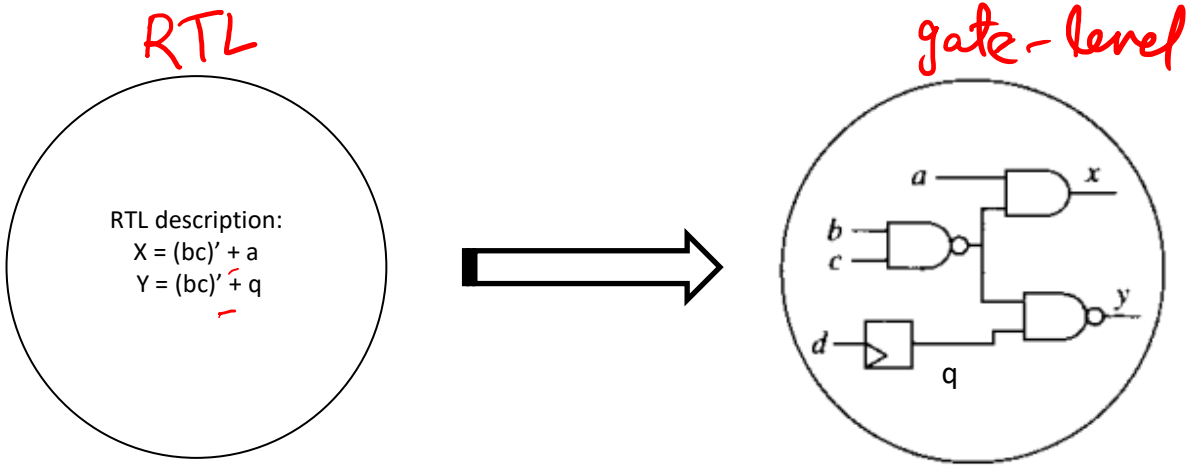
- Determines macroscopic circuit structure, including resource assignment and timing.




Picture Source: Giovanni De Micheli “Synthesis and Optimization of Digital Circuits”v

# Logic-level synthesis

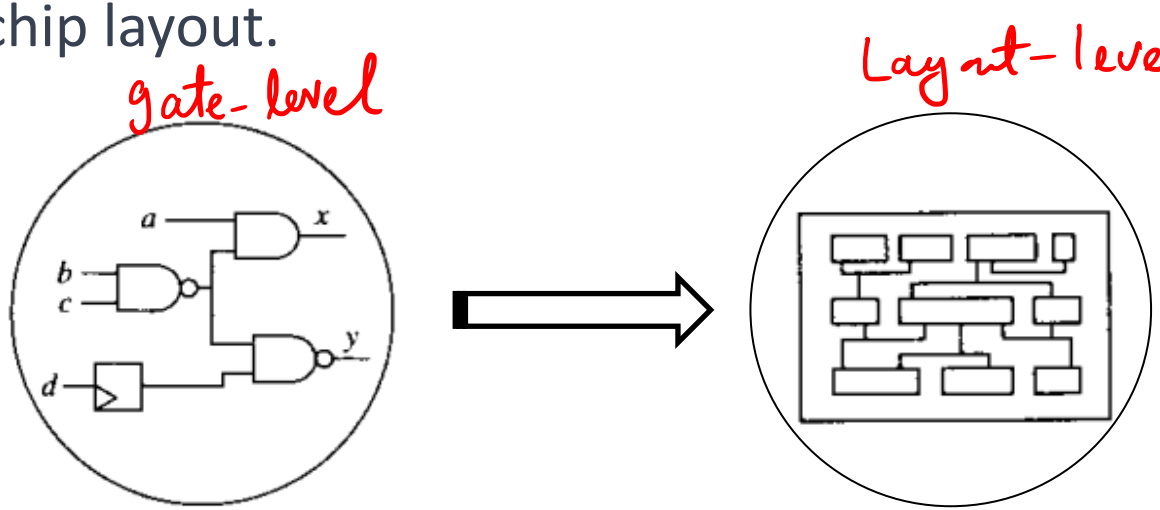
- Creates gate-level circuit structure from logic specifications.




Picture Source: Giovanni De Micheli "Synthesis and Optimization of Digital Circuits"

# Geometrical-level synthesis

- Involves creating a physical view at the geometric level, defining chip layout.




Picture Source: Giovanni De Micheli “Synthesis and Optimization of Digital Circuits”

# Thank You