



IIT ROORKEE



NPTEL ONLINE
CERTIFICATION COURSE

VLSI Physical Design with Timing Analysis

Lecture – 16: STA considering OCV and CRPR (Hold check)

Bishnu Prasad Das

Department of Electronics and Communication Engineering



Contents

- Launch FF and Capture FF
- Min. timing analysis (hold check) without variation
- Min. timing analysis (hold check) with on-chip variation (OCV)
- Min. timing analysis (hold check) with OCV + CRPR

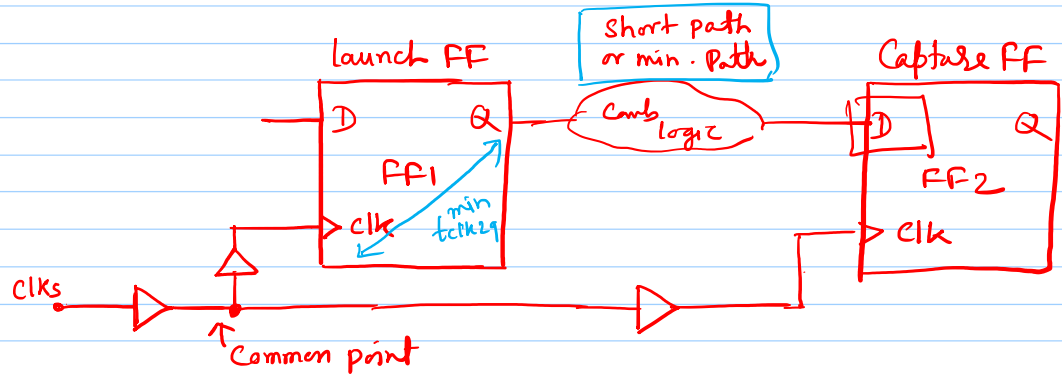


STA (Minimum Timing Analysis)



Hold Check

For Hold check



$$\text{Data arrival time (DAT)} = \text{launch Clock Path} + \text{Min Data Path}$$

$t_{\text{clk2q}}^{\text{min}} + t_{\text{comb}}^{\text{min}}$

$$\text{Data Required time (DRT)} = \text{Capture Clock Path} + t_{\text{hold}}$$

For Hold check: Data arrival time \geq Data Required time

$$\text{Slack} = \text{Data arrival time} - \text{Data Required time}$$

Case I: Slack is +ve $\Rightarrow \text{DAT} > \text{DRT} \Rightarrow$ No hold violation

Case II: Slack is -ve $\Rightarrow \text{DAT} < \text{DRT} \Rightarrow$ hold violation



Special Case! (No buffer in the clk tree)

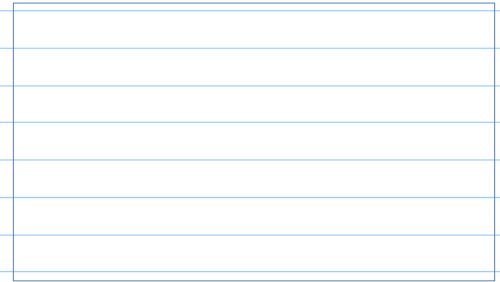
launch Clk Path = 0

Capture Clk Path = 0

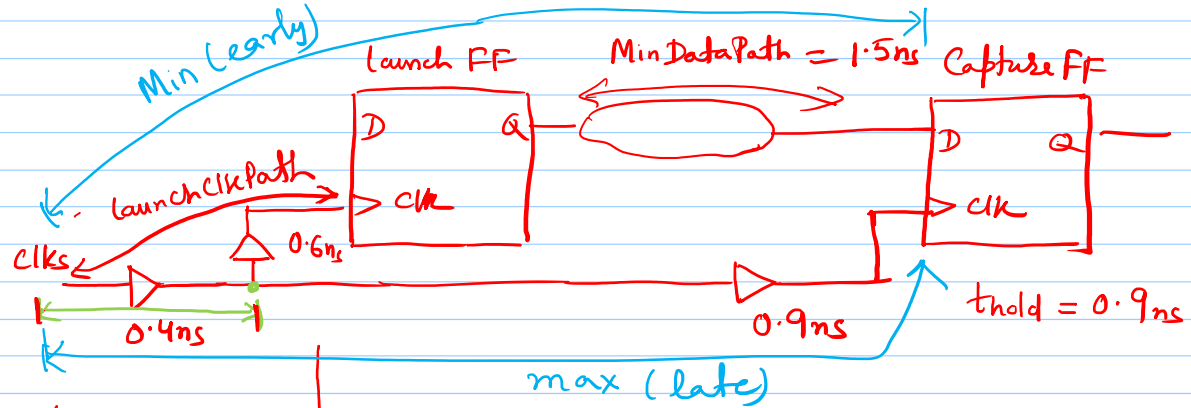
D.A.T. \geq D.R.T.

Min Data Path \geq t_{hold}

$$\Rightarrow \boxed{t_{clk2q}^{\min} + t_{comb}^{\min} \geq t_{hold}}$$



Ex: 1



Case I (without variation)

$$\text{launchClkPath} = 0.4 + 0.6 = 1\text{ns}$$

$$\text{MinDataPath} = 1.5\text{ns}$$

$$\text{CaptureClockPath} = 0.4 + 0.9 = 1.3\text{ns}$$

$$\text{thold} = 0.9\text{ns}$$

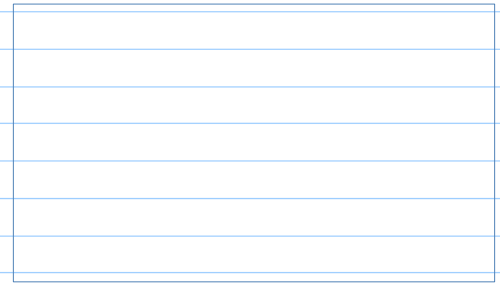
$$\text{DAT} = 1\text{ns} + 1.5\text{ns} = 2.5\text{ns}$$

$$\text{DRT} = 1.3\text{ns} + 0.9\text{ns} = 2.2\text{ns}$$

$$\text{Slack} = \text{DAT} - \text{DRT} = 2.5 - 2.2 = 0.3\text{ns}$$

Slack is +ve

hold requirement is met



Case II (with OCV) — local variation inside the same die

set-timing-derate - early 0.85

set-timing-derate - late 1.1

set-timing-derate - early 0.9 - cell-check
thold

Launch Clk Path = $1\text{ns} \times 0.85 = 0.85\text{ns}$
Min Data Path = $1.5\text{ns} \times 0.85 = 1.275\text{ns}$
Capture Clk Path = $1.3\text{ns} \times 1.1 = 1.43\text{ns}$

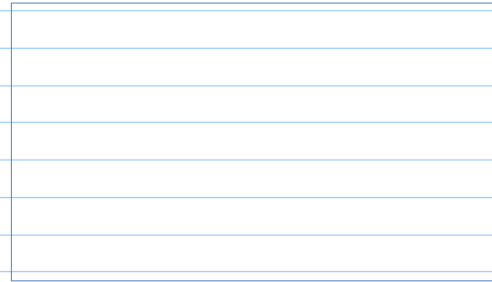
early

late

DAT = 2.125ns ; DRT = 2.24ns

$$\text{Slack} = \text{DAT} - \text{DRT} = -0.115\text{ns}$$

Slack is -ve \Rightarrow hold violation.



Case III (with OCV + CRPR)

$$CPP = 0.4 \times 1.1 - 0.4 \times 0.85 = 0.1ns$$

$$Slack = -0.115 + \overset{0.1ns}{CPP} = -0.015 \\ = -15ps$$

Hold violation exists



Buffer insertion in the Datapath

Note! Hold check is independent of the time period of the clk.

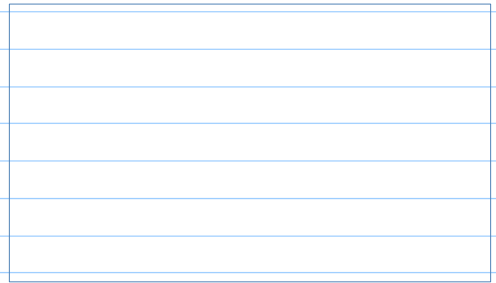
$$\boxed{Slack = DAT - DRT}$$

Case II (OCV)

$$Slack(OCV) = DAT - DRT$$

Case III (OCV + CRPR)

$$Slack(OCV + CRPR) = DAT - DRT + \underline{CPP} \\ = (DAT + CPP) - DRT$$



Thank You

