IIT ROORKEE

FREE ONLINE EDUCATION swayam शिक्षित भारत, उन्नत भारत

NPTEL ONLINE CERTIFICATION COURSE

VLSI Physical Design with Timing Analysis

Lecture – 10: Delay Parameters of Sequential Circuit

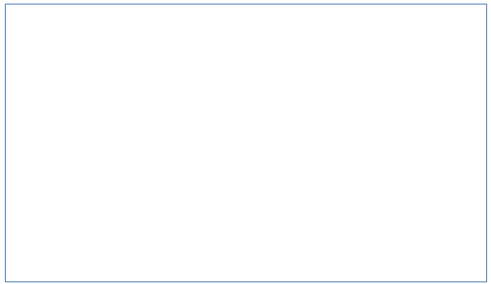
Bishnu Prasad Das

Department of Electronics and Communication Engineering

Contents

- Sequential Circuits
- Delay Parameters of Sequential Circuits

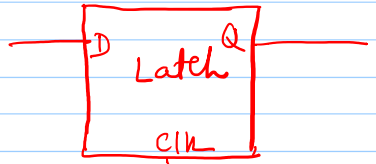
  (1) Setup time (2) Hold time and (3) Clock-to-Q delay
- Reason of Setup time in a Flip-flop
- Reason of Hold time in a Flip-flop



Sequential Circuits

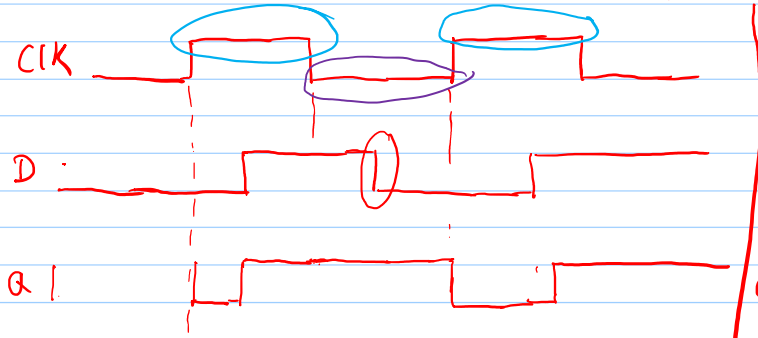
① Flip-flop (FF)
(Edge-triggered)

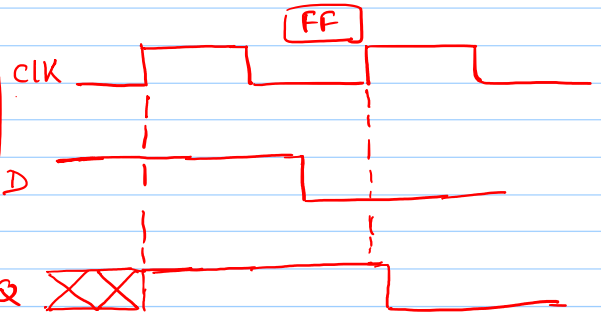
② Latch
(level triggered)

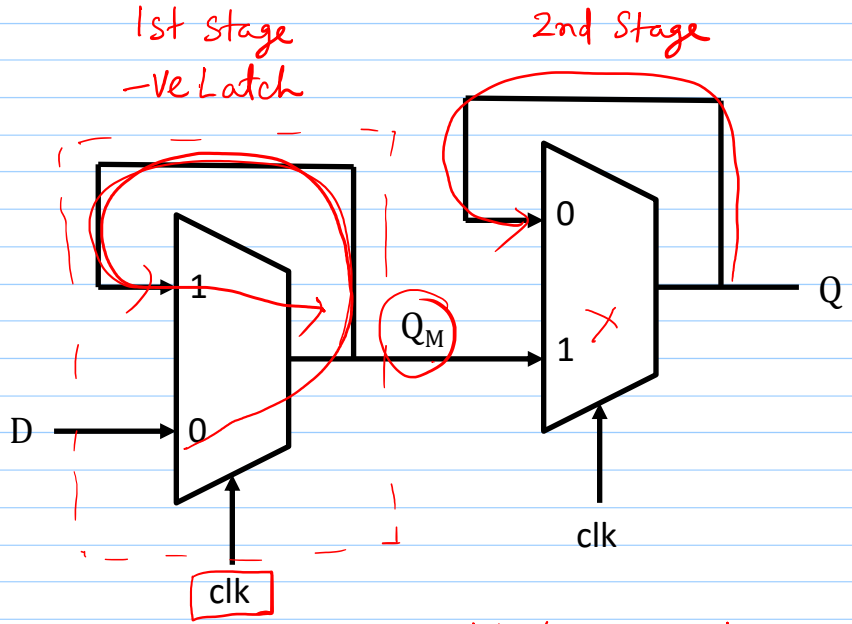


Latch — Positive-transparent latch

+ve edge-triggered FF





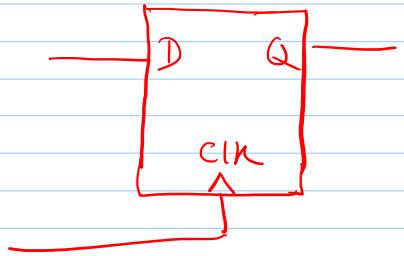


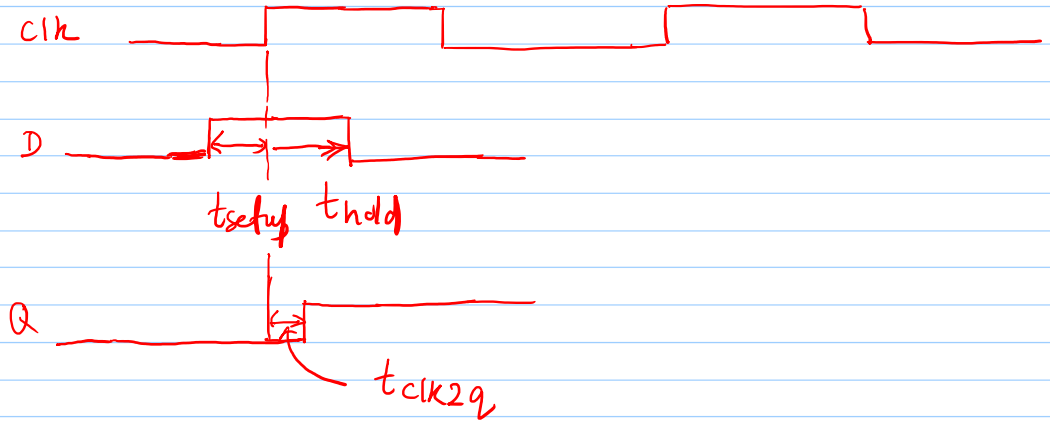
FF has two latches
① Master Latch (1st stage)
② Slave latch (2nd stage)
FF is a +ve-edge triggered in this case.

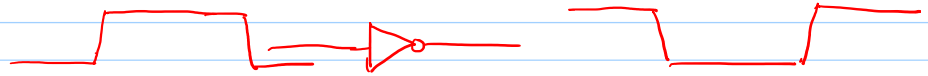
In 1st stage, CLK=0; it samples the input 'D', Hence it -ve Latch.

In 2nd stage, CLK=1, it samples the value in 'Q_M', Hence it is +ve Latch.

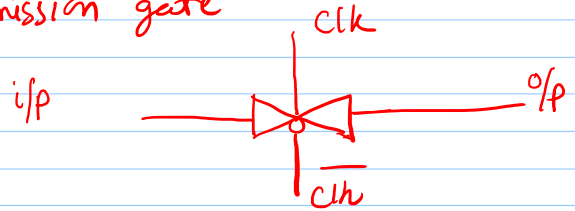
1. Setup time (t_{setup})
2. Hold time
3. t_{clk2q} delay





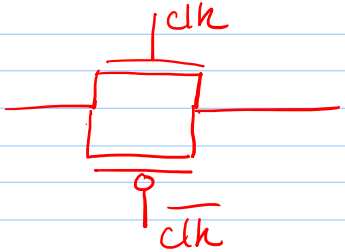


Transmission gate

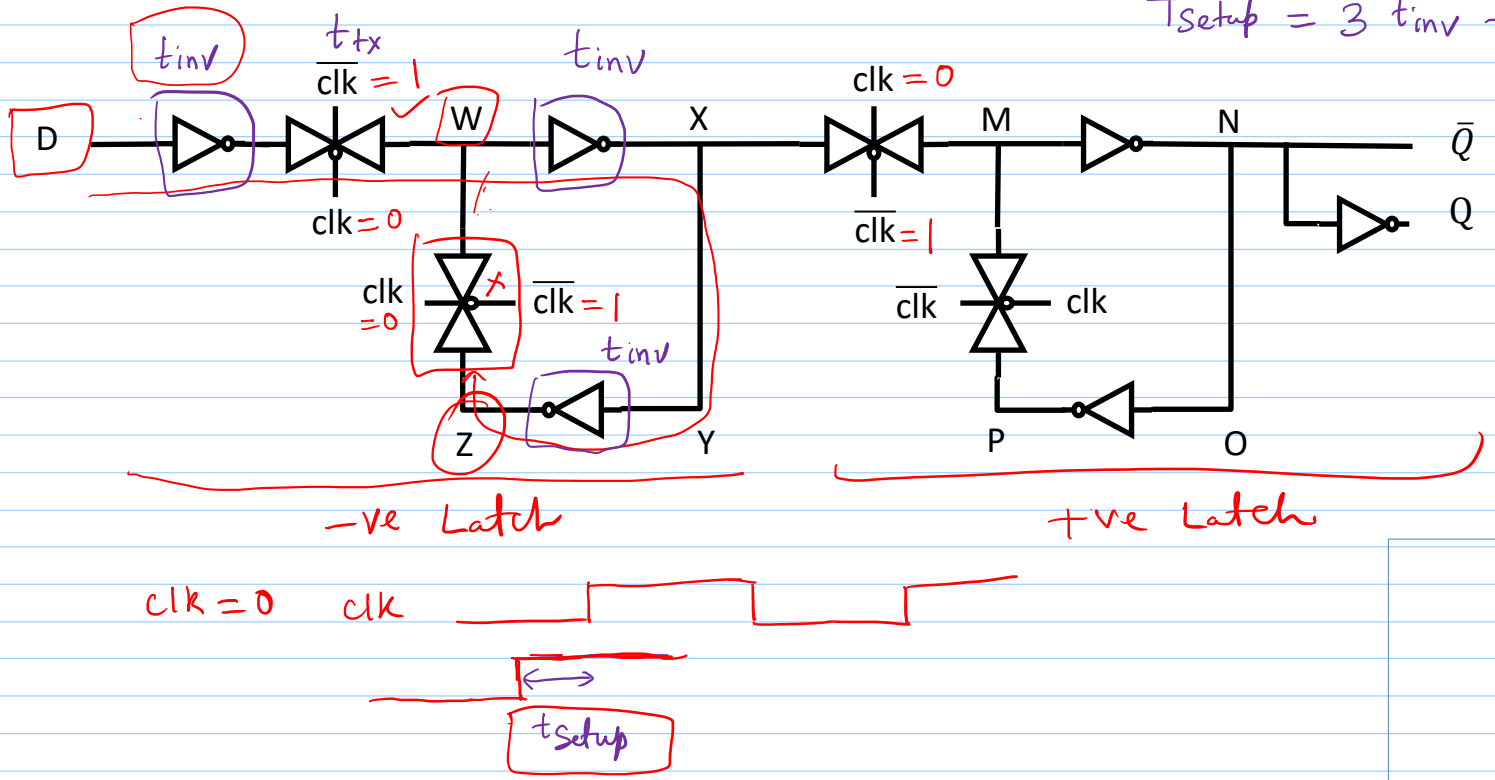


clk = 1 and $\overline{clk}$ = 0 ⇒ o/p = delay version of i/p

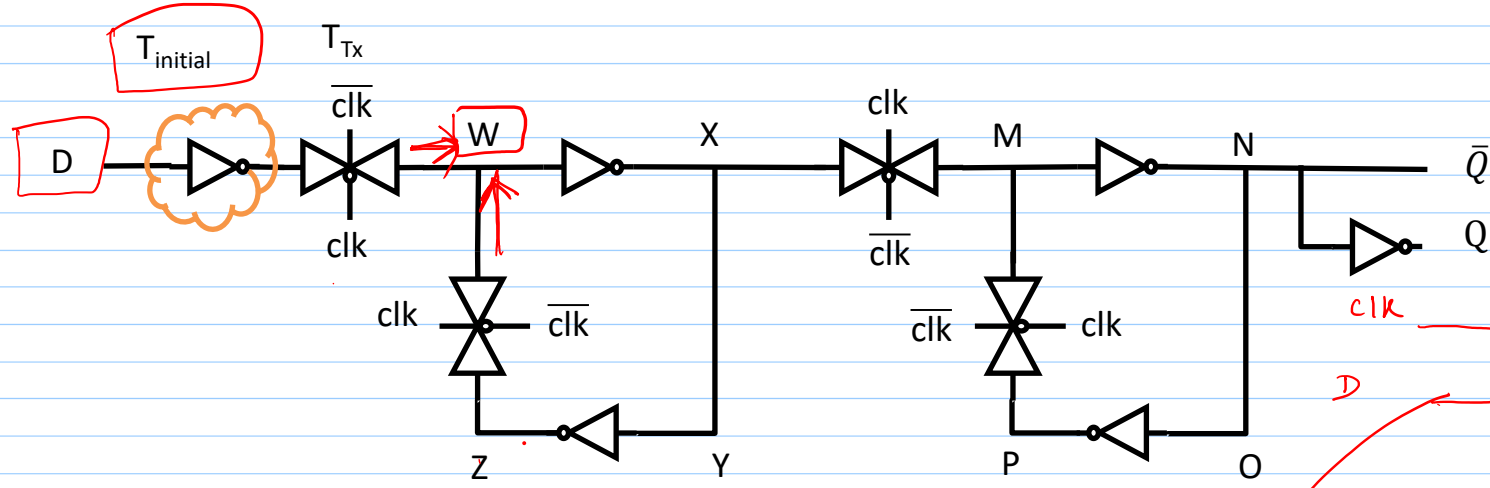
clk = 0 and $\overline{clk}$ = 1 ⇒ o/p

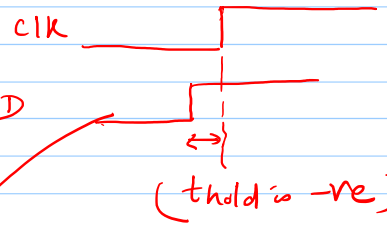


Reason for Setup Time



Reason for Hold Time



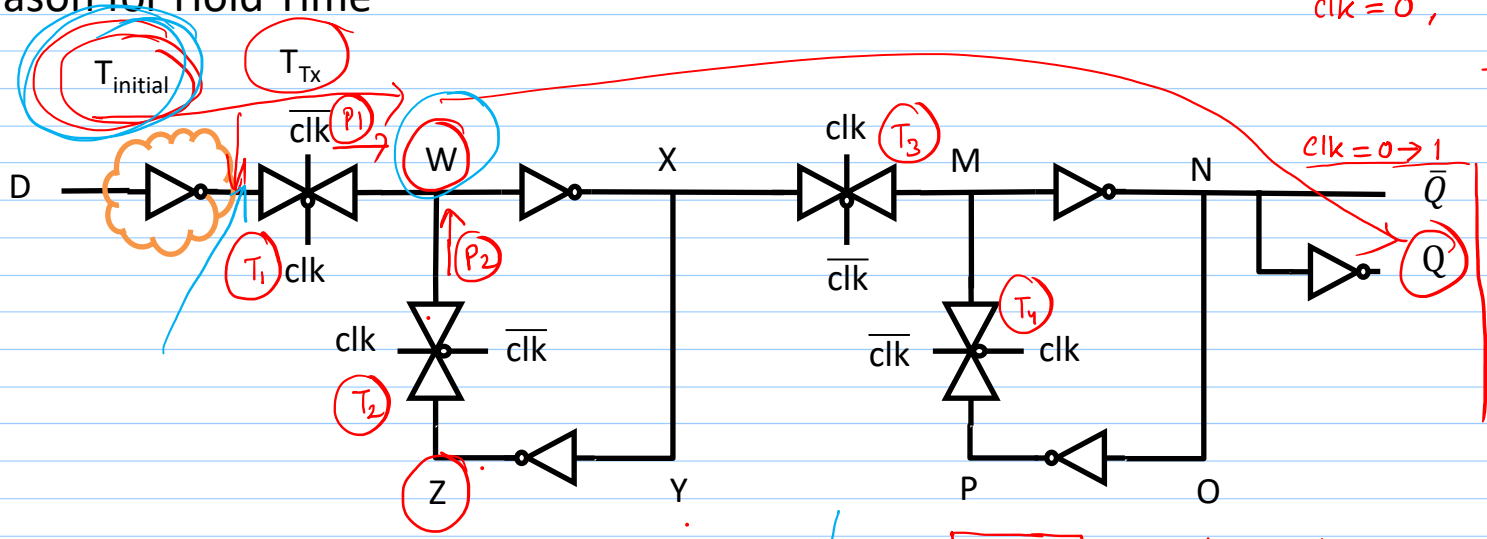


Case 1 : $T_{Tx} > T_{initial}$ → hold time +ve

Case 2 : $T_{Tx} = T_{initial}$ → hold time is 0

Case 3 : $T_{Tx} <$ Tinitial → hold time is -ve

Reason for Hold Time



clk = 0, T_1 and T_4 are 'ON'

T_2 and T_3 are 'OFF'

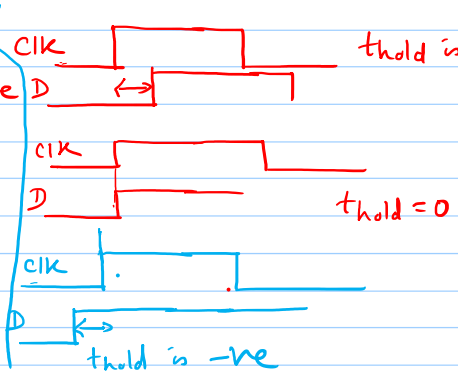
clk = 0 → 1 T_1 and T_4 are 'OFF'

T_2 and T_3 are 'ON'

Case 1: $T_{Tx} > T_{initial}$ → hold time is +ve

Case 2: $T_{Tx} = T_{initial}$ → hold time is 0

Case 3 $T_{Tx} < T_{initial}$ → hold time is −ve



Thank You