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NPTEL ONLINE CERTIFICATION COURSE

VLSI Physical Design with Timing Analysis

Lecture – 7: Overview of Timing Analysis

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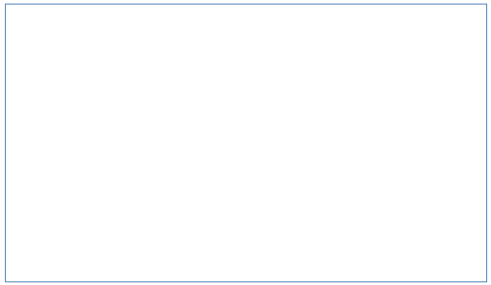
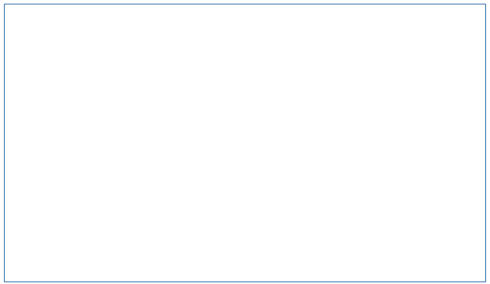
Contents

- Timing Analysis
- Significance of Static Timing Analysis
- STA in VLSI Physical Design
- Static Timing Analysis
- Dynamic Timing Analysis
- Timing Paths



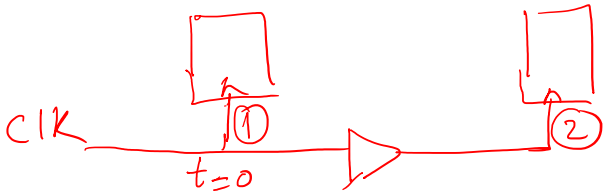
Timing Analysis

- Timing Analysis assesses and ensures that the designed circuit meets timing and performance requirements.
- Timing parameters of the circuit or chip, such as setup and hold times, clock-to-Q delays, and critical paths are evaluated and optimized.

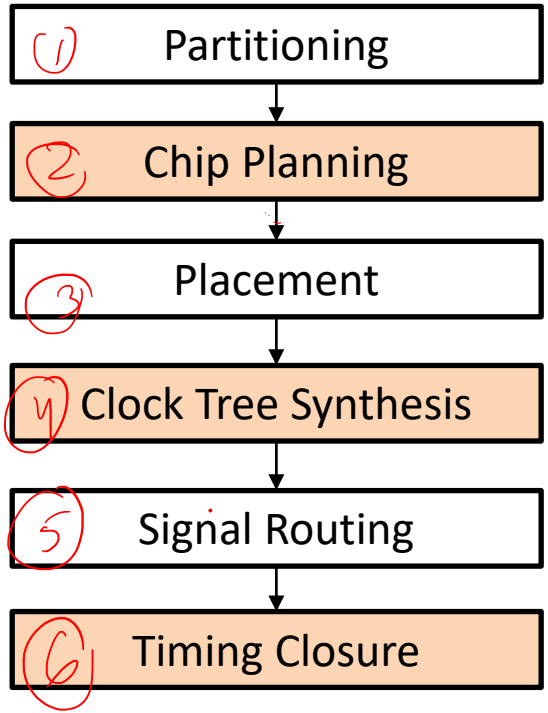


Significance of Static Timing Analysis

- Determines the **critical path** of the design, which in turn determines the performance of the design.
- Determines the **shortest path** in the design (To avoid hold violation).
- Impact of **clock skew** and **clock jitter** on the timing of the design.
- Impact of **process variations** on the timing of the design.



STA in VLSI Physical Design

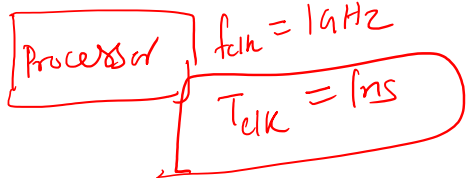


Timing Analysis

- Timing constraints for a chip are tested at a specified clock rate by employing either
  - Static Timing Analysis(STA) or
  - Dynamic Timing Analysis(DTA).

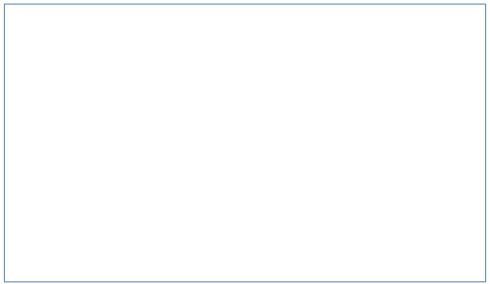
Static Timing Analysis(STA)

- Checks static delay requirements of the circuit without applying input vectors or monitoring output vectors.
- Process of Static Timing Analysis:
  1. Break a design down into **timing paths**.
  2. Calculate the signal propagation delay along each path.
  3. Check for violations of timing constraints inside the design and at the input/output interface.

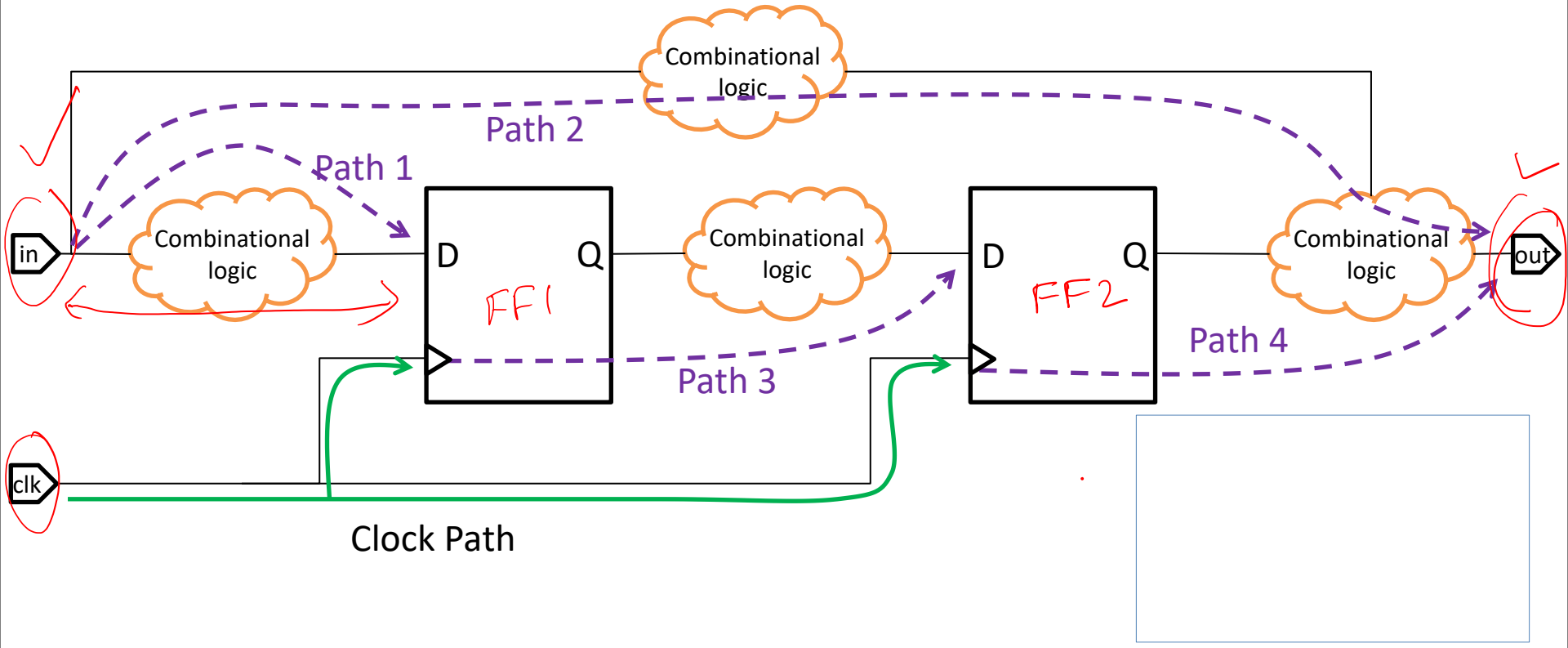


Dynamic Timing Analysis(DTA)

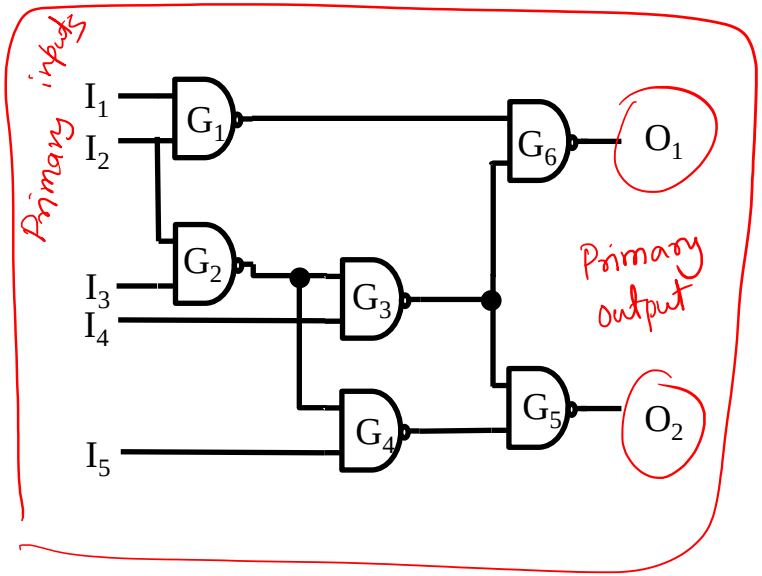
- Verifies functionality of the design by applying input vectors and checking the outputs against expected outputs.
- Checks for logical correctness of the designed circuit.
- Simulation time is relatively more than STA as all inputs need to be checked.
- Best suitable for designs having clocks crossing multiple domains

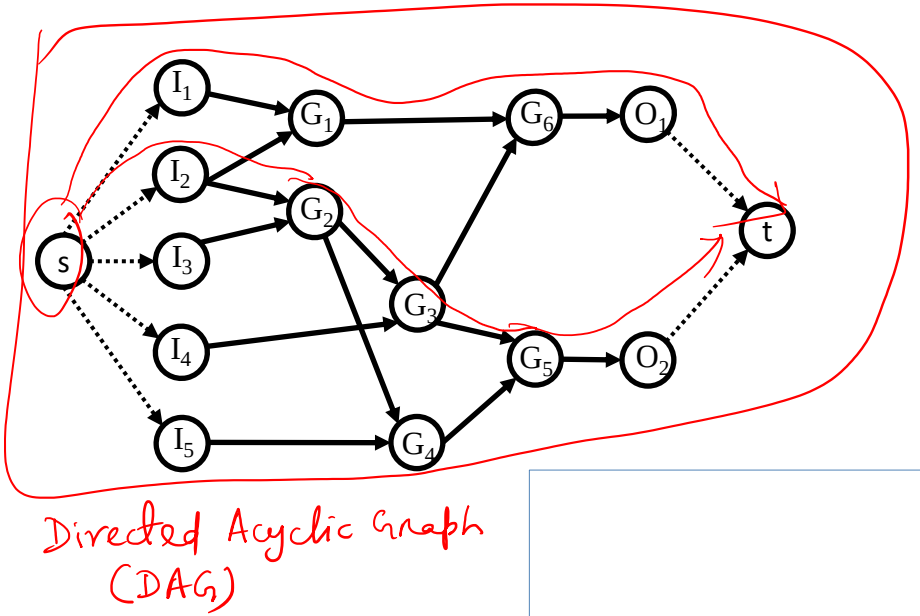


Timing Paths



Timing Paths





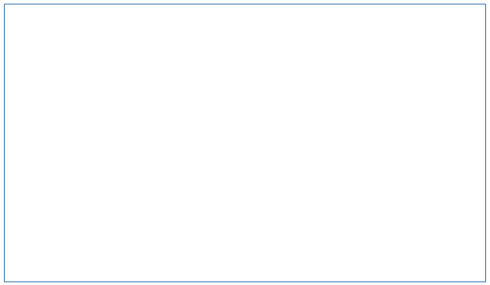
Combinational Logic may have multiple paths

Timing Paths

- Critical Path: The path between an input and an output with the **maximum** delay.
- Shortest Path: The path between an input and an output with the **minimum** delay.

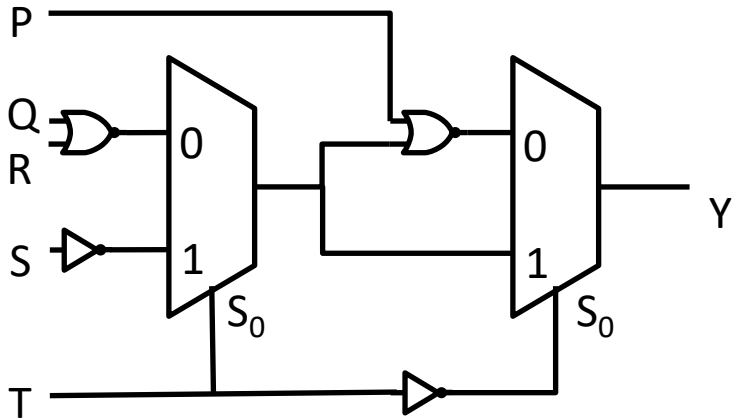
False Path

- A false path is **a path that exists in the design** which:
  1. is not functional; or
  2. is not required to meet its timing constraints for the design to function properly.



Example

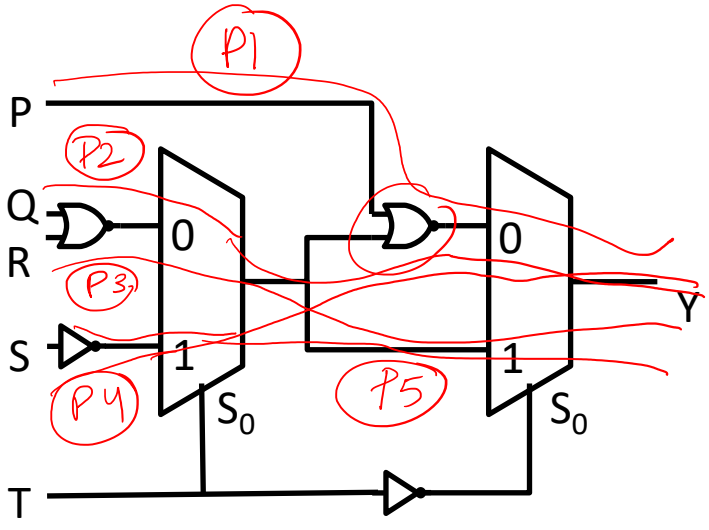
- Let
  - Delay of the NOR gate = 4 ns
  - Delay of the MUX = 3 ns
  - Delay of the NOT gate = 1 ns



- Now, let's find the critical, shortest, and False paths in the given circuit.

Example

- Consider the given circuit
  - It has five paths
    - P1: NOR + MUX
    - P2: NOR + MUX + NOR + MUX
    - P3: NOR + MUX + MUX
    - P4: NOT + MUX + NOR + MUX
    - P5: NOT + MUX + MUX



Example

- Delay of P1 = NOR + MUX

  = 4 + 3

  = 7 ns

- Delay of P2 = NOR + MUX + NOR + MUX

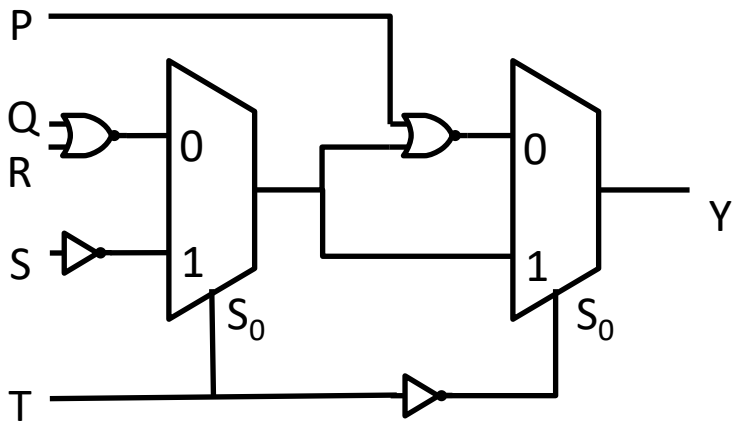
  = 4 + 3 + 4 + 3

  = 14 ns

- Delay of P3 = NOR + MUX + MUX

  = 4 + 3 + 3

  = 10 ns



- Delay of P4 = NOT + MUX + NOR + MUX

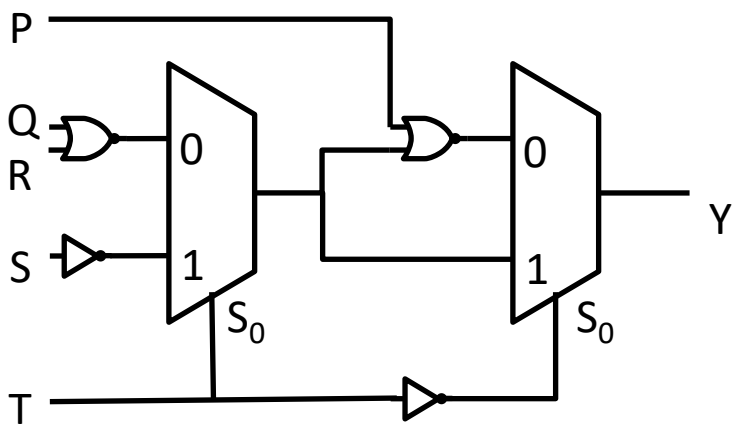
  = 1 + 3 + 4 + 3

  = 11 ns

- Delay of P5 = NOT + MUX + MUX

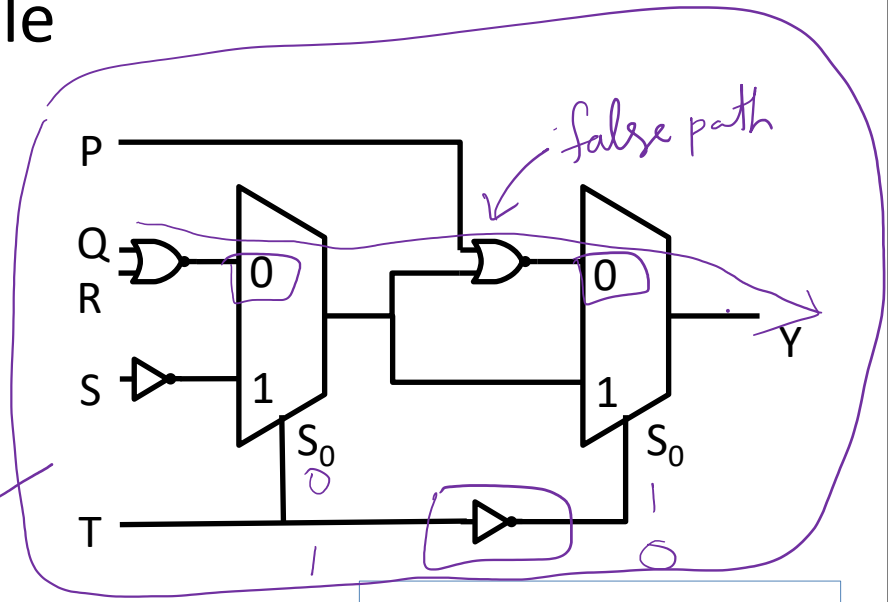
  = 1 + 3 + 3

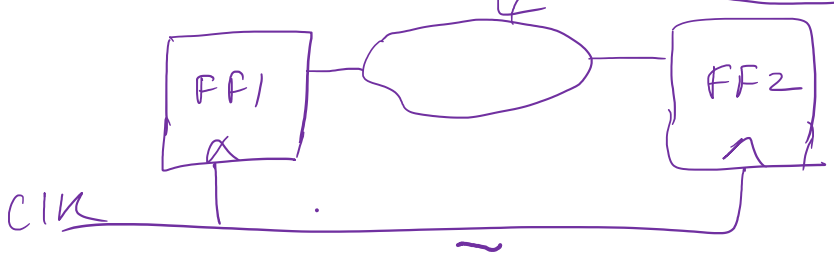
  = 7 ns



Example

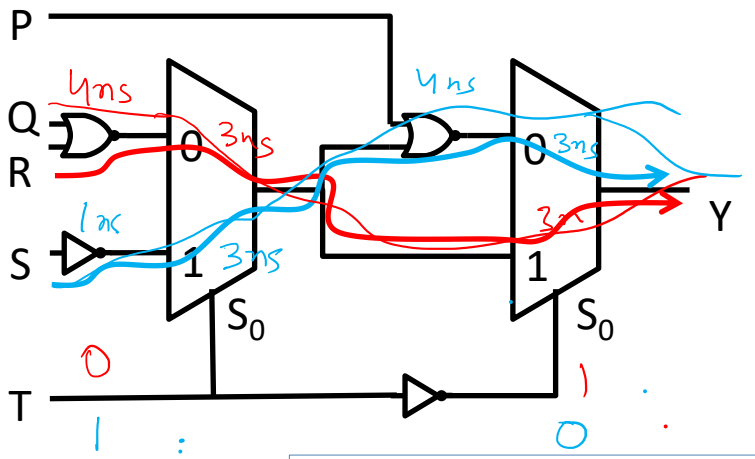
- Delay of P1 = 7 ns
- Delay of P2 = 14 ns
- Delay of P3 = 10 ns
- Delay of P4 = 11 ns
- Delay of P5 = 7ns





Example

- Critical Path:
  - Case – 1: T = 0
    - Delay of P3 = NOR + MUX + MUX
      = 4 + 3 + 3
      = 10 ns
  - Case – 2: T = 1
    - Delay of P4 = NOT + MUX + NOR + MUX
      = 1 + 3 + 4 + 3
      = 11 ns Critical path delay



Thank You