001. If at a time A_0 and BHE (active low) both are zero then, the chip(s) selected will be **C**

A RAM B ROM
C RAM and ROM D ONLY RAM

002. How many pins does the 8255 PPI IC contains? **D**

A 24 B 20
C 32 D 40

003. In which mode do all the Ports of the 8255 PPI work as Input-Output units for data transfer? **B**

A BSR mode B Mode 0 of I/O mode
C Mode 1 of I/O mode D Mode 2 of I/O mode

004. How many bits of data can be transferred between the 8255 PPI and the interfaced device at a time? or What is the size of internal bus of the 8255 PPI? **C**

A 16 bits B 12 bits
C 8 bits D 32 bits

005. To obtain 16-bit data bus width, the two 4K*8 chips of RAM and ROM are arranged in **A**

A parallel B serial
C both serial and parallel D neither serial nor parallel

006. If (address line) A_0=0 then, the status of address and memory are **C**

A address is even and memory is in ROM B address is odd and memory is in ROM
C address is even and memory is in RAM D address is odd and memory is in RAM

007. The semiconductor memories are organized as _____ dimension(s) of array of memory locations. **B**

A one dimensional B two dimensional
C three dimensional D four dimensional

008. To address a memory location out of N memory locations, the number of address lines required is **A**

A log N (to the base 2) B log N (to the base 10)
C log N (to the base e) D log (2N) (to the base e)

009. Port C of 8255 can function independently as **C**

A input port B output port
C either input or output ports D both input and output ports

010. All the functions of the ports of 8255 are achieved by programming the bits of an internal register called **C**

A data bus control B read logic control
C control word register D none of the mentioned

011. The data bus buffer is controlled by **B**

A control word register B read/write control logic
C data bus D none of the mentioned

012. The port that is used for the generation of handshake lines in mode 1 or mode 2 is **D**

A port A B port B
C port C Lower D port C Upper

013. In which of the following modes we do not consider the D6, D5 and D4 bits of the control word? **A**

A BSR mode B Mode 0 of I/O mode
C Mode 1 of I/O mode D Mode 2 of I/O mode

014. How many data lines in total are there in the 8255 PPI IC? **C**

A 8 data lines B 32 data lines
C 24 data lines D None of the above

015. In which of the following modes is the 8255 PPI capable of transferring data while handshaking with the interfaced device? **C**

A BSR mode B Mode 0 of I/O mode

C Mode 1 of I/O mode D Mode 2 of I/O mode

016. In which of the following modes of the 8255 PPI, only port C is taken into consideration? **A**

A BSR mode B Mode 0 of I/O mode
C Mode 1 of I/O mode D Mode 2 of I/O mode

017. In 8251, Modem Control Block performs_____. **C**

A Read and write operation B Converts Parallel data to serial format
C communication between Modem and USART D for reset operation

018. In 8251, _____ signal indicates to the CPU that internal circuit of the transmitter is ready to accept a new character for transmission from the CPU. **B**

A RXREADY B TXREADY
C DSR D CTS

019. In 8251, RxD is a_____ pin. **A**

A Input B Output
C Input or Output pin D no such pin exits

020. In 8251, two control words are present. What are they? **A**

A Mode Instruction control word and command instruction control word B modem control word and command instruction control word
C Mode Instruction control word and stack instruction control word D Mode Instruction control word only

021. In 8086 microprocessor the following has the highest priority among all type interrupts. **A**

A NMI B DIV 0
C TYPE 255 D OVER FLOW

022. In 8251, Transmit buffer block performs_____. **B**

A Converts serial data to Parallel format B Converts Parallel data to serial format
C reading operation D for receiving data

023. What is the purpose of blanking (BI) associated with the 7-segment display operations? **A**
A. To turn ON the display B. To turn OFF the display C. To pulse modulate the brightness of display D. To pulse modulate the lightness of display

A B & C B A & D
C A & B D C & D

024. What does the RAM location at 44H indicates about the 7-segment code? **A**

A 7-segment code for the third character B 7-segment code for the fourth character
C Display of select code for third display D Display of select code for fourth display

025. The popular technique that is used in the integration of ADC chips is **C**

A successive approximation B dual slope integration
C successive approximation and dual slope integration D none

026. Which is the ADC among the following? **D**

A AD 7523 B 74373
C 74245 D ICL7109

027. The conversion delay in successive approximation of an ADC 0808/0809 is **B**

A 100 milliseconds B 100 microseconds
C 50 milliseconds D 50 milliseconds

028. The number of inputs that can be connected at a time to an ADC that is integrated with successive approximation is **C**

A 4 B 2
C 8 D 16

029. The input and output operations are respectively similar to the operations, **C**

A read, read B write, write
C read, write D write, read

030. The time taken by the ADC from the active edge of SOC(start of conversion) pulse till the active edge of EOC(end of conversion) signal is called **C**

A edge time B conversion time
C conversion delay D time delay

031. In 8251, which signal will decide transmission rate? **B**

A Receiver Clock input B Transmitter Clock input
C Clock D Reset

032. In 8 channel-ADC interface how many address lines needed to operate the start of conversion channels? **C**

A 1 B 2
C 3 D 4

033. The device that is used to obtain an accurate position control of rotating shafts in terms of steps is **C**

A DC motor B AC motor
C Stepper motor D Servo motor

034. The priority between the DMA channels requesting the services can be resolved by **C**

A timing and control block B program command control block
C priority block D none of the mentioned

035. When interface 8237 does not have any valid pending DMA request then it is said to be in **C**

A Active state B Passive state
C Idle state D Dual state

036. To complete a DMA transfer, a memory to memory transfer requires **C**

A a read from memory cycle B a write to memory cycle
C a read from and write to memory cycle D a read to memory cycle

037. The number of pulses required for one complete rotation of the shaft of the stepper motor is equal to the **A**

A number of internal teeth on a rotor B number of internal teeth on a stator
C number of internal teeth on a rotor and stator D number of external teeth on a stator

038. A simple scheme for rotating the shaft of a stepper motor is called **C**

A rotating scheme B shaft scheme
C wave scheme D none

039. To save the DAC from negative transients the device connected between OUT1 and OUT2 of AD 7523 is **B**

A p-n junction diode B Zener
C FET D BJT

040. The DAC 0800 has a settling time of **A**

A 100 milliseconds B 100 microseconds
C 50 milliseconds D 50 microseconds

041. Which interrupt mode can be used to handle buffer problems in 8259? **B**

A Edge and Level Triggered Mode B Buffered Mode
C Poll Command D Fully Nested Mode

042. Which register stores all the interrupt requests in it in order to serve them one by one on priority basis? **B**

A Priority Resolver B Interrupt Request Register
C Interrupt Mask Register D Interrupt Control logic

043. 8259A provides_____ vectored interrupts. **B**

A Four B Eight
C Six D Seven

044. When non-specific EOI command is issued to 8259 it will automatically_____. **A**

A Reset the ISR B Set the ISR
C Reset the INTR D set the INTR

045. Which operating mode is preferred when all the interrupts have equal priority in 8259? **A**

A Automatic Rotation
B Automatic End of Interrupt mode
C End of Interrupt mode
D Fully Nested Mode

046. Which mode will decide whether an interrupt should be level or edge triggered in 8259? **C**

A Edge and Level Triggered Mode
B Automatic End of Interrupt mode
C Poll Command
D Fully Nested Mode

047. The mode of 8237 in which the device transfers only one byte per request is **B**

A Block transfer mode
B Single transfer mode
C Demand transfer mode
D Cascade mode

048. _____ is the default operating mode in 8259. **D**

A Special Mask Mode
B Automatic End of Interrupt mode
C End of Interrupt mode
D Fully Nested Mode

049. In 8051, when EA &#39 is held low, code is fetched from_____. **C**

A Internal Program Memory Location
B External Program Memory Location and Internal Program Memory Location
C External Program Memory Location
D Internal Program Memory Location and External Program Memory Location

050. In 8051, when ALE=1 then what happens? **A**

A Port 0 has address from A0-A7 and data, Port 2 has address from A8-A15
B Port 1 has address from A0-A7 and data, Port 3 has address from A8-A15
C Port 0 has address from A0-A7 and data, Port 3 has address from A8-A15
D Port 1 has address from A0-A7 and data, Port 2 has address from A8-A15

051. What is pin no. 40 in 8051? **C**

A ground
B reset
C V_{CC}
D P2.2

052. In 8051, Program Counter stores Address of_____. **B**

A current instruction
B next instruction
C previous instruction
D cannot be determined

053. Which of the following is the features of 8051? **B**

A 16 bit bi-directional data bus
B 16 bit address
C 32 bit data pointer
D 8 bit Stack pointer

054. In 8051, which of the following is an Open drain Bi-directional I/O Port? **A**

A Port 0
B Port 1
C Port 2
D Port 4

055. In 8259, the interrupt control logic **B**

A manages interrupt acknowledge signals
B manages priority of the interrupt
C resets the 8259
D manages the power supply

056. In a cascaded mode, the number of vectored interrupts provided by 8259A is **B**

A 8
B 64
C 16
D 32

057. Which of the following Port in 8051 can be used only as I/O? **B**

A Port 0
B Port 1
C Port 2
D Port 3

058. How many bytes are allocated for general Purpose registers in 8051? **A**

A 80 bytes
B 32 Bytes
C 16 Bytes
D 90 Bytes

059. In 8051, TR1 and TF1 bits are present is in _____ Special Function register. **C**

A IE
B TMOD
C TCON
D SCON

060. In 8051, to select timer 1 and mode 1 what value has to be loaded into TMOD register. **B**

A 0010 0000B
B 0001 0000B

C 0101 0000B D 0011 0000B

061. In 8051, What is the value of over flow flag when we add two hexadecimal numbers 37H+21H? **C**

A 1 B 2
C 0 D 3

062. 8051 has _____ timers/counters_____ bits. **B**

A 1, 8 B 2, 16
C 3, 24 D 3,16

063. How are the bits of the register PSW affected if we select Bank 3 of 8051? **B**

A PSW.4=0 and PSW.3=1 B PSW.4=1 and PSW.3=1
C PSW.4=0 and PSW.3=0 D PSW.4=1 and PSW.3=0

064. In 8051, the default address of Stack Pointer is_____. **A**

A 07H B 08H
C 09H D 10H

065. In 8051, DAA command adds 6 to the nibble if_____. **B**

A If nibble become less than 9 B CY=1 or AC=1 or if nibble become greater than 9
C If nibble become greater than 9 D CY=1 and AC=1

066. In 8051, after performing addition the result will be stored in_____ **B**

A B Register B Accumulator only
C Register D SP

067. In 8051, which of the following is the unconditional Jump instruction? **B**

A JC B JZ
C JMP D JNC

068. Temporary Registers TMP1 and TMP2 can be used only by _____ block in 8051. **B**

A Timer and control B ALU
C Oscillator D PC incrementer

069. For performing Serial Communication using 8051, which Special Function Register are used? **B**

A IP B Both SCON and TMOD
C SCON only D TMOD only

070. In 8051, priority of the interrupts can be changed by using _____ special function register. **A**

A IP B IE
C SCON D TMOD

071. In 8051, which interrupt has highest priority? **A**

A IE0 B IT0
C IE1 D Serial Interrupt

072. In 8051, which interrupt has least priority? **D**

A IE0 B IT1
C IE1 D Serial Interrupt

073. In 8051, To act as counter, the clock pulses are taken from_____. **A**

A P3.4 or P3.5 of 8051 B Clock pulses are sourced from oscillator of 8051
C P 3.6 or P3.7 of 8051 D cannot be determined

074. In 8051, To act as Timer, the clock pulses are taken from_____. **B**

A P3.4 or P3.5 of 8051 B Clock pulses are sourced from oscillator of 8051
C P 3.0 or P3.1 of 8051 D cannot be determined

075. Statement I:8051 has built-in RAM and ROM Statement II: Microprocessor has built-in RAM and ROM **C**

A Both Statement I and Statement II are true B Both Statement I and Statement II are False

C Statement I is true and Statement II is false
D Statement I is false and Statement II is true

076. INC AIf this instruction is executed using 8051 compiler, then what is the value of A after the execution of this instruction if A=FFH? **B**

A 100H
B 00H
C 01H
D FFH

077. In 8051, when CJNE statement is executed _____ flag is updated. **A**

A CY
B AC
C No flag is updated
D Overflow flag

078. In a microcontroller to act as input port we load with _____value. **A**

A FFH
B 00H
C 11H
D 22H

079. In a microcontroller to act as output port we load with _____value. **B**

A FFH
B 00H
C AAH
D BBH

080. While programming the ADC0808/0809 IC what steps are followed? **B**

A select the analog channel, start the conversion, monitor the conversion, display the digital results
B select the analog channel, activate the ALE signal (L to H pulse), start the conversion, monitor the conversion, read the digital results
C select the analog channel, activate the ALE signal (H to L pulse), start the conversion, monitor the conversion, read the digital results
D select the channel, start the conversion, end the conversion

081. In ADC0808/0809 IC which pin is used to select Step Size? **A**

A Vref
B Vin
C Vref/2 & Vin
D Vref/2

082. In 8051, when serial communication is performed then which of the following flag has to be monitored whether the data is transmitted or not? **A**

A TI
B RI
C INTO
D TF

083. External Interrupts are given from which port in 8051? **A**

A P3.2 and P3.3 of 8051
B P3.4 or P3.5 of 8051
C P 3.0 or P3.1 of 8051
D P3.6 or P3.7 of 8051

084. What do you mean by not bit addressable Register in 8051? **A**

A Bit change is not possible
B Bit change is possible
C cannot be determined
D Bit by bit operation can be performed on it

085. In 8051, Which of the following SFR is not bit Addressable? **C**

A IP
B IE
C PCON
D TCON

086. How many times will the following loop execute using 8051 compiler? MOV R6,#10HHERE: DJNZ R6, HERE END **A**

A 10
B 14
C 12
D 13

087. What is described by this command: CJNE A,#00001111b, ROW1 **D**

A it masks the bit and then jumps to the label where ROW1 is written
B it makes the value of the accumulator 0FH and then jumps at the address where ROW1 label is written
C it compares the value of the accumulator with 0FH and jumps to the location where ROW1 label is there if the value becomes equal
D it compares the value of the accumulator with 0FH and jumps to the location where ROW1 label is there if the value is not equal

088. To identify that which key is being pressed, we need to: **B**

A ground all the pins of the port at a time
B ground pins of the port one at a time
C connect all the pins of the port to the main supply at a time
D Both B & C

089. Which of the following steps detects the key in a 4*4 keyboard matrix about the key that is being pressed? **D**

A masking of bits
B ensuring that initially, all keys are open
C checking that whether the key is actually pressed or not
D all of the mentioned

090. Which of the following statements are true about DAC0808? **A**

A parallel digital data to analog data conversion
B it has current as an output
C Both A & B
D None of the mentioned

091. What is the function of the SCLK pin in MAX1112? **B**

A It is used to bring data in
B It is used to bring data out and send in the control byte, one at a time
C It is used to get output clock
D It is used to get serial output

092. How can we control the speed of a stepper motor? **A**

A by controlling its switching rate
B by controlling its torque
C by controlling its wave drive 4 step sequence
D cant be controlled

093. Which of the following can be a unit for torque? **B**

A kg/m^2
B ounce-inch
C $kg\text{-}m^3$
D g/m

094. With a stator having 8 teeth and a rotor having 6 teeth, what step angle will an application be able to achieve? **A**

A 15^o
B 51^o
C 20^o
D 105^o

095. A modern traffic signal system consists of _____ basic subsystems:i) The signal lights in their housing ii) The supporting arms or poles iii) The electric controller **C**

A i& ii only
B i& iii only
C i, ii & iii only
D ii & iii only

096. What is the difference between full-step and half-step? **D**

A In full-step two phases are on and in half-step only one phase is on.
B More resonance is evident in half-step
C More power required for full-step
D Half-step offers better resolution

097. How many data lines are there in a 16*2 alphanumeric LCD? **B**

A 16
B 8
C 4
D 32

098. For writing commands on an LCD, RS bit is **B**

A set
B reset
C set & reset
D None of the mentioned

099. Which command of an LCD is used to shift the entire display to the right? **A**

A 0x1C
B 0x18
C 0x05
D 0x07

100. Which of the following step/s is/are correct for sending data to an LCD? i) set the R/W bit ii) set the E bit iii) set the RS bit **C**

A i& ii only
B i& iii only
C i, ii & iii only
D ii & iii only

101. If the Most Significant Byte (MSB) is stored first while ordering byte values for storing data in memory, it is called as **A**

A Big-endian
B Little-endian

C Big- and Little-endian D None of them

102. How do Direct Addressing Mode instructions compare with respect to the Indirect Addressing Mode instructions? **A**

A Faster B Slower
C No difference D None of the above

103. Evaluate the following statements and select the appropriate answer given from the choices below. I. Von Neumann Architecture shares common memory for Data and Instructions II. Harvard Architecture has separate physical memories for Data and Instructions **C**

A Only I is true B Only II is true
C Both I and II are true D None of them is true

104. ARM processors where basically designed for _____ **C**

A Main frame systems B Distributed systems
C Mobile systems D Super computers

105. The address space in ARM is _____ **D**

A 2^{24} B 2^{64}
C 2^{16} D 2^{32}

106. Memory can be accessed in ARM systems by _____ instructions. i) Store ii) MOVE iii) Load iv) arithmetic v) logical **B**

A i, ii, iii B i, ii
C i, iv, v D iii, iv, v

107. Which of the following register in ARM7 is used to point to the location of currently executing instruction in a program? **C**

A R1 B R5
C R15 D R8

108. Which of the following statements are true with respect to pipelining.I. Pipelining is an implementation technique whereby multiple instructions are overlapped in execution. It is not visible to the programmerII. Each step is called a pipe stage or pipe segmentIII. Pipeline machine cycle is the time required to move an instruction one step down the pipeline **A**

A All are true B I and III are true
C II and III are true D None of them are true

109. Control signals can be categorized by the pipeline stage that uses them. Which one of the following signal could be used in the Execution stage of an instruction? **C**

A MemRead B RegWrite
C ALUop D PCsrc

110. How many bits are required to specify the Register operands in anARM7 instruction? **C**

A 32 bits B 16 bits
C 4 bits D 2 bits

111. Which of the following statements are true? I. In Little endian mode it is easier to determine a sign of the numberII. Little endian mode is easier for addition and multiplication of multi-precision numbersIII. Big endian mode is easier to divide two numbersIV. Big endian mode is easier to compare two numbers **D**

A I & II are true B III & IV are true
C I & III are true and II and IV are false D I & II are false and III and IV are true

112. Consider a 4-bit ALU which does 4-bit arithmetic. When the following 4-bit numbers are added, what is the status of NZCV flags? 1101 + 1011 **D**

A NZCV = 0111 B NZCV = 1000
C NZCV = 1001 D NZCV = 1010

113. Evaluate the following statementsI. R13 is traditionally used as the stack pointer and stores the head of the stack in the current processor modeII. R14 is the link register where the core puts the return address on executing a subroutineIII. R15 is the program counter and contains the address of the next instruction to be fetched **A**

A All the options are true
B I and II are true
C II and III are true
D I and III are true

114. How many registers are there in ARM7? **C**

A 35register (28 GPR and 7 SPR)
B 37registers (28 GPR and 9 SPR)
C 37registers (31 GPR and 6 SPR)
D 35register (30 GPR and 5 SPR)

115. Which type of non-privileged processor mode is entered due to raising of high priority of an interrupt? **B**

A User mode
B Fast Interrupt Mode (FIQ)
C Interrupt Mode (IRQ)
D Supervisor Mode (SVC)

116. Using only two instructions, add a 64-bit integer contained in R2 and R3 to another 64-bit integer contained in R0 and R1, and place the result in R4 and R5. **B**

A ADD r4, r0, r2 ; ADC r5, r1, r3 ;
B ADDS r4, r0, r2 ; ADCS r5, r1, r3 ;
C ADD r4, r0, r2 ; ADD r5, r1, r3 ;
D ADD r4, r0, r2 ; ADCS r5, r1, r3 ;

117. An instruction that is used to move data from an ARM Register to a Status Register (CPSR or SPSR) is called _____. **C**

A MRC
B MRS
C MSR
D MCS

118. Which among the following data processing instructions does not use the barrel shifter? **A**

A ADD R2, R5, R4
B MOV R5, R4, LSL #2
C MOV r5, R4, LSR #2
D MOV r5, R4, ROR #2

119. If the initial register contents of R0, R1 and R2were R0= 0x00000000 R1= 0x02040608 R2= 0x10305070 Assume R0 is the result register, after one of the operations below was performed on R1 and R2, which has been modified to R0 = 0x12345678 What was the operation performed on the contents of R2 and R1? **B**

A AND
B ORR
C BIC
D MUL

120. What are the contents of R1 and R2after MVN R1 R2 are executed, assume R2 is 0x01010101 **B**

A i) R2 = 0x01010101 ii) R1 = 0x01010101
B i) R2 = 0x01010101 ii) R1 = 0x10101010
C i) R2 = 0x10101010 ii) R1 = 0x01011101
D i) R2 = 0x01100110 ii) R1 = 0x01010101

121. In the branch instructions of ARM, what does the mnemonic BVC imply? **D**

A Overflow Set
B Carry Set
C Carry Clear
D Overflow Clear

122. In Cortex-A processor series, which among the following is the standalone and smallest processor in size constraints with high-end application support? **A**

A Cortex-A5
B Cortex-A9
C Cortex-A53
D Cortex-A59

123. Which mnemonic implies plus meaning in the branch instructions? **A**

A BPL
B BEQ
C BMI
D BAL

124. Abort mode generally enters when _____ **A**

A an attempt access memory fails
B low priority interrupt is raised
C ARM processor is on rest
D undefined instructions are to be handled

125. _____ number of non-privileged modes in ARM **B**

A 6
B 1
C 2
D 7

126. Which of the following is not privileged mode **D**

A Abort
B FIQ
C Undefined
D User

127. _____ number of privileged modes in ARM **A**

A 6 B 5
C 4 D 7

128. The built-in NVIC supports up to _____ external interrupt inputs. **A**
A 240 B 120
C 256 D 128

129. How many Stack pointers (SPs) available in the Cortex-M3 processor? **C**
A 4 B 3
C 2 D 1

130. Which bus interface provides access to the Static Random-Access Memory (SRAM), peripherals, external RAM, external devices, and part of the system level memory regions? **B**
A Code memory buses B System bus
C Private peripheral bus D AMBA bus

131. What is the capability of ARM Cortex M3 instruction for second? **B**
A 110 MIPS B 150 MIPS
C 125 MIPS D 130 MIPS

132. Performance of Cortex-M3 processor with CoreMark 1.0 benchmark is **B**
A 1.25 MHz B 3.34 MHz
C 12.56 MHz D 1.98 MHz

133. What is/are the configuration status of control unit in RISC Processors? **A**
A Hardwired B Microprogrammed
C Microcontroller/Microprocessor D RISC/CISC

134. _____ is the feature of Nested Vectored Interrupt Controller (NVIC). i. Nested interrupt supportii. Vectored interrupt support iii. Dynamic priority changes support iv. Reduction of interrupt latency **D**
A i, ii & iii B ii, iii & iv
C iii, iv &i D i, ii, iii & iv

135. The pseudo instruction used to load address into the register is **D**
A LOAD B STORE
C LDR D ADR

136. In the ARM, PC is implemented using_____ **C**
A Caches B Heaps
C General purpose register D Stack

137. What are the Rules for stack use? i) Stack should always be balanced, i.e. functions should have an equal number of pushes and pops ii) Stack accesses (push or pop) should not be performed outside the allocated area iii) Stack reads and writes should not be performed within the free area iv) Stack accesses (push or pop) should be performed outside the allocated area **D**
A i& iii only B ii & iv only
C i, ii & iv only D i, ii & iii only

138. Which stack pointer is used by the operating system (OS) kernel, exception handlers, and all application codes that require privileged access? **A**
A Main stack pointer B Process stack pointer
C PUSH stack pointer D POP stack pointer

139. In the Cortex-M3 processor, the Program Status Registers (PSRs) are subdivided into i) Application Program Status register (APSR)ii) Interrupt Program Status register (IPSR)iii) Execution Program Status register (EPSR) **D**
A i& iii B ii & iii
C i& ii D i, ii & iii

140. The Nested Vectored Interrupt Controller (NVIC) is located in a memory region called the **A**
A System Control Space (SCS) B Advanced High-Performance Bus (AHB)
C Advance Peripheral Bus (APB) D Private Peripheral Bus (PPB)

141. In Cortex-M3 processor, which mode is Used to execute application software? **C**

A Handler mode B Unprivileged mode
C Thread mode D User Mode

142. The System bus interface contains logic that controls bit-band accesses as follows: i) It remaps bit-band alias addresses to the bit-band region. ii) For reads, it extracts the requested bit from the read byte, and returns this in theLeast Significant Bit(LSB) of the read data returned to the core. iii) For writes, it converts the write to an atomic read-modify-write operation. iv) The processor does not stall during bit-band operations unless it attempts to access the System bus while the bit-band operation is being carried out. **D**

A i, ii & iii B ii, iii & iv
C iii, iv &i D i, ii, iii & iv

143. _____ enables reconstruction of program execution. **C**

A Trace Port Analyzer(TPA) B Memory Protection Unit(MPU)
C Embedded Trace Macrocell (ETM) D Data Watchpoint and Trace (DWT)

144. _____ is only used if the bus waits the data phase of the buffered store, otherwise the transaction completes on the bus. **A**

A Write buffer B Bit field
C System address D Load/Store timing

145. Application Program Status register (APSR) access from? **A**

A Any processor mode B Privileged mode only
C Non Privileged mode only D User Mode

146. The benefits of using thumb instruction are as follows **C**

A Low power consumption B High power consumption
C Reduction in code memory D Increase in code memory

147. ARM processors where basically designed for_____ **D**

A Main frame systems B Distributed systems
C Super computers D Mobile systems

148. The offset used in the conditional branching is _____ bits. **C**

A 8 B 16
C 24 D 32