Electrical and Electronics Circuit LAB (EEE F246) LAB Examination

Max. Marks: 20 **Time: 45 Min + 10 Min (Uploading files)**

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1. Design a biasing network in order to implement a CE amplifier in LTSpice for the specifications, V_{CC} = 20V, I_B = 50 µA, V_{CE} = 10V, I_C = 10.58 mA, V_{BE} = 0.717V and Av = 250. Verify whether the biasing is done properly or not. Verify the gain in the mid frequency region by applying a ac small signal at the input.

(Circuit with Calculated Resistances – 8M and Gain verification – 4 M)

2. After the design, calculate the capacitance (C_{C1}, C_{C2} and C_E) and calculate the 3 dB frequency (fL)?

(Calculation of Capacitances – 4 M) and 3 dB frequency (4 M)

Instructions:

1. Upload the. asc file in the link mentioned below. Save the individual files as firstname_lastfourdigits ID (Ex: prateek_0485.asc)

2. Write down the answers all the values of resistances and capacitance calculated using the text command

3. Link for uploading the .asc files: https://forms.gle/9iBF6BxQzuFznPmy9
