Assignment 1: Modelling of Field Effect Nano Devices (EEE 477)

From the Nano-hub Nano TCAD ViDES Tool choose the following parameters for Symmetric Double Gated Silicon Nanowire Transistor simulations:
Channel length: 10 nm
Channel width: 4 nm
Channel height: 4 nm
Supply Voltages: 0.6 V
Source/Drain Overlap: 1 nm
Source/Drain Doping: 1×10^{18} cm^{-3}
Source/Drain Length: 10 nm

Keep all other device/simulation parameters at default values.

Find out the following and incorporate the figure of your simulated I-V characteristics to support your analysis
Perform a comparative transfer characteristics simulations for the below cases keeping V_{DS} = 0.3 V and 0.6 V. In symmetric Front and Back Gates

Effective Oxide Thickness corresponding to 10 nm physical thickness of HfO_2 (k=20)

Effective Oxide Thickness corresponding to 5 nm physical thickness of HfO_2 (k=20)

i) Note the I_{on} and I_{off} for V_{DS} = 0.6 V for each of the above cases and justify your findings from a electrostatic analysis [**5M**]
ii) Analyze the DIBL effects in each of these cases supported by simulation results [**3M**]
iii) Suggest one device engineering technique to reduce the DIBL for the worst DIBL affected device design without changing the gate specifications and channel length [**2M**]

Assignment 2: Modelling of Field Effect Nano Devices (EEE 477)

1. From the Nano-hub Nano TCAD ViDES Tool choose the following parameters for Symmetric Tri Gated Silicon Nanowire Transistor simulations:

Channel length: 10 nm
Channel width: 4 nm
Channel height: 4 nm
Gate height: 5 nm
Front Gate Effective oxide thickness: 1 nm
Back Gate Effective oxide thickness: 3 nm
Supply Voltages: 0.6 V
Source/Drain Overlap: 1 nm
Source/Drain Doping: 1×10^{18} cm^{-3}
Source/Drain Length: 10 nm
Keep all other device/simulation parameters at default values.
Find out the following and incorporate the figure of your simulated I-V characteristics as well as transmission spectrums to support your analysis

Perform a comparative transfer characteristics simulations for the below cases keeping V_{DS} = 0.6 V.
Longitudinal mass = 0.1, transverse mass = 0.1
Longitudinal mass = 0.1, transverse mass = 1
Longitudinal mass = 1, transverse mass = 0.1

i) Note the I_{on} and I_{off} for each of the above cases and physically correlate your findings with effective mass [**3M**]
ii) Analyze the change in transmission spectrums for on-state (at V_{GS} = 0.5 V) condition in each of these cases [**3M**]

2. Based on Level-0 VSM, develop an I_D-V_{DS} model for all region of applied V_{DS} of an n-channel bulk nano-MOSFET that is having 2nm thick Si_3N_4 (bottom insulator) and 1 nm thick HfO_2 (top insulator) stack in the gate region. [**4M**]