

AV 211 - Analog Electronics

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Synthesis of Automatic Gain Control (AGC) Circuit

Analog Electronics Project

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Abstract

The document describes the electronic design of the Automatic Gain Control(AGC) circuit. The document provides step by step detailed approach of various blocks involved in the AGC system designed with suitable fundamental concepts being revised wherever felt necessary. Additionally, LTspice simulations results of the circuit designed is also attached along with experimental observations.

Declaration by the Members

We hereby declare that this document titled “**Synthesis of Automatic Gain Control (AGC) Circuit**” is our original work and is a result of our own efforts. All the sources of information have been duly acknowledged , with appropriate references.

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I. Introduction

In the age of radio circuits and RF technology development, fading of input signal's amplitude received due to various factors like attenuation and propagation losses during transmission and external environmental factors was very common problem . This required continuous adjustments in the receiver's side gain in order to maintain an approximately constant output signal. Such situation led to the design of circuits, whose main objective was to maintain a constant signal level at the output, irrespective of the signal's variations at the input side of the system. Originally, these circuits were designed under the name of Automatic Volume Control (AVC) circuits , a few years later they were generalized under the name of Automatic Gain Control (AGC) circuits.

If the input signal is too low, then the AGC system will increase (amplify) the signal and if is too high, the AGC system will decrease(attenuate) it to maintain a constant level as much as possible.

Nowadays, AGC circuits can be found in any device or system where wide amplitude variations in the output signal could lead to a lost of information or to an unacceptable performance of the system. All modern day receivers are furnished with Automatic Gain Control, which enables tuning to stations of varying signal strengths without appreciable change in the volume of the output signal.In addition, principle of Automatic Gain Control helps to smooth out the rapid fading which may occur during long-distance transmission and reception and indirectly prevents overloading of the amplifying system which might otherwise have occurred.

II. Theory of the Automatic Gain Control system

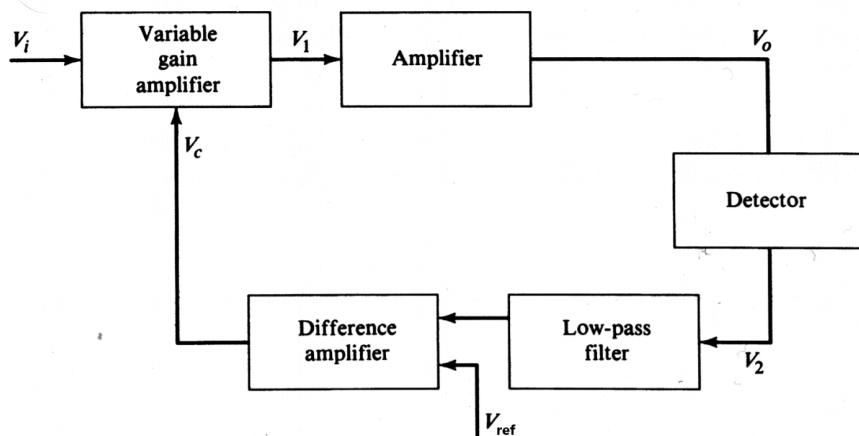


Figure 1: AGC block diagram

Several models have been proposed in the past to design a completely working accurate model of an AGC system. Each model has its own advantages and disadvantages. The trivial models are simpler and easy to design and understand, but they come with high degree of inaccuracy. As the complexity of each block in the AGC system being designed increases, it in turn increases the accuracy and precision of system.

From a practical point of view, the most general description of an AGC system is presented in Figure 1. The input signal is amplified by a **variable gain amplifier** (VGA), whose gain is controlled by an external signal V_c . The output from the VGA is further amplified by a second stage (**fixed gain amplifier**) to generate an adequate level of V_o . The output signal V_o is then rectified and passed through a low-pass filter and the combination of (rectifier + low-pass filter), is what is acting as an **Envelope Detector**. The output of this envelope detector circuit is an approximately constant DC voltage level and this is fed into the next stage's differential amplifier's input. The **differential amplifier** compares the fed back voltage level from previous stage with a predetermined reference voltage level and gives a differential output. The result of the comparison is used to generate the control voltage (V_c) and adjust the gain of the VGA.

In this document, we go by a detailed step by step description of each block associated in Figure-1 of AGC. Note that each block of the AGC can be designed with increasing complexity and each block may have many alternative designs. We come up with a design which draws a trade-off between complexity and accuracy.

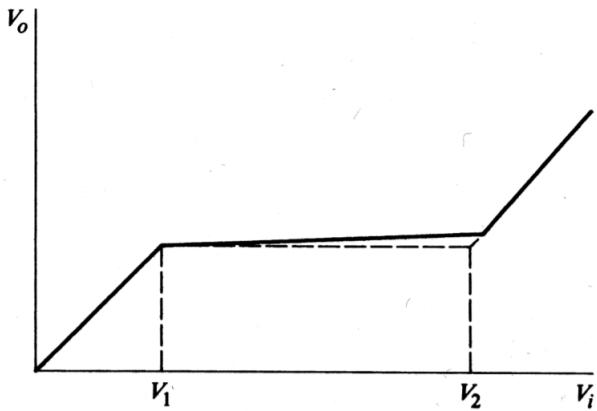


Figure 2: AGC's ideal transfer function

Since an AGC is essentially a **negative feedback system**, the system can be described in terms of its transfer function. The idealized transfer function for an AGC system is illustrated in Figure 2. For low input signals the AGC is disabled and the output is a linear function of the input, when the output reaches a threshold value (V_1) the AGC becomes operative and maintains a constant output level until it reaches a second threshold value (V_2). At this point, the AGC becomes inoperative again; this is usually done in order to prevent stability problems at high levels of gain.

III. Design of AGC System's Circuit

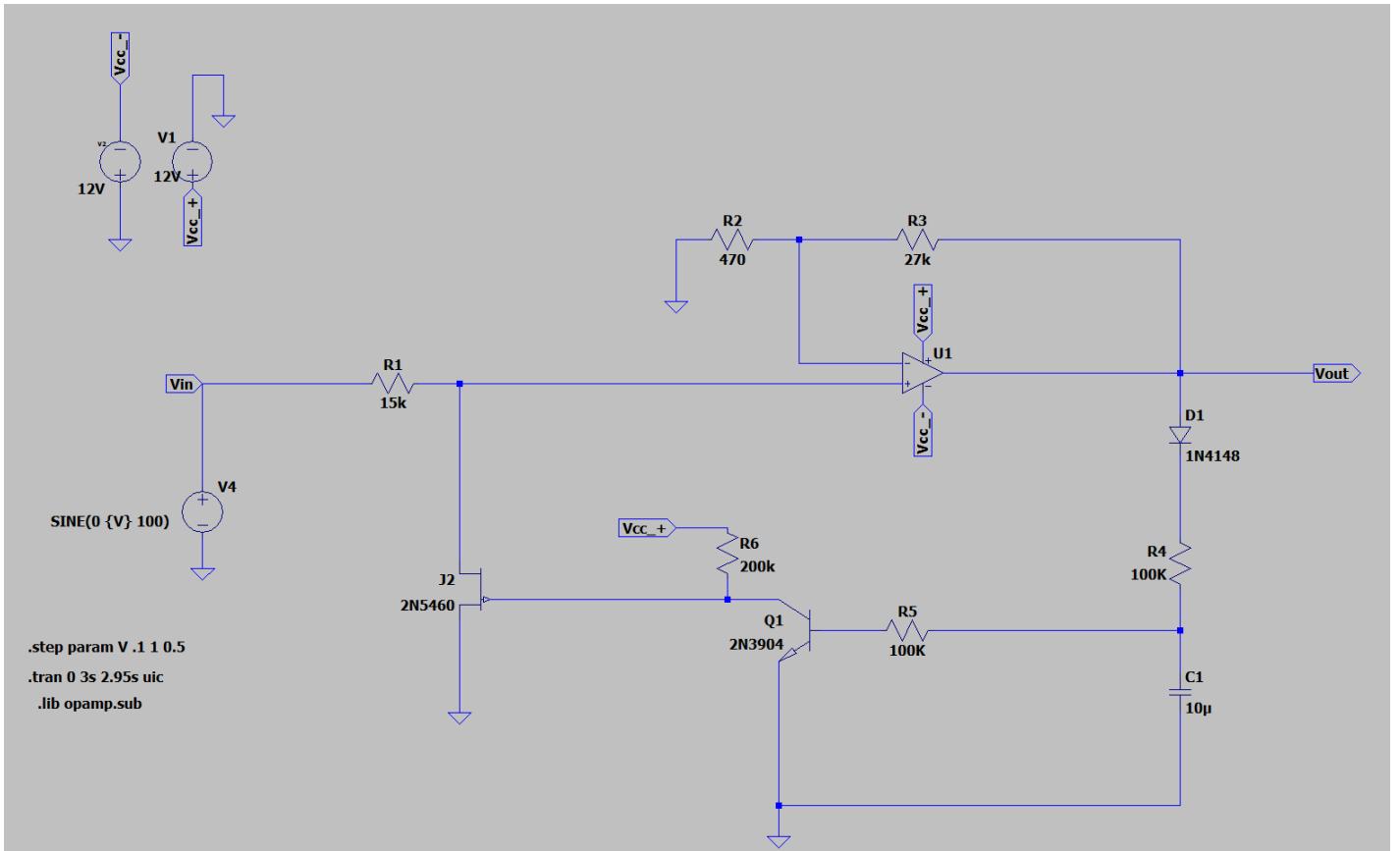


Figure 3: Circuit Schematic of AGC being proposed

The circuit shown above is the schematic of AGC being implemented in the project. The circuit's design parameters such as values of resistors, capacitors being used have been carefully chosen after rigorous testing in lab and as well as in simulations, so as they produce the desired output. Models of BJTs, JFETs and Op-Amps being used have been selected on basis of parameters mentioned in data sheets of the electronic components. Any alternative models may also be used, but the data sheet is to be studied carefully to get the desired output.

From now on in this document, we try to focus on explaining the circuit shown in Figure-3 by sub-dividing it into blocks as shown in Figure-4 and provide the relevant circuit theory behind the block, wherever felt necessary.

Classification of Circuit into Sub-Blocks

- Fixed Gain Amplifier
- Half Wave Rectifier
- Low Pass RC Filter
- Envelope Detector

- CE Mode BJT Amplifier
- Variable Gain Amplifier (VGA)

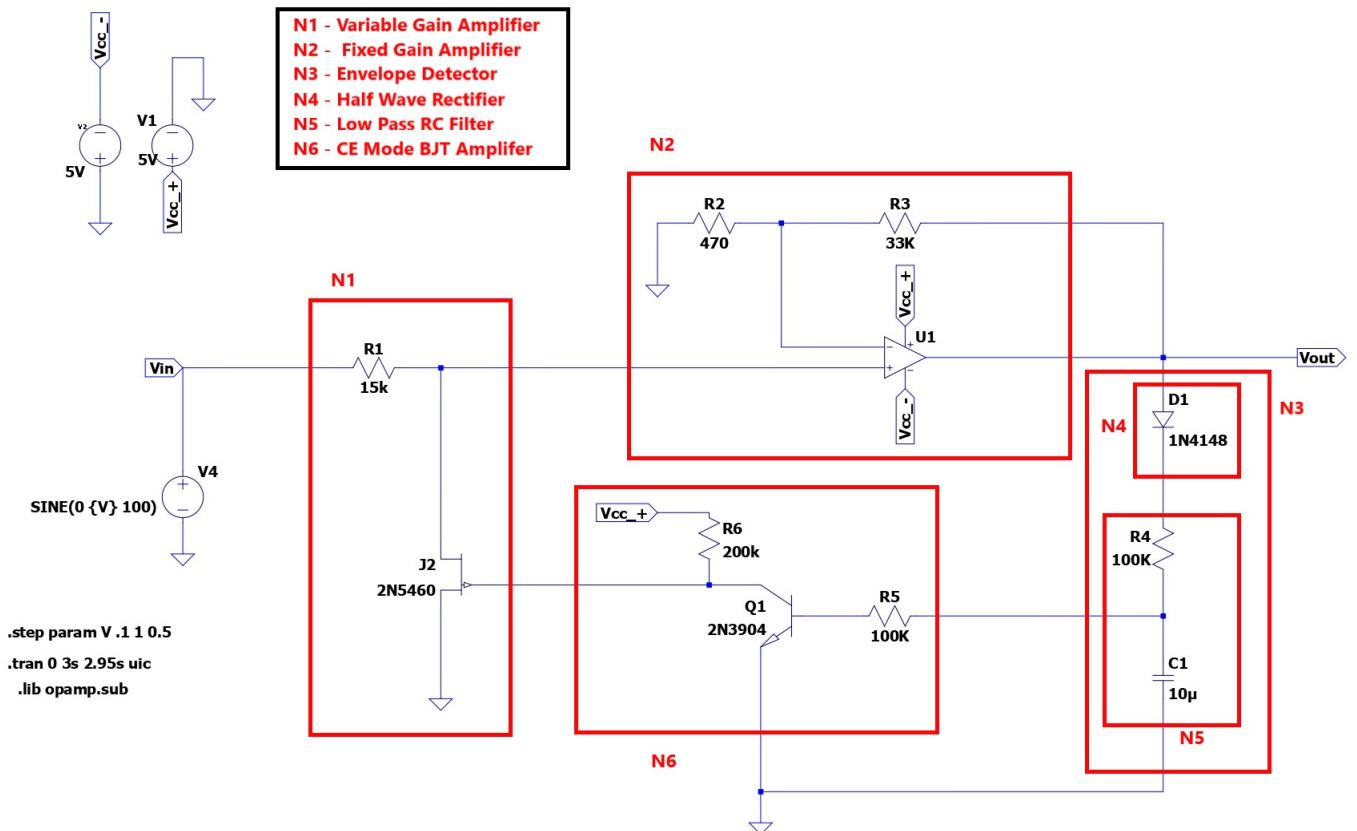


Figure 4: Circuit Schematic of AGC divided into sub-blocks

III . I . Fixed Gain Amplifier

- The fixed gain amplifier block (N2) as shown in Figure-4 is a Non-Inverting Amplifier designed using Op-Amp, provided with proper negative feedback.
- The Op-Amp is provided with sufficient turn on bias DC voltage to ensure it's correct operation.

A simple non-inverting op-amp can be described as the following :-

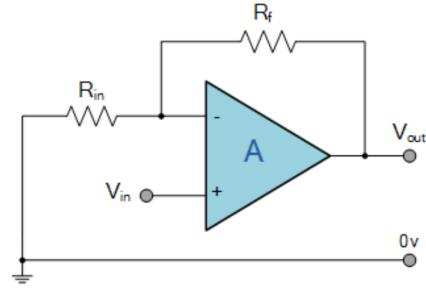


Figure 5: Simple Non-Inverting Op-Amp

From the concept of virtual ground in operation amplifiers, we can easily obtain the following relation between V_{in} and V_{out} :-

$$V_{out} = V_{in}(1 + R_f/R_{in}) \quad (1)$$

III . II . Half Wave Rectifier

- A simple diode connection here, acts as a half wave rectifier .
- In Figure-4 (N4) is a diode D_1 connected, which is forward-biased whenever potential on V_{out} side is higher than the potential on the Low-Pass RC filter side and reverse-biased for the opposite condition.

A simple half-wave rectifier can be illustrated as the following :-

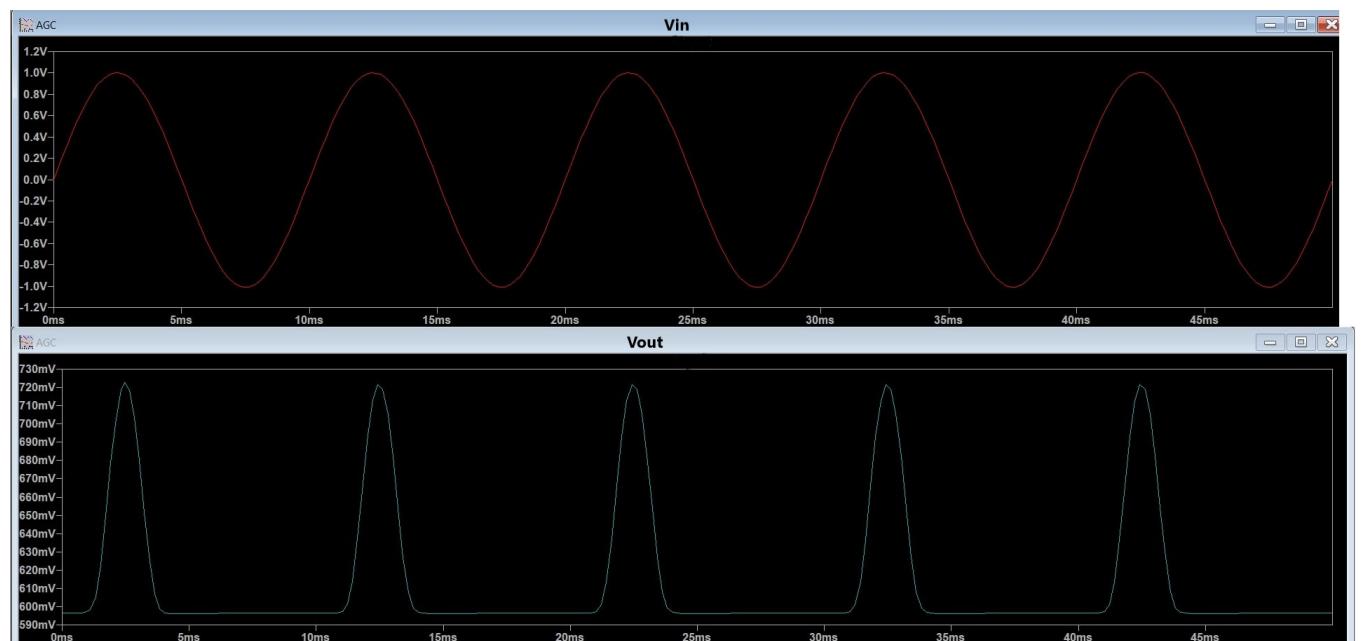


Figure 6: Working of Diode as Half-Wave Rectifier

III . III . Low Pass RC Filter (LPF)

- Whenever a half-wave rectified output passes through a LPF, the capacitor acts as a smoothing capacitor.
- In Figure-4 (N5) the capacitor C_1 acts as a smoothing capacitor and produces an approximately constant DC voltage with very small ripple (negligible).

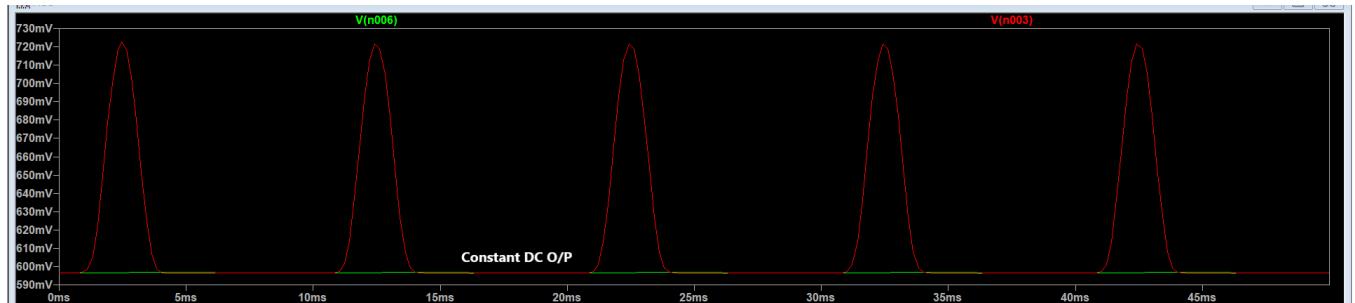


Figure 7: Constant DC output due to smoothing effect of C_1

III . IV . Envelope Detector

- The combination of (Diode + Low Pass RC Filter) together acts as the Envelope Detector circuit.
- In Figure-4 (N3) represents the envelope detecting block module.

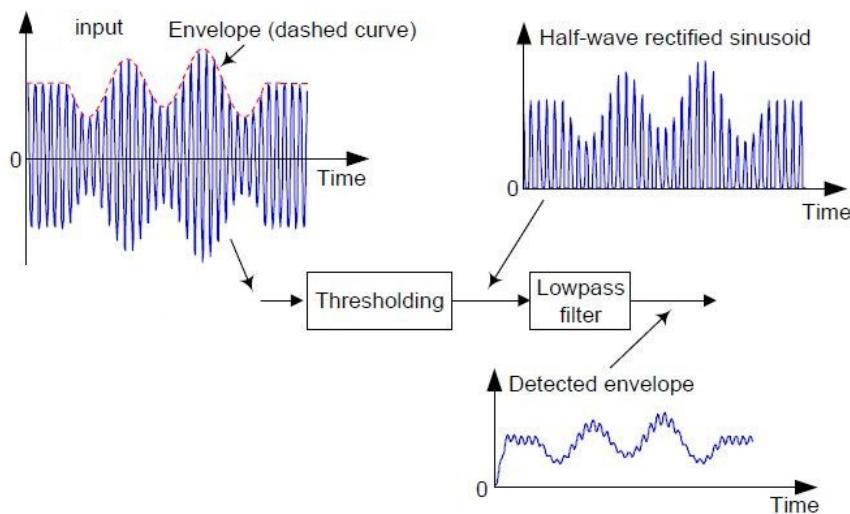


Figure 8: Working of Envelope Detector Circuit

III . V . CE Mode BJT Amplifier

- In Figure-4 (N6) represents the common emitter mode BJT amplifier.
- This is an additional intermediate amplifying stage included so as to ensure that the signal being driven to JFET (i.e. VGA) is sufficiently large enough so that JFET turns on and operates properly .

- We have to ensure that BJT is properly biased using V_{CC} and V_{BE} minimum required is provided to the BJT , so that it turns ON and operates in the Active Region.
- Note that , the BJT when operated in CE Mode produces a 180° phase shifted output with respect to the input provided.

III . VI . Variable Gain Amplifier (VGA)

- In Figure-4 (N1) represents the VGA block .
- It consists of a p-channel JFET . It is simply acting as a voltage dividing block between input signal and the signal being fed into the fixed-gain amplifier stage.
- The concept behind the development of VGA block is that a JFET acts as a **Voltage Controlled Resistor** i.e. based on the Gate to Source Voltage being applied across the JFET , the current through JFET varies.
- The ratio of this current(I_D) and the voltage being applied to JFET (V_{GS}) can be modelled as a resistance(say some R_J) . The value of this resistance is not fixed and is dynamic .
- JFET is governed by the well-known **Shockley's Equation** , which is given as :-

$$I_D = I_{DSS}(1 - V_{GS}/V_P)^2 \quad (2)$$

V_P = pinch-off voltage

V_{GS} = gate-source voltage being applied

I_D = drain-source current

I_{DSS} = saturation current at zero gate-source voltage

IV. Working Mechanism

- Consider the case in which the system receives a weaker signal by an amount of (ΔV) than the nominal signal (V) i.e. the system receives $(V-\Delta V)$.
- Initially, the system will have a natural tendency to give an output of $A(V-\Delta V)$, which is under damped w.r.t the nominal output (AV) that it is expected to give,where A is the gain of Fixed-Gain Amplifying Stage.
- Due to this decrease in output, the voltage being fed back from the Envelope Detector unit to the BJT, will be a constant DC value which is lower than the nominal DC voltage that it produces (say the decrease w.r.t nominal value is some $\delta V_x (\downarrow)$).
- Since we know that BJT produces a 180° phase shift to the output , from the collector of the BJT (this means a decreased input would produce an increased output and vice-versa).Hence, we get an incrementally increased output wrt nominal value (say the increase w.r.t nominal value is some $\lambda V_y (\uparrow)$).
- The output from collector terminal of BJT is fed back into the Gate terminal of the p-JFET. Since the output of BJT has increased by a value of λV_y , the V_{GS} being provided to the JFET has increased ($V_{GS} \uparrow$)

- From equation 2 , we can say that I_D of the JFET has decreased ($I_D \downarrow$) If we consider the resistance that the JFET provides to be as R_J , we can say that R_J has increased w.r.the nominal resistance that JFET offers($R_J \uparrow$).
- Since VGA block is nothing but a simple voltage divider block between input signal and the signal being fed into the fixed-gain amplifier stage, and we see that R_J has increased , so the voltage being fed into fixed-gain amplifier stage increases and eventually the output increases till the nominal constant value, for which it is designed is attained.

$$V_{fed \text{ into } fixed \text{ gain } amplifier} = \frac{(V_{in})R_J}{R_J + R1}$$

- Since $R_J \uparrow$, $V_{fed \text{ into } fixed \text{ gain } amplifier} \uparrow$, $V_{out} \uparrow$ till the nominal set value of output is attained.
- A similar argument can be proposed in the case when the input signal increases by an amount (ΔV) than the nominal signal (V) i.e. the system receives ($V+\Delta V$). In this case , $R_J \downarrow$, $V_{fed \text{ into } fixed \text{ gain } amplifier} \downarrow$, $V_{out} \downarrow$ till the nominal set value of output is attained.
- In this manner, negative feedback ensures that the output remains constant, irrespective of variations on the input side.

V. LTSpice Simulation Results

- Three different signals were given at input and the output was observed and plotted using LTSpice.
- We observe that we get an approximately **constant output signal** for input signals varying over a range of values.

V_{input}	V_{output}
$0.2 \text{ } V_{p-p}$	$1 \text{ } V_{p-p}$
$1.2 \text{ } V_{p-p}$	$0.98 \text{ } V_{p-p}$
$2 \text{ } V_{p-p}$	$0.96 \text{ } V_{p-p}$

Table 1: LTSpice Results

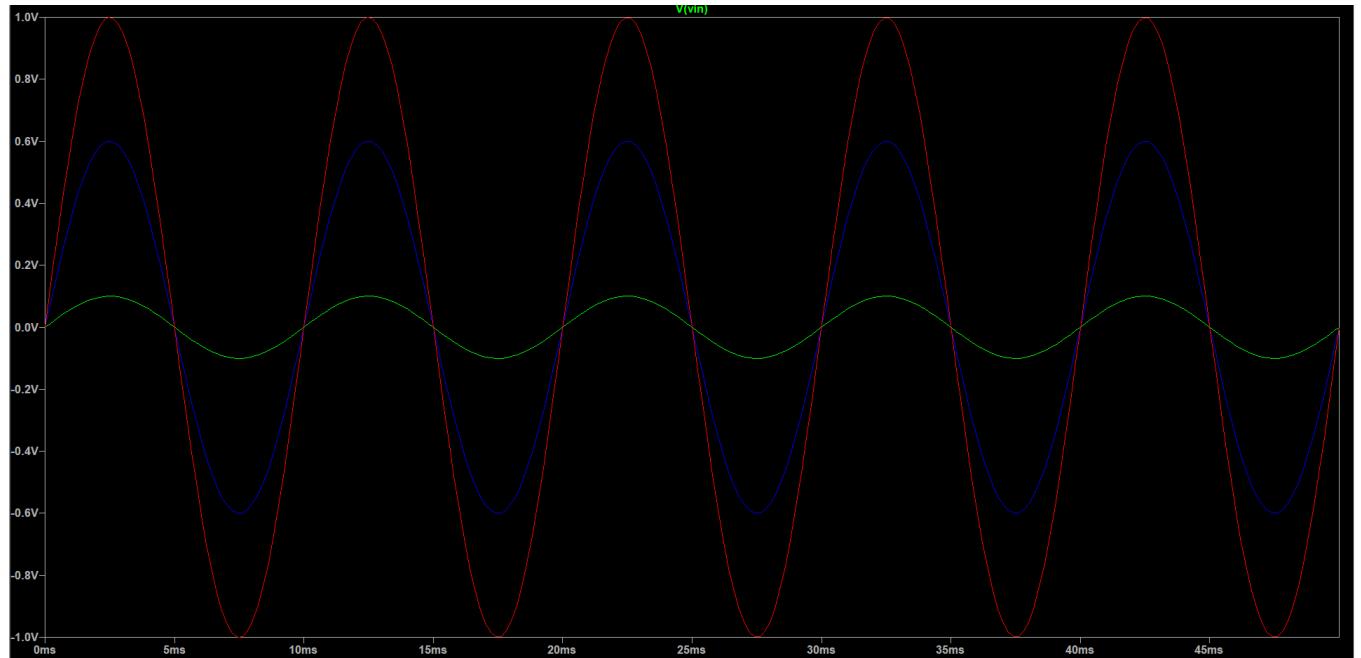


Figure 9: Three different input signals applied

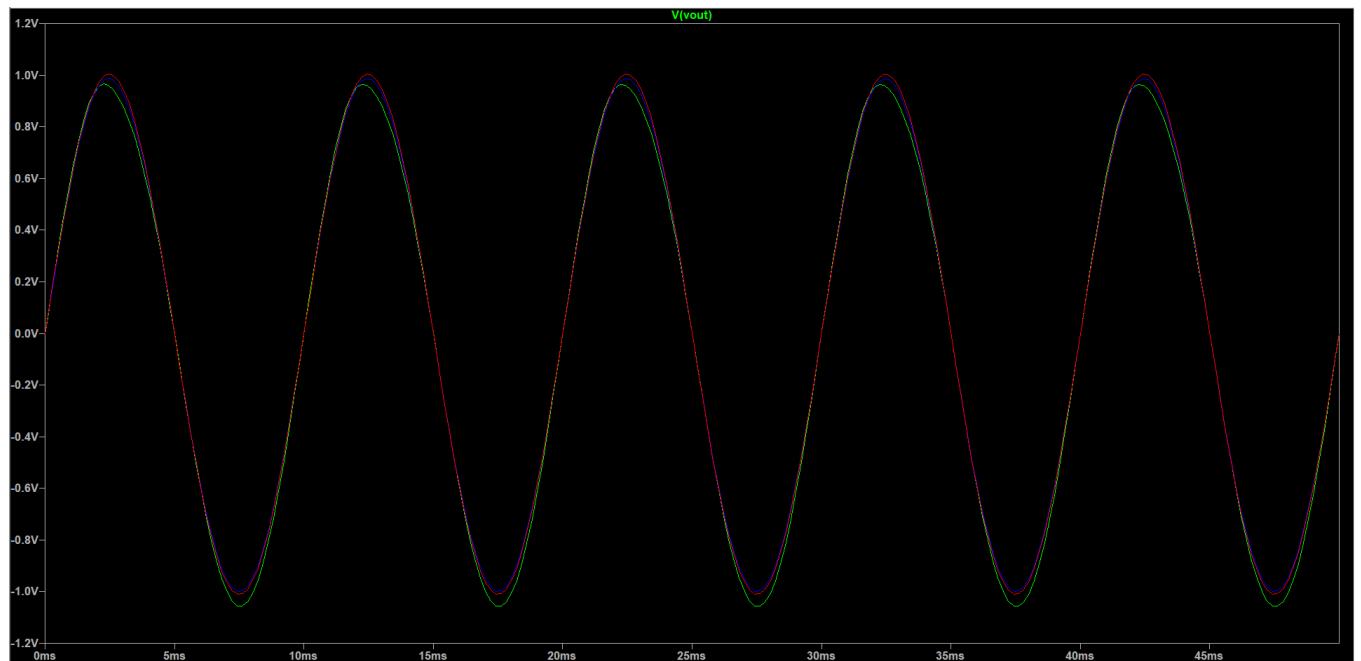


Figure 10: Output observed as constant

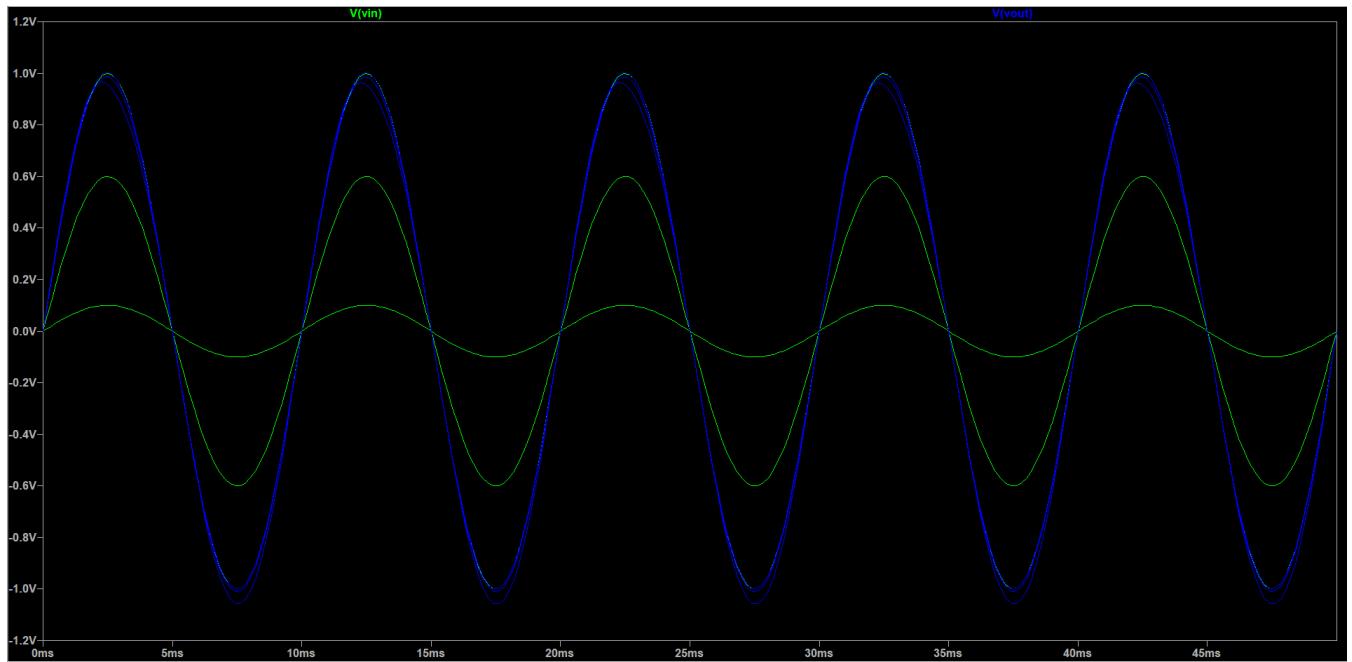


Figure 11: Inputs and Output plotted on a single screen

VI. Experimental Results

$V_{input_{p-p}}$	$V_{output_{p-p}}$
400mV	1.680 V
500mV	1.680V
600mV	1.700V
700mV	1.702V
1V	1.815V
2V	1.920V
3V	2.010V
4V	2.100V
5V	2.175V
6V	2.265V
7V	2.415V
8V	2.450V

Table 2: Experimental Observations



Figure 7: Wave Generator Input $400mV_{p-p}$ (vs) Oscilloscope Output $1.680V_{p-p}$



Figure 8: Wave Generator Input $2V_{p-p}$ (vs) Oscilloscope Output $1.920V_{p-p}$



Figure 9: Wave Generator Input $6V_{p-p}$ (vs) Oscilloscope Output $2.265V_{p-p}$



Figure 10: Wave Generator Input $8V_{p-p}$ (vs) Oscilloscope Output $2.450V_{p-p}$

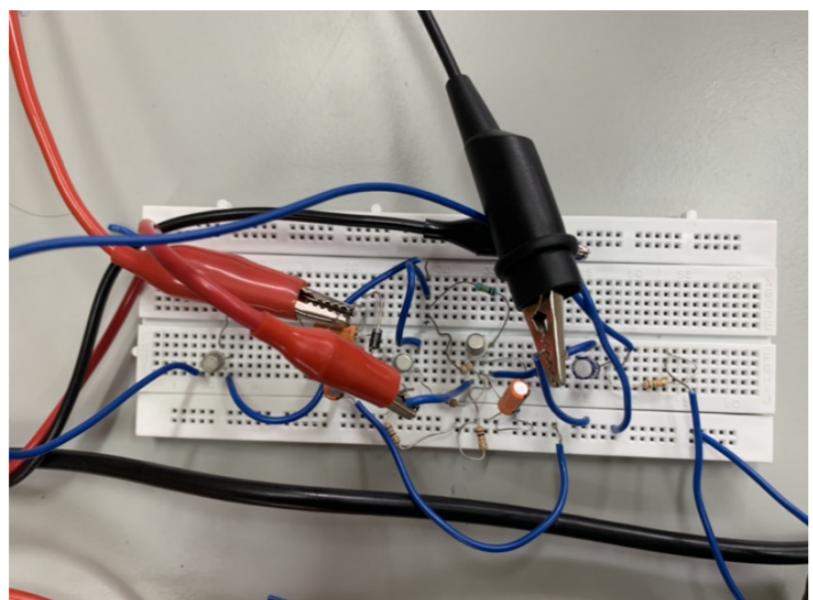
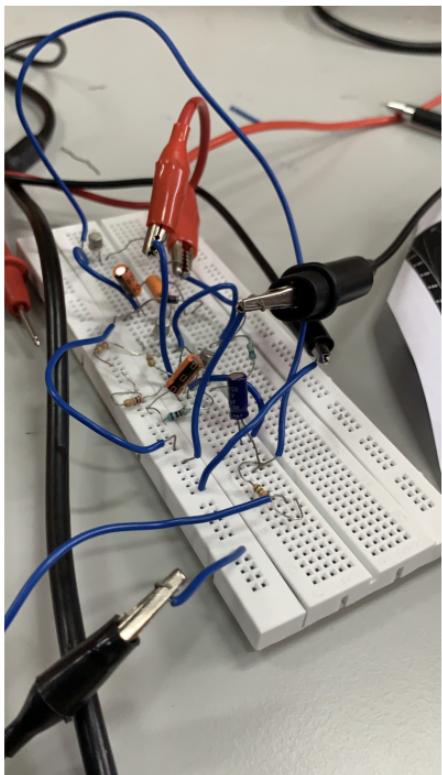


Figure 11: Circuit Realised on Bread-Board in LAB

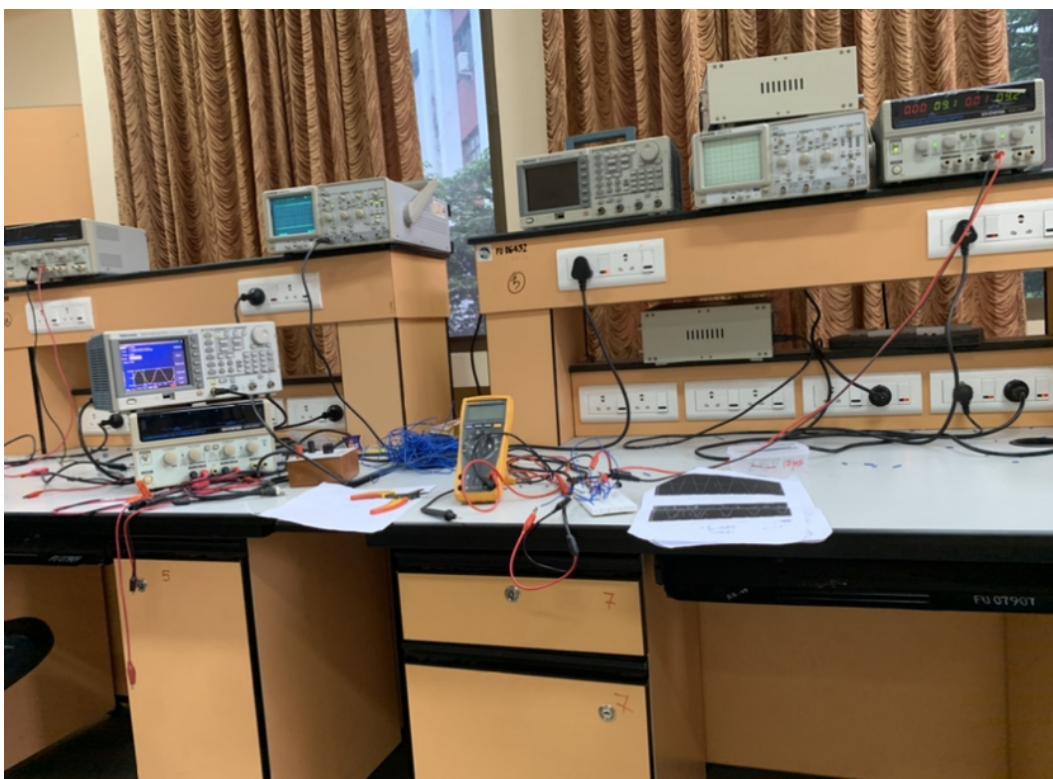


Figure 12: Whole Experimental Test Workbench

VII. Alternative Circuit Approach

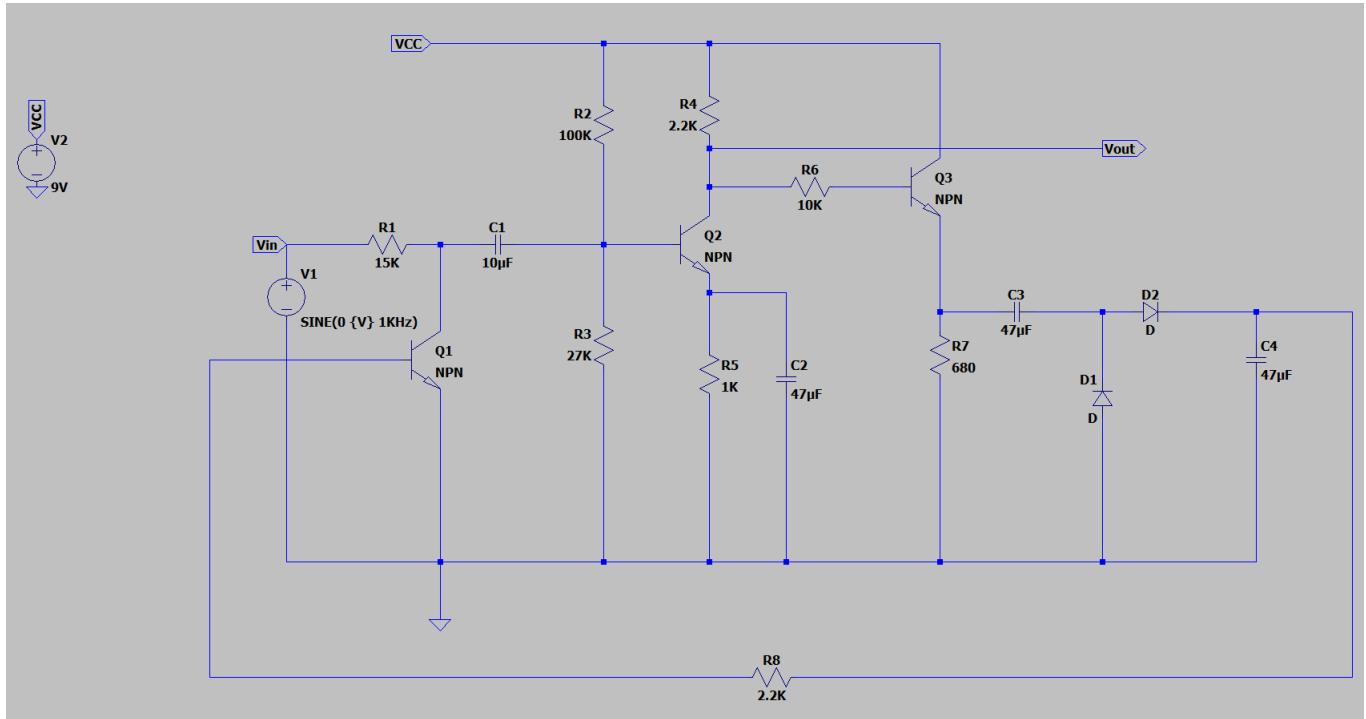


Figure 13: Alternative circuit Schematic of AGC being proposed

VIII. Applications

- AM radio receivers / FM receivers
- Radars
- Audio/video
- Vogad (voice-operated gain-adjusting device)
- Telephone recording
- Microwave Radiometers
- PID Algorithm Implementation in Control Systems

IX. Conclusions

- An AGC system with approximately constant output of $1.9V_{p-p}$, with input varying from $400mV_{p-p}$ to $8V_{p-p}$ was realised using BJT's.
- The deviations observed in the output were due to the tolerances of resistances and capacitors, which is unavoidable in practical cases.
- Also, noises like Thermal/Johnson noise and Flicker noise and some harmonic distortions can be stated as some of the reasons of the deviations seen in practical case.

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