

## **ABSTRACT**

Signal accuracy decides the quality of analogue communications. The most fundamental characteristic of an analogue signal is continuous, where in real-time applications any amplitude or phase error could cause fault for the entire system communications.

Therefore, this project aims to design a signal amplitude and phase control system to detect and fix errors between two input signals. The system consists of two parts: the estimation part is able to detect the amplitude and phase errors respectively and simultaneously. Compared with conventional methods, the estimations of amplitude and phase are achieved by using the same phase comparison technique. Especially for the amplitude measurement, the sum and difference signal of two inputs are produced in terms of driving to the phase comparator to detect the amplitude error using phasor forms. The other part is correction. Unlike the estimation part, this part is a digital signal processing that designed to correct the error detected in the previous part and then provide feedback. Eventually, the two inputs would be matched.

The amplitude and phase control system can be widely used for testing any points of analogue communications, by comparing the real-time signal with the desired reference signal. Also, the system can modulate the signal by a predefined amplitude and phase offsets.

# BRIEF PROJECT OUTLINE

The main contribution and achievement of this project is implementing a signal amplitude and phase control system. A new theoretical methodology is implemented for amplitude error estimation by using same phase comparison technique. This is a type II project that to implement analogue integrated circuit based on mathematic consequences. Also, a control block is designed and implemented using Verilog-A. The following list of bullet points are achieved within project,

- The different techniques of signal amplitude and phase estimation circuits were researched and compared to choose an optimised methodology.
- The mathematic consequence of estimation was presented in details in order to investigate the signal transmission within estimation process.
- An analogue integrated circuit was designed and implemented to estimate and detect any amplitude and phase errors by outputting DC signals.
- The correction block was designed and implemented to control the target signal in terms of tracking the reference signal as a feedback path.
- Different techniques for estimation circuit were implemented and compared in order to increase the ability for the control system becoming able to work for high frequency environments.

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# 1 INTRODUCTION

This project is an analogue integrated circuit design and is simulation based. The specification of the system is to design and implement transistor level analogue circuits to control sinusoid signals. The system contains two sinusoid input signals: one is regarded as the reference signal and the other input is in antiphase with amplitude and phase error. The output of the system should be able to track the reference signal.

The system simulated in this project can be widely used in a signal communication system to detect and fix amplitude and phase errors. In communication, a signal is an electric current or electromagnetic field used to transfer data. For instance, any direct current (DC) signal can present ‘0’ and ‘1’ by switching on and off. Furthermore, an alternating current (AC) is able to deal with more complex cases. In mathematics, the Fourier series decomposes any periodic function or periodic signal into the sum of a set of simple oscillating functions, namely sine and cosine functions (or complex exponentials) [1]. By applying the Fourier transform, signals can be represented in the frequency domain [2]. In this term, any sines and cosines are determined by their amplitude and phase. Therefore, an accurate signal should control its amplitude and phase. To a signal, amplitude is the magnitude of change in the oscillating variable with each oscillation within an oscillating system. Take the example of a sine wave: the amplitude is the peak value in the time domain while oscillating. On the other hand, a periodic function has elapsed, and is measured from some fixed origin. If the time for one period is expressed as  $360^\circ$  along a time axis, the phase position is called the phase angle. Thereby, phase difference is the difference between two waves having the same frequency and referenced to the same point in time. The total phase difference can be expressed in degrees from  $0^\circ$  to  $360^\circ$ , or in radians from 0 to  $2\pi$ . The antiphase is defined as occurring when the phase difference is 180 degrees ( $\pi$  in radians). Regarding the amplitude and phase, the signal estimation consists of two parts, the amplitude comparison and phase difference circuit.

The technique implemented in signal estimation was phase comparison for both amplitude and phase estimations. The phase part is straightforward, and the amplitude error was detected by comparing the phase difference between sum and difference signal of the inputs. Based on the theoretical consequence (in section 4.4), 90 degrees between sum and difference signals represented the error free situation; in other words, the estimation of amplitude can be detected as a DC voltage. Similarly, the output of estimation was a DC signal, detecting the amplitude and phase error respectively.

The second stage of this project was to use the detected DC voltage error offset to control the input signal to eventually track the reference signal. Verilog-A was used to correct the error. In analogue communications, Verilog-A is a standard modelling

language for analogue circuits widely used in industry. It is an extension of Verilog as a hardware description language. The advantage of Verilog-A is that it only requires analogue simulation tools (Cadence) during simulation instead of building the actual analogue circuit. Also, it can model analogue behaviours of digital circuits. However, the major drawback of this language is that it is difficult to model complex digital systems. Associated with this project, the DC signal is simple enough to process. A feedback loop was implemented to control the error signal and continuously compared to the reference signal depending on the sampling frequency of feedback loop.

As the second stage was digital communication depended on the sampling frequency, the working frequency of the control system was determined by the analogue estimation. For this project, the maximum frequency allowed for system was around 60MHz. Input signals beyond this frequency range caused the distortion. Referring to the discussion in section 5, the estimations were limited to the frequency response of the operational amplifier (OPAMP). Furthermore, compared to the discussion for ideal OPAMP in section 4.7.1, a high gain ensured the input impedance became infinite so that no current would cost for the input. However, considering the size of the fabrication level simulated in this project was 180nm, a large transconductance and capacitance was carried out. It caused the current flowed into input terminal while a relatively high frequency loaded. Therefore, the smaller scaling transistor provided faster operation in order to further increase the working frequency.

## 2 AIM AND OBJECTIVES

### 2.1 Aim

The aim of this project is to design, simulate, optimise and test a signal amplitude and phase control system based on phase comparison technique.

### 2.2 Objectives

- Research and compare the different technologies of signal amplitude and phase comparison circuits in order to choose an optimised design that uses fewer components in a signal control system.
- Study and understand the new approach of using phase comparison technique and implement a signal amplitude and phase estimation circuit.
- Design, implement and test a feedback block.
- Use software to design and simulate the transistor level schematic of the signal control system.

- Test the system with wide range of input signals to evaluate the signal control system.

### 2.3 Scope

The project covered both analogue and digital signal communication. The first part of project is to detect the amplitude and phase error. This part is an analogue integrated circuit design in terms of processing an analogue signal, which is a sinusoid wave. The purpose of the second part is to correct the amplitude and phase errors. Unlike the first part, this was achieved by coding, using digital signal processing. Essentially, digital signal processing is much more fixable and convenient. Different functions of digital processing can be easily changed dependent on design specifications. For instance, the filter design: the digital filter can be easily implemented by calculating and storing the coefficients in registers. Any signal can be filtered by convolution. On the other hand, the analogue filter design should be calculated to choose the components (resistors and capacitors); the accuracy is less than digital design as components can have errors. Also, it is specific, as any change requires to recalculation and choosing a new component. However, the analogue communication provides a continuous signal. The digital signal processing is limited to the speed of analogue-to-digital conversion as the digital communication is discrete. The lower the sampling frequency, the more data will be lost. Therefore, high frequency is a significant judgement for the signal amplitude and phase estimation. According to the theoretical consequence, the amplitude and phase error can be represented in DC output. If the DC signal is settled as a constant, the digital communication can be used in the second part of project, the correction. Therefore, another significant judgement for the signal amplitude and phase estimation is stability.

## 3 BACKGROUND AND CONTEXT

### 3.1 Amplitude and phase estimation

This section will discuss the relevant amplitude and phase comparison respectively.

#### 3.1.1 Amplitude comparison circuits

In this section, the discussion will focus on different signal amplitude comparison circuits. Within each method, in the subsection, the key circuit elements will also be evaluated.

##### 3.1.1.1 Signal amplitude comparator with non-linear pair circuit

A signal amplitude comparator [3] had two inputs, one was the input signal and another was the reference signal. The circuit of amplitude comparator included an amplifier, a filter and a comparator, showed in following diagram.

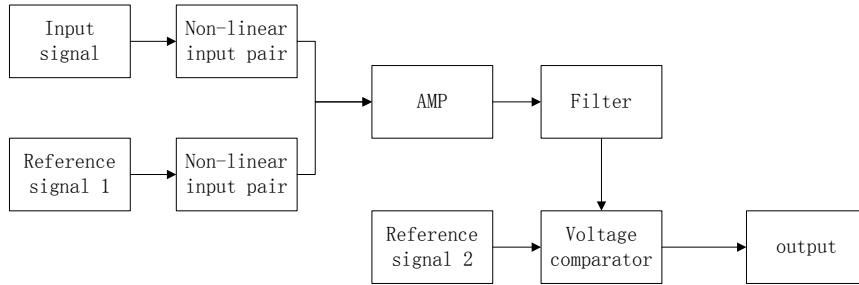


Fig 3.1 Amplitude comparator with non-linear pair circuit

Refer to the block diagram showed in figure 3.1, the signal comparator included two differential input circuits. The first differential received an input signal and generated an output signal that was a non-linear function of the input signal. Meanwhile, the second input circuit received a reference input signal 1 and generated a second output signal that generally track process, temperature and supply variation. The signal amplitude comparator also included an amplifier, a filter and a comparator. The amplifier amplified a signal difference between the first and second output signals and outputted a train of pulses if a peak of the input signal exceeded the reference input signal. A second reference signal was applied to the comparator, which generated an output which indicated whether the input signal exceeded a pre-determined threshold value. The signal amplitude comparator also included a pair of input amplifiers, which received and translated the input and reference input signals to levels suitable for the input circuits. The advantage of this design included two main aspects. Firstly, the design was able to detect the presence or absence of high frequency signals in a system. The second was, by using of a second threshold, to make a circuit more sensitive to the peak amplitude of a signal applied to the circuit. Generally, this design provided a better signal level than operation in linear mode for a given power level at a given offset

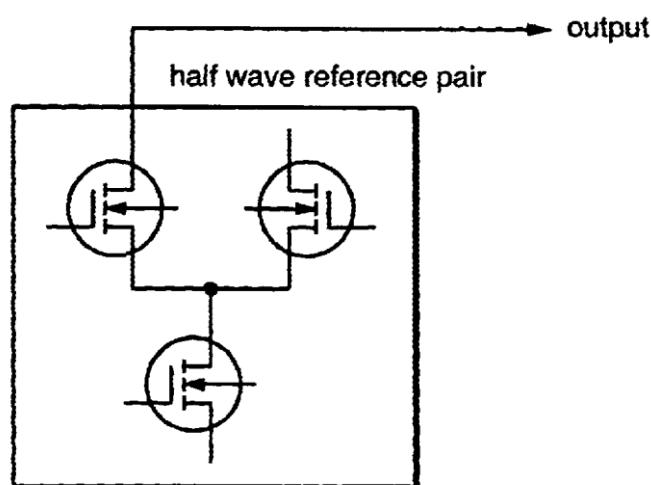


Fig 3.2 Half wave reference circuit

(Reference: <http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/rectifiers.html>)

The circuit showed above illustrated the structure of the input circuit. It made of pairs of the transistor, connect to both of input signal and reference signals.

### 3.1.1.1.1 Peak amplitude comparator

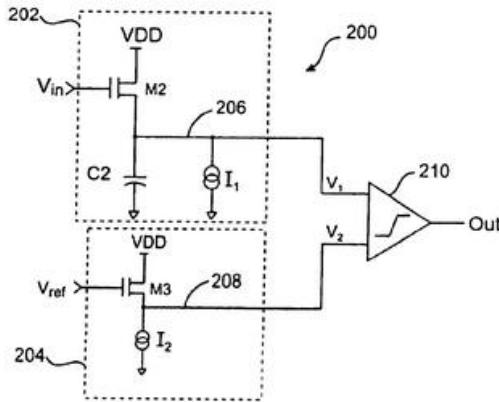


Fig 3.3 Amplitude compare circuit

(Reference: <http://newton.ex.ac.uk/teaching/cdhw/Electronics2/SimSheet-04.html>)

Figure 3.3 presented a possible circuit for amplitude comparison circuit [4] associate with the block diagram showed in figure 3.1. The peak amplitude comparator circuit provided comparison of two parts. The first part was input circuit receiving an input signal. It stored a first signal with amplitude which initially equal to a peak amplitude of the input signal minus a predetermined voltage drop in order to generate the stored first signal and send to output terminal. Similarly, another circuit received the reference signal. Then, the magnitude of two signals will be compared to detect the differential signal. The differential signal will be used to drive the switch. For instance, the switch will be turned on to charge a capacitor when the input signal increases in amplitude, and turning off when the input signal starts to decrease. This design was sensitive to detect the amplitude difference in high speed operation. However, it still have the limitation because of the feedback circuit, say GigaHz rang was not able to run in this design. Nevertheless, this design provided an example of compare the voltage or amplitude of two input signals.

### 3.1.1.1.2 Voltage comparator circuit

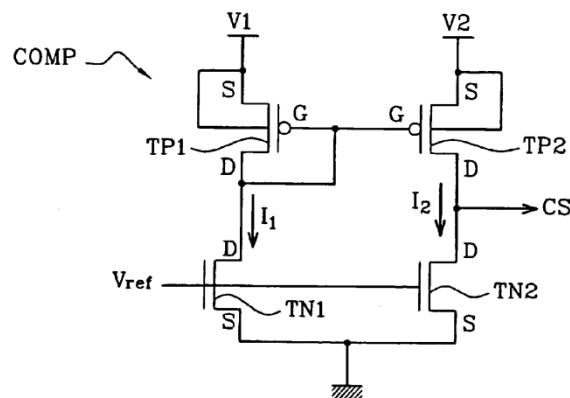


Fig 3.4 Voltage compare circuit

(Reference: [http://baec.tripod.com/projects/maplin\\_book1\\_1983\\_logic\\_probe.htm](http://baec.tripod.com/projects/maplin_book1_1983_logic_probe.htm))

Figure 3.4 provided another example to implement the amplitude comparison [5]. The circuit has two input voltage, V1 and V2 associated with the diagram. The first PMOS transistor, on the top left of the circuit, connected source the first input voltage. Meanwhile, the second PMOS transistor on the top right of the circuit received second voltage V2. Here, the comparator included first and second PMOS transistors arranged as current mirrors. On the other hand, the output of the comparator was connected to the drain of one of the transistors, named CS on the circuit. It propagates an output signal had a first value when the second voltage was higher than the first voltage, or having a second value when the second voltage was lower than the first voltage. The advantage of this design was the comparator allowing two voltages to be compared without requiring a third voltage distinct from the two voltages to be compared.

### 3.1.1.1.3 High gain amplifier

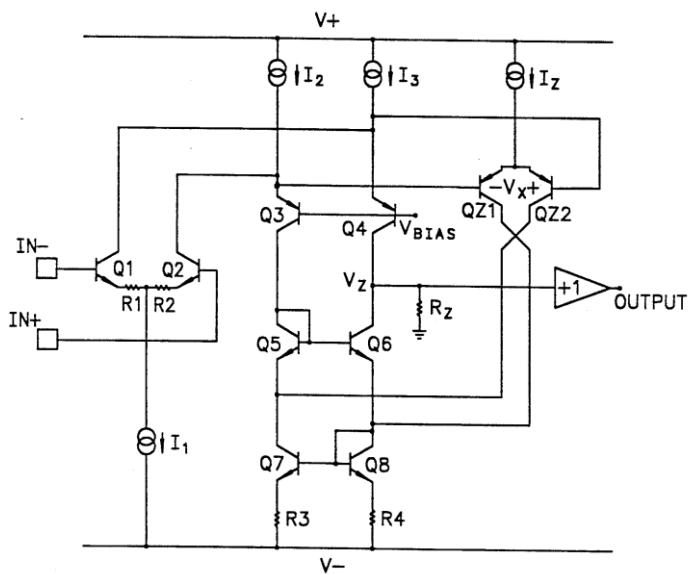


Fig 3.5 Amplifier circuit  
*(reference: <http://www.freepatentsonline.com/5168243.pdf>)*

Amplifier proportionally increasing the input signal in terms of achieving high gain and stability. Figure 3.5 provided a high gain design of a integrated amplifier, which can be used to amplify the difference signal associate the with block diagram showed in figure 3.1. Referring to the 3.5, a high gain amplifier circuit [6] was illustrated. It had a high impedance node as collector of transistor coupled. Also, a sense circuit, which sensing the emitter base voltage, generated a correction current that coupled to boost the gain of the amplifier. This circuit can be used after the comparison for both amplitude and phase in terms of extend the range for small offsets.

### 3.1.1.2 Amplitude comparator with hybrid circuit

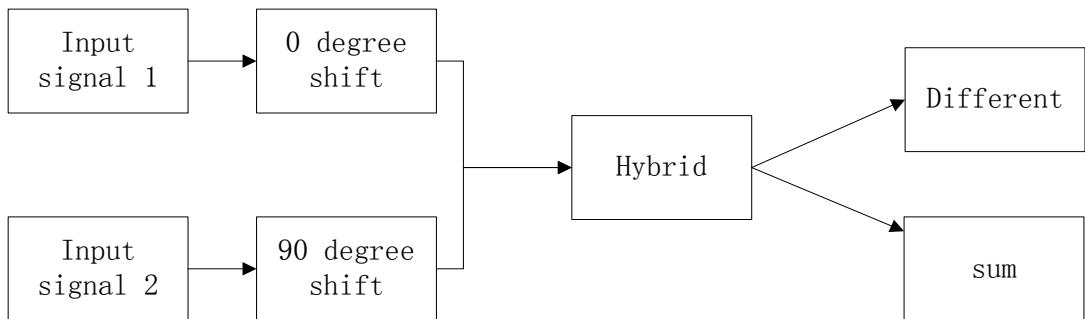


Fig 3.6 Amplitude comparator with hybrid circuit

As the diagram showed above, the amplitude comparator was made of two types of hybrid circuits [4]. The first type is phase shift hybrid that able to shift the input signal by about 90 degree. Refer the block diagram, the input signal 2 is shifted 90 degrees, while the input signal shifts 0 degrees in terms of balance the delay for two signal. Another type of hybrid circuit was able to produce the difference and sum of the two inputs signal.

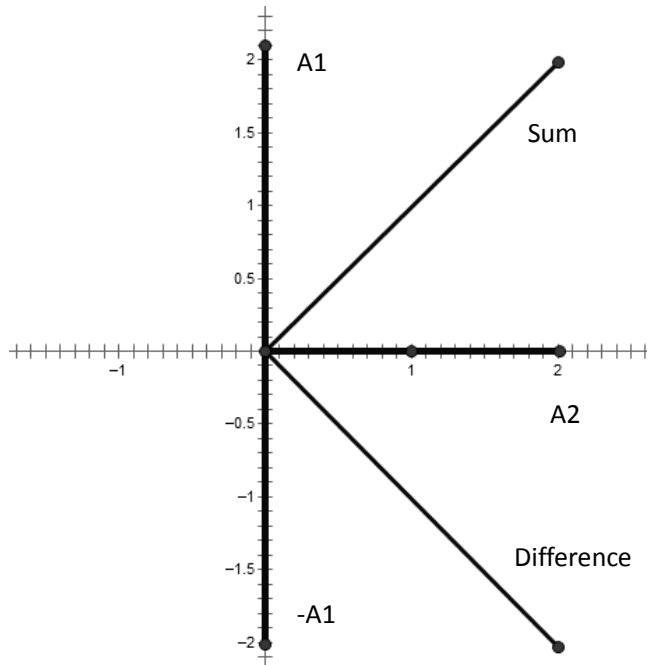


Fig 3.7 Example of hybrid circuit

The figure 3.7 illustrates an example of the hybrid circuit, where  $A_1$  and  $A_2$  is the amplitude of two input signal respectively. The sum and difference can be represented in the phase form. Therefore, associate with the diagram, only when the input signals have the same amplitude, the phase between sum and difference become 90 degrees.

### 3.1.1.2.1 Phase Hybrid circuit

Associate with the block diagram in figure 3.6, the first stage hybrid circuit shifts the phase for input signal 2 by 90 degree. Meanwhile, input signal 1 needs shifted 0 degrees to obtain the same delay through the phase hybrid circuits.

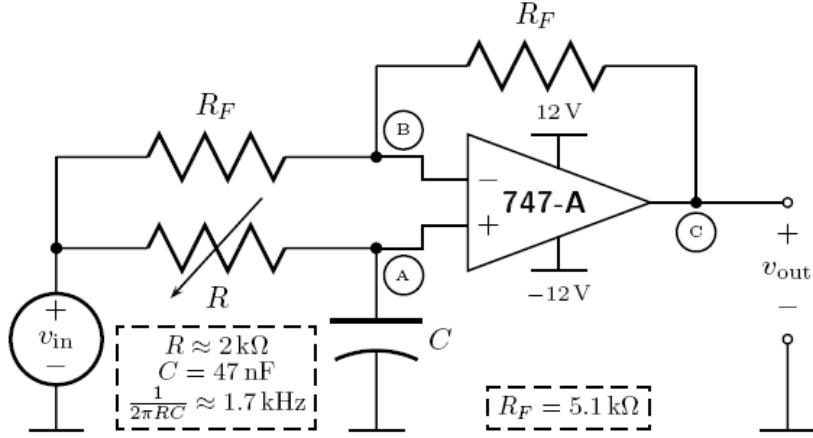


Fig 3.8 Basic circuit for phase shifter

(Reference:

[http://www2.ece.ohio-state.edu/~pavlict/ece209/lab1\\_intro/lab1\\_intro\\_phase\\_shifter.pdf](http://www2.ece.ohio-state.edu/~pavlict/ece209/lab1_intro/lab1_intro_phase_shifter.pdf)

Figure 3.8 illustrate a basic phase shifter circuit made of operational amplifier (OP\_AMP) [8]. Overall, the phase shifter circuit uses a first-order low-pass filter to create a phase shift and negative feedback to compensate for non-unity gain.

Refer to the circuit, at node A, it implements a low-pass filter, assume the transfer function is,

$$H_{LPF} = \frac{1}{sRC + 1}$$

Hence, the voltage at node A is

$$V_A(s) = V_{in}(s)H_{LPF}(s)$$

At node B, it is the input of the OP\_AMP, and the current can be represented as,

$$\frac{V_{in}(s) - V_A(s)}{R_F} = \frac{V_{in}(s) - V_{in}(s) \cdot H_{LPF}(s)}{R_F}$$

The current in the feedback loop can be found by applying the a virtual ground,

$$\begin{aligned} V_{out} &= V_B(s) - I_B(s)R_F = V_{in}(s) \cdot H_{LPF}(s) - \frac{V_{in}(s) - V_{in}(s) \cdot H_{LPF}(s)}{R_F} \cdot R_F \\ &= V_{in}(s)[2H_{LPF}(s) - 1] = V_{in}(s)\left[2 \times \frac{1}{sRC + 1} - 1\right] = V_{in}(s) \cdot \frac{1 - sRC}{sRC + 1} \end{aligned}$$

Therefore, the transfer function for the system is,

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{V_{in}(s) \cdot \frac{1 - sRC}{sRC + 1}}{V_{in}(s)} = \frac{1 - sRC}{1 + sRC}$$

Hence, the phase shift of the system can be written as,

$$\angle H(j\omega) = \arctan(-\omega RC) - \arctan(\omega RC) = -2 \cdot \arctan(\omega RC)$$

Hence,

$$\angle H(j\omega) = \begin{cases} 0 & (\omega = 0) \\ -\frac{\pi}{2} & (\omega = \frac{1}{RC}) \\ -\pi & (\omega \rightarrow +\infty) \end{cases}$$

The design provides a method for implementing a phase shifter by set justify the resistance and capacitance to obtain difference phase shifting based on the equation highlight in the rectangular.

### 3.1.1.2.2 Sum and difference hybrid circuit

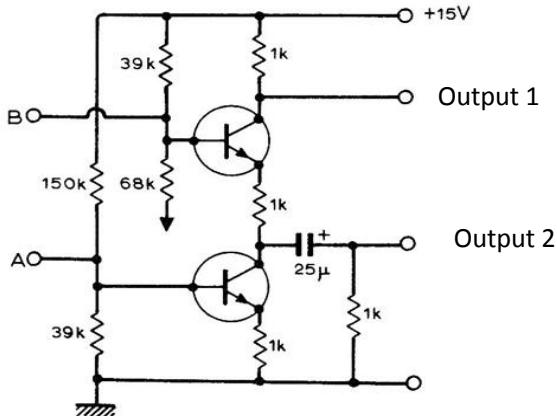


Fig 3.9 Sum and difference hybrid circuit

(Reference: [http://www.seekic.com/forum/22\\_circuit\\_diagram/21320\\_SUM\\_AND\\_DIFFERENCE](http://www.seekic.com/forum/22_circuit_diagram/21320_SUM_AND_DIFFERENCE))

Figure 3.9 shows a example structure of a hybrid circuit [9] in order to output sum and difference signal depended on the input signal A and B. In this design two transistor BC109 [10] are used. Here, the output can be written as,

$$V_{o1} = \frac{-1}{2(V_A + V_B)}$$

And,

$$V_{o2} = \frac{-1}{2(V_A - V_B)}$$

### 3.1.2 Phase difference circuit

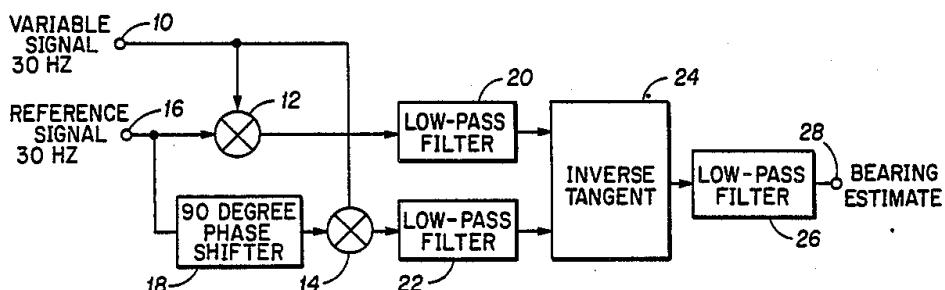


Fig 3.10 Phase comparator circuit

(Reference: <http://www.freepatentsonline.com/4675614.html>)

Figure 3.10 illustrates a circuit for phase difference measurement [11], it provide the phase measurement for in-phase and quadrature phase signals. The system compared two inputs signal, included variable and reference signal, where the reference signal was driven to have 90-degree phase shift. Assume, the variable signal was,

$$V(t) = \sin(\omega t + \varphi)$$

And the reference signal was,

$$R(t) = \sin(\omega t)$$

After the phase shifting,

$$R'(t) = \cos(\omega t)$$

Refer to the circuit, the input signals will send to the multipliers,

$$f(t) = V(t) \cdot R(t) = \sin(\omega t + \varphi) \cdot \sin(\omega t) = 0.5 \times [\cos(\varphi) - \cos(2\omega t + \varphi)]$$

And,

$$g(t) = V(t) \cdot R'(t) = \sin(\omega t + \varphi) \cdot \cos(\omega t) = 0.5 \times [\sin(\varphi) - \sin(2\omega t + \varphi)]$$

Through the low-pass filter, only the low frequency parts are remained. Hence,

$$f(t) = \cos(\varphi)$$

And,

$$g(t) = \sin(\varphi)$$

Then, input signals send to a phase locked loop to lock onto the input signal and uses the output of a voltage controlled oscillator located in the loop to derive the sine and cosine of the input signal, so that to address a sine/cosine look-up table. This progress provides two sine wave output signals, in-phase and quadrature phase, with equal amplitude and phase shifted by 90°. After the signals through a low-pass filter, an inverse tangent will produce the signal output for the system, which representing a detected phase difference.

### 3.1.2.1 Low-pass filter

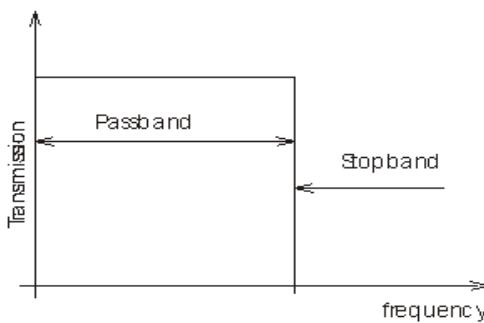


Fig 3.11 Ideal low pass filter in frequency domain

(Reference: lecture notes of electronics 3)

Low-pass filter has attenuation of frequencies above their cut-off points as the diagram showed above.

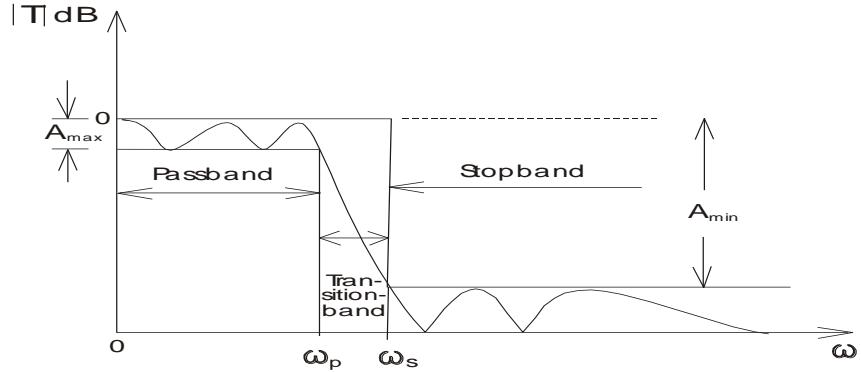


Fig 3.12 Real low-pass filter

(Reference: lecture notes of electronics 3)

Compare to the ideal filter, the real design will have ripple in both passband and stopband. Also, the real one has the transition band between pass the stop band, rather than cutoff the frequency straightly.

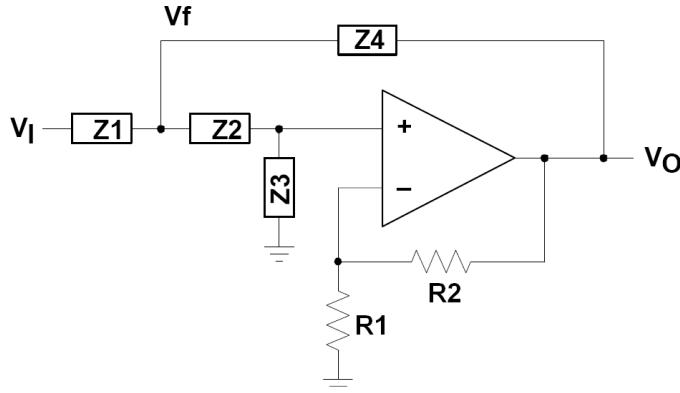


Fig 3.13 Generalized structure of salien-key filter

(Reference: [http://www.stefanv.com/calculators/hp67\\_sallen\\_key.html](http://www.stefanv.com/calculators/hp67_sallen_key.html))

An example design is sketched in figure 3.13, assume the OP\_AMP is virtual short,

$$V_+ = V_-$$

The voltage can be represented as,

$$\begin{aligned} \left( \frac{R1}{R1 + R2} \right) \times V_o &= V_i \times \left( \frac{Z2Z3Z4}{Z2Z3Z4 + Z1Z2Z4 + Z1Z2Z3 + Z2Z2Z4 + Z2Z2Z1} \right) \\ &\quad + V_o \times \left( \frac{Z1Z2Z3}{Z2Z3Z4 + Z1Z2Z4 + Z1Z2Z3 + Z2Z2Z4 + Z2Z2Z1} \right) \end{aligned}$$

Hence, the transfer function is,

$$T = \frac{V_o}{V_i} = \frac{\frac{Z2Z3Z4}{R1}}{\frac{Z2Z3Z4 + Z1Z2Z4 + Z1Z2Z3 + Z2Z2Z4 + Z2Z2Z1}{R1 + R2} - \frac{Z1Z2Z3}{R1 + R2}}$$

Here, letting

$$\frac{R1}{R1 + R2} = \frac{1}{Avo}$$

The transfer function become,

$$\begin{aligned}
T &= \frac{\frac{Z2Z3Z4}{Z2Z3Z4 + Z1Z2Z4 + Z1Z2Z3 + Z2Z2Z4 + Z2Z2Z1}}{\frac{1}{Avo} - \frac{Z1Z2Z3}{Z2Z3Z4 + Z1Z2Z4 + Z1Z2Z3 + Z2Z2Z4 + Z2Z2Z1}} \\
&= \frac{\frac{Z2Z3Z4}{Z2Z3Z4 + Z1Z2Z4 + Z1Z2Z3 + Z2Z2Z4 + Z2Z2Z1}}{\frac{1}{Avo} - \frac{Z1Z2Z3}{Z2Z3Z4 + Z1Z2Z4 + Z1Z2Z3 + Z2Z2Z4 + Z2Z2Z1}} \\
&= \frac{\frac{Z2Z3Z4}{Z2Z3Z4 + Z1Z2Z4 + Z1Z2Z3 + Z2Z2Z4 + Z2Z2Z1}}{\frac{(Z2Z3Z4 + Z1Z2Z4 + Z1Z2Z3 + Z2Z2Z4 + Z2Z2Z1) - Avo \cdot Z1Z2Z3}{(Z2Z3Z4 + Z1Z2Z4 + Z1Z2Z3 + Z2Z2Z4 + Z2Z2Z1) \cdot Avo}}
\end{aligned}$$

Because of the design showed in figure 3.10 required a low-pass filter, the impedance can be written as,

$$Z1 = Z2 = R \text{ and } Z3 = Z4 = \frac{1}{j\omega c}$$

In this term, the transfer function can be specified as,

$$\begin{aligned}
T = \frac{V_o}{V_i} &= \frac{\frac{Avo \cdot \frac{R}{j\omega c}}{\frac{R}{(j\omega c)^2} + \frac{3 \cdot R^2}{j\omega c} + R^3 - Avo \cdot \frac{R^2}{j\omega c}}}{\frac{Avo \cdot \frac{R}{j\omega c}}{\frac{R}{(j\omega c)^2} + \frac{R^2}{j\omega c} \cdot (3 - Avo) + R^3}} \\
&= \frac{\frac{Avo}{(j\omega c \cdot R)^2}}{\frac{1}{(j\omega c \cdot R)^2} + \frac{1}{j\omega c \cdot R} \cdot (3 - Avo) + 1} \\
&= \frac{\frac{Avo}{(c \cdot R)^2}}{\frac{1}{(c \cdot R)^2} + \frac{j\omega}{c \cdot R} \cdot (3 - Avo) + (j\omega)^2}
\end{aligned}$$

Letting  $\omega_0 = \frac{1}{c \cdot R}$ , eventually, the transfer function is,

$$T = \frac{V_o}{V_i} = \frac{Avo \cdot \omega_0}{\omega_0^2 + j\omega(3 - Avo)\omega_0 + (j\omega)^2}$$

Any complex low-pass filter can be made of first order and second order filters. Furthermore, the resistance and capacitance is depended on the requirement, the ripple, passband frequency and stopband frequency. For a given specification, the order of the filter can be calculated from,

$$A(\omega_s) = 10 \cdot \log_{10} \{ 1 + \varepsilon^2 \cdot \cosh^2 [N \cosh^{-1} (\omega_s / \omega_p)] \}$$

Where the parameter  $\varepsilon$  is given by,

$$\varepsilon = \sqrt{10^{\frac{A_{\max}}{10}} - 1}$$

There are many types of filter, taking the Chebyshev filter [13], the pole of the filter can be represented as,

$$\begin{aligned} \mathbf{p}_k &= -\omega_p \cdot \sin\left(\frac{2k-1}{N} \cdot \frac{\pi}{2}\right) \cdot \sinh\left(\frac{1}{N} \sinh^{-1} \frac{1}{\epsilon}\right) + \\ &+ j \omega_p \cdot \cos\left(\frac{2k-1}{N} \cdot \frac{\pi}{2}\right) \cdot \cosh\left(\frac{1}{N} \sinh^{-1} \frac{1}{\epsilon}\right) \quad \text{for } k = 1, 2, 3, \dots, N. \end{aligned}$$

Finally, the transfer function of the filter can be found,

$$T(s) = \frac{K \omega_p^N}{\epsilon 2^{N-1} (s - p_1)(s - p_2) \dots (s - p_N)}$$

Associate with the transfer function the second order or first order element, the resistance and capacitance of can be determined.

### 3.1.2.2 Phase locked loop (PLL)

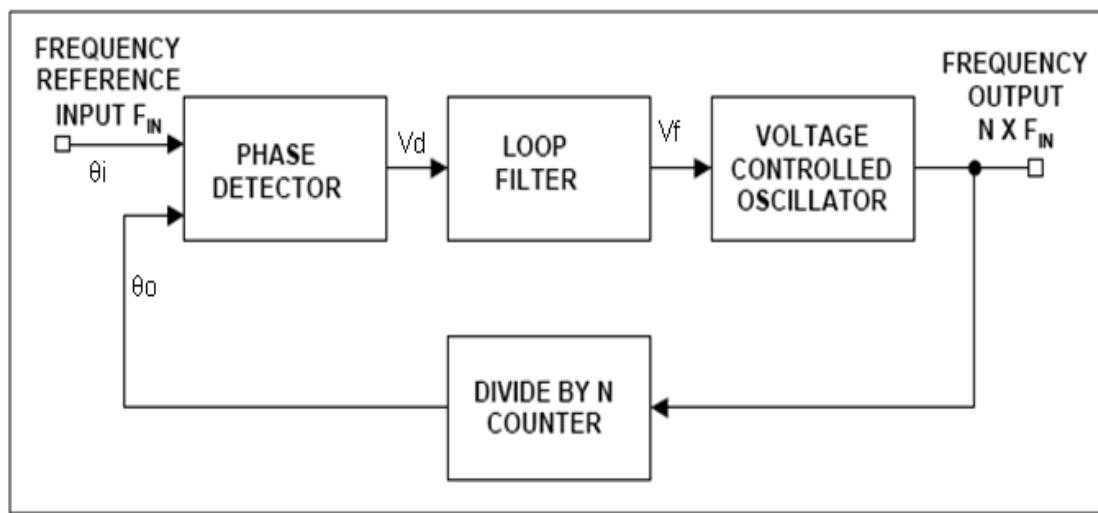


Fig 3.14 Basic structure of PLL  
*(Reference: <http://www.irational.org/sic/radio/tech.html>)*

Generally, as the diagram showed above, PLL has three basic elements, include a phase detector, a variable electronic oscillator, and a feedback path (which often includes a frequency divider). Phase detector (PD) compares phase of input signals, and generates a periodic output for the different phase.

$$V_d = K_d(\theta_i - \theta_o)$$

Where, the  $K_d$  was the phase-detector gain factor. The output signal from PD was applied to the loop filter which determined the dynamic characteristics of the PLL. The filtered signal can be written as  $V_f$ , and it would send to voltage controlled oscillator (VCO),

$$V_f = F(s) \cdot V_d(s)$$

Where,  $F(s)$  was the transfer function of the filter

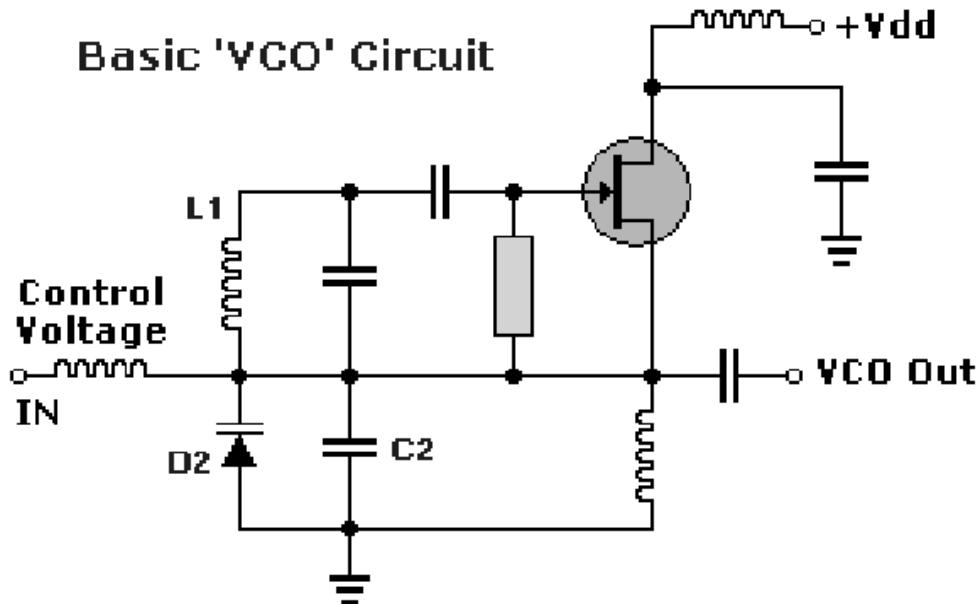


Fig 3.15 Basic VCO circuit

(Reference: <http://www.porlidias.gr/Papers/PLL.pdf>)

The figure 3.15 showed above is a basic circuit of VCO. Oscillations occur at the resonant frequency, which is typically changed or tuned by varying the resonator capacitance. VCOs are oscillators whose resonant tank circuit can be tuned via a control voltage that is applied across a varactor in the tank circuit. Frequency of oscillation was determined by L1, C2, and D2. When reverse bias, the diode acted as a capacitor and its depletion zone became the dielectric properties. Changing the amount of reverse bias within the diode's breakdown limits occur the changing of depletion zone width. Therefore, the diode determined the effective capacitance which corresponding the frequency oscillation of circuit. The output for VCO can be written as,

$$\theta_o(s) = \frac{k_o \cdot V_f}{s}$$

Where  $k_o$  was the VCO gain factor. Hence, the close loop transfer function was,

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{k_o \cdot k_d \cdot F(s)}{s + k_o \cdot k_d \cdot F(s)}$$

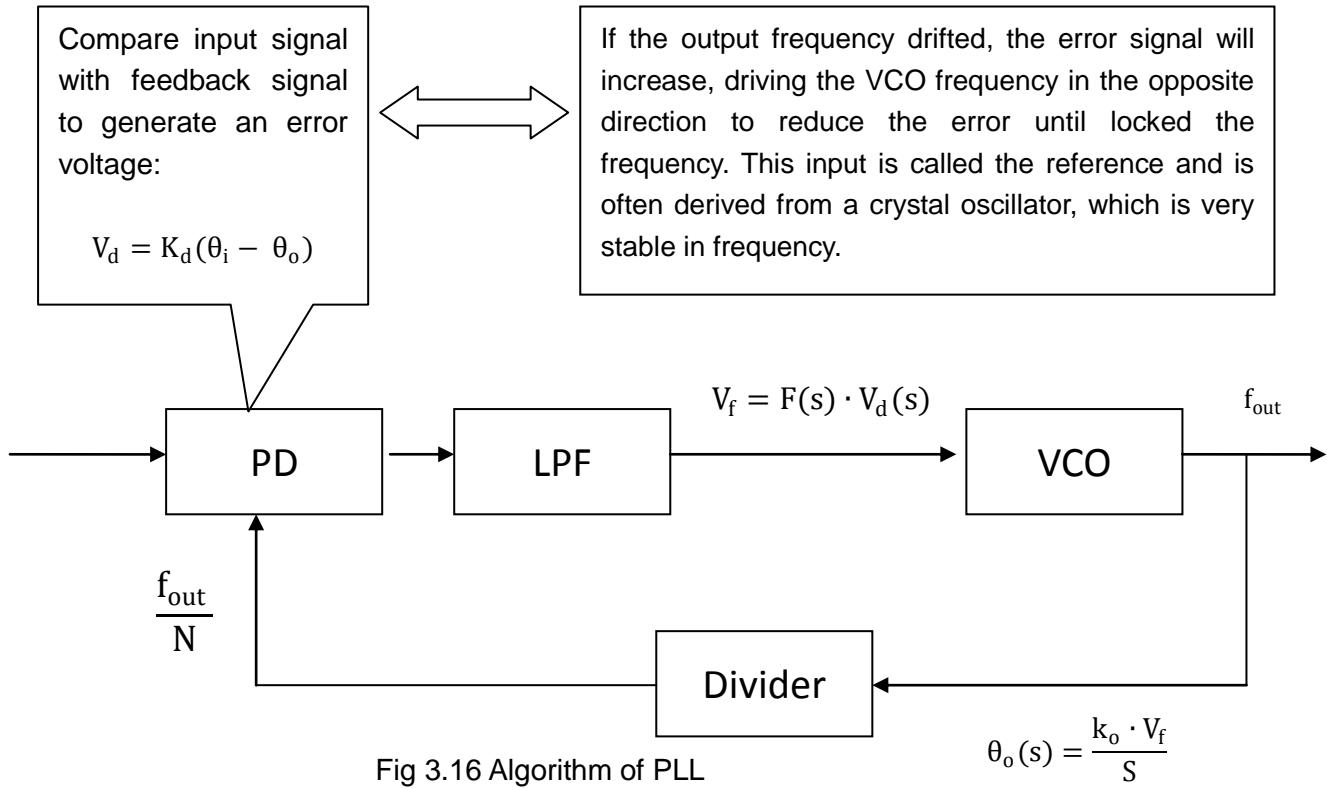
For the phase error,

$$H_e(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{\theta_o(s) - \theta_i(s)}{\theta_i(s)} = \frac{s}{s + k_o \cdot k_d \cdot F(s)} = 1 - H(s)$$

Also, the filtered signal or the control voltage can be written as,

$$V_c(s) = V_f(s) = \frac{s \cdot k_d \cdot F(s) \cdot \theta_i(s)}{s + k_o \cdot k_d \cdot F(s)} = \frac{s \cdot \theta_i(s)}{k_o} \cdot H(s)$$

In all, the algorithm of PLL can be summarized as,



### 3.2 Amplitude and phase control

In 1988, Dixon published a paper to provide a method to use indirect current control a unity power factor sinusoidal Current. The circuit was implemented based on Fourier Series of sinusoidal PWM (Pulse-width modulation).

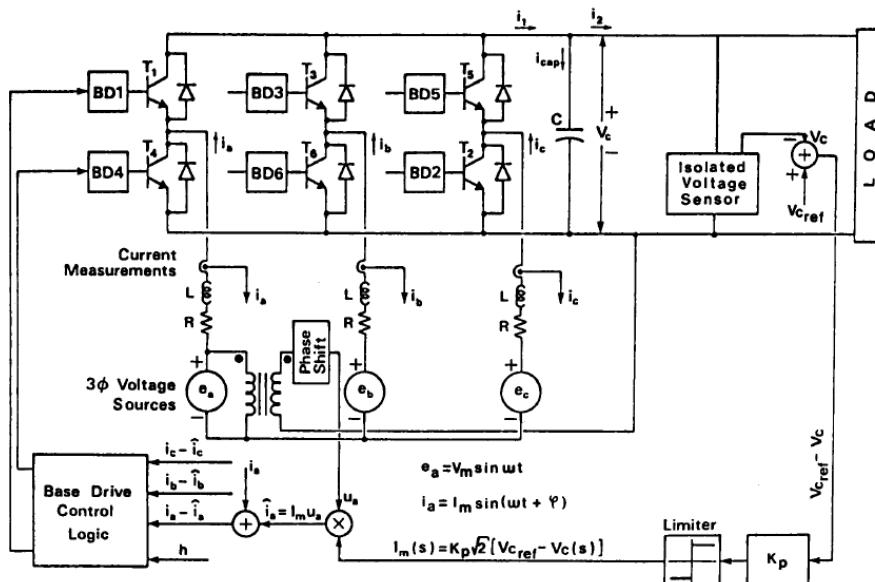


Fig 3.17 Schematic diagram of hysteresis current controlled rectifier  
(Reference: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9172>)

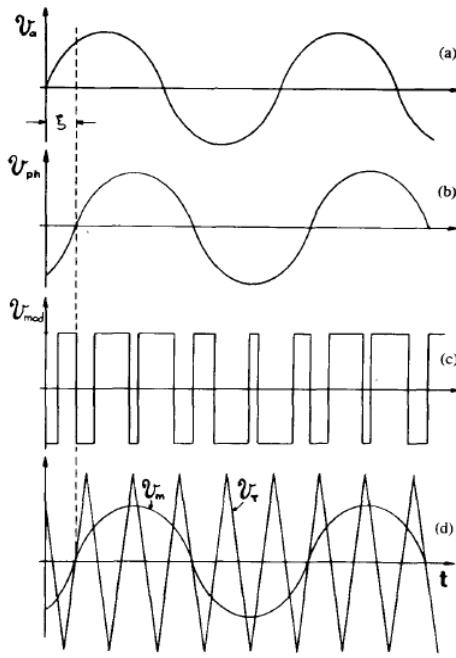


Fig 3.18 Sinusoidal PWM Control

(Reference: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9172>)

Figure 3.18 illustrated the control mechanism between sine wave and PWM. On the diagram, the waves of figure (a) and (b) can be represented as,

$$V_a(t) = \sqrt{2}V \sin(\omega t)$$

And,

$$V_{pha}(t) = \sqrt{2}V_{ph} [\sin(\omega t) \cos(\varphi) - \cos(\omega t) \sin(\varphi)]$$

In the expression showed above,  $V_{pha}(t)$  is the fundamental component of the voltage at the rectifier terminals, the rectifier being under sinusoidal PWM control. Associated with figure (c), if one of the input imagines capacitor to have a centre-tap, the output waveform of the voltage between the A-phase rectifier terminal and the centre-tap consists of the square wave. Hence, this method provided modulating waveform switches from  $+0.5 V_c$  to  $-0.5V_c$ , and the switching pattern yielded as fundamental component the waveform of  $V_{pha}(t)$ .

Meanwhile, figure (d) presented the switching pattern generated in the conventional sinusoidal PWM strategy. The switching instants are based on the intersections of the triangular waveform  $V_t$  and the modulating sinusoidal waveform  $V_m(t)$ .  $V_m(t)$  was the Fourier Series of the output voltage waveform, can be written as,

$$V_m(t) = \sqrt{2}V_m [\sin(\omega t) \cos(\varphi) - \cos(\omega t) \sin(\varphi)]$$

And, the output voltage is,

$$V_{mod}(t) = \frac{\sqrt{2}}{2} \frac{V_m}{V_{t_{peak}}} V_c [\sin(\omega t) \cos(\varphi) - \cos(\omega t) \sin(\varphi)] + \text{Bessel function harmonic terms}$$

Therefore, when,

$$V_m < V_{t_{peak}}$$

While increasing the carrier frequency, the fundamental component for the output voltage was able to dominate over the harmonic terms, and consequently the harmonic distortion in the current can become negligible.

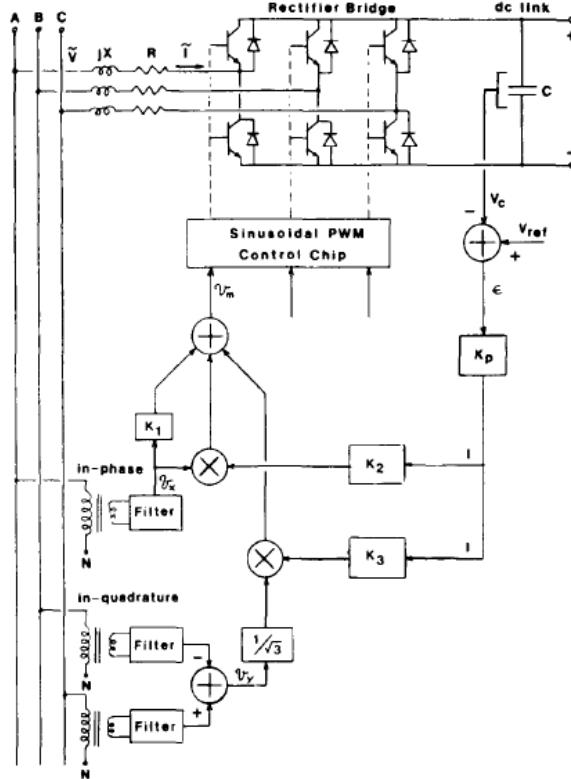


Fig 3.19 Block diagram implementing indirect current control.

(Reference: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9172>)

Figure 3.19 showed the circuit for using current control the sinusoid wave. On the diagram, the input signal  $I$  was electronically multiplied to the in-phase and the in-quadrature, so that the parameters  $k$  can be used as the coefficient for the output voltage, as

$$V_{\text{mod}}(t) = \frac{\sqrt{2}}{2} \frac{V_m}{V_{t_{\text{peak}}}} V_c ([k_1 + k_2 I] \sin(\omega t) - k_3 \cos(\omega t)] + \text{Bessel function harmonic terms}$$

Assumed that all time harmonic terms are negligible, the control current can be written as

$$i_a = \sqrt{2} I \sin(\omega t) + A e^{-t/T}$$

Where,  $A$  was the constant of the integration and  $T=L/R$ .

### 3.2.1 Stability

The signal control system would drive the detected offset (both amplitude and phase) feedback to the input signal in terms of tracing the reference signal. Therefore, the stability of feedback loop can be found from bode plot. For industry design, the phase margin should above  $75^\circ$  (minimum  $60^\circ$ ).

Associate with the flowing sketch, the difference between the value of  $|A\beta|$  at  $\omega_{180}$  and unity, called the gain margin [12], usually expressed in decibels. The gain margin represents the amount by which the loop gain can be increased while stability is maintained.

On the other hand, the difference between the phase angle at this frequency and  $180^\circ$  is termed the phase margin. If at the frequency of unity loop-gain margin, the phase lag is in excess of  $180^\circ$ , the amplifier will be unstable.

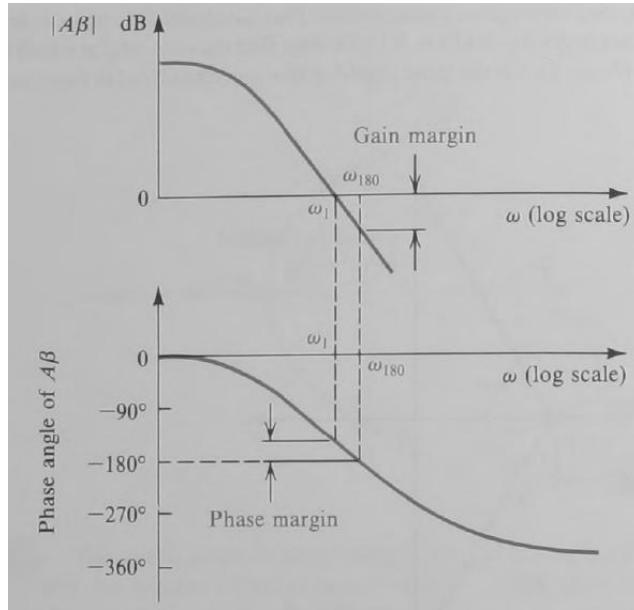


Fig 3.20 Bode plot

(Reference: *Microelectronics Circuits, 5th Edition, page 846*)

### 3.3 Relevant work

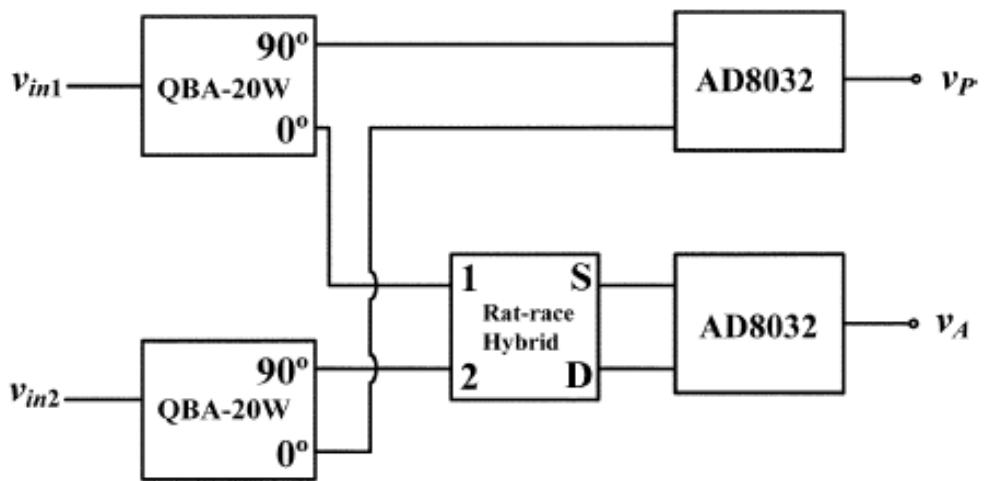


Fig 3.21 Implementation for signal amplitude and phase control system

(Reference: Paul A. Warr, Nirmal Bissonauth, 'Amplitude offset estimation by phase comparison in suppression loops', *IEEE Transactions on Microwave Theory and Techniques*)

Refer [7] and the mathematic consequence in section 4.2, the algorithm of using phase comparison to implement the control system was designed as figure 3.20 showed, where, QBA-20W was a 90 degree phase hybrids and AD8032 was dual voltage feedback amplifiers. These devices are existing on the market for the high speed performance applications. For this project, in order to design the signal control system as an integrated chip, there elements should be re-designed in transistor level schematic. For instance, the amplifier can be design based on the discussion in section 3.1.1.1.3 and the phase shifter hybrid circuit can be implemented based on section 3.1.1.2.1 by optimise the parameters of the circuits. Meanwhile, the sum and difference hybrid circuit is discussed in section 3.1.1.2.2. Therefore, the signal amplitude and phase control system project is start with design the basic element circuits based on the information provided in the previous sections.

## 4 WORK CARRIED OUT

### 4.1 Comparison of different technology

In section 3.1, the discussion listed different technology for amplitude and phase comparison. For the signal amplitude, there are two options, either using a non-linear pair (section 3.1.1.1) or using the hybrid circuit (section 3.1.1.2).

The advantage of non-linear pair implementation was it could accurately detect the peak amplitude of two signals. However, the result was switching between two inputs to indicate which one had larger amplitude. The main drawback of this method is that if there were a phase error, the sinusoid wave would not reach the peak value at same time, even if the amplitude was correct.

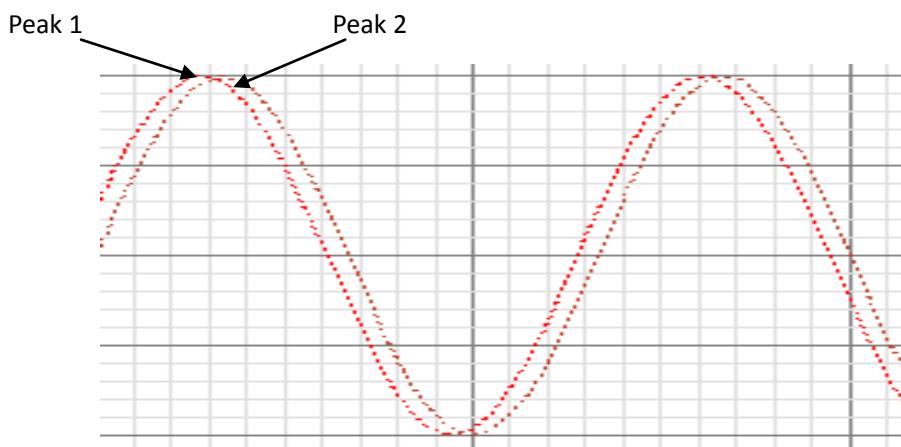


Fig 4.1 Example of sinusoid wave with phase difference

Associated with the diagram shown above, two inputs had the same amplitude with small phase differences. The output of the peak value detector (shown in figure 3.3) would keep switching as the maximum values were not produced at same time. The solution of this problem was to implement a phase locker loop. An advantage for PLL was the divider extended the range of the frequency. This combination of using PLL

and amplitude comparator required working in sequence. In other words, the input signal should firstly lock the phase to the reference signal before measuring the amplitude. Any change of the input caused the sequence to repeat, and it took a long time for amplitude and phase error estimation by implementing the combination. Another technique, discussed in section 3.1.1, was to use a hybrid circuit to generate the sum and difference signal for reference and target inputs. Compared to the combination above, this method was able to estimate the error of amplitude and phase simultaneously. Also, it used the same methodology, phase comparison in suppression loops, so that fewer components were required, which can be considered a cost-saving method. Based on a mathematical format (discussed later), the amplitude or phase error can be detected independently and simultaneously. Therefore, compared to the combination mentioned previously, the hybrid circuit was able to detect the amplitude and phase error immediately during any change of the input.

Furthermore, based on the results of [3] and [7], both of the methods achieved high accuracy, especially [7]; it presents 3% accuracy with the frequency range at 1600 to 2000 MHz. Considering the complexity of the design, the hybrid circuit method estimated the amplitude offset into a phase comparison loop. It can be used in both amplitude and phase comparison parts. Section 3.1.2 also presented a general technology for phase comparison, and an innovation in that design is to use phase shifter circuits to extend the comparison range. Associated with section 3.1.2.1, the phase shifter circuit is able to shift the reference signal without changing its amplitude. However, the hybrid method was chosen to implement the signal amplitude and phase control system to reduce the components.

## 4.2 Signal amplitude and phase offset detection

In this section, the structure of control system will be decided based on the discussion in section 2, 3 and 4. The hybrid method will be implemented for both amplitude and phase comparator.

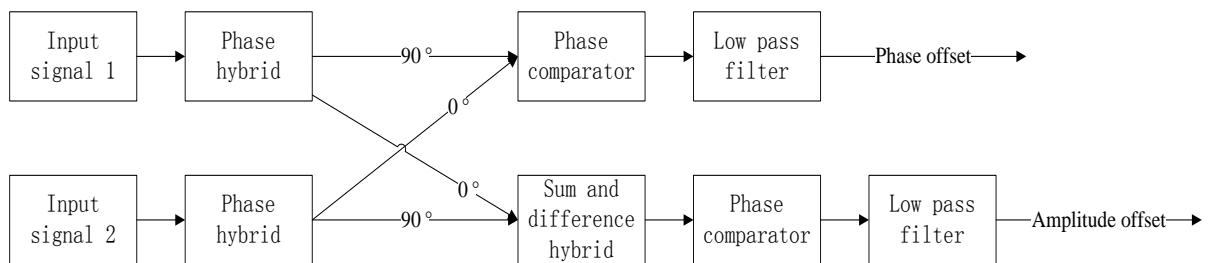


Fig 4.2 Block diagram of signal amplitude and phase control system  
In reference to the block diagram, there are two input signals:

$$V_{in1} = A \cos(\omega t)$$

$$V_{in2} = -k \cdot A \cos(\omega t + \varphi)$$

Where  $A$  is the original amplitude, with  $k$  representing the scaling factor of the antiphase. Meanwhile,  $\varphi$  is the phase error between two inputs.

### 4.2.1 Amplitude comparison

Associated with the block diagram of the system, the second input is driven to the phase hybrid circuit to obtain 90-degree phase shifting,

$$V_{\text{in } 2-\text{shift}} = -k \cdot A \cos\left(\omega t + \varphi - \frac{\pi}{2}\right) = -k \cdot A \sin(\omega t + \varphi)$$

The signal will then send to the sum and difference hybrid,

$$\begin{aligned} V_{\text{sum}} &= V_{\text{in } 1} + V_{\text{in } 2-\text{shift}} = A \cos(\omega t) - k \cdot A \sin(\omega t + \varphi) \\ &= A \cos(\omega t) - kA[\sin(\omega t) \cos(\varphi) + \cos(\omega t) \sin(\varphi)] \\ &= [A - k \sin(\varphi)] \cos(\omega t) - kA \cos(\varphi) \sin(\omega t) \end{aligned}$$

For the difference,

$$\begin{aligned} V_{\text{difference}} &= V_{\text{in } 1} - V_{\text{in } 2-\text{shift}} = A \cos(\omega t) + k \cdot A \sin(\omega t + \varphi) \\ &= A \cos(\omega t) + kA[\sin(\omega t) \cos(\varphi) + \cos(\omega t) \sin(\varphi)] \\ &= [A + k \sin(\varphi)] \cos(\omega t) + kA \cos(\varphi) \sin(\omega t) \end{aligned}$$

The phase relationship between  $V_{\text{sum}}$  and  $V_{\text{difference}}$  is shown below to be a function of the amplitude ratio  $k$  between the input signals. The phase form of sum and difference signal is,

$$\overline{V_{\text{sum}}} = \begin{pmatrix} A - k \sin(\varphi) \\ -kA \cos(\varphi) \end{pmatrix}$$

And,

$$\overline{V_{\text{difference}}} = \begin{pmatrix} A + k \sin(\varphi) \\ kA \cos(\varphi) \end{pmatrix}$$

The phase angle can be obtain based on the dot product,

$$\cos\theta = \frac{\mathbf{a} \cdot \mathbf{b}}{|\mathbf{a}| \cdot |\mathbf{b}|}$$

The dot product of vectors expressed in an orthonormal basis is related to their length and angle, as depicted in the following sketch.

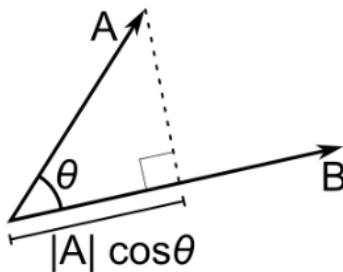


Fig 4.3 Sketch of the dot product

Hence,

$$\begin{aligned} \overline{V_{\text{sum}}} \cdot \overline{V_{\text{difference}}} &= [A - k \sin(\varphi)] \cdot [A + k \sin(\varphi)] + [-kA \cos(\varphi)] \cdot [kA \cos(\varphi)] \\ &= A^2 - k^2 A^2 \sin^2(\varphi) - k^2 A^2 \cos^2(\varphi) = A^2 - k^2 A^2 \end{aligned}$$

$$\begin{aligned} |\overline{V_{\text{sum}}}| &= \sqrt{[A - k \sin(\varphi)]^2 + [-kA \cos(\varphi)]^2} \\ &= \sqrt{A^2 - 2kA^2 \sin^2(\varphi) + k^2 A^2 \sin^2(\varphi) + k^2 A^2 \cos^2(\varphi)} \\ &= \sqrt{A^2 - 2kA^2 \sin^2(\varphi) + k^2 A^2} \end{aligned}$$

$$\begin{aligned}
|\overline{V_{\text{difference}}}| &= \sqrt{[A + kA\sin(\varphi)]^2 + [kA\cos(\varphi)]^2} \\
&= \sqrt{A^2 + 2kA^2\sin^2(\varphi) + k^2A^2\sin^2(\varphi) + k^2A^2\cos^2(\varphi)} \\
&= \sqrt{A^2 + 2kA^2\sin^2(\varphi) + k^2A^2}
\end{aligned}$$

Therefore, the angle between sum and difference is,

$$\begin{aligned}
\cos\theta &= \frac{\overline{V_{\text{sum}}} \cdot \overline{V_{\text{difference}}}}{|\overline{V_{\text{sum}}}| \cdot |\overline{V_{\text{difference}}}|} = \frac{A^2 - k^2A^2}{\sqrt{A^2 - 2kA^2\sin^2(\varphi) + k^2A^2} \cdot \sqrt{A^2 + 2kA^2\sin^2(\varphi) + k^2A^2}} \\
&= \frac{1 - k^2}{\sqrt{1 - 2k\sin^2(\varphi) + k^2} \cdot \sqrt{1 + 2k\sin^2(\varphi) + k^2}} \\
&= \frac{1 - k^2}{\sqrt{1 - 2k^2[1 - 2\sin^2(\varphi)] + k^4}} = \frac{1 - k^2}{\sqrt{1 + 2k^2\cos^2(2\varphi) + k^4}}
\end{aligned}$$

The equation indicated the relation between the phase difference, amplitude ratio  $k$ , and phase error. A surface plot  $\theta$  against  $k$  and  $\varphi$  is shown in following diagram.

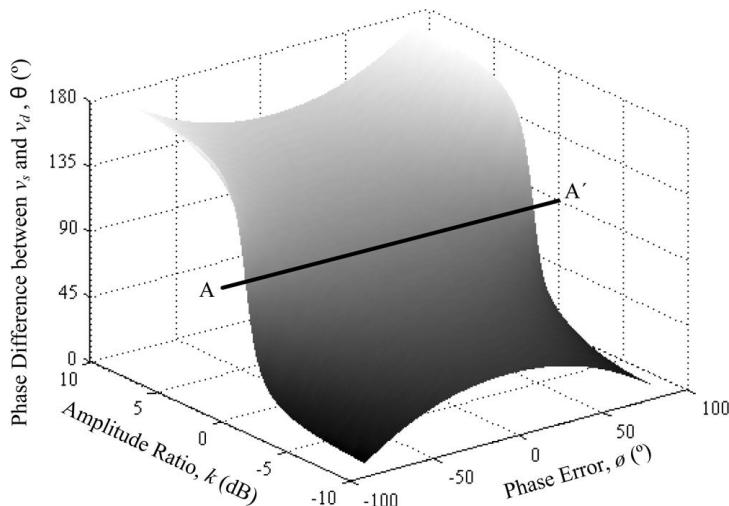


Fig 4.4 Phase difference between  $v_s$  and  $v_d$ ,  $\theta$  ( $^\circ$ )

(Reference: Paul A. Warr, Nirmal Bissonauth, 'Amplitude offset estimation by phase comparison in suppression loops', IEEE Transactions on Microwave Theory and Techniques)

As figure 4.4 shows that  $k \rightarrow 1$  as (0 dB), the dependency of  $\theta$  on  $\varphi$  reaches a minimum, as the cross line shows in the diagram. Also, where  $\theta \rightarrow 90^\circ$ , the error in the measurement of 'k' reduces to zero regardless of the phase error. Therefore,  $\varphi$  may be assumed to be zero for the amplitude measurement,

$$\theta = \cos^{-1}\left(\frac{1 - k^2}{1 + k^2}\right)$$

By the application of the chain and quotient rules for differentiation,

$$(f \cdot g)' = f' \cdot g' \quad \text{and} \quad \left(\frac{f}{g}\right)' = \frac{f' \cdot g' + g \cdot f'}{g^2}$$

it can be shown that the rate of change of with is given by,

$$\frac{d\vartheta}{dk} = \frac{-1}{\sqrt{1 - (\frac{1-k^2}{1+k^2})^2}} \cdot \frac{-4k}{(1+k^2)^2} = \frac{2}{(1+k^2)^2}$$

Hence, associate with the equation, when  $k \rightarrow 1$  (0 dB), the rate of change of phase difference between the two signals entering the phase comparison reaches the maximum processing at 1 rad/unit-k (2 rad/dB). Therefore, if a phase comparison could be made between these two signals with greater than half the accuracy in absolute radians than could be observed on the difference in power of the two, then a more accurate amplitude estimation would result.

#### 4.2.2 Phase comparison

The phase comparison was straightforward as the hybrid circuit provides the phase measurement directly. Associated with the block diagram shown in figure 4.2, the first input has 90 degrees shifting before driving to the phase comparator.

$$V_{in\text{ 1-shift}} = A \cos\left(\omega t - \frac{\pi}{2}\right) = A \sin(\omega t)$$

The two signals will then be mixed,

$$V_m = A \sin(\omega t) \cdot [-k \cdot A \cos(\omega t + \varphi)] = \frac{kA^2}{2} [\sin(\varphi) - \sin(\omega t + 2\omega t + \varphi)]$$

After the low-pass filter, the high frequency part is removed,

$$V_{phase} = \frac{kA^2}{2} \sin(\varphi)$$

Hence, the maximum accuracy is reached when  $\varphi \rightarrow 0$ .

### 4.3 Mathematic modelling

#### 4.3.1 MATLAB plot

In this section, MATLAB (a high-level language and interactive environment to perform computationally intensive tasks) was used to model and plot the mathematical format discussed in section 4.2. The phase estimation was straightforward, using phase comparison technique to output a DC signal. Meanwhile, the amplitude offset can be represented as,

$$\cos\vartheta = \frac{\overline{V_{sum}} \cdot \overline{V_{difference}}}{|\overline{V_{sum}}| \cdot |\overline{V_{difference}}|} = \frac{1 - k^2}{\sqrt{1 + 2k^2 \cos(\omega t + 2\varphi) + k^4}}$$

Hence, the expression indicated that the amplitude error can be estimated by using phase comparison as well.

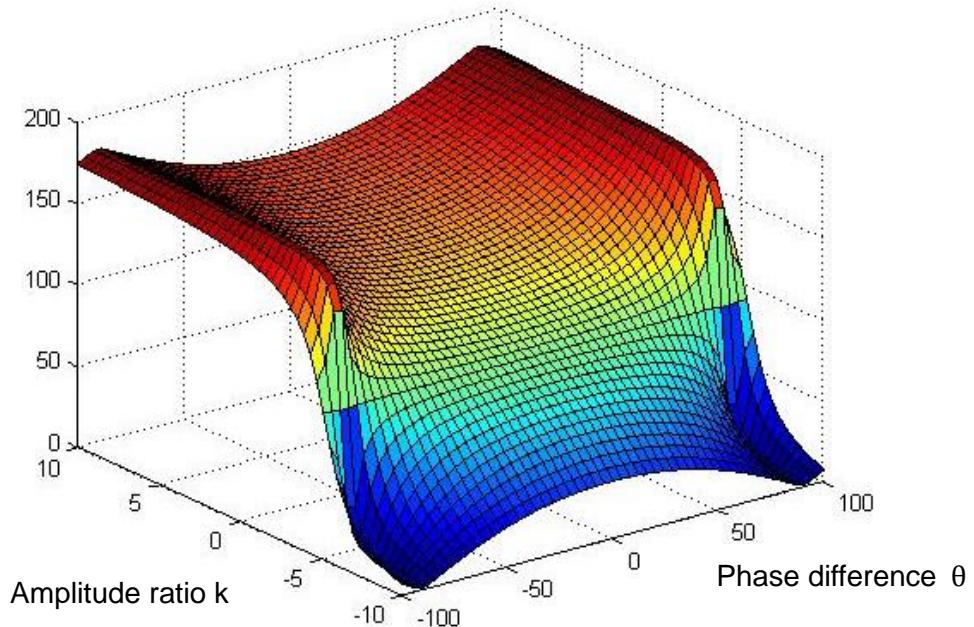


Fig 4.5 Phase difference plot by MATLAB

The diagram shown above was the MATLAB plotting of the phase difference of amplitude offset detected by phase comparison (the code can be found in appendix A). By looking at the value in the matrix of phase difference  $\vartheta$  and amplitude ratio  $k$ , when  $\vartheta \rightarrow 90^\circ$ ,  $k \rightarrow 0$  dB. It is same as the analysis of the equations listed in section 4.2.1. This part achieved researching the wider context as described in the review section. Meanwhile, specific research is achieved corresponding to researching the potential elements to implement the control system.

#### 4.4 Circuit structure of signal amplitude and phase estimation

In reference to the calculation in section 4.2, the common circuit components of amplitude and phase estimation were an analogue multiplier and low-pass filter. For amplitude error detection, the mixed signal for sum and difference signal can be represented as the following consequence. In association with figure 4.2, the target signal was shifted by 90 degrees,

$$V_{Q2} = -k \cdot \text{Acos}(\omega t + \varphi - \pi/2) = -k \cdot \text{Asin}(\omega t + \varphi)$$

Then, the signal will send to the sum and difference hybrid,

$$\begin{aligned} V_{\text{sum}} &= V_{\text{in}1} + V_{\text{in}2-\text{shift}} = \text{Acos}(\omega t) - k \cdot \text{Asin}(\omega t + \varphi) \\ &= \text{Acos}(\omega t) - k[\sin(\omega t) \cos(\varphi) + \cos(\omega t) \sin(\varphi)] \\ &= [A - k\text{Asin}(\varphi)] \cos(\omega t) - kA \cos(\varphi) \sin(\omega t) \end{aligned}$$

For the difference,

$$\begin{aligned} V_{\text{difference}} &= V_{\text{in}1} - V_{\text{in}2-\text{shift}} = \text{Acos}(\omega t) + k \cdot \text{Asin}(\omega t + \varphi) \\ &= \text{Acos}(\omega t) + k[\sin(\omega t) \cos(\varphi) + \cos(\omega t) \sin(\varphi)] \\ &= [A + k\text{Asin}(\varphi)] \cos(\omega t) + kA \cos(\varphi) \sin(\omega t) \end{aligned}$$

Mixed signal,

$$V_{m2} = V_{\text{sum}} \cdot V_{\text{difference}} = [\text{Acos}(\omega t) - k \cdot \text{Asin}(\omega t + \varphi)] \cdot [\text{Acos}(\omega t) + k \cdot \text{Asin}(\omega t + \varphi)]$$

$$\begin{aligned}
&= [A \cos(\omega t)]^2 - [k \cdot A \sin(\omega t + \varphi)]^2 = A^2 \cos^2(\omega t) - k^2 A^2 \sin^2(\omega t + \varphi) \\
&= A^2 \cos^2(\omega t) - k^2 A^2 [\sin(\omega t) \cos(\varphi) + \cos(\omega t) \sin(\varphi)]^2 \\
&= A^2 \{\cos^2(\omega t) - k^2 [\sin(\omega t) \cos(\varphi) + \cos(\omega t) \sin(\varphi)]^2\} \\
&= A^2 \{\cos^2(\omega t) - k^2 [\sin^2(\omega t) \cos^2(\varphi) \\
&\quad + 2 \sin(\omega t) \cos(\varphi) \cos(\omega t) \sin(\varphi) + \cos^2(\omega t) \sin^2(\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) - k^2 [\sin^2(\omega t) \cos^2(\varphi) \\
&\quad + 2 \sin(\omega t) \cos(\omega t) \cos(\varphi) \sin(\varphi) + \cos^2(\omega t) \sin^2(\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) - k^2 [\sin^2(\omega t) \cos^2(\varphi) + \frac{1}{2} \sin(2\omega t) \sin(2\varphi) + \cos^2(\omega t) \sin^2(\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) - k^2 [\frac{1}{2} \sin(2\omega t) \sin(2\varphi) + \sin^2(\omega t) \cos^2(\varphi) + \cos^2(\omega t) \sin^2(\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) - k^2 [\frac{1}{2} \sin(2\omega t) \sin(2\varphi) + [1 - \cos^2(\omega t)] \cos^2(\varphi) + \cos^2(\omega t) \sin^2(\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) - k^2 [\frac{1}{2} \sin(2\omega t) \sin(2\varphi) + \cos^2(\varphi) - \cos^2(\omega t) \cos^2(\varphi) + \cos^2(\omega t) \sin^2(\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) - k^2 [\frac{1}{2} \sin(2\omega t) \sin(2\varphi) + \cos^2(\varphi) - \cos^2(\omega t) [\cos^2(\varphi) - \sin^2(\varphi)]]\} \\
&= A^2 \{\cos^2(\omega t) - k^2 [\frac{1}{2} \sin(2\omega t) \sin(2\varphi) + \cos^2(\varphi) - \cos^2(\omega t) \cos(2\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) - k^2 [\frac{1}{2} \sin(2\omega t) \sin(2\varphi) + \cos^2(\varphi) - \frac{1}{2} (1 + \cos(2\omega t)) \cos(2\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) - \frac{k^2}{2} [\sin(2\omega t) \sin(2\varphi) + 2 \cos^2(\varphi) - (1 + \cos(2\omega t)) \cos(2\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) - \frac{k^2}{2} [\sin(2\omega t) \sin(2\varphi) + 2 \cos^2(\varphi) - \cos(2\varphi) - \cos(2\varphi) \cos(2\omega t)]\} \\
&= A^2 \{\cos^2(\omega t) + \frac{k^2}{2} [\cos(2\varphi) \cos(2\omega t) - \sin(2\omega t) \sin(2\varphi) + \cos(2\varphi) - 2 \cos^2(\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) + \frac{k^2}{2} [\cos(2\varphi) \cos(2\omega t) - \sin(2\omega t) \sin(2\varphi) + \cos(2\varphi) - 2 \cos^2(\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) + \frac{k^2}{2} [\cos(2\omega t + 2\varphi) + \cos(2\varphi) - 2 \cos^2(\varphi)]\} \\
&= A^2 \{\cos^2(\omega t) + \frac{k^2}{2} [\cos(2\omega t + 2\varphi) - 1]\} \\
&= A^2 \{\frac{1}{2} [1 + \cos(2\omega t)] + \frac{k^2}{2} [\cos(2\omega t + 2\varphi) - 1]\} \\
&= \frac{A^2}{2} \{[1 + \cos(2\omega t)] + k^2 [\cos(2\omega t + 2\varphi) - 1]\} \\
&= \frac{A^2}{2} \{1 - k^2 + \cos(2\omega t) + k^2 \cos(2\omega t + 2\varphi)\}
\end{aligned}$$

Hence, the amplitude difference can be obtained as an DC voltage, by removing the high frequency part. In this term, the remaining part can be written as,

$$\mathbf{V}_a = \frac{A^2}{2} (\mathbf{1} - \mathbf{k}^2)$$

Meanwhile, for the phase error, the reference signal should be shifted 90 degrees,

$$V_{Q1} = A \cos(\omega t - \pi/2) = A \sin(\omega t)$$

And the mixed output was,

$$\begin{aligned} V_{m1} &= V_{Q1} \cdot V_{in2} = A \sin(\omega t) \times -k A \cos(\omega t + \varphi) \\ &= kA^2 \{ \sin(\omega t) \cdot [\sin\varphi \cdot \sin(\omega t) - \cos\varphi \cdot \cos(\omega t)] \} \\ &= kA^2 [\sin\varphi \cdot \sin^2(\omega t) - \cos\varphi \cdot \cos(\omega t) \cdot \sin(\omega t)] \\ &= \frac{kA^2}{2} [2 \times \sin\varphi \cdot \sin^2(\omega t) - 2 \times \cos\varphi \cdot \cos(\omega t) \cdot \sin(\omega t)] \\ &= \frac{kA^2}{2} [\sin\varphi \cdot 2\sin^2(\omega t) - 2 \times \cos\varphi \cdot \cos(\omega t) \cdot \sin(\omega t)] \\ &= \frac{kA^2}{2} \{ \sin\varphi \cdot [1 - [1 - 2\sin^2(\omega t)]] - \cos\varphi \cdot \sin(2\omega t) \} \\ &= \frac{kA^2}{2} \{ \sin\varphi \cdot [1 - \cos(2\omega t)] - \cos\varphi \cdot \sin(2\omega t) \} \\ &= \frac{kA^2}{2} \{ \sin\varphi - [\sin\varphi \cdot \cos(2\omega t) + \cos\varphi \cdot \sin(2\omega t)] \} \\ &= \frac{kA^2}{2} [\sin\varphi - \sin(2\omega t + \varphi)] \end{aligned}$$

Therefore, by implementing a low-pass filter, (removing the high frequency part) the phase error can be detected as DC voltage as well,

$$V_p = \frac{kA^2}{2} \sin\varphi$$

## 4.5 Analogue multiplier

The analogue multiplier was able to mix two signals. Associated with this project, this was a common circuit for both amplitude and phase estimation.

### 4.5.1 Diode based

A simple example to create a mixer was to use the diode. For a diode,

$$I = I_S \left( e^{\frac{qV_D}{nkT}} - 1 \right)$$

Hence, the diode mixer provided the original frequencies as well as their sum and their difference. As the diode was a non-linear device, it cannot reproduce the frequency from the input signal. Therefore, it allowed the desired frequency manipulation. For the equation, the exponent can be expanded as,

$$e^x = \sum_{n=0}^{\infty} \frac{x^n}{n!}$$

And,

$$e^x - 1 \approx x + \frac{x^2}{2}$$

Assuming that the sum of the two inputs  $v_1 + v_2$  were applied to a diode, the output voltage became proportional to the current through the diode,

$$v_o = (v_1 + v_2) + \frac{1}{2}(v_1 + v_2)^2 + \dots$$

The first term was the sum signal followed by the square of the sum, which can be rewritten as,

$$(v_1 + v_2)^2 = v_1^2 + 2v_1v_2 + v_2^2$$

Hence, the multiplication was achieved. Also, the ellipsis represents all the higher powers of the sum that are assumed to be negligible for small signals.

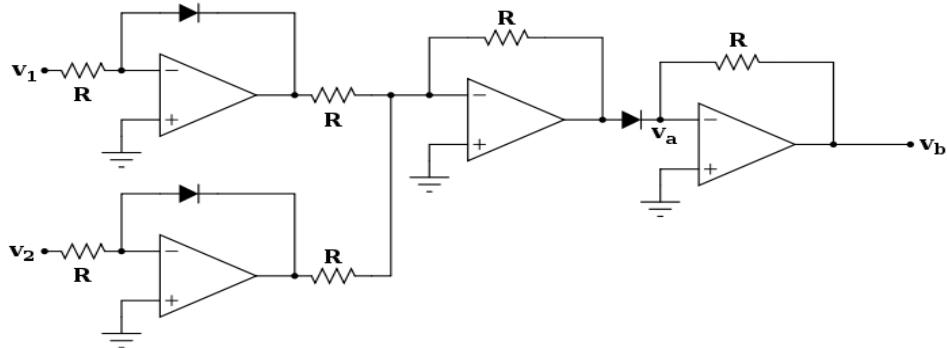


Fig 4.6 Diode based multiplier

(Reference: [http://en.wikibooks.org/wiki/Electronics/Analog\\_multipliers](http://en.wikibooks.org/wiki/Electronics/Analog_multipliers))

Assuming that all the resistors had the same value, and in association with the current relationship, the voltage for node A can be written as,

$$v_a = - \left[ -V_T \ln \left( \frac{v_1}{RI_s} + 1 \right) - V_T \ln \left( \frac{v_2}{RI_s} + 1 \right) \right] = V_T \ln \left[ \left( \frac{v_1}{RI_s} + 1 \right) \left( \frac{v_2}{RI_s} + 1 \right) \right]$$

And the output of the circuit was,

$$v_b = -RI_s \left( e^{\frac{v_a}{V_T}} - 1 \right) = -\frac{v_1 \cdot v_2}{RI_s} - (v_1 + v_2)$$

Therefore, in order to remain the multiplication, only a sum circuit can be added,

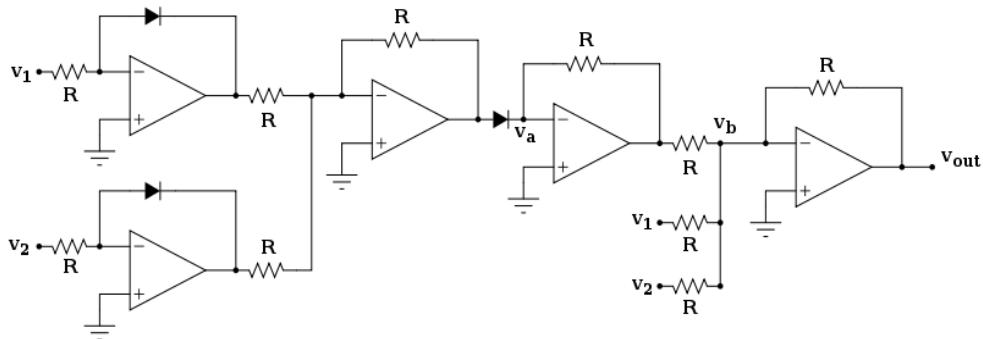


Fig 4.7 Diode based multiplier with sum circuit

(Reference: [http://en.wikibooks.org/wiki/Electronics/Analog\\_multipliers](http://en.wikibooks.org/wiki/Electronics/Analog_multipliers))

Here, refer to the discussion in section 4.8, an inverting amplifier was added with the input in parallel. Therefore the output of this circuit is represented as,

$$v_{out} = - \left( -\frac{v_1 \cdot v_2}{RI_s} - (v_1 + v_2) + (v_1 + v_2) \right) = \frac{v_1 \cdot v_2}{RI_s}$$

#### 4.5.2 Combiner based

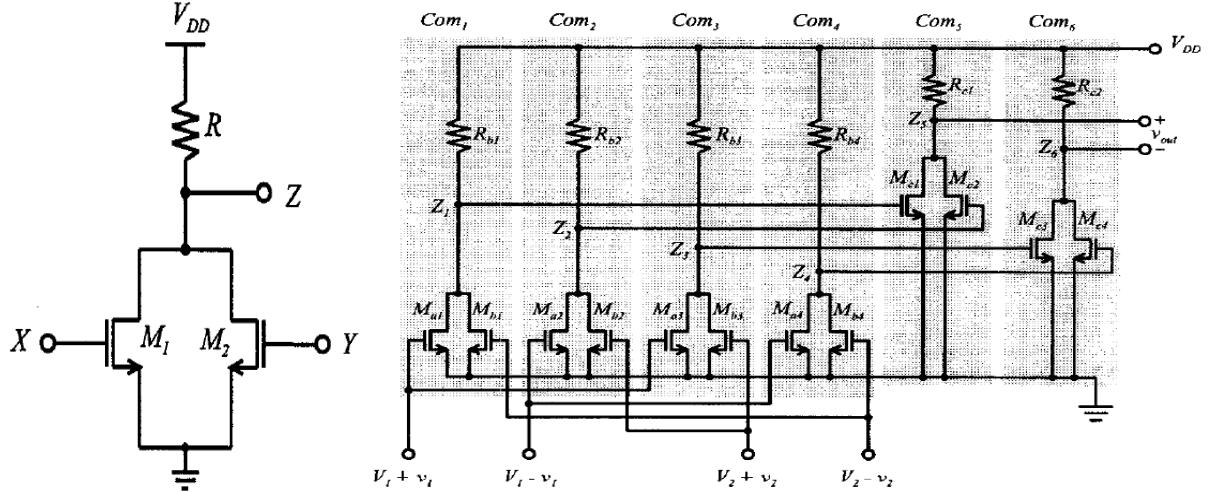


Fig 4.8 Combiner based multiplier

(Reference: S. Hsiao and C. Wu "A 1.2 V CMOS Four-Quadrant Analog Multiplier," 1997

IEEE International Symposium on Circuits and Systems, June 9-12, 1997, Hong Kong)

Figure 4.8 illustrates a combiner-based multiplier [29]. The simple circuit shown on the left was a single combiner, X and Y were the differential input, and Z was the output of combiner,

$$\begin{aligned} Z &= V_{DD} - R \left[ K_1 (X - V_T)^2 + K_2 (Y - V_T)^2 \right] \\ &= -RK_1 X^2 - RK_2 Y^2 + 2RK_1 V_T X + 2RK_2 V_T Y \\ &\quad + \left( V_{DD} - RK_1 V_T^2 - RK_2 V_T^2 \right) \end{aligned}$$

Meanwhile, the right circuit indicated how to use six combiners to implement a multiplier,

$$\begin{aligned} Z_1 &= A_1(V_1 + v_1)^2 + A_2(V_2 + v_2)^2 + A_3(V_1 + v_1) + A_4(V_2 + v_2) + A_5 \\ Z_2 &= A_1(V_1 - v_1)^2 + A_2(V_2 - v_2)^2 + A_3(V_1 - v_1) + A_4(V_2 - v_2) + A_5 \\ Z_3 &= A_1(V_1 + v_1)^2 + A_2(V_2 - v_2)^2 + A_3(V_1 + v_1) + A_4(V_2 - v_2) + A_5 \\ Z_4 &= A_1(V_1 - v_1)^2 + A_2(V_2 + v_2)^2 + A_3(V_1 - v_1) + A_4(V_2 + v_2) + A_5 \end{aligned}$$

Also, for the second stage of the combiner, the Z output can be written as,

$$\begin{aligned} Z_5 &= B_1 Z_1^2 + B_2 Z_2^2 + B_3 Z_1 + B_4 Z_2 + B_5 \\ Z_6 &= B_1 Z_3^2 + B_2 Z_4^2 + B_3 Z_3 + B_4 Z_4 + B_5 \end{aligned}$$

Where A and B were controlled by resistor and threshold voltage,

$$\begin{aligned}
A_1 &= -R_b K_a \\
A_2 &= -R_b K_b \\
A_3 &= 2R_b K_a V_T \\
A_4 &= 2R_b K_b V_T \\
A_5 &= V_{DD} - R_b K_a V_T^2 - R_b K_b V_T^2 \\
B_1 &= B_2 = -R_c K_c \\
B_3 &= B_4 = 2R_c K_c V_T \\
B_5 &= V_{DD} - 2R_c K_c V_T^2
\end{aligned}$$

Therefore, the output of the multiplier can be represented as,

$$v_{out} = \left[ -32R_c K_c R_b^2 K_b K_a (V_1 - V_T)(V_2 - V_T) \right] v_1 v_2$$

The advantage of this structure was that it required low supply voltage. Also, the inputs were independent to each other, and both of the input amplitudes can sweep within the supply voltage. Furthermore, the circuit was able to work as symmetric or asymmetric by setting the values of  $K_a$  and  $K_b$ . In other words, it was a symmetric design in that the signal paths from both inputs to the output can be equal. However, refer to the expression for output, the multiplication was complicated to achieve, as many parameters affected the result.

#### 4.5.3 Gilbert cell based

A differential input, source-coupled pairs could be employed in a multiplier circuit. In analogue electronics, the Gilbert cell was widely used as basic structure to implement multiplication. Associated with the following circuit, it contained three source-coupled pairs, two of them controlled by the input  $X$ , and the third one by the  $Y$  input,

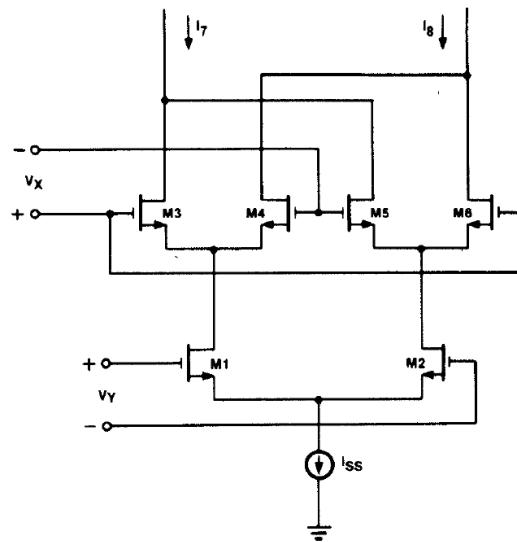


Fig 4.9 Gilbert cell

The output current can be written as,

$$\begin{aligned}
I_{out} &= I_7 - I_8 = (I_3 + I_5) - (I_4 + I_6) \\
&= (I_3 - I_4) - (I_6 - I_5).
\end{aligned}$$

Where  $I_3$  to  $I_6$  represents the currents flowing in corresponding transistors,

$$\begin{aligned}
 I_{\text{out}} &= kV_X \left[ \sqrt{\left( \sqrt{\frac{I_{SS}}{k}} - \frac{V_Y^2}{2} + \frac{V_Y}{\sqrt{2}} \right)^2} - V_X^2 \right. \\
 &\quad \left. - \sqrt{\left( \sqrt{\frac{I_{SS}}{k}} - \frac{V_Y^2}{2} - \frac{V_Y}{\sqrt{2}} \right)^2} - V_X^2 \right] \\
 I_{\text{out}} &\approx kV_X \left[ \sqrt{\left( \sqrt{\frac{I_{SS}}{k}} - \frac{V_Y^2}{2} + \frac{V_Y}{\sqrt{2}} \right)^2} \right. \\
 &\quad \left. - \sqrt{\left( \sqrt{\frac{I_{SS}}{k}} - \frac{V_Y^2}{2} - \frac{V_Y}{\sqrt{2}} \right)^2} \right] \\
 &= \sqrt{2} kV_X V_Y.
 \end{aligned}$$

Therefore, a multiplication was achieved. Compared to other structures, the Gilbert cell provided a direct result using differential current output. Unlike the previous two examples, the output can be proportional controlled by the output resistance. The Gilbert cell also required fewer components, which will save costs for industry fabrication.

## 4.6 Low-pass filter

Table 1 Different type of filter

Filter type	Description	Advantage	Disadvantage
Butterworth	<p>pass-band edge <math>\omega_p</math> :</p> $ T(j\omega)  = \frac{1}{\sqrt{1 + \epsilon^2 \cdot (\omega/\omega_p)^{2N}}}$ <p>parameter <math>\epsilon</math> determines <math>A_{\max}</math> according to:</p> $A_{\max} = 20 \cdot \log_{10} \sqrt{1 + \epsilon^2}$ $\epsilon = \sqrt{10^{A_{\max}/10} - 1}$ <p>stop-band edge, <math>\omega_s</math>, the attenuation is given by:</p> $A(\omega_s) = -20 \cdot \log_{10} \left[ 1 / \sqrt{1 + \epsilon^2 \cdot (\omega_s/\omega_p)^{2N}} \right]$ $= 10 \cdot \log_{10} \left[ 1 + \epsilon^2 \cdot \left( \omega_s/\omega_p \right)^{2N} \right]$ <p>transfer function:</p> $T(s) = \frac{K \omega_0^N}{(s - p_1)(s - p_2) \dots (s - p_N)}$	<p>Maximally flat magnitude response in the pass-band.</p> <p>Pulse response better than Chebyshev.</p> <p>Rate of attenuation better than Bessel.</p>	<p>Some overshoot and ringing in step response.</p>
Chebyshev	<p>pass-band edge <math>\omega_p</math>:</p> $ T(j\omega)  = \frac{1}{\sqrt{1 + \epsilon^2 \cdot \cos^2(N \cos^{-1}(\omega/\omega_p))}} \quad \text{for } \omega \leq \omega_p$	<p>equal ripple magnitude</p>	<p>Ripple in pass-band.</p> <p>Considerably more</p>

	$ T(j\omega)  = \frac{1}{\sqrt{1 + \epsilon^2 \cdot \cosh^2(N \cosh^{-1}(\omega/\omega_p))}}$ for $\omega \geq \omega_p$ Amax: $A_{max} = 10 \cdot \log_{10}(1 + \epsilon^2)$ parameter $\epsilon$ $\epsilon = \sqrt{10^{A_{max}/10} - 1}$ At the stop-band edge, $\omega_s$ , $A(\omega_s) = 10 \cdot \log_{10} \left[ 1 + \epsilon^2 \cdot \cosh^2 [N \cosh^{-1}(\omega_s/\omega_p)] \right]$ The poles of the Chebyshev filter: $\begin{aligned} p_k &= -\omega_p \cdot \sin \left( \frac{2k-1}{N} \cdot \frac{\pi}{2} \right) \cdot \sinh \left( \frac{1}{N} \sinh^{-1} \frac{1}{\epsilon} \right) + \\ &+ j \omega_p \cdot \cos \left( \frac{2k-1}{N} \cdot \frac{\pi}{2} \right) \cdot \cosh \left( \frac{1}{N} \sinh^{-1} \frac{1}{\epsilon} \right) \quad \text{for } k = 1, 2, 3, \dots, N. \end{aligned}$ The transfer function: $T(s) = \frac{K \omega_p^N}{\epsilon 2^{N-1} (s - p_1)(s - p_2) \dots (s - p_N)}$	Better rate of attenuation beyond the pass-band than Butterworth Unlike Butterworth and Bessel response, which have 3dB attenuation at the cutoff frequency	
Bessel maximally flat time delay	Due to its linear phase response, this filter has excellent pulse response (minimal overshoot and ringing). For a given number of poles, its magnitude response is not as flat, nor is its initial rate of attenuation beyond the -3dB cutoff frequency as steep as the Butterworth. It takes a higher-order Bessel filter to give a magnitude response similar to a given Butterworth filter, but the pulse response fidelity of the Bessel filter may make the added complexity.	Best step response-very little overshoot or ringing	Slower initial rate of attenuation beyond the pass-band than Butterworth

As discussed in table 1, the Chebyshev filter provided less attenuation and less number of orders compared to other types. However, the Butterworth filter had less ripple in passband. Therefore, the Chebyshev filter became first option to implement the low-pass filter.

## 4.7 Operational amplifier

### 4.7.1 Ideal OPAMP (Operational amplifier)

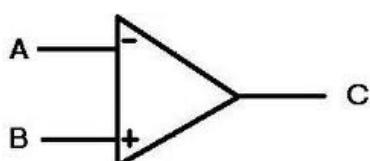


Fig 4.10 Ideal OPAMP

As shown in the above diagram , an ideal OPAMP has three terminals: two input terminals and one output terminal. Here, A and B were inputs, and C was the output terminal. Usually, the OPAMP required a DC voltage supply, shown in the following diagram.

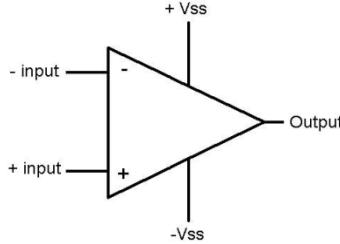


Fig 4.11 Ideal OPAMP with DC supply

An ideal OPAMP was able to sense the difference between the voltage signals applied at its two input terminals, and multiply by the OPAMP gain A. Therefore, in association with figure 4.6,

$$V_c = A \cdot (V_B - V_A)$$

The ideal OPAMP would not draw any input current, or say the signal current into the two input terminals were both zero. It means the input impedance of an ideal OPAMP was desired to be infinite. Similarly, output impedance of an ideal OPAMP should be zero.

#### 4.7.2 Two-stage OPAMP

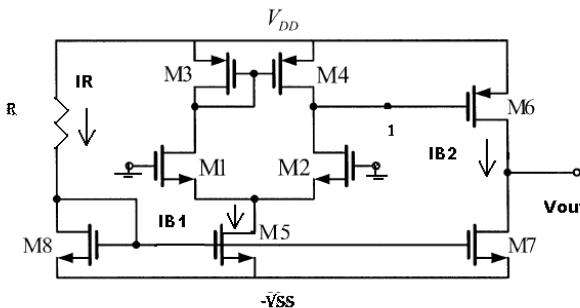


Fig 4.12 Two-stage CMOS op-amp

(Reference: [http://lyle.smu.edu/ee/7321/MOS\\_op-amp\\_design.pdf](http://lyle.smu.edu/ee/7321/MOS_op-amp_design.pdf))

Figure 4.12 illustrates a basic two-stage CMOS OPAMP. On the circuit, the resistor was used to adjust the biasing current, and then driving the current mirrors (M8, M5 and M7). The differential pair was built by M1 and M2, where M3 and M4 provided the active load for the differential amplifier. Furthermore, the M6 was a common source amplifier as the second stage of OPAMP.

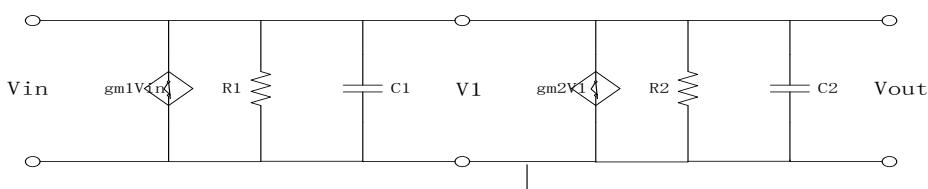


Fig 4.13 Small signal mode of compensated two-stage OPAMP

(Reference: *Microelectronics Circuits, 5th Edition, page 873*)

Figure 4.13 illustrates a small signal mode of the two-stage OPAMP associated with figure 4.12. Here, the S-plane pole locations for each stage can be written as,

$$p_1' = -\frac{1}{R_1 C_1} = -\omega_1$$

And,

$$p_2' = -\frac{1}{R_2 C_2} = -\omega_2$$

Hence, the transfer function was,

$$T(s) = -\frac{g_m R_1}{1 + s R_1 C_1} \times -\frac{g_m R_2}{1 + s R_2 C_2} = \frac{g_m g_m R_1 R_2}{(1 + s/\omega_1)(1 + s/\omega_2)}$$

#### 4.7.3 Compensated two-stage OPAMP

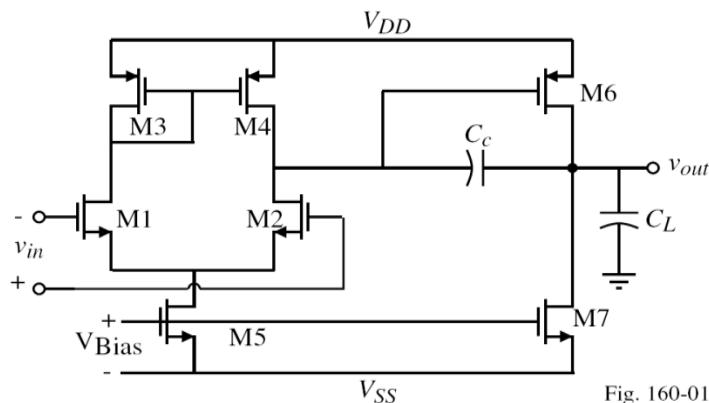


Fig. 160-01

Fig 4.14 Compensated two-stage OPAMP

(Reference: [http://lyle.smu.edu/ee/7321/MOS\\_op-amp\\_design.pdf](http://lyle.smu.edu/ee/7321/MOS_op-amp_design.pdf))

Figure 4.14 is a compensated two stage OPAMP. Compared to the basic OPAMP shown in figure 4.8, a compensated capacitor was added as feedback path from the output to the second stage amplifier. The capacitor is known as the Miller capacitor based on the Miller effect, which can be summarised as the capacitance increase of an amplifier due to amplification of the effect of capacitance between the input and output terminals. Here the additional capacitor separated the poles between two stages in the frequency domain, so that one became dominant. Positioning the capacitor across the inverting voltage amplifier formed by the second stage increased its effect on the circuit performance.

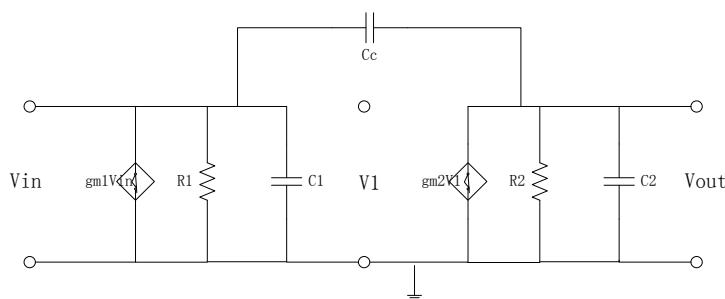


Fig 4.15 Small signal mode of compensated two-stage OPAMP

(Reference: *Microelectronics Circuits, 5th Edition, page 874*)

Again, figure 4.15 is the small signal mode of a compensated two-stage OPAMP in terms of representing the split poles,

$$p_1 \approx -\frac{1}{g_{m2}R_1R_2C_c}$$

And,

$$p_2 \approx -\frac{g_{m2}}{C_2}$$

Compared to the poles in section 4.7.2, the location of the first pole remained on the real axis of the S-plane with a reduced magnitude. Meanwhile, the magnitude of the second pole increased. Thereby, the pole split in terms of increasing the stability. Based on the analysis in section 2.3, stability was an essential consideration for designing the signal amplitude and phase estimation circuits. In other words, a Miller capacitor would improve the performance of the project.

#### 4.7.4 Cascoded two-stage OPAMP

In terms of increasing the gain of the OPAMP, an additional stage can be implemented. However, it required more transistors. Else the transconductance of the amplifier can be increased. Another option was to increase the output resistance. Refer to the calculation of the bias current; the output resistance was proportional to the current, while the transconductance increased as the square root of the bias current. Hence, increasing the output resistance was more effective. However, in VLSI fabrication design, the polysilicon caused a longer delay. To increase the output resistance, as the OPAMP was two stage, both of the stages can be improved by cascoding the mirror. If the first stage was cascaded, the output resistance of first stage would be increased and the overall gain of OPAMP increased. However, the disadvantage of this method was reduction of the input common-mode range as the cascaded mirror required more voltage drop. Furthermore, the stability of the circuit diminished for the large capacitive loading at the output. Another option was cascoding the second stage. It overcame the problem of common-mode range. However, the stability of the OPAMP was reduced. Associated with the signal amplitude and phase estimation, the stability was significant based on the analysis in section 2.3. Hence, a cascaded two-stage OPAMP was not necessary for the project.

### 4.8 Sum and difference circuit

The most fundamental application for the OPAMP was an inverting amplifier. As shown in figure 4.10, connecting the positive node to the ground and using resistors to connect between the negative and output.

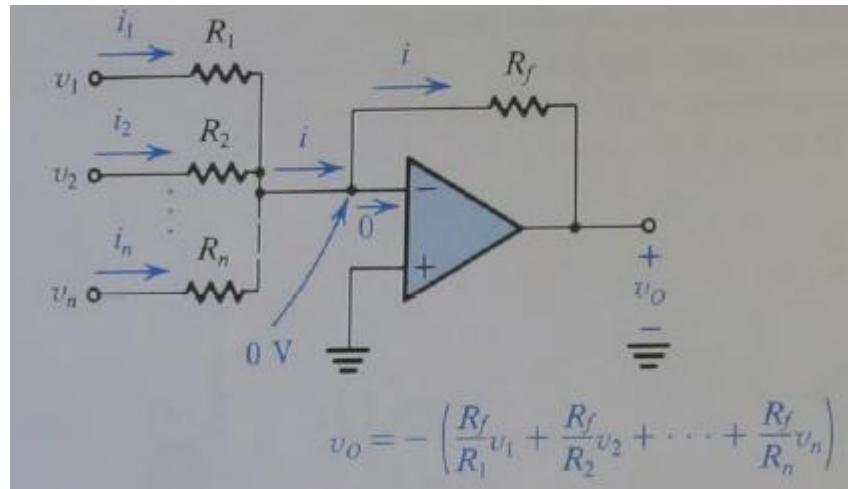


Fig 4.16 Inverting amplifier

(Reference: Microelectronics Circuits, 5th Edition, page 76)

The circuit shown in figure 4.16 indicates that the parallel inputs provided the inverting sum of output depended on the ratio of the resistor. Hence, a positive output can be obtained by inverting twice.

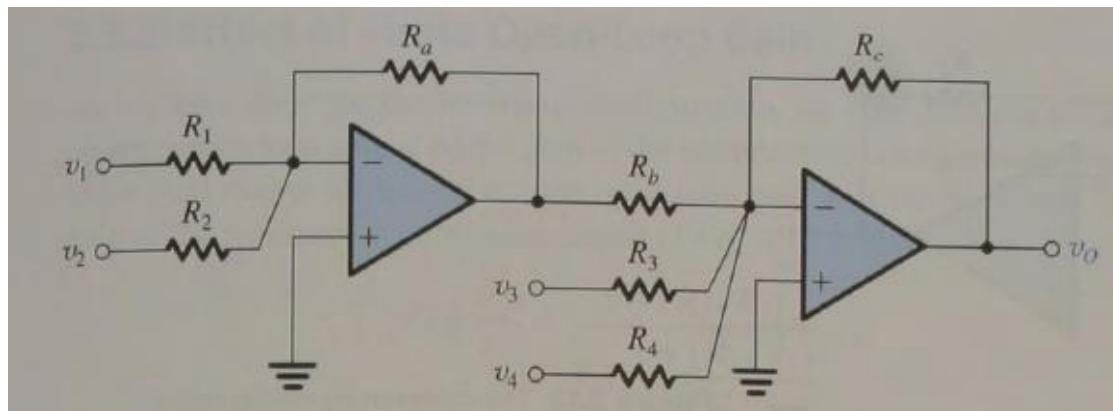


Fig 4.17 Two inverting amplifier

(Reference: Microelectronics Circuits, 5th Edition, page 76)

Therefore, the sum and difference circuit could be implemented by the inverting amplifier by setting the ratio of the resistors to one. To obtain different results, the input was required to connect in order. For instance, the sum circuit could be implemented by connecting the inputs to the first inverting amplifier in parallel. Meanwhile, the difference circuit should connect the inputs to different amplifiers.

# 5 ANALYSIS OF RESULTS

## 5.1 Operational amplifier

### 5.1.1 Two-stage OPAMP

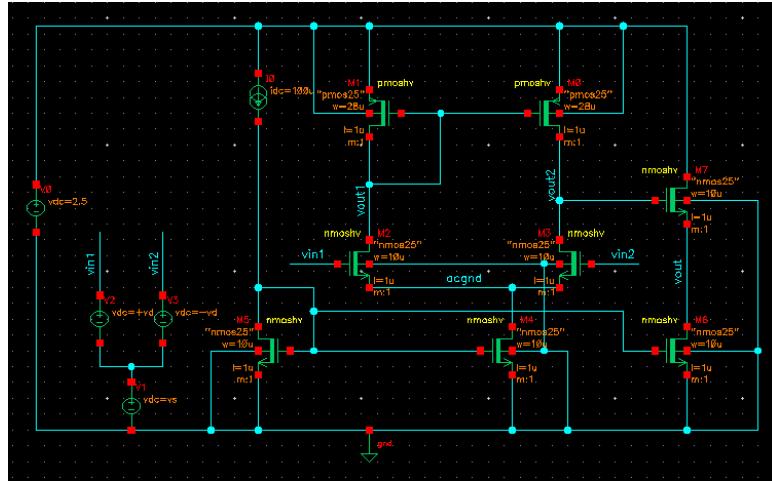


Fig 5.1 Two stage OPAMP

The circuit shown in figure 5.1 was the basic two stage operational amplifier. The first stage was implemented as a pair of differential amplifier and the second stage was achieved by another MOS on the right-hand side of the circuit.

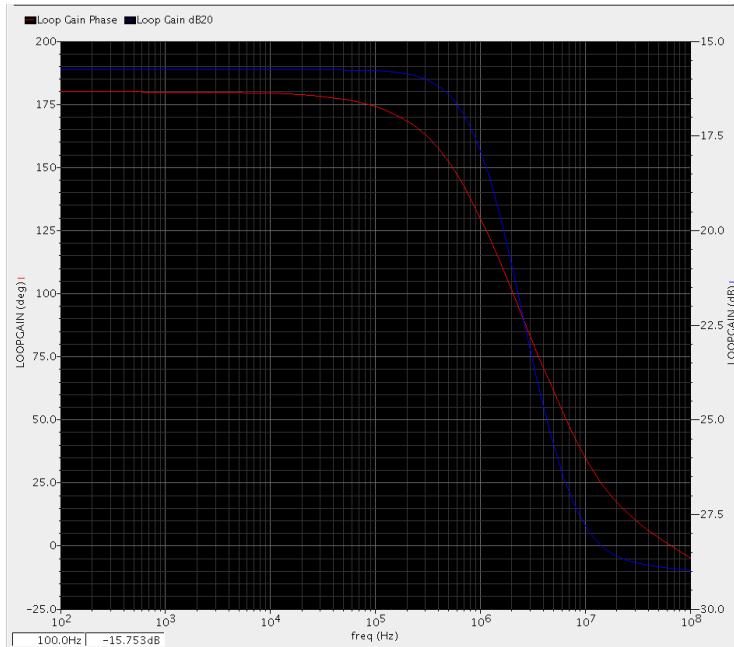


Fig 5.2 Frequency response of two-stage OPAMP

As the result shows, the gain margin was about 28.9dB without phase margin. In other words, this design was not stable and the gain was low.

### 5.1.2 Compensated two-stage OPAMP

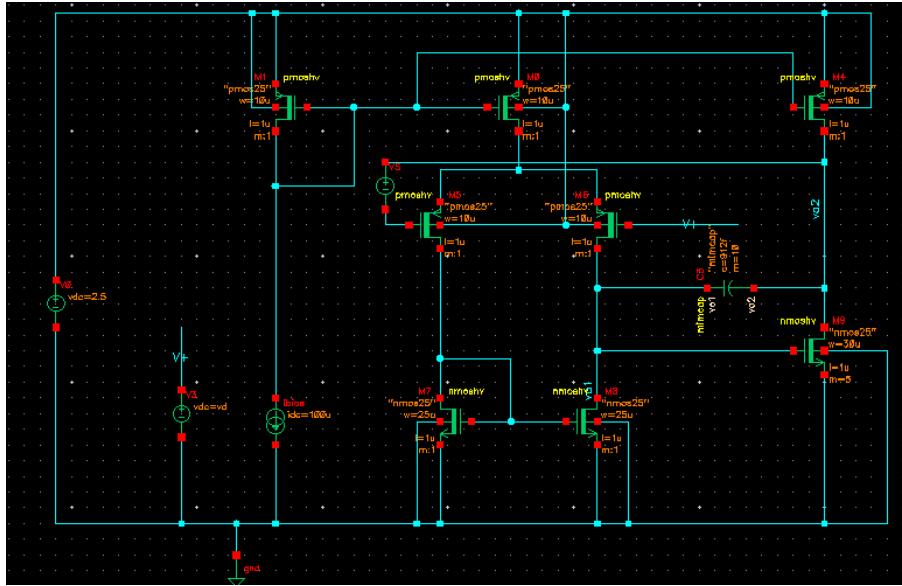


Fig 5.3 Compensated two-stage OPAMP

Figure 5.3 illustrates a compensated two-stage OPAMP. Compared to figure 5.1, a Miller capacitor was added in terms of splitting the poles to increase the stability. Another change was increasing the width of the first and second stage amplifier. Meanwhile, the width of active loads increased to provide a larger output resistance to achieve higher gain.

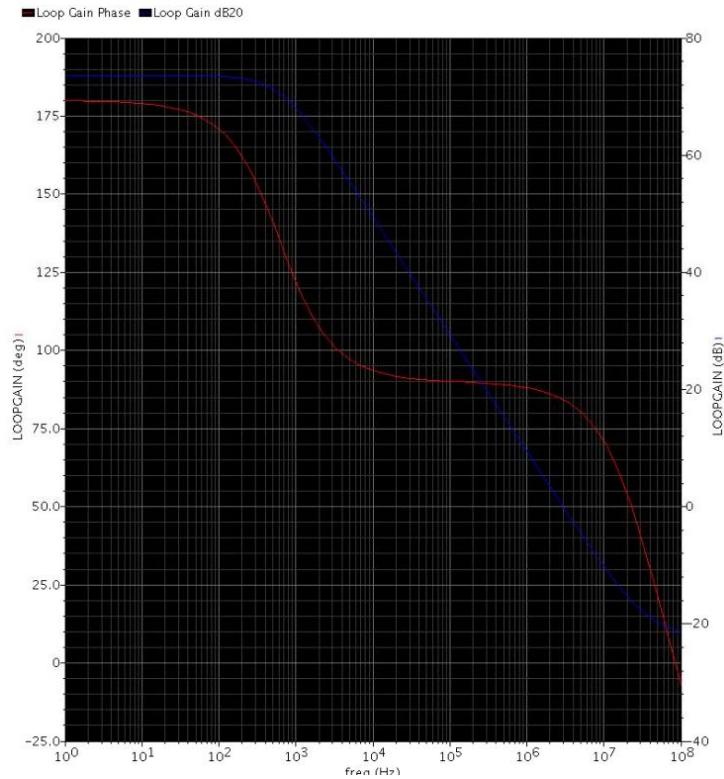


Fig 5.4 Frequency response of compensated two-stage OPAMP

Refer to figure 5.4 and figure 3.20, the phase margin of this design was 74.2 located at 2.98MHz and the gain margin was 20.987 obtained at 85.5MHz. The results indicated the design was stable for industry.

## 5.2 Analogue multiplier

### 5.2.1 Gilbert cell

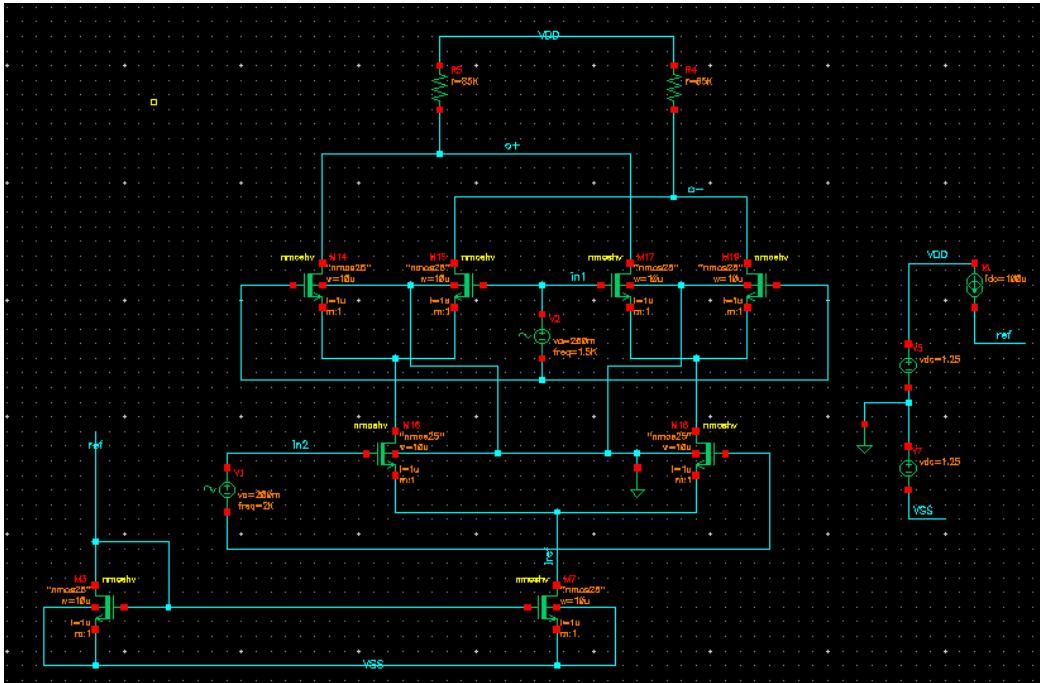


Fig 5.5 Gilbert cell 1

The diagram shown above was an analogue multiplier based on a basic Gilbert cell. It was combined from three pairs of differential amplifiers, and two pairs on the top connected to the one for input, and another input was connected to the bottom pair. The output included, positive and negative nodes labelled on the diagram.

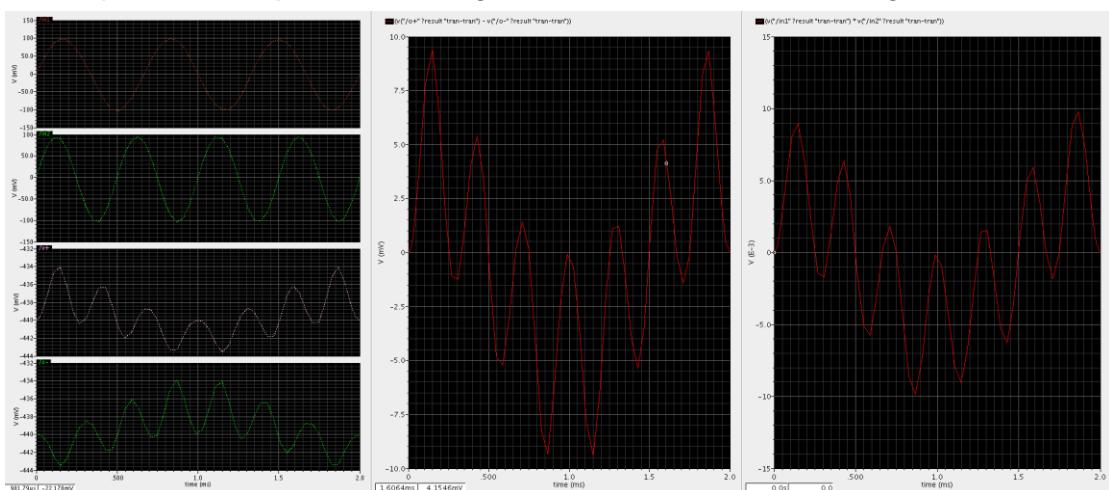


Fig 5.6 Result of Gilbert cell multiplier 1

Figure 5.6 shows the simulation of the Gilbert cell 1. The left window displays the

inputs and output of the multiplier. Meanwhile, the middle window shows the wave for using the calculation to find the difference between two labels. Finally, the right window was the calculation of the multiplication of two inputs. Refer to the output waves, the voltage between two nodes can match the calculation. Hence the Gilbert cell can be chosen as the analogue multiplier. However, there should be only one output voltage to drive the low-pass filter. There were two potential options. One was driving the outputs to the difference circuit. Another was using the current mirror to copy the currents and then drive them to one node; based on the KCL (Kirchhoff's Current Law), the total current flow in is equal to the current flow out, and the difference current can be obtained. A resistor can then be used to proportional control the output voltage for the Gilbert cell based on the difference current.

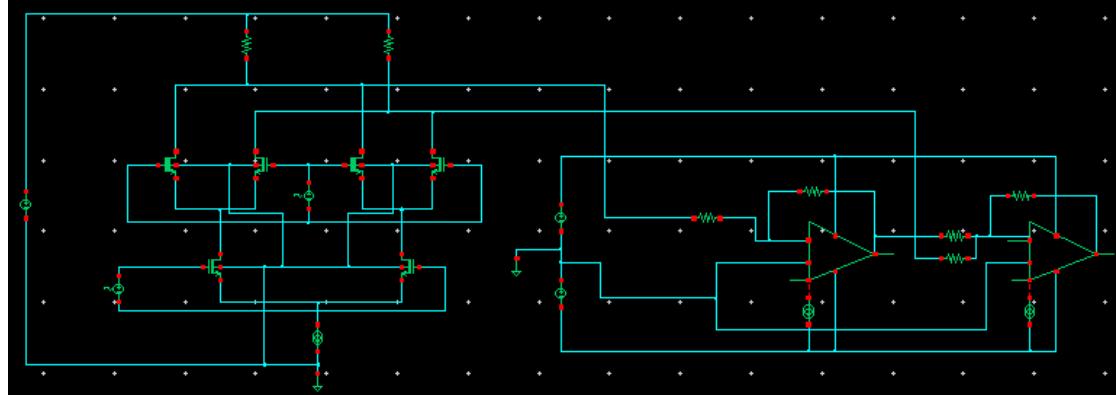


Fig 5.7 Gilbert cell 2

The circuit shown in figure 5.7 was using the difference circuit (in section 4.8) to detect the differential outputs between the positive and negative nodes.

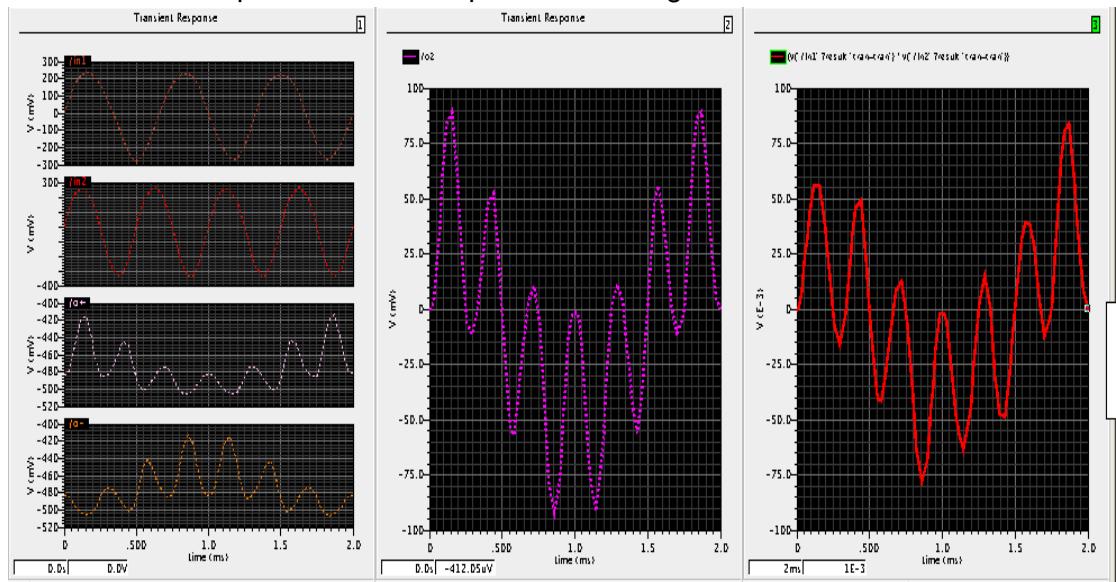


Fig 5.8 Result of Gilbert cell multiplier 2

Figure 5.8 was the output of Gilbert cell 2, the output of the difference circuit can track the multiplication of the inputs. In fact, compared to the circuit for Gilbert cell 1, the resistor was increased to achieve the same result. In other words, the resistor of

difference circuit cost some of the current. Therefore, the output resistance of Gilbert cell had to increase. In order to reduce the effect of the resistor, a voltage follower can be implemented, as shown in the following diagram,

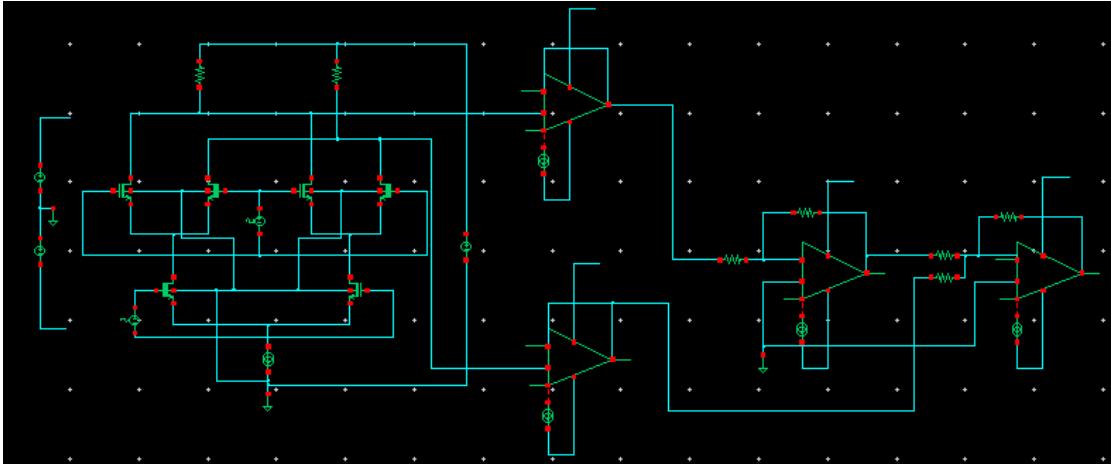


Fig 5.9 Gilbert cell 3

Compared to Gilbert cell 2, the voltage followers were added between the output nodes and the difference circuit.

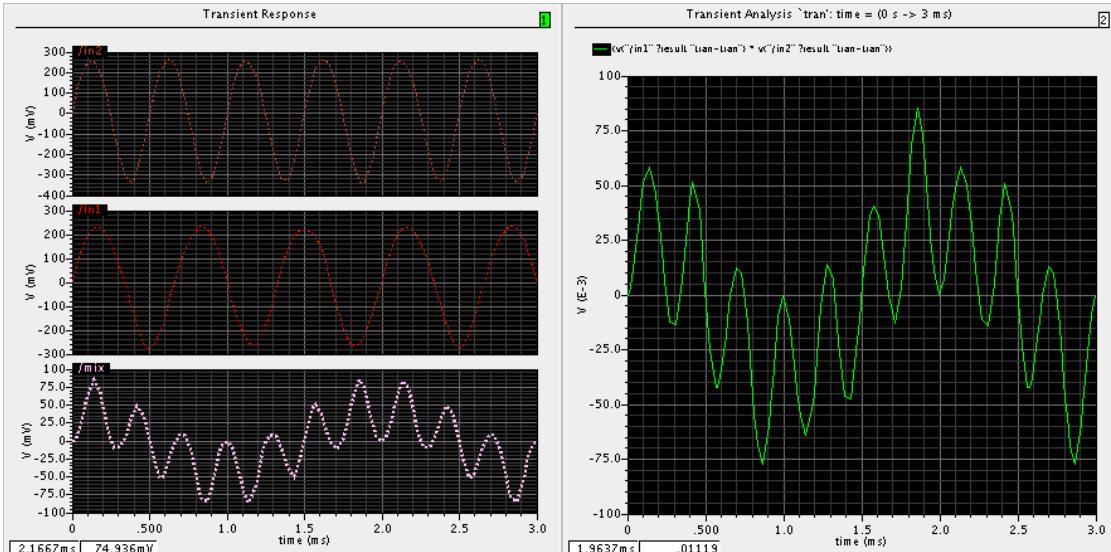


Fig 5.10 Result of Gilbert cell multiplier 3

There were two windows on the diagram: the bottom left was the output wave from the difference circuit, which was matched with the calculation shown in the right window. Here, the output resistor was same as the value used in Gilbert cell multiplier 1. Hence, the voltage follower can buffer the voltage as it had high input impedance and low output impedance.

Based on the previous analysis, another option to obtain the difference voltage between the Gilbert cell's nodes was using the current mirror to copy the currents to a single node.

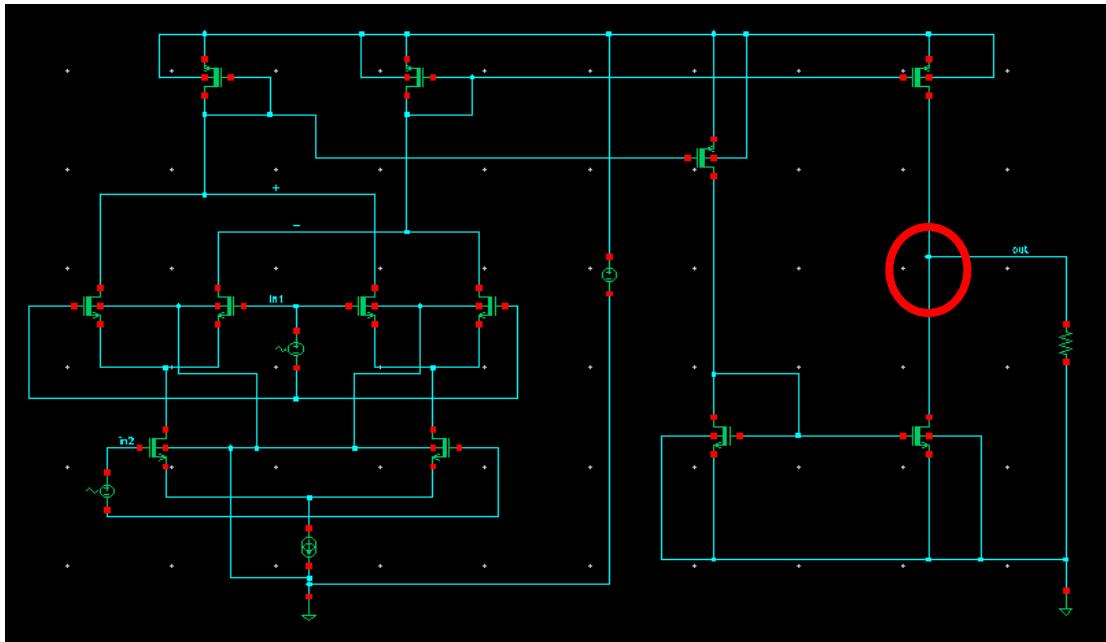


Fig 5.11 Gilbert cell 4

Gilbert cell 4 used a current mirror. Two pairs of current mirrors copy the current from the positive and negative node respectively, and are driven to the same node as the red circle shown. Hence, according to the KCL, the current flowing out of the node is equal to the difference current flowing in. Furthermore, a resistor was used to proportional control the output voltage.

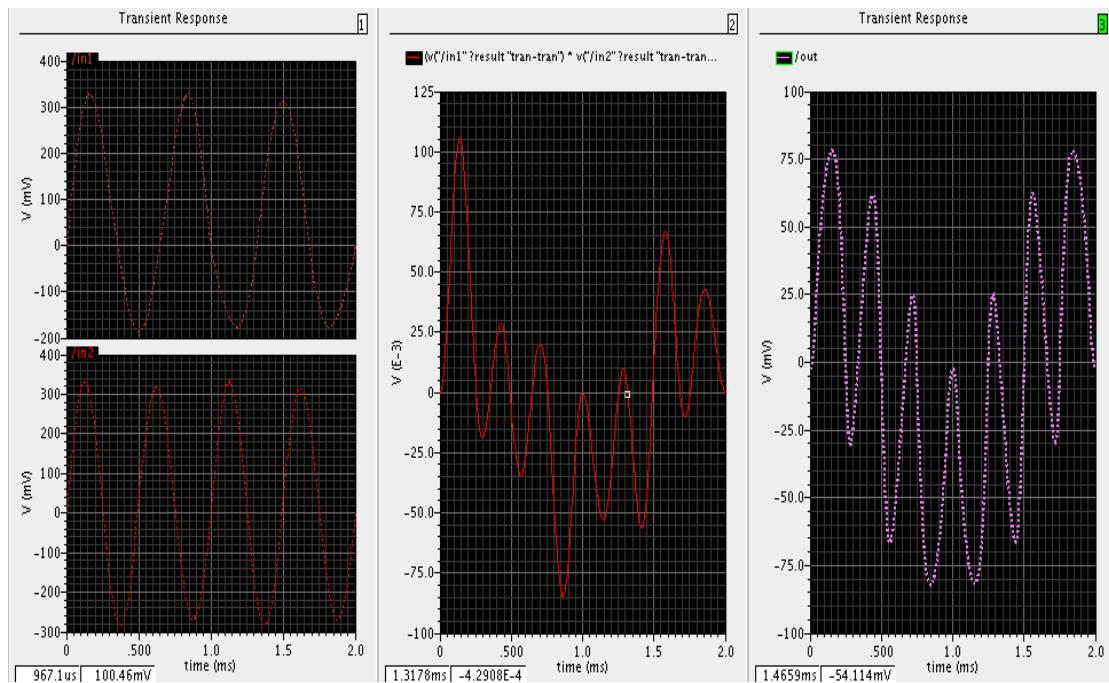


Fig 5.12 Result of Gilbert cell multiplier 4

Figure 5.12 shows that the output matched the calculation. Also, compared to the resistor based, the active load MPS provided larger output resistance as the resistor was much smaller than the resistor based. However, there the current was distorted,

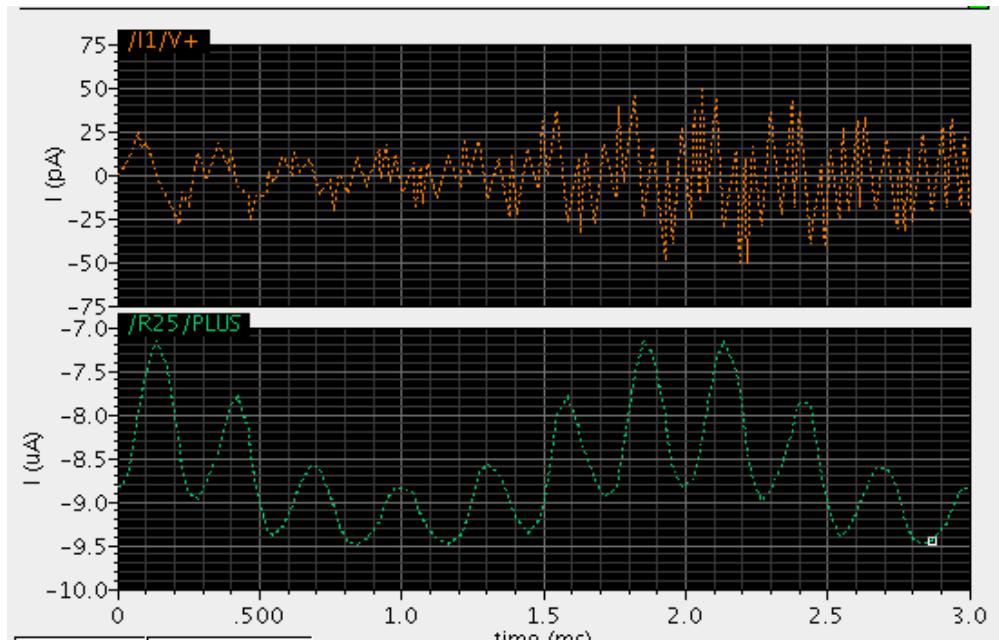


Fig 5.13 Current distortion

As shown in the diagram above, the current for the output node of the Gilbert cell was distorted. To overcome this problem, the output resistance of the Gilbert cell should be increased.

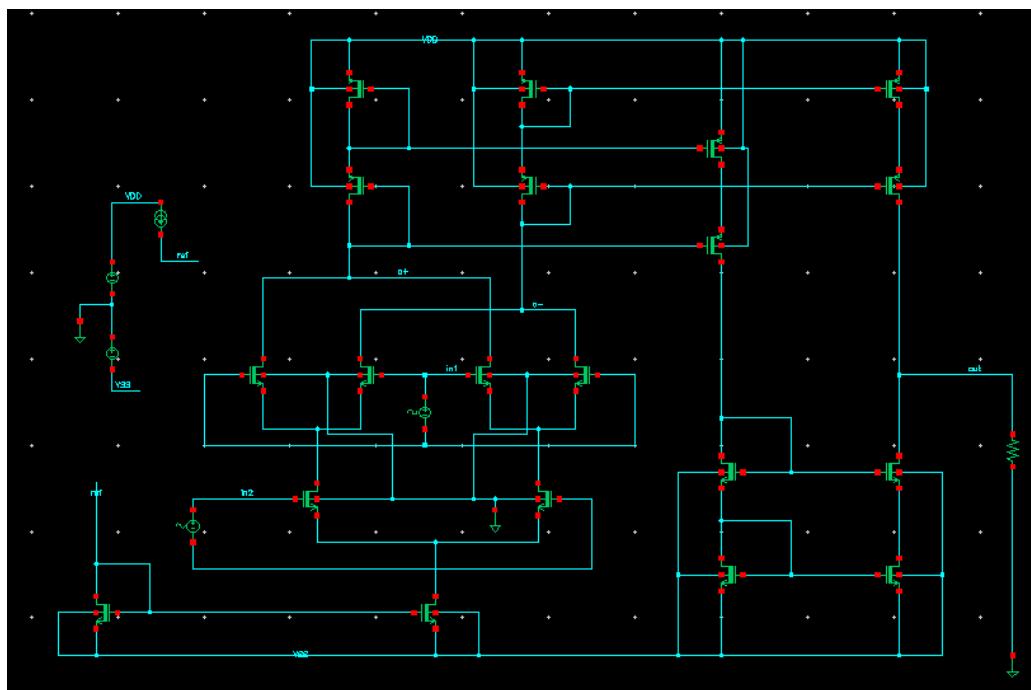


Fig 5.14 Gilbert cell 5

Compared to Gilbert cell 4, this design used the cascode current mirror to increase the output impedance of the Gilbert cell.

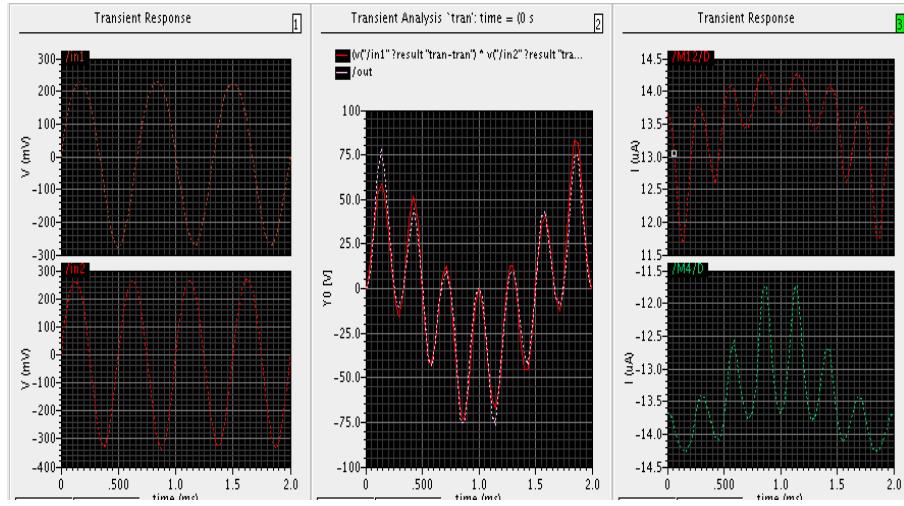


Fig 5.15 Result of Gilbert cell multiplier 5

Again, the output was able to match the multiplication of the inputs as shown in the middle window. At the same time, as the right window shows, the current was sweeping in a smaller range without distortion. The resistor was increased corresponding to the decreased current. Another advantage of implementing a cascaded mirror was that the linearity of the analogue multiplier increased.

### 5.3 Low-pass filter

#### 5.3.1 Chebyshev low-pass filter

As a result of the analysis discussed in section 4.6, a Chebyshev low-pass filter was designed.

##### 5.3.1.1 Specification

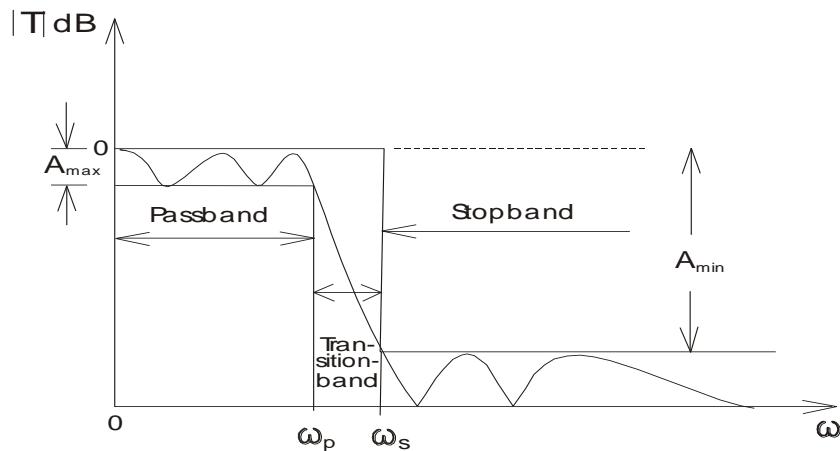


Fig 5.16 real low-pass filter

Table 2 Design specification of Chebyshev low-pass filter

F <sub>p</sub>	F <sub>s</sub>	A <sub>max</sub>	A <sub>min</sub>
20 Hz	40 Hz	1.0 dB	45 dB

### 5.3.1.2 Calculation

The parameter can be calculated as:

$$\begin{aligned}\varepsilon &= \sqrt{10^{\frac{A_{\max}}{10}} - 1} \\ &= \sqrt{10^{0.1} - 1} = \sqrt{1.2589 - 1} = 0.5088\end{aligned}$$

According to,

$$A(\omega_s) = 10 \cdot \log_{10} \{ 1 + \varepsilon^2 \cdot \cosh^2 [N \cosh^{-1} (\omega_s / \omega_p)] \}$$

Substituting the value (from specification) into equation,

$$45 = 10 \cdot \log_{10} \{ 1 + 0.2589 \cdot \cosh^2 [N \cosh^{-1} (2\pi f_s / 2\pi f_p)] \}$$

$$4.5 = \log_{10} \{ 1 + 0.2589 \cdot \cosh^2 [N \cosh^{-1} (f_s / f_p)] \}$$

$$10^{4.5} = 1 + 0.2589 \cdot \cosh^2 [N \cosh^{-1} (f_s / f_p)]$$

$$\cosh^2 [N \cosh^{-1} 2] = 122138.96$$

$$\cosh(N \cdot 1.316) = 349.484$$

$$N \cdot 1.316 = 6.5496$$

$$N = 4.973$$

So the number of order for the low-pass filter was chosen as 5. Then, referring to section 4, the locations of poles and zeros can be found. In this particular case, the order was calculated as N=5,

Pole 1:

$$\begin{aligned}P_1 &= -\omega_p \sin \left( \frac{1}{5} \cdot \frac{\pi}{2} \right) \cdot \sinh \left( \frac{1}{5} \cdot \sinh^{-1} \frac{1}{0.5088} \right) + j\omega_p \cdot \cos \left( \frac{1}{5} \cdot \frac{\pi}{2} \right) \\ &\quad \cdot \cosh \left( \frac{1}{5} \cdot \sinh^{-1} \frac{1}{0.5088} \right) \\ &= -\omega_p 0.309 \cdot \sinh(0.285) + j\omega_p \cdot 0.951 \cdot \cosh(0.285) \\ &= -\omega_p 0.309 \cdot 0.2895 + j\omega_p \cdot 0.951 \cdot 1.041 \\ &= \omega_p (-0.0895 + j0.9901)\end{aligned}$$

Pole 2:

$$\begin{aligned}P_2 &= -\omega_p \sin \left( \frac{3}{5} \cdot \frac{\pi}{2} \right) \cdot \sinh \left( \frac{1}{5} \cdot \sinh^{-1} \frac{1}{0.5088} \right) + j\omega_p \cdot \cos \left( \frac{3}{5} \cdot \frac{\pi}{2} \right) \\ &\quad \cdot \cosh \left( \frac{1}{5} \cdot \sinh^{-1} \frac{1}{0.5088} \right) \\ &= -\omega_p \sin \left( \frac{3}{5} \cdot \frac{\pi}{2} \right) \cdot 0.2895 + j\omega_p \cdot \cos \left( \frac{3}{5} \cdot \frac{\pi}{2} \right) \cdot 1.041 \\ &= -\omega_p 0.809 \cdot 0.2895 + j\omega_p \cdot 0.5878 \cdot 1.041 \\ &= \omega_p (-0.2342 + j0.6119)\end{aligned}$$

Pole 3:

$$\begin{aligned}
P_3 &= -\omega_p \sin\left(\frac{5}{5} \cdot \frac{\pi}{2}\right) \cdot \sinh\left(\frac{1}{5} \cdot \sinh^{-1} \frac{1}{0.5088}\right) + j\omega_p \cdot \cos\left(\frac{5}{5} \cdot \frac{\pi}{2}\right) \\
&\quad \cdot \cosh\left(\frac{1}{5} \cdot \sinh^{-1} \frac{1}{0.5088}\right) \\
&= -\omega_p \sin\left(\frac{5}{5} \cdot \frac{\pi}{2}\right) \cdot 0.2895 + j\omega_p \cdot \cos\left(\frac{5}{5} \cdot \frac{\pi}{2}\right) \cdot 1.041 \\
&= -\omega_p \cdot 0.2895 + j\omega_p \cdot 0 \cdot 1.041 \\
&= \omega_p (-0.2895)
\end{aligned}$$

Pole 4:

$$\begin{aligned}
P_4 &= -\omega_p \sin\left(\frac{7}{5} \cdot \frac{\pi}{2}\right) \cdot \sinh\left(\frac{1}{5} \cdot \sinh^{-1} \frac{1}{0.5088}\right) + j\omega_p \cdot \cos\left(\frac{7}{5} \cdot \frac{\pi}{2}\right) \\
&\quad \cdot \cosh\left(\frac{1}{5} \cdot \sinh^{-1} \frac{1}{0.5088}\right) \\
&= -\omega_p \sin\left(\frac{7}{5} \cdot \frac{\pi}{2}\right) \cdot 0.2895 + j\omega_p \cdot \cos\left(\frac{7}{5} \cdot \frac{\pi}{2}\right) \cdot 1.041 \\
&= -\omega_p \cdot 0.809 \cdot 0.2895 + j\omega_p \cdot -0.5857 \cdot 1.041 \\
&= \omega_p (-0.2342 - j0.6119)
\end{aligned}$$

Pole 5:

$$\begin{aligned}
P_5 &= -\omega_p \sin\left(\frac{9}{5} \cdot \frac{\pi}{2}\right) \cdot \sinh\left(\frac{1}{5} \cdot \sinh^{-1} \frac{1}{0.5088}\right) + j\omega_p \cdot \cos\left(\frac{9}{5} \cdot \frac{\pi}{2}\right) \\
&\quad \cdot \cosh\left(\frac{1}{5} \cdot \sinh^{-1} \frac{1}{0.5088}\right) \\
&= -\omega_p \sin\left(\frac{9}{5} \cdot \frac{\pi}{2}\right) \cdot 0.2895 + j\omega_p \cdot \cos\left(\frac{9}{5} \cdot \frac{\pi}{2}\right) \cdot 1.041 \\
&= -\omega_p \cdot 0.309 \cdot 0.2895 + j\omega_p \cdot -0.951 \cdot 1.041 \\
&= \omega_p (-0.0895 - j0.9901)
\end{aligned}$$

Also, the  $P_5$  will be the conjugate of the  $P_1$ , and there were two poles that can be the type of the denominator of the transfer function.

$$\begin{aligned}
(s - P_1) \cdot (s - P_5) &= [s - \omega_p (-0.0895 + j0.9901)] \cdot [s - \omega_p (-0.0895 - j0.9901)] \\
&= (s + 0.0895\omega_p)^2 - (j0.9901\omega_p)^2 \\
&= s^2 + 0.1789\omega_p s + 0.00801\omega_p^2 + 0.9803\omega_p^2 \\
&= s^2 + 0.1789\omega_p s + 0.9883\omega_p^2
\end{aligned}$$

Similar to  $P_1$  and  $P_5$ , the  $P_2$  and  $P_4$  will be another denominator of the transfer function,

$$\begin{aligned}
(s - P_2) \cdot (s - P_4) &= [s - \omega_p (-0.2342 + j0.6119)] \cdot [s - \omega_p (-0.2342 - j0.6119)] \\
&= (s + 0.2342\omega_p)^2 - (j0.6119\omega_p)^2 \\
&= s^2 + 0.4684\omega_p s + 0.05485\omega_p^2 + 0.3744\omega_p^2 \\
&= s^2 + 0.4684\omega_p s + 0.4293\omega_p^2
\end{aligned}$$

And the real pole should be,

$$(s - p_3) = [s - \omega_p(-0.2895)] = (s + 0.2895\omega_p)$$

Therefore, the transfer function can be written as,

$$T(s) = \frac{K \omega_p^N}{\epsilon 2^{N-1} (s - p_1)(s - p_2) \dots (s - p_N)}$$

$T(s)$

$$\begin{aligned} &= \frac{k\omega_p^5}{8.1408 \cdot [s - \omega_p(-0.0895 + j0.9901)] \cdot [s - \omega_p(-0.2342 + j0.6119)] \cdot [s - \omega_p(-0.2895)]} \\ &\quad \cdot [s - \omega_p(-0.2342 - j0.6119)] \cdot [s - \omega_p(-0.0895 - j0.9901)] \\ &= \frac{k\omega_p^5}{8.1408 \cdot (s + 0.2895\omega_p) \cdot (s^2 + 0.4684s\omega_p + 0.4293\omega_p^2) \cdot (s^2 + 0.1789s\omega_p + 0.9883\omega_p^2)} \end{aligned}$$

The transfer function for the first order filter was,

$$T_1 = \frac{V_{out}}{V_{in}}(s) = k_1 \cdot \left( \frac{\omega_p}{s + a_1 \omega_p} \right) = A_{vo} \cdot \left( \frac{\omega_o}{s + \omega_o} \right)$$

Where,  $\omega_o = a_1 \cdot \omega_p = \frac{1}{CR}$ ,  $A_{vo} = \frac{k_1}{a_1}$

Taking the  $(s + 0.2895\omega_p)$  as the first order,

Where,  $a_1 = 0.2895$

Hence,  $\omega_o = a_1 \cdot \omega_p = 0.2895 \times 2\pi \times 20 = 36.38 \text{ rads/s}$

Choose the capacitor as 100nf,

The resistor should be,

$$R = \frac{1}{C \cdot \omega_o} = \frac{1}{10^{-7} \times 36.38} = 274879\Omega$$

The transfer function for first second order filter was,

$$T_2(s) = \frac{k_2 \cdot \omega_p^2}{s^2 + a_1 \omega_p s + a_2 \omega_p^2} = \frac{A_{vo} \cdot \omega_o^2}{s^2 + (3 - A_{vo})\omega_o s + \omega_o^2}$$

Taking the  $s^2 + 0.1789\omega_p s + 0.9883\omega_p^2$  the first second order. In this case,

$a_1 = 0.1789$ ,  $a_2 = 0.9883$ ,

$$a_2 \omega_p^2 = \omega_o^2$$

$$\rightarrow \omega_o = \sqrt{a_2} \cdot \omega_p = 0.9941 \times 2\pi \times 20 = 124.9 \text{ rads/s}$$

Choose the capacitor as 100nf,

The resistor should be,

$$R = \frac{1}{C \cdot \omega_o} = \frac{1}{10^{-7} \times 124.9} = 800649.77\Omega$$

Also,

$$3 - A_{vo} = \frac{a_1}{\sqrt{a_2}} = \frac{0.1789}{0.9941} = 0.179956$$

$$A_{vo} = 2.820044$$

Because of,

$$A_{vo} = 1 + \frac{R_2}{R_1}$$

$$\rightarrow \frac{R_2}{R_1} = 1.82$$

Choose the value of the  $R_1$  to  $10k\Omega$ , then  $R_2$  should be  $18.2k\Omega$

The transfer function for second second-order was similar to the first one,

$$T_3(s) = \frac{k_2 \cdot \omega_p^2}{s^2 + a_1 \omega_p s + a_2 \omega_p^2} = \frac{A_{vo} \cdot \omega_0^2}{s^2 + (3 - A_{vo})\omega_0 s + \omega_0^2}$$

Taking the  $s^2 + 0.4684\omega_p s + 0.4293\omega_p^2$  as second second-order,

Here, the  $a_1 = 0.4684$ ,  $a_2 = 0.4293$ ,

Hence,

$$\omega_0 = \sqrt{a_2} \cdot \omega_p = 0.6552 \cdot 2\pi \times 40 = 82.33 \text{ rads/s}$$

Choose the capacitor as  $100\text{nf}$ ,

The resistor should be,

$$R = \frac{1}{C \cdot \omega_0} = \frac{1}{10^{-7} \times 82.33} = 121455.23\Omega$$

The  $R_1$  and  $R_2$  can be determined by

$$3 - A_{vo} = \frac{a_1}{\sqrt{a_2}}$$

$$3 - A_{vo} = \frac{0.4684}{\sqrt{0.4293}} = \frac{0.4684}{0.6552} = 0.714885$$

$$A_{vo} = 2.28$$

Hence,

$$\frac{R_2}{R_1} = A_{vo} - 1 = 1.285$$

Therefore, choose the  $10k\Omega$  as  $R_1$ , the  $R_2$  should be  $12.85k\Omega$ .

The overall gain of the low-pass filter was,

$$k = k_1 \cdot k_2 \cdot k_3 = k_1 \times 2.82 \times 2.285 = 6.4437k_1$$

Where  $k_1$  was the gain for the first-order filter.

### 5.3.1.3 Implementation

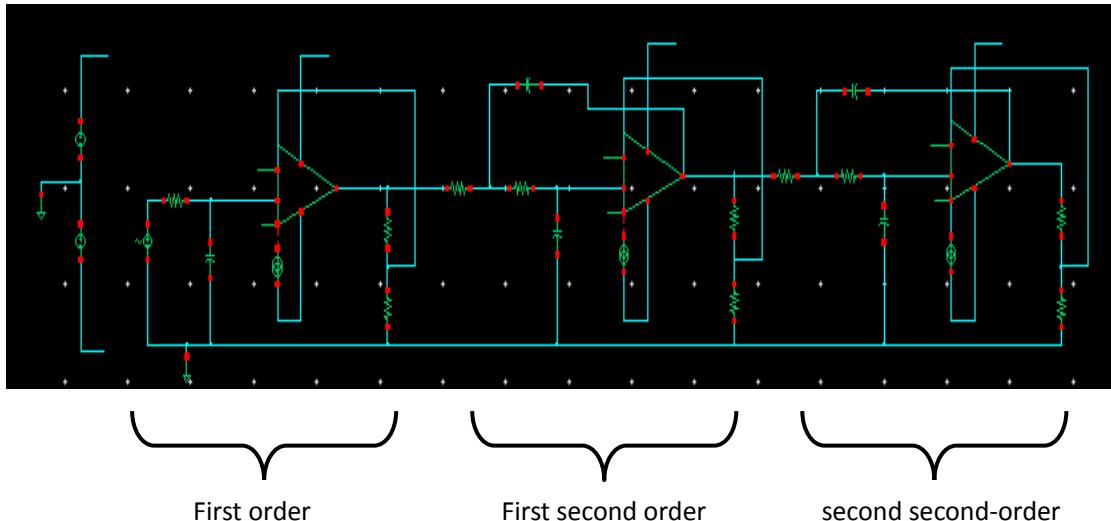


Fig 5.17 Chebyshev low-pass filter

The circuit shown above was the Chebyshev low-pass filter, as described in the calculation in the last section.

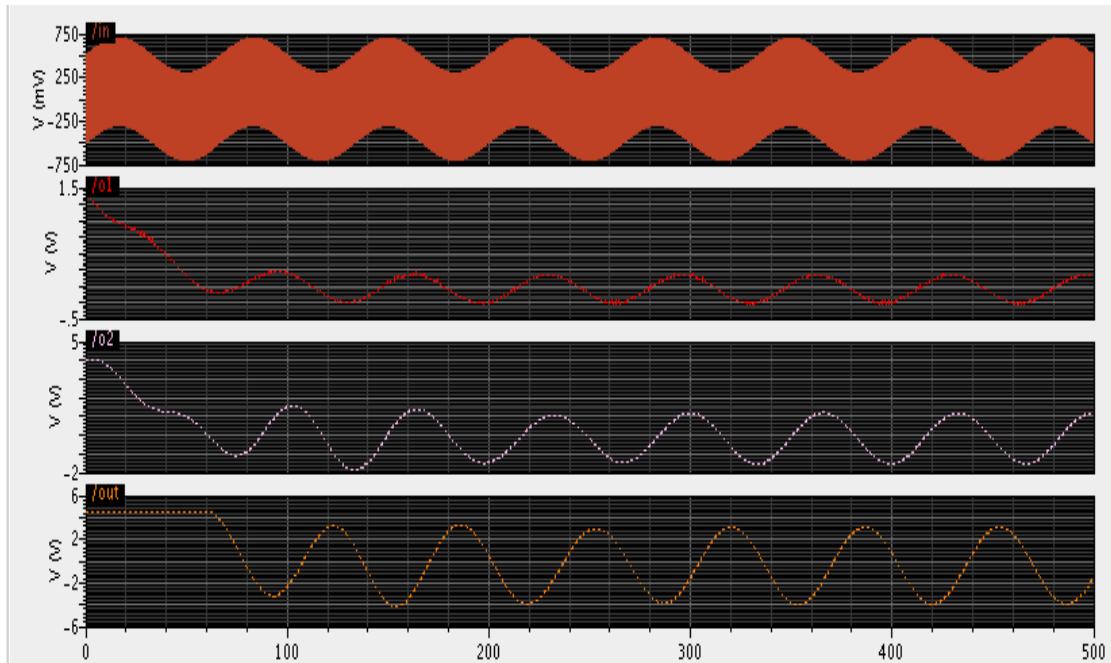


Fig 5.18 Transient response of Chebyshev low-pass filter

Figure 5.18 was the transient simulation of the Chebyshev low-pass filter. Here, the input signal (the top wave) contained two frequency parts. The bottom three windows show the output waves of different orders. Basically, the filter was able to output the low frequency part only. However, the amplitude of different orders were different and controlled by the gain of the filter. Also, the phase was shifted for different orders.

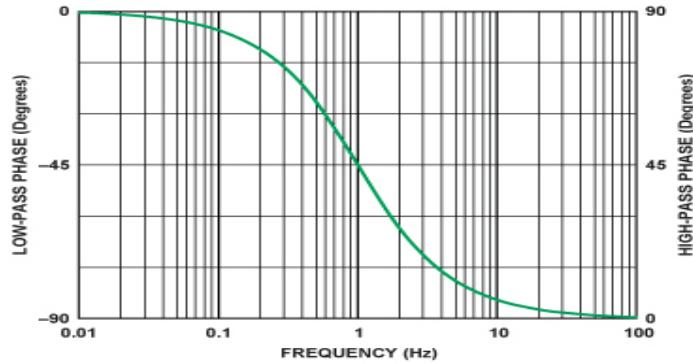


Fig 5.19 Phase response for first order low-pass filter

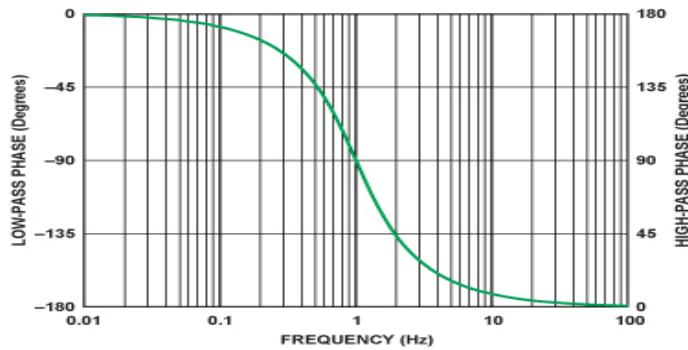


Fig 5.20 Phase response for second-order low-pass filter

(Reference:

[http://www.analog.com/library/analogdialogue/archives/43-09/active\\_filters.html](http://www.analog.com/library/analogdialogue/archives/43-09/active_filters.html)

Associated with the diagrams shown above, for the first-order low-pass case, the transfer function has a phase shift given by:

$$\varphi(\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_0}\right)$$

On the other hand, the equation for the second-order was,

$$\varphi(\omega) = -\tan^{-1}\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_0} + \sqrt{4 - \alpha^2}\right)\right] - \tan^{-1}\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_0} - \sqrt{4 - \alpha^2}\right)\right]$$

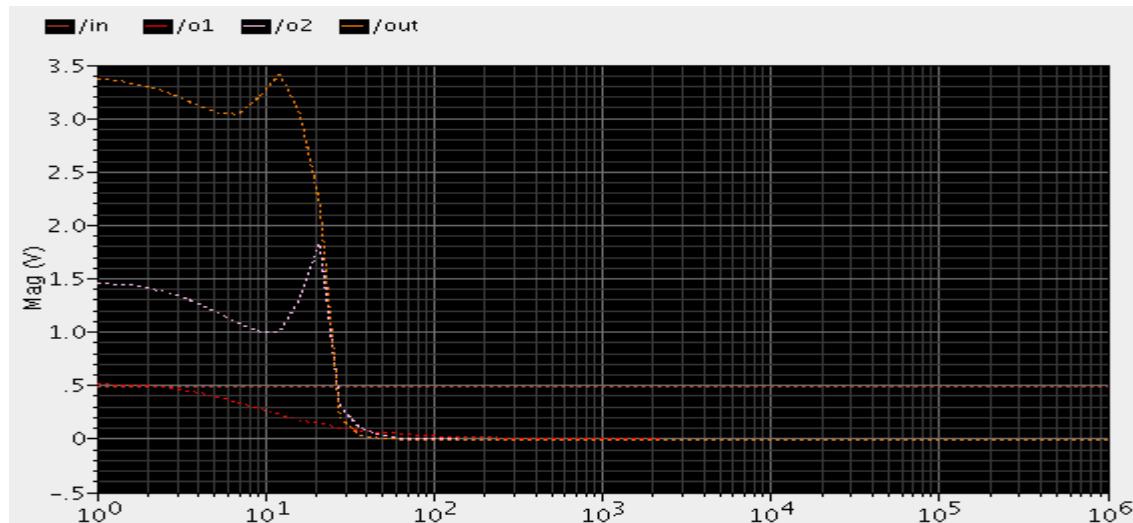


Fig 5.21 Frequency response of Chebyshev low-pass filter

Figure 5.21 was the frequency response of the filter design. The input remained the same magnitude (0.5 volts) in the frequency domain. The outputs started being suppressed at 20Hz and reduced to zero at about 40Hz, which matched the calculation. Here, the ratio of the first-order was close as the second resistor had a large value in order to protect the current from distortion.

## 5.4 Phase shift circuit

As discussed in sections 3.1.2 and 5.3.1.3, the filter can be implemented as a phase shifter circuit. In order to avoid the frequency response, the all-pass filter can be used by setting the ratio of resistors to one.

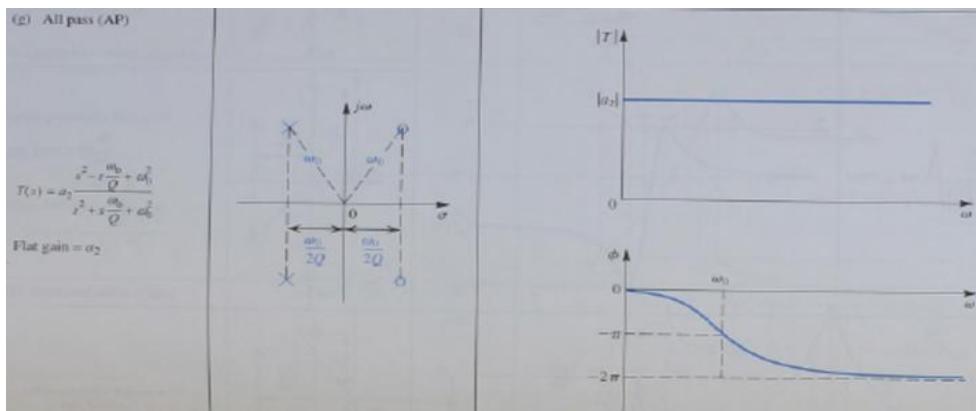


Fig 5.22 All-pass filter

(Reference: *Microelectronics Circuits, 5th Edition, page 874*)

As the diagram shows, when the centre frequency is equal to the frequency of the input signal, 90-degree shifting can be achieved.

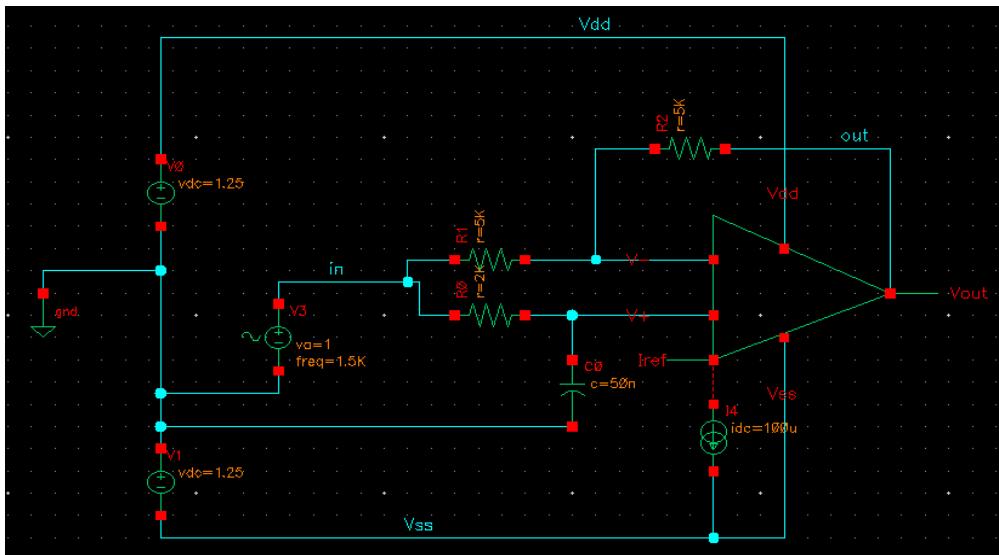


Fig 5.23 Circuit of the all-pass filter

The diagram shown above was the circuit for the all-pass filter with gain equalled to one by setting the ratio of the resistor to one. The phase shifting was controlled by the resistor and capacitor. Refer to the circuit,

$$R = 2 \text{ k}\Omega \quad C = 50\text{nF}$$

Therefore the centre frequency was,

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 2 \times 10^3 \times 50 \times 10^{-9}} = 1.59 \text{ kHz}$$

Here, the input frequency was 1.5kHz, which was near to the centre frequency.

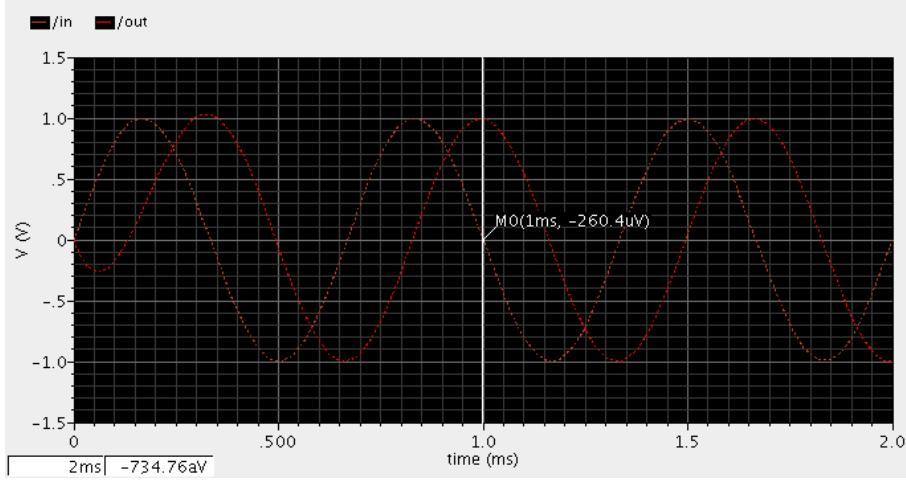


Fig 5.24 Phase simulation of the all-pass filter

As the transient response of the all-pass filter showed, the output had the same amplitude as the input signal, which indicated the gain of the filter was one. However, the amplitude of the output was initially greater than one in the first period. Then it settled down to one after the second period of sinusoid wave. The reason for debounce could be a ripple of the filter.

The phase can be tested by adding a vertical line as shown by the white marker. Ideally, when the amplitude of the input signal equals zero, the output should reach the maximum amplitude. Associated with the simulation, the amplitude of the output was about one. In order to increase the accuracy, the resistor should be recalculated,

$$R = \frac{1}{2\pi Cf_c} = \frac{1}{2\pi \times 50 \times 10^{-9} \times 1.5 \times 10^3} = 2,122.066\Omega$$

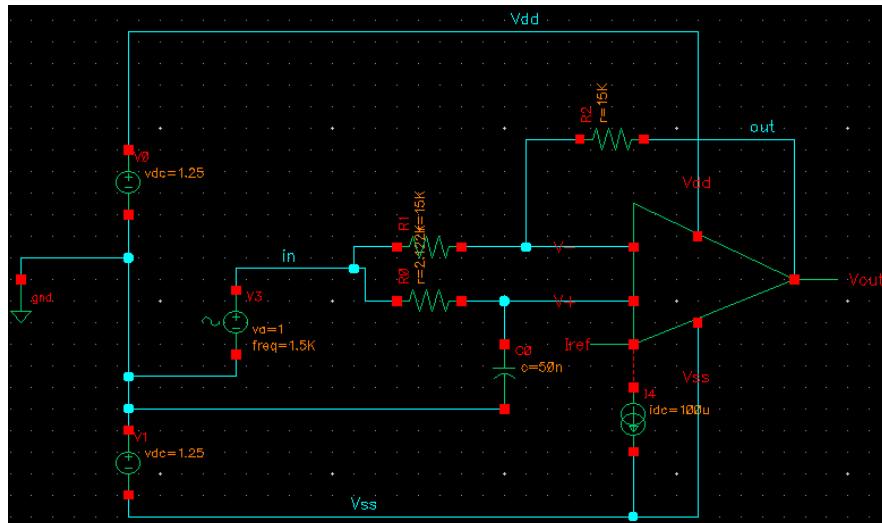


Fig 5.25 Phase shifter circuit 2

Compared to the previous circuit, the resistor was changed based on the calculation.

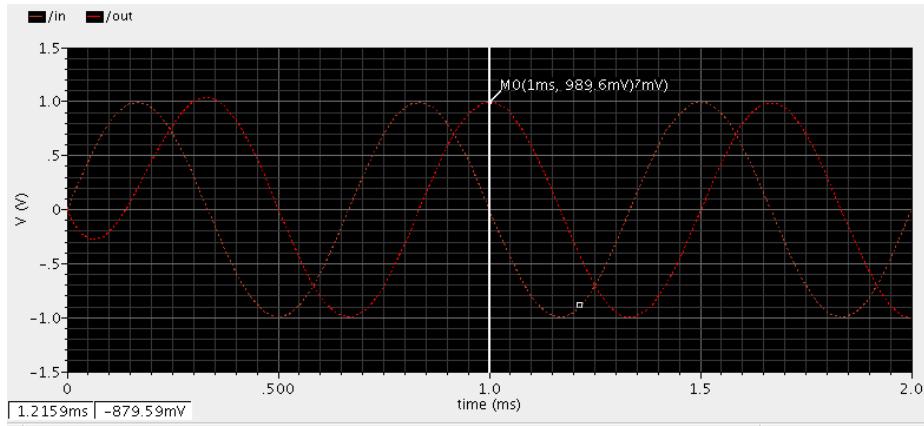


Fig 5.26 Phase simulation for phase shifter 2

Refer the marker shown on the diagram: when the input is equal to zero, the output is located in the centre of one period of the sinusoid wave. Hence, by changing the value of the resistor and capacitor, a more accurate phase shifting can be achieved. However, as  $\pi$  is an infinite fraction, there always had the error for phase shifter dependent on the tolerance of the specification. Associated with the signal amplitude and phase estimation, especially for the phase detection, the phase error had essentially the same effect for the result. However, based on the theoretical consequence, the output of the phase estimation was a DC voltage output dependent on the phase error, a stable offset could exist. Therefore, a disadvantage of using an all-pass filter as a phase shifter is that it is difficult to control the accuracy. Considering the industry cost, it was expensive to fabricate a highly accurate resistor.

## 5.5 Amplitude estimation

The amplitude estimation was designed based on the theoretical discussion in section 4.3,

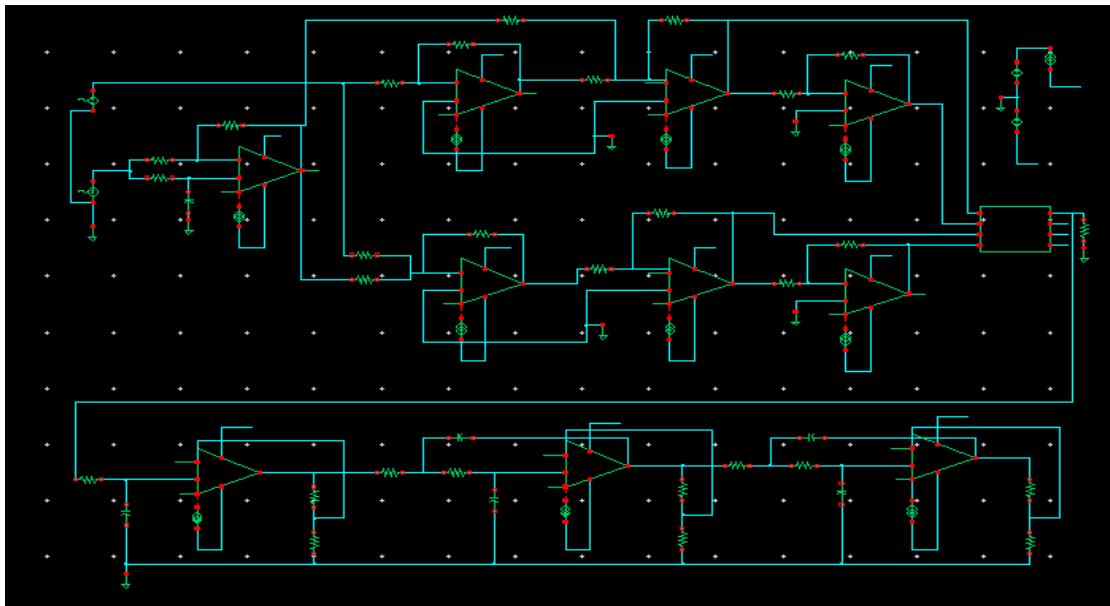


Fig 5.27 Amplitude estimation

In reference to the circuit shown above, two inputs were generated by the sinusoid wave voltage source with 1.5kHz frequency. Here, input 1 was regarded as the reference signal and input 2 became the target signal.

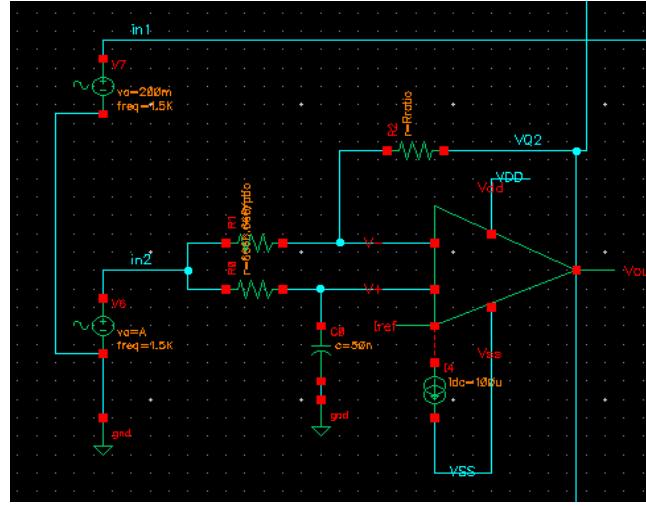


Fig 5.28 Input of amplitude estimation

Figure 5.28 was the inputs from the circuit shown in figure 5.27. The amplitude of input 1 or the reference signal was set to 200mV. Also, the block was the Gilbert cell based analogue multiplier,

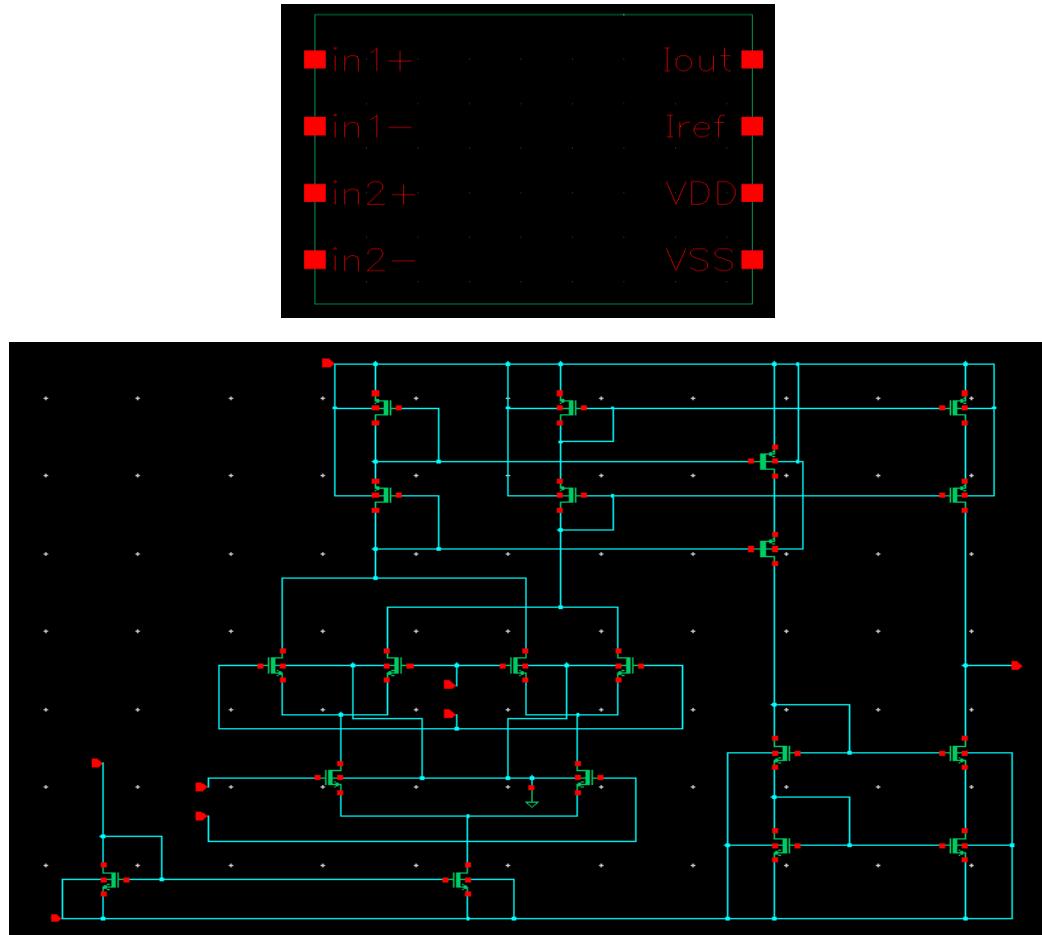


Fig 5.29 Block diagram of analogue multiplier

As the Gilbert cell required differential inputs, associated with the circuit shown in figure 5.27, an inverting amplifier was implemented to provide the opposite of the inputs. Also, a resistor was used to proportional control the output missed signal.

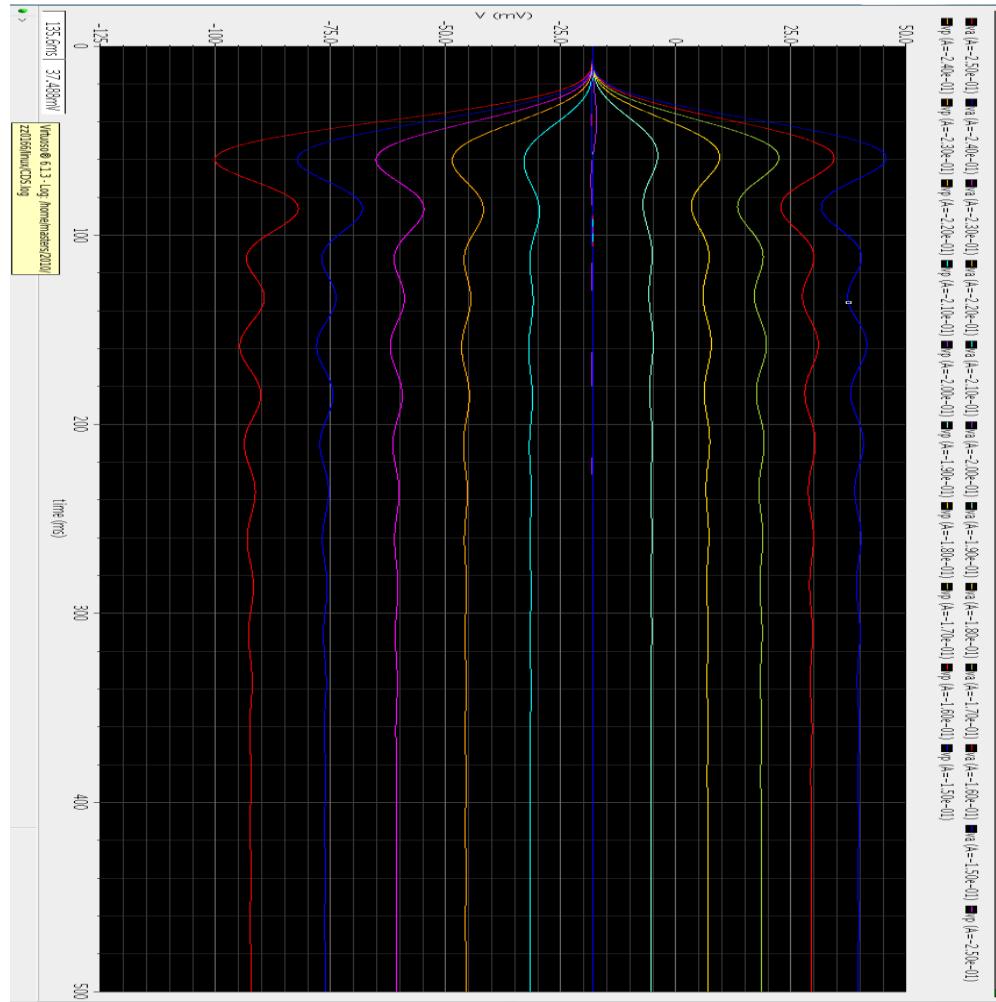


Fig 5.30 Simulation for amplitude estimation sweeping amplitude

Figure 5.30 is the simulation for amplitude estimation by sweeping the amplitude of the target signal from -150 to -250mV.

Table 3 Result for amplitude estimation

A1 (mV)	A2 (mV)	k=A2/A1	output (mV)	desired	lpfgain=6.6	offset
200	150	0.75	39.625	8.75	57.75	18.125
200	160	0.8	29.392	7.2	47.52	18.128
200	170	0.85	18.498	5.55	36.63	18.132
200	180	0.9	6.8637	3.8	25.08	18.2163
200	190	0.95	-5.3519	1.95	12.87	18.2219
200	200	1	-18.143	0	0	18.143
200	210	1.05	-31.683	-2.05	-13.53	18.153
200	220	1.1	-45.689	-4.2	-27.72	17.969
200	230	1.15	-60.718	-6.45	-42.57	18.148
200	240	1.2	-76.229	-8.8	-58.08	18.149
200	250	1.25	-92.399	-11.25	-74.25	18.149

The table shown above was the result of the amplitude estimation. The first two columns on the left were the amplitude of inputs; one of them was a reference signal remaining at 200mV, another sweeps from 150 to 250 in antiphase. The third column indicates the ratio of the amplitudes. The fourth column was the outputs captured from figure 5.30. The remainder of the data was then calculated. The fifth column was desired mixed output based on the mathematic formula,

$$V_a = \frac{A^2}{2} (1 - k^2)$$

Furthermore, the seventh column presented the desired mixed signal multiplied by the low-pass filter gain. The last column compared the desired output with the detected simulation; the offset was stable and about 18.1mV. Meanwhile, when the amplitude ratio was one, the output for the estimation was about -18.1mV. Hence, the amplitude estimation had 18.1mV offset. There are two possibilities for the offset. One could be the accuracy of the phase shifter, because the parameter  $\pi$  was infinite. Another reason could be the low-pass filter, as it had a ripple in passband.

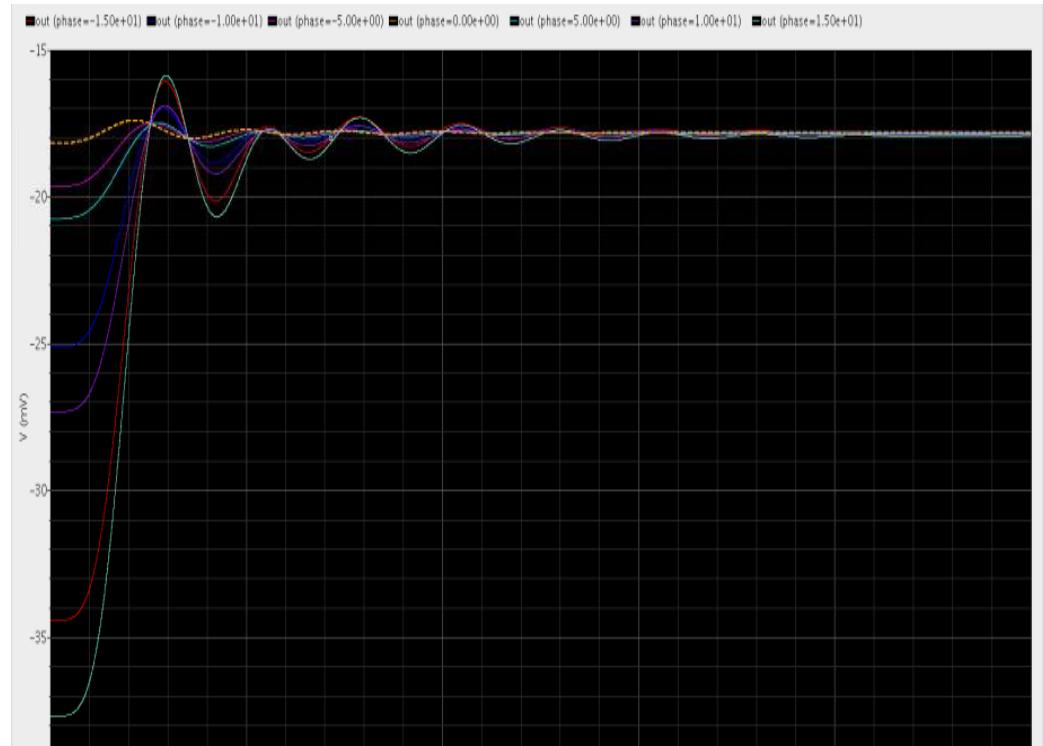


Fig 5.31 Simulation for amplitude estimation sweeping phase

Similarly, associated with the simulation shown in figure 5.31, the amplitude estimation was tested by sweeping the phase from -15 to 15 degrees. As shown in the diagram, the outputs were eventually matched. It indicated that the amplitude estimation was independent to the phase errors. However, as shown by the dashed line in figure 5.31, the bounce was smallest, or it settled down faster. Therefore, it proved that zero degree phase difference helped the amplitude estimation reached the maximum accuracy.

## 5.6 Phase estimation

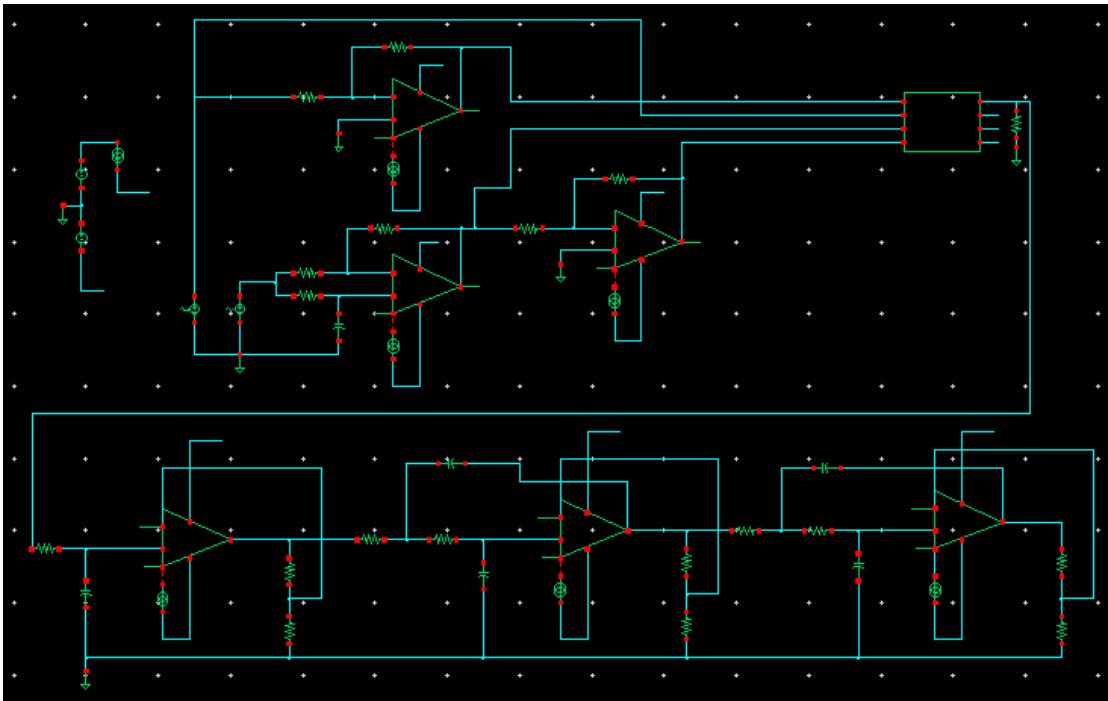


Fig 5.32 Phase estimation

The circuit shown above was the circuit for phase estimation. Compared to amplitude estimation, it removed the sum and difference circuit. Also, the reference signal was connected to the phase shifter instead of the target signal based on the calculation.

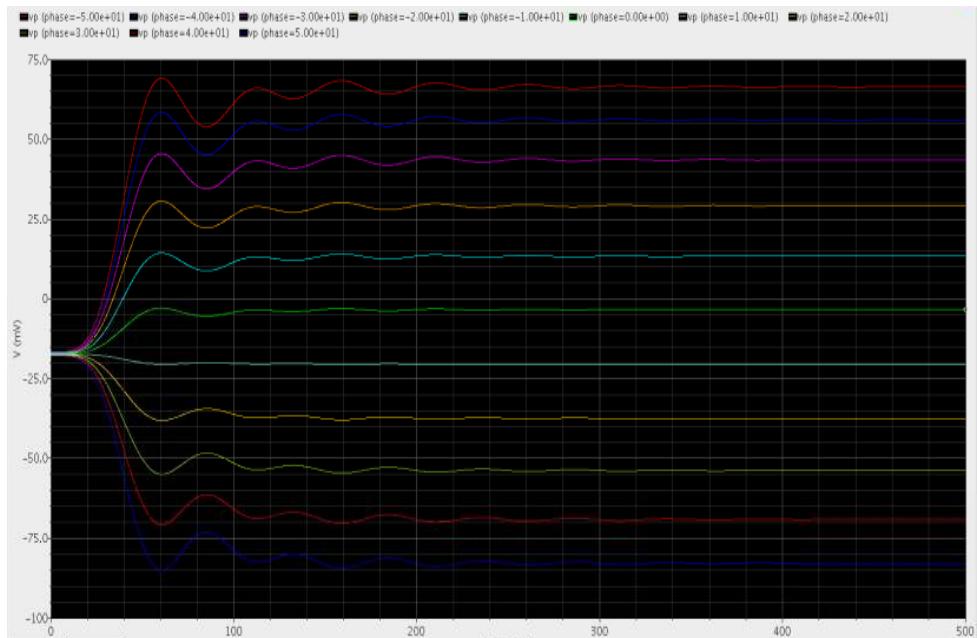


Fig 5.33 Simulation for phase estimation sweeping phase

Figure 5.33 is the simulation for phase estimation by sweeping the phase difference between -50 to 50 degrees.

Table 4 Result for phase estimation

phase	output	desired mix	desired output	offset
50	83.011	15.32088886	101.1178665	18.106866
40	66.733	12.85575219	84.84796448	18.114964
30	47.876	10	66	18.124
20	27.015	6.840402867	45.14665892	18.131659
10	4.7827	3.472963553	22.92155945	18.138859
0	-18.145	0	0	18.145
-10	-41.071	-3.47296355	-22.92155945	18.149441
-20	-63.298	-6.84040287	-45.14665892	18.151341
-30	-84.152	-10	-66	18.152
-40	-103	-12.8557522	-84.84796448	18.152036
-50	-119.27	-15.3208889	-101.1178665	18.152134

Here, the first column lists the sweeping phase with the captured output from phase estimation circuit shown in figure 5.32. The third column provides the desired mix signal based on the calculation,

$$V_p = \frac{kA^2}{2} \sin\varphi$$

Also, the fourth column is the desired output from the phase estimation obtained by multiplying by the gain of the low-pass filter. Again, comparing the actual output with the desired output, the offset was about 18.1mV. The value was same as the offset of the amplitude estimation.

## 5.7 Signal amplitude and phase control system

The control system was designed based on the amplitude and phase estimation discussed in the previous section. There were two potential options: one was to implement a complex circuit as discussed in section 3.2. The other was that digital signal processing could be used. The digital processing was acceptable as the output of estimations was unchanged by DC voltage, and a low sampling frequency would not affect or miss any data if the DC signal remained the same value.

There were different types of language that could be used to process the signal, like C, Assembly or MATLAB. In order to process the signal in same software instead of storing the data for processing, Verilog-A was used. It was supported by Cadence. In fact, there was another option for Cadence to implement the correction block by using the VCVS (voltage controlled voltage source). The errors could be fixed by defining coefficients of polynomials. In mathematics, a Taylor series is a representation of a function as an infinite sum of terms that are calculated from the values of the function's derivatives at a single point.

$$\begin{aligned}\sin x &= x - \frac{x^3}{3!} + \frac{x^5}{5!} - \frac{x^7}{7!} + \dots \\ &= \sum_{n=0}^{\infty} \frac{(-1)^n x^{2n+1}}{(2n+1)!}, \\ \cos x &= 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \frac{x^6}{6!} + \dots \\ &= \sum_{n=0}^{\infty} \frac{(-1)^n x^{2n}}{(2n)!}.\end{aligned}$$

The formula shown above is an example for how to use polynomials to represent trigonometric functions. However, this method is limited to polynomial dimensions. For Cadence, it just supported Two-Dimensional Functions. Hence, for the arcsin() function, it was not accurate to use the Taylor series.

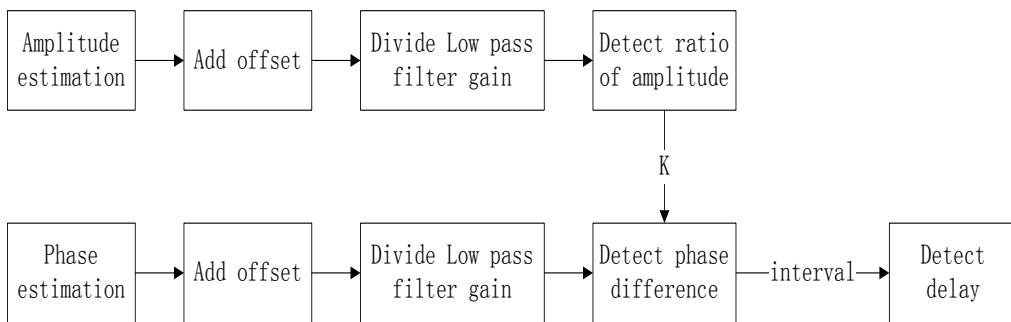


Fig 5.34 Block diagram of correction

Figure 5.34 shows a block diagram of corrections based on the performance of amplitude and phase estimations. The detected voltage from estimations would drive to the correction control block and follow the process shown in figure 5.34.

The common steps of the correction were adding the offset, which was 18.1mV, and dividing the gain of the low-pass filter. Then for the amplitude correction, the ratio of the amplitude would be detected. Hence the desired amplitude can be obtained by using the target signal divided by the ratio. For the phase correction, the ratio detected previously should be used to calculate the phase difference. By comparing the interval of one period of reference signal, a delay can be detected to correct the phase error.

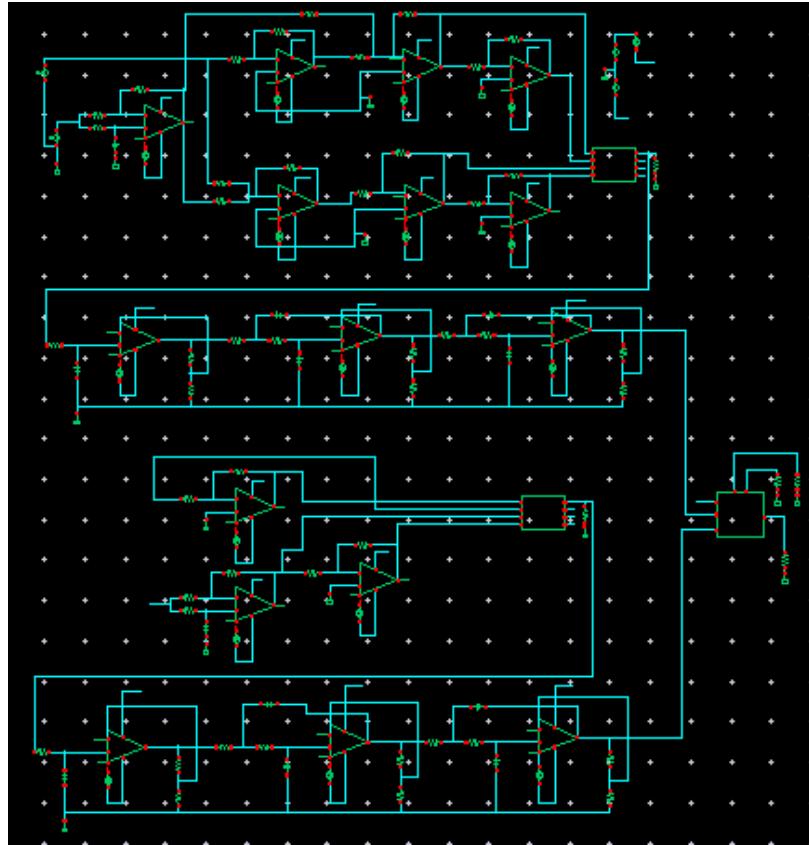


Fig 5.35 Correction circuit

To correct the amplitude and phase error, a correction block was added,

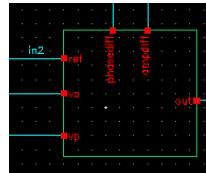


Fig 5.36 Basic correction

Associated with figure 5.36, the amplitude and phase estimation were connected as the input of the correction block. Another input was the target signal. The Verilog-A code can be found in appendix B. An important syntax was,

`absdelay( expr,time_delay[,max_delay] )`

where

*expr* is the expression to be delayed

*time\_delay* is a nonnegative expression that defines how much *expr* is to be delayed

If the optional *max\_delay* is specified, the value of *time\_delay* can change during a simulation, as long as it remains positive and less than *max\_delay*. If *max\_delay* is not specified, any changes to *time\_delay* are ignored. If *max\_delay* is specified and changed, any changes are ignored and the simulator will continue to use the initial value.

Referring to the description above, the `max_delay` is required to be specified in order to support the dynamic parameter. It was necessary to provide a dynamic declaration, as the simulation for amplitude or phase estimation was unstable at initial stage. The DC output was eventually settled down at about 300mS, hence it was dynamic.

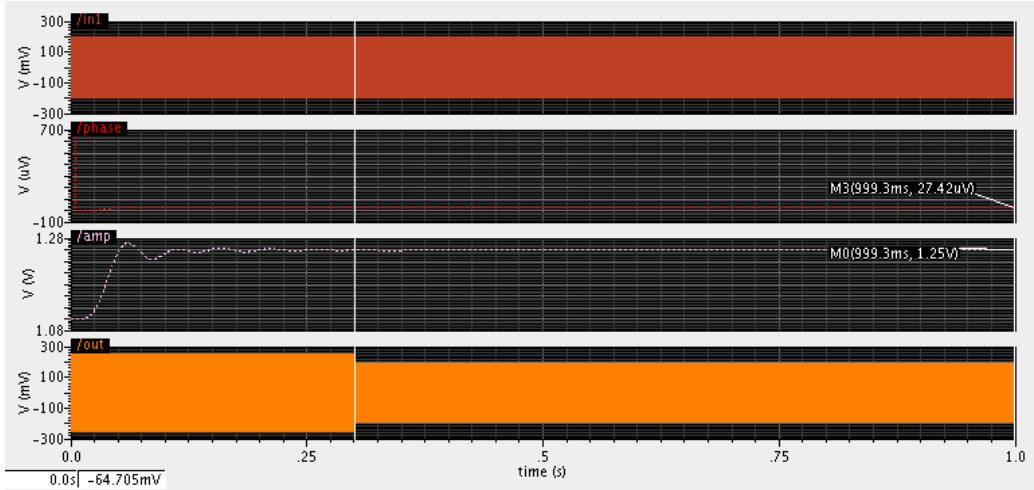


Fig 5.37 Simulation of basic correction

Figure 5.37 is the transient simulation for basic correction. The top window was the reference signal, and the second and third was the detected ratio and delay to correct the target signal. For this simulation,

$$A = 250\text{mV} \text{ and } \text{phase} = 15^\circ$$

Hence,

$$k = \frac{250}{200} = 1.25$$

And, the desired delay was,

$$\text{delay} = \frac{1}{f_{\text{in}}} \times \frac{\text{phase}}{360} = \frac{1}{1500} \times \frac{15}{360} = 27.7 \mu\text{s}$$

Regarding the simulation, the detected amplitude ratio was 1.2501 and the delay was 27.424uS. The result was very close to the calculation.

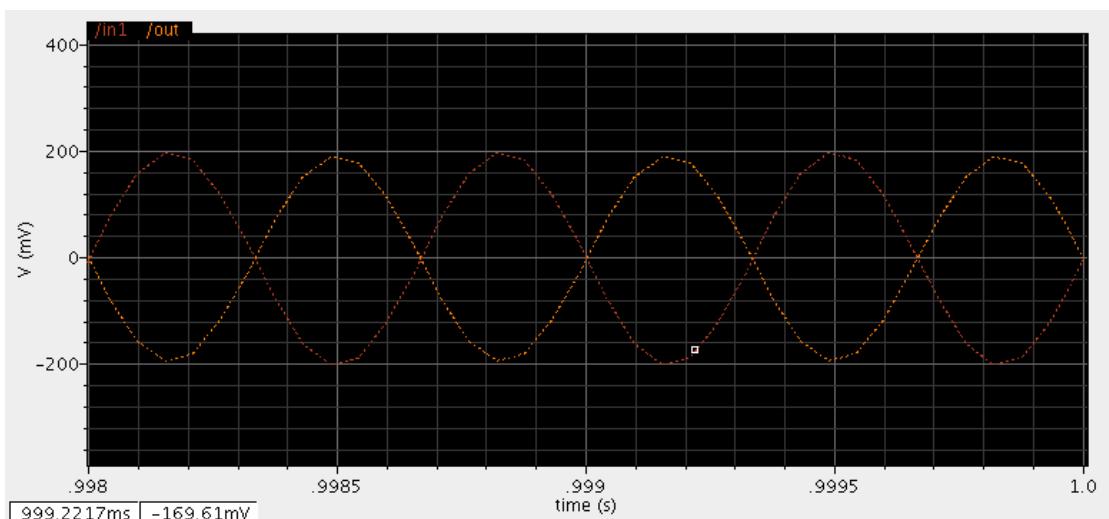


Fig 5.38 Comparing the input and output of basic correction

As shown in the figure above, the corrected signal (called out in simulation) was eventually able to track the reference signal in antiphase.

Another marker on figure 5.38 indicated the output signal changed the amplitude at 300mS. It was controlled by Verilog-A,

```
@(timer(300m)) begin
```

At 300mS, the block started to correct the target signal. The reason was, refer the estimation simulation in figure 5.30 and 5.33, it took about 300mS to settle down the output of the estimations to eventually become a DC signal. Furthermore, the timing parameter was flexible depending on how fast the estimation can be achieved.

However, there were still some tiny errors. In order to accurately correct the target signal, the corrected signal should feedback to the estimation circuit.

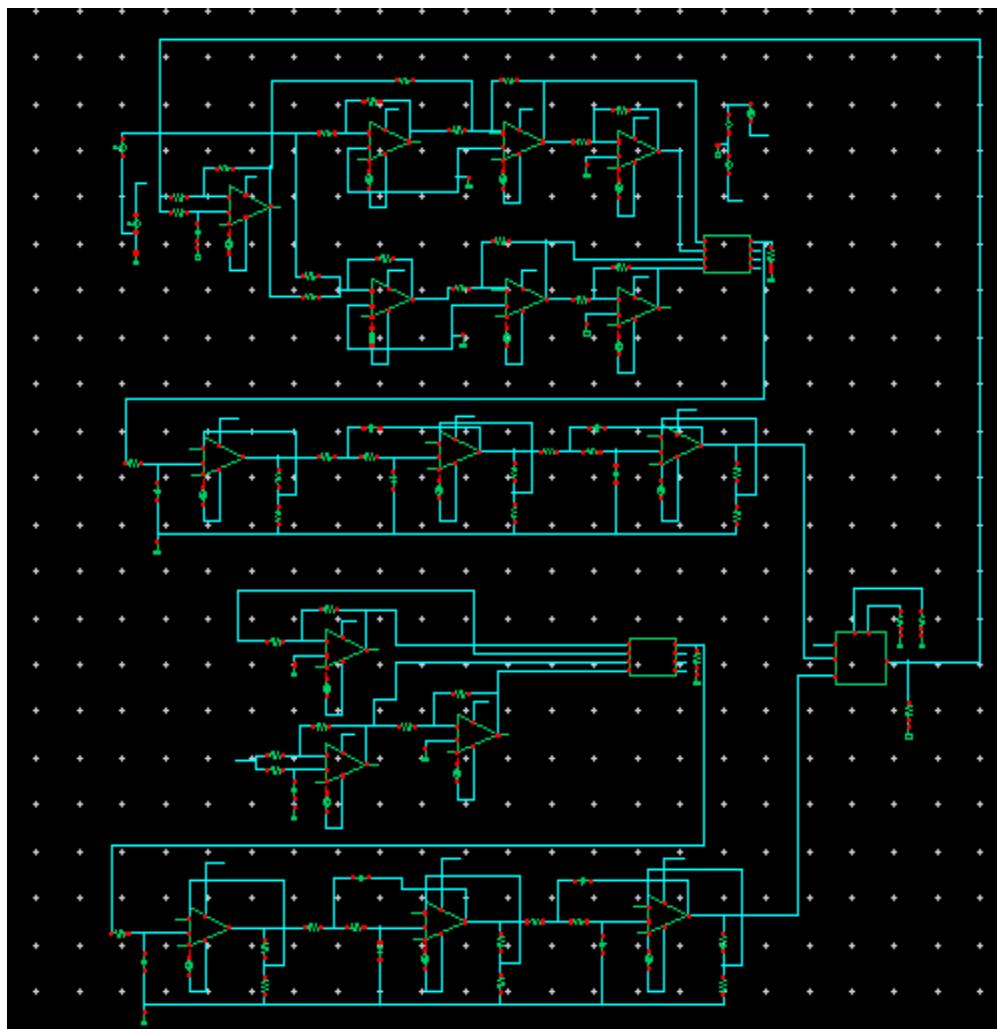


Fig 5.39 Basic feedback control

The circuit shown above was the basic feedback controlling the amplitude and phase. Compared to the correction circuit shown in figure 5.35, a feedback path was connected to the target signal instead of a sinusoid wave voltage source. Similar to

the correction, the output of the correction block would output the target signal until 300mS.

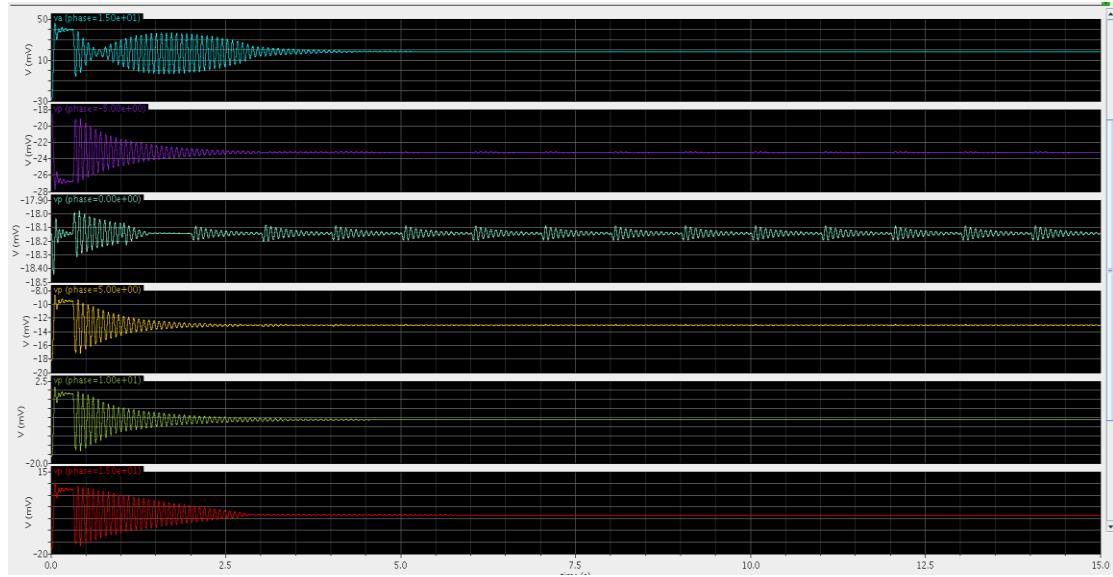


Fig 5.40 Amplitude ratio of basic feedback control

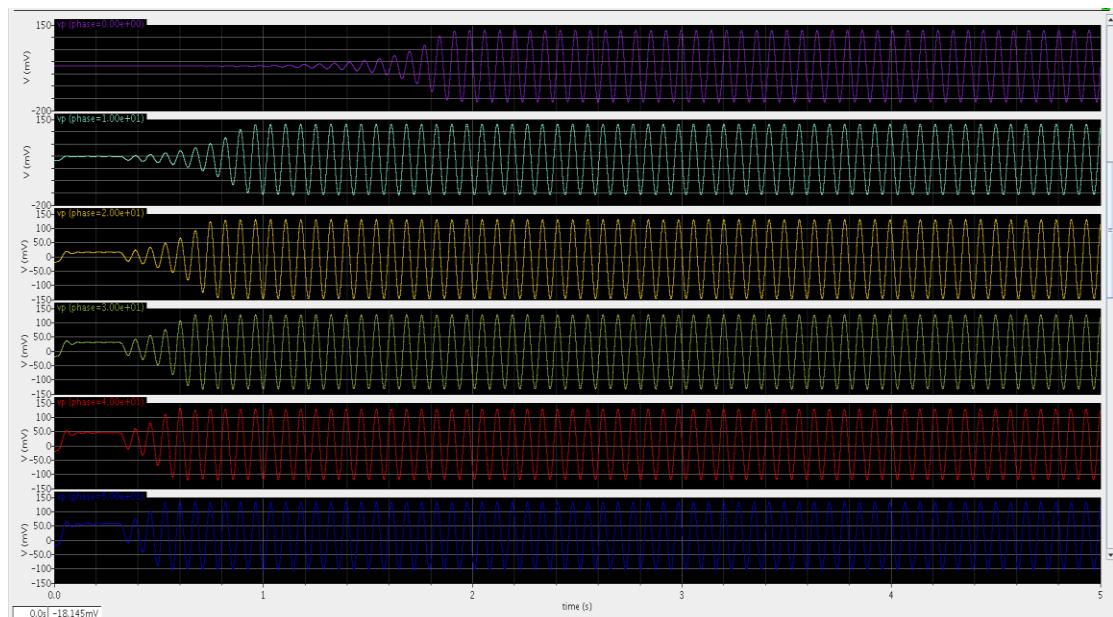


Fig 5.41 Delay of basic feedback control

As the simulation results show, the corrected amplitude ratio and phase delay kept bouncing after 300mS. However, the calculated amplitude ratio and delay were correct at 300mS. The error occurred because the detected amplitude and phase error was between the reference and target signal, at 300mS; the target signal would be corrected and feedback to the estimation circuit. Then, the estimation circuit would detect an error free signal, which caused the correction block to feedback the target signal back again. Hence, the signal bounced between the reference and target signal forever. To fix this error, it was necessary to store the corrected signal in order to become new target signal for next the correction. The Verilog code can be found in appendix C. A temporary signal was obtained to be stored as the target signal for next correction.

To optimise the code, two variables were used instead of storing the whole signal. Therefore, less data is required to be stored. Another advantage of this method is the amplitude ratio and phase difference can be predefined to provide an accurately controlled amplitude and phase toward the reference signal.

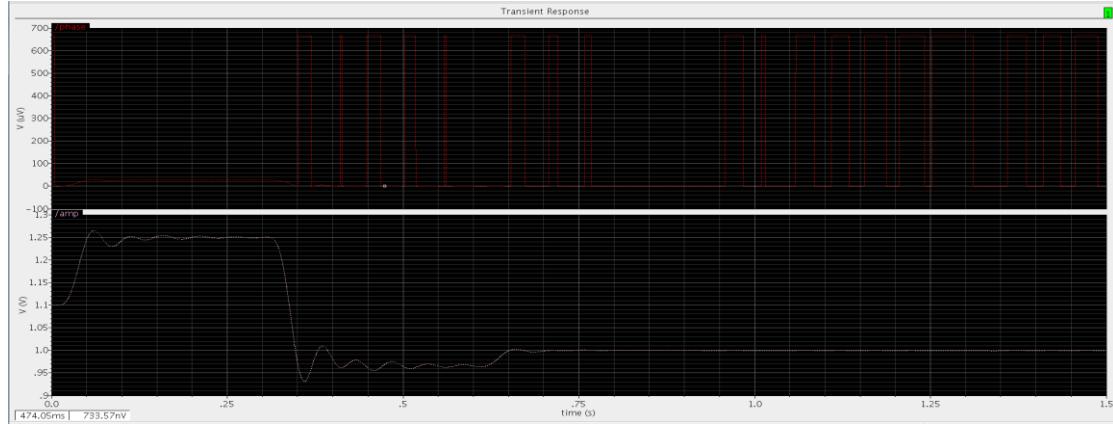


Fig 5.42 Simulation for advanced feedback control

Figure 5.42 indicates that the corrected signal was able to track the reference signal after 3 periods' correction. For instance, the amplitude ratio detected the ratio at about 1.25 in the first period with 300mS. Then, in the range of 300 to 600mS, the ratio was about 0.92 because of the offset of the first period. Eventually after 900mS, the ratio became one. On the other hand, the phase error was fixed within 600mS. However, it bounced between zero and 666uS, corresponding to zero and 360 degree. Hence the feedback was able to correct any amplitude or phase error within 3 periods of correction.

### 5.7.1 Butterworth filter implementation

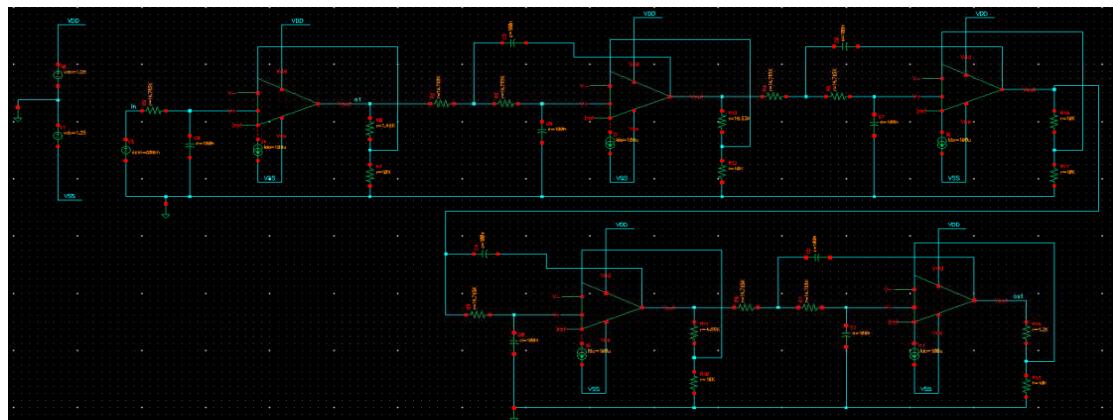


Fig 5.43 9-order Butterworth low-pass filter

The circuit was a 9-order Butterworth low-pass filter, with the design specification,

Table 5 Design specification of Butterworth low-pass filter

F <sub>p</sub>	F <sub>s</sub>	A <sub>max</sub>	A <sub>min</sub>
10 Hz	15 Hz	1.0 dB	25 dB

All the parameters were calculated based on the description listed in table 1.

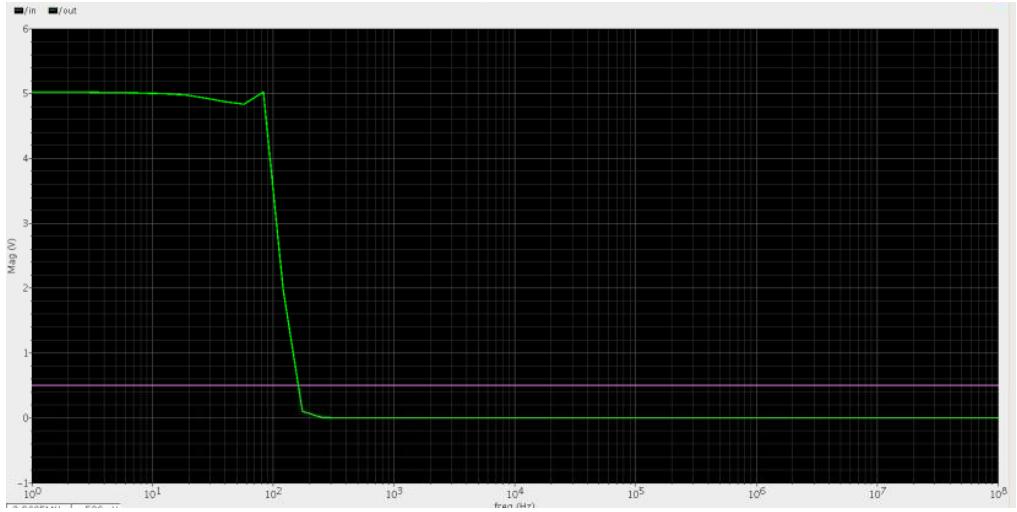


Fig 5.44 Simulation of the Butterworth low-pass filter

Referring to figure 5.44, the Butterworth low-pass filter (calculation discussed in appendix E) was able to remove any signal beyond 15Hz in the frequency domain. Compared to the Chebyshev type shown in figure 5.21, it proved a small ripple. However, it achieved more orders.



Fig 5.45 Amplitude estimation using the Butterworth low-pass filter

The simulation was obtained by replacing filter in circuit showed in figure 5.35.

Table 6 Result of amplitude estimation using Butterworth low-pass filter

A1	A2	output(mV)	ratio=A2/A1	desired mix	desired output	offset
200	180	7.921	0.9	3.8	38	30.079
200	190	-10.66	0.95	1.95	19.5	30.16
200	200	-30.2	1	0	0	30.2
200	210	-50.74	1.05	-2.05	-20.5	30.24
200	220	-72.4	1.1	-4.2	-42	30.4

Similar to the analysis for table 3, the stable offset was detected at about 30.2 mV. Compared to Chebyshev design, this type of filter provided faster transient response (about 100mS), but had a large offset. However, for digital correction, the stable offset can be predefined. Therefore, the Butterworth low-pass filter provided a faster operation for the system.

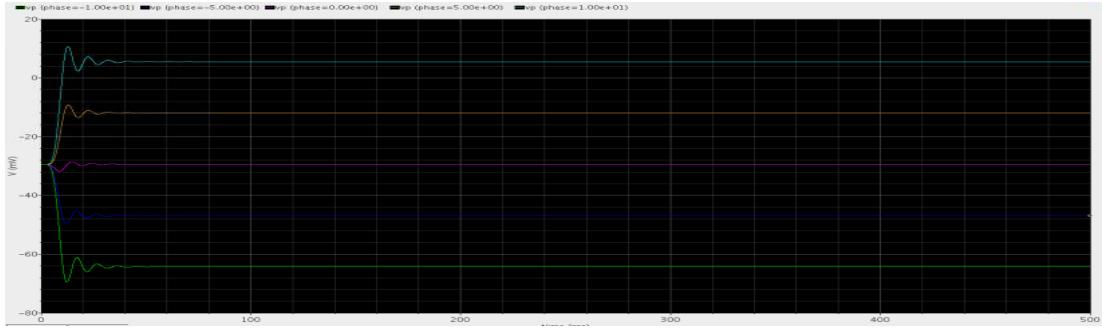


Fig 5.46 Phase estimation using Butterworth low-pass filter

Table 7 Result of phase estimation using Butterworth low-pass filter

phase	output(mV)	desired mix	desired output	offset
-10	-64.75	-3.47296355	-34.72963553	30.02036447
-5	-47.89	-1.74311485	-17.43114855	30.45885145
0	-30.1	0	0	30.1
5	-12.88	1.743114855	17.43114855	30.31114855
10	4.486	3.472963553	34.72963553	30.24363553

As shown in the calculation in table 7, it detected the same offset for phase estimation. However, there were errors because the accuracy of the phase shifter had a larger effect on phase estimation.

### 5.7.2 Increase input frequency

Digital communication was easy to implement, change and program. Hence, one purpose in designing an analogue circuit was to provide a high frequency environment that the digital sampling frequency cannot reach. Associated with the circuit, only amplitude and phase estimations required increasing the frequency. As the low-pass filter, sum and difference circuit, and phase shifter was designed based on the OPAMP. One issue for increasing frequency was to improve the OPAMP so that it was able to work for high frequency.

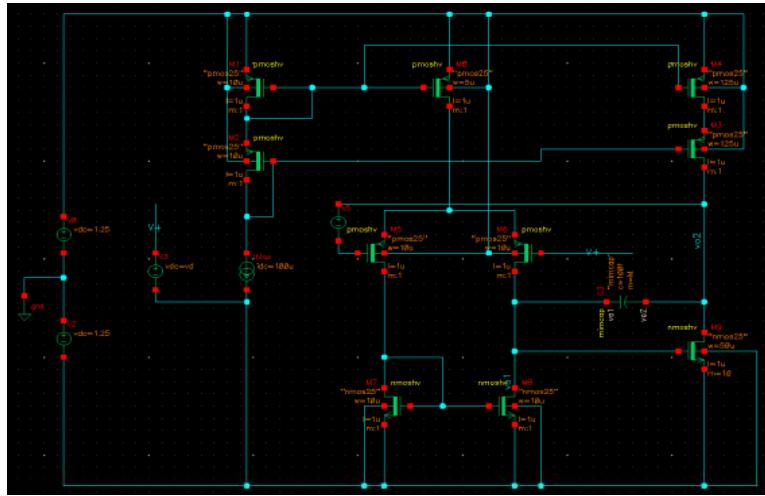


Fig 5.47 OPAMP for high frequency

Figure 5.47 illustrates an OPAMP that is able to perform an operation for high frequency. In order to extend the frequency range, the split poles should be decreased by decreasing the capacitance of the compensated capacitor. It will decrease the dominant pole in the frequency domain, which causes the stability to decrease. For industry consideration, the phase margin should not be less than 65 degrees. Meanwhile, as the frequency increases, the gain will drop. Hence, the gain should be increased. Associated with the circuit, a cascaded mirror was implemented for the second stage in order to increase the output impedance. However, the increased second gain would pull the dominant pole close to the first stage pole. Therefore, the stability was increased by decreasing the gain of the first stage. Here, the transconductance of first stage differential pair was decreased.

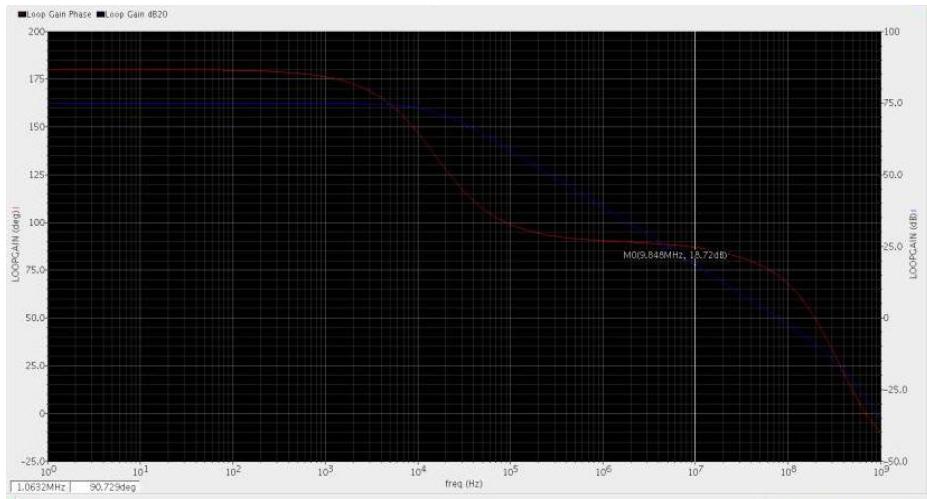
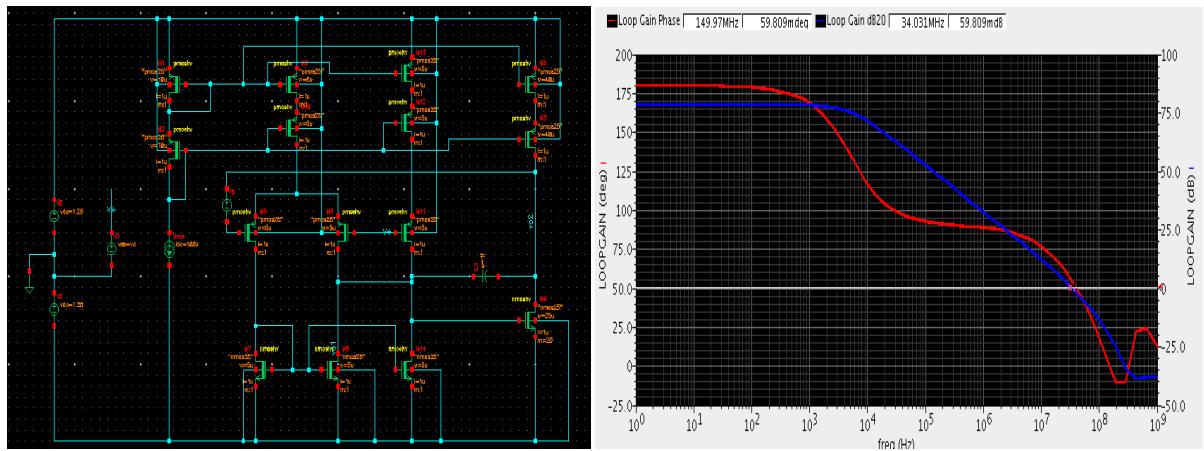
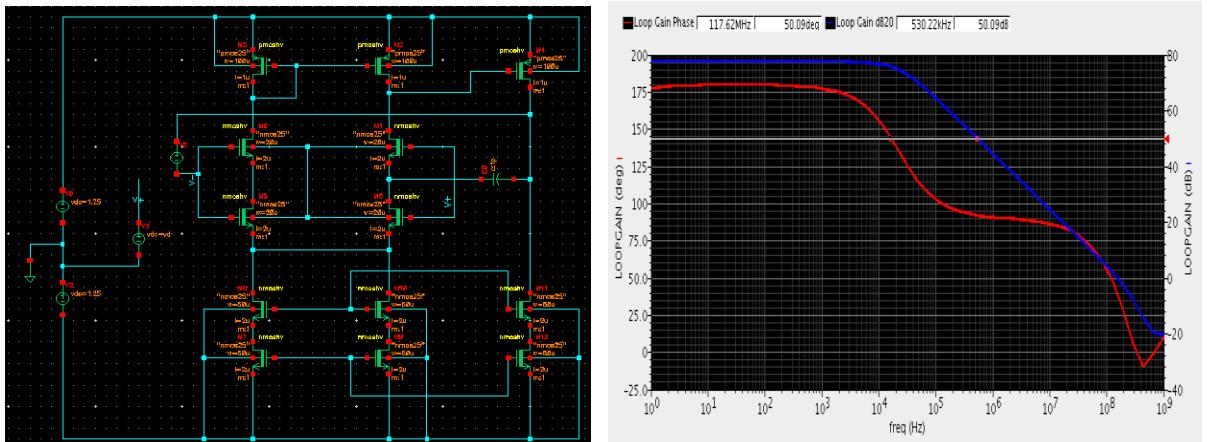


Fig 5.48 Frequency response of OPAMP

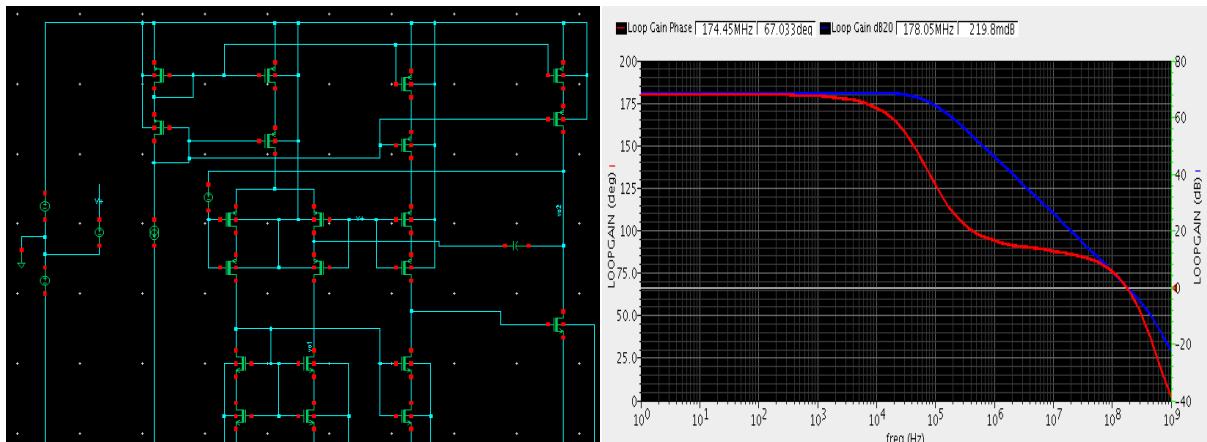
Figure 5.48 is a frequency simulation for the OPAMP shown in figure 5.47. As the marker shows, the gain remained a positive gain within 80MHz.



(A)



(B)



(C)

Fig 5.49 Different type of two-stage OPAMP

Figure 5.49 illustrates other structures of OPAMP. The top one showed in figure A, was cascaded the PMOS active load in terms of increasing the output resistance of stages, which increasing the 3dB point to about 6KHz. Figure B cascaded the first stage differential amplifier. It located the 3dB point at 35KHz. Finally, figure C cascaded the entire first stage included the active loads. This method achieved 3dB point at 55Khz. Hence, the method showed in figure C was chosen as OPAMP to increase the system working frequency.

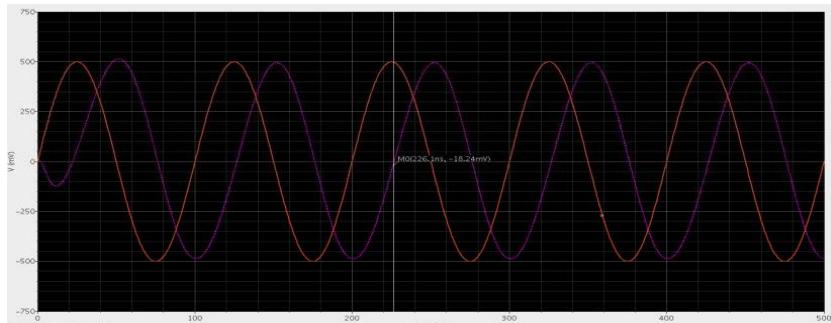


Fig 5.50 Phase shifter simulation

Figure 5.50 provided a simulation for 10MHz phase shifter. Associated with waves, when the input was zero, the output reached the maximum value, which means a 90-degree shifting was achieved for the sinusoid wave.

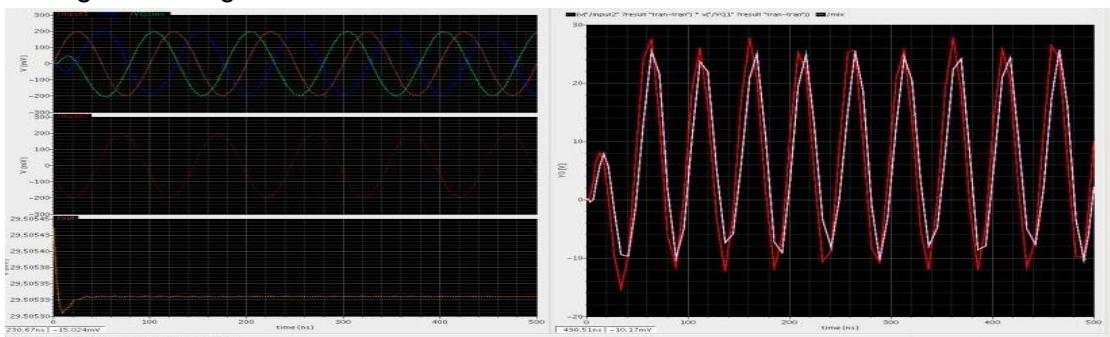


Fig 5.51 Simulation for amplitude estimation

Figure 5.51 shows a simulation for amplitude estimation. In the left window, the top diagram indicates a 90-degree shifting signal and its inverting signal in terms of driving the Gilbert cell. The right window indicates that the mixed signal was able to match the multiplication.

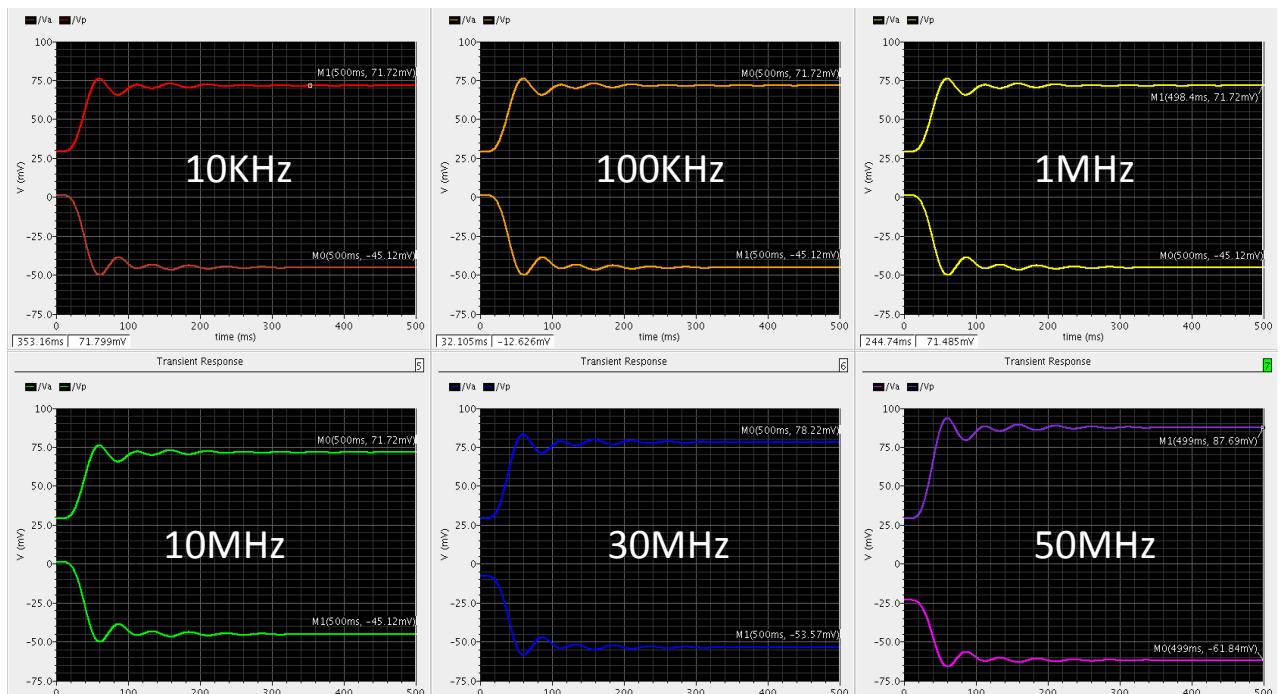


Fig 5.52 Estimations for different frequency

Figure 5.52 was the estimation outputs by sweeping input frequency. Here, the amplitude was 250mV and the phase error was 15 degree. Associated with the waves, the output matched the calculation, referring to table 3 and 4, while the frequency below 10MHz. As the frequency increased to 30MHz, the offset of estimations was larger. Further, as the frequency increased to 50MHz, the offset increased as well. Hence, the high frequency caused larger offsets. It was acceptable for digital correction, as the offset can be predefined. The limitation for the system was about 60MHz as the OPAMP cannot provide enough gain for high frequency.

### 5.7.3 PVT variation

The purpose of PVT variation was for industry considerations so that to ensure the system would work for different variations.

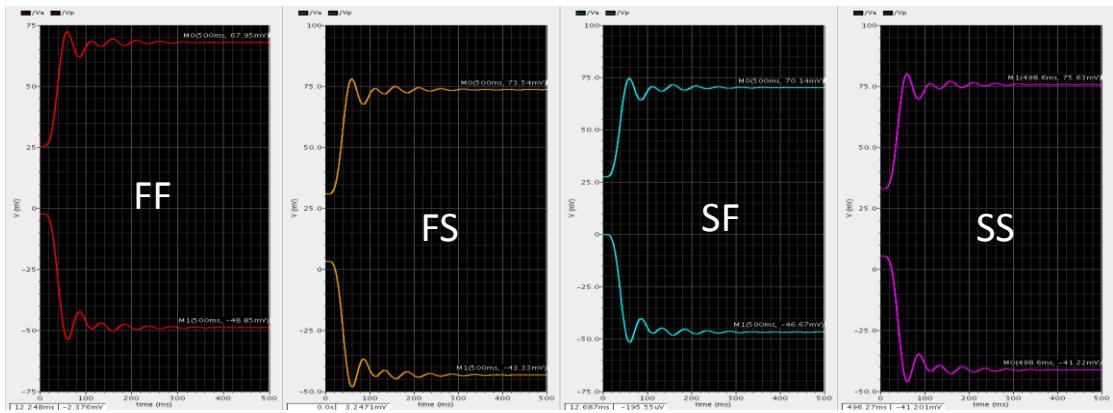


Fig 5.53 Process corner

Process corner was analysis for transistor speed. It included FF, FS, SF and SS processes. Where, F was fast and S was slow indicated the NOMS and POMS respectively. Refer to the results showed above, the slow devices caused larger offset for estimations.

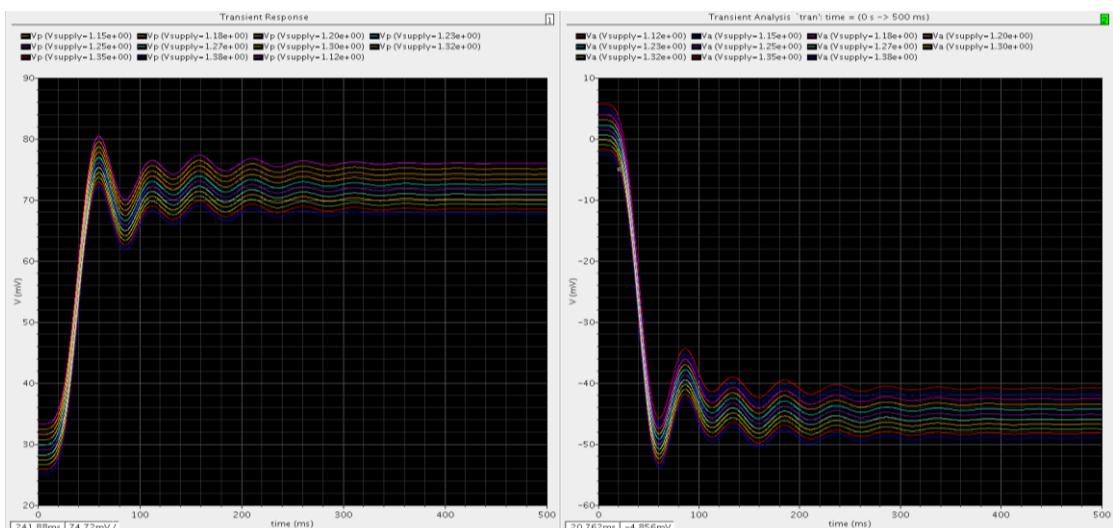


Fig 5.54 Voltage corner

Figure 5.54 sowed the voltage corner by sweeping the supply voltage from -10% to

10%. Associated with waves, the larger difference of supply voltage, either positive or negative, provided larger offsets.

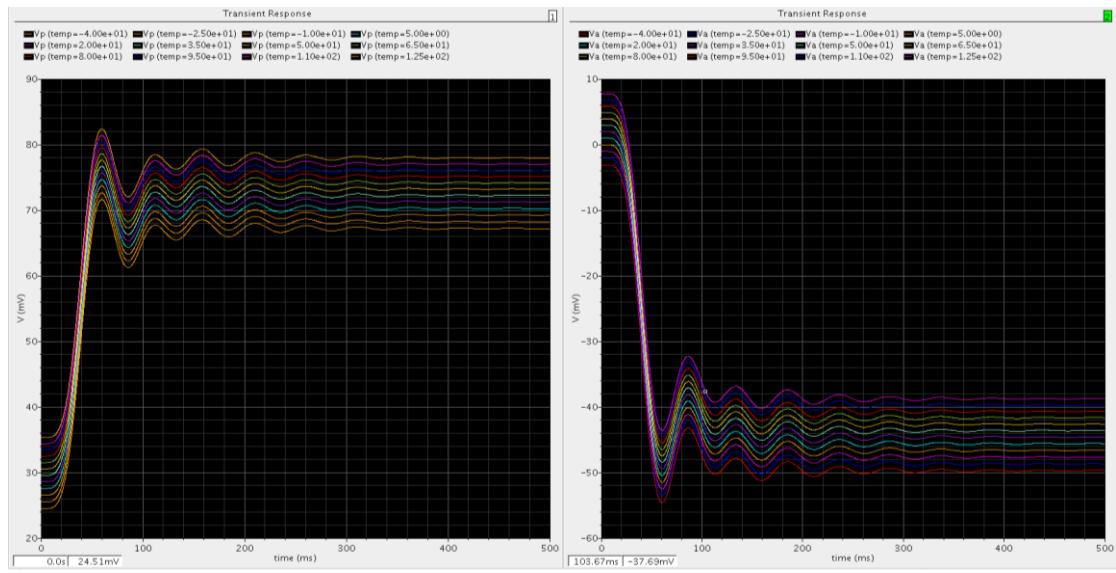


Fig 5.55 Temperature corner

Temperature corner sweep the temperature form  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . According the simulation, higher temperature caused larger offset. The reason was the high temperature increased the resistance of the transistors.

## 6 CRITICAL EVALUATION AND CONCLUSION

In this section, the critical evolutions were discussed corresponding to the objectives listed in section 2, which were all achieved within this project. Each objective was illustrated in the textbox following with analysis.

- Research and compare the different technologies of signal amplitude and phase comparison circuits in order to choose an optimised design that uses fewer components in a signal control system.

The project started with researching relevant technology for signal amplitude and phase comparison. The phase estimation was directly developed based on the mathematic consequence. In addition, it was difficult to directly detect amplitude error. A traditional method uses a peak value detector. However, considering the analogue signal was continuous, any phase shifting would cause error in amplitude estimation. Therefore, PLL could be used to lock the phase before detecting the peak value of amplitudes. There were two drawbacks in this method: one was the circuit was complicated to implement, and another was it could not detect the amplitude and phase errors simultaneously. As a result, a new technique was chosen, which used a phase comparison loop to detect the amplitude error. An obvious advantage of this method was that the amplitude estimation was independent from phase effects. Therefore, amplitude and phase estimations could be achieved at the same time.

- Study and understand the new approach of using phase comparison technique and implement a signal amplitude and phase estimation circuit.

The theoretical consequence was calculated in detail by referring to the trigonometric formulas. The issue for trigonometric consequence (section 4.4) was to distinguish the output into high and low frequency parts. By the implementation of a low-pass filter, only the low frequency part remained. Therefore, a signal estimation circuit would output DC signals representing the amplitude and phase error respectively. Therefore, refer to section 4, the analogue components were chosen to implement the estimation circuits based on the mathematic consequences.

Furthermore, in reference to the theoretical consequences, the estimation circuits were built. The circuit included an analogue multiplier, phase shifter, sum and difference circuit, and low-pass filter. As the operational amplifier should be used as basic elements for more circuits, a two-stage compensated differential amplifier was defined. The judgement was stability rather than high gain. Associated with the discussion in section 4.7, a compensated capacitor can be added in order to dominate the pole to provide stable output. The cascode amplifier was not implemented as it sacrificed stability to achieve high gain. Associated with section 5, an OPAMP was designed to achieve high stability by using Miller capacitor compensation so that the two poles of different stages split. The phase margin of the two stages OPAMP was

74 degrees with high gain. Compared to the conventional OPAMP, the compensated design was chosen for implementing the low-pass filter, phase shifter and sum difference circuits. Actually, phase shifter was implemented as all-pass filter by configure the centre frequency equal to the input frequency. As the DC gain of all-pass filter set to one, a 90-degree shifting was achieved. The accuracy of shifting was controlled by the resistor and capacitor. For a low frequency range in the estimation simulated for this objective, the phase shifter was able to output stable shifted signal.

For the multiplication, refer to discussion for different types of multiplier in section 4.5, the Gilbert cell provided high impedance, high speed, high linearity and low power supply requirement. Other types of multiplier were simulated and discussed in appendix D. Hence, the Gilbert cell was chosen as the structure for multiplication. Based on the simulation, the result of the Gilbert cell matched the calculation. However, a drawback of Gilbert cell was, it was not a single-ended output. This problem was solved by using either difference circuit or mirror the current to a single-ended node in order to drive a resistor. Also, the output of this method can be proportionally controlled by using different output resistance.

For the low-pass filter, a 5-order Chebyshev and 9-order Butterworth low-pass filter were implemented. The Chebyshev filter provided a lower offset (about 18mV), but longer time (about 300mS) to settle down. On the other hand, the Butterworth filter settled down faster (about 100mS) with a higher offset (about 30mV). For the filter, the narrower the pass-band, the faster the estimation can settle down. Associated with the feedback path, the Butterworth filter was better, because the offset can be defined as a constant and it was faster.

- Design, implement and test a feedback block.

The feedback path was built by a digital block writing in Verilog-A. The inputs of the correction block included target signal, amplitude and phase error detected from the estimation circuits. The amplitude error was fixed by dividing the calculated amplitude ratio, and the phase error was fixed by the delay function. The delay was determined from the detected phase angle compared to time interval for one period of reference signal. This method provided an accurate correction by calling the predefined functions in Verilog-A. Referring to the simulation showed in section 5.7, the target signal was able to track the reference signal within 3 to 4 periods. Associated with figure 5.42, the first period fixed the main error for amplitude and phase. Here, the length of period was determined by the speed of the estimation processing. By using the timer() function in Verilog-A, it equivalent to declare the sampling frequency of feedback path. In this project, the feedback was a sequential communication, required to record the previous output which would be regarded as the target signal for current period.

Another method was to use the VCVS. However, this method was limited to

polynomial dimensions as the software only supported two dimensions. Although, the  $\arcsin()$  function can be represented in Taylor series, only two dimensions was not accurate for this project. It caused more periods to track the reference signal.

- Use software to design and simulate the transistor level schematic of the signal control system.

The software used in this project was Cadence Virtuoso SPICE simulator. It supported the library of 180nm technique CMOS transistor. Associated with circuits implemented in the project, all the transistors had same scaling level. The geometry of transistor was considered for fabrication, by scaling the length of transistor to 1um. Hence, the desired transconductance was obtained by sweeping the weight of transistors. Also, for large weight, the finger was used to support optimise number of contacts in order to reduce the resistance and capacitance of the transistor, so that the device can be faster.

The control system was tested by sweeping the signal amplitude and phase errors. The sweeping range for amplitude was from 150 to 250mV, which corresponding to sweeping amplitude ratio from 0.75 to 1.25. Meanwhile, the sweeping range for phase error was from -50 to 50 degrees. Refer to the results listed in section 5.7, the control system was able to track reference signal within three periods. The length of period was determined by the shortest transient response for estimations to be settled down in time domain. Also, a predefined amplitude or phase offset can control the reference signal. Associated with the correction block, it can be either counting the period of feedback, or comparing the estimation with error free situation, so that to eventually load the predefined offsets after the target signal matched the reference signal.

- Test the system with wide range of input signals to evaluate the signal control system.

Analogue communication had two advantages comparing to digital processing. One was continues, another one was able to operate for high frequency that ADC (analogue to digital conversion) cannot handle. Therefore, the last objective was aimed to achieve high frequency environment for the control system. The original input frequency configuration was set to 1.5KHz. Then, the frequency was increased to 10KHz, 100KHz, 1MHZ, 10MHz and 50Mhz respectively. The Maximum frequency allowed for the simulation was about 60MHz. However, while the frequency increased, the accuracy of phase shifter reduced, which caused larger offsets for amplitude and phase estimation. It was acceptable as the correction was digital block. Therefore, the offset of correction required to reset while increasing the frequency based on estimations.

The major limitation was caused by the operational amplifier. Refer to the frequency response of OPAMP, the gain decreased while the frequency increased. In other word,

the current could flow into the input terminal as the gain was low (within 20dB). In this term, the OPAMP cannot operate as inverting configuration which caused the faults for signal amplitude and phase estimations. Therefore, associated with section 5.7.2, different types of two-stage OPAMP were simulated to extend frequency response. The main technique to improve the OPAMP was to reduce the dominated pole. It increased the 3dB point to about 55KHz. On the other hand, the phase margin reduced to about 59 degrees, which indicated the stability became lower.

In summary, all the objectives were achieved. By accomplishing this project, a signal amplitude and phase control system was implemented. All the analogue circuits were designed and simulated based on the mathematical consequences of error estimations. Also, both analogue and digital communication were practiced in this project, corresponded to estimation and correction part respectively. A new technique of estimations using phase comparison in suppression loops was implemented to provide independent detection of signal amplitude and phase simultaneously.

## **7 SUGGESTIONS ON THE POSSIBLE IMPROVEMENTS AND FURTHER WORK**

The major improvement for the signal amplitude and phase control system will be further increasing the input frequency. As the limitation of the current achievement is OPAMP, a high gain and high speed OPAMP will be required. This can be achieved by using small scaling size of transistor or multi-stage configurations.

Also, a new mechanism of phase shifter will improve the accuracy of estimations. It can use the inductor and capacitor based circuits. Referring to the comparison of low-pass filter, a narrower pass-band will improve the system become faster for estimations.

In order to achieve pure analogue communication as continuous processing, the feedback block can be implemented as analogue circuits. However, it increases the complexity.

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## Appendix A

```
function [ cosx ] = fig3( A1db,A2db,P1deg,P2deg )  
    % A1db amplitude in db for input signal 1  
    % A2db amplitude in db for input signal 2  
    % P1deg phase for input signal 1  
    % P2deg phase for input signal 2  
  
Adb=(A2db-A1db)/50;      % find amplitude range  
A1=db2mag(A1db);         % Convert decibels (dB) to magnitude  
A2=db2mag(A2db);  
A=(A2-A1)/50;             % amplitude in magnitude  
  
P1=deg2rad(P1deg);        % Convert to radius  
P2=deg2rad(P2deg);  
Pdeg=(P2deg-P1deg)/50;  
P=(P2-P1)/50;  
[phdeg,kdb]=meshgrid(P1deg:Pdeg:P2deg,A1db:Adb:A2db); %3d grid set  
[ph,k]=meshgrid(P1:P:P2,A1:A:A2);  
  
numerator=1-(k.^2);  
x=1+2.* (k.^2).*cos(2.*ph)+(k.^4);  
denominator=x.^(1/2);  
cosx=numerator./denominator;  
cosxrad=acos(cosx);           % calculate based on algorithm  
cosxdeg=abs(rad2deg(cosxrad));  
surf(phdeg,cosxdeg,kdb);       % 3D plot  
  
end
```

## Appendix B

```
// VerilogA for project, fix, verilogA
/*
this code was basic version to fix the amplitude
and phase error based on the estimations.
*/

`include "constants.vams"
`include "disciplines.vams"

module fix(out, ampdiff, phasediff, ref, va, vp);
output out;
electrical out;
inout ampdiff;
electrical ampdiff;
inout phasediff;
electrical phasediff;
input ref;
electrical ref;
input va;
electrical va;
input vp;
electrical vp;

parameter real ofset=18.1425e-3;           // predefined offset
parameter real amp=0.04;                  // square of the amplitude of the
                                           // reference signal
parameter real lpfgain=6.6;              // gain of low pass filter
parameter real fin=1500;                  // input frequency

//local variables
real ph,base,angle,inv;
real ks;
real k,rad;
real vas,aout;

analog begin

vas=(V(va)+ofset)/lpfgain;          // desired amplitude estimation
ks= 1-2*(vas)/amp;                  // detect amplitude ratio
k=sqrt(ks);                         // output amplitude ratio as analogue signal
V(ampdiff) <+ k;
```

```

aout=V(ref)/k;           // correct amplitude
ph=(V(vp)+offset)/lpfgain; // desired phase estimation
base=2*(ph)/(k*amp);
angle=asin(base);        // detect phase error in radian
inv=1/fin;               // find time interval for one period
rad=angle*(inv/2*M_PI)/10; // calculate corresponding delay

if (rad<0)
begin
  rad=inv+rad;           // ensure delay as a positive number
end
V(phasediff) <+ rad;      // output delay as a analogue signal

V(out) <+ absdelay(aout,rad,1); //correct phase error
end

endmodule

```

## Appendix C

```
// VerilogA for project, fix6, veriloga
/*
this code was advanced version to fix the amplitude
and phase error based on the estimations.
using timing event control and record previous signal
for next correction
*/
`include "constants.vams"
`include "disciplines.vams"

module fix6(out, ampdiff, phasediff, temp1, temp2, temp3, ref, va, vp);
output out;
electrical out;
inout ampdiff;
electrical ampdiff;
inout phasediff;
electrical phasediff;
inout temp1;
electrical temp1;
inout temp2;
electrical temp2;
inout temp3;
electrical temp3;
input ref;
electrical ref;
input va;
electrical va;
input vp;
electrical vp;

parameter real ofset=18.1425e-3; // predefined offset
parameter real amp=0.04; // square of the amplitude of the
// reference signal
parameter real lpfgain=6.6; // gain of low pass filter
parameter real fin=1500; // input frequency

//local variables
real ph,base,angle,inv;
real k,k3,ks,rad;
real vas,aout;
```

```

real coff1,coff2,coff3,coff4;           // use coefficient to control output
real find,kfind,phfind;
real find1,kfind1,phfind1;
real find2,kfind2,phfind2;
real find3,kfind3,phfind3;
real find4,kfind4,phfind4;
real ktemp,phtemp;

analog begin

@(initial_step) begin
coff1=1;
coff2=0;
coff3=0;
coff4=0;
// initialise
kfind1=1;
kfind2=1;
kfind3=1;
end

@(timer(300m)) begin
coff1=0;
coff2=1;
coff3=0;
coff4=0;
end

@(timer(600m)) begin
coff1=0;
coff2=0;
coff3=1;
coff4=0;
end

@(timer(900m)) begin
coff1=0;
coff2=0;
coff3=0;
coff4=1;
end

vas=(V(va)+offset)/lpfgain;

```

```

ks= 1-2*(vas)/amp;
k=sqrt(ks);
V(ampdiff) <+ k;

ph=(V(vp)+offset)/lpfgain;
base=2*(ph)/(k*amp);
angle=asin(base);
inv=1/fin;
rad=angle*(inv/2*M_PI)/10;
if (rad<0)
begin
rad=inv+rad;
end
V(phasediff) <+ rad;

if(coff1==1) begin
kfind1=k; // within 300mS, record ratio as k1
phfind1=rad; // within 300mS, record phase error as phasel
ktemp=1;
phtemp=0;
end

if(coff2==1) begin
kfind2=k;
phfind2=rad;
ktemp=kfind1;
phtemp=phfind1;
end

if(coff3==1) begin
kfind3=k;
phfind3=rad;
ktemp=kfind1*kfind2;
phtemp=phfind1+phfind2;
end

if(coff4==1) begin
kfind4=k;
phfind4=rad;
ktemp=kfind1*kfind2*kfind3;
phtemp=phfind1+phfind2+phfind3;
end

```

```

$strobe("k1=%f,k2=%f,k3=%f",kfind1,kfind2,kfind3);
                                // print the captured values

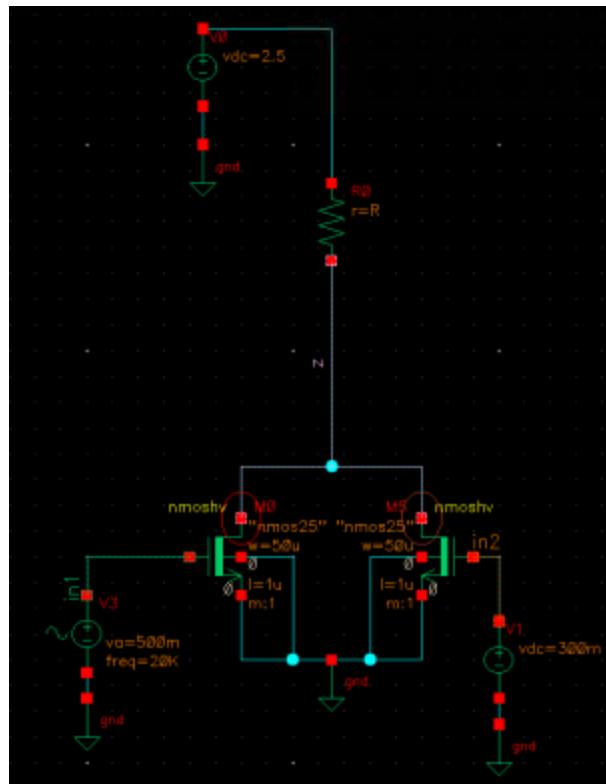
/* method 1: record signal as target for next correction
V(temp1) <+ absdelay(V(ref)/kfind,phfind,1);
V(temp2) <+ absdelay(V(temp1)/kfind2,phfind2,1);
V(temp3) <+ absdelay(V(temp2)/kfind3,phfind3,1);
V(out) <+ coff1*V(ref)+coff2*V(temp1)+coff3*V(temp2)+coff4*V(temp3);
*/
/* method 2: record detected ratio and phase error only*/
V(out) <+
coff1*V(ref)+(coff2+coff3+coff4)*absdelay(V(ref)/ktemp,phtemp,1);

end
endmodule

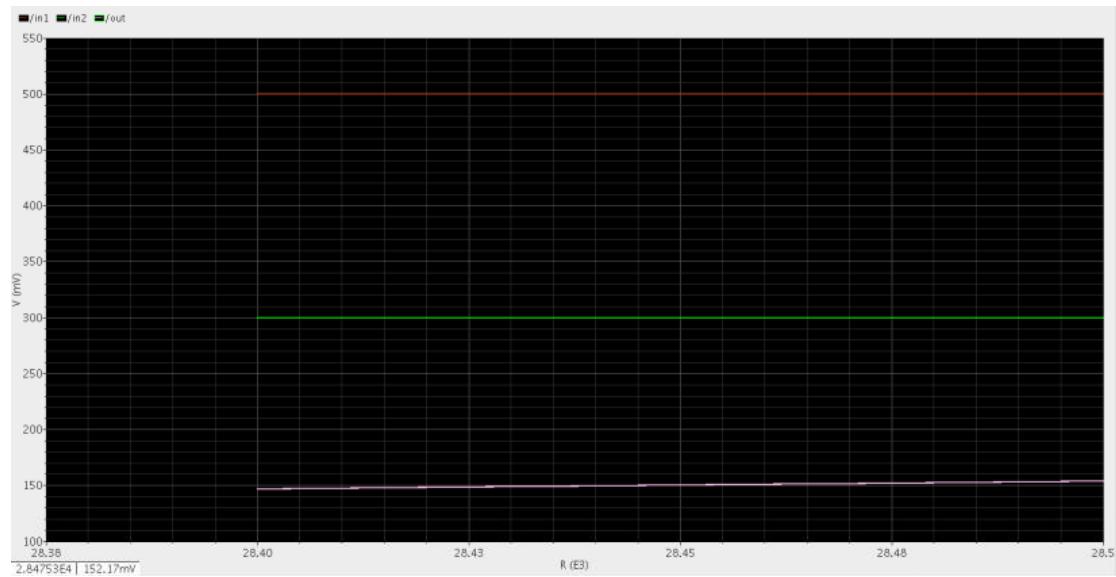
```

## Appendix D

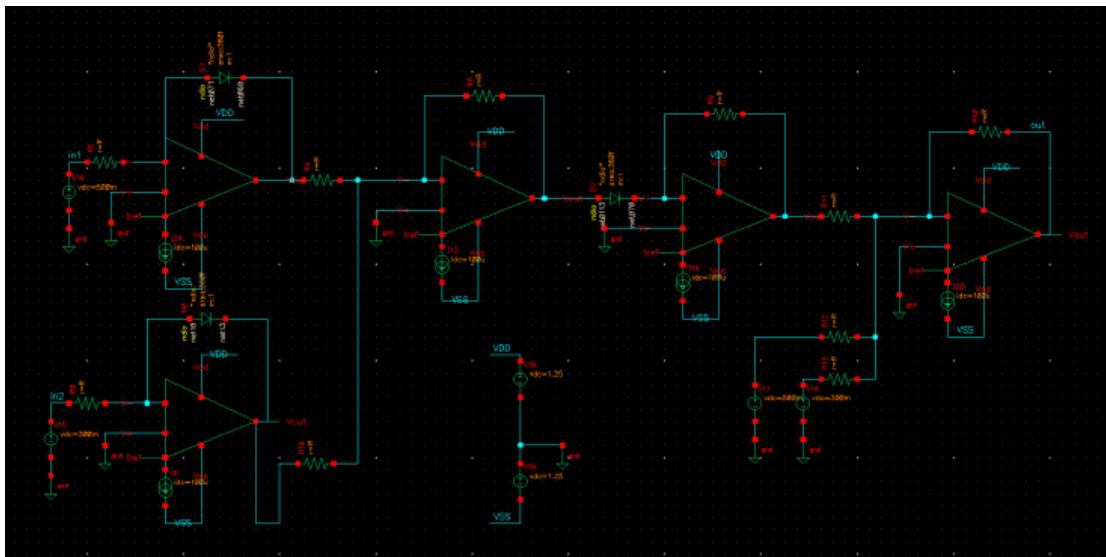
In this section, different types of analogue multiplier were listed.



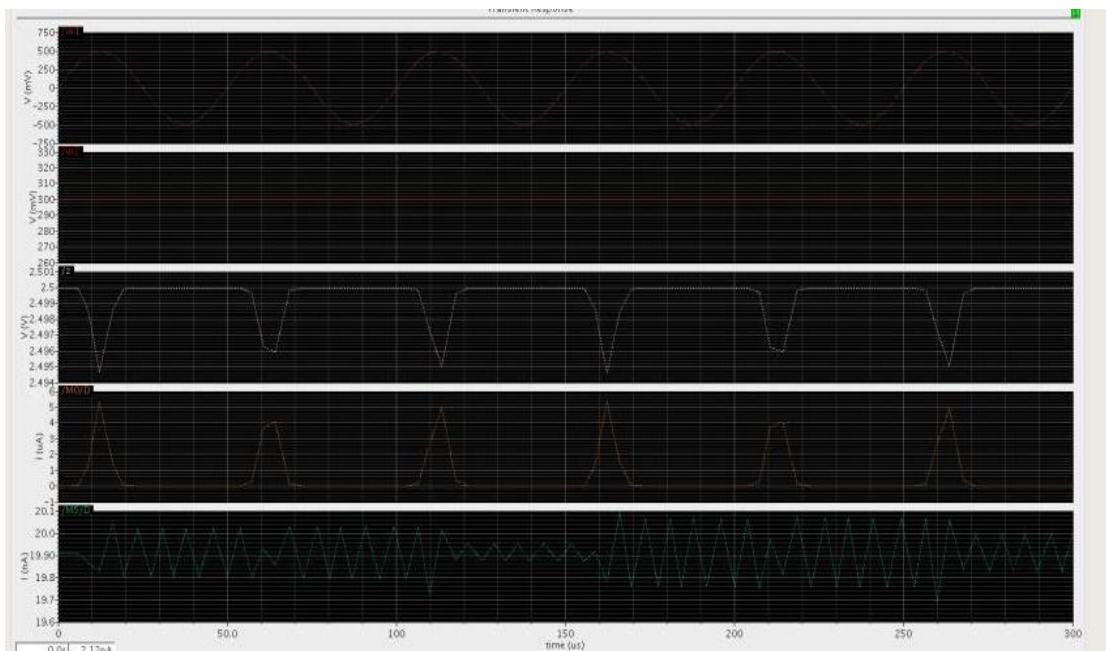
The circuit showed above was single combiner.



Refer to simulation for combiner, it was able to provide a simply multiplication. The inputs were DC voltage setting to 300 and 500mV. Also, the output was about 150mV.



The circuit was the diode based multiplier.



The simulation was not matched the calculation. It was limit by the geometrical layout.

## Appendix E

Calculation for 9-order Butterworth filter:

- Choose resistor and capacitor for filters,

$$\omega_0 = 2\pi f_p = 67.73 \text{ rads/s}$$

Choose capacitor as 100nF

$$R = \frac{1}{100 \times 10^{-9} \times 67.73} = 14.765 \text{ k}\Omega$$

- Parameter  $\epsilon$

$$\epsilon = \sqrt{10^{A_{max}/10} - 1}$$

$$= \sqrt{10^{1/10} - 1} = 0.05088$$

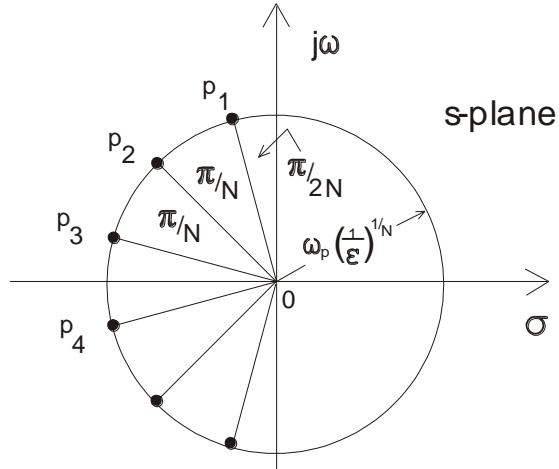
- Order

$$\begin{aligned} A(\omega_s) &= -20 \cdot \log_{10} \left[ 1 / \sqrt{1 + \epsilon^2 \cdot (\omega_s / \omega_p)^{2N}} \right] \\ &= 10 \cdot \log_{10} \left[ 1 + \epsilon^2 \cdot (\omega_s / \omega_p)^{2N} \right] \\ 25 &= 10 \cdot \log_{10} \left[ 1 + \epsilon^2 \cdot (\omega_s / \omega_p)^{2N} \right] \end{aligned}$$

$$25 = 10 \log_{10} \left[ 1 + 0.2589 \times \left( \frac{15}{10} \right)^{2N} \right]$$

Here, N=8.76. Hence, choose 9 as the order number.

- Poles



$$P1 = \omega_0(-\cos 80^\circ + j\sin 80^\circ) = \omega_0(-0.1736 + j0.9848)$$

And p9 will be the conjugate of p1, i.e.

$$P9 = \omega_0(-0.1736 - j0.9848)$$

In the transfer function denominator, these two poles will be of the type:

$$(s - p1)(s - p9) = (s + \alpha - j\beta)(s + \alpha + j\beta) = (s + \alpha)^2 + \beta^2$$

Note that  $\alpha$  and  $\beta$  are BOTH positive, so that

$$(s-p_1)(s-p_9) = s^2 + 2\alpha s + (\alpha^2 + \beta^2) = s^2 + 2*0.1736*s\omega_0 + (0.1736^2 + 0.98482)\omega_0^2$$

or, as  $(0.1736^2 + 0.98482) = 1$ :

$$(s - p_1)(s - p_9) = s^2 + 0.3472s\omega_0 + \omega_0^2$$

The other conjugate pole-pairs may be shown to give:

$$(s - p_2)(s - p_8) = s^2 + s\omega_0 + \omega_0^2$$

$$(s - p_3)(s - p_7) = s^2 + 1.5321s\omega_0 + \omega_0^2$$

$$(s - p_4)(s - p_6) = s^2 + 1.8794s\omega_0 + \omega_0^2$$

and the real pole gives:  $(s - p_5) = (s + \omega_0)$ .

So the complete transfer function will be:

$$T(s) = 10\omega_0^9 / [(s + \omega_0)(s^2 + 0.3472s\omega_0 + \omega_0^2)(s^2 + s\omega_0 + \omega_0^2)^* \\ * (s^2 + 1.5321s\omega_0 + \omega_0^2)(s^2 + 1.8794s\omega_0 + \omega_0^2)]$$

The values for resistor and capacitor showed in section one will also be used for all the second order sections. It is important to note that in the second order section the OPAMP gain AVO =  $(1 + R_2/R_1)$  is used to obtain the multipliers of  $s\omega_0$ . Comparing the first second order term in the T.F.  $(s^2 + 0.3472s\omega_0 + \omega_0^2)$  with the T.F. of the filter:

$$T(s) = \frac{V_{out}(s)}{V_{in}} = \frac{A_{vo}\omega_0^2}{\omega_0^2 + (3 - A_{vo})s\omega_0 + s^2}$$

we find that for the first second order section we must have:

$$0.3472 = 3 - A_{vo} = 3 - (1 + R_2/R_1) = 2 - R_2/R_1$$

Hence:  $R_2/R_1 = 2 - 0.3472 = 1.6528$ . So we could use, for example,  $R_1 = 10k\Omega$  and  $R_2 = 16.53k\Omega$ . We should note that the dc gain of this section will be  $AVO = (1 + R_2/R_1) = 2.653$ .

In exactly the same way, the values of the feedback resistors  $R_2$  and  $R_1$  can be calculated for the other THREE second-order sections. For the second one (i.e. U3) we have:  $R_2/R_1 = 2 - 1 = 1$ . So we could use, for example,  $R_1 = 10k\Omega$  and  $R_2 = 10k\Omega$ . We should note that the dc gain of this section will be  $AVO = (1 + R_2/R_1) = 2$ .

The third one (U4) will be:  $R_2/R_1 = 2 - 1.5321 = 0.4679$ . So we could use, for example,  $R_1 = 10k\Omega$  and  $R_2 = 4.68k\Omega$ . We should note that the dc gain of this section will be  $AVO = (1 + R_2/R_1) = 1.468$ .

And finally for U5  $R_2/R_1 = 2 - 1.8794 = 0.1206$ . So we could use, for example,  $R_1 = 10k\Omega$  and  $R_2 = 1.2k\Omega$ . We should note that the dc gain of this section will be

$$AVO = (1 + R2/R1) = 1.12.$$

So the gains of all four second order sections will be:

$$1.12 * 1.468 * 2 * 2.653 = 8.724$$

So for a dc gain of 10 the first order section will have to have a gain of  $10/8.724 = 1.146 = (1 + R2/R1)$ . Hence  $R2/R1 = 1.146 - 1 = 0.146$ . So we could again use:  $R1 = 10k\Omega$  and  $R2 = 1.46k\Omega$ .