Abstract

Due to the CMOS technology scaling, digital systems that can consume the lowest quantity in power are required due to the large demand of portable and mobile devices or systems. One effective methodology for these ultra-low-power applications is to lower the power supply voltages to sub-threshold region. But the major limitations to reduce SRAM supply voltage are the stability degradation of the cell and the raise of process variation with process scaling, which increase the difficulty in the low power SRAM design. Large variability in nano-CMOS technologies can easily causes functional failures in the conventional 6T SRAM cell at low supply voltage because it can not provide large noise margin for proper operation.

According to the previous research work, the read and write decoupled scheme can be considered as an effective strategy to enhance the SNM with low power operation. In this paper, we compare the performance of lots existing SRAM cells designed by using various process technologies and a novel 10T SRAM cell is presented in different CMOS technologies employing separate bitline and wordline for read and write operation and a virtual ground during the write operation to increase the immunity against the process variation. The impact of process parameter variations of the proposed 10T cell and the conventional 6T cell, with supply voltage scaling, is investigated to evaluate cell functionality and performance. Monte Carlo simulations indicate a 158% increase in the read stability, a 17% write time accelerated and a 80% power saving compared to the conventional 6T SRAM cell with a 48% area overhead. A Built In Current Sensor (BICS) technique is used in this proposed SRAM cell to estimate single event upsets (SEUs) in the cell working and idle conditions. The appearance of soft errors can be detected by generating an error signal to high. Hence, this BICS SRAM cell can monitor soft error when it is appeared on the cell at any second time in both operating and standby conditions.

Contents

Chapter 1: Introduction and Context

Based on today's integrated circuits design, a large amount of area and energy is consumed by cache memories. However, the modem microprocessor design, which occupies the majority of the overall chip area, requires lower power consumption and higher power efficiency due to increasing demand of battery powered mobile electronic devices. Thus the SRAM caches are proposed and investigated as the integral part of the advanced microprocessor, due to these portable devices and systems have both high speed requirements and complicated functionalities. One effective method used to improve the system performance is to increase the density of SRAM caches, but minimizing the size of transistor will lead to increase devices variation and leakage, which brings more challenges of developing SRAM with higher reliability and performance while ensuring the SRAM cell can meet the low-power –consumption requirements. The motivation of low power fault tolerant design of embedded SRAM memory in nano CMOS comes from two emerged requirements, low power consumption and Single-Event-Upset (SEU) analysis.

1.1 Motivation

1.1.1 Low power design

Power management becomes the most important issue concerning the popularity of battery powered embedded systems and mobile devices. Reducing the power dissipation in these systems and devices can improve the system power efficiency, performance, reliability, while the speed is the secondary consideration.

Many portable medical monitoring systems and devices either invasive or non-invasive, which are applied in the biomedical area, the low-power or even ultra-low-power dissipation design is proposed since the light-weight and long-term requirements. In nowadays, power is always the most crucial limitations as large battery is too heavy to make the monitoring device to be convenient for patients. For battery free monitoring systems which has the power harvest device for power supply, but the energy harvesting module can only supply small power consumption of normal semiconductor devices which lead the pressure of power dissipation is extremely critical. In space technology area, most of the power consumption of the satellites is provided by the solar panels during their lifetime, therefore if the power consumption could be minimized then the weight of satellites could be reduced and more other equipment can be carried on board as the solar panel will be decreased. Furthermore, although the rechargeable battery is very popular today, but the

operation time is still a critical limitation for most consumer level portable electronics devices.

Reducing the supply voltage is the most efficient way to minimum the total power consumption in semiconductor devices. Either static or dynamic power dissipation can be reduced along with the supply voltage scaling down. Static power is lowered as the leakage current is reduced. The following equation represents the relationship between supply voltage and dynamic power dissipation:

$$P_{dyn} \propto f*Vdd^2*C$$

Where, f is operation frequency of the circuits, Vdd is the power supply, and C is the load capacitance connected between ground and Vdd. To greatly reduce the Vdd to sub-threshold range of CMOS transistors can be used to achieve the low-power requirements. But if CMOS technology scales down, then the SRAMs are more sensitive to process variations in width, length, gate oxide thickness and have great different in threshold voltage, which will significantly affect the decrease of the supply voltage. The tranditional 6-Transistor SRAM will be out of use when the supply voltage is lowered to sub-threshold range, this is because of the greatly reduction of Static Noise Margin (SNM). Thus, the first stage is to design and functional and stable SRAM against process variation, this is applied to reduce the supply voltage which is in order to meet the low power requirements.

1.1.2 Single Event Upset Detection Design

Single Event Effects (SEE) in microelectronics are normally appeared when energetic particles his sensitive regions or paths of a microelectronic circuit in the natural space environment [2]. Once the SEE make a different of logic state, it is called Single Event Upset (SEU). For SEUs that applied in memory, there were several reports bot in terrestrial and space microelectronics back to 1970's [3, 4]. They could be induced by two different ways: the alpha-particle contaminant packages for terrestrial memories and cosmic-rays for satellites concern subsystem. With the scaling of CMOS technologies, the major consideration of high reliability microelectronics design will be SEUs. Such as rocket science, even the error rate of one per 24 hours cannot be neglected [2].

The SRAM which is working under sub-threshold voltage is more susceptible to SEUs than the SRAMs which is working under normal voltage, this because of the noise margin is limited by the lower supply voltage [5]. Thus, if it is intend to achieve ultra-low-power SRAMs design in space or other crucial applications with high requirement of reliability, the technology of detecting and correcting SEUs must be considered as initial work. The SEUs could be detected by the most recently techniques such as Build in Current Sensor (BICS). In traditional way, the SEUs can only be detected under the cell standby mode. As the SEUs is possible to appear at

any moment, i.e. either standby or operating mode. Thus, it is important to investigate another BICS technique that applied to the memory cells to detect the SEUs with higher efficiency.

1.2 Aims and Objectives

The primary aim of this particular project is to improve the existing memory cell structure and develop new approaches to design a new memory cell which is functional and highly stable against the nanoscale process variations, as well as significantly low power consumption. The effectiveness of the proposed solution will be validated through extensive HSPICE and Matlab simulations. In addition, the secondary aim is to implement an efficient technique to detect soft errors in SRAM Cells.

The main objectives can be briefly described as follows:

1. Research methods and techniques for low voltage operation of memory cell.
2. Research and analyze the performance of existing SRAM cells, compare the functionality and static noise margin (SNM) under process variation.
3. Research the existing test techniques using for soft errors detection in SRAM Cells
4. Design and implement a new approach in order to improve the SRAM performance under process variation while reducing power dissipation, such as improve cell reliability and stability, increase the read and write margins, speed up read and write access time.
5. Implement an efficient technique to detect the occurrence of soft error in SRAM design.
6. Evaluate all the designs or solutions by HSPICE and Matlab simulations.

1.3 Thesis Outline

This thesis can be organized as follows. In Chapter 2, SRAM design and the stability problem is described first. Next, previous successful low-power SRAM designs will be analysis and compared as well as the various technologies they have used to compensate the problems in low power SRAM design. The background to SEU and its typical model used in SRAMs, as well as effective SEU detection methods are discussed in Chapter 2. The challenges in low power SRAM design will be listed in detail in Chapter 3. The whole architecture, include the involved designs are proposed in Chapter 4, such as the SRAM cell, sense amplifier design, Address Transient Detector (ATD), row decoder and column multiplexer etc. Chapter 5 will present

some simulation results about the proposed SRAM Cell design in different nano-scale CMOS technology, the SRAM Cell layout is also included. The SEU detection results of the proposed SRAM cell design will be shown in Chapter 6. Conclusion and future work will be described in Chapter 7 and Chapter 8 respectively.

Chapter 2: Background and Previous work

Like most sequencing elements in digital systems, memory cells used in on-chip memories can be divided into static and dynamic structures. While dynamic structure uses a capacitor needed to be periodically refreshed, static structure employs cross-coupled inverters to keep the data. Static memories are faster and more stable, but require more area per bit.

2.1 Conventional SRAM Cell

The most common used structure in today's commercial SRAMs is the conventional 6-Transistor (6T) SRAM Cell structure. It is the key component to all other kinds of memory cells.

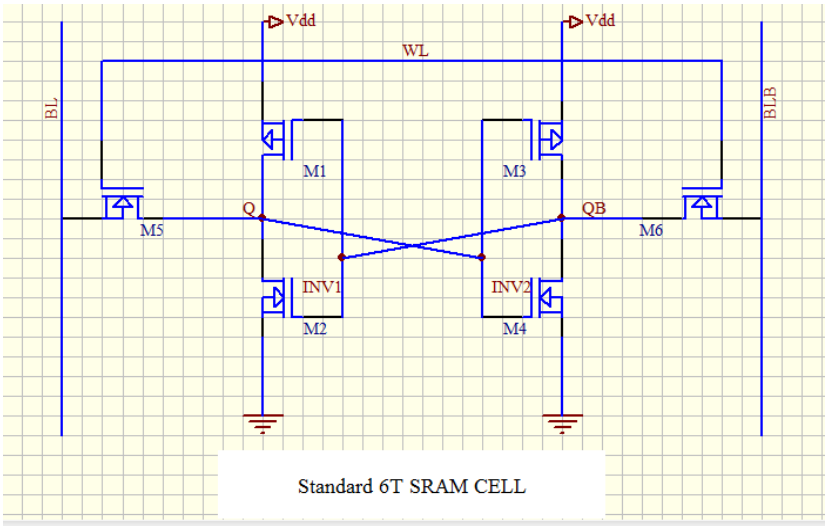


Figure 2.1: conventional 6T SRAM Cell

Figure 2.1 shows the schematic of the conventional 6T SRAM Cell. It consists of a cross-coupled inverter pair formed by M1- M4 and two pass transistors M5 and M6. The storage nodes are specified by Q and QB. Assume node Q stores data "0" and QB stores data "1". During standby operation when the circuit is idle, the word line "WL" is not asserted while two bitlines BL and BLB both remain at precharged value Vdd. During the read operation when the data is requested, the word line "WL" is asserted which turns on the pass transistors M5 and M6. The values on storage nodes Q and QB will be transferred to the bitlines BL and BLB respectively by leaving BLB at its precharged value and discharging BL to GND through M5 and M2. As the bitlines BL and BLB will have a small difference of voltage between them, a sense amplifier is required to sense which line has got the higher voltage and to determine whether the output should be "1" or "0".

During the write operation when updating the SRAM Cell's contents, first apply the new value that will be written to the two bitlines. If the operation is writing "1", we should set BL to "1" and BLB to "0". WL is then asserted and the pass transistors M5 and M6 are both enabled. BL will charge storage node Q to Vdd through M5, while on the BLB side, transistor M4 will pull BLB down to GND. Therefore, the values on storage nodes Q and QB are both reversed which indicate new data has been written into the SRAM Cell.

In the conventional 6T SRAM (Figure 2.1), the cell is required to be stable during the read operation and writeable during the write operation ignoring redundancy. However, the 6T SRAM Cell has poor read stability as during read operation the pass transistors M5 and M6 provides direct access to the SRAM cell storage nodes. The storage node Q will rise above "0" because of the voltage division between the pass transistor M5 and the driver transistor M6.

Therefore, improper sizing of the pass transistors and storage inverters will cause a read upset. For example, a stored "0" can be rewritten by "1" if the voltage of node Q rises higher than the Vth of transistor M4 to pull node QB down to "0" and accordingly pull node Q up to "1". Ignoring the body and short-channel effects of the transistors, the maximum allowed voltage ΔV on node Q during the read operation can be expressed below:

$$\Delta V = \frac{V_{DSATn} + CR(V_{DD} - V_{THn}) - \sqrt{V_{DSATn}^2(1+CR) + CR^2(V_{DD} - V_{THn})^2}}{CR}$$, where

$$CR = \frac{W2/L2}{W5/L5}$$ defined as the cell ratio.

Since the 6T SRAM cell is symmetrical, CR is the same for transistors M4 and M6.

The relationship between ΔV and CR is shown in Figure 2.2 (the cell is simulated in CMOS 130nm technology, $V_{DD} = 1.2V$). In order to achieve a non-destructive read operation, CR should be not less than one and can be varied which lies on the target application of the SRAM Cell. Larger CRs cause higher leakage current (speed as well) and stability during read access but larger area, while smaller CRs provides a more compact SRAM Cell with moderate speed and stability. To ensure the cell stability and reduce the leakage current, it is suggested to employ a minimum width with a bit larger than the minimal length pass transistors and a minimal length with a bit larger than minimal width driver transistors.

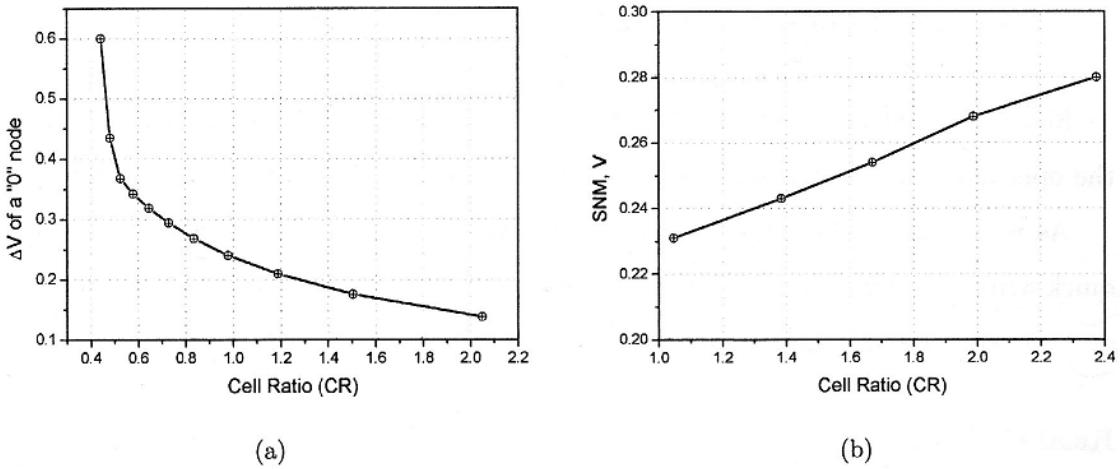


Figure 2.2: The rise ΔV of the "0" mode (a) and the SNM (b) as a function of the Cell Ratio (CR) in a 6T CMOS SRAM cell (simulated in CMOS 0.13 μm technology,Vdd=1.2V) [43]

Therefore, the read stability can be improved if providing strong storage inverters but weak pass transistors. However, for reaching higher write ability, the opposite is desirable to strengthen the pass transistors while weaken the storage inverters. This is because the voltage on the "1" storage node can be defined as a function of the pull-up ratio (PR) of a 6T SRAM Cell, which can be expressed as follows:

$$V_{"1"} = V_{DD} - V_{THn} - \sqrt{(V_{DD} - V_{THn})^2 - 2\frac{\mu_p}{\mu_n} PR((V_{DD} - |V_{THp}|)V_{DSATp} - \frac{V_{DSATp}^2}{2})}$$

Where $PR = \frac{W1/L1}{W5/L5}$, defined as the pull-up ratio.

Since the 6T SRAM cell is symmetrical, PR is the same for transistors M3 and M6.

The relationship between pull-up ratio and voltage drop on "1" storage node is shown in Figure 2.3 (the cell is simulated in CMOS 130nm technology, V_{DD} =1.2V). The pull-up transistors are used to keep the high level on the "1" storage node and prevent it will not discharge through the driver transistors due to the off-state leakage current during the data retention and to provide data transition(low to high) when overwriting. During the data overwriting, in order to pull the voltage on the "1" storage node below V_{THn}, it is desirable that the W/L of the pull-up transistor should be smaller than the W/L of the pass transistor. So during the write access, it is required to provide a

strong pass transistor and weak pull-up transistors, especially for the worst process conditions, such as in the fast PMOS and slow NMOS corner. Thus despite 6T SRAM Cell is the most common structure used in today's SRAMs, the need of read stability and write ability cannot be optimized simultaneously because of the same pass transistors used during both read and write operation.

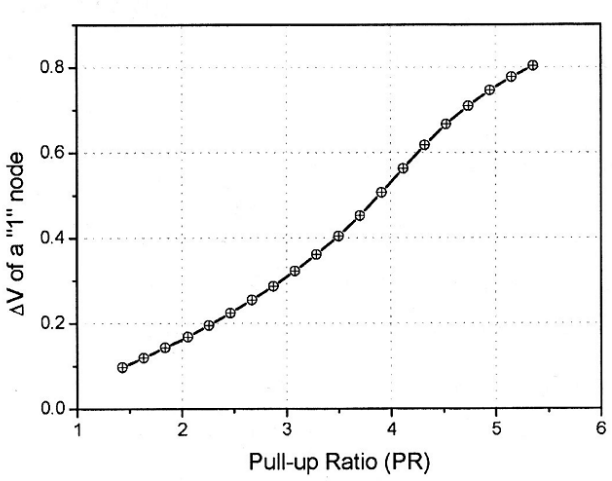


Figure 2.3: The voltage drop at node $V_{"1"}$ during write access as a function of the Pull-Up ratio (PR) of a 6T CMOS SRAM cell (simulated in CMOS 0.13 μm technology, Vdd=1.2V) [43]

2.2 SRAM Cell Stability

2.2.1 Introduction to SRAM Stability

The stability of embedded SRAM is usually measured and analyzed by the dynamic and static performance during the SRAM normal operation state. As CMOS technology scales down in the nanometer region, it makes the designer hard to achieve a reliable behavior as the process variation defects the performance of the memory cell more frequently.

There are many published designs to evaluate and enhance the SRAM stability. [6] In 2006, Khellah et al. [7] suggested the wordline and bitline pulsing schemes to improve SRAM cell failure rates at low power supply voltages. Another successful improvement is published by Suzuki et al. [8] described a SRAM with an 8-T SRAM cell that copes with cell disturbances in unselected columns during a write operation. In 2007, Khellah et al. [9] presented a method to measure the dynamic SRAM stability degradation due to the power supply noise. These popular techniques are

based on the memory cell stability characteristic in both read and write events and have improved the overall cell stability.

2.2.2 SRAM SNM and Process Variation

2.2.2.1 SNM and Process Variation Definition

Several different ways have been proposed to define the stability of SRAM [10], while Static Noise Margin (SNM) and its analytical criteria introduced by Seevinck [11], are more common used to estimate the SRAM Cells' stability. The noise margin is defined as the input voltage to output voltage characteristic, VTC (Voltage Transfer Characteristic). Generally, it is the maximum spurious signal that can be tolerated by the cell while maintaining the cell operating state. Assume that the noise pulse is long enough for enabling the circuit to react, such as the noise is static or dc. Therefore, static noise margin is proposed if the noise is a dc source and can represent the minimum DC noise margin to affect the cell operation state and help to evaluate the stability of memory cell with a static approach.

As shown in Figure 2.4, consider that the 6T SRAM Cell has two cross-coupled inverters INV1 and INV2, the SNM can be defined as the maximum value of Vn that can be accept by the cell to ensure the correct operation.

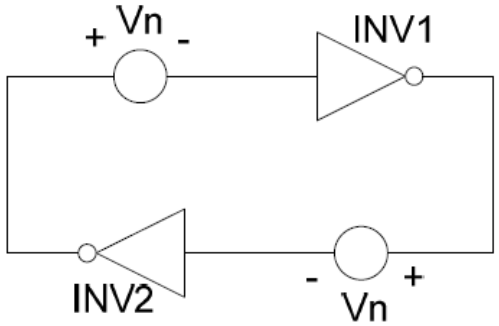


Figure 2.4: Cross coupled inverter with noise source [35]

In the conventional 6T SRAM Cell(Figure 2.1),the SNM can be found during the SRAM Cell standby and read operations, defined as read SNM and hold SNM respectively. During the read access, pass transistors M5 and M6 are both turned on, two bitlines BL and BLB are precharged to Vdd, the internal node which stores "0" will be possible to pull upward to "1" because of the voltage division effect between pass transistors and drive transistors, so the read SNM is degraded. In standby operation, the pass transistors M5 and M6 are both off, hence the hold SNM is much larger than read SNM which indicate that read SNM has less resilience to noise and is

more crucial in evaluating the stability of SRAM Cell. In the following part of this paper, the SNM is represented to read SNM unless specified.

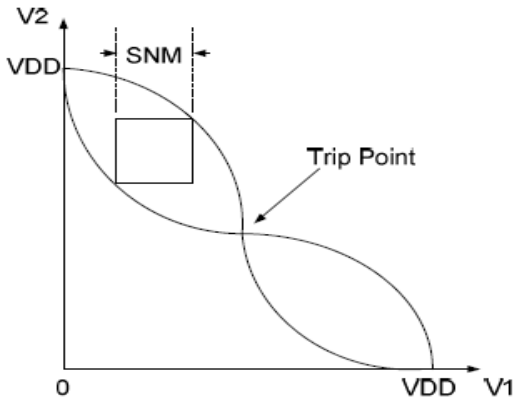


Figure 2.5: SNM estimation based on maximum square [36]

From the butterfly characteristic curves of the SRAM Cell, shown in Figure 2.5, the SNM can be estimated by the largest square box that can be fitted inside the curves. The edge length of the largest square is the SNM. Therefore, the larger square box is obtained in the butterfly curve, the higher SNM as well as higher stability of the SRAM Cell is achieved in the SRAM cell design.

An effective simulation method for measuring the SNM was also introduced by Seevinck [10]. The maximum value of the difference between the outputs Vout1-Vout2 can be computed from the simulation, which is equal to the diagonals of the largest square fitted in the butterfly characteristic curves. SNM can be achieved by multiplying the value of Vout1-Vout2 by $1/\sqrt{2}$. Therefore, in the following parts of this paper, this simulation method will be applied for the stability comparison of different SRAM Cell designs.

As CMOS technology scales down, the feature size of transistor is decreased which makes difficult in fabricating such small structure consistently across a die or a wafer [12]. Due to the small geometry of the transistor, its parameters are easily to vary die to die or within the same die. Therefore, the inability to obtain small geometric transistor size and the inability to control dopant fluctuation induced threshold voltage will lead to the functional failures in SRAM Cell, as well as unexpected parametric yield degradation [13],[14].

Several factors, such as changes in dielectric thickness, substrate, polysilicon and implant impurity levels; surface charge; and lithographic process, need to be considered because it may affect these transistor parameter variations. Normally, variations in process parameters can be classified into inter-die and intra-die variations. Inter-die variations represent the random variations that occur between

different chips in one wafer or different wafers, whereas *intra-die* variations represent the random variations that occur between different devices and interconnects in the same chip [13].

Random intra-die variations which are primarily caused by the threshold voltage variation due to the random dopant fluctuations will lead to several parametric failures in the SRAM Cell [13,14], such as changes on data during the read operation, unsuccessfully write the data into the cell, data flipping at a lower operating voltage when the cell is idle.

Environmental factors and physical factors can be considered to be two main sources in process variation [15]. The environmental factors depend on the operating conditions of the circuit, such as temperature, supply voltage. And another main source physical factors is owing to the limitations in the fabrication process, including the effective channel length and width, gate oxide thickness and threshold voltage variations. SRAM can fail due to any of the above parametric variations.

2.2.2.2 Process Variations effect on SRAM SNM

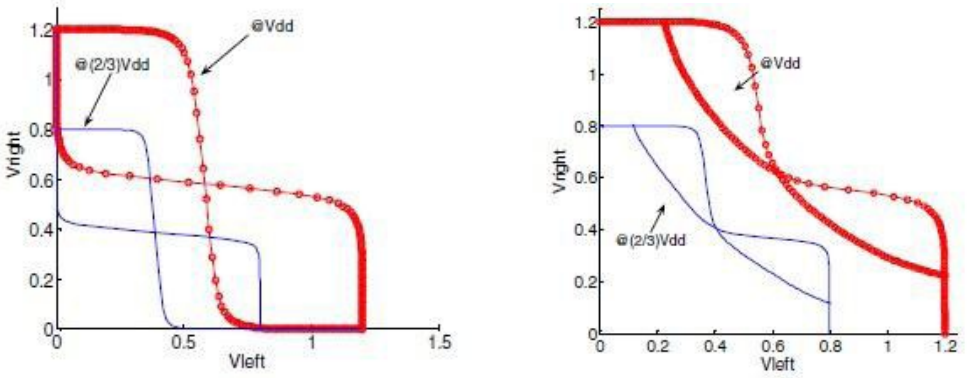
As discussed above, process variations in transistor parameters such as channel length (L), width (W), gate oxide thickness (TOX) and threshold voltage (Vth) have a significant effect on the SRAM Cell functionality, and caused unexpected degradation in yield.

Threshold Voltage (Vth) Variation: Vth variations due to dopant fluctuations, line edge roughness, poly gate grain size variations and systematic variations will greatly reduced the read and write margins of memory cells. If Vth is varied in one of the transistors, it will cause the device mismatch which will directly change the shape of VTC, and thus lead to a significant impact on the SNM. As the driver transistor Vth Variation has the most effect on VTC due to its larger W/L transistor ratio, thus it plays a dominant role in SNM variations. Therefore, Vth reduction in the access transistor of SRAM cell will improve the SNM.

The dopant fluctuation in the channel region will lead to a random variation in the threshold voltage of the SRAM transistor, which acts as a Gaussian distribution. Thus, the randomness of channel dopant distribution will become another major source for the SNM analysis. It is suggested that cell ratios should be increased to gain an acceptable SNM and yield in the future SRAM Cells.

Operating Voltages Variation: variations in power supply voltage (Vdd), bit line voltage(Vbl) or word line voltage(Vwl), will greatly affect the SNM of an SRAM cell Figure 2.6 shows the results of the SNM during hold and read operations with two different power supply voltages Vdd and 2/3Vdd applied to an 6T SRAM Cell with

minimum transistor size. It can be clearly visible that when lowering the supply voltage, it will have lower impact on SNM in both HOLD and Read cases.



(a) HOLD operation (b) READ operation

Figure 2.6: "Butterfly" curve during HOLD & READ operation for different power supply voltages. [37]

The effect of bit line voltage variation can be discussed based on Figure 1.7. The write operation is occupied in the region with the bit line voltage is lower than the write margin. Thus write margin is a crucial parameter to determine the SRAM Cell write stability. In Figure 2.7(b), four regions can be found between ground and precharge points when the bitline voltage increases. Thus balance between bitline voltage variation and cell stability need to be carefully considered.

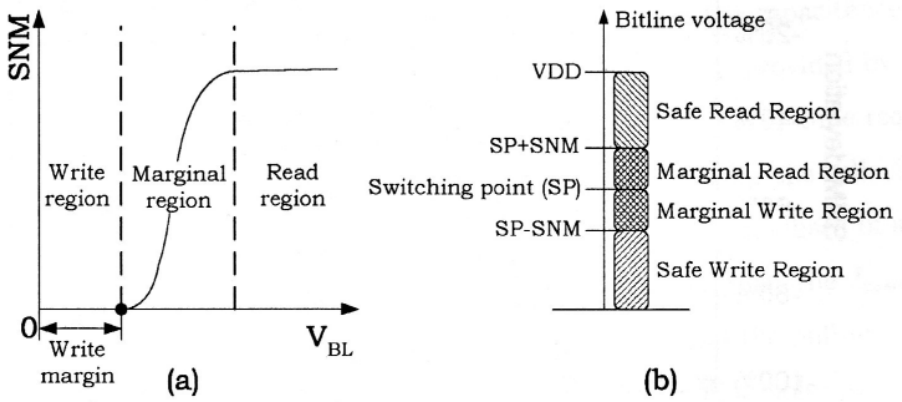


Figure 2.7: Read and Write regions in SRAM Cell [37]

Somehow, in fact, if the transistors are really tiny, the parameters of the transistor will be varied from die to die or even in the exactly same die. Which means each transistor in a die or wafer is totally different. Therefore, the considerations of design based on the nominal models may be wrong because the models are either overestimations or underestimations of real values, so the resultant circuit may not be practical.

In conclusion, with the CMOS technology scaling, process variations are of great concerns during ICs fabrication process as they will degrade the performance of the cell, and thus deviate the designer's original intent based on the nominal models. Therefore, models and methods for dealing with process variations are needed to be carefully investigated for high performance circuit design. In the following part of this paper, we will present the impact of such process variations to evaluate the SRAM Cell's functionality and stability.

2.3 Previous SRAM Cell Design

Different SRAM Cells' structures have been implemented at various technologies to improve the stability and power consumption of the cells. Since in conventional 6T SRAM Cell, the conflicting need of read stability and write ability causes the two conditions cannot be optimized at the same time, hence most of the previous cell designs provide separate read and write port to decouple read and write access. Therefore, the read SNM is increased although need additional transistors which will increase the cell area.

2.3.1 7T SRAM Cell

(i) At 90nm CMOS Technology

This proposed 7T SRAM Cell develops a novel write mechanism to control the feedback connection between the two cross-coupled inverters, as shown in Figure 2.8. An extra transistor N5 is used to switch on or off the feedback connection and the cell relies only on bitline BL_bar during the write operation.

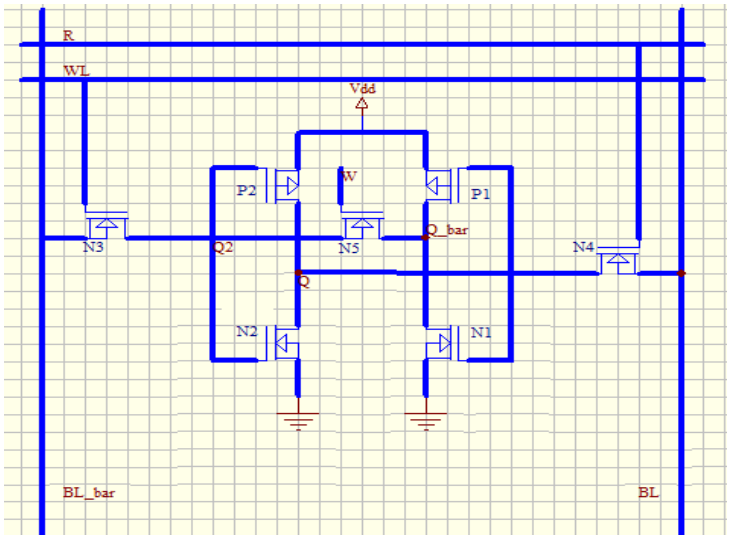


Figure 2.8: 7T SRAM Cell

Upon read and write access, the two bitlines BL and BL_bar are precharged to Vdd. The write operation starts by not selecting write signal (W) which means turning N5

off to disconnect the feedback between the inverters. Then Word line WL is asserted while read signal R is set to “0”, N3 turns on and N4 is off. Since the two inverters INV1 (P1 and N2), INV2 (P2 and N2) are one followed by the other one, BL_bar transfers the complement of the data to node Q2 through transistor N3, the output of INV2 will drive INV1 and then Q_bar is developed. The bitline BL_bar do not need to be discharged for every write operation, since during write “0”, BL_bar is kept to Vdd.

During read “0” operation, as transistor N5 is turned on, the cell totally behaves like the conventional 6T SRAM Cell, the critical path consists of N2 and N4, can be shown in Figure 2.9(a). Whereas in reading “1” operation, the critical path is formed by N1, N5 and N3, as shown in Figure 2.9(b). The three transistors need to be carefully sized to avoid reducing the drive ability of the cell.

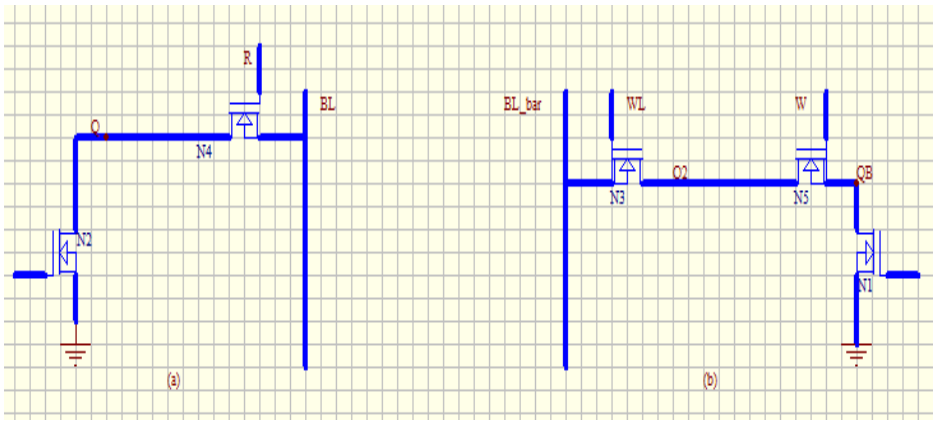


Figure 2.9: Read path (a) Q=”0” (b) Q=”1”

The write power consumption is reduced in this SRAM Cell design as the activity factor of discharging the bitlines is below “1”. Proper transistor sizing will provide acceptable read delay and SNM of the cell. Compared to the conventional 6T SRAM cell, the cell area is increased in this design.

2.3.2 8T SRAM Cell

(i) At 90nm technology

A dual-port cell (8T SRAM Cell) is implemented by adding two transistors to a conventional 6T SRAM Cell, shown in Figure 2.10. The isolation of data retention structure and data output structure means that the cell disturbs during the read operation are significantly eliminated due to the separate read/write bitlines and word lines.

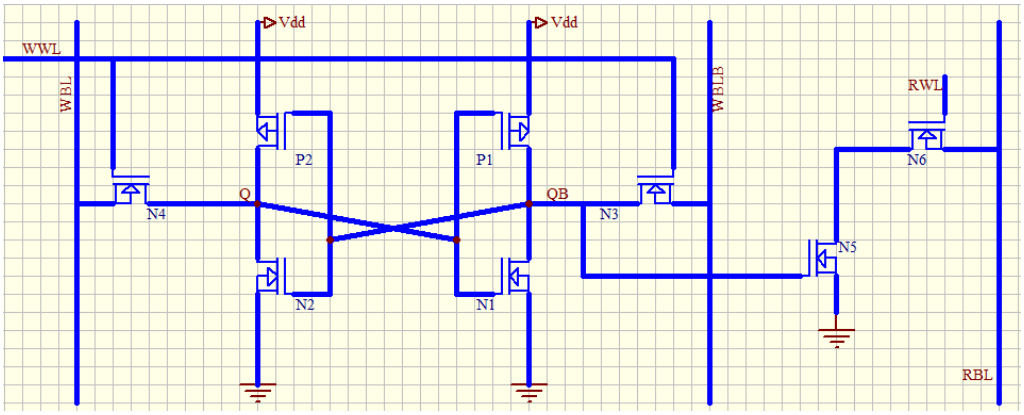


Figure 2.10: 8T SRAM Cell

As shown in Figure 2.10, during the read operation when node Q stores "0" and node QB stores"1", transistor N5 is kept on and RWL is asserted, therefore read bitline RBL is discharged to Gnd through N5 and N6 and data "0" is read out.

This 8T cell design also ensure there is no relationship between the read SNM and cell current Icell. The value of read SNM in this design is increased compared to the conventional 6T cell, but the cell current Icell is not degraded. It is also possible to decrease the threshold voltage of the NMOS transistors to optimize Icell. This 8T cell has 30% area overhead than the conventional 6T cell due to the additional two transistors and contact area of the WWL within a cell.

(ii) At 65nm technology

An ultra dynamic voltage scaling 8T cell is proposed to provide a virtual ground for read buffer of the accessed cell and remain at Vdd for the cells which are not accessed. The MCHd is also a virtual node and its voltage can be pulled down during the write operation in order to weaken the pull-up transistor to improve cell write ability. In addition, low operating voltage at about 420mv can be successfully achieved in this 8T Cell design. The limitations of this cell design are the area overhead and design complexity.

As the read bitline RBL will be precharged to Vdd upon read and write access, thus no leakage current flows in the un-accessed cells and the cell number added to one bitline can be increased. In order to ensure the read buffer sink enough to enable more cells attached to one row, a charge pump circuit is proposed which can be shown in Figure 2.11. Sense amplifier redundancy concept can be used to decrease the sensing error caused by the offset in a given area constraint [16].

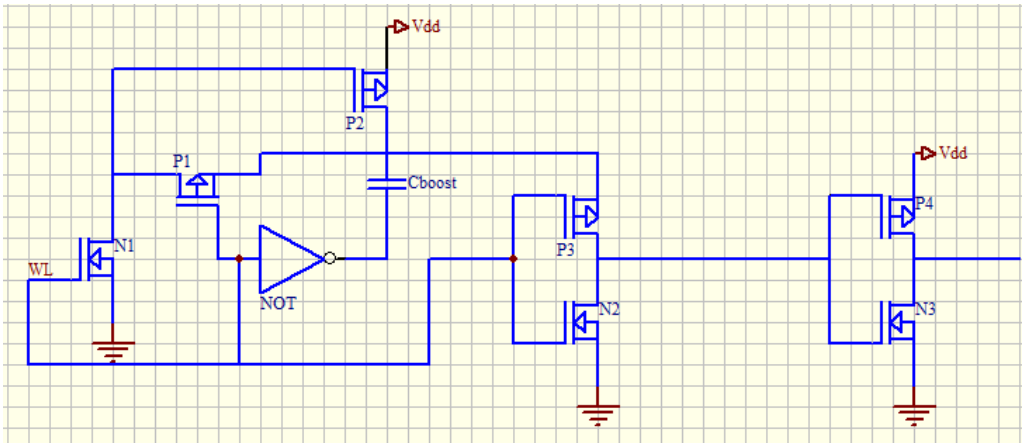


Figure 2.11: Charge pump circuit schematic

(iii) At 45nm technology

In the dual-port 8T Cell design, a precharge circuit must be carried out on the read bitline RBL to ensure RBL can be discharged to Gnd through the two NMOS transistors at the read port when reading "0". Thus there is a certain amount of power consumption during the precharge operation. Besides the precharge circuit, a bitline keeper is required, as shown in Figure 2.12. This bitline keeper scheme will worsen the read out time and make the delay overhead increases when lowering the supply voltage.

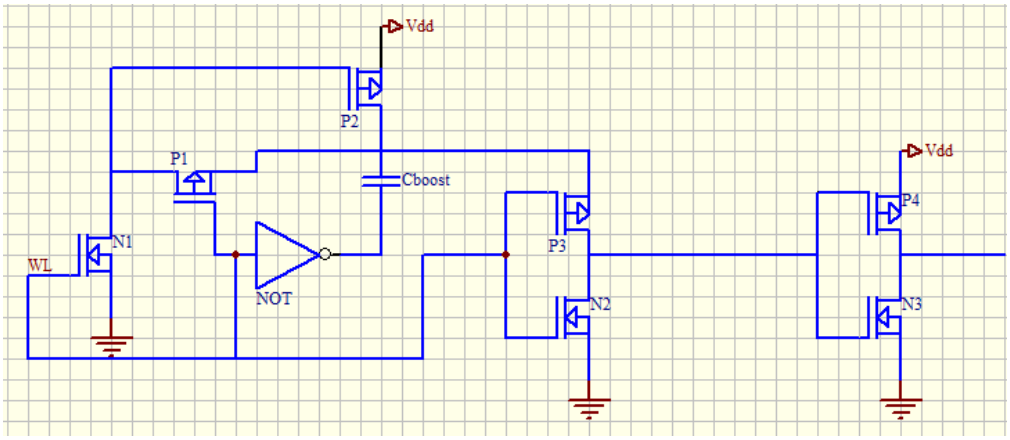


Figure 2.12: Bitline keeper schematic

2.3.3 9T SRAM Cell

(i) At 65nm technology

The 9T SRAM Cell is proposed in order to improve the cell stability and reduce leakage power, as shown in Figure 2.13. This new scheme separates the data during the read access and its read SNM is improved by 2 compared to the conventional 6T SRAM Cell. During the standby mode, this SRAM Cell is in the condition of super cutoff sleep, which makes the leakage power consumption reduced by 22% compared to the conventional 6T SRAM Cell at 65nm CMOS technology.

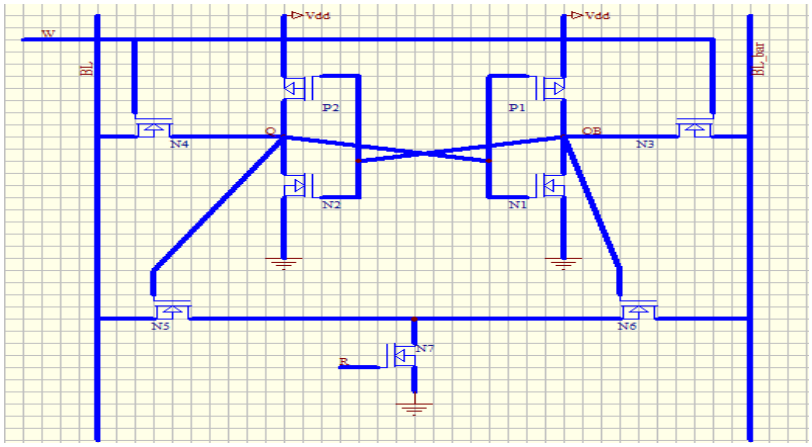


Figure 2.13: 9T SRAM Cell

2.3.4 10T SRAM Cell

(i) At 65nm technology

The dual port 10T SRAM structure can be shown in Figure 2.14. It also consists of separate read and write ports which is able to improve and read stability and write ability simultaneously.

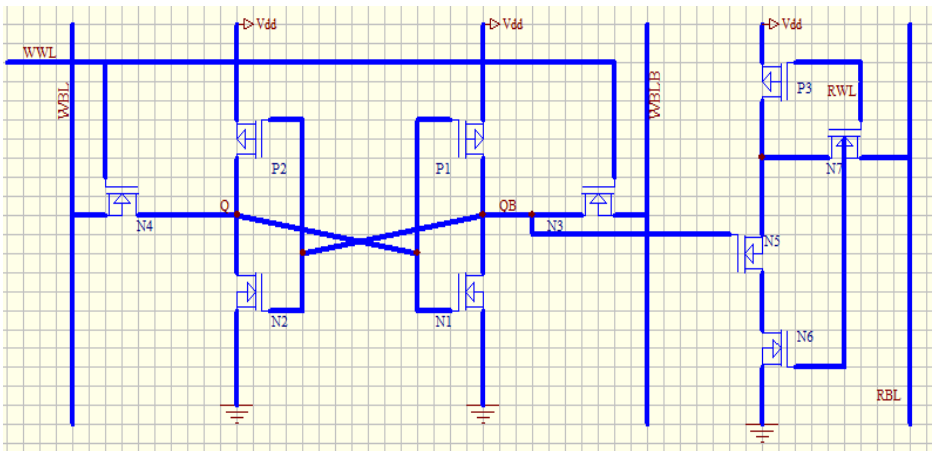


Figure 2.14: 10T SRAM Cell

The write bitilines WBL & WBLB and read bitline RBL are precharged to Vdd upon the read and write access. During read operation, assume that QB stores “1” and Q stores “0”, then RBL will be discharged to Gnd through the read access transistors and data “0” can be read out. Otherwise, RBL will remain at Vdd and data “1” can be read out.

The feature of this SRAM Cell structure is the four decoupled read access transistors. They are implemented in order to enable more cells to be attached to one bitline. Therefore, the leakage current does not depend on the stored data any more. During the standby mode, the drain voltage of P3 is Vdd and the leakage current will flow from the cell to the bitline no matter what the data is. If the cell is not idle and stores data “0”, then the level of RBL is determined by the read current of the cells that have been accessed and leakage current of the other unaccessed cells. If the cell stores data “1”, then RBL will be kept at Vdd. Thus the bitline voltage fluctuating during read process could be able to achieve as possible as 130mV at a 0.2 V supply voltage for a 1k cell bitline. [17].

The main limitations for this design are the area overhead and the cell speed might be scarified in order to maintain the low power consumption.
At 45nm Technology
A 10T SRAM with a single end read bitline, shown in Figure 2.15, is proposed at 45nm technology. It has two additional PMOS transistors and an additional signal /RWL which is reverse to the signal RWL to control the transistor P4 compared to the 8T SRAM Cell design.

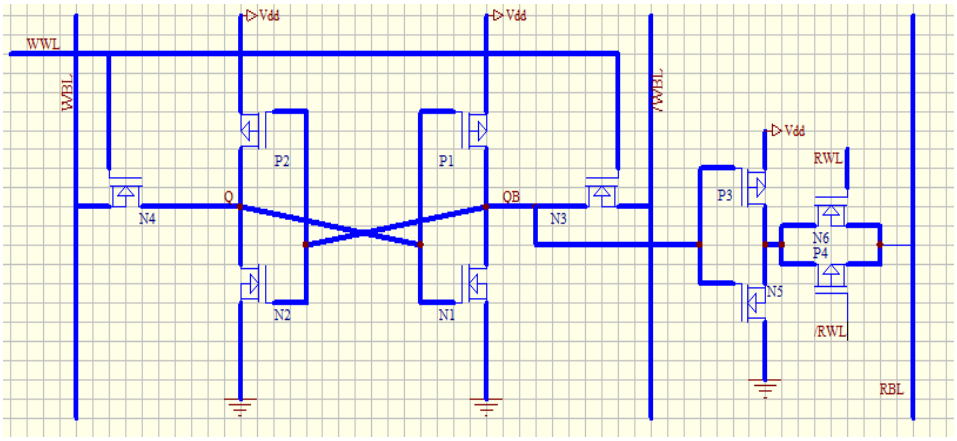


Figure 2.15: 10T Single End SRAM Cell

In this design, there is no need to precharge the read bitline RBL because the inverter at the read port can entirely charge/discharged the RBL. During the read operation, when the signals RWL and /RWL are both asserted, transistors N6 and P4 are kept on. The data on the storage node can be connected to the RBL, thanks to the inverter. A large amount of power can be saved in this design when take the consideration of a sequence of random data in order to keep the transition possibility of the RBL at 50%. Since in these single end read access SRAM Cell design, the leakage current of bitlines will cause the bitline swing reduction. In order to solve this problem, another 10T SRAM Cell with differential read bitlines is proposed, as shown in Figure 2.16.

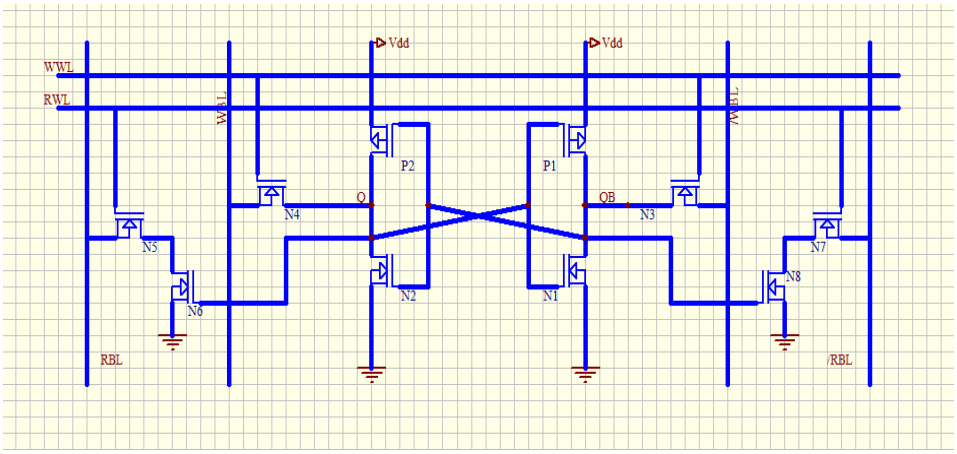


Figure 2.16: 10T Differential SRAM Cell

In this design, four additional NMOS transistors are appended for read bitlines RBL and /RBL compared to the conventional 6T SRAM Cell. The precharge circuits are needed for both RBL and /RBL. During the read operation, RWL is set to high and read bitlines RBL or /RBL will be discharged from the precharged Vdd to Gnd depending on the values at stored node Q and QB.

Since the two write access transistors N3 and N4 are possible to reduce the write ability of the cell if the sizes are improper, A higher voltage 4/3 Vdd has been employed to the gate of these two transistors to minimum the cell area without increasing the sizes of them. The sense amplifier used in this design is replaced by a latch-type sense amplifier in order to minimize the sensing margin. According to [18], this 10T SRAM Cell design can operate properly when the supply voltage is lowered to 320 mV.

Existing SRAM Cell Summary:

In conclusion, the most important part in the existing SRAM Cell design is to improve the read SNM of the cell via different topologies. They use either separate read and write port scheme or enlarge the size of read and write access transistors for higher SNM. The cell can operate properly at the supply voltage as low as 320mV once improving the read SNM. Since the speed of cell is not the top priority in such low power SRAM Cell design, sense amplifiers are not recommended to be implemented. Therefore, an inverter-type read buffer is more desirable to be used to balance the speed of the cell.

2.4 SEU in SRAM Design and Estimation Methods

2.4.1 SRAM Soft Error and Single-Event Upset

In recent years, there has been great interest in discussing about the radiation immunity of electronic circuit. This issue is particularly severe in a modern processor design. Since a great amount of register files/SRAMs will be added in a processor chip, then these devices occupy a large area in the chip and catch a large amount of the particles in radiation condition which may increase the soft error rate of the chip.

Errors existed in the SRAMs can be divided into hard and soft errors. Hard errors are permanent faults which means it cannot be corrected by rewritten [19]. Soft errors are caused by the excess charge carriers due to the external radiations and lead to change the internal data states [20]. The heavy particle striking on the sensitive nodes of the SRAM will cause electron-hole pairs and this ionization impact will lead to the changes on data [20]. Therefore, soft errors will significantly affect the functionality and reliability of SRAMs. The correction of the soft errors can be achieved by rewriting the correct data into the cell to cover the false [19].

If soft error is the main reason that caused the cell reliability reduction, then it can be called as single event upset (SEU) which are induced principally by external radiation due to the high energy neutrons that generated by cosmic rays and alpha particles that generated by packaging materials. [21]. As CMOS technology scales down, SEU can result in a big problem for the system as soft errors are more frequent to occur due to the unsteady isotopes in the packaging material of a chip [22]. Therefore, avoid SEU is vital for progressing the system towards technology scaling.

The mechanism of SEU in SRAM Cell, as shown in Figure 2.17, is the most approved mechanism proposed by Dodd [23]. Assume that node Q is low and node QB is high, then transistors N2 and P1 are turned off, and transistors N1 and P2 are kept on.

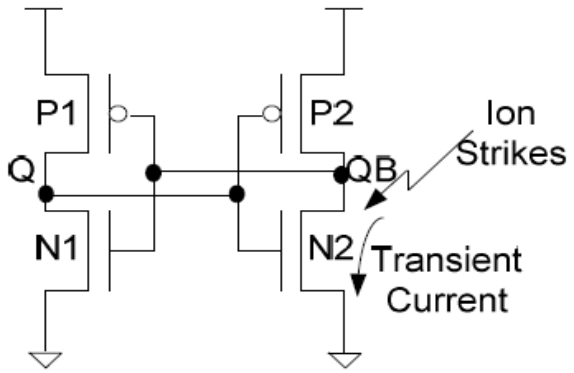


Figure 2.17: Mechanism of SEU in SRAM Cell [38]

During SRAM hold mode, the drain junction of N2 and P1 are the two sensitive locations due to they are in off state. The drain of these off MOS transistors creates the reverse-biased PN junctions and substrates as well, as shown in Figure 2.18, which is easy to be affected by particle strikes. When the particle strikes go through the PN connections, the electrons will pass through the positive voltage of reverse-biased junction and holes move toward the negative voltage side.

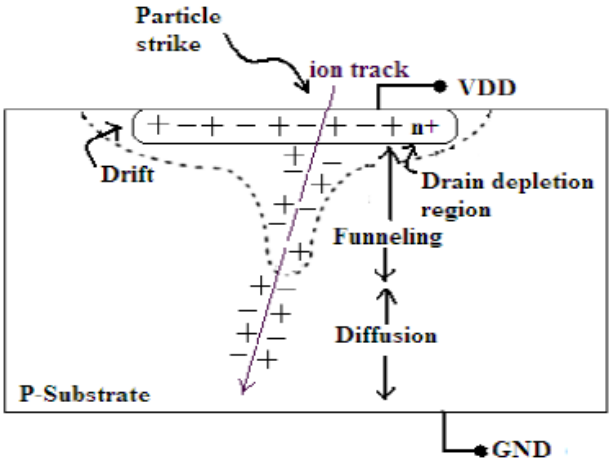


Figure 2.18: Particle strike and charge generation [34]

Suppose that the particle strikes on transistor N2, the movement of charges causes a transient current flowing through the stuck transistor. The source current of restoring transistor P2 is keep trying to balance the particle-induced current. Since transistor P2 only has a finite channel conductance, it will result in a voltage drop at storage node QB. If the voltage drop is large enough to cause the flip of data which means the collected charge exceeds the critical charge. The critical charge is defined as the minimum amount of charge required to upset a circuit node. Therefore, the generation of single-event current transient pulse at the sensitive nodes of the cell causing the voltage transient pulse is actually the mechanism that results in the flip of data in SRAM Cells. Therefore, SEUs in SRAM Cell are always simulated by injecting the current transient pulse at the sensitive nodes of the cell. The shape of the current pulse can be expressed below:

$$I_{\alpha}(t) = \frac{Q}{t_f - t_r}\left(e^{\frac{-t}{t_f}} - e^{\frac{-t}{t_r}}\right)$$

Where Q is the charge collection because of the particle strike, t_r is the rise time and t_f is the fall time.

2.4.2 SEUs Estimation Methods

To achieve SRAM Cell SEU immunity, there have been a number of solutions published [24]. Most of these solutions can be divided into three categories: 1) hardening, 2) recovery, 3) protection.

Hardening technique is proposed by inserting transistors acted as the duplication of the SRAM cell to make the cell is not susceptible to SEUs [25]. The main drawback of this technique is the SRAM area overhead

Recovery technique is implemented by inserting the current monitor to detect SEUs on the fly and mitigate the effects of single event by applying Error Correcting Codes (ECC) or redundancy [25]. However, ECC is possible to cause SRAM area overhead and more power consumption. This technique only allows the errors to be detected and corrected under the reading process of the faulty bit, which leads the delay between the appearance of the SEU and correction. Furthermore, this will produce accumulation of SEUs.

Protection technique uses capacitors connected to the sensitive nodes in SRAM Cell [26]. So when particle strikes on these nodes, the capacitors get charged and absorb the excessive charge. The limitation of this technique is it can only function well for standby condition. While for operating condition, it will affect adversely cell access time.

These drawbacks in the techniques above can be solved by applying Built In Current Sensor (BICS). This technique is considered to be an effective approach to detect the SEUs in SRAM Cell. Traditional BICS [27] are proposed by monitoring the static current consumption in the circuit, as shown in Figure 2.19.

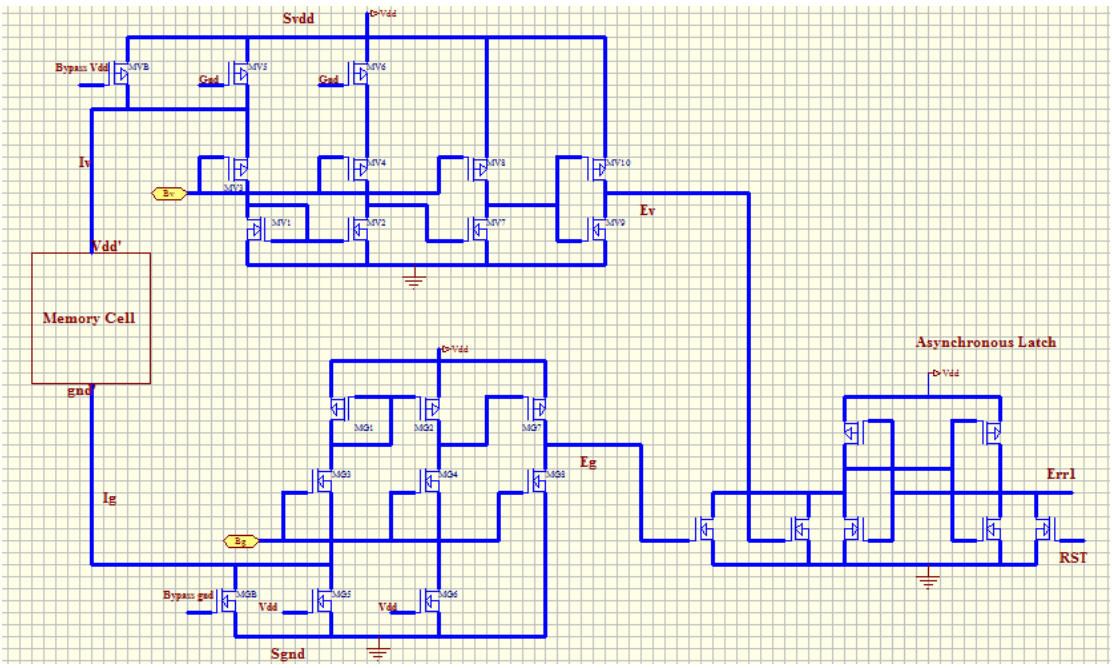


Figure 2.19: Traditional BICS structure

The traditional BICS structure includes two comparators and one asynchronous latch, and each comparator basically consists of two parts: 1) the current mirror, which is used to amplify the upset current; 2) the current source inverter, which is used to convert the amplified current pulse into logic level voltage. In Figure, Svdd is a 1 to 0 data flipping detector, used for observing data changes from 1 to 0 caused by radiation, and similarly Sgnd is used for observing 0 to 1 data changes. Both Svdd and Sgnd generate logic level voltage pulses to indicate data flipping and the two output pulses are connected to the asynchronous latch. The latch will be triggered and the error signal Err1 will be given as high when any of the two outputs goes high. The asynchronous latch could be reset by the reset signal (RST) after the upset is founded and during R/W operation. The reference voltage generator is presented to provide the biasing voltage Bv, Bg for Svdd and Sgnd. This BICS is only capable to detect soft error under standby condition.

It is known that the soft error not only occurs during standby condition, but also occurs in the SRAM Cell during operating conditions. It has been researched that data can flip in SRAM Cell during the read operation or at the end of write access, by injecting a current pulse to model the SEUs strikes [28]. Thus, a more reliable BICS structure should be investigated which is able to detect soft errors at both standby and operating conditions, which will be discussed in the following part of this thesis project.

Chapter 3: Challenges in SRAM design

There are several challenges when the supply voltage is scaled down to sub-threshold region, including the stability of cells, reduced number of cells per bitline and sense amplifier problems. Modern CMOS nanometer technology and supply voltage scalings bring several challenges for future high performance SRAM Cells design. They have a great impact on stability of cells, reduced number of cells attached to one bitline, sense amplifier problems and soft error tolerance.

3.1 Stability of SRAM Cells

When applying the standard supply voltage to the conventional 6T SRAM Cell for different CMOS technology, the SNM can be large enough to make the cell stable and the soft error rate can be acceptable. However, when lowering the supply voltage, especially for scaling down to sub-threshold region, the SNM reduces significantly. It was reported that Vdd cannot be scaled down below 0.7 V for a conventional 6T SRAM to function well in 65nm CMOS technology [30,31]

Table 3.1summarizes the hold SNMs of cell under different supply voltage in different technology [29]. The hold SNMs are 356.2mV, 346.0mV and 335.2mV in 130nm, 90nm and 65nm technologies when the supply voltage is 1V. But when scaling down the supply voltage to 0.4v which makes the SRAM operate in sub-threshold region, the SNMs are reduced to 153.8mV, 148.4mV and 142.5mV respectively. Therefore, It is known that for traditional 6T SRAM, the minimum value of Vdd will not lower than 0.7V for a SRAM to achieve full functionalities in 65mm CMOS technology.

CMOS Technology	Supply Voltage(V)	Hold SNM(V)
130nm	1.0	0.3562
	0.8	0.3019
	0.6	0.2334
	0.4	0.1538
90nm	1.0	0.3460
	0.8	0.2949
	0.6	0.2273
	0.4	0.1482
65nm	1.0	0.3352
	0.8	0.2880
	0.6	0.2218
	0.4	0.1425

Table 3.1: Hold SNM for different supply voltage in CMOS technologies [29]

As CMOS technology scales, the channel lengths of the transistors are variable and to be sub-wavelength of light. This will worsen the process variation problem, as it will be difficult to control the typical 3 σ of the critical dimensions within 10% variation. Since one chip will be made of several billion transistors, some of these transistors may have more than 3 σ critical dimension variation which will mismatch with the others, and hence will lead to the SRAM functional failures and affect SRAM Cell Stability.

3.2 Sense Amplifier Problems

In SRAM design, sense amplifier plays an important role as it affects the cell speed and power consumption of SRAM Cell. Since sense amplifier are always used in SRAM Cell design for fast sensing which typically consists of two matched transistors within a positive feedback environment, it needs to be carefully examined under process variations due to CMOS technology scaling. The process variation leads to mismatch between the pair of sense transistors and hence significant yield loss. It was reported that not all sense amplifiers can function well in a wide supply voltage range and are speedy enough [32]. Although all transistors in these sense amplifiers can work when lowering the supply voltage, the speed of the cell is incredibly lower than which under the normal operation condition.

3.3 Soft Error Tolerance

As technology scales down, process variations will also affect soft error tolerance which will remain a reliability challenge in the future SRAM Cell design. Critical charge in each sensitive node reduces and will cause flip on data more easily. Therefore, the total number of nodes per chip increases which will cause reliability reduction. In addition, with smaller supply voltage applied, the noise margin of the cell is decreased which causes the cell is more susceptible to soft errors.

3.4 Reduced Number of Cells attached to one bitline

The sum of cells that can be attached to one bitline depends on the ratio between the read current I_{read} of the accessed cell and the leakage current $I_{leakage}$ of the un-accessed cells, as shown in Figure 3.1.

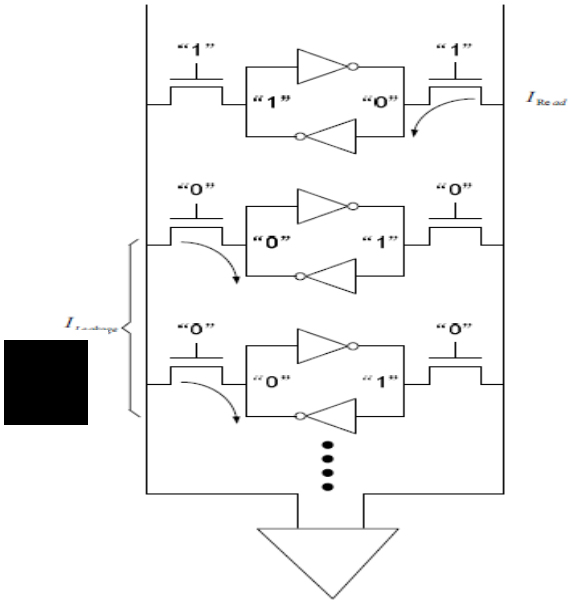


Figure 3.1: leakage current scheme in one bitline [39]

When lowering the supply voltage of SRAM Cell, this current ratio is reduced and hence less cells can be driven to one bitline which will limit the cell density. It has been noticed that most of the 64 cells are be able to be attached to one bitline only if there is no any other technique was employed. This value is too small when compare to more than 256 cells attached to one bitline for most currently available memories in the markets.

Other elements in SRAM such as decoder design, read and write sequences generation circuits, address transient detector, are also needed to be implemented properly under the process variation, although they are not the major concerns of SRAM design compared to the cell and sense amplifier. In conclusion, the design of SRAM will be faced with several serious challenges to achieve no performance penalty and minimized power penalty under supply voltage reduction and process variation.

Chapter 4: Low Power SRAM memory Design

4.1 Overview of the chip design

Figure 4.1 shows an example of the SRAM chip architecture. It consists of row address inputs A0 to A7 and column address IOs A8 to A10, as well as data IOs D0 to D7. WR and RD signals are used to enable the write and read operation respectively.

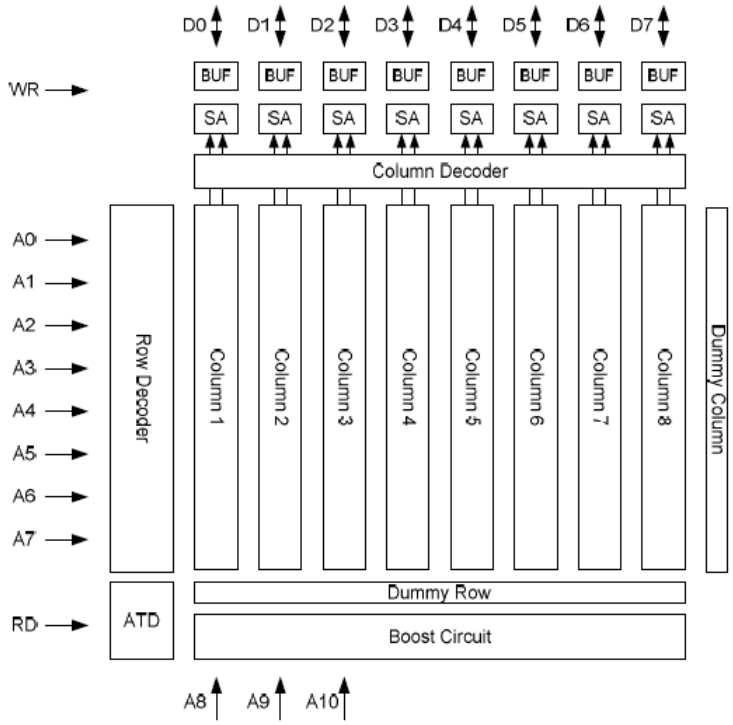


Figure 4.1: SRAM chip architecture [40]

The chip can be divided into two main parts, the memory core and periphery elements. The memory core includes the cell, dummy column and row, boost circuit and sense amplifiers. Their functions are described below:

- Cell: the key component in SRAM design used to store the data. In Figure 4.1, the example SRAM chip contains a cell array with 8 columns, 256×8 bits on each column.

- Dummy Column: This column is designed to produce the activate signal for sense amplifiers. For example, in Figure 4.1, the dummy column contains 256 bits, as well as same capacitance as that in cell array. But the read current is doubled compared to that of cell array in order to generate the Sense Amplifier enable signal.

- Dummy Row: This row is designed to obtain the dummy read wordline signal when the cells in dummy column are under read operation. With this additional row implemented, it ensures that the dummy read wordline have the capacitance as same as that in the cell array of the wordines.

- Sense Amplifier: Latch-type SA with two differential inputs is needed in this SRAM chip in order to amplify the voltage coming off the bitlines. It also helps to decrease the delay times in the chip, as well as power savings.

- Boost Circuit: This circuit is applied to generate the higher voltage to run the write access transistors under write process. It also can raise the input voltage to double of Vdd. For example, the highest allowed voltage in 130nm CMOS technology is about 1.4V, then the maximum supply voltage in this SRAM chip can be reduced to 0.7V with the effect of boost circuit.

The functions of some other important elements inside this SRAM chip can be listed as follows:

- Bitline conditioning circuits: it is used to precharge the bitlines upon both read and write operations.

- Row Address Decoder and Column Multiplexer: Row Address Decoder is used to select a wordline inside the SRAM chip, while Colunm Multiplexer is for connecting selected bitline to the selected dataline. In Figure 4.1, since the chip contains 8 row addresses and 3 column addresses, then an 8-256 row decoder and a 3-8 column decoder are required for this SRAM chip.

- Address Transition Detector (ATD): Address-Transition Detector (ATD) is implemented in asynchronous SRAM to generate a pulse of an expected period on every address transition.

- Data Buffer: Since data bus is bi-directional, the data buffer should be designed to latch the data during the read access and be turned off during the write access.

4.2 Detailed SRAM Design

4.2.1 SRAM Cell Design

A novel 10T SRAM Cell is proposed in this project, shown in Figure 4.2, decouples read and write operation by using the isolated read-port transistors (N6,N7,P3). Therefore, the cell can achieve no constrained read and write stability optimization compared to the conventional 6T SRAM Cell. A cross coupled inverter pair inside this cell is used to store a single bit of data. The write bitlines WB and WBB are used to transfer the data into the cell by the access transistors N3 and N4 during the write operation, while the read bitline RB is used for reading the data from the cell by the read-port transistors during the read operation. In addition, the two separate control signals, read wordline RWL and write wordline WWL, are implemented in this cell in order to manage the read and write operations.

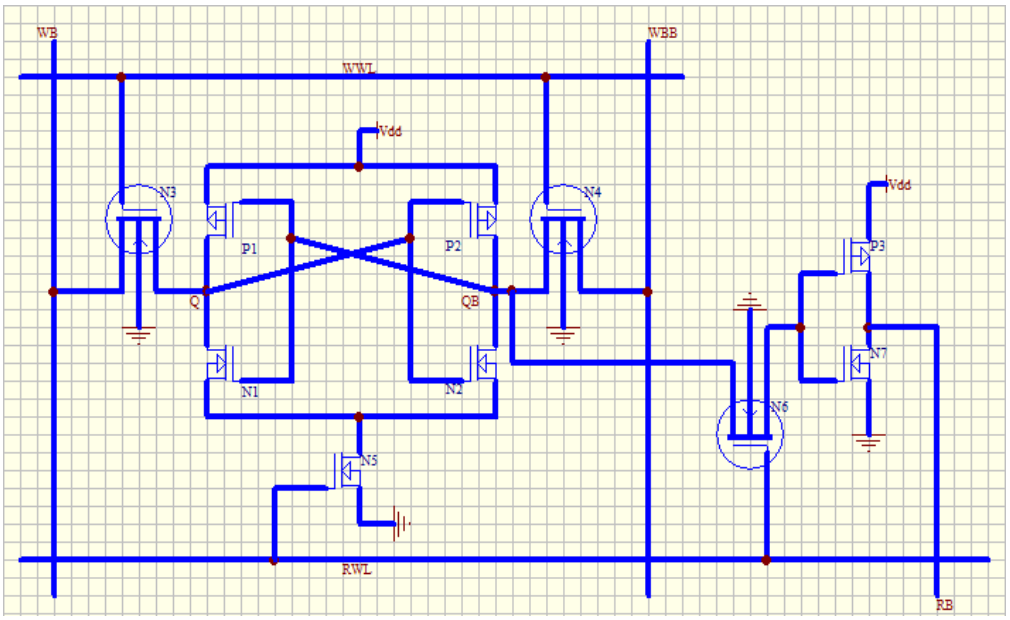


Figure 4.2: proposed SRAM Cell Schematic

Write operation:

A tail NMOS transistor N5 which connected to the pull-down transistors N1 and N2 is used for saving the power during the write operation. Switching activity of this transistor depends on the read wordline RWL. Prior to a write operation, the write bitlines WB and WBB are precharged to Vdd. Initially, assume storage node Q stores data “0”, QB stores data “1”. In a write operation, first drive the data to the write bitline and make read wordline is not asserted so that transistor N5 remains switched off during the write operation by providing a virtual ground. The word wordline is then set to high to turn on both access transistors N3 and N4 which are connected to the word bitlines and thus data can be forced onto storage node Q and QB through the

two access transistors. Since in the conventional 6T SRAM cell, data may get flipped due to the strong storage inverter, therefore we use transistor N5 which is turned off during the write operation to weaken the cell storage and disable the regeneration of data in the normal feedback mechanism, results in improved write ability and speed.

The cell drive current that flows during the write operation and write power are also reduced. This is because the floating ground provided by transistor N5 make the drive transistors (N1,N2) and access transistors (N3,N4) in series, which will result in lower cell current and power consumption.

Read Operation:

Data read out from this proposed SRAM Cell can be implemented by a separate read bitline RB. There is no need to precharge RB before the read operation which can save power during the precharge period and reduce the complexity of precharge structure in a large memory cell array. During the read operation, the write wordline is disabled and read wordline RWL rises from low to high in order to turn on transistor N6. Transistor N5 is also switched on to hold a strong "0" or "1" stored without any disturbance during the read operation. If node QB stores "1", since NMOS transistor N6 is not perfect in passing "1" which results in the source voltage of transistor N4 to below Vdd, therefore, the gate voltage of transistor N7 is decreased and hence reducing the gate leakage. The transistor N7 should be designed with low threshold voltage at the sub-threshold operation. Therefore, read bitline RB is discharged to Gnd through transistor N7 and data "0" can be read out. Alternatively, if node Q stores "0", since NMOS transistor N6 is good in passing "0", RB get charged to Vdd by transistor P3 and data "1" can be read out. Therefore, the separate data retention and data output structures implemented in this SRAM Cell provide no disturbance during the cell read operation and hence improve the cell read stability.

The proper transistor size in this proposed 10T SRAM design is crucial as they will significantly affect the performance and functionality of the cell. If the size has been overestimated, then the valuable silicon material will be wasted, the leakage will be increased, and the switching power dissipation will be worse. Vice versa, if the size has been underestimated, then the speed for either write or read operation would be really delayed due to the growing resistance to ground. Since the role of transistor N5 is only to weaken the cross coupled inverters, thus it can be designed with a minimum size. Two pass transistors N3 and N4 should be strengthen with the minimum sizing storage inverters in order to increase the pull-up ratio and thus improve the write ability and speed. Since the need for lower threshold voltage in transistor N6 primarily depends on the gate oxide thickness. Therefore, the read-port transistors should be provided with minimum dimensions to ensure low resistive path to read current, as well as reduce the cell area overhead.

Since this proposed cell design is implemented by separate read and write ports, it allows the use of a write assist transistor N5 to improve the write ability and speed with lower power consumption during the write operation. Another design feature enables the cell to obtain leakage power reduction in the read operation by using low threshold NMOS transistor N6. As a consequence, this proposed cell design can achieve both read and write power savings, as well as speed and stability separately improved.

4.2.2 Write Driver Design

The SRAM Write Driver is used to rapidly discharge one of the bitlines from the percharge level to ground. Normally, the write driver is activated by asserting a write enable signal and fully discharge the bitlines from the precharge level to gnd. In this SRAM design, we use one of the typical write driver circuits, as shown in Figure 4.3.

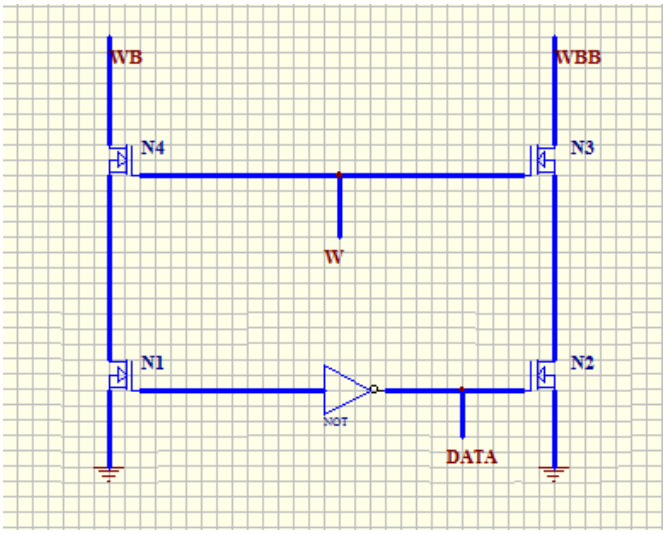


Figure 4.3: Write Driver Circuit Schematic

The write driver presented in this SRAM design consists of a pair of transistors on each write bitline for the data and the write enable signal W. The sources of both N1 and N2 are connected to gnd. The input data will turn on one of the transistors N1 or N2. When write signal W is enabled, transistors N3 and N4 are both kept on, therefore, one of the write bitlines will get discharged from its precharge level to gnd. For example, if input data is “0”, then N1 is turned on and WB is discharged to gnd through transistors N1 and N4. Therefore, data “0” has been applied to WB.

For large SRAM cell array, only one write driver is implemented for each SRAM column, presented in Figure 4.4. Thus, all the SRAM Cell in one column shares one write driver and the entire space of the write drivers is nothing to do with the total amount of the cells in the column and the size could be larger if it is needed.

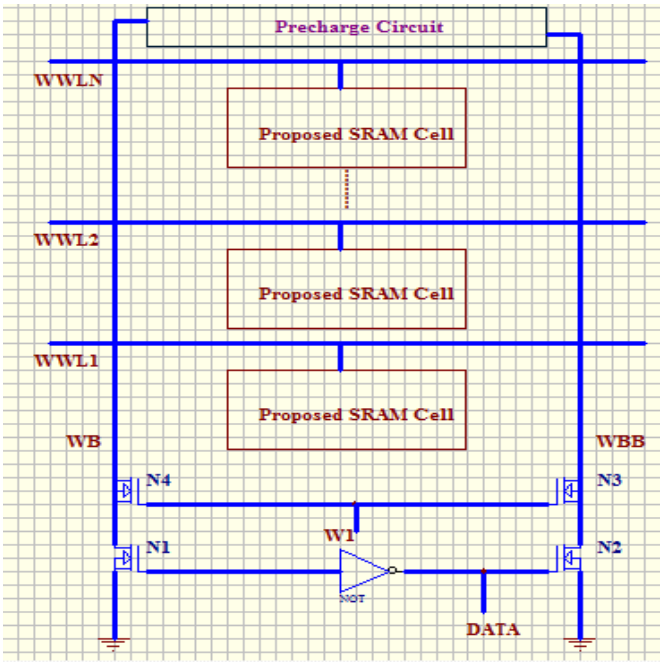


Figure 4.4: Write driver used in large SRAM Cell array

4.2.3 Row decoder Design

The speed of the row decoder has a great impact on memory performance. The decoder asserts the word lines based on the input addresses, it is designed to drive the capacitance of the word lines of the word lines and have high power efficiency. There is only one driver is active at each R/W operation to make the SRAM cells connected to the corresponding word line accessible. For most of the decoder structures, there will be an initial pre-decoder stage, a process which used to decode the group of address inputs to give the pre-decoder outputs. These will be then combined to the next stage either of decoders or the wordlines.

Assume that a SRAM chip has 8 row addresses A0 to A7, thus, an 8-256 row decoder is realized by using two stages implementation to improve the speed and area performance, as shown in Figure 4.5. RD and WR are presented as inputs due to the decoupled read and write operation structure in the proposed SRAM Cell.

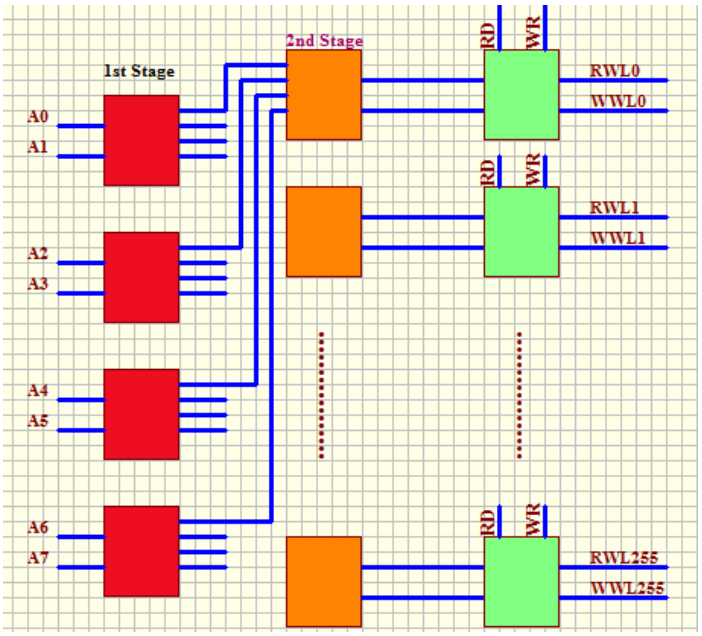


Figure 4.5: Row decoder structure

Although multi-stage SRAM row decoder is quite popular used in large memory cell, for small single block memory, a single-stage row decoder is introduced. The performance related to the delay and power consumption of single-stage decoder can be greatly optimized by applying fast and low power basic gates. Figure 4.6 illustrates the various common used gates configurations.

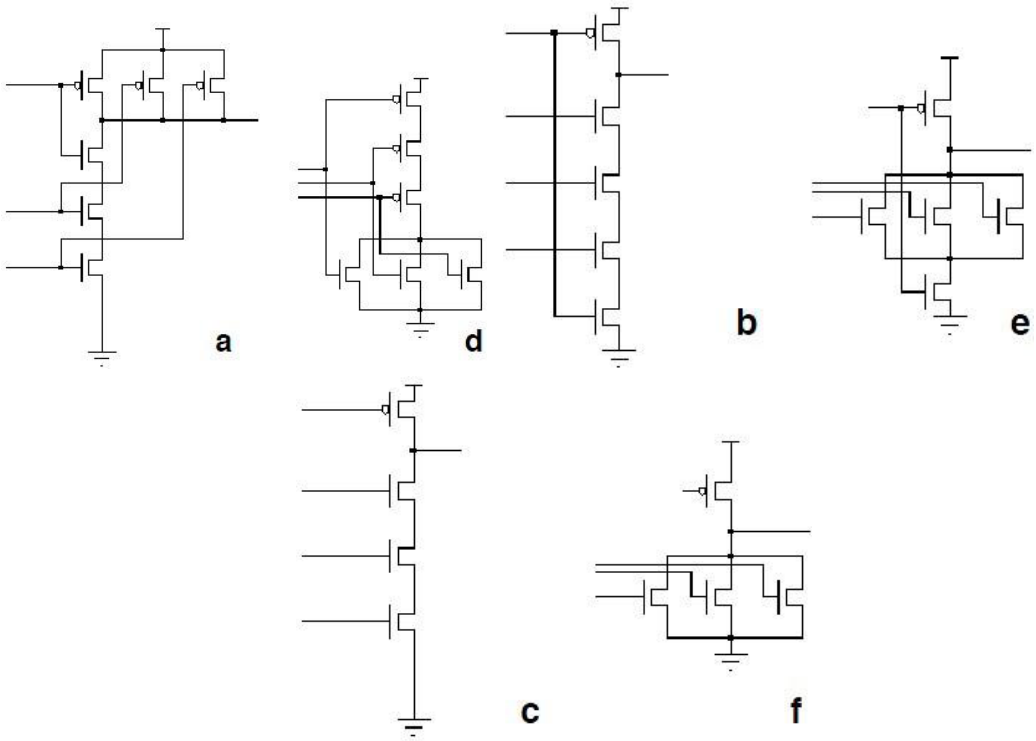


Figure 4.6: Different 3 Input Basic Gates: a) CMOS Nand, b) Dynamic Nand, c) Skewed Nand, d) CMOS Nor, e) Dynamic Nor, f) Skewed Nor. [41]

The simulation results of all gates configurations based on HSPICE software can be shown in Figure 4.7. It could be observed that the Dynamic Nands with shared NMOS and PMOS transistors have the least power consumption as they are part from the direct VDD/GND path all the time, therefore, it is more desirable in single block SRAM decoder design in order to improve the speed and power consumption.

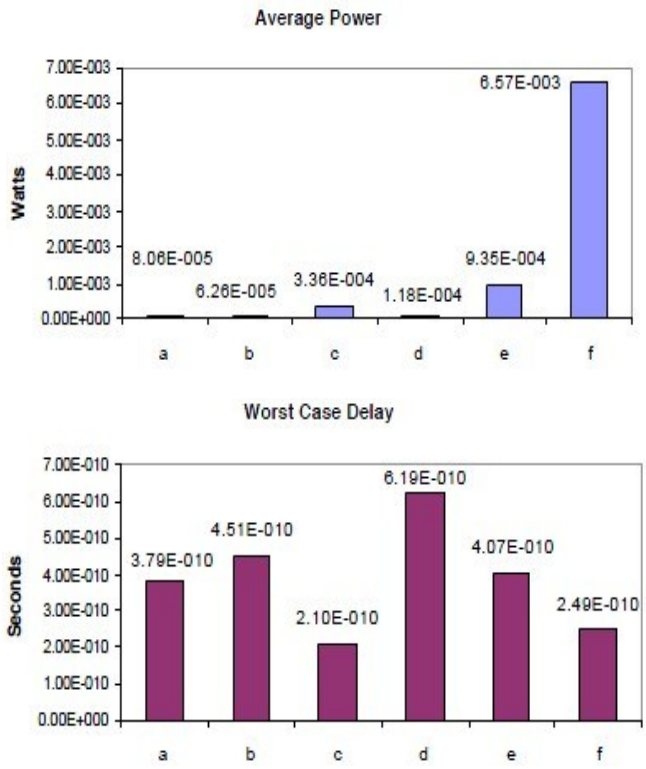


Figure 4.7: Performances of decoder with various gates configurations [41]

4.2.4 Column multiplexer design

The column multiplexer is formed by the pass gates that allows the data to be written into the memory cell or be passed onto the sense amplifier. The circuitry of the column multiplexer could either be wide enough when less resistance is required or small enough to fit the size of the memory cell. Furthermore, the PMOS transistors for the circuits will be used during the data read operation while the NMOS transistors will be used during the date write operation. This set of transistors will be applied to every column multiplexer for each column of bitlines.

In the column multiplexer design, signals could be either generated by a column multiplexers' tree decoder or a separate column decoder. As shown in Figure 4.8(a), signals are generated from the tree decoder, the column address lines enable the pass transistors to let the data being routed through. However, both read and write operations are slightly delayed due to the series pass transistors. Therefore, the increased propagation delay will result in slow usage for large tree-based column multiplexer.

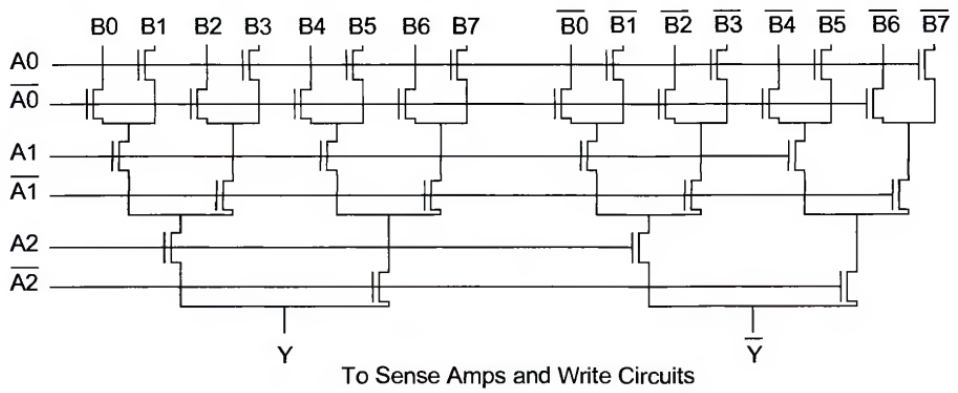


Figure 4.8(a): Tree decoder column multiplexer [44]

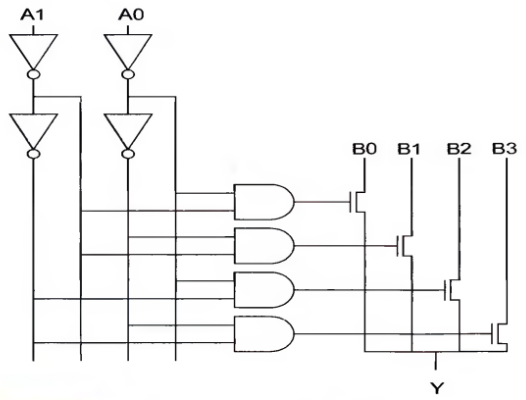


Figure 4.8(b): Column multiplexer with separate decoder [44]

Figure 4.8(b) shows a column multiplexer based separate column decoder. The multiplexer is faster due to there is only one series transistor for the data from bitline to pass thorough. The column decoding is represented in parallel with row decoding which is better than the previous one (tree decoder) as this does not affect delay.
It is easier to employ column multiplexing technique to lay out the sense amplifier since it can expand the bit pitch of each column, and multiple columns are enabled for the remainder of column circuitry after multiplexing. In addition, the number of power-hungry amplifiers required in the array can be reduced by placing sense amplifiers after the column multiplexers.

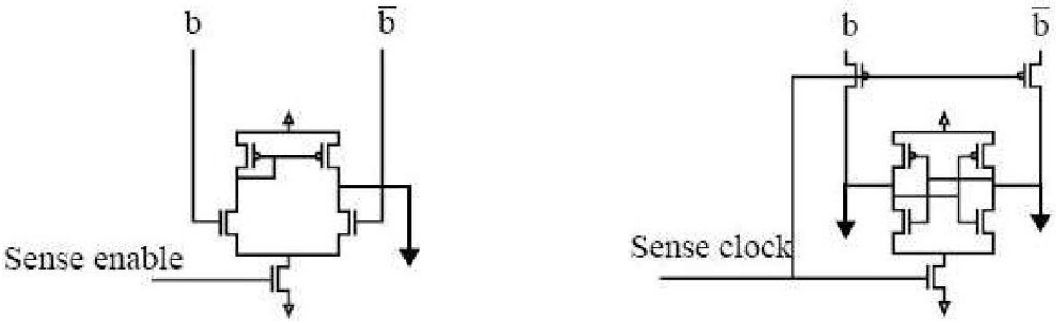
4.2.5 Sense Amplifier Design

Since the memory cells are too weak to discharge the bitlines fast enough, thus the sense amplifier is used to amplify the data of bitlines during the read operation. The bitlines will continue to slew which will lead significant power dissipation due to the large capacitances of the bitlines unless a large differential bitlines is formed between them. So the amount of charge pulled down by the bitlines and the power dissipation could be controlled by limiting the word line pulse width.

For example, the word line pulse width could be maintained to be wide enough for a differential voltage by using external structures like replica bitlines, then the sense amplifiers can read the data reliably.

Figure 4.9 indicates the two different kinds of sense amplifiers: linear amplifier Figure 4.9(a) and latch amplifier Figure 4.9(b). The linear amplifier only consumes biasing power and works under limited supply voltage, these advantages made the linear amplifier are more preferred when the design requires low power and low supply voltage levels.

The latch type sense amplifier consumes the least amount of power. There are two cross coupled gain stages of the sense amplifier and are enabled by the sense clock signal. The negative points of latch sense amplifier is that they might be slower due to some timing margin is necessary for the generation of the sense clock signal. However the sense amplifier could lead to an incorrect output while it is enabled before the differential voltage is formed.



(a) Typical Linear Type Sense Amplifier (b) Typical Latch Type Sense Amplifier

Figure 4.9: Sense Amplifiers [41]

Since the proposed SRAM Cell has separate read and write bitlines, the sense amplifier used in this cell is designed with a static inverter-type read buffer, as shown in Figure 4.10.

a. Read buffer with VGND b. Read buffer with zero ground level

Figure 4.10: Read buffer schemes for sensing [40]

The virtual ground VGND shown in Figure 4.10(a) can be achieved from a dummy column by Replica Technique. It is used to provide lower level than the ground level, thus the trip point of the read buffer can be successfully fixed to the middle of the RBL's high and low levels to improve the sensing margin compared to the conventional read buffer with zero ground level, shown in Figure 4.10(b).

4.2.6 Bitline conditioning circuits design

The bitline conditioning circuitry is designed to precharge the bitlines to high prior to read and write operations. Three different schemes shown in Figure 4.11: (a) a simple bitline conditioner with a pair of PMOS transistors;（b）a weak pull-up transistor based pseudo-NMOS SRAMs where on clock is available;(c)To precharge through NMOS transistors, this technique improve the speed of single-ended bitline sensing as it helps to reduce the swing on the bitlines. On the other hand, this method decreases the noise margins and need more precharge time.

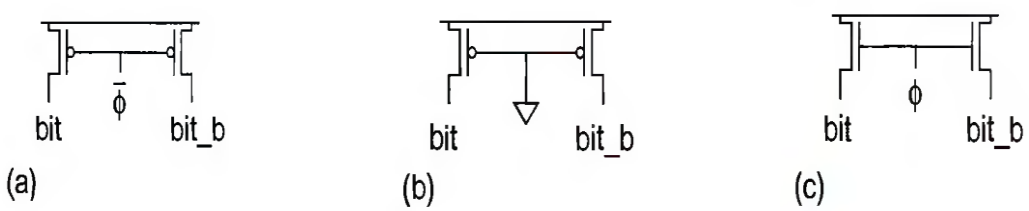


Figure 4.11: Bitline conditioning circuits [41]

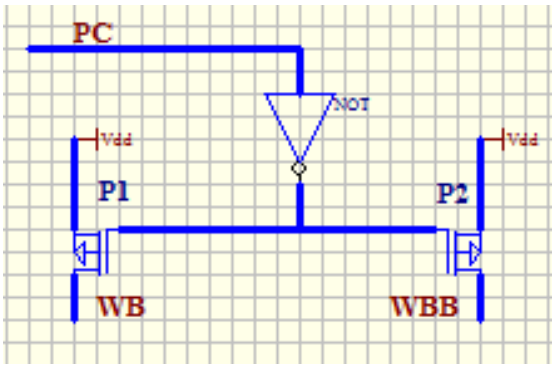


Figure 4.12: Precharge circuit in the proposed SRAM cell

The precharge circuit used in this SRAM design is presented in Figrue 4.12. It uses two PMOS transistors P1 and P2 to drive the bitlines WB and WBB to the precharge level Vdd, since PMOS transistor operates faster than NMOS transistor which can reduce the precharge times. During the precharge operation, the enabled signal PC is set to high which can turn on the two drive PMOS transistors P1 and P2, thus WB and WBB will be precharged to Vdd. Since the size of the two PMOS transistors relates to the recovery speed of the cell, especially critical for the situation that the bitline is discharged after a write operation, thus proper size of the two PMOS transistors should be determined.

4.2.7 Address Transition Detector (ATD) design

In an asynchronous SRAM a read or a write operation is initiated by an address change or chip enable signal, whereas in synchronous SRAMs a read or write operation is initiated by the system's master clock. The terms asynchronous and synchronous relate to the memory-system interface rather than to internal chip operation.

Since the SRAM designed in this thesis project is an asynchronous SRAM. Therefore there will be no external clock signal to generate the read or write control sequences. All the control sequences must come from the signal transient of the input addresses and the read or write enable signals. A typical address transition detector is shown in Figure 4.13, which is desirable to be used in this SRAM design.

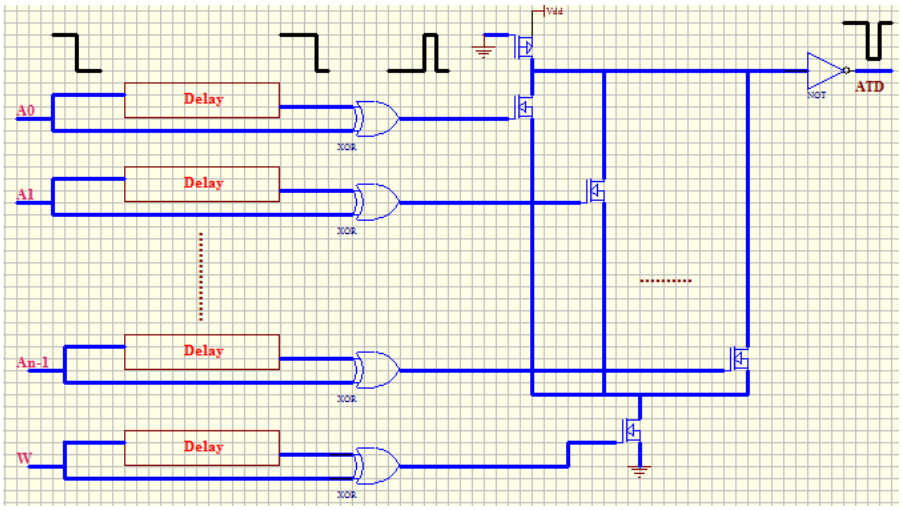


Figure 4.13: Typical Address Transition Detector Circuit

This address transition detector circuit is implemented as a wide-XOR gate comprising a set of delay circuits as shown in Figure. Every transition of address bus A0- A_{n-1} produces a pulse on the output, which initiates a read or a write operation.

During the write operation, when write signal W is enabled, if A0 jumps from "1" to "0", the output of the XOR gate with A0 and delayed A0 inputs will generate a positive pulse. This pulse will turn on one of the NMOS transistors and consequently a negative pulse will be generated at the output of the buffer. The transient waveform can be found in Figure, in which a small PMOS transistor with gate shorted to ground is used as a pseudo resistor. It keeps the output of ATD high while there is no address transition.

The key component in ATD is the delay circuits which generate a proper delay time of the input addressed. There are two main ways to design a delay component in a circuit, including RC delay circuits and inverter chains. In this design, the delay circuit is made of inverter chain with irregular transistor sizing, shown in Figure 4.14

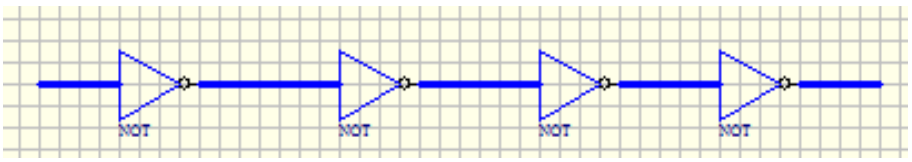


Figure 4.14: Inverter chain based delay circuit

It can generate an approximately 25 ns reading pulse at 0.3 V supply voltage. The small first stage inverter will drive the relatively large second stage inverter (25 times of the first stage inverter). The second inverter can be viewed as a large capacitor due

to its large gate area. The third and fourth stages are used as buffers to obtain steeper signal transient edges.

4.2.8 Input/Output Buffer Design

Since we want to use bi-directional data bus, the data buffer should be designed carefully. It should latch the data in the buffer during read operation and be switched off during write operation. In addition, the buffer should have enough drive capacity to obtain a reasonable speed at lower supply voltages. This concern of sub-threshold drive capacity imposes an additional requirement for this data buffer design. The data buffer used in this SRAM design is shown in Figure 4.15.

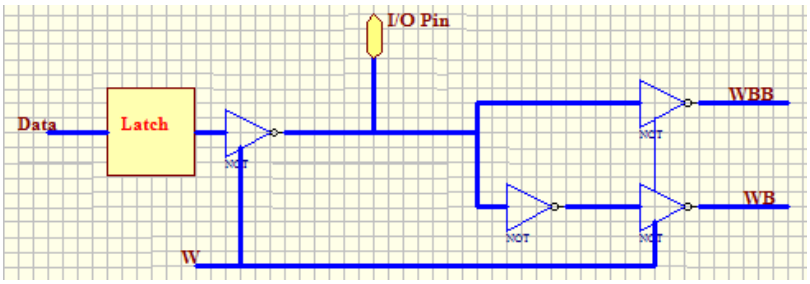


Figure 4.15: Bidirectional data bus

During read operation, W is low, the buffers driving the bitlines WB and WBB are disabled, therefore they can be pre-charged to Vdd. When the sense amplifier is enabled and data is sensed, data will be locked in latch and drive the I/O pin through a buffer. This buffer is used to drive the I/O pad's large capacitance (often several pico-farads) and reshape the output data signal.

4.2.9 SEUs Detect SRAM Model based on BICS technique

Since it has been discussed before, SEUs will occur in SRAM Cell under both standby and operating conditions which will significantly affect the performance and functionality of the cell. The traditional BICS can only detect the soft errors in SRAM under standby condition, therefore, an advanced BICS, proposed by N.M Sivamangai in 2010[34], is implemented in the proposed SRAM Cell which is able to detect soft errors at both standby and operating conditions, shown in Figure 4.16.

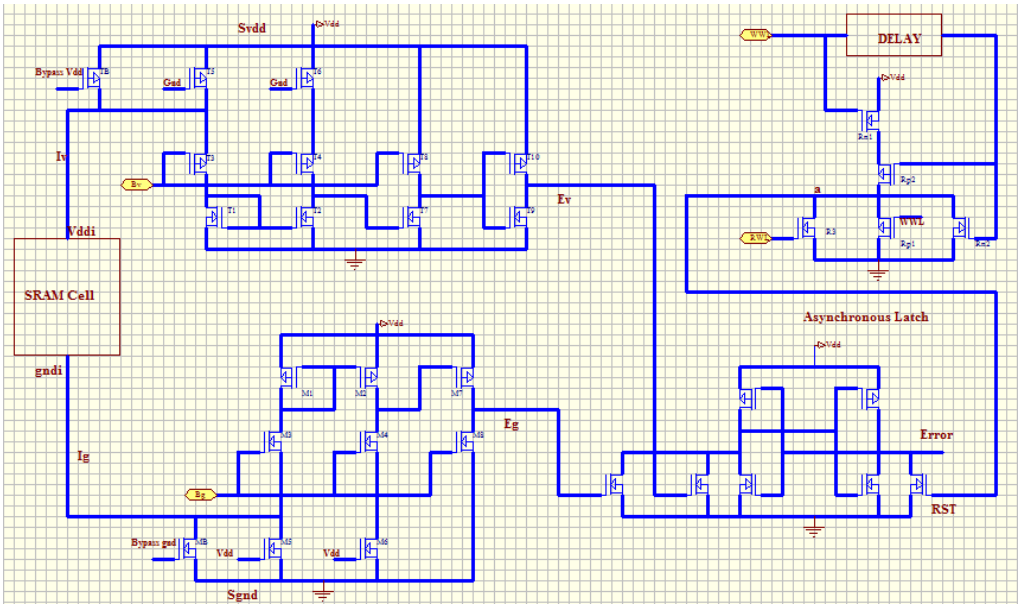


Figure 4.16: Advanced BICS SRAM design

This more advanced structure consists of two comparators and one asynchronous latch. The comparator comprises one current mirror and one current source load inverter. The Svdd part is formed by transistors T1 to T8, where T1, T2 is used as current mirror and T7, T8 is used as current source load inverter. The current mirror has two source transistors T5, T6. Transistors T3, T4 and T8 provide the source current for both current mirror and inverter. All these three transistors are biased according to the reference voltage Bv. It is used to compare the voltage drop on line vddi to monitor 1 to 0 change by applying the three reference voltages to Bv. Similarly, another compartator Sgnd is formed by M1 to M8 with the reference voltage Bg. It is designed to monitor the voltage on line gndi to monitor 0 to 1 flip.The signals Bypassvdd and Bypassgnd are presented to provide vddi and gndi to the memory column of SRAM array under read and write operation of the memory.

The feature in this advanced BICS design is the additional logic circuitry with delay element being employed to enable the BICS operation under operating process. The reset control circuit is formed with one delay element and the transistors Rp1, Rp2, Rn1, Rn2 and Rn3 as shown in figure 8. The write wordline WWL is acted as the input to the delay element and read wordline RWL is connected to the gate of the transistor R3. The WWL will be delayed by the delay element when it is enabled under write condition. Buffer can be used as the delay element in order to generate the expected delay. The required delay could be 8.5 ns if the write time is assumed to be 10 ns, then the required delay can be generated by the buffer in such a way that the reset signal being activated for first 8.5 ns under write access. After that, the delayed signal is transferred to the transistor Rp2, Rn2 and the WWL will be transfer to Rp1, Rn1.

During SRAM Cell standby condition, WWL is not enabled which turns on transistor Rp1, therefore node a is discharged. Reset signal goes to low which makes the BICS work, and error signal will be generated if any soft error occurs in the cell. During the SRAM Cell read operation, WWL and RWL signals are both set to high, thus transistor R3 is kept on. Node a is get discharged and reset signal remains at logic 0, so the BICS is able to generate error signal under read operation.

In a SRAM Cell write operation, WWL is enabled and RWL is disabled, the delay output will keeps at logic 0 for the first 8.5ns, switching on transistors Rp2 and Rn1 to charge node a to Vdd. Therefore, reset signal goes high and the BICS will be disabled during the first 8.5ns. After that, WWL signal becomes high for the last 1.5ns and node a is discharged forcing the reset signal low. Therefore, it allows the BICS to operate at the end of write operation.

The transient current pulse will be generated at the struck node when a particle hit the drain of the OFF NMOS transistor. The current flowing from Vdd to the struck node through the ON PMOS transistor forces the current flowing through either T1 or T2 get reduced. This will lead the rise of voltage drop from the drain to source of the transistor T2. According to the connection between the drain of the transistor T2 and the gate of the transistor T7, the gate to source voltage of T7 will be raised. Thus a voltage pulse at the drain of T7 is generated due to the increase of the gate to source voltage. The transistors T9 and T10 is designed to amplify and reverse this voltage to make full logic value at node Ev. Similarly if the particle hits at the drain of the OFF PMOS transistor of the cell then the voltage drop will be generated by Sgnd at node Eg. Since the outputs Ev and Eg perform as inputs to the asynchronous latch, the latch will be activated to generated the error signal (Error) high when any of the two outputs goes high.

In conclusion, this advanced BICS design is able to detect SEUs in the SRAM Cell happened at any instant of time at both standby and operating conditions due to the delay block and generated reset signal. As a consequence, the BICS technique is quite an effective way to detect fault tolerance in SRAM Cell design under radiation environment.

In this chapter, an overview of the main SRAM blocks is presented. A 10T SRAM Cell is proposed, and the cell performance and stability are improved compared to the conventional 6T SRAM Cell. We also discussed the several types of write drivers, row decoder and column multiplexer strategies, sense amplifier design, Input/Output buffer design and address transition detector used in asynchronous SRAMs. Some of the discussed circuit techniques have been implemented in this proposed SRAM design. Advanced BICS technique used in this SRAM design can effectively detect the SEUs occurred at any instant of time at both standby and operating conditions. The following chapter will test this proposed SRAM cell performance and Cell self – SEUs-detect ability.

Chapter 5: SRAM Cell Design Simulation

5.1 Simulation techniques

5.1.1 Monte Carlo method

Monte Carlo simulation is a method that usually used in complex systems to evaluate a selected model through a couple of random parameters. In this thesis project, with the need to evaluate the impacts of process variation in SRAM Cell, Monte Carlo simulation using statistical models is required. The flow chart of this method is shown in Figure 5.1.

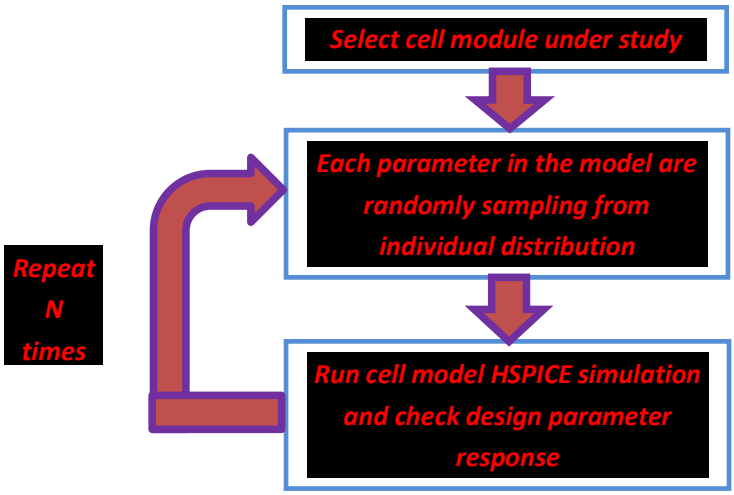


Figure 5.1: Monte Carlo method flow chart

The first step for this approach is to choose a specific cell module under simulation. The next step is to select the parameters inside the model and each parameter is randomly sampled using a certain specified probability distribution. And the third step is to perform cell model simulation once and check the design parameter response. Repeat step 2 and 3, and finally aggregate the response of each computation into the final results.

5.1.2 Gaussian distribution

Since the design parameter used in Monte-Carlo analysis are randomly generated from probability distribution, a proper distribution should be chosen for the parameters that can most closely models the random variation.

In this project, the Monte-Carlo analysis in circuit design will use Gaussian distribution for each design parameter to characterize the process variation (the Vth fluctuations of each transistor, etc.). This leads to the design parameter will be varied around the average of the distribution. The Gaussian function can be expressed as follows and its characterization bell curve is shown in Figure 5.2.

$$f(x) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}$$

where parameters μ and σ^2 is the mean and the variance respectively. The distribution with $\mu = 0$ and $\sigma^2 = 1$ is defined as normal operation.

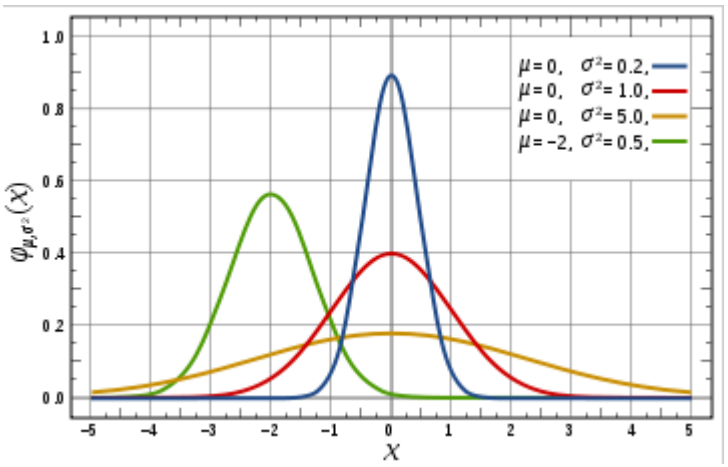


Figure 5.2: Gaussian Function curve [42]

From Figure 5.2: it can be seen that the shape of Gaussian Function is varied around the peak at the mean. In statistics, the three-sigma rule used for standard normal distribution operation, that can include almost all values plotted within 3 normal deviation around the mean, as shown in Figure 5.3.

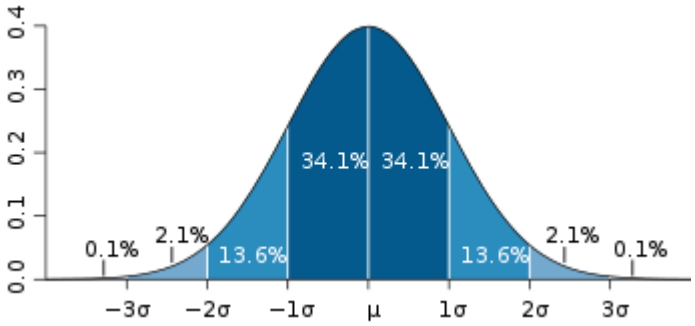


Figure 5.3: 3 sigma role in Gaussian normal distribution [42]

In this project, the design parameter variations inside the SRAM Cell will be generated by Gaussian normal distribution within 3 standard deviation of the mean $\mu \pm 3\sigma$ to estimate the effect of process variations on the cell.

5.2 Simulation Setup and Environment

Different SRAM Cell circuits designed with the minimum transistor size will be simulated by HSPICE and MATLAB simulation tools. The CMOS transistors SPICE models used for the simulation are gained from the Predictive Technology Model (PTM) [45] website in different nano-technologies.

Variable Parameters inside this cell are set to be threshold voltage (Vth), channel width (W), channel length (L), gate oxide thickness (tox) and supply voltage (Vdd). All variable parameters are being applied with 10% variation with a deviation of 3σ unless particularly specified and assumed to be independents of each other. Simulation temperature is held at $25^{o}C$, thus temperature variations will not be discussed in this paper and design parameter response (power, write/read time, etc.) will be analyzed.

5.3 SRAM Cell Function Test

The proposed SRAM Cell is simulated by using HSPICE and MATLAB tools under various different CMOS technology. Simulated results are compared with the existing 6T, 7T, 8T, 10T SRAM Cells. Monte Carlo analysis will be employed to examine the impact of process variation on the power, stability, read and write time of the different individual SRAM cell.

5.3.1 Write and Read operation test in Proposed SRAM Cell

65nm CMOS Technology

Cell Model: Proposed 10T SRAM Cell

Simulation type: HSPICE simulation transient analysis

Simulation time: 0 to 1000ns

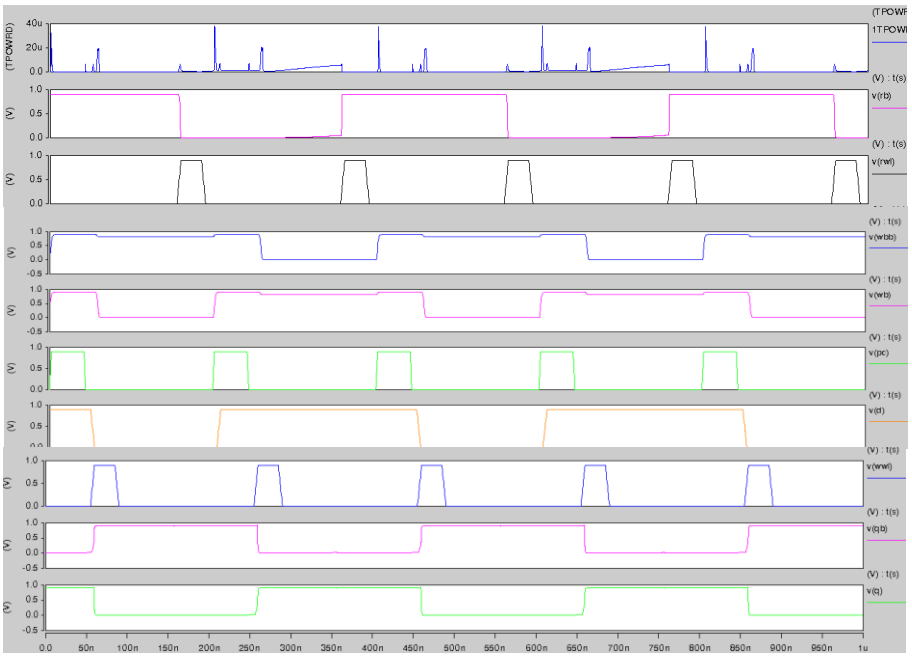


Figure 5.4: Proposed 10T SRAM Cell operation waveform

The transient waveforms of our proposed 10T SRAM Cell during the read and write operation in 65nm CMOS technology is shown in Figure 5.4. During write “0” operation, when write word line WWL is enabled, the state of Q and QB changes to “0” and “1” respectively, which can indicate that the write operation is working properly as the content of the memory has been updated. Ideally, after the write operation, the logical values on WB and WBB should matches with Q and QB respectively. The mismatch existed in this experiment is caused by dynamic energy

consumption in charging and discharging write bitlines. In the reading "1" cycle, when the read wordline RWL is asserted, the data"1"can be read out from read bitline RB. The writing "1" and reading "0" work similarly to the writing "0" and reading "1" operations. Therefore, data can be successfully written into this proposed cell when WWL is enabled and also can be read out from the read bitlines RB when RWL is asserted.

In Figure 5.4, during the write operation, only a small swing of bitlines occurred in our proposed SRAM Cell instead of full swing bitlines in the conventional 6T SRAM Cell. Therefore, very small voltage swings on bitlines will lead to a significant reduction of the active power in the SRAM Cell as we expected, because the active power is mainly consumed by charging and discharging of the highly capacitive bitlines.

5.3.2 Power and delay comparison for different cells

45nm CMOS Technology

Cell Model: 6T, 7T, 8T, 10T and Proposed SRAM Cells

Simulation type: HSPICE simulation transient analysis

Simulation time: 0 to 1000ns

Figure 5.5 shows the comparison of average power consumption, read and write time in the case of 6T, 7T, 8T, 10T and proposed SRAM Cells. The read time is calculated when the read wordline RWL rises to half Vdd, to a time when the output voltage of read bitline RB is reached to half Vdd. Similarly, write time is the amount of time that taken to change the output of either Q or QB to half Vdd when write wordline WWL rises to half Vdd. Our proposed SRAM Cell achieves about 80% power savings compared to the conventional 6T SRAM Cell. This power reduction is primarily caused by the small swing bitline scheme using a tail transistor N5 to provide a high resistive path to the current flow and decrease the leakage during the write operation.

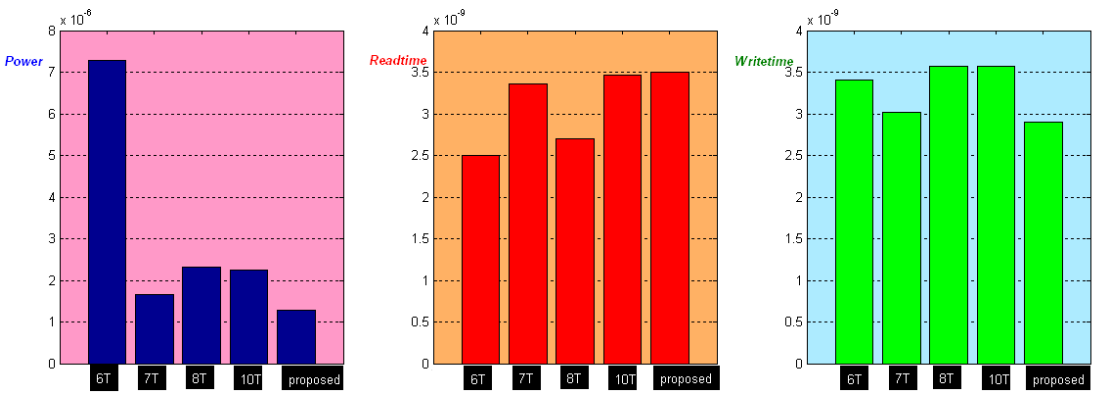


Figure 5.5: Average power & read and write time in different SRAM Cells

The read time of our proposed SRAM Cell is 40% higher compared to the 6T SRAM Cell because of the low cell read current that causes longer time to discharge the read bitline, while the write time is 17% accelerated due to the extra tail transistor N5 connected to the pull down transistors which will weaken the storage inverters in the cell. The write time can be improved if increasing the power supply on write wordline WWL or enlarging the size of transistor N5.

5.3.3 SNM measure in different SRAM Cells

45nm CMOS Technology
Cell Model: Conventional 6T SRAM Cell, Proposed SRAM Cell
Simulation type: HSPICE simulation DC analysis
Simulation time: 0 to 1000ns

Static noise margin (SNM) is often used as a metric to evaluate the stability. In order to calculate the SNM of the SRAM Cell, butterfly approach is implemented.
Figure 5.6 illustrates the butterfly curves of both conventional 6T and proposed 10T SRAM Cells with no variability. Conventional 6T SRAM Cell provides a SNM of 0.095 for a 0.7V power supply whereas the proposed cell achieves a SNM of 0.246 for the same supply voltage, provides 158% read stability improvement. Thus, a big tolerance can be indicated to compare with the read failures for the advanced design as the storage nodes Q and QB are difficult to be disturbed under a read process.

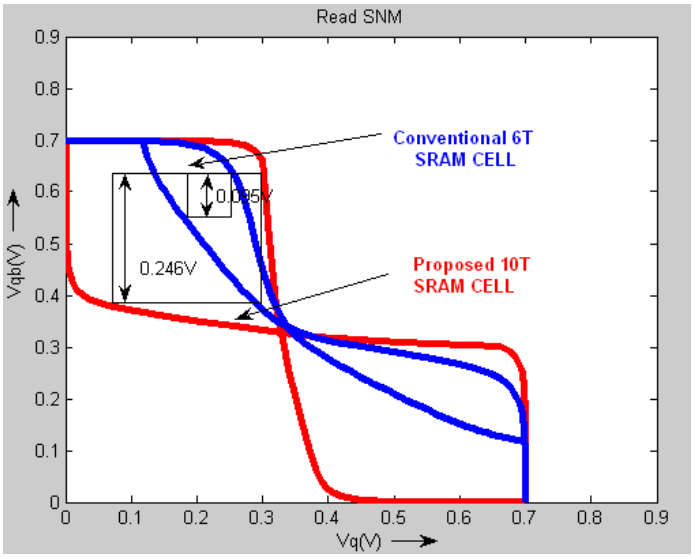


Figure 5.6: SNM in 6T and Proposed SRAM Cells

This SNM enhancement in the proposed SRAM Cell results in increasing the expense due to the additional transistors compared to the conventional 6T SRAM Cell.

However, the device variation will cause further reduction of SNM in the conventional 6T SRAM Cell which can be compensated by increasing the cell ratio to enhance the read SNM and thus significantly increase the cell area, whereas the proposed SRAM Cell can provide a significant SNM enhancement without any transistor size changing.

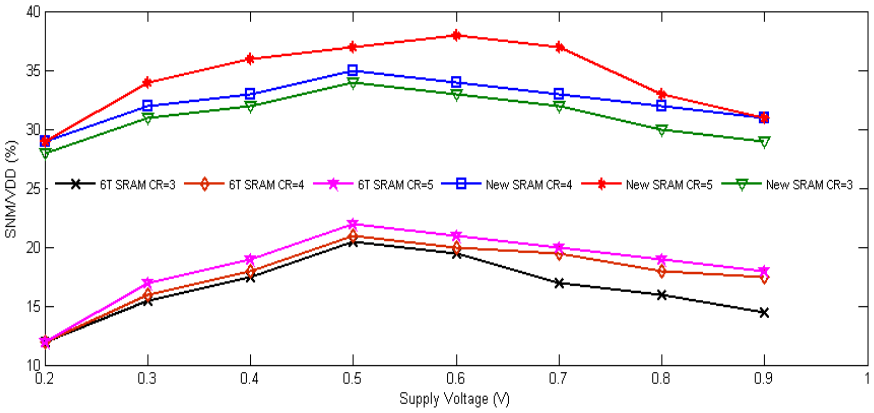


Figure 5.7: SNM against supply voltages in different CR

Figure 5.7 shows that increase the cell ratio CR will provide a great SNM improvement in both conventional 6T SRAM Cell and proposed 10T SRAM Cell owing to the liner relation between sizing of the transistor and transistor drive current. However, when lowering the supply voltage, increasing the CR would not be an effective method to provide large SNM for future technologies. Because of there is a linear relation between the transistor drive current and the sizing, which just as opposed to a quadratic or exponential dependence on supply voltage. SNM is reduced at a ultra-low power supply, thus, the use of sizing transistor in SRAM design becomes less effective.

5.3.4 SRAM Cell performance testing under process variation

i) SRAM Cell simulation results under Vth variation

45nm CMOS Technology
Cell Model: Conventional 6T SRAM and Proposed 10T SRAM Cells
Variable Parameter: Threshold Voltage Vth with a deviation of 3σ variations
Simulation Type: HSPICE simulation DC analysis, sweep monte = 100
Simulation time: 0 to 1000ns

In order to investigate the process variation effect on the SRAM Cell, 10% variation is applied in threshold voltage Vth with 3 σ deviation, acted as an independent random variable for all the transistors inside SRAM cell with a Gaussian distribution. From Figure 5.8, it can be observed that the read SNM of both conventional 6T and proposed 10T SRAM Cell is degraded compared to the normal SNMs in Figure owing to the Vth variation. The read SNM of conventional 6T SRAM Cell is reduced up to 45%, whereas in the proposed design approximately 15% SNM reduction, so conventional 6T SRAM cell is more susceptible to process variation.

Therefore, the 10% Vth variation to the transistors results in small box inside the conventional 6T SRAM cell butterfly curves. Whereas for the proposed SRAM cell, the same Vth variations lead to small effect on read SNM which can be tolerated by the cell. In addition, the proposed 10T SRAM Cell also can achieve 2.6 times higher read SNM as compared to the conventional 6T SRAM cell under the same Vth variation. Thus, the proposed 6T SRAM cell provides better read stability and is process variation tolerant.

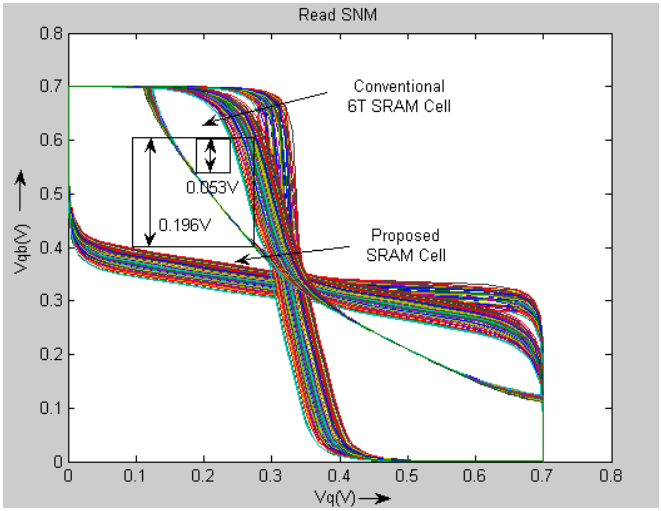


Figure 5.8: Read SNM under Vth variation in different cells

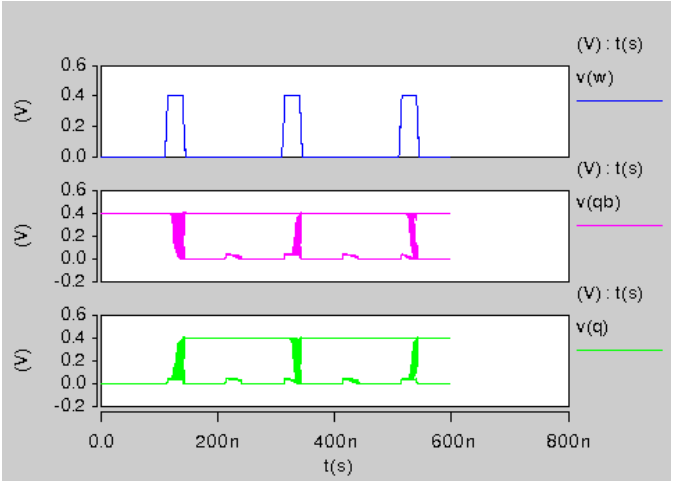


Figure 5.9: Write Ability under Vth variation in the conventional 6T SRAM Cell

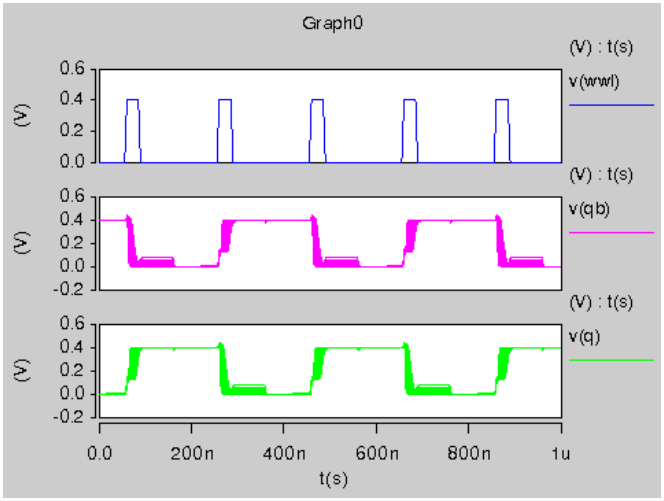


Figure 5.10: Write Ability under Vth variation in the proposed 10T SRAM Cell

Since the 6T SRAM Cell can not function well at a lower supply voltage due to the insufficient noise margin, thus in order to evaluate the write ability under the process variation of both conventional 6T and proposed SRAM Cells, Monte Carlo simulation with 10% Vth variation is applied to both the cells using PTM-45nm models at a supply voltage of 0.4V. As it can be observed in Figure 5.9 and Figure 5.10, the Vth variation in the 6T SRAM Cell causes the write failures as the data on storage node Q and QB in some cases has reached the same level, which violates the principle of the write operation. Whereas in the proposed cell, it can achieve a stronger write ability although the data on node Q and QB slightly varied during the write operation which is caused by the Vth variation.

ii) SRAM Cell simulation results under supply voltage variation

Different CMOS techniques
Cell Model: Proposed 10T SRAM Cell
Variable Parameter: Supply voltage Vdd
Simulation Type: HSPICE simulation transient analysis and dc analysis
Simulation time: 0 to 1000ns

Lower supply voltage is considered to be one of the most effective way to reduce the power consumption in the SRAM cell design in order to pursue ultra-low power operation. Thus, to carry out a comparative analysis of the power in various SRAM Cells, we uses the PTM-45nm device models for all the cell designs. Figure 5.11 illustrates the simulated power consumption under different supply voltage in various SRAM cells. When lowering the supply voltage from 1.4V to 0.4V, the average power consumption in all SRAM cells are significantly reduced and the proposed 10T SRAM cell always achieves the lowest power dissipation at different supply voltage

due to the floating ground that leads to the cell current reduction and the single ended read circuitry used to allow no precharge for the read bitline.

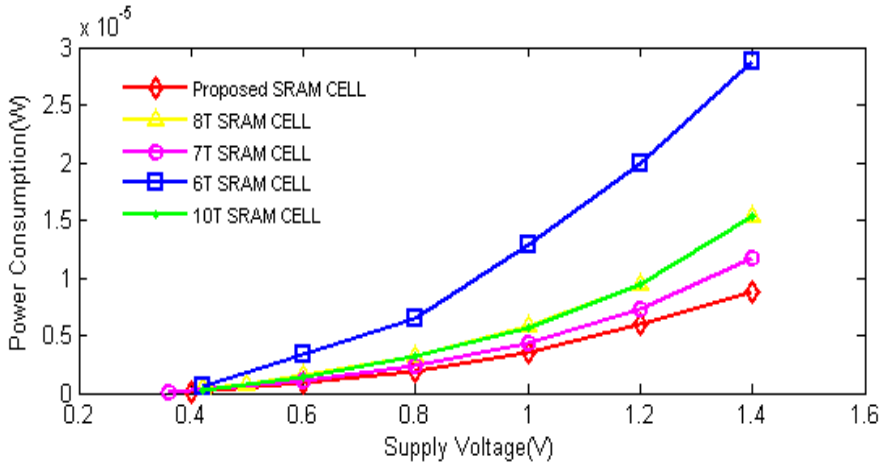


Figure 5.11: Power Consumption in various SRAM cells under Vdd variation

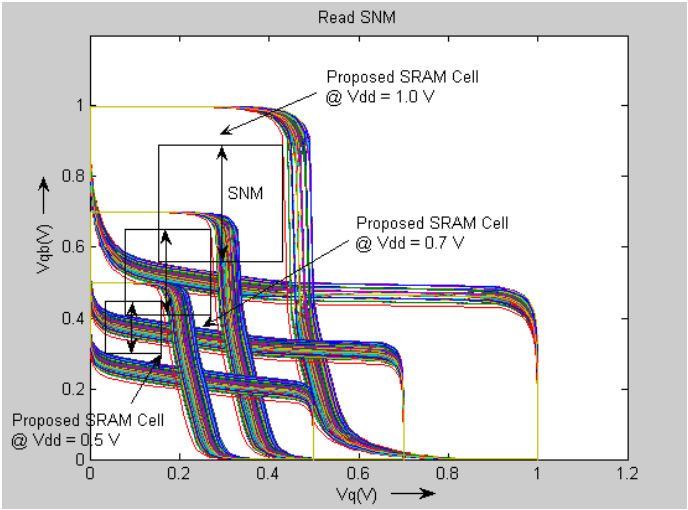


Figure 5.12: Read SNM in proposed SRAM Cell under Vdd variation

Figure 5.12 shows the simulation results the variation of the "butterfly" curves in the proposed SRAM cell at different supply voltage Vdd. We can observe that a significant degradation in SNM during the read operation when Vdd is reduced from 1.0V to 0.5V. Therefore, lower the supply voltage will further aggravate the effect on SNM and cause the circuit more susceptible to soft errors.

Lower supply voltage will also increase both read and write time in CMOS nano-scale technologies, as shown in Figure 5.13 and Figure 5.14. The proposed 10T SRAM cell is simulated at different CMOS technologies in order to evaluate the impact of the CMOS technology scaling on cell's read and write time. It can be observed that when using PMT-32nm device models, the write time of proposed SRAM Cell achieves highest value but its read time is lowest under Vdd Variation compared to other technologies. Thus, the read and write time can not be optimized simultaneously by

CMOS technology scaling down, which requires the designer to strike a good balance between read and write time. However, either of the read and write time can be compensated by enlarging the size of read or write access transistor.

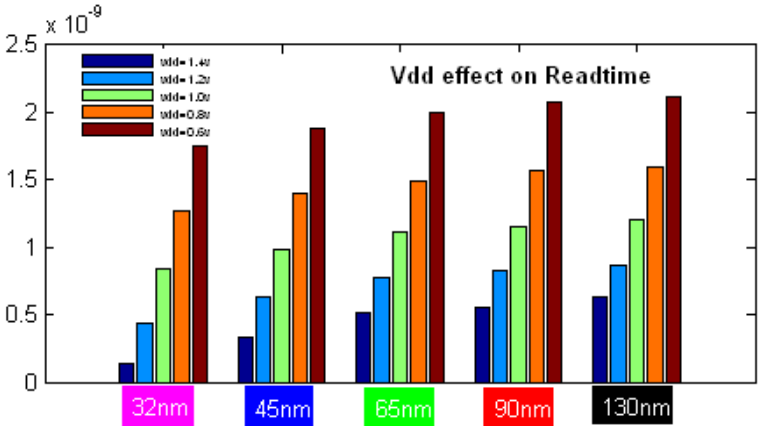


Figure 5.13: Proposed SRAM cell read time measure under Vdd variation

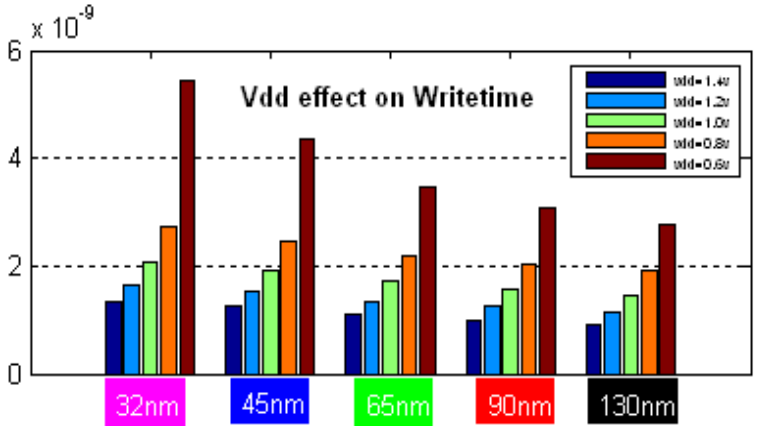


Figure 5.14: Proposed SRAM cell write time measure under Vdd variation

Figure 5.15 shows the write time plot for different SRAM Cells under supply voltage Vdd variation. When lowering the supply voltage from 0.6V to 0.4V, we can see a significant increase in read and write time for both conventional 6T and proposed SRAM cell.

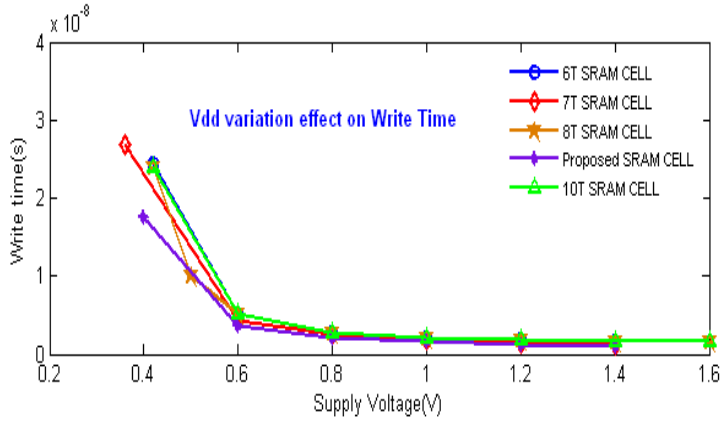


Figure 5.15: Write time measure under Vdd variation in different SRAM Cells

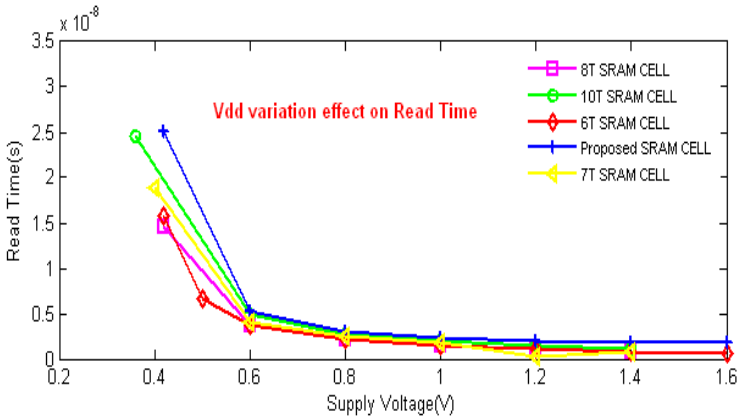


Figure 5.16: Read time measure under Vdd variation in different SRAM Cells

The proposed SRAM cell provides approximately 27% write time reduction at a supply voltage of 0.4V compared to the conventional 6T SRAM cell. Similar write time enhancement can be also observed at other low voltages supplied.

As mentioned before, the write time improvement in the proposed 10T SRAM cell is due to the weakening of the storage inverters in the cell by switching off the write transistor N5 to provide a floating ground terminal of the storage inverters. Since a single read transistor N6 in the proposed SRAM cell is implemented for an entire world line during the read access, the low cell current makes the cell take longer time to discharge the read bitline RB and thus increase the read time of the proposed cell compared to the conventional 6T SRAM cell, as shown in Figure 5.16. One read time enhancement approach is to size the read transistor in order to increase the read bitline discharge speed, but it will also increase the area overhead.

iii) SRAM Cell Simulation Results under device parameter variation

45nm CMOS technique
Cell Model: Conventional 6T and proposed 10T SRAM Cells
Variable Parameter: Channel length L, channel width W, gate oxide thickness tox and threshold voltage Vth.
Simulation Type: HSPICE simulation transient analysis, sweep monte=1000
Simulation time: 0 to 1000ns

In this experiment, the read & write time and power consumption of SRAM Cells owing to the process fluctuation in the channel length L, channel width W, gate oxide thickness tox and the threshold voltage Vth are evaluated. Each parameter is assumed to own a normal Gaussian statistical distribution with a 3σ variation of 10% and all parameters vary simultaneously. Monte Carlo Simulations with 1000 randomized instances are applied to estimate the effect of process variation on read and write time of the proposed 10T and conventional 6T SRAM cells.

Figure 5.17 and Figure 5.18 show the Monte Carlo simulation results of power consumption under PTM-45nm device parameter variation. The mean power consumption of proposed SRAM cell is about 1.3 μ W, which is very close to the value of power in Figure 5.5 when the proposed SRAM cell is simulated with no parameter variability. Whereas, the mean power consumption in the conventional 6T SRAM cell reaches to about 8 μ W, which is 12% higher than the power (7.2 μ W) shown in Figure 5.5 when the 6T SRAM cell is in the normal operation with no parameter variability. In addition, it can be also observed that a 84% decrease in the mean power consumption of the proposed cell compared to the 6T cell. Thus, the proposed SRAM cell is less susceptible to device parameter variation compared to the conventional 6T SRAM cell and consumes less average power.

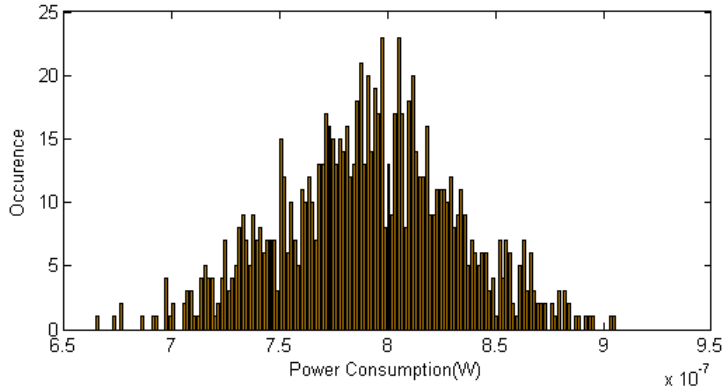


Figure 5.17: power consumption distribution in the conventional 6T SRAM Cell

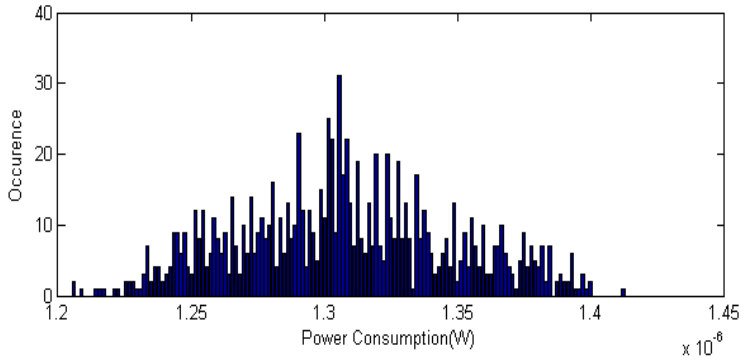


Figure 5.18: power consumption distribution in the proposed 10T SRAM Cell

Simulation results of read and write time distribution in both conventional 6T and proposed 10T SRAM Cells under PTM-45nm device parameter variation can be illustrated in Figure 5.19 and Figure 5.20. Compared to Figure 5.5, as it can be seen, the mean of read time in the proposed SRAM cell is approximately 3.6ns, which is 2.7% higher compared to the read time (3.5ns) of the same cell under no device parameter variation (Figure 5.5), while the mean read time (2.7ns) in the 6T SRAM cell achieves a 7.4% increase compared to the read time (2.5ns) without the device parameter variation (Figure 5.5).

Similarly, the mean of write time (3.6ns) in the proposed SRAM cell, which is 3.3% higher compared to the write time (3.5ns) of the same cell under no device parameter variation (Figure 5.5), while the mean write time (3.6ns) in the 6T SRAM cell achieves a 5.5% increase compared to the write time (3.4ns) without the device parameter variation (Figure 5.5).

It can be concluded that the proposed 10T SRAM Cell is less susceptible to device parameter variation compared to 6T SRAM Cell. Even in the presence of 10% parameter variation, the proposed SRAM cell can still achieve 15% write time accelerated compared to 6T SRAM cell. Although both read and write time increase due to the mismatch between the transistors which is caused by the parameter variation, the two SRAM cells can still achieve high speed performance.

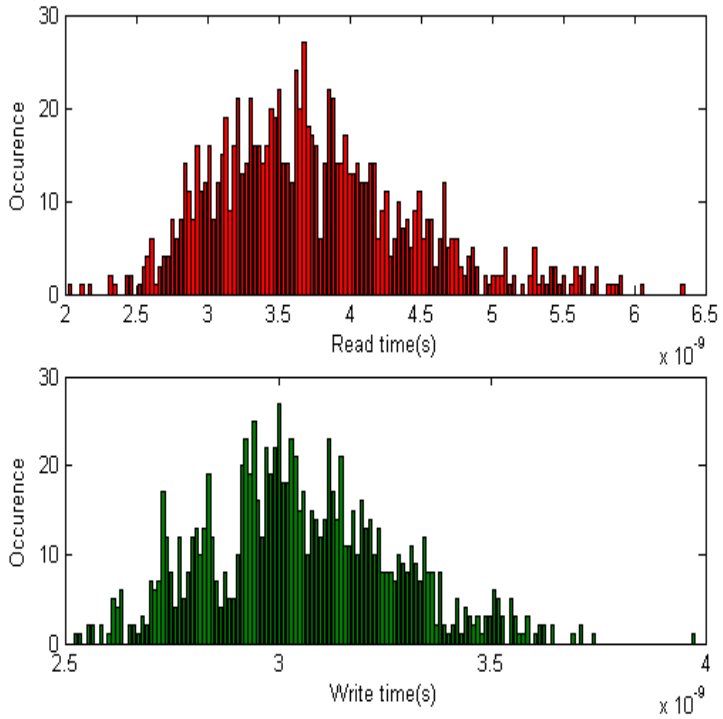


Figure 5.19: Read and write time distribution in proposed 10T SRAM Cell

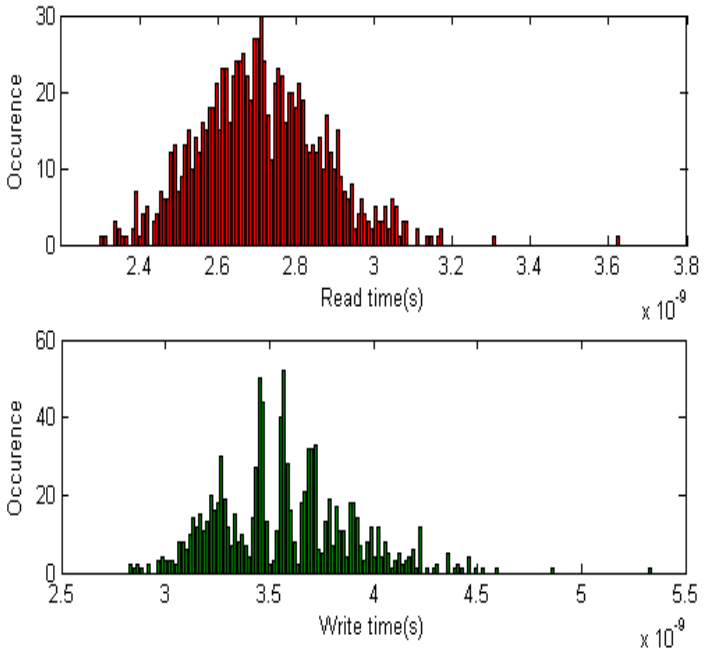


Figure 5.20: Read and write time distribution in conventional 6T SRAM Cell

5.4 SRAM Cell Layout

The layout of both conventional 6T and proposed 10T SRAM Cells design with minimum sized transistors are carried out in 0.70 μ m process by using Microwind Version 3.1, as shown in Figure 5.21 and Figure 5.22. The total size of proposed 10T SRAM layout is 42.5 $\mu m \times 33\ \mu m$, which is 48% area overhead compared to conventional 6T SRAM layout due to the four additional transistors and separate read wordline and bitline implementation in the proposed SRAM Cell.

However, in practice, 6T SRAM Cell design needs to enlarge the size in transistors to compensate the conflict of read and write performance requirement. Whereas, in the proposed SRAM Cell, although it has higher area cost than 6T SRAM Cell, lower power consumption and high performance can be achieved during both read and write operation without sizing transistors, which results in no further area overhead.

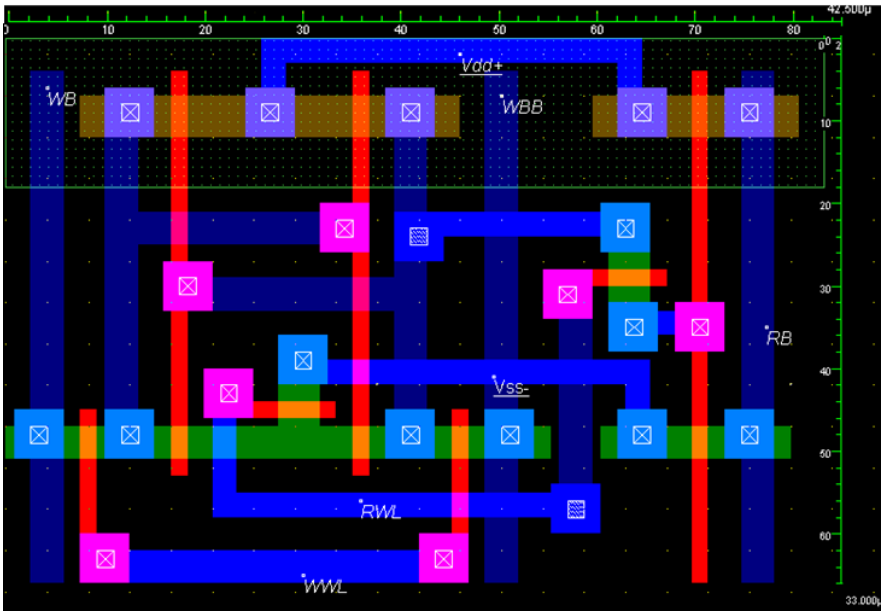


Figure 5.21: Layout view of proposed 10T SRAM Cell

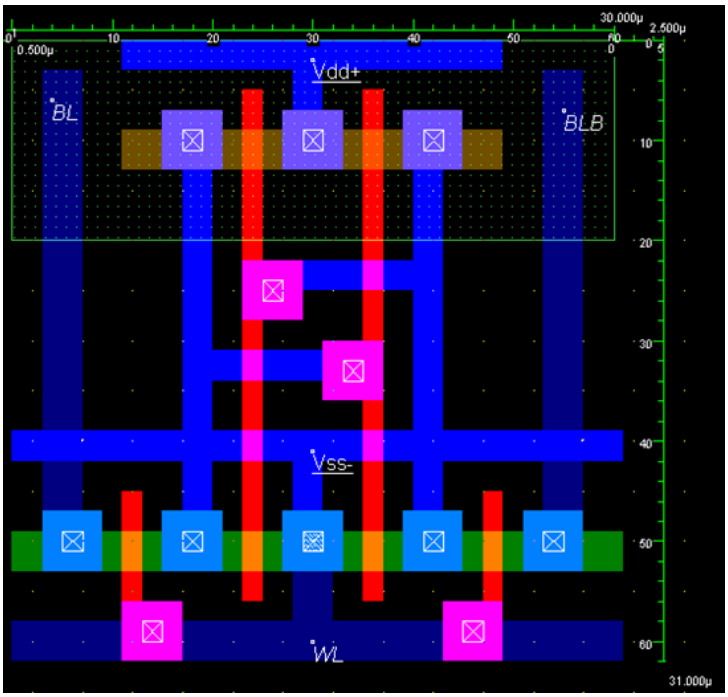


Figure 5.22: Layout view of conventional 6T SRAM Cell

Chapter 6: SRAM Cell SEUs Detection Test

In order to test the proposed SRAM Cell susceptibility to the SEUs and analysis the propagation of radiation effect on the cell during the standby, read and write modes, the particle strikes is simulated by injecting a transient current pulse at the sensitive node Q.

The current will be measured up to a point where it causes the data flip on storage node Q and QB. The current pulse that results from the particle strikes is expressed as follows:

$$I(t) = \frac{Q}{t_f - t_r}(e^{-\frac{t}{t_f}} - e^{-\frac{t}{t_r}})$$

Where Q is the amount of charge collected due to the ion strike, and t_f is the fall time and t_r is the rise time.

To evaluate the BICS detection capability on SEUs, we choose 32nm CMOS technology for HSPICE simulation. According to the three different operation conditions (standby, write and read) in SRAM, the reference voltages Bv and Bg used in the BICS SRAM model should be determined. Table 6.1 shows the different reference voltages used in this experiment.

Operation Mode	Reference Voltage (V)	
	Bv	Bg
Standby	0.5	0.7
Write	0.4	0.8
Read	0.6	0.5

Table 6.1: BICS Reference Voltages

Simulation results for SEUs under standby condition:

Figure 6.1 illustrates the simulation results of the BICS Cell during standby mode. The current pulse itrans is generated with t_r =5ps and t_f =100ps. We can observe that the current is injected after the write wordline WWL is disabled and thus the BICS cell is idle. The data on node Q and QB get flipped when current pulse itrans=220uA is injected at 20ns and can be detected by BICS since the error signal goes high to indicate the occurrence of SEUs in this BICS cell.

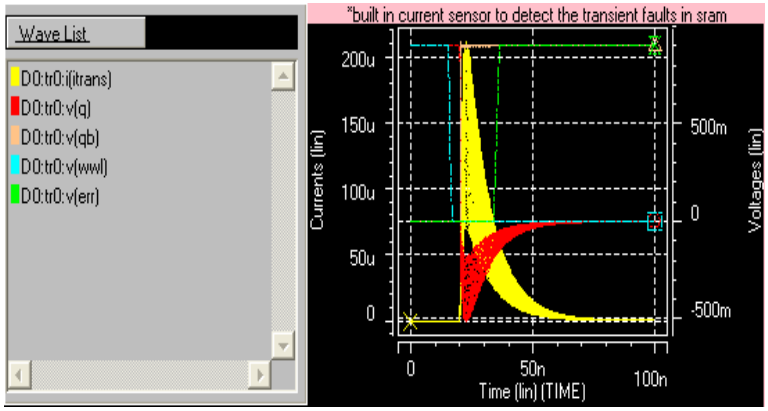


Figure 6.1: SEUs detection in BICS during standby mode

Simulation results for SEUs under operating condition:

As described before, the data upset in the cell caused by the SEUs not only occur during the standby condition, but also existed during the cell operating condition, as shown in Figure 6.2. During the write operation, since the delay element is used in the cell to control the reset signal RST, thus the current pulse should be generated after RST becomes low to ensure it is injected at the end of the write operation. From Figure, it can be observed that the current pulse itrans=420u injected at 12ns results in 1 to 0 data flip in the cell and thus error signal is generated.

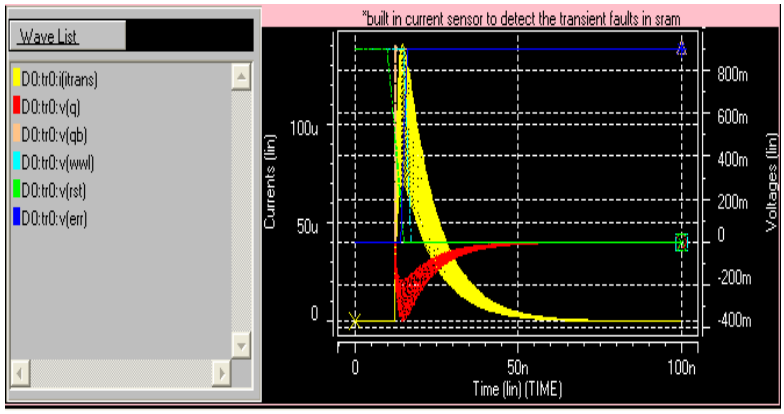


Figure 6.2: SEUs detection in BICS at the end of write operation

During the read operation, as shown in Figure 6.3, when the current pulse itrans=140uA is injected at 30ns, after the read wordline RWL is enabled, the data also gets flipped (Q becomes 0 and QB becomes 1), thus error signal is generated due to the particle hits on the cell sensitive node QB. Therefore, our simulation results have shown that this BICS cell has obtained high detection sensitivity to SEUs, which can clearly indicate the occurrence of soft error at both standby and operating conditions.

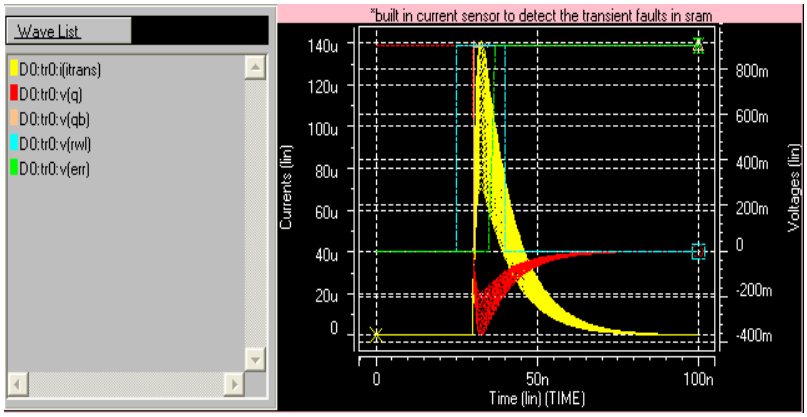


Figure 6.3: SEUs detection in BICS during read operation

Chapter 7: Conclusion

The reduced SNM of SRAM when lowering the supply voltage imposes great challenges to the modern SRAM design. The conventional 6T SRAM cell cannot function well because it can not achieve enough noise margin due to the conflict of read and write operation requirements. In order to achieve low power operation, previous research work has demonstrated that the read and write decoupled scheme is a good approach to enhance the SNM.

A robust 10T low power SRAM Cell is proposed and simulated in different CMOS nano-technologies in this paper, as described in chapter 4. The proposed cell is based on asymmetric cell topology and uses separate read and write circuitry to enhance read/write stability. The write speed/power is significantly enhanced by providing a floating ground during the write operation.

In chapter 5, Monte Carlo simulations indicate a 158% read stability improvement, a 17% write time accelerated and a 80% overall power saving in new cell compared to the conventional 6T SRAM Cell, which fits for ultra-low-power applications. This increase comes at the cost of additional transistors, wordline and bitline that have a 48% area overhead. The proposed cell architecture can provide high speed and significant read and write data stability, even in the presence of process variations and device parameter mismatch, by isolating the read path from the write path. The improved read and write ability, reduced power consumption and high speed compared to 6T SRAM cell makes this new approach attractive for nano-CMOS regime in low power applications when the process variation is considered as a major design constraint.

In chapter 6, a single event upsets (SEUs) detection technique BICS is implemented in this SRAM design and evaluated through HSPICE simulations. Thus, it is capable to detect SEUs at any instant of time by generating an error signal to indicate the occurrence of soft errors, especially useful for real radiation environments for the applications such as space applications which require high-reliability.

Chapter 8: Future work

Although a lot of work has been carried out in the concept of the low power SRAM design in nano-CMOS technology, a few extensions to this project still need to be studied. In this chapter, the discussion based on the existing work and future development will be presented.

This project has presented a novel SRAM Cell design methodology for low power and high performance. With separate read and write circuitry implementation in this new cell, the static noise margin is enhanced as well as significant power savings compared to conventional 6T SRAM Cell. Some of the corresponding periphery circuit techniques have been discussed in this proposed SRAM design, such as write drivers, row decoder and column multiplexer, sense amplifier design, but we have not simulated their performance and evaluated the practicability. Thus, in the future, we intend not only to enhance the performance of the essential SRAM Cell design, but also to change our research motivation into these periphery circuit designs, to explore new and effective techniques for these applicants improvement

The impact of temperature variation should be investigated in the future, as it may influence the circuit operating conditions and thus the performance. Since the nano-CMOS technologies scales down, it has been demonstrated that the process variations will greatly affect the performance of SRAMs and may create the functional failures in memory. More specifically, the other failure mechanisms, such as the data flipping hold failure need to be analyzed in the future. Different directions of failure with various falling condition also need to be studied. The SRAM reliability could be improved by developing the design of variation tolerant approach to decrease the effects of process induced variations.

The single SRAM Cell implemented in this project is needed to apply to cell array inside the SRAM chip to enable large memory capacity to meet the modern commercial product requirements. The chip applicability and fabrication should be evaluated.

During this project, both the impact of radiation effects on SRAMs and various soft errors decrease methods are discussed, in addition, a BICS-based SRAM has been introduced, which is used to detect the soft errors induced by the radiation. Design methodologies to offer the immunity to these particle strikes and soft errors needs to be studied in the future in order to implement radiation hardened memories.

Bibliography:

[1] L. Turicchia, S. Mandal, M. Tavakoli, L. Fay, V. Misra, J. Bohorquez, Sanchez, and R. Sarpeshkar, “Ultra-low-power Electronics for Non-invasive Medical Monitoring,” IEEE Custom Intergrated Circuits Conference (CICC), pp. 85-92, 2009

[2] P. Dodd and L. Massengill, “Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics,” IEEE Transactions on Nuclear Science, Vol. 50, No. 3, pp. 583-602, Jun. 2003

[3] T. May, M. Woods, “Alpha-Particle-Induced Soft Errors in Dynamic Memories,” IEEE Transactions on Electron Devices, pp. 2-9, Jan. 1979

[4] D. Binder, E. Smith and A. Holman, “Satellite Anomalies from Galactic Cosmic Rays,” IEEE Transactions on Nuclear Science, Vol.22, No. 6, pp. 2675-2680, Dec. 1975

[5] C.H. Lin, K.K. Das, L. Chang, R.Q. Williams, W.E. Haensch, C. Hu, “VDD Scaling for FinFET Logic and Memory Circuits: the Impact of Process Variations and SRAM Stability,” International Symposium VLSI Technology, Systems, and Applications, pp. 1-2, Nov. 2006

[6] Z. Guo et al., "Large-Scale Read/Write Margin Measurement in 45nm CMOS SRAM Arrays,” in *VLSI Circuits Symp. Dig.*, Jun. 2008, pp. 42–43.

[7] M. Khellah *et al.*, “Wordline and bitline pulsing schemes for improving SRAM cell stability in low-Vcc 65 nm CMOS designs,” in VLSI Circuits Symp. Dig., 2006, pp. 12–13.

[8] T. Suzuki et al., “A stable SRAM cell design against simultaneously R/W disturbed accesses,” in VLSI Circuits Symp. Dig., Jun. 2006, pp. 14–15.

[9] M. Khellah *et al.*, “Effect of power supply noise on SRAM dynamic stability,” in *VLSI Circuits Symp. Dig.*, Jun. 2007, pp. 76–77.

[10] E. Seevinck, F. List and J. Lohstroh, “Static-Noise Margin Analysis of MOS SRAM Cells,” IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5, pp. 748-754, Oct. 1987

[11] M. Yamaoka, K. Osada, R. Tsuchiya, M. Horiuchi, S. Kimura, and T. Kawahara, “Low Power SRAM Menu for SOC Application Using Yin-Yang-Feedback Memory Cell Technology,” Symposium on VLSI Circuits (VLSI) Digest of Technical Papers, pp. 288-291, 2004

[12] D. Boning and S. Nassif. Models of process variations in device and interconnect. In *Design of High-Performance Microprocessor Circuits, A.Chandrakasan, Chapter 6*, pp.98 – 115, IEEE Press 2001.

[13] A. Bhavnagarwala *et al.*, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 658–665, Apr. 2001.

[14] S. Mukhopadhyay et al., "Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS," IEEE Trans.omput.-Aided Des., vol. 24, no. 12, pp. 1859–1880, Dec. 2005.

[15] A. Agarwal, B. C. Paul, S. Mukhopadhyay and K. Roy, "Process Variation in Embedded Memories: Failure Analysis and Variation Aware Architecture", IEEE Journal of Solic-State Circuits, vol. 40, no. 9, pp1804-1814,Sep. 2005.

[16] Joyce Kwong, Yogesh K. Ramadass, Naveen Verma, Anantha P. Chandrakasan, "A 65 nm Sub-Vt Microcontroller With Integrated SRAM and Switched Capacitor DC-DC Converter," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 115-126, January 2009.

[17] B.H. Calhoun and A.P. Chandrakasan, "A 256-kb 65-nm Subthreshold SRAM Design for Ultra-Low-Voltage Operation", in Solid-State Circuits, IEEE Journal of, Volume 42, Issue 3, March 2007 Page(s):680 – 688

[18] I. Chang, J. Kim, S. Park and K. Roy, "A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS," IEEE Journal of Solid-State Circuits, Vol. 44, No. 2, pp. 650-658, Feb. 2009

[19] L.Geppert, "A Static RAM Says Goodbye to Data Errors," IEEE Spectrum, Feb, 2004

[20] . Gokhale, P. Graham, E. Johnson, N. Rollins, and M. Wirthlin. Dynamic reconfiguration for management of radiation-induced faults. *Proceedings of the 18th Parallel and Distributed Processing Symposium*, page 145, april 2004.

[21] Y.Z.Xu, H.Puchner, A.Chatila, 0. Pohland, B. Bruggeman, B.Jin, D.Radaelli and S.Daniel, "Process Impact on SRAM alpha-Particle SEU Performance", 42 nd IEEE Intern, Reliability Physics Symp.,pp.294-299, 2004

[22] G. Asadi and M. B. Tahoori. Soft error rate estimation and mitigation for SRAMs. *Proceedings of the 2005 ACM/SIGDA 13th international symposium on Fieldprogrammable gate arrays*, pages 149–160, February 2005.

[23] P. E. Dodd and L. W. Massengill, “Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics,” IEEE Transactions on Nuclear Science, Vol. 50, No. 3, pp. 583-602, Jun. 2003

[24] G. Asadi and M. Tahoori. An accurate SEU estimation method based on propagation probability [soft error rate]. *Proceedings of Design, Automation and Test in Europe 2005*, pages 306–307, 2005.

[25] B. Gill, M. Nicolaidis, C. Papachristou, F. Wolff, and S.Garverick, “An efficient bics design for SEUs detection and correction in semiconductor memories. IEEE Design, Automation and Test in Europe (DATE-05), pp 592-597, 2006

[26] F. Lima Kanstensmidt, G. Neuberger, R. Hentschke, L. Carro, R. Reis, “Designing Fault-Tolerant Techniques for SRAM-based FPGAs”, IEEE D& T of Computers, pp. 552－562, Nov-Dec 2004

[27] Balkaran Gill, M. Nicolaidis, F. Wolff, C. Papachristou, and S. Garverick, “An Efficient BICS Design for SEUs Detection and Correction in Semiconductor Memories,” Proceedings of the conference on Design, Automation and Test in Europe, pp. 592-597, 2005.

[28] Y. Shiyanovskii, F. Wolff, and C. Papachristou, “SRAM Cell Design Protected from SEU Upsets,” Proceedings of the 14th IEEE International On-Line Test Symposium, pp. 169-170, 2008.

[29] E. I. Vătăjelu and J. Figueras, “Supply Voltage Reduction in SRAMs: Impact on Static Noise Margins,” IEEE International Conference on Automation, Quality and Testing, Robotics, Vol. 1, pp. 73-78, 2008

[30] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Yang, B. Zheng, and M. Bohr, “A SRAM Design on 65nm CMOS Technology with Integrated Leakage Scheme,” Symposium on VLSI Circuits (VLSI) Digest of Techical Papers, pp. 294-295, 2004

[31] M. Yamaoka, K. Osada, R. Tsuchiya, M. Horiuchi, S. Kimura, and T. Kawahara, “Low Power SRAM Menu for SOC Application Using Yin-Yang-Feedback Memory Cell Technology,” Symposium on VLSI Circuits (VLSI) Digest of Technical Papers, pp. 288-291, 2004

[32] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, “A Current Controlled Latch Sense Amplifier and a Static Power-Saving Input Buffer For Low-Power Architecture,” IEEE Journal of Solid-State Circuits, vol. 28, pp. 523–527, Apr. 1993

[33] N. Verma and A. Chandrakasan, “A 256 Kb 65 nm 8T Subthreshold SRAM Employing Sense-Amplifier Redundancy,” IEEE Journal of Solid-State Circuits, Vol.43, No.1, pp. 141-149, Jan. 2008
[34] N.M.Sivamangai, Dr.K.Gunavathi, P.Balakrishnan, “ BICS Design to Detect Soft Error in CMOS SRAM”, (IJCSE) International Journal on Computer Science and Engineering, Vol. 02, No. 03, pp 734-740, 2010

[35] C.H. Lin, K.K. Das, L. Chang, R.Q. Williams, W.E. Haensch, C. Hu, “VDD Scaling for FinFET Logic and Memory Circuits: the Impact of Process Variations and SRAM Stability,” International Symposium VLSI Technology, Systems, and Applications, pp. 1-2, Nov. 2006

[36] E. Seevinck, F. List and J. Lohstroh, “Static-Noise Margin Analysis of MOS SRAM Cells,” IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5, pp. 748-754, Oct. 1987

[37] B. Alorda, G. Torrens, S. Bota and J. Segura, “Static-Noise Margin Analysis during Read Operation of 6T SRAM Cells”, April 2008

[38] J. Bisgrove, J. Lynch, P. McNulty, W. Abdel-Kader, V. Kletnieks and W. Kolasinski, “Comparison of Soft Errors Induced By Heavy Ions And Protons,” IEEE Transactions on Nuclear Science, Vol. NS-33, No. 6, pp. 1571-1576, Dec. 1986

[39] Ken’ichi Agawa, Hiroyuki Hara, Toshinari Takayanagi, and Tadahiro Kuroda, “A Bitline Leakage Compensation Scheme for Low-Voltage SRAMs”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 5, MAY 2001

[40] Kuande Wang, “Ultra Low-Power Fault-Tolerant SRAM Design in 90nm CMOS Technology”, pp56-78, June 2010

[41] Jeyran Hezavei, N. Vijaykrishnan, M. J. Irwin, “A Comparative Study of Power Efficient SRAM Designs”, 2005

[42] R. Kanj, R. Joshi, S. Nassif, “Mixture importance sampling and its application to the analysis of SRAM designs in the presence of rare failure events,” Design Automation Conference, pp. 69-72, July 2006.

Books:

[43] Andrei Pavlov, Manoi Sachdev, “CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test”, Springer, 2008

[44] Neil H.E. Weste, David Harris, “CMOS VLSI Design”, 3rd Edition, Academic Press, 2005

Website:

[45] http://ptm.asu.edu/

Appendix: Source code

Due to restrictions on space, only the basic SRAM Cells simulation models excluding different CMOS technology models as well as SEUs detection implementation are appended.

Proposed SRAM Cell in 45nm technology

```
*Proposed SRAM    Memory    with single read and write circuitry
.param cload=0.1pf
.param rft=5n
.param vdd=0.7
.param l=45n
.param w=90n
 VCC 1 0 'vdd'
.IC V(Q)=0
.IC V(QB)='vdd'
.param nvt= 0.466v
.param pvt= -0.4118v
.GLOBAL 1

VD    D    0 pulse    0 'vdd'    50n 5n 5n 150n    400n
VPC PC 0 pulse    0 'vdd'    0n 2n 2n 40n    200n
VWWL WWL 0 pulse 0 'vdd' 55n 5n 5n 25n    200n
VW    W    0 pulse 0 'vdd' 55n 5n 5n 25n    200n
VRWL RWL 0 pulse 0 'vdd' 155n 5n 5n 25n 200n

*Precharge Circuit
XIPC PC PCB INV
MPCWB WB PCB 1 1    PMOS W='w' L='l'
MPCWBB WBB PCB 1 1    PMOS W='w' L='l'
CWB WB 0 cload
CWBB WBB 0 cload
CRB RB 0 cload

* SRAM CELL
 M1 Q QB    1    1 PMOS W='w' L='l'
 M2 Q QB    Q4    0 NMOS W='w'    L='l'
 M3 QB Q    1    1 PMOS W='w' L='l'
 M4 QB Q    Q4    0 NMOS W='w' L='l'
 M5 Q    WWL WB 0 NMOS W='w' L='l'
 M6 QB WWL    WBB 0 NMOS W='w' L='l'
 M7 QB RWL    Q3    0 NMOS W='w' L='l'
 M8 RB Q3    1    1 PMOS W='w' L='l'
 M9 RB Q3    0    0 NMOS W='w' L='l'
```

```
 M10 Q4 RWL 0 0 NMOS W='w' L='l'

*Write Circuit
MWBIT    WB    W Q1    0    NMOS W='w' L='l'
MWBITB WBB    W Q2    0    NMOS W='w' L='l'

*Read Circuit
XIOUT D DB INV
MRBIT    Q1    DB    0    0    NMOS W='w' L='l'
MRBITB Q2    D      0    0    NMOS W='w' L='l'

.SUBCKT INV in out1
*Node 1 is VDD; node 0 is GND
MI1 out1 in 1 1 PMOS W='w' L='l'
MI3 out1 in 0 0 NMOS W='w' L='l'
.ENDS INV

.TRAN 0.1n 100n      sweep monte=1
.MEASURE rms_pow rms power
.MEASURE ReadTime        trig    v(RWL)      VAL='0.5*vdd' Rise=2
+                                targ    v(RB)      VAL='0.5*vdd' Fall=1
.MEASURE WriteTime       trig v(WWL)      VAL='0.5*vdd' Rise=1
+                                targ v(QB)      VAL='0.5*vdd' Fall=1

.option    nopage nomod    post

*PTM 45nm NMOS
*PTM 45nm PMOS
.END
```

6T SRAM Cell in 45nm technology

```
*6 Transistor SRAM Memory with single read and write circuitry
.param cload=0.1pf
.param rft=5n
.param vdd=0.7
.param l=45n
.param w=90n
 VCC 1 0 'vdd'
.IC V(Q)=0
.IC V(QB)='vdd'
.param nvt= 0.466v
.param pvt= -0.4118v
.GLOBAL 1
```

```
VD    D    0 pulse 0 'vdd'    108n 5n 5n 150n    400n
VPC PC 0 pulse 0 'vdd'    50n 2n 2n 50n    100n
VWL WL 0 pulse 0 'vdd' 110n 5n 5n 25n    100n
VW    W    0 pulse 0 'vdd' 110n 5n 5n 25n    200n

*Precharge Circuit
XIPC PC PCB INV
MPCBIT    BIT    PCB 1 1    PMOS W='w' L='l'
MPCBITB BITB PCB 1 1    PMOS W='w' L='l'

CBIT    BIT    0 cload
CBITB BITB 0 cload

*6 transistors cell
  M1 Q QB    1    1 PMOS W='w' L='l'
  M2 Q QB    0    0 NMOS W='w' L='l'
  M3 QB Q    1    1 PMOS W='w' L='l'
  M4 QB    Q 0    0 NMOS W='w' L='l'
  M5 Q      WL BIT    0 NMOS W='w' L='l'
  M6 QB    WL BITB 0 NMOS W='w' L='l'

*Write Circuit
MWBIT    BIT    W    Q1    0    NMOS W='w' L='l'
MWBITB BITB W    Q2    0    NMOS W='w' L='l'

*Read Circuit
XIOUT D DB INV
MRBIT    Q1    DB    0    0    NMOS W='w' L='l'
MRBITB Q2    D      0    0    NMOS W='w' L='l'

.SUBCKT INV in out1
*Node 1 is VDD; node 0 is GND
MI1 out1 in 1 1 PMOS W='w' L='l'
MI3 out1 in 0 0 NMOS W='w' L='l'
.ENDS INV

.TRAN 0.1n 1000n      sweep monte=1
.MEASURE rms_pow rms power
.MEASURE ReadTime       trig v(WL) VAL='0.5*vdd'    Rise=2
+                                targ v(BITB)      VAL='0.5*vdd' Fall=2
.MEASURE WriteTime      trig v(W) VAL='0.5*vdd'    Rise=1
+                                targ v(QB)      VAL='0.5*vdd'    Fall=1
.option    nopage nomod    post
* PTM 45nm NMOS
```

```
*PTM 45nm PMOS
.END
```

7T SRAM Cell in 45nm technology

```
*7 Transistor SRAM    Memory    with single read and write circuitry
.param cload=0.1pf
.param rft=5n
.param vdd=0.7
.param l=45n
.param w=90n
Vdd 1 0 vdd.
.IC V(Q)=0
.IC V(QB)='vdd'
.param nvt= 0.466v
.param pvt= -0.4118v
.GLOBAL 1

VD    D    0 pulse 0 'vdd'    100n 5n 5n 150n    400n
VSL SL    0 pulse    'vdd' 0 50n 5n 5n 150n 200n
VPC PC 0 pulse 0 'vdd'    50n 2n 2n 40n    100n
VWL WL 0 pulse 0 'vdd' 110n 5n 5n 25n    100n
VW    W    0 pulse 0 'vdd' 110n 5n 5n 25n    200n

*Precharge Circuit
XIPC PC PCB INV
MPCBIT    BIT    PCB 1 1    PMOS W='w' L='l'
MPCBITB BITB PCB 1 1    PMOS W='w' L='l'
CBIT    BIT    0 cload
CBITB BITB 0 cload

*7 transistors cell
  M1 Q QB    1    1 PMOS W='w' L='l'
  M2 Q QB    Q3 0 NMOS W='w' L='l'
  M3 QB Q    1    1 PMOS W='w' L='l'
  M4 QB    Q Q3 0 NMOS W='w' L='l'
  M5 Q      WL BIT    0 NMOS W='w' L='l'
  M6 QB    WL BITB 0 NMOS W='w' L='l'
  M7 Q3    SL    0      0 NMOS W='w' L='l

*Write Circuit
MWBIT    BIT    W    Q1    0    NMOS W='w' L='l'
MWBITB BITB W    Q2    0    NMOS W='w' L='l'

*Read Circuit
```

```
XIOUT D DB INV
MRBIT    Q1    DB    0    0    NMOS W='w' L='l'
MRBITB Q2    D      0    0    NMOS W='w' L='l'

.SUBCKT INV in out
*Node 1 is VDD; node 0 is GND
MI1 out in 1 1 PMOS W='w' L='l'
MI3 out in 0 0 NMOS W='w' L='l'
.ENDS INV

.TRAN 0.1n 1000n      sweep monte=1
.MEASURE rms_pow rms power
.MEASURE ReadTime        trig v(WL) VAL='0.5*vdd'    Rise=2
+                                targ v(BITB)      VAL='0.5*vdd' Fall=2
.MEASURE WriteTime      trig v(W) VAL='0.5*vdd'    Rise=1
+                                targ v(QB)      VAL='0.5*vdd'    Fall=1

.option    nopage nomod    post
* PTM 45nm NMOS
*PTM 45nm PMOS
.END
```

8T SRAM Cell in 45nm technology

```
*8 Transistor SRAM    Memory    with single read and write circuitry
.param cload=0.1pf
.param rft=5n
.param vdd=0.7
.param l=45n
.param w=90n
Vdd 1 0 vdd
.IC V(Q)=0
.IC V(QB)='vdd'
.param nvt= 0.466v
.param pvt= -0.4118v
.GLOBAL 1

VD    D    0 pulse 0 'vdd'    50n 5n 5n 150n    400n
VPC PC 0 pulse 0 'vdd'    0n 2n 2n 40n    100n
VWWL WWL 0 pulse 0 'vdd' 55n 5n 5n 25n    200n
VW    W    0 pulse 0 'vdd' 55n 5n 5n 25n    200n
VR    R    0 pulse 0 'vdd' 155n 5n 5n 25n 200n

*Precharge Circuit
XIPC PC PCB INV
```

```
MPCWB WB PCB 1 1    PMOS W='w' L='l'
MPCWBB WBB PCB 1 1    PMOS W='w' L='l'
MPCRB RB PCB 1 1    PMOS W='w' L='l'
CWB WB 0 cload
CWBB WBB 0 cload
CRB    RB 0 cload

*8T SRAM Cell
 M1 Q QB    1    QB PMOS W='w' L='l'
 M2 Q QB    0    QB NMOS W='w'    L='l'
 M3 QB Q    1    Q PMOS W='w' L='l'
 M4 QB Q    0    Q NMOS W='w' L='l'
 M5 Q    WWL WB 0 NMOS W='w' L='l'
 M6 QB WWL    WBB 0 NMOS W='w' L='l'
 M7 Q3 QB    0    0 NMOS W='w' L='l'
 M8 RB R    Q3 0 NMOS W='w' L='l'

*Write Circuit
MWBIT    WB    W Q1    0    NMOS W='w' L='l'
MWBITB WBB    W Q2    0    NMOS W='w' L='l'

*Read Circuit
XIOUT D DB INV
MRBIT    Q1    DB    0    0    NMOS W='w' L='l'
MRBITB Q2    D    0    0    NMOS W='w' L='l'

.SUBCKT INV in out1
*Node 1 is VDD; node 0 is GND
MI1 out1 in 1    1 PMOS W='w' L='l'
MI3 out1 in 0    0 NMOS W='w' L='l'
.ENDS INV

.TRAN 0.1n 1000n      sweep monte=1
.MEASURE rms_pow rms power
.MEASURE ReadTime       trig    v(R)      VAL='0.5*vdd' Rise=2
+                                targ    v(RB)      VAL='0.5*vdd' Fall=1
.MEASURE WriteTime       trig v(WWL)      VAL='0.5*vdd' Rise=1
+                                 targ v(QB)      VAL='0.5*vdd' Fall=1
.option    nopage nomod    post
* PTM 45nm NMOS
*PTM 45nm PMOS
.END
```

10T SRAM Cell in 45nm technology

```
*10 Transistor SRAM    Memory    with single read and write circuitry
.param cload=0.1p
.param rft=5n
.param vdd=0.7
.param l=45n
.param w=90n
 Vdd 1 0 vdd .
.IC V(Q)=0
.IC V(QB)='vdd'
.param nvt= 0.466v
.param pvt= -0.4118v
.GLOBAL 1

VD    D    0 pulse 'vdd' 0    50n 5n 5n 150n    400n
VPC PC 0 pulse 0 'vdd'    0n 2n 2n 40n    100n
VWWL WWL 0 pulse 0 'vdd' 55n 5n 5n 25n    200n
VW    W    0 pulse 0 'vdd' 55n 5n 5n 25n    200n
VRWL RWL 0 pulse 0 'vdd' 155n 5n 5n 25n 200n

*Precharge Circuit
XIPC PC PCB INV
MPCWB WB PCB 1 1    PMOS W='w' L='l'
MPCWBB WBB PCB 1 1    PMOS W='w' L='l'
MPCRB RB PCB 1 1    PMOS W='w' L='l'
CWB WB 0 cload
CWBB WBB 0 cload
CRB RB 0 cload

*10T SRAM Cell
 M1 Q QB    1    1 PMOS W='w' L='l'
 M2 Q QB    0    0 NMOS W='w'    L='l'
 M3 QB Q    1    1 PMOS W='w' L='l'
 M4 QB Q    0    0 NMOS W='w' L='l'
 M5 Q    WWL WB 0 NMOS W='w' L='l'
 M6 QB WWL    WBB 0 NMOS W='w' L='l'
 M7 Q3 RWL    0    0 NMOS W='w' L='l'
 M8 Q4 QB    Q3 0 NMOS W='w' L='l'
 M9 Q4 RWL RB 0 NMOS W='w' L='l'
 M10 Q4 RWL 1    1 PMOS W='w' L='l'

*Write Circuit
MWB    WB    W Q1    0    NMOS W='w' L='l'
MRB    WBB    W Q2    0    NMOS W='w' L='l'
```

```
*Read Circuit
XIOUT D DB INV
MDB    Q1    DB    0    0    NMOS W='w' L='l'
MD      Q2    D      0    0    NMOS W='w' L='l'

.SUBCKT INV in out1
*Node 1 is VDD; node 0 is GND
MI1 out1 in 1    1 PMOS W='w' L='l'
MI3 out1 in 0    0 NMOS W='w' L='l'
.ENDS INV

.TRAN 0.1n 1000n      sweep monte=1
.MEASURE rms_pow rms power
.MEASURE ReadTime        trig    v(RWL)      VAL='0.5*vdd' Rise=2
+                                targ    v(RB)      VAL='0.5*vdd' Fall=1
.MEASURE WriteTime        trig v(WWL)      VAL='0.5*vdd' Rise=1
+                                 targ v(QB)      VAL='0.5*vdd' Fall=1
.option    nopage nomod    post
* PTM 45nm NMOS
*PTM 45nm PMOS
.END
```

SEUs Detection Model in 65nm technology

```
.param cload=0.1pf
.param vdd=1.2
.param l=32n
.param w=64n
.param Bv=0.5
.param nvt= 0.5088v
.param pvt= -0.450v
.param Bg=0.7
 VCC 1 0 'vdd'
.IC V(vddi)='vdd'
.IC V(gndi)=0
.IC V(Q)='vdd'
.IC V(QB)=0
.param Tra=1u
.TRAN 0.1n 100n    SWEEP Tra 100u 200u 4u
.param Delay=20n
.param RiseTime=1n
 ITrans Q 0 exp (0 Tra Delay RiseTime 'RiseTime*5' 'RiseTime*10')
.PROB I(Itrans)

 *SRAM Cell
```

```
VD    D    0 pulse    0 'vdd'    0n 1n 1n    15n    50n
VPC PC 0 pulse    0 'vdd'    0n 1n 1n    2n    50n
VWWL WWL 0 pulse 0 'vdd' 0n 0n 0n 15n    100n
VW    W    0 pulse 0 'vdd' 0n 1n 1n 15n    100n
VRWL RWL 0 pulse 0 'vdd' 25n 0n 0n 15n 100n

*Precharge Circuit
XIPC PC PCB INV
MPCWB WB PCB 1 1    PMOS W='w' L='l'
MPCWBB WBB PCB 1 1    PMOS W='w' L='l'
CWB WB 0 cload
CWBB WBB 0 cload
CRB RB 0 cload

        M1 Q QB    vddi    1 PMOS W='w' L='l'
        M2 Q QB    Q4    0 NMOS W='w'    L='l'
        M3 QB Q    Vddi    1 PMOS W='w' L='l'
        M4 QB Q    Q4    0 NMOS W='w' L='l'
        M5 Q    WWL WB 0 NMOS W='w' L='l'
        M6 QB WWL    WBB 0 NMOS W='w' L='l'
        M7 QB RWL    Q3    0 NMOS W='w' L='l'
        M8 RB Q3    1    1 PMOS W='w' L='l'
        M9 RB Q3    0    0 NMOS W='w' L='l'
        M10 Q4 RWL gndi 0 NMOS W='w' L='l'

*Write Circuit
MWBIT    WB    W Q1    0    NMOS W='w' L='l'
MWBITB WBB    W Q2    0    NMOS W='w' L='l'

*Read Circuit
XIOUT D DB INV
MRBIT    Q1    DB    0    0    NMOS W='w' L='l'
MRBITB Q2    D      0    0    NMOS W='w' L='l'

.SUBCKT INV in out1
*Node 1 is VDD; node 0 is GND
MI1 out1 in 1 1 PMOS W='w' L='l'
MI3 out1 in 0 0 NMOS W='w' L='l'
.ENDS INV

* 1st Comparator Svdd
        TB vddi 1    1    1 PMOS W='w' L='l'
        T5 vddi 0    1    1 PMOS W='w'    L='l'
        T6 a3 0    1    1 PMOS W='w' L='l'
```

```
        T3 a6 Bv vddi 1 PMOS W='w' L='l'
        T1 a6 a6 0    0 NMOS W='w' L='l'
        T4 a6 Bv a3 1 PMOS W='w' L='l'
        T2 a5 a6 0    0 NMOS W='w' L='l'
        T8 a4 a5 1    1 PMOS W='w' L='l'
        T10 Ev a4    1    1 PMOS W='w' L='l'
        T9 Ev a4 0    0 NMOS W='w' L='l'

* 2nd Comparator Sgnd
        M1 b1 b1 1    1 PMOS W='w' L='l'
        M2 b7 b2 1    1 PMOS W='w'    L='l'
        M7 Eg b7 1    1 PMOS W='w' L='l'
        M3 b1 Bg Bg 0 NMOS W='w' L='l'
        M4 b7 Bg Bg 0 NMOS W='w' L='l'
        M8 Eg Bg Bg 0 NMOS W='w' L='l'
        M6 Bg 1 0    0 NMOS W='w' L='l'
        M5 gndi 1 0    0 NMOS W='w' L='l'
        MB gndi 0 0    0 NMOS W='w' L='l'

* Asynchronous Latch
        R1 errb err 1    1 PMOS W='w' L='l'
        R2 err n 1    1 PMOS W='w'    L='l'
        R3 errb Ev 0    0 NMOS W='w' L='l'
        R4 errb err 0 0 NMOS W='w' L='l'
        R5 errb Eg 0 0 NMOS W='w' L='l'
        R6 err n    0 0 NMOS W='w' L='l'
        R7 err rst 0    0 NMOS W='w' L='l'

* DELAY
        XIWWL1 WWWL WWL1 INV
        XIWWL2 WWL1 WWL2 INV
        XIWWL3 WWL2 WWL3 INV
        XIWWL4 WWL3 WWL4 INV
        Rn1 1 WWL n 0 NMOS W='w' L='l'
        Rp2 rst WWL4 n 1 PMOS W='w' L='l'
        Rp1 0 WL rst 1 PMOS W='w' L='l'
        Rn2 rst WWL2 0 0 NMOS W='w' L='l'
        R3    rst RWL    0 0 NMOS W='w' L='l'

  .option nopage nomod    post
* PTM 32nm NMOS
*PTM 32nm PMOS
.END
```