# Abstract

As we face the end of scaling Si-based CMOS technologies, new devices are being developed to replace them. Carbon Nanotube-based transistors seem very promising due to their similar behaviour and their near-ballistic transport properties. However, this technology has defect issues, such as metallic tubes and misaligned or undeposited tubes.

In order to make this technology realizable, reliability needs to be improved. This project presents a detailed description of the CNFET behaviour as well as reliability enhancement and assessment techniques based mainly on the concept of redundancy.

In this work, fault tolerance is tackled from a design point of view rather that a fabrication one. In this way, some structures and layout configurations are presented and analyzed from a probabilistic point of view to assess any improvements made to the reliability of circuits.

The achievements accomplished in this project are as follows:

- A model of a CNFET was analyzed thoroughly in order to fully understand its behaviour.
- Different design structures were used based on redundancy to improve reliability.
- Probabilistic models were used to analyze reliability enhancement through such structures.
- Several layout configurations were used so as to improve reliability, and thus yield for building logic gates.
- Design tradeoffs were analyzed to understand the overhead that the reliability techniques bring.

# Acknowledgements

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# Chapter 1

# Introduction

Silicon based CMOS technologies are facing their practical limits. For years the approach has been to scale down the transistors, but as devices are made smaller, materials experience new physical effects. After the 32nm barrier, the most important challenges are standby power dissipation and the variability of device characteristics (1). Other problems that arise as technologies approach nanoscale sizes are reduced noise margin, gate threshold, band to band tunneling and energy levels reaching the computing thermal limits, among others.

New technologies are being researched to battle these obstacles. These include devices that are based on different transport phenomena, such as single spin devices (spintronics), ferromagnetic devices or molecular devices (2).

A different approach is to develop devices to be extensions to CMOS. This is, to generate devices in which the channel of the FET is replaced with high carrier mobility materials that display semiconductor behaviour if in quantum confinement (even though they have no semiconductor characteristics as bulk materials).

Carbon nanotube transistors are one of such extension to CMOS devices, which shows great promise to replace Si-based technologies in the future. They replace the channel of the transistor with one or several carbon nanotubes. CNTs can be either semiconducting or metallic, depending on the chirality, or twist of the tube, which is controlled during fabrication. Semiconducting CNTs are the ones used in the channel of transistors, where they can be controlled to build either n-type or p-type devices in order to construct logic gates in the same manner as CMOS technologies.

The major challenge for this kind of devices is that fabrication processes cannot guarantee defect free transistors. Defects include metallic CNTs (which translate into a short between source and drain terminals of the transistor), misaligned and undeposited CNTS. In order to make this technology feasible, reliability has to be improved.

This project presents a set of reliability enhancement techniques as well as models to assess such reliability. This techniques are based on redundancy, which is replicating a device, component or system in order to improve fault tolerance. It is notable to say that reliability is enhanced in this project through a design perspective, rather than a fabrication point of view, where defects are tackled in a different way and up to a certain extent.

Chapter 2 presents the aims and objectives of the project carried out. Chapter 3 introduces the behaviour of CNFETs with a detailed section on the channel characteristics including capacitance. Next, redundancy techniques are presented in chapter 4, along with the corresponding probabilistic models to analyze them. Yield is then discussed in chapter 5, where different layout configurations are presented. Chapter 6 describes and discusses results obtained. The project is then critically evaluated from different angles in chapter 7 and concluded in chapter 8.

# Chapter 2

# Aims and Objectives

The main aim of this project is to find design solutions to enhance the reliability of CNFET-based circuits.

In order to meet this aim, it is broken down into the next objectives:

- Literature review: study reliability enhancement techniques and different approaches to make circuits defect tolerant. It is also needed to study how to assess the reliability of such circuits, in order to be able to quantize the improvement made to the circuit by applying fault tolerant techniques.
- Understand the behaviour of CNFETs: to be capable of working with CNFETs, we have to fully understand how they work and what are their upsides and downsides. If we want to improve the feasibility of this technology in the future, we need to thoroughly know their defects, when and why do they present themselves and how to mitigate them.
- Analyze Reliability: once the techniques to be used are known, the objective is to apply them and analyze whether they improve reliability of the circuits. The analysis is made trough probabilistic models of the circuits designed.
- Based on the analysis, make suggestions of which structure or configuration to use under certain specified circumstances.

## 2. AIMS AND OBJECTIVES

# Chapter 3

# Carbon Nanotube Field Effect Transistors

## 3.1 Summary

This chapter presents the Carbon Nanotube transistors. It includes detailed analysis on their behaviour, specially in the channel area. This chapter also introduces analysis on the capacitance of the transistor and it presents the main defects that appear in the CNFETs due to fabrication issues.

## 3.2 CNFETs

Carbon Nanotubes (CNTs) were discovered in 1991 in Japan at the NEC Fundamental Research Laboratory (3). A CNT is a form of carbon with a cylindrical shape. It can be thought of as a graphene sheet rolled into a cylinder with a hemispherical fullerene on each end. CNTs can be found in two forms: single- and multi-walled, where multi-walled CNTs are nested single-walled CNTs.

CNTs have great physical properties such as their strength, flexibility and light weight. In the field of electronics, the most important property is their ability to be either metallic or semiconducting depending on their chirality. Applications can be found for both types of CNTs. For example, metallic CNTs can be used to build interconnects, while semiconducting CNTs are suitable for transistors.

The way different types of CNTs exist is explained by their chirality, given their chiral vector (n,m). The vector equation $\vec{R} = n\vec{a_1} + m\vec{a_2}$, where n and m are integers

is explained through the diagram in figure 3.1. If a nanotube is unraveled into a planar sheet and two lines (in blue) are drawn along the axis where the nanotube was separated, two points can be found, A and B in figure 3.1. A is any point in one of the blue lines that intesects a carbon atom. Now, we can draw a line, called the armchair line, that goes along the hexagons and cuts them exactly in half. The nearest carbon atom to the armchair line along the other blue line is point B. The chiral vector $\vec{R}$ (in red) is the one that connects point A and B. The wrapping angle $\phi$ is formed between $\vec{R}$ and the armchair line.

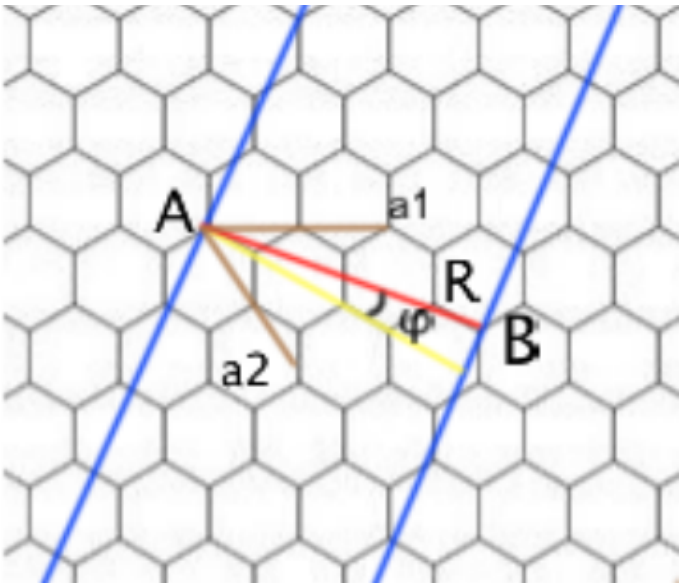


**Figure 3.1:** Graphical representation of the chirality vector

If the wrapping angle is 0°, $\vec{R}$ lies along the armchair line, and the nanotube is called armchair. If $\phi = 30°$ then the tube is called zigzag. Otherwise, if $0° < \phi < 30°$ then it is a chiral tube (4).

The values of $n$ and $m$ determine the chirality of the nanotube. If the value of $n - m$ is divisible by three, then it is a metallic nanotube, otherwise it is semiconducting. Therefore, for random values of n and m, a third of the tubes fabricated are metallic,while the other two thirds are semiconducting. With chiralities (n,m) the diameter of the tube is given by 3.1, where $a = 2.49\mathring{A}$ is the lattice constant.

$$D_{CNT} = \frac{a\sqrt{n^2 + nm + m^2}}{\pi} \tag{3.1}$$

The band gap (Eg) of metallic CNTs is 0. For semiconducting CNTs, their Eg is dependent on the diameter of the tube, as well as their chirality. Transistors made with CNTs (CNFETs) behave very similar to silicon-based transistors. The fact that these devices are one-dimensional reduces the scattering probability, which in turn make possible ballistic or near-ballistic transport under low voltage biasing (5).

## 3.3 Behavior of CNFETs

A typical way of fabricating CNFETs is as top-gated CNFETs, as shown in the layout in figure 3.2. CNTs are first deposited and aligned in a silicon substrate. Then source and drain contacts are placed and finally the gate is placed on top of the CNTs. The CNTs in the source and drain areas are doped accordingly, but are left undoped in the channel region, so that the conduction is controlled by the gate.

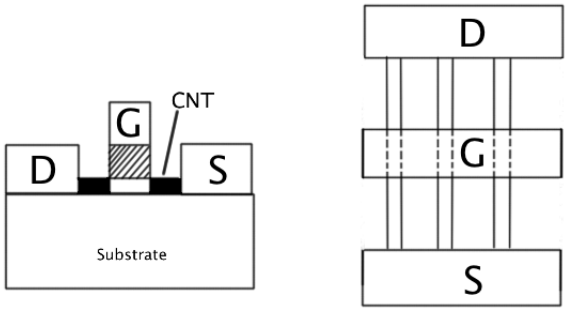


**Figure 3.2:** CNFET layout structure

Like the MOSFET, the CNFET I-V characteristics are controlled by their parameters such as node voltages, threshold voltage and width and length of the channel. However, in CNFETs some other parameters also come in play. These are the number of CNTs in a transistor, the pitch, which is the spacing between CNTs and the position of such CNTs along the channel.

Several simulation models have been proposed to understand and evaluate the performance of CNFETs. The one used in this project was created at Stanford University (6, 7, 8).

The current of a semiconducting CNT is modeled by the equations 3.2 and 3.3. J. Deng explains in (6) that only electron current is considered for nFETs due to the suppressing of hole current by heavily doping the source and drain ends of the CNT. $(m, l)$ is the $lth$ substate at the $mth$ subband. The contribution of that substate to the current is given by 3.4, where $V_{xs}$ is the voltage between node x and the source. $e$ is the electronic charge, and the Fermi velocity is $v_F = 1/\hbar \cdot \partial E/\partial k_l$. $m$ is assummed to be 2 and $l$ to be 9 because only the first two or three subbands and the first 10 to 15 substates have a significant impact on the current.

$$I_{semi}(\Delta\phi_B, V_{DS}) = 2\sum_{m=1}^{2}\sum_{l=0}^{9}[T_{LR}J_{m,l}(0, \Delta\phi_B)|_{+k} - T_{RL}J_{m,l}(V_{DS}, \Delta\phi_B)|_{-k}] \quad (3.2)$$

$$\Delta\phi_B = \frac{e}{(C_{gc\_p} + C_{SUB})} \times [C_{gc\_p} \cdot V_{GS} - \frac{4e}{L_g}\sum_{m=1}^{2}\sum_{l=0}^{9}[\frac{1}{1 + e^{(E_{m,l} - \Delta\phi_B)/KT}} + \frac{1}{1 + e^{(E_{m,l} - \Delta\phi_B + eV_{DS})/KT}}]] \quad (3.3)$$

$$J_{m,l}(V_{xs}, \Delta\phi_B) = 2envF \quad (3.4)$$

In 3.4, $n$ is the number of electrons in the substate $(m, l)$, given by 3.5, in which $\Delta\phi_B$ is the change in channel surface potential given a gate-drain bias, $f_{FD}(E)$ is the Fermi-Dirac distribution function and $E_{m,l}$ is the carrier energy at the substate $(m, l)$.

$$n = \frac{f_{FD}(E_{m,l} + eV_{xs} - \Delta\phi_B)}{L_g} \quad (3.5)$$

$$f_{FD}(E) = \frac{1}{1 + e^{E/KT}} \quad (3.6)$$

$T_{LR}$ and $T_{RL}$ in equation 3.2 are the transmission probabilities of the carriers flowing from drain to source (corresponding to the $+k$ branch) and from source to drain (corresponding to the $-k$ branch) respectively. They are calculated as in equations 3.7 and 3.8, where $l_{eff}$ is calculated by taking into account the effective acoustic phonon scattering, $l_{ap}$, and the effective optical phonon scattering, $l_{op}$, of the semiconducting subbands.

$$T_{LR} = \frac{l_{eff}(V_{ch,DS}, m, l)}{l_{eff}(V_{ch,DS}, m, l) + L_g} \quad (3.7)$$

$$T_{RL} = \frac{l_{eff}(0,m,l)}{l_{eff}(0,m,l) + L_g} \tag{3.8}$$

$$\frac{1}{l_{eff}(V_x s,m,l)} = \frac{1}{l_{ap}(V_x s,m,l)} + \frac{1}{l_{op}(V_x s,m,l)} \tag{3.9}$$

## 3.4 Gate Capacitance

As it can be seen, the current of a CNFET changes with the variation of the pitch and position of the CNTs. This means that even though we keep increasing the number of CNTs in a transistor, the current will not increase linearly. This is due to the screening effect from the CNTs, which affects the potential in the gate region.

The gate capacitance depends mainly on two capacitances, the gate to channel capacitance and the gate to gate capacitance, as well as the dimensions of the gate (width and length) (9).

$$C_{gg} \approx C_{gc} \times L_g + C_{gtg} \times W_g \tag{3.10}$$

### 3.4.1 Gate to gate Capacitance

The gate to gate capacitance ($C_{gtg}$) is separated into two terms, the first one is the gate to gate plate capacitance ($C_{gtg\_nr}$) which is due to the normal electric field between two parallel plates (equation 3.11). The second term is the gate to gate fringe capacitance ($C_{gtg\_fr}$), which is approximated as the capacitance between two parallel cylinders with equivalent radius. In equation 3.12, $\alpha_{gtg\_sr}$ is a factor due to screening. It is equal to one if the height of the adjacent gate is 0, but it is commonly approximated to 0.7 for the case when the height of the adjacent gate is equal to the height of the gate. The total $C_{gtg}$ is the addition of both its components, given in the next equations.

$$C_{gtg\_nr} = \frac{k_2 \epsilon_0 H_{gate}}{L_{sd}} \tag{3.11}$$

$$C_{gtg\_fr} = \alpha_{gtg\_sr} \cdot \frac{\pi k_2 \epsilon_0}{ln(\frac{2\pi(L_{sd}+L_g)}{2L_g+\tau_{bk}H_{gate}})} \tag{3.12}$$

$L_{sd}$ is the distance between the two parallel plates, $H_{gate}$ is the height of the gate, $k_2$ is the relative permitivity of the material in the region and $\tau_{bk}$ is the factor that accounts

for the effect of the back plates and is empirically approximated after knowing that potential caused by fringe flux decreases logarithmically with respect to the distance.

### 3.4.2 Gate to channel Capacitance

In order to calculate the gate to channel capacitance, we have to consider the parallel conducting channels as the CNTs and the gate electrode. $C_{gc}$ is calculated with 3.13. It varies with respect to the capacitance of the gate to the CNTs at the two ends of the transistor, called $C_{gc\_e}$, the capacitance of the gate to the rest of the CNTs located in the middle, $C_{gc\_m}$, and the total number of CNTs in the transistor, N.

$$C_{gc} = min(N, 2) \times C_{gc\_e} + max(N - 2, 0) \times C_{gc\_m} \tag{3.13}$$

A distinction is made between the capacitance in the CNTs of the end and the middle due to the coupling capacitances between the CNTs. Since the CNTs at the end only have one neighbour, their capacitance is different than the one of a CNT in the middle, which has two neighbours. Only the nearest objects are considered because the influence of objects with a greater distance is negligible.

If we consider the structure in figure 3.3, when a voltage is applied between the three CNTs (objects 1, 2 and 3) and the gate electrode (object 0), certain coupling capacitances appear and the charges $Q_1$, $\eta_1 Q_1$ and $\eta_2 Q_1$ appear on objects 1, 2 and 3 respectively. $\eta_1$ and $\eta_2$ are the ratios of the coupling capacitances, as equation 3.14 reflects, and they are dependent on the geometry and position of the CNTs.

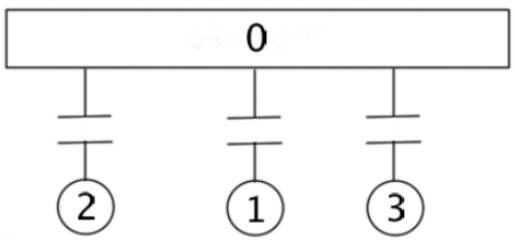


**Figure 3.3:** Gate to channel capacitance

$$\eta_1 = \frac{C_{02}}{C_{01}} \, \eta_2 = \frac{C_{03}}{C_{01}} \tag{3.14}$$

The coupling capacitance between object 0 and object 1 is calculated as in equation 3.15, where $C_{gc\_sr\_1}$ and $C_{gc\_sr\_2}$ are the equivalent capacitances due to screening effects of the other two CNTs and $C_{gc\_inf}$ is the capacitance between the gate electrode and CNT number 1. $C_{gc\_sr}$ and $C_{gc\_inf}$ are calculated with equations 3.16 and 3.17, and so $C_{01}$ becomes $C_{gc}$ for each CNT. If the CNT is at either end, $\eta_1 = 1$ and $\eta_2 = 0$, but if the CNT is in the middle, then $C_{gc\_sr\_1} = C_{gc\_sr\_2}$ and the factors $\eta_1 = \eta_2 = C_{gc\_e}/C_{gc\_m}$. Therefore, $C_{gc\_e}$ and $C_{gc\_m}$ can be calculated using equations 3.18 and 3.19.

$$C_{01} = \frac{1}{\frac{1}{C_{gc\_inf}} + \eta_1 \cdot \frac{1}{C_{gc\_sr\_1}} + \eta_2 \cdot \frac{1}{C_{gc\_sr\_2}}} \tag{3.15}$$

$$C_{gc\_sr} = \frac{4\pi k_1 \epsilon_0}{ln(\frac{s^2+2(h-r)\cdot[h+\sqrt{h^2-r^2}]}{s^2+2(h-r)\cdot[h-\sqrt{h^2-r^2}}) + \lambda_1 \cdot ln(\frac{(h+d)^2+s^2}{9r^2+s^2}) \cdot tanh(\frac{h+r}{s-d})} \tag{3.16}$$

$$C_{gc\_inf} = \frac{2\pi k_1 \epsilon_0}{cosh^{-1}(\frac{2h}{d}) + \lambda_1 \cdot ln(\frac{2h+2d}{3d})} \tag{3.17}$$

$$C_{gc\_e} = \frac{C_{gc\_inf} \cdot C_{gc\_sr}}{C_{gc\_inf} + C_{gc\_sr}} \tag{3.18}$$

$$C_{gc\_m} = 2C_{gc\_e} - C_{gc\_inf} \tag{3.19}$$

$$\lambda_1 = \frac{k_1 - k_2}{k_1 + k_2} \tag{3.20}$$

All the analysis up to this point considers the pitch to be constant. This is, the distance between any adjacent CNTs is the same. However, when defects are found in a CNFET, such as undeposited CNTs, or after metallic CNTs have been removed from the transistor, the pitch varies (10). (Defects and metallic CNT removal will be explained in a later section).

For such cases, the correct spacing needs to be taken into account. Since the pitch is fixed prior to defining gates and contacts, the intervals between deposited CNTs are multiples of the pitch. Figure 3.4 shows a configuration with four deposited CNTs and three undeposited CNTs, creating three different intervals. In this case, the pitch is $s$ and the intervals are $int_1 = 2s$, $int_2 = 3s$ and $int_3 = s$.

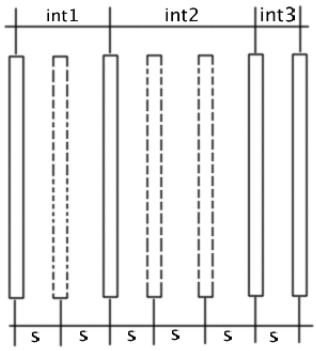


**Figure 3.4:** Intervals between deposited CNTs

In order to extend this to the previous model, equation 3.13 is modified to be equation 3.21, where $N_{CD}$ is the number of undeposited CNTs and $N - N_{CD}$ is the number of deposited CNTs. A distinction also needs to be made regarding $C_{gc\_m}$. If the intervals are the same, then it is symmetric and that capacitance is named $C_{gc\_symmetric}$ and it is calculated with equation 3.19. But if the intervals are different then it becomes $C_{gc\_asymmetric}$, and two values for $C_{gc\_e}$,$C_{gc\_m\_symmetric}$ and $C_{gc\_sr}$ have to be found, one for $int_1$ and one for $int_2$. $C_{inf}$ does not change because it is independent from the intervals. In light of this, if undeposited CNTs are found, then equations 3.14 and 3.15 change to equations 3.22 and 3.23.

$$C_{gc} = min(N - N_{CD}, 2) \times C_{gc\_e} + max(N - N_{CD} - 2, 0) \times C_{gc\_m} \tag{3.21}$$

$$\eta_1 = \frac{C_{gc\_e\_int1}}{C_{gc\_m\_symmetric_int1}} \; \eta_2 = \frac{C_{gc\_e\_int2}}{C_{gc\_m\_symmetric_int2}} \tag{3.22}$$

$$C_{gc\_m\_asymmetric} = \frac{1}{\frac{1}{C_{gc\_inf}} + \frac{C_{gc\_e\_int1}}{C_{gc\_m\_symmetric_int1}} \cdot \frac{1}{C_{gc\_sr\_int1}} + \frac{C_{gc\_e\_int2}}{C_{gc\_m\_symmetric_int2}} \cdot \frac{1}{C_{gc\_sr\_int2}}} \tag{3.23}$$

To compare the variation of capacitance, $C_{gc\_e}$ (in blue), $C_{gc\_m\_symmetric}$ (in red) and one value of $C_{gc\_m\_asymmetric}$ (in green) are plotted in figure 3.5.

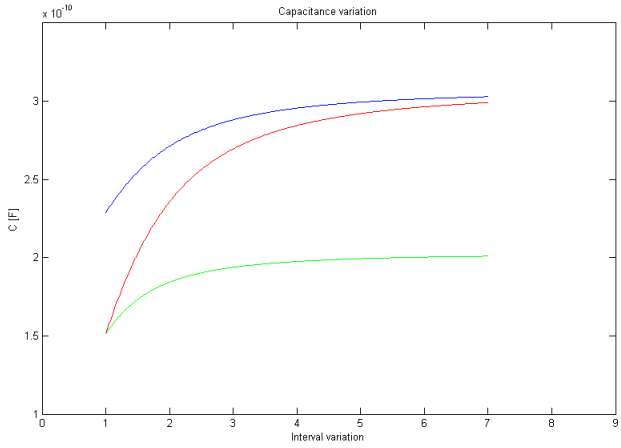


**Figure 3.5:** Gate to channel capacitance variation

## 3.5 Defects in CNFETs

Variations in the fabrication process of CNFETs may lead to defects and malfunctioning. Apart from the typical Si-based process variations (geometry of gate, contacts, etc. as well as variation in doping), CNFET fabrication has some special fabrication disparities. For example, CNTs that are larger or smaller than expected may lead to electrical features different from what is expected.

As it has been stated, CNTs may be metallic or semiconducting depending on their chirality. Chirality can be controlled by fabrication. Nevertheless, current fabrication processes yield between 10 and 30% of metallic CNTs. The conductivity of metallic CNTs cannot be controlled by the gate voltage, so they effectively create a short between source and drain, which leads to excessive leakage and/or logic malfunctioning, with very degraded noise margin.

Figure MISSING shows the variation of CNFET current with a different number of metallic CNTs.

If the fabrication process does not have the ability to grow perfectly aligned and uniformly distributed CNTs, it leads to variations in CNT density which may result in CNFETs with no semiconducting CNTs. This translates into an open defect. Variations in CNT density, as well as their diameter translate into variations in delay and power consumption.

Another kind of defect comes with misaligned CNTs, which can cause unintended shorts inside logic structures and result in incorrect logic functionality (11). Figure 3.6 shows three circuits representing a NAND gate, the first one with aligned CNTs and the second one has misaligned CNTs, resulting in inappropriate circuit functionality. This kind of defects can sometimes be prevented by designing the layout in such way that even though there are misaligned CNTs, the circuit is still functional, as the third circuit in figure 3.6.

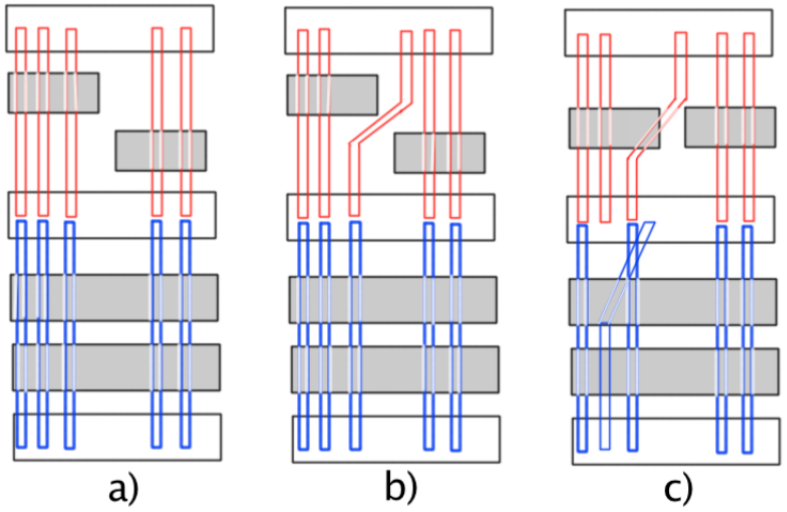


**Figure 3.6:** NAND gates with a)no misaligned CNTs, b)misaligned CNTs causing a short and c)misaligned CNT-immune configuration.

## 3.6 metallic CNTs removal techniques

The main obstacle of nanotube-based technologies to replace Si-based CMOS is the fact that no method exists to obtain only semiconducting CNTs without any metallic tubes. For this reason, from the fabrication point of view, some methods have been used to remove metallic nanotubes from the circuits. The main methods are electrical burning and chemical etching (12).

Current induced electrical burning removes metallic CNTs by effectively passing a high value of current until they break. Even though CNTs are able to resist current densities up to $10^9 A/cm^2$ due to the strong carbon-carbon bonding, at a high enough

current, metallic CNTs break (13). The removal of the CNTs through this method can be observed both electrically, since current stops flowing, and through microscopy. However this method is not so scalable to VLSI applications, since it requires to contact each transistor individually.

Selective chemical etching removes m-CNTs by hydrocarbonating them. The way it selects which CNTs to remove is by selecting a cutoff metallic tube diameter, $c_m$. Any metallic tube smaller than the cutoff diameter is removed. However, the etching also affects semiconducting tubes up to another cutoff diameter, $c_s$.

In this way, any semiconducting tube with a diameter between $c_s$ and $c_m$ survives the etching, but smaller tubes are etched away. Also, metallic tubes bigger than $c_m$ survive. So the ideal etching would have $c_s = 0$ and $c_m \to \infty$ so that all m-CNTs are removed and all s-CNTs survive, but real cases are not like this (14). This method can be used in VLSI fabrication processes.

# Chapter 4

# Redundancy

## 4.1 Summary

This chapter discusses the reliability enhancement techniques made through redundancy. First, the concept of redundancy is explained, then transistor redundancy concepts are introduced. This is followed by the introduction of the concept of correlation in CNFET fabrication and some techniques to undermine its undesired effects to reliability. Analysis to assess reliability of redundant structures is also presented in this chapter.

## 4.2 Redundancy

Reliability is the ability of a system to perform the functions that is required to do during a certain period of time under certain conditions. The reliability of a system can be enhanced through fault tolerance, which is designing a system so that it continues to operate correctly even though there are certain specified faults (15).

In order to improve reliability and fault tolerance of a system, redundancy is used. The concept of redundancy means having a certain number of back-up systems in case of a defect or a fault.

If we consider a system made up of N elements, then the correct operation of this system implies that all N elements work correctly. In this way, the reliability of the system is calculated as follows (16):

$$R_0 = P_1 \cdot P_2 \cdot P_3 \cdots P_N = \prod_i^N P_i \tag{4.1}$$

If all elements have the same reliability, then equation 4.1 becomes:

$$R_0 = P^N \tag{4.2}$$

It can be appreciated that as $N \to \infty$, $R \to 0$ despite the reliability of P. For this reason, redundancy is required.

Failure probability is the complement of reliability, so for a system with reliability $R$, the failure probability is $F = P_F = 1 - R$.

As discussed in previous sections, a CNFET has an open defect if the transistor is void, meaning that there are no s-CNTs in the channel. A short defect reflects mainly a m-CNT present in the transistor. We can define the failure probability of a CNFET as the addition of the probabilities of having an open defect and a short defect. This failure probability reflects the probability of a transistor being defective.

$$P_{F,CNFET} = P_O + P_S \tag{4.3}$$

The defect probability of a CNFET with the current fabrication processes is around $10^{-1}$ to $10^{-2}$. In order to achieve functioning VLSI circuits using CNFETs it is needed to improve fault tolerance.

## 4.3 Transistor Redundancy

Fault tolerance approaches have been focused mainly on adding redundancy at the functional or unit level through traditional techniques such as Triple Modular Redundancy (TMR), however it has been seen that adding redundancy at the transistor level improves reliability in a better way (17).

Transistor redundancy is based on having a series or a parallel connection of CNFETs to replace a single transistor. This is generally known as N-transistor redundancy. This can be seen in figure 4.1

In the series structure, if any of the transistors has an open defect, the complete structure fails. With this in mind, The failure probability of open defects for this

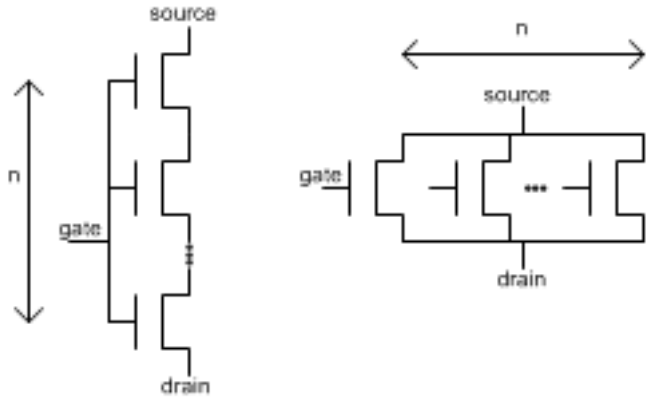


**Figure 4.1:** Series and Parallel redundancy

structure is calculated with equation 4.4, where $n$ is the number of transistors in such structure (18). A short defect is found in the series structure if all the transistors have a short defect, and its probability is calculated with equation 4.5. Finally, the failure probability of the series structure is the addition of the short and open defect probabilities (equation 4.6).

$$P_{O,series} = 1 - (1 - P_{O,CNFET})^n \tag{4.4}$$

$$P_{S,series} = (P_{S,CNFET})^n \tag{4.5}$$

$$P_{F,nseries} = 1 - (1 - P_{O,CNFET})^n + (P_{S,CNFET})^n \tag{4.6}$$

Regarding the parallel structure, if all CNFETs have an open defect, then the structure has an open defect, and if any of the devices has a short defect, then the whole structure has a whole defect. The failure probability of the parallel structure is, thus, the addition of the open and short defect probabilities.

$$P_{S,parallel} = 1 - (1 - P_{S,CNFET})^n \tag{4.7}$$

$$P_{O,parallel} = (P_{O,CNFET})^n \tag{4.8}$$

$$P_{F,nparallel} = (P_{O,CNFET})^n + 1 - (1 - P_{S,CNFET})^n \tag{4.9}$$

By combining series and parallel structures, we can obtain an open and short defect immune structure. In this way, we can get two kinds of structures. The first one is done by putting a number of series structures in parallel (PS) and the second one is done by putting several parallel structures in series (SP), as it can be seen in figure 4.2. This kind of structures are called $N^2$ structures, due to the fact that they replace a single transistor with $N^2$ transistors.

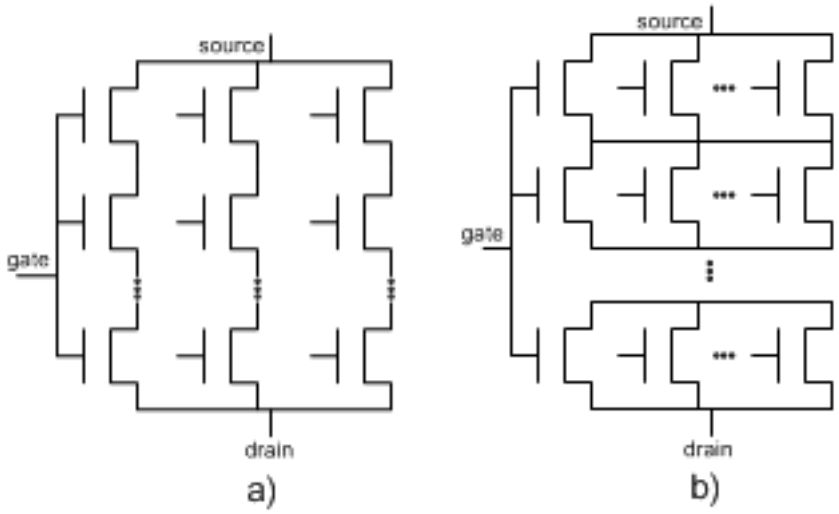


**Figure 4.2:** Schematics for a)SP structure and b) PS structure

Failure probabilities of the $N^2$ structures can be derived in the same way as the ones for $N$ structures. Their equations are shown next:

$N^2$ SP structure failure probability:

$$P_{O,SP} = 1 - (1 - (P_{O,CNFET})^n)^n \tag{4.10}$$

$$P_{S,SP} = [1 - (1 - P_{S,CNFET})^n]^n \tag{4.11}$$

$$P_{F,SP} = 1 - (1 - (P_{O,CNFET})^n)^n + [1 - (1 - P_{S,CNFET})^n]^n \tag{4.12}$$

$N^2$ PS structure failure probability:

$$P_{O,PS} = [1 - (1 - P_{O,CNFET})^n]^n \tag{4.13}$$

$$P_{S,PS} = 1 - (1 - (P_{S,CNFET})^n)^n \tag{4.14}$$

$$P_{F,PS} = [1 - (1 - P_{O,CNFET})^n]^n + 1 - (1 - (P_{S,CNFET})^n)^n \tag{4.15}$$

## 4.4 Correlation

When CNFETs are fabricated on aligned CNTs, there is a correlation between transistors built with the same tubes. In the same manner, if the transistors are placed along the direction that the CNTs are grown, those transistors are completely independent. This is important because if a tube is defective, all transistors that share the same tube are likely to be defective, however, if they don't share the same tubes, their defect probabilities are completely independent.

In the figure 4.3 we can observe CNTs aligned on one direction. It can be seen that there are two directions. All transistors built on the I direction are independent, and transistors built on the C direction are correlated. If two transistors share exactly the same tubes, they are fully correlated, but if they share some but not all tubes, the correlation factor varies between 0 and 1.

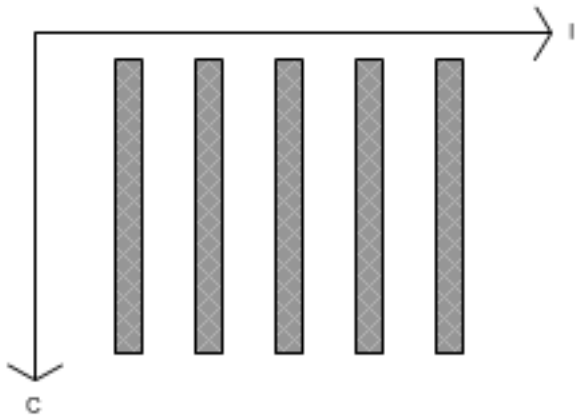


**Figure 4.3:** Correlated and independent directions according to CNT alignment

Because of this correlation, the failure probability of the structures previously discussed depend on the layout of the redundant transistors. All the analysis that has been presented corresponds to transistors that are independent.

When a series structure is built along the C direction, a Correlated n Series structure (CnSeries) is obtained. The failure probability of this structure is the same as the failure probability of a single CNFET since they share the same CNTs, which means that if one transistor fails, they all fail. On the other hand, when the series structure is built along the I direction, the Independent n Series structure (InSeries) is obtained. The failure probability of this structure is the same as the failure probability of the n Series structure.

$$P_{F,CnSeries} = P_{F,CNFET} \tag{4.16}$$

$$P_{F,InSeries} = P_{F,nseries} \tag{4.17}$$

In the same manner, parallel structures built along the C direction (CnParallel) have the same failure probability of a single transistor, while parallel structures built along the I direction have the failure probability of an n parallel structure. This can be observed in figure 4.4.

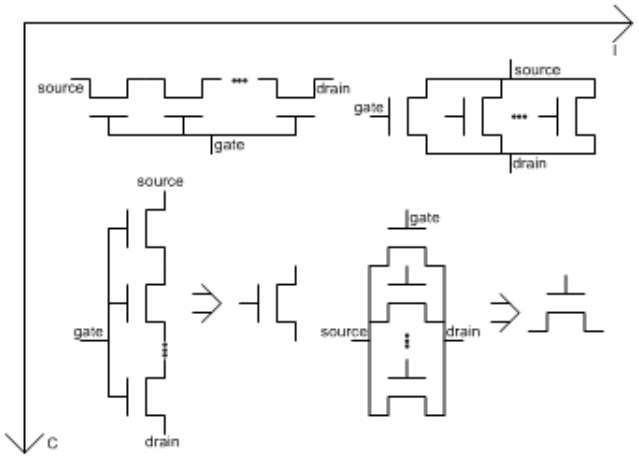


**Figure 4.4:** Independent and correlated series and parallel structures

$$P_{F,CnParallel} = P_{F,CNFET} \tag{4.18}$$

$$P_{F,InParallel} = P_{F,nparallel} \tag{4.19}$$

In order to fully analyze $N^2$ structures in CNFET technology we have to take into account the correlation of transistors. For this purpose, different configurations are created combining series and parallel structures as well as correlated and independent structures. In this manner, the SP structures are now either Correlated Series, Independent Parallel (CSIP) or Independent Series, Correlated Parallel (ISCP). The CSIP structure has bundles with $n$ series transistors that are aligned in the direction that the CNTs grow, which means that they are correlated, thus, identical, and the n parallel bundles are independent. The failure probability of this structure is therefore the same as the one for the n parallel structure.

$$P_{F,CSIP} = P_{F,InParallel} \tag{4.20}$$

In the ISCP structure, the n parallel transistors are fully correlated, and the n series bundles are independent, so the failure probability of this structure is the same as the failure probability of the n series structure.

$$P_{F,ISCP} = P_{F,InSeries} \tag{4.21}$$

In the same way, PS structures are divided into Correlated Parallel, Independent Series (CPIS) and Independent Parallel, Correlated Series (IPCS). Using the same analysis, it can be seen that the failure probability of CPIS is the same as the failure probability of the n series structure, while the failure probability of IPCS is the same as the failure probability of the n parallel structure.

$$P_{F,CPIS} = P_{F,InSeries} \tag{4.22}$$

$$P_{F,IPCS} = P_{F,InParallel} \tag{4.23}$$

It is notable that correlation increases the failure probability, since $N^2$ structures behave in the same way as $N$ structures, which means that even though we increase

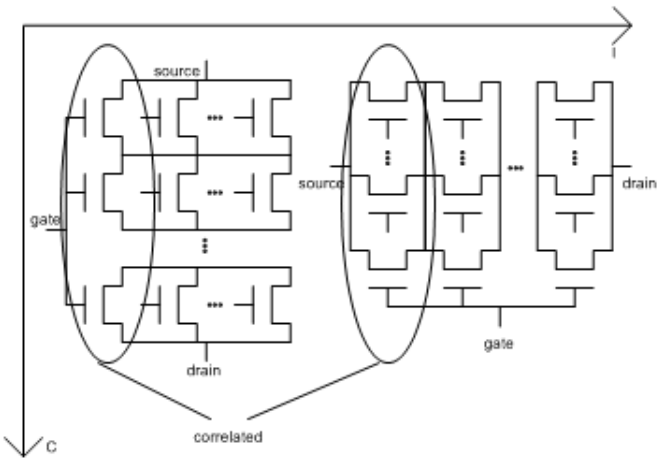


**Figure 4.5:** CSIP and ISCP structures

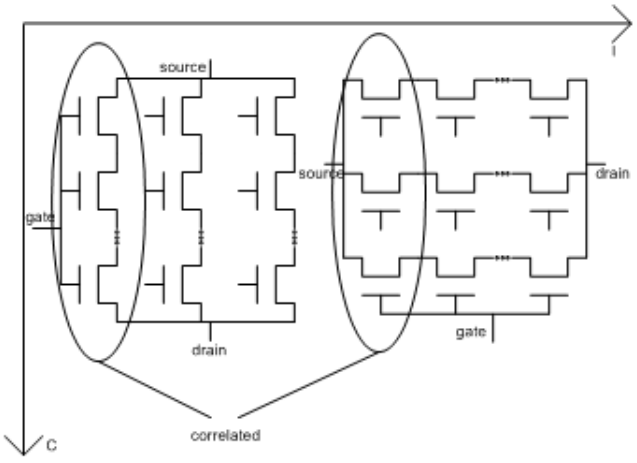


**Figure 4.6:** CPIS and IPCS structures

redundancy, reliability is not increasing. Therefore we need efficient structures that take advantage of higher levels of redundancy while eliminating the poor effects of correlation.

## 4.5 Efficient structures

As it has been said in previous sections, redundancy is the vehicle to improve reliability and fault tolerance. It has been shown that $N^2$ structures help tackle both open and short defects. However, in CNT technology, correlation increases failure probability, so different structures are needed in order to take advantage of the benefits of redundancy while eliminating correlation.

If transistors are placed in such a way that we obtain SP or PS structures, without having any correlated CNFETs we get all the benefits while diminishing the damaging effects of correlated CNFETs.

Under this circumstances, two structures are built: Independent Series-Parallel (ISP) and Independent Parallel-Series (IPS). The failure probabilities of these structures are equal to the failure probabilities of SP and PS structures respectively, since their design is so that CNFETs are independent.

Figure 4.7 shows the ISP structure, where bundles of parallel transistors are connected in series in the Independent direction. In the IPS structure the series transistors are aligned in the independent direction, and then these bundles are connected in parallel, as shown in figure 4.8.

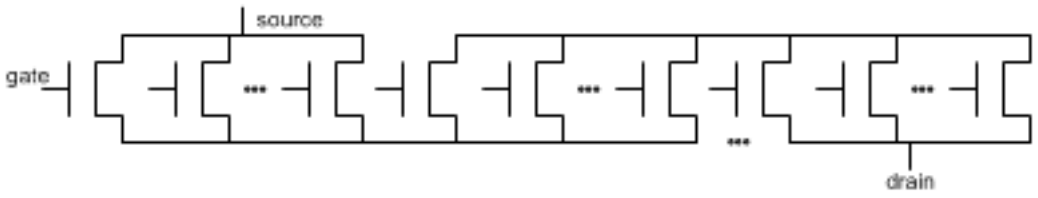


**Figure 4.7:** ISP structure

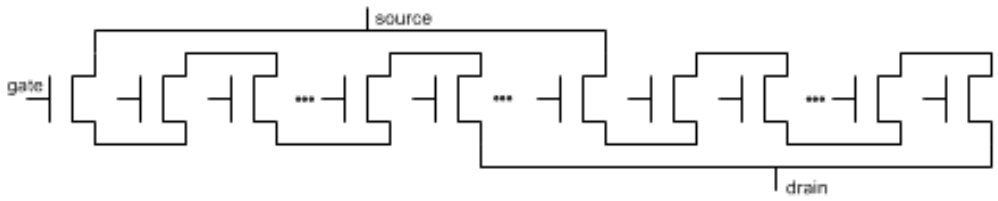


**Figure 4.8:** IPS structure

# Chapter 5

# Yield

## 5.1 Summary

This chapter presents yield analysis of CNFET-based circuits. The concept of yield is introduced first, and then certain layout configurations are presented. The analysis to assess yield is described in following sections.

## 5.2 Yield

Jha and Gupta define the yield as the fraction of the manufactured parts that has no defects. The value of yield is approximated as the ratio of the number of functional parts (non defective parts) to the total number of parts (19). The process yield is defined as 5.1, where $p$ is the failure probability, and n is the number of faults. It is also equal to the product of the probabilities of each stage of a system being functional, which is evident from equation 5.1 considering that $(1 - p)$ is the probability of being functional.

$$Y = (1 - p)^n \tag{5.1}$$

Logic gates are considered to be functional if their delay and power consumption are below a specified constraint, even in the presence of faults. Thus, the functional yield of a logic gate is dependent on such constraints as well as the number of metallic tubes.

Yield is evaluated on different layout configurations of CNFETs for building a logic gate. In this way, we build a logic gate and given the configuration its yield is calculated. In the next sections, the different configuration styles that have already been proven to work experimentally are discussed. Then calculation of yield is explained for an inverter, with such layout configurations.

## 5.3 Layout configurations

The shared tube configuration has one tube in which source and drain are alternated in order to create four transistors in parallel. However, in this configuration, all CNFETs are fully correlated, meaning that if the tube is metallic, all transistors will have their source and drain terminals shorted. Yield of this configuration is deterministic, since once known whether the tube is metallic, it is known that the CNFET will fail.

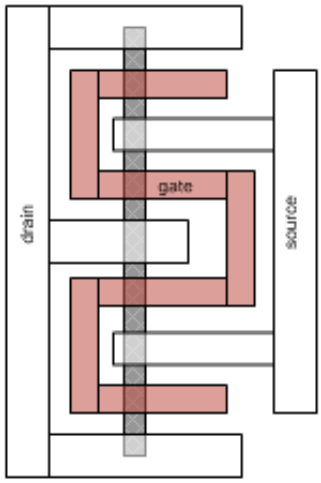


**Figure 5.1:** Shared Tube configuration

In the Parallel Tube configuration (PT), shown in figure 5.2, several tubes are aligned in parallel and share source and drain connections. As it has been explained previously, using this configuration opens the possibility of having correlated tubes, if the layout of the circuit is done in such way that two or more transistors share the same CNTs. However, the desirable state is to have all CNFETs independent from

each other. The presence of metallic tubes in this configuration implies a short between source and drain (20).

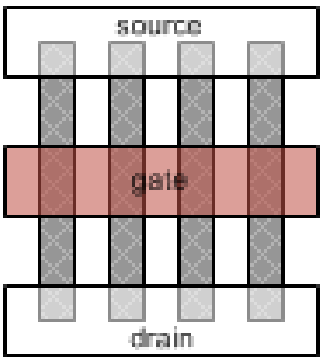


**Figure 5.2:** Parallel Tubes configuration

The next configuration is known as Transistor Stacking (TrS), in which two transistors with uncorrelated CNTs are stacked and connected through a shared contact. The number of tubes has to remain the same in all configurations in order to maintain input capacitance constant. TrS configuration is shown in figure 5.3.

The last configuration is Tube Stacking (TuS), where all connecting contacts are independent, so that each path between source and drain is completely independent. In this way, the probability of a short defect is decreased, but the feasibility of this configuration depends on the resolution of the fabrication process. This configuration can be seen in figure 5.4. This configuration also requires to maintain the same number of tubes as the PT configuration so input capacitance is not changed.

Stacking configurations do reduce the failure probability of transistors, however they can reduce performance up to four times, since the number of channels is halved so that the input capacitance is not changed (21).

## 5.4 Functional Yield analysis

Functional yield is calculated as a function of drive strength that the circuit requires, which is given by the number of CNTs needed, and as a function of the percentage of m-CNTs, which is usually defined by the fabrication process.

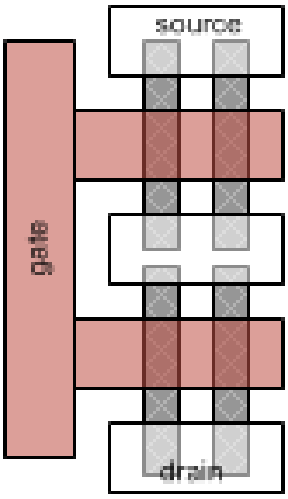


**Figure 5.3:** Transistor Stacking configuration

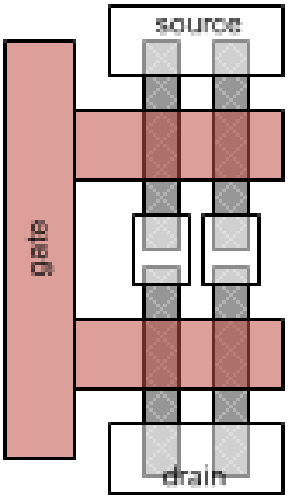


**Figure 5.4:** Tube Stacking configuration

If there is a finite number of metallic tubes, the logic gate has a finite delay penalty due to the current from the OFF network that does not appear when there are no m-CNTs. If the maximum delay ratio ($X_{max}$) is defined as the ratio of average delay in the presence of metallic tubes to the average delay without m-CNTs, for a given number of tubes in the CNFET, there is a maximum number of metallic tubes ($N_m$) that can be tolerated without violating the given delay penalty.

The power constraint is implied if it assumed that in an s-CNT, $I_{ONs} \gg I_{OFFs}$, and for a metallic tube $I_{ONm} = I_{OFFm} = I_{ONs}$.

Given the number of metallic tubes in a transistor, the probability of a network being functional in order to meet the delay constraint can be calculated. Such probabilities can be distinguished between the pull up and the pull down networks of a logic gate ($P_{PU}$ and $P_{PD}$, respectively). They can be calculated by adding the probabilities of a network being functional varying the number of tolerable metallic tubes from zero to $N_m$, as shown in equation 5.2, where $P_m$ is the probability of a tube being metallic, and $C_i^{N_{tur}}$ is the number of different combinations of having $i$ metallic tubes from the $N_{tur}$ number of total tubes in a transistor.

$$P_{PU/PD} = \sum_{i=0}^{N_m} (1 - P_m)^{(N_{tur} - i)} P_m^i C_i^{N_{tur}} \tag{5.2}$$

Finally, functional yield is obtained by multiplying the probabilities of the pull up and pull down networks since it is considered that a logic gate is functional if both networks are functional.

$$Y_f = P_{PU} \times P_{PD} \tag{5.3}$$

### 5.4.1 Yield analysis for an inverter

An inverter has the same configuration in its pull up and pull down networks, therefore the calculation of yield requires only one of them and square it, according to 5.3. Next, is the analysis made for a PT inverter, followed by the TrS and TuS configurations for that logic gate.

#### 5.4.1.1 PT inverter yield analysis

In an inverter both networks have only one transistor, so in order to calculate the maximum number of metallic tubes, equation 5.4 is used.

$$N_{m\_inv} = \lfloor N_{tur}(1 - \frac{1}{X_{max}}) \rfloor \tag{5.4}$$

The calculation of the probabilities of the pull up and pull down networks being functional is exactly the same. Equation 5.2 is transformed into equation 5.5 when $N_m$ is replaced by $N_{m\_inv}$. In this case the value of $N_{tur}$ used is the actual number of tubes in a transistor.

$$P_{PU/PD\_inv\_PT} = \sum_{i=0}^{N_{m\_inv}} (1 - P_m)^{(N_{tur}-i)} P_m^i C_i^{N_{tur}} \tag{5.5}$$

In this way, the functional yield of a Parallel Tubes inverter is obtained through equation **??**

$$Y_{f\_inv\_PT} = [\sum_{i=0}^{N_{m\_inv}} (1 - P_m)^{(0.5N_{tug}-i)} P_m^i C_i^{0.5N_{tug}}]^2 \tag{5.6}$$

In equation 5.6, $N_{tur}$ is replaced by $0.5N_{tug}$. These two values are equivalent for an inverter, considering that $N_{tug}$ is the total number of CNTs in the gate. Since each transistor has the same amount of tubes, $N_{tug}$ is twice the value of $N_{tur}$.

#### 5.4.1.2 TrS inverter yield analysis

In the TrS configuration, two transistors stacked on top of each other replace the single PT transistor. The number of tubes in the gate ($N_{tug}$) does not change so that the drive strength remains the same. As it can be seen from figure 5.5, the pull up and pull down networks have 2 transistors each now ($P_1$ and $P_2$ for pull up and $N_1$ and $N_2$ for pull down). Both networks are still the same in order to keep the same behaviour of the gate (inverter gate), so the analysis made for one network is valid for the other one. In this case, the pull up network will be analyzed and the same conclusions can be drawn for the pull down network.

The probability of PU network being functional depends on three conditions:

- The OFF current of transistor $N_1$ is smaller than $I_{OFF\_max}$.

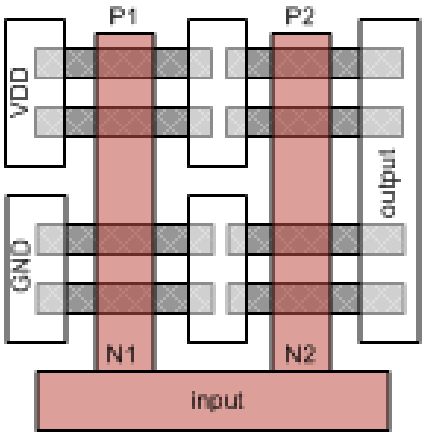


**Figure 5.5:** Transistor Stacking inverter

- The OFF current of transistor $N_2$ is smaller than $I_{OFF\_max}$.
- The OFF current of both transistors is smaller than $I_{OFF\_max}$.

The probability of the PU network being functional is then the addition of the probabilities of $N_1$ and $N_2$ being functional minus the joint probability of both transistors being functional, as shown in equation 5.7.

$$P_{PU\_inv\_TrS} = 2P_{PU\_inv\_PT} - P^2_{PU\_inv\_PT} \tag{5.7}$$

The functional yield of the transistor stacking inverter is calculated with equation 5.3 by substituting the probabilities of the pull up and pull down networks with the ones obtained with equation 5.7.

#### 5.4.1.3 TuS inverter yield analysis

In order for a TuS transistor to fail, both CNTs stacked on top of each other have to be metallic. Therefore, the probability of a double stacked tube failing is the product of the probability of one tube failing and the second tube also failing, as shown in the next equation:

$$P_{ms} = (P_m)^2 \tag{5.8}$$

The maximum number of metallic tubes allowed is obtained by using $N_{turs}$ (number of double stacked tubes in a transistor) in equation 5.4 instead of $N_{tur}$.

Finally, by using the value of $P_{ms}$ calculated with equation 5.8, the functional yield is obtained with equation 5.6, as shown next:

$$Y_f\_inv\_TuS = [\sum_{i=0}^{N_m\_inv} (1 - P_{ms})^{(0.5N_{tug}-i)} P_{ms}^{i} C_i^{0.5N_{tug}}]^2 \tag{5.9}$$

# Chapter 6

# Results and analysis

This chapter is divided in the same way as the first chapters of this written work. The first section delivers and analyzes the results of adding redundancy at the transistor level in CNFETs. Next, yield is discussed and the last section talks about power consumption of these circuits.

The tools used in this project were HSPICE, a tool to simulate circuits, in which the Stanford CNFET model was used to build and analyze circuits. The probabilities and yield were calculated using MATLAB scripts according to the analytical models discussed in previous sections.

## 6.1 Effects on reliability of adding redundancy

Using the models discussed in chapter 4, the probability of an open defect was calculated for four structures: series, parallel, SP and PS. It has been shown that when taking into account correlation, the probabilities of the four kinds of structures (CSIP, ISPC, CPIS IPCS) as well as the probabilities for the ISP and IPS structures are equal to the ones for SP or PS, therefore, the results discussed in here also apply for such structures.

Figure 6.1 shows the variation of open defect probability while varying the number of redundant transistors. It can be seen that in presence of open defects, the series structure failure probability increases, which implies that this structure is not suitable for circuits prone to that kind of defects. On the other hand, the failure probability of the parallel and SP structures decrease when adding more redundancy. The parallel-series structure has a specific value of redundancy for which the failure probability

under open defects is minimized. Adding more redundancy after such value decreases reliability.

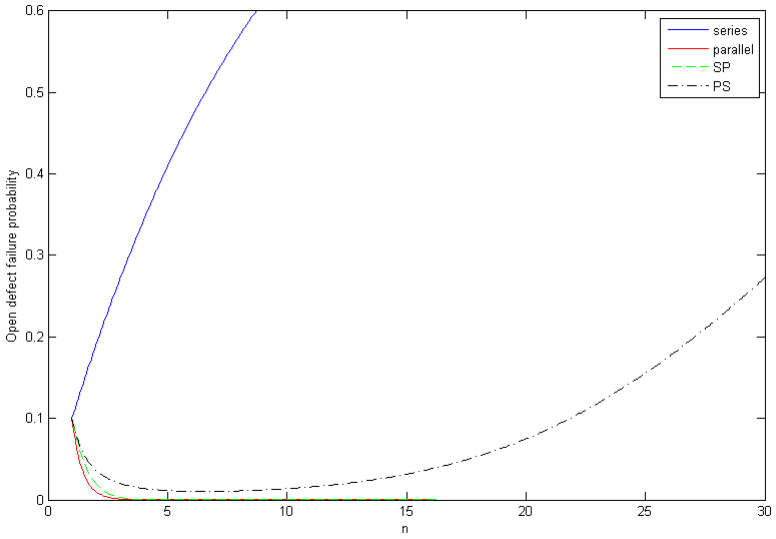


**Figure 6.1:** Open defect failure probability variation with respect to redundancy for various structures.

Regarding the failure probability due to short defects, it can be seen in figure 6.2 that as the amount of redundancy increases, the parallel structure is more prone to fail, so it is not suitable to increase reliability in circuits that have high short defect probabilities. The series and PS structures, however, are suitable to mitigate this kind of defects. By adding more redundancy to both these structures, the short defect failure probability keeps decreasing. This time, the SP structure has a certain amount of redundancy, in which the short defect failure probability is minimized.

Next, the total failure probability (i.e. the combination of both open and short defects) was calculated. Figure 6.3 shows that the series and parallel structures do not decrease the reliability of the circuit when more redundancy is added. On the other hand, the SP and PS structures show that by adding redundancy up to an optimized level where failure probability is minimum.

These results are based on the assumption that the open and short failure probabilities are equal to 0.1, thus figures 6.1 and 6.2 start at 0.1. Since figure **??** is the

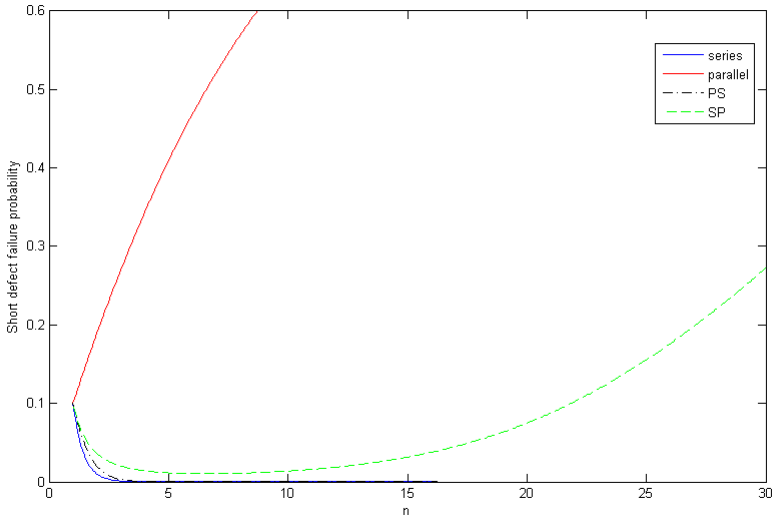


**Figure 6.2:** Short defect failure probability variation with respect to redundancy for various structures.

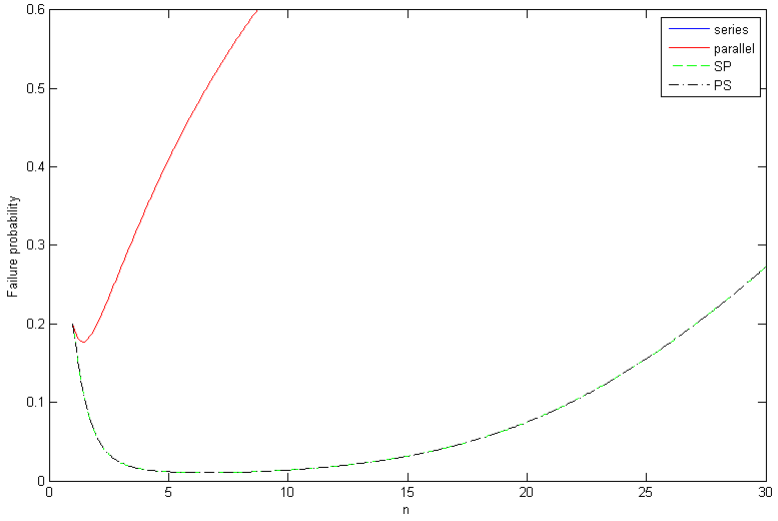


**Figure 6.3:** Failure probability variation with respect to redundancy for various structures.

combination of the previous two, the graphs start at 0.2.

If we vary the values of $P_O$ and $P_S$ simultaneously and analyze the failure probability of IPS and ISP structures, as defined in chapter 4, we obtain figurefig:mesh. The plot shows the subtraction of the failure probability of the Independent Parallel-Series structure minus the failure probability of the Independent Series-Parallel structure, in order to compare the behaviour of these structures. It can be seen that when the open defect probability increases, the failure probability of the ISP structure is bigger, thus the subtraction becomes negative (blue section of the plot). When the short defect probability increases, the failure probability of the IPS structure is bigger, therefore the subtraction function is positive (red section of the plot). When both probabilities are of the same value, the failure probability of both structures is the same, that is why the value of the subtraction is zero (green section of the plot).

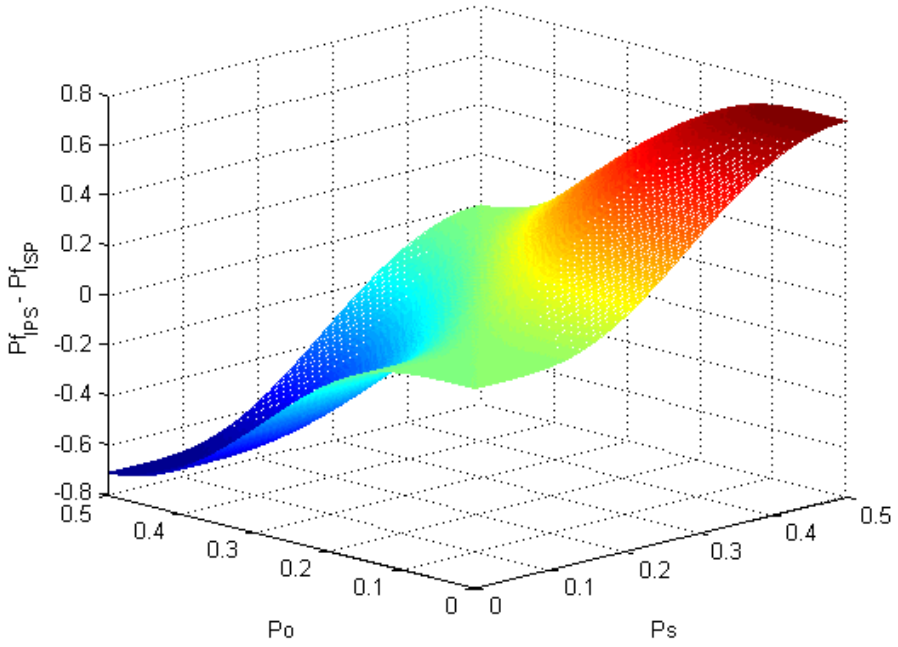


**Figure 6.4:** Plot of $P_{F\_IPS} - P_{F\_ISP}$ for different values of open and short defect probabilities.

From figure 6.4 we can deduce that when a fabrication process is more prone to short defects, then the ISP structure is more suitable for increasing reliability of the

circuit. Having a bigger $P_S$ means that the fabrication is prone to metallic CNTs, which would mean that no removal technique as the ones explained in section 3.6 has been applied. When one of such techniques is used in the fabrication process, then $P_S$ would be minimized and the IPS structure would be more suitable to increase reliability. Finally, it is evident that a fabrication process which has the same probability of having an open or a short defect, then any of the two structures would be suitable to minimize failure probability.

## 6.2 Yield analysis

Increasing reliability also means increasing yield. In this project, yield was analyzed with the model presented in chapter 5. Using the equations explained in that section, and assuming the $X_{max}$ value to be 1.3 and the probability of a tube being metallic equal to 4% then we obtain the plots shown in figure 6.5, where the blue line corresponds to the yield of the PT configuration, the green line to the TrS configuration, and the red line to the TuS configuration.

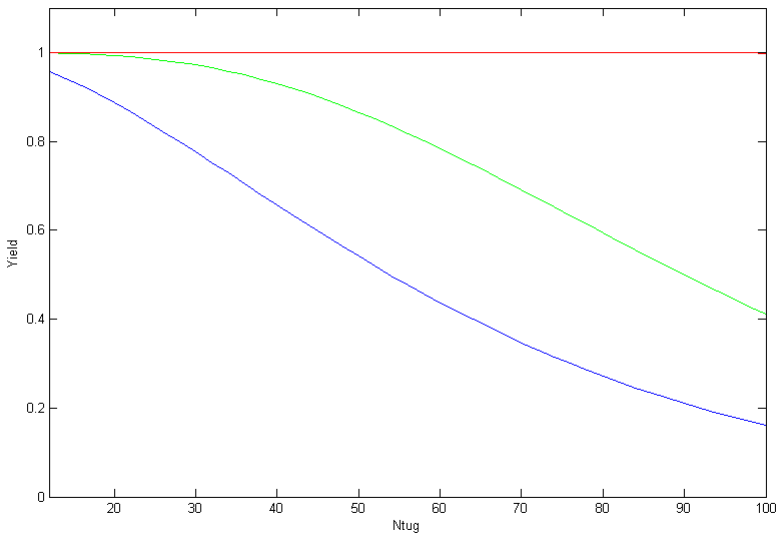


**Figure 6.5:** Yield analysis for PT, TrS and TuS configurations while increasing the number of CNTs in an inverter with $X_{max}$=1.3 and $P_m$=0.04.

Firstly, it is evident that stacking helps increase yield, since both transistor and

tube stacking configurations have a higher yield than the parallel tubes configuration. The TuS configuration is the one that has the higher yield, as it can be seen in figure 6.5. However, the feasibility of the TuS configuration depends on the resolution of the technology. If the fabrication process has a low resolution, then the TuS configuration would not be suitable. Figure 6.6 shows the same analysis with $P_m$ equal to 10%. As expected, if it is more probable to have a metallic tube, then yield decreases, but the stacking configurations still produce more yield than the PT configuration.

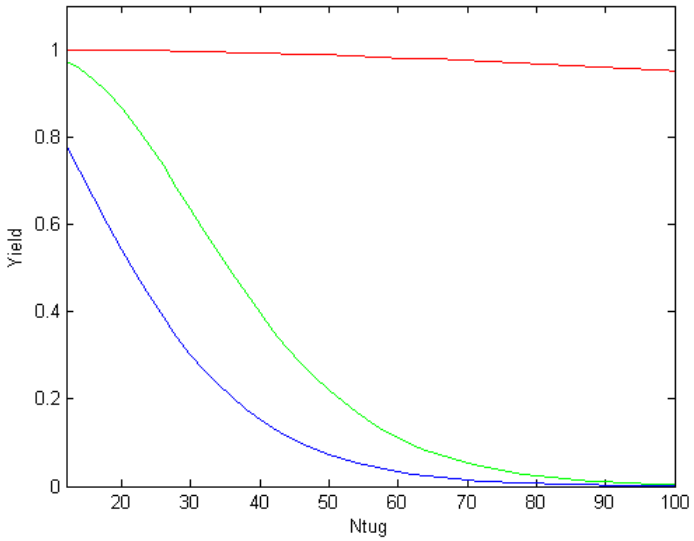


**Figure 6.6:** Yield analysis for PT, TrS and TuS configurations while increasing the number of CNTs in an inverter with $X_{max}$=1.3 and $P_m$=0.1.

## 6.3 Power and area

It is clear that when more metallic tubes appear in a CNFET, the power consumption increases, since there is current flowing regardless from the transistor being on or not. m-CNTs imply a certain leakage current. Figure 6.7 shows the Monte Carlo analysis of an inverter switching with different number of metallic CNTs. It can be seen that the output varies from the value that one would expect to get from an inverter in presence of different number of m-CNTs in the transistors of the gate, which implies static power consumption.

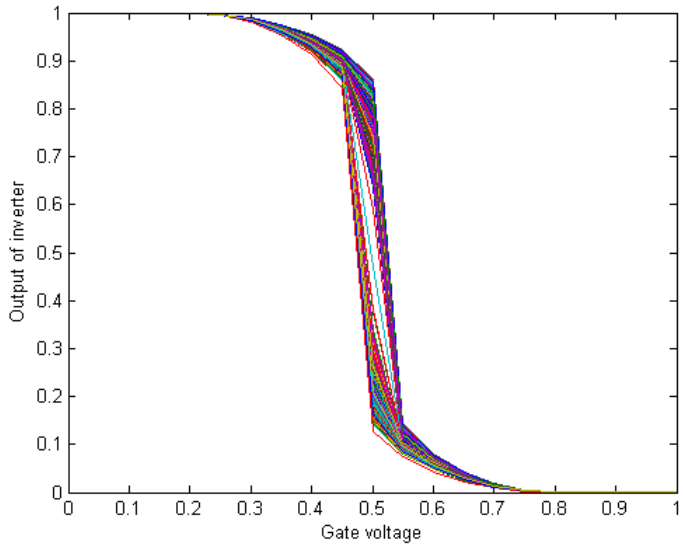


**Figure 6.7:** Monte Carlo analysis of a switching inverter made with CNFETs

On the other hand, analyzing the $N^2$ structures previously discussed, it can be seen that the current decreases with the number of CNTs in series, while it increases as the parallel CNTs increase. So, the drive current of an $N^2$ structure is the same of a CNFET, as shown in equation 6.1. This shows that there is no power penalty when using this kind of structures to improve reliability.

$$I_{drive} = \frac{n}{n} * I_{CNFET} = I_{CNFET} \tag{6.1}$$

In terms of area, however, it is clear that an $N^2$ structure will consume more space than a single transistor. If we define the area of a single transistor in terms of its length (L), width (W), and minimum feature size of the fabrication technology (F), as shown in equation 6.2, then the area of the ISP and IPS structures will increase according to equations 6.3 and 6.4 respectively.

$$area_{CNFET} = (L + 4F)W \tag{6.2}$$

$$area_{ISP} = (L + 4F)(((n * W) + F) * n) \tag{6.3}$$

$$area_{ISP} = (L + 4F)((n * (W + F)) * n) \tag{6.4}$$

Regarding the area overhead of the layout configurations, the stacking configurations will be twice as long as the PT configuration, but half as wide as the PT configuration, since the amount of CNTs used has to remain the same in order to maintain the same drive current.

# Chapter 7

# Evaluation of the work

This chapter discusses the work made throughout the course of the project, in terms of the choices made, the results obtained and whether the aims and objectives drawn at the beginning were met.

## 7.1 Choices made

During the initial stages of the project, when the literature review and interim report writing were taking place, the project was much wider. The objective was to enhance the reliability of nano-technologies, not only of CNFETs, but of many if not most of the novel nano-scale circuits, such as GNR transistors, nanowire transistors, Single Electron Transistors, molecular devices, etc. (22, 23, 24, 25, 26). The way to do this was drawn out to use traditional redundancy techniques on a gate, unit or higher levels, such as Triple Modular Redundancy (TMR) (27), and analyze the new structures using a probabilistic modeling approach, through a set of MATLAB tools (28, 29, 30).

However, right at the beginning of the project, this seemed to be too broad for a project of this nature, therefore, it was decided to only concentrate on CNFETs, which literature review points to them being very promising technology. In order to do this change, a review of CNFETs and their behaviour was needed, so a certain amount of effort and time went to thoroughly understanding this kind of nano-technology.

Also, certain articles found during this literature review pointed to the fact that redundancy at lower levels was more suitable and effective to improve fault tolerance, as discussed in chapter 4. Therefore, this approach was taken to carry out the work.

Since this choice was made, the probabilistic models to analyze reliability were taken from basic reliability and fault tolerance theories rather than nanolab, the automated tool, even though MATLAB was still used for this purpose.

These choices made it possible to finish the project on time and with specific results consistent with the literature.

## 7.2 Discussion of results

The results obtained in this project and explained in chapter 6 indicate an improvement on reliability of CNFET circuits through the techniques used and explained in chapters 4 and 5. In the results section, the impact on power and area of the techniques used is also explained. Results are consistent with literature and indicate design choices according to the fabrication process to be used. For example, whether the fabrication process applies metallic CNT removal techniques, or whether its resolution is sufficient to create the contacts needed in the TuS configuration. Once this is established, the designer can decide which reliability enhancement technique to use.

## 7.3 Evaluation

In order to meet the main aim, several objectives were drawn at the beginning of the project. A literature review was made to understand the need of reliability enhancement in CNFET-based circuits. This was also needed during the main stage of the project due to the change of direction explained previously. In the literature review fault tolerant techniques were studied, along with reliability assessment techniques through probabilistic models, needed to analyze the new structures.

The second part of the main stage of the project was to study the behaviour of CNFETs and circuits built with them. This was made through the Stanford CNFET model, as previously explained. This model explains the behaviour of the channel, which is the main difference between this kind of technology and Silicon-based CMOS. Also, the impact of m-CNTs and undeposited CNTs on the capacitance of the transistor. This, due to the fact that the capacitance plays a major role in the model of the drain current of the transistor.

Next, reliability enhancement techniques were applied on circuits and analyzed as the literature pointed. The results showed that reliability was improved with the work carried out, therefore the objective was met satisfactorily.

With the analysis made, design suggestions could be drawn out for specific fabrication methods, and their techniques used to mitigate defects from the fabrication point of view.

In general, the aims and objectives were properly met. Reliability of CNFET-based circuits was improved.

# Chapter 8

# Conclusions

This written work presents techniques to enhance and assess reliability of circuits made with Carbon Nanotube transistors. Reliability enhancement is done by redundancy, which is a fault tolerant technique based on replicating the circuit. It was found that $N^2$ transistor redundancy is the best choice to improve reliability. Specifically for CNFETs, correlation is a factor that needs to be taken into account in order to design appropriate design structures to increase, rather than decrease, reliability through redundancy. It was seen that if the fabrication process used is capable of removing metallic CNTs, then the IPS structure is the best option for reliability enhancement. If there is no m-CNT removal then the ISP structure is the more suitable.

As reliability is improved, the yield is also enhanced. Layout configurations were analyzed in order to observe and decide the best option to improve yield for a given fabrication process. It was understood that the shared tube configuration is very prone to failure, since a single tube is used for several transistors; therefore, reliability is dependent on the nature of such CNT. When several tubes are used in a transistor, such as in the PT configuration, then the configuration is less likely to fail. However, yield is best improved when using stacking configurations. Out of these, the tube stacking configuration was found to be the best option, however its feasibility depends on the resolution of the fabrication process to build the small contacts needed. If this is not the case, transistor stacking configuration would be most fitting.

Finally, power and area trade offs were analyzed. It was seen that an $N^2$ structure does add a big amount of area simply by the fact of replacing a single transistor with $N^2$ transistors. Drive current however is not affected by the new structure. In terms of

layout configurations, area is not affected since the number of CNTs has to be consistent in any of the configurations in order to keep the drive current constant.

## 8.1 Future work

The work carried out in this project was limited by the amount of time to submit results. This could be an ongoing project to enhance even further or automate enhancement of reliability for CNFET circuits. Future work could include the following points:

- Detailed analysis of overheads such as power and area, done while simulating CNFET-based circuits.
- Transport the analysis made to a design tool, such as HSPICE.
- A tool that automates the analysis explained in this work.
- Creation of design and synthesis tools so that CNFET-based circuits can be designed using schematics and layout schemes.

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