Abstract

The aim of this project was to research and explore variability aware design optimization of Voltage controlled Oscillator (VCO) in Nano-CMOS, compare the performance of different kinds of VCO. In this dissertation, performance metrics mainly includes frequency and power consumption.

VCO designs can be divided into single-ended ring oscillator and three kinds of double-ended ring oscillators, which uses triode load, symmetric load and combine cross-couple differential delay cell with symmetric loads respectively.

Experiments show the attributes of VCO, get a design that has robust process variation tolerance ability through comparison, and compare the power consumption of each design.

Although this project get certain extend of success in Nano-CMOS VCO, there is still a great deal of room for growth in Nano-CMOS technology. Suggestions for the future work of this project are given finally.

Table of Contents

Chapter 1: Introduction, Motivation and Aims

1.1 Project summary

Recently, technology of electronics needs higher and higher demand on performance enhancement of analogue and mixed signal circuits, these complex integrated circuits contain billions of transistors with line widths of less than 100nm. In addition, modern CMOS technologies are dominated by the nanoscale CMOS with line widths of 45nm and below. To many electronic systems, the performance of Nano-CMOS transistors is very important, which affects both time to market and product cost, especially for SoC (system-on-chip) designs. The operation of analogue circuits is very sensitive on mismatches between the components and their dynamic range is limited by noise, offset and distortions. With technical progress, Nano-CMOS transistors are being used on both digital circuits and analogue circuits, and the designs based on Nano-CMOS will make the situation more complex [1, 2].

VCO (voltage-controlled oscillator) is an electronic oscillator that there are correspondence between the frequency of output and input control voltage. VCO is mainly consisted of CMOS circuits; it usually has three kinds of structures, single pMOS, single nMOS, pMOS and nMOS current multiplexing structure. VCO has been widely used in many kinds of electronic device. For example, VCO is an important part of RF circuit, which can change the frequency of the circuit according to the voltage of input signal. In addition, to PLLs (Phase-locked loops), which are essential components of typical SoCs operating in synchronous mode [3]; VCO is also a major element.

To electronic system, improve performance and reduce energy consumption are quite crucial, however, it is impossible to test these circuits in hardware, which is time-consuming and costly. Actually, people usually simulate and analyse the circuits on software first. With the development of microelectronic technique and the enhancement of the scale of integrated circuit, it will have higher design demand to the performance of circuits; some high level software will be used as well.

On the demands of highly integration systems, the frequency will increase constantly, which leads to more power consuming, and brings the problems of overheating. The fault rate increases 2 times per 10□ increment of temperature [4]. This project focuses on an active area of analogue and mixed signal circuits, in order to optimize the power-performance values of the circuits systems, which using nanoscale CMOS voltage controlled oscillator (VCO) to research the efficient simulation and characterization. This project can be used for fast and accurate estimation of power-performance values of nano-scale CMOS design alternatives of digital systems. This project mainly needs to use two kinds of software, Hspice and Matlab. Hspice is a kind of traditional software; it was developed at the Electronics Research Laboratory of the University of California, Berkeley by Laurence Nagel with direction from his research advisor, Prof. Donald Pederson. In industry the circuits need to

be simulated with Hspice to test the working condition at the transistor level first, and then the designs can be used to manufacture. In this project, Hspice is used to simulate circuits and analyse performance, such as steady-state analysis, transient analysis, and transient analysis and so on. Hspice can also generate the waveforms of output, delay time, etc. Matlab is a kind of computer programming language. In this project, Matlab loads the signals that generated by Hspice and does some postprocessings. According to the results, some parameters of Nano-CMOS can be modified to optimize the circuits.

1.2 Aims and Objectives

The overall aim of this project is to research and explore a variability aware design optimization of different kinds of VCO in Nano-CMOS. Test the factors that affect the performance of the system and focus on the process variation tolerance design of VCO. In general, the objectives of this project can be summarized as four points:

1. The first key aim of this project is to implement existing designs and its performance analysis to compare the process variation effects. Be familiar with the software and related circuits through simple operation and analysis first, in order better to understand the overall concept of this project.
2. The second key aim of this project is to develop methods and techniques process variation tolerance in a VCO. In this part, according to the tests before, some extend design can be analyze and design process variation tolerance effects.
3. The overall objective of the project is to develop a robust process variation tolerant design of VCO and implement using state of the art design tools and to determine if an adaptive-aggressive scaling strategy can be used for future scaled technologies.
4. If time permits, further research will be undertaken in this area.

This project is based on experiments by using software, thus, skilled with Hspice and Matlab is the first step. The results of this project need a great amount of data, which should be generated by software, and make innovations to optimize the performance of the circuits.

1.3 Organisation of this dissertation

This dissertation consists of four main parts.

Firstly, in the next chapter the background of this project will be introduced and the overview of the relative methods and principle will be described, and used circuits as well. Some previous work are also been presented.

Secondly, Chapter 3 introduces the detailed designs of this project, the aims

of this project and how to achieve them. In addition, the detailed experiments steps and examples are also been explained.

Thirdly, the results of experiments will be given in Chapter 4. And analysis about these data will be explained as well.
Then, an evaluation of this project and a conclusion for this project will be given in chapter 5.

Finally, some further work suggestion will be given that possible to improve the performance of this experiment.

Chapter 2: Background and Previous Work

2.1 Milestones in Nano-CMOS area

To the development of semiconductor industry, process dimension of silicon technology is getting smaller and smaller, which has entered the era of Nano-CMOS, it is a technical revolution in the history of modern industry. The dimensions of the device have been reduced to a millionth in the past 100 years [5]. Nowadays the widths of 40nm CMOS has already been in mass production, and sub-10 nm transistors expected at the 22 nm technology node, which is scheduled for production in 2018, and 4 nm transistors have already been demonstrated experimentally [6, 7].

At the same time, the performance of the circuits is higher and higher, which needs huge power consumption by the increment of the clock frequency and the chip density. However, this significant increment in power density will cause the insufficient supply voltage reduction. One way to solve this problem partially is using cooling technologies, and low power technology is another way, which is more efficient but different to implement [5].

2.2 Introduction of Process Variation

In actual circuits, there are no two components that are absolutely the same. In fact, there will be significant variation from die to die and from wafer to wafer due to process-variability [8]. In addition, even if the characteristics are identical, the characteristics will also diverge with time as defects accumulate within the components in response to activity of nodes and input patterns [9–13]. Nowadays process variation has become a basic problem of Nano-CMOS technologies, which limits the performance of integrated circuits. Process variation can lead to unexpected faults, so if ignore process variation in the test, some faults cannot be detected, which will lead to system failure. Unfortunately, the process variation is unavoidable and also hard to model or predict, that is because there are too many factors contribute to process variation, it is intractable to model or predict process variation, a better way to research it is using simulation experiment.

Generally, there are two main sources of process variation, one is the physical factors (intrinsic variation), the other is environmental factors (dynamic variation). The physical factors are permanent, which are caused by fabrication process. As the technology scales of Nano-CMOS, the significant size decrease is requiring more sophisticated fabrication process, it is impossible to avoid the process variation with the current fabrication process technology. Physical factors mainly include effective channel length, threshold voltage, oxide thickness, and so on. Environmental factors mainly include temperature, power supply, switching activity, and so on. In this dissertation,

only physical factors are considered because these factors are major factors that affect the system [14].

There are four ranges of physical variations in general, which are Within-Die Die-to-Die Wafer-to-Wafer and Lot-to-Lot variations. In nanometric transistors, process variations can be classified into two categories basically: Inter-Die variations and Intra-Die variations. Both of them are independent of device location. Inter-Die variation is across different dies that means that all CMOS transistors are sharing the same random variable related to one process parameter. As opposed to Inter-Die variation, Intra-die variation occurs within a single die then each transistor has unique random variable.

2.3 Implement of Process Variation

2.3.1 Monte Carlo Simulation

Monte Carlo Simulation (probability simulation) is a method that has been proposed to simulate process variation and calculate frequency and average power statistically [15, 16]. Monte Carlo simulation is a kind of stochastic simulation, which is a computing method based on principle of probability and Statistics.

For process variation, the model distributes randomly, a random value, which based on the range of the estimates, can be generated discretionarily and be selected for each task. Save the result of each task and repeat this procedure with different random value then the process variation can be simulated. Generally Monte Carlo simulation repeats the model for thousands or ten thousand with different random values. In this project, ten thousand times simulation is chosen for simulating process variation.

The results of Monte Carlo simulation are vast amounts of data; after treatment these data are used to describe the tendencies or distributions of the model. In this project, Monte Carlo simulation is specially used to simulate the variable changing with process variation.

2.3.2 Gaussian Distribution

As stated above, Monte Carlo simulation selects a random value based on a range of the estimates, for process variation, this range can be defined by Gaussian Function, which is used to describe physical events when the number of events is large. The function shows below:

$$f(x) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \tag{2.1}$$

where μ is mean value and σ is standard deviation. This function is a

probability density function. When the scatter of data depends on independent and equally weighted factors, the distribution will be a bell-shaped curve. Most data distributed centrally in the vicinity of the mean value, the farther away from the mean value, the sparser data are. According to the different concentration ratio, the Gaussian distribution will be various. The Figure 2.1 shows the Gaussian distribution in different values of σ, the value of blue one is 0.8, and the value of red one is 1.2. It can be seen clearly that the less σ represents a more concentrated distribution.

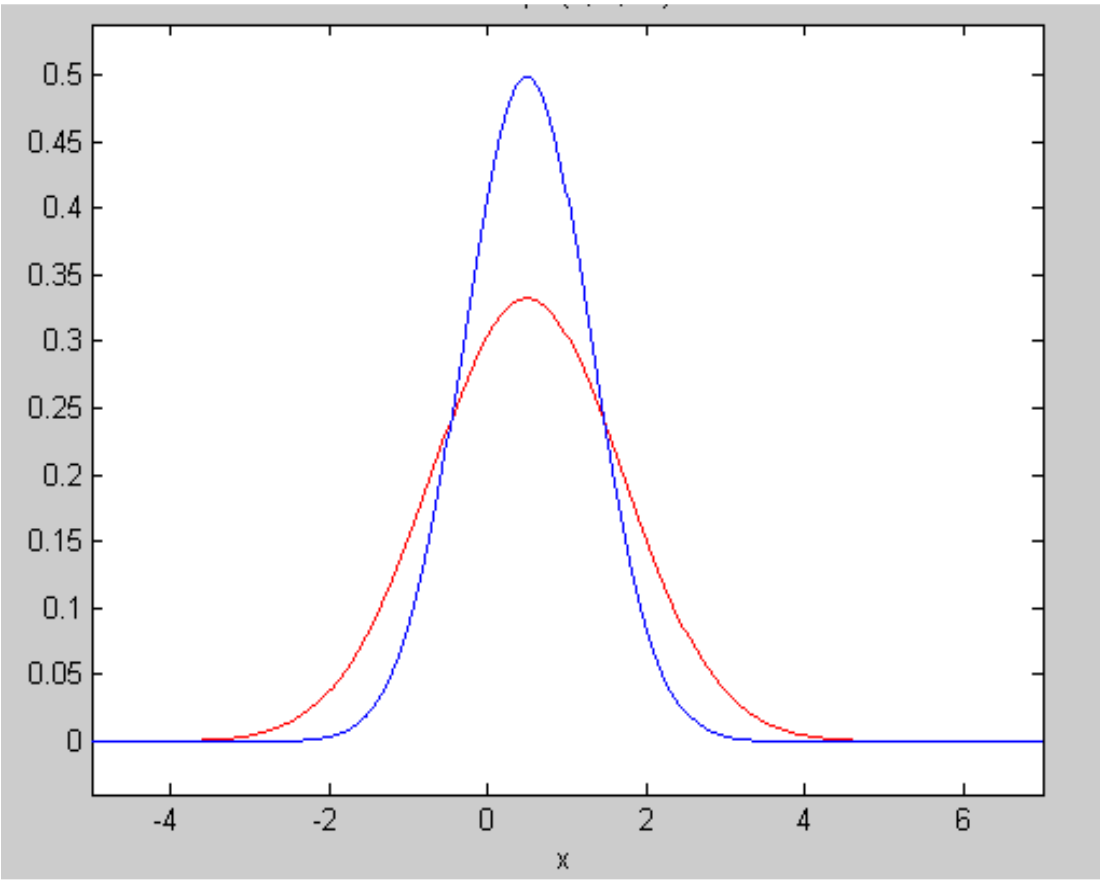
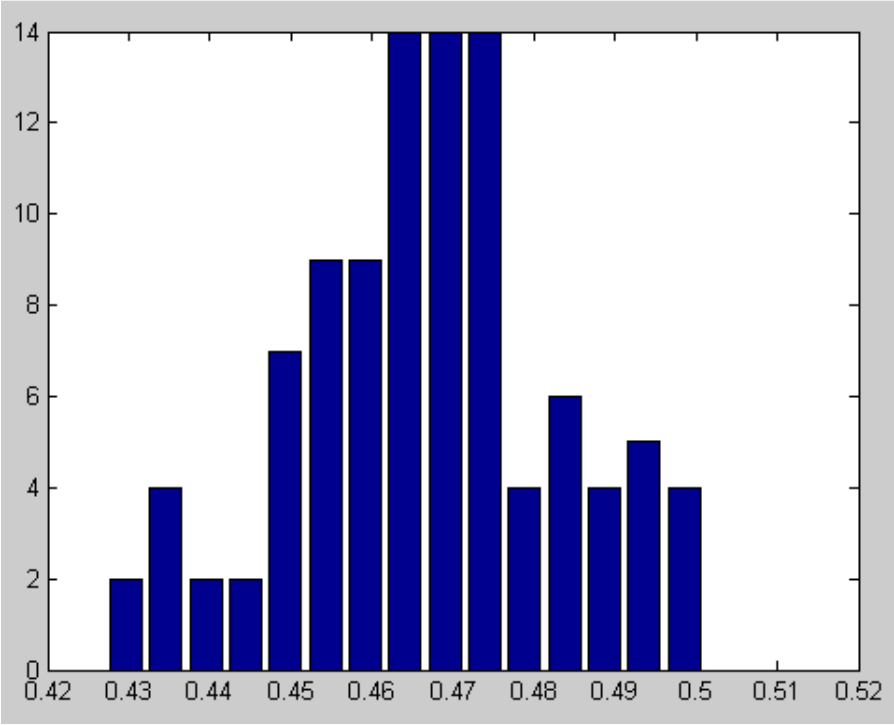


Figure 2.1
Gaussian distribution in different σ

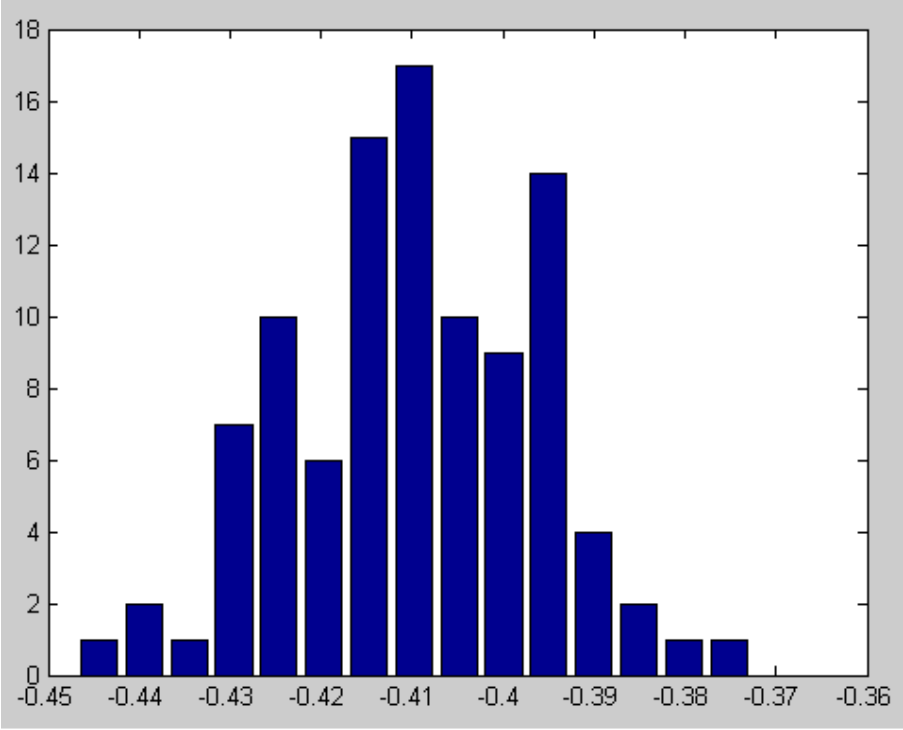
In the simulation of this process variation, the variation chooses 10% and the deviation is 3 σ. In this situation, when the mean values of threshold voltage are 0.22 and -0.22 for NMOS (nvt) and PMOS (pvt) respectively, the distributions are showed in Figure 2.2(a) (b), this is the result of 100 times simulation, and Y-axis means the times of that case happened in the relative region. This result is using Monte Carlo simulation to run 100 times, as can be seen from the figure, varying the values of nvt and pvt simultaneously with Gaussian distribution, through 100 times is not enough to get a quite precise result, the distributions are roughly bell-shaped curve.

Because of the variation of nvt and pvt, power consumption and frequency of the system are also changed, see Figure 2.2(c) (d), it can image that these variation will extremely affect the stability of the system. The details will be

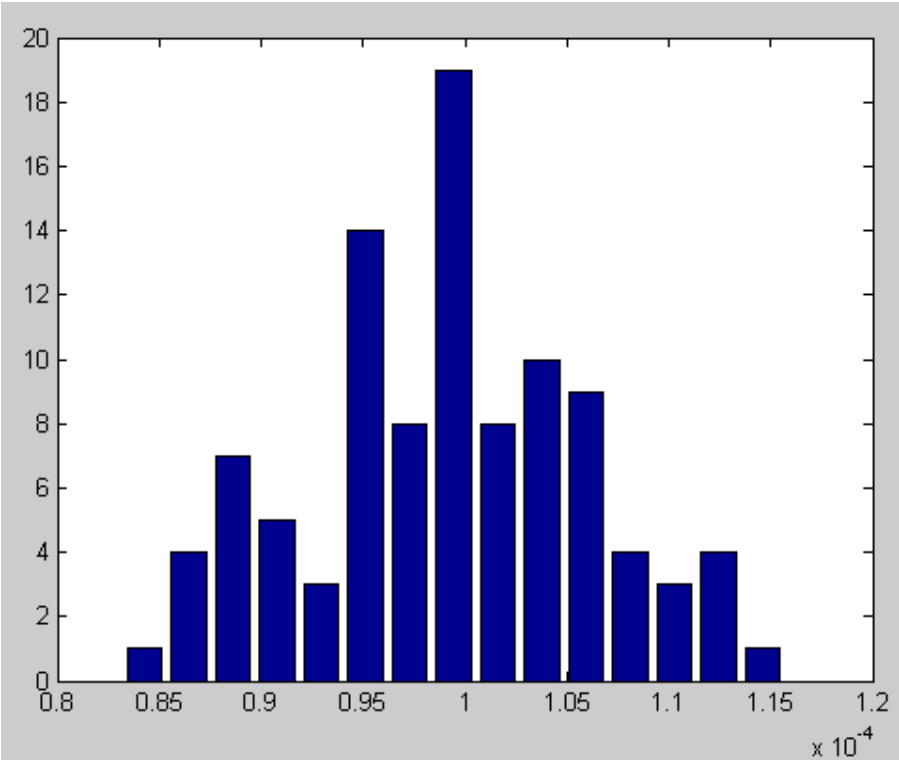
given in the next chapter.



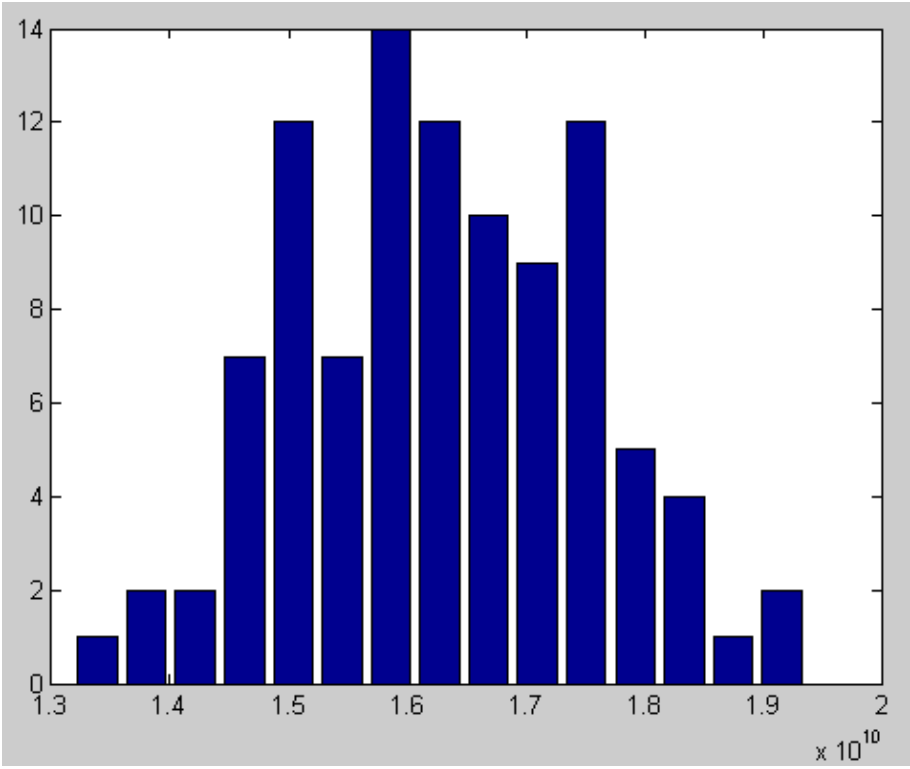
(a) NMOS



(b) PMOS



(c) Power consumption



(d) Frequency

Figure 2.2
Threshold Distribution with Process Variation

2.4 Integrated VCO Circuit

2.4.1 VCO Study

Voltage controlled oscillator (VCO) circuits are the objective system of this project. VCO is one of the most important parts not only for digital but also for radio-frequency integrated circuits (RFICs) [17]. In addition, VCO is used to be the oscillating part of all kinds of automatic frequency control (AFC) system, such as PLL system.

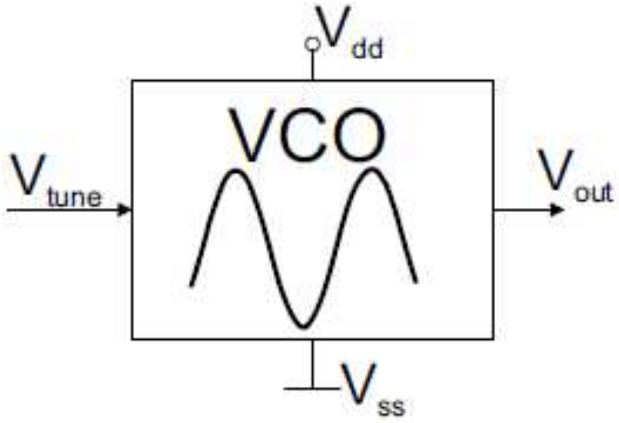


Figure 2.3 [18]
Basic VCO

Basic VCO can be depicted as Figure 2.3; it has an input and a periodic oscillating output (V_{tune} and V_{out} in the figure). V_{dd} and V_{ss} are used to connect power supply. VCO is a circuit that has an output without any inputs, so it needs some situations to make it oscillates by itself. So how it works? It can use transfer function to analyze. Suppose the open-loop transfer function of VCO is H(s), then closed-loop transfer function can be described below:

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 + H(s)} \tag{2.2}$$

As can be seen from Formula 2.2, when H(s) = -1, the output is infinite, then the negative feedback has changed into positive feedback, so if any nodes of the system occurs a jitter, it will make the system begin to oscillate. It is not allowed in operational amplifier; however, positive feedback is an essential condition of VCO systems.

In general, a negative system has to satisfy the Barkhausen Criterion for oscillation [18]. The first condition is that $|H(s)| \geq 1$; the other one is that the open-loop phase deviation is 180 degrees. In order to tolerant the influences that caused by deviation of process and temperature, and the other nonlinear factors, the open-loop gain usually is more than 2 times of the theoretical value.

The performance evaluation of VCO mainly includes adjustable frequency range, output power, frequency stability, phase noise, spectrum purity, regulating speed, frequency pulling etc. In this project, frequency is primary research objects that used to measure the performance of VCO. Frequency can be controlled by adding storage elements. Generally, add variable capacitance diode in the oscillatory circuit, and applied voltage in this diode can make the capacitance of the diode change, and then the oscillating frequency will change as well.

Then basic discussion about calculation about VCO will be introduced. VCO time-domain equations are described below:

$$V_{out}(t) = V_o \sin(\omega_c t + \varphi) \tag{2.3}$$

where φ is phase, V_o is amplitude and ω_c is angular carrier frequency, which is

$$\omega_c (V_{tune}) = 2\pi f_c(V_{tune}) \tag{2.4}$$

where f_c is centre frequency.

Ideal sinusoidal VCO is:

$$V_{out}(t) = V_o \cos[2\pi f_c t + \Phi] \tag{2.5}$$

where Φ is a fixed phase.

However, actually $V_o(t)$ and $\Phi(t)$ will generate fluctuations, then the frequency will fluctuate close f_c with symmetrical distribution around (Figure 2.4).

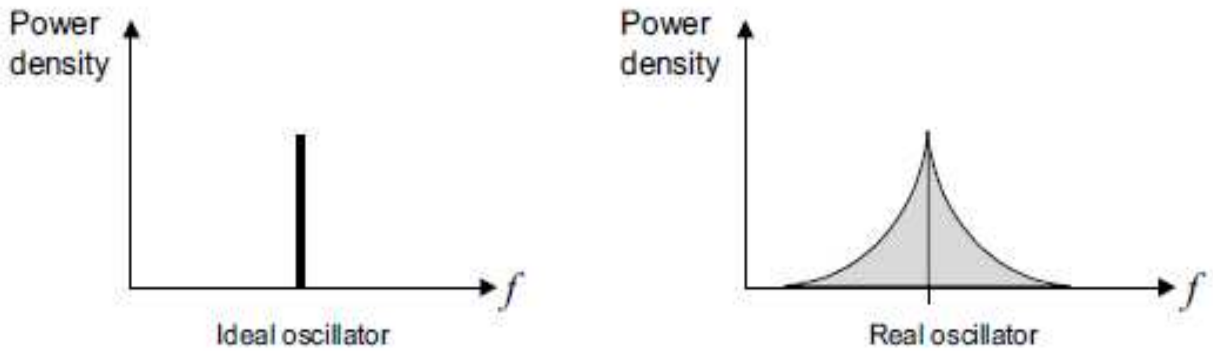


Figure 2.4 [18]
Frequency fluctuation with symmetrical distribution around

Generally, frequency variations are usually caused by signal sideband noise spectral density that normalized to the carrier signal power [18]. It is defined as

$$L_{total}(f_c \Delta f) = 10\log\left[\frac{P_{sideband}(f_c + \Delta f, 1Hz)}{P_{carrier}}\right] \quad (3.4)$$

where $P_{carrier}$ is the signal power when the carrier frequency f_c and $P_{sideband}$ shows the power of single sideband, which has an offset □f from f_c and a 1Hz measurement bandwidth.

2.4.2 Common VCO Models

LC Oscillators

LC Oscillators are crucial blocks in high performance communication systems. A basic LC VCO is depicted in Figure 2.5, which contains an inductor, a capacitor and a couple of resistance. Generally, this circuit will oscillate through the conversion of electric field energy and magnetic field energy. There is no current before it is plugged in, when it is connect to power, inductor will generate a back electromotive force that is as high as the voltage of power, the current in this branch will increase from 0; on the other hand, there is no charge in the capacitor at the beginning, then it starts to charge and generate a back electromotive force gradually, and the current will decrease as well. Then disconnect the power when the status of the circuit is stable, the capacitor starts to discharge, and generate a circuit that decreases gradually, then inductor will generate an electromotive force again to block the change of current, this electromotive force can charge the capacitor renewedly. This procedure goes in cycle, the circuit is oscillating.

The resonant frequency of LC oscillator with an inductor-capacitor circuit is:

$$\omega_0 = \sqrt{\frac{1}{LC}} \quad (2.6)$$

LC oscillators have a quite limited tuning range; however, the phase noise is low at low power consumption [18].

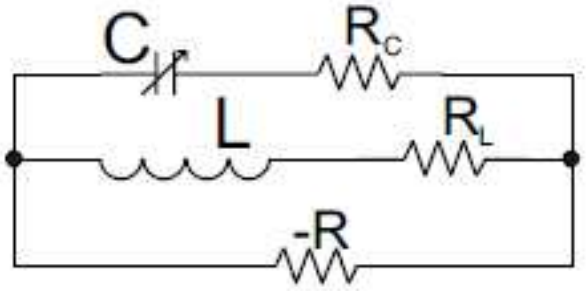


Figure 2.5 [18]
LC Oscillator

Ring Oscillators

Another one of classical oscillator designs is that connect NOT gates or inverters in a chain, and the last stage output needs to feed back to the first one. The oscillation will happen when the phase shift over the chain exceeds 360^{o} due to Barkhausen's criteria [19]. So the number of the stages must be an odd number. This kind of VCO is the main research object of this project.

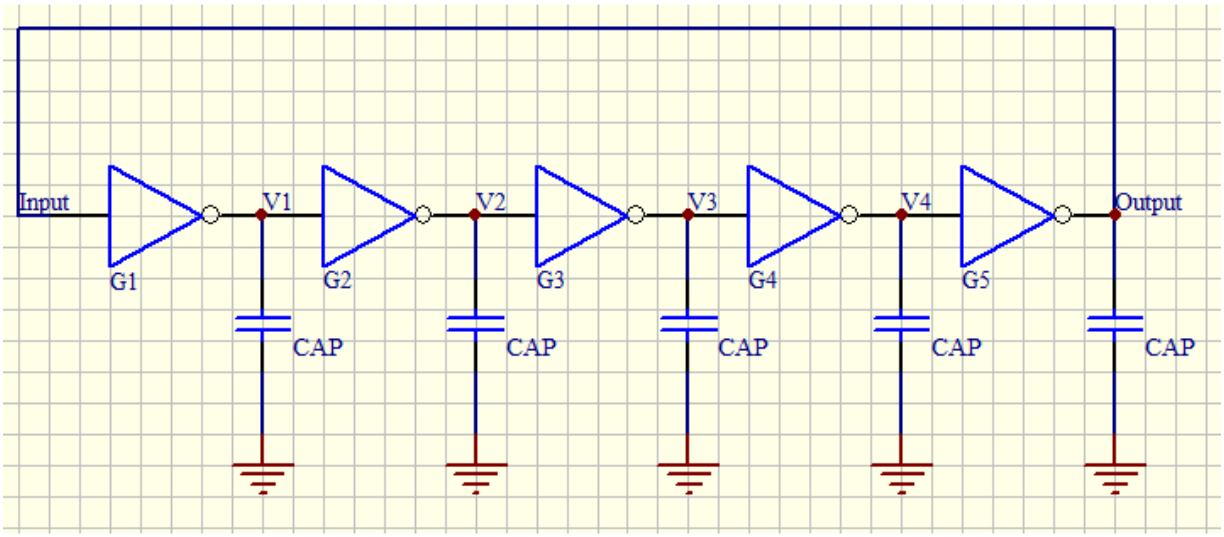


Figure 2.6
Five-Stage Ring Oscillator

Take a five-stage ring oscillator as an example, which is depicted in Figure 2.6. Ring oscillators use the principle of inherent transmission delay time of gate circuit, connect odd number of inverters, each inverter is a delay stage, and the capacitors can be used to adjust the frequency, increasing capacitance will increase the charge & discharge time then decrease the frequency.

This circuit will not be stable. When there is no oscillations happen, the inputs and outputs of these inverters are impossible to stabilize in high level or low level, which can only stand between high and low level and stand in amplifying mode.

It can assume that there is a redundant positive leap in V1, through the transmissions of G2 with a delay time(t_{pd}); V2 generates a larger negative leap and delay a little time(t_{pd}), it can infer after $5t_{pd}$(a cycle), V1 will have a negative leap, this procedure goes round and round, then oscillations are generated. It is simple to get that the oscillating period is $10t_{pd}$. To sum up, the frequency of ring oscillator is determined by the length of the delay stages, which is

$$f_0 = (\frac{1}{2Nt_D}) \tag{2.7}$$

where N is the number of cells and t_D is the delay time of each delay cell.

Ring oscillator is used in a very small area, but it is convenient for integration and design. The significant disadvantage is the high power consumption and phase noise [20, 21].

2.5 Optimization of VCO Performance

Focus on ring oscillations, the operating frequency of the VCO is simply defined as

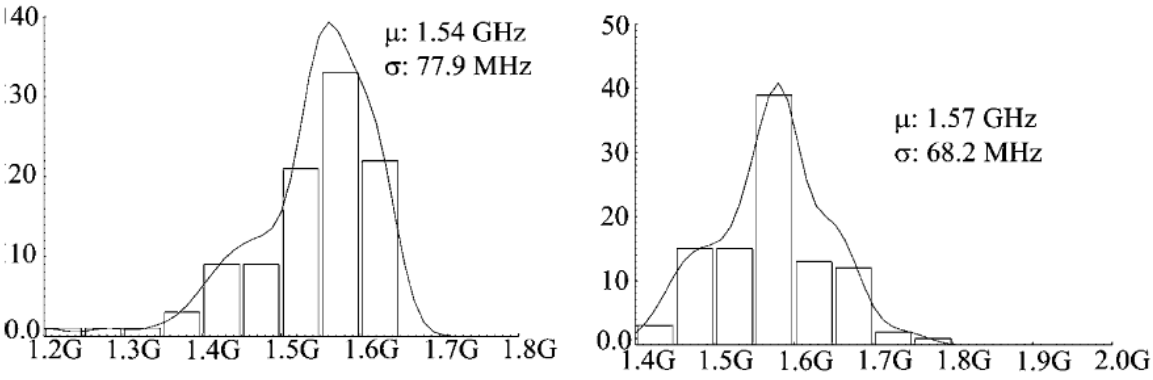
$$f_0 = (\frac{1}{N \times T}) = (\frac{I_D}{N \times C_{TOT} \times V_{DD}}) \quad (2.8)$$

where I_D is the current in the inverter, N must be an odd number that is the number of inverters, C_{TOT} is the total capacitance in the drain of inverter, and V_{DD} is supply voltage. It is clearly from (Formula 2.8) that the oscillation frequency depends on the value of current, the number of inverters and the specification of CMOS that in the inverters (C_{TOT} depends on the width and length of both NMOS and PMOS in the transistors).

Thus, the performance of VCO is determined by the specification of CMOS in a large part, such as the threshold voltage of NMOS (V_{Tnmos}) and that of PMOS (V_{Tpmos}), gate-oxide thickness of NMOS (T_{oxnmos}) and that of PMOS (T_{oxpmos}). In addition, V_{DD} is another important parameter that has a significant influence on frequency.

According to the research of D. Ghai, the effects on frequency are mainly observed for five cases: (a) only V_{DD} variation; (b) only V_{Tnmos} variation; (c) only V_{Tpmos} variation; (d) simultaneous T_{oxnmos} and T_{oxpmos} variation; and (e) simultaneous V_{DD}, V_{Tnmos}, V_{Tpmos}, T_{oxnmos} and T_{oxpmos} variation [22]. By using Gaussian distribution, f_0 in different situation is shown in Figure 2.7.

According to this conclusion, this project chooses threshold voltage and gata-oxide voltage as the main variables for experiments of process variation.



(a) Only V_{DD} (b) Only V_{Tnmos}

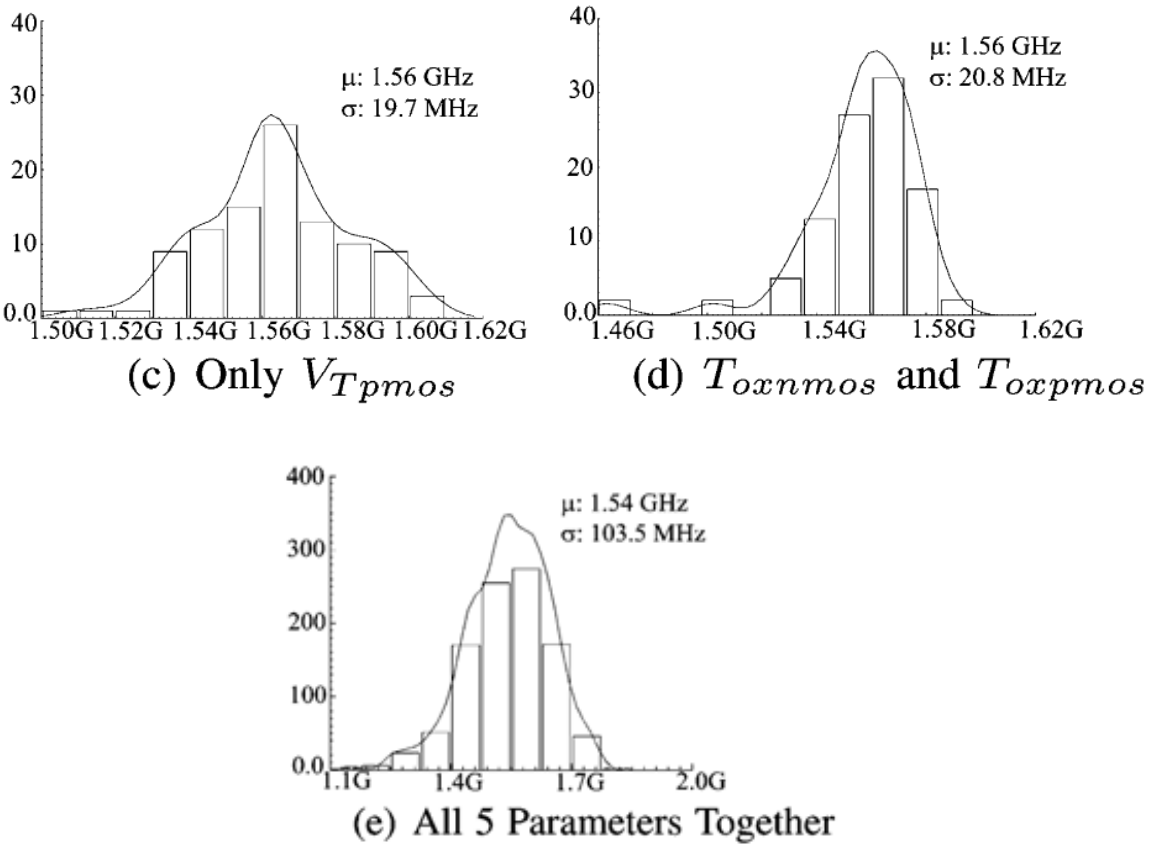


Figure 2.7[22]
Frequency with process variation of different parameters

Variation aware optimization is another important part of performance optimization of VCO. In actual circuit board, it will have some deviations between the actual value and theories value, the values of V_{DD}, V_{Tnmos}, V_{Tpmos}, T_{oxnmos} and T_{oxpmos} usually fluctuate by about ±10% [22], moreover, when some of them are decreased by 10% and the others are increased by 10%, the deviations will be magnified. Then the parameter of the circuit needs to match the design variables and reach the required oscillation frequency even in the worst case, it needs high flexibility of the design. In order to meet this requirement, the attributes of the VCO need to be set through the experimental data, especially the parameters of NMOS and CMOS, the change of width and length will cause different results. In this project, 10% variation is chosen for process variation experiments. The relative experimental data will be shown in the Chapter 4.

2.5 Tools Used

There are two kinds of software used in this project, which are Hspice and Matlab. Hspice is mainly used to run all the simulations and generate the text files of results that will be deal with by Matlab. Matlab is a tool for data processing, calculation and graph generating.

2.5.1 Hspice

From the description above, Hspice is a core tool to research the performance of CMOS circuits. Hspice usually can be run in Windows and UNIX operating systems, the basic working principle is that creating netlists first, simulating them, and then get waveforms that can reflect the quality of the circuit.

Hspice only takes in a netlist, which is similar as a text file, in the netlist, it contains the description, parameters, analysis options and so on information of the circuit. The suffix of the HSPICE netlist is .sp, such as lab1.sp. It will have lots of output files, such as lab1.ic0, lab1.mt0 etc, however, the one and only file need to be used is lab1.lis, which contains all the important results from the Hspice simulation, for example, operating points, measurement results, error message, etc. It is necessary to check and ensure that there is no error in the netlist after simulating this circuit.

The syntax of Netlist will be introduced below. Firstly, it should be noticed that the first line of a netlist is a comment, and Hspice will ignore it, so it is only used to make a short description. In addition, any texts following the asterisk are comments, too. Then some models need to be defined for the transistors or diodes (the components do not have only single value) that will be used in circuits. Each component has its own unique command, and then the topology of the circuits can be described, which is that give unique name to each node and connecting components between nodes.

After completing a description of a circuit topology, it can begin to enter analysis commands part. Some options may be defined to control the simulations. At the last line of netlist must be .end, Hspice will stop reading the netlist here.

2.5.2 Matlab

Matlab (Matrix Laboratory) is another software that will be used in this project, Matlab is mainly used to analyse data that generated by Hspice. The program file of Matlab is end up with .m extension, such as lab1.m, which contains a series of statements. In addition, Matlab can execute simple instructions that input in command window. The type of .m file is normal text file, which can be edited by Word and Notepad.

Command file can be divided into two parts, program and explanatory note. Matlab has custom function, which can execute mathematical functions, these functions can be called and return the result as an output. Not only executing mathematic arithmetic, Matlab can also implement simulations.

In this project, Matlab will be combined with Hspice, and the Hspice toolbox bridges the gap between these two kinds of software. The detail will be explained by examples.

2.5.3 Hspice and Matlab Interworking

Hspice only have a text interface, it is not visualized to plot some kinds of charts, then some data need to be simulated in Hspice and view and analyze in Matlab, the interworking of Hspice and Matlab is necessary. There is a toolbox in Hspice to implement this function, which is used to collect the routines of Matlab then the simulations in Hspice can be generated as signals chart in Matlab.

Simply add the file of Hspice Toolbox into the path of Matlab, and the command in Hspice can be used in Matlab.

2.6 Summary

This chapter has reviewed the basic concept of process variation, and common research approach for testing process variation – Monte Carlo Simulation, and Gaussian distribution. Using Gaussian function to imitate the distribution of threshold of NMOS & PMOS with process variation, and using Monte Carlo simulation to generate random numbers following Gaussian distribution for several thousand times to analyze the attribute of variables.

The object circuits of this project are VCO systems, LC VCO and Ring VCO are two kinds of common VCOs, and ring VCO is chosen to research.

Hspice and Matlab are two kinds of software that used in this project, Hspice is used to do simulation experiments and generate data text files, and Matlab is used to analyze this data and generate graphs after calculation.
The next chapter describes the major work in terms of designs of this project, including details of aim of each experiment, the process of each experiment, and some key points during the experiments.

Chapter 3: Project Design

3.1 Introduction

The aim of this project is to research the performance of VCO circuits in Nano-CMOS technology, especially the ability of process variation tolerance. The main theory to be used in this project is Monte Carlo simulation and Gaussian distribution, which was introduced in Chapter 2. This project is based on experiments, so two kinds of software, namely Hspice and Matlab, are used for simulation and calculation.

At the beginning of this project, it need to write the code to describe different kinds of VCO circuits, and make sure each VCO can work normally. Then select different technologies of Nano-CMOS libraries and simulate each design of VCO circuit to compare the influences caused by scale of Nano-CMOS. The next step is adding process variation in the simulation, and then gets the variable frequency distribution of each design, compare with each other to get a design which has robust process variation tolerance ability.

In this chapter, the detailed process of this project will be introduced, and some examples will be used to describe this procedure.

3.2 Project Design

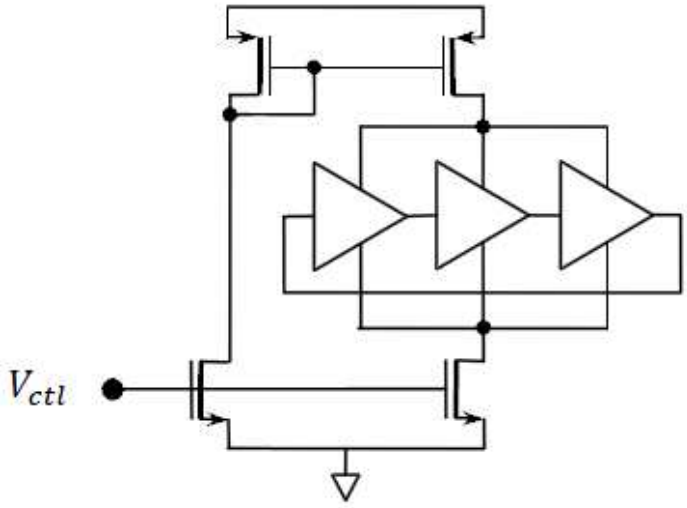
This project planned to start by debug the code of each VCO design until get the correct waveform of the output of each design in each technology. Then, the tendencies of frequency and power consumption, which are influenced by the variable of supply voltage and scale of Nano-CMOS, will get through experiments. During this step, it is possible to have some failed cases; it will be discussed in Chapter 4.

The next part is about process variation tolerance, it is the main objective of this project. Through experiments to get different the distribution of frequency with process variation, and then show on the results intuitively through bar chart. Adjust the frequency of each design to make each one has the same default frequency in the same voltage supply, then the comparison among each design can distinguish the process variation tolerance ability directly. All the analysis will be described in detail in the next chapter.

3.3 VCO Designs

In order to measure the ability of process variation tolerance, four kinds of VCO circuits are used to research.

3.3.1 Single-ended Ring Oscillator



Single-ended ring oscillator
Figure 3.1

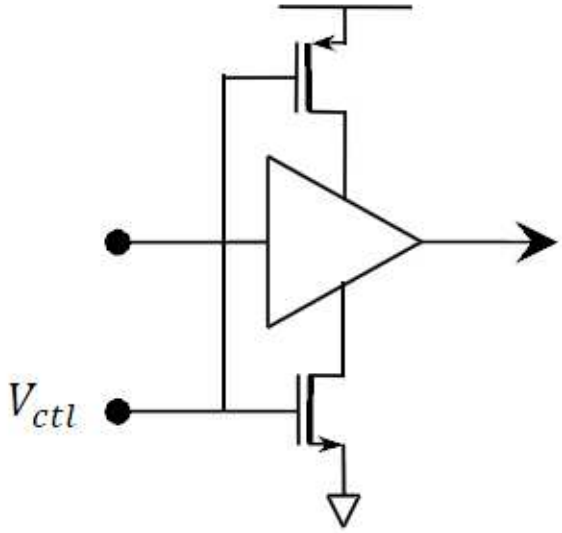


Figure 3.2
Current-starved inverter cell

The first design is a single-ended ring oscillator; the circuit is in Figure 3.1. There are three delay cells in this circuit; the delay time is determined by the parasitic capacitances and resistances at the output node. Figure 3.2 shows the throttle part of this design, which called current-starved inverter, change the control voltage (V_{ctl}) can control the switching time of the inverter. Single-ended ring oscillator is a circuit that has simple structure and easy to control.

3.3.2 Double-ended Differential Ring Oscillator

The other three kinds of circuits all belong to double-ended differential ring oscillator; the difference is that different designs use different delay cells. Generally, double-ended differential ring oscillators use the differential amplifier as the delay cell, the primary circuit shows in Figure 3.3. There are four delay cells in this design. According to the starting condition for oscillation as described in Chapter 2, the gain of the amplifier need to greater than 1. For the phase change, due to the differential delay cell, the phase will be changed through every delay cell, so it can oscillate whatever the delay cell is odd number or even number. However, even number of delay cells is benefit to generate a clock and inverter clock, or quadrature signals [23].

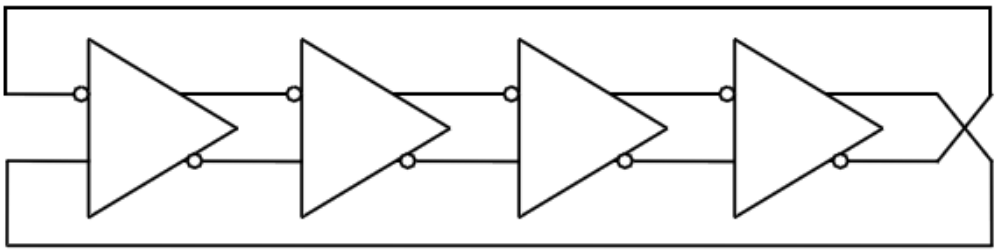


Figure 3.3
Double-ended differential ring oscillator

Compare with the single-ended ring oscillator, double-ended differential oscillator have some advantages. Because of the structure of differential amplifier, common-mode amplifier makes the voltage variation less sensitive, which will increase the stability of the circuit; it also can decrease attenuation of even harmonics dramatically. In addition, using different delay cells also have dissimilar influences to the circuits. In this project, three kinds of delay cells are used in double-ended differential ring oscillator.

Triode Load

The first design uses triode load as delay cell (Figure 3.4). In this design, voltage-controlled resistors are used and load resistance depends on bias voltage.

Symmetric Load

The second design is symmetric load delay cell (Figure 3.5). Symmetric load is using a voltage-controlled current source loads back to back with a voltage-controlled resistive load symmetrically.

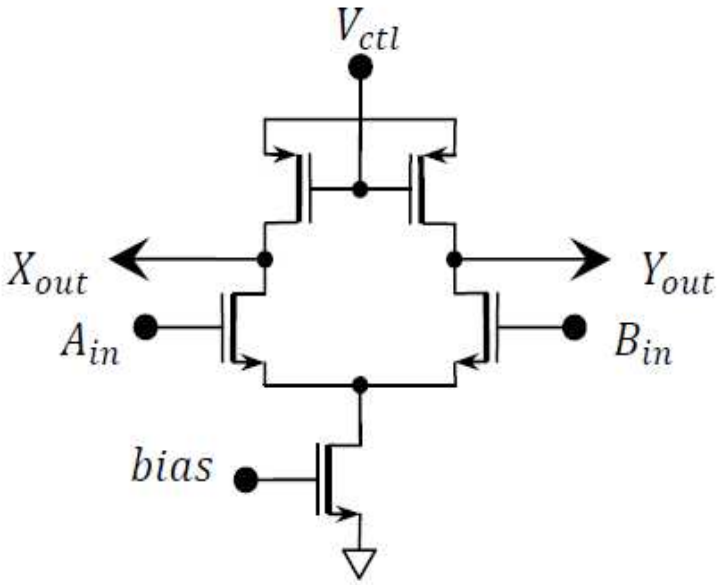


Figure 3.4
Triode load

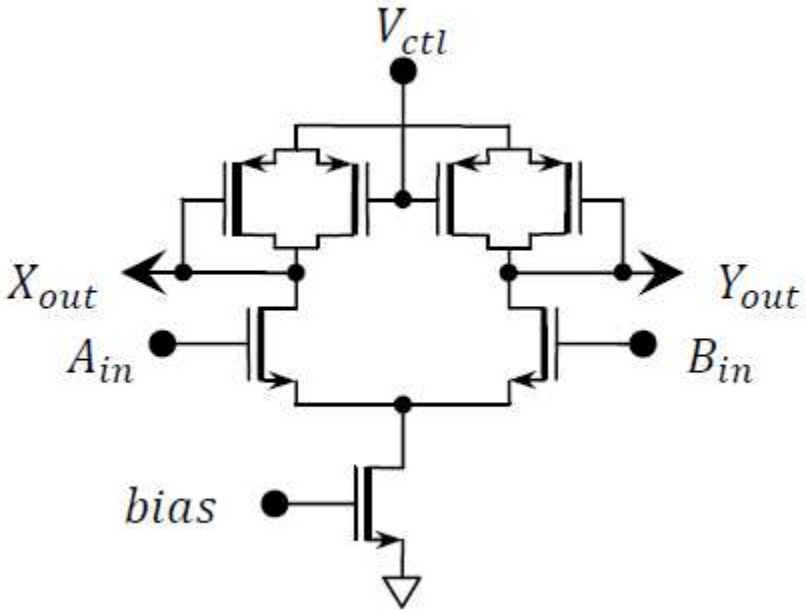


Figure 3.5
Symmetric load

Combined Cross-Coupled Differential Delay Cell with Symmetric Loads

The delay cell of third design is combined cross-coupled differential delay cell with symmetric loads, which is the most complex one (Figure 3.6). This configuration makes use of cross-coupled differential load to combine positive and negative resistances together, and then form a resistance that approach infinity. It can suppress the fluctuation in the circuit observably.

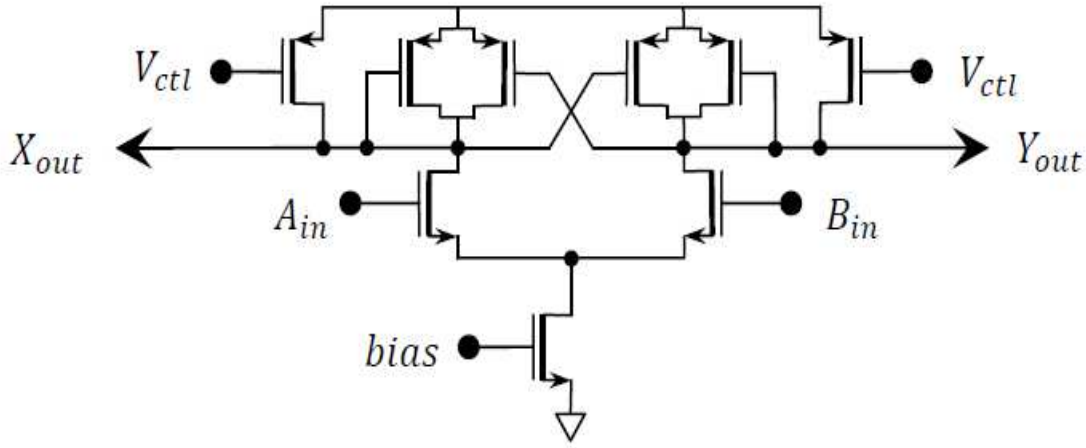


Figure 3.6
Cross-coupled differential delay cell with symmetric loads

3.4 Experiments Flow

As introduced above, the experiments of this project can be divided into two main parts:

1. Obtain the tendencies of power and frequency with different variables or technologies.
2. Use Monte Carlo simulation to test the frequency variation with process variation. By comparison, get a best design that has robust process variation tolerance.

For the first part, the supply voltage range will be tested first, make the supply voltage vary from 0.2V to 2.0V with step of 0.1V, and observe the waveform if VCO can oscillate in each voltage, thereby getting the working voltage of each design. Then measure the frequency tendency varies with the voltage, it needs to use Matlab to synthesize all these data and generate graphs to observe directly. Select different technologies (35n, 45n, 65n, 90n and 130n) of Nano-CMOS to measure the frequency tendency variation with the scale of Nano-CMOS. Repeat this step to measure the power tendency as well.

The aim of the first part is that realize the basic attributes of all the VCO designs, including their starting conditions for oscillation, influences of voltages and scales of transistors on frequency and power of VCO. Moreover, the stability of each VCO can also get a preliminary understanding from this part.

The second part is the experiments about process variation. As described above, process variation experiments need to use Monte Carlo simulation and Gaussian distribution to implement, Figure 3.7 shows the flow chart of this experiment.

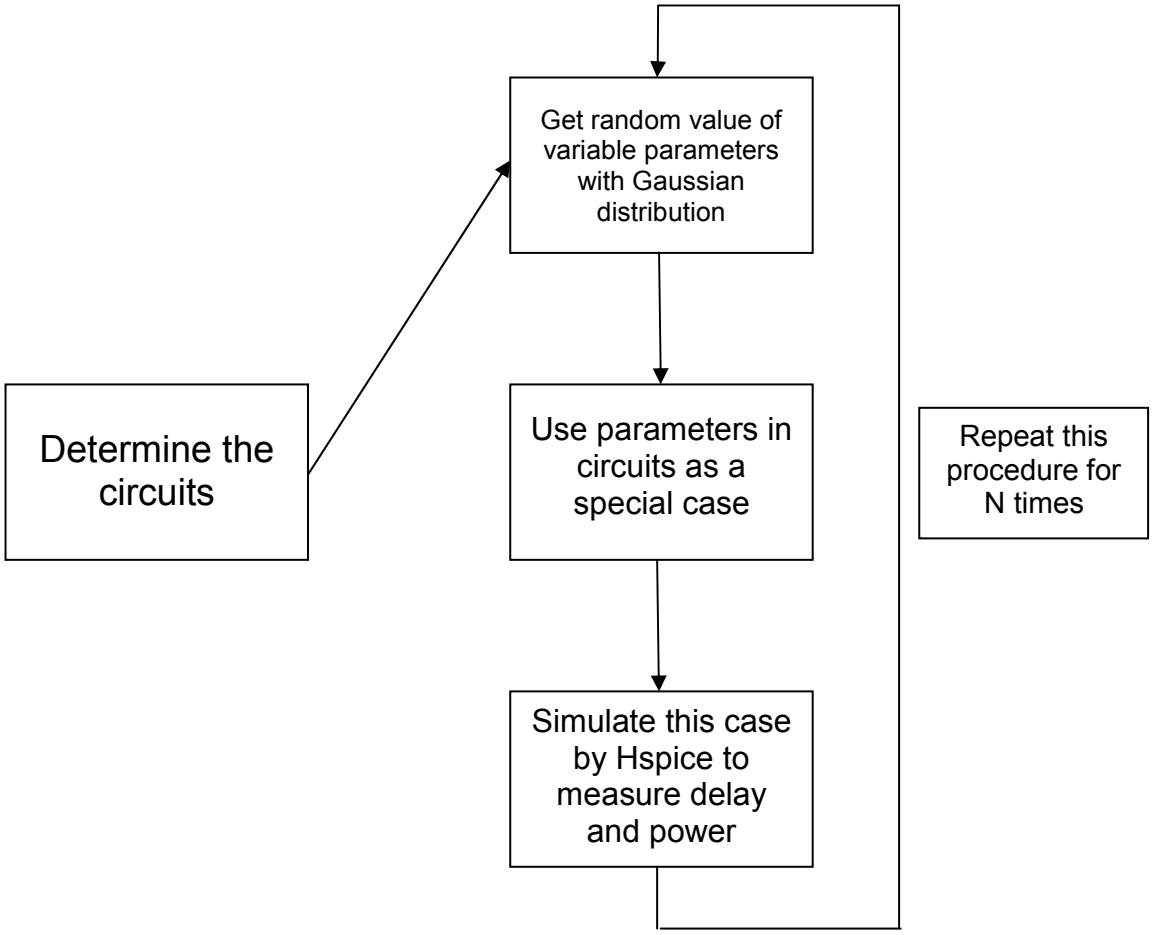


Figure 3.7
Flow Chart for Process Variation Simulation Experiment

As can be seen from this flow chart, firstly, determine which design will be used, then set the variation and distribution of the target parameters, which are about process variation in this experiment, for Monte Carlo simulation. During Monte Carlo simulation, random values of the parameters will be generated and used in the circuits as a special case. After that, this case will be simulated to measure some attributes of the circuits. Get another random value to repeat this procedure for N times, and then the distribution with process variation can be obtained by using Matlab. For the convenience of comparison of process variation tolerance ability, all the frequencies of designs need to be adjusted into the same value with theory parameters. The detailed work of software will be given later.

3.5 Software Simulation

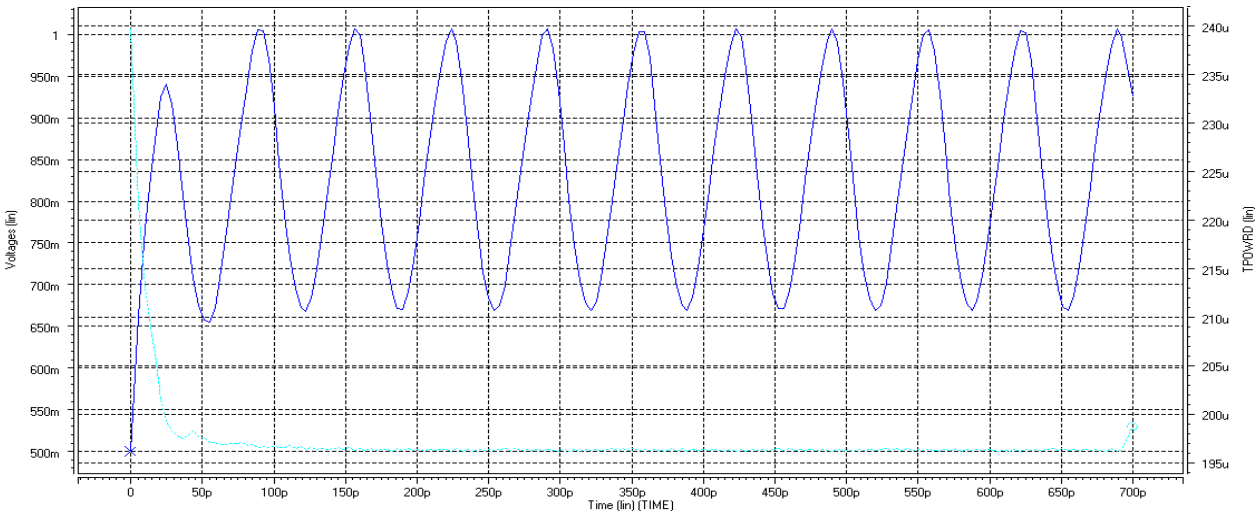
Software simulation only needs to use Hspice, process can be divided into three steps. Firstly, write the code of each design, add the test methods and environments, and set the variables that need to measure. Secondly, run this simulation; make sure there is no error during simulations. Finally, observe the

waveform through “Avanwaves” or “Cscope” (two functions of Hspice used to observe the waveforms), check the correctness of generated files, both of them need to call .tr0 file. Figure 3.8 shows simply graphs that generated by Avanwaves and Cscope. In Figure 3.8(a), dark blue is voltage waveform, and light blue is power waveform, it can be seen that Avanwaves combine and show all the waveforms together. Different from Avanwaves, Cscope shows each graph individually (Figure 3.8(b)), which is clearer but needs more time to initialize the programme.

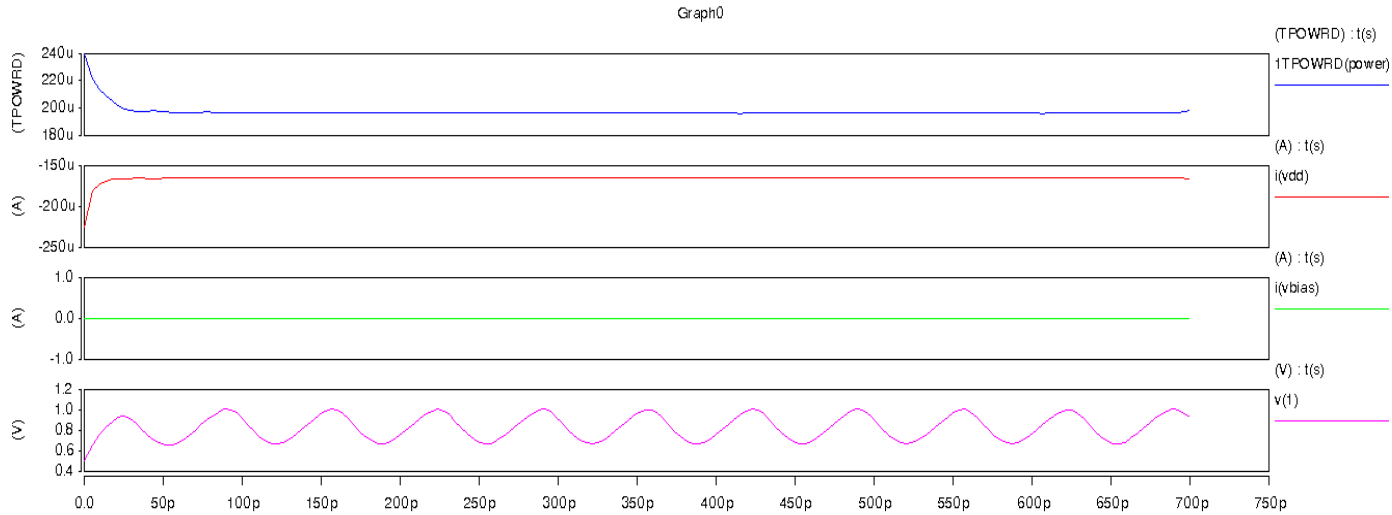
For simulation, .sp file needs to be written first. The code in this file can be divided into 4 parts. The first part is that define the attributes of the simulations, such as initial conditions, variables, simulation mode etc. The second part is circuit description, which is used to simulate a circuit by code. The next part is the information about measurement, including measured parameters and measure methods. The final part is the library of the Nano-CMOS, when add process variation, some parameters in this library can be replaced by a distribution.

After simulation, it has some generated files, which record all the data during the simulation, that can be used to calculate or statistics. To the experiments in this project, the format of generated files is .mt0, which records data such as supply power, temperature, random values of the parameters (only for process variation experiments), measured parameters etc. This file can be opened by Matlab.

In Matlab, .mt0 file can be divided into several parts by different parameters, each parameter forms an array. Then Matlab can generate graphs for arrays. It also can combine different arrays into the same graph that make the comparison more intuitive.



(a) Waveform from Avanwaves



(b) Waveform from Cscope

Figure 3.8

Waveforms generator

3.6 Example

In this section, a simple example will be given to explain this simulation. Here is a piece of code about single-ended ring oscillator with process variation (The content of the library is omitted, which is too long to give here. The relevant information can be found in appendix A):

```
1.  *signal-ended 45n
2.  .option nopage nomod post
3.  *initial condition
4.  .ic v(3)=0
5.  .param l=45n
6.  .param nvt= agauss(0.466v,0.0466v,3)
7.  .param pvt= agauss(-0.4118v,0.04118v,3)
8.  .tran 20p 0.8n sweep monte=5
9.  *voltage sources
10. v1 vcc   0 1.2
11. v2 vcc2 0 0.6

12. *Components
13. m1 vcc    1    1  vcc pmos l='l' w='4*l'
14. m2 vcc    1    2  vcc pmos l='l' w='4*l'
15. m3  1    vcc2 0    0  nmos l='l' w='4*l'
16. m4  6    vcc2 0    0  nmos l='l' w='4*l'
17. Xinv1 3 4 2 6 inv
18. Xinv2 4 5 2 6 inv
19. Xinv3 5 3 2 6 inv
20. .subckt inv in out vdd gnd
21. m5 vdd in out  vcc pmos l='l' w='4*l'
22. m6 out  in gnd   0  nmos l='l' w='4*l'
23. .ends inv
```

```
24. *measure
25. .meas m_power rms power
26. .meas tran maxval MAX v(3) from=0.5ns to=0.8n
27. .meas tran minval  MIN  v(3) from=0.5ns to=0.8n
28. .meas tran tdelay trig v(3) val='(maxval + minval)*0.5' fall=5
29. +targ v(3) val='(maxval + minval)*0.5' fall=6

30. *library
31. *…
32. .end
```

Any words after ”*” will be ignored as comments. The first line is the title of this experiment, any information can be written in this line. Second line define the optional information, for this one means choosing suppresses page ejects for title headings (nopage) and suppresses printout of model parameters (nomod). Line 4 defines the initial condition, it is used to create a jitter to start the oscillation, and Line 5 set the scale of Nano-CMOS is 45 nanometers. From Line 6 to Line 8 is used for process variation, threshold voltages of nmos and pmos are set as Gaussian distribution with 10% variation and 3 σ deviation, and use transient analysis with 20 picoseconds timestep and 0.8 nanoseconds intervals. Then “sweep” indicates that this simulation has a different variation type, such as DEC, OCT, DATA etc, this one is using Monte Carlo simulation for 5 times. Line 9 to 11 is supply voltage and control voltage. From Line 12 to Line 23 is the description of circuits (the schematic see Figure 3.9). No. 24 to No. 29 lines are the measurements definition, it uses RMS (root mean squared) to calculate the power consumption, and find the maximum and minimum value of the voltage in Node 3, and the time delay between the fifth fall edge and the sixth edge to calculate the cycle of oscillation (Hspice cannot measure frequency directly, so cycle needs to be measured first and uses Matlab to calculate frequency). At the end of the code is the library of 45n technology. Moreover, for the experiments about tendency, code about Monte Carlo simulation and Gaussian distribution need to be removed.

Run this simulation, the waveforms of some parameters can be get as Figure 3.10. Because of process variation, the tracks of the oscillation begin to shift obviously relative to each other, and the cycle and frequency will change with it (Figure 3.10(a)). Power consumption is also changed with process variation (Figure 3.10(b)); furthermore, the phase of oscillation is another factor that affects power consumption.

In addition, six different files are generated by simulation, and two of them are worth to focus on, which are .lis file and .mt0 file. In the .lis file, it shows all the warnings and errors that happen during the simulation, it is convenient to correct errors according to the information in this file. .mt0 file record all the experiments data, which can be used in Matlab.

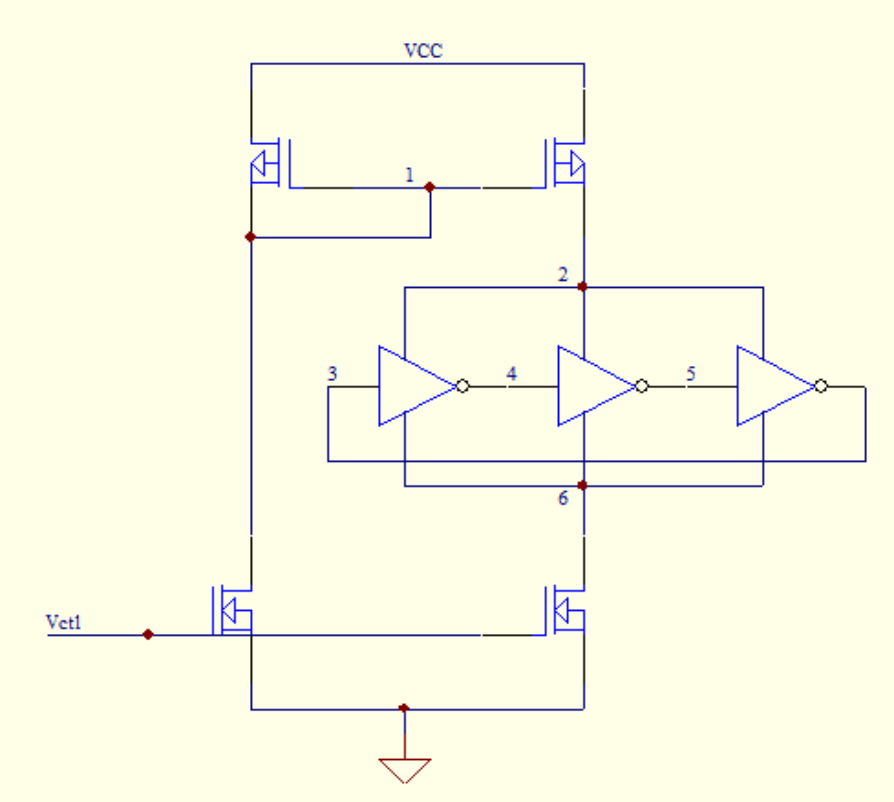
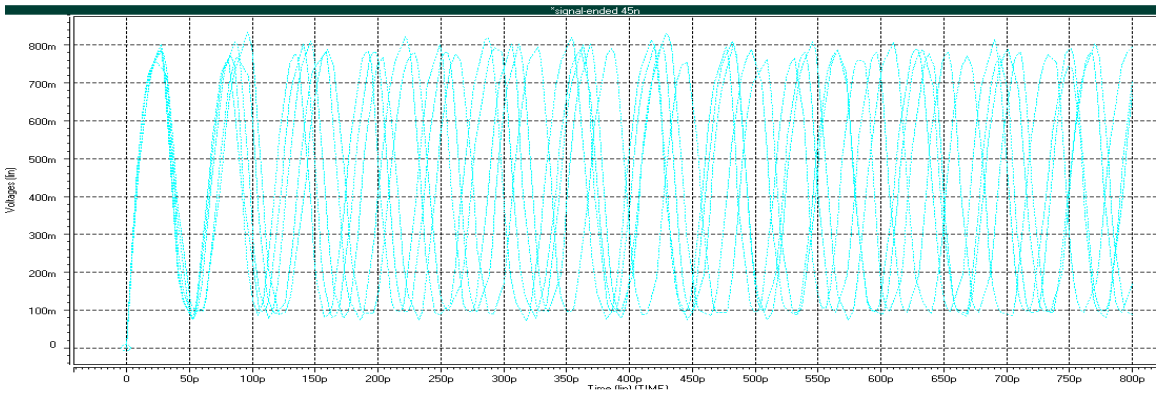
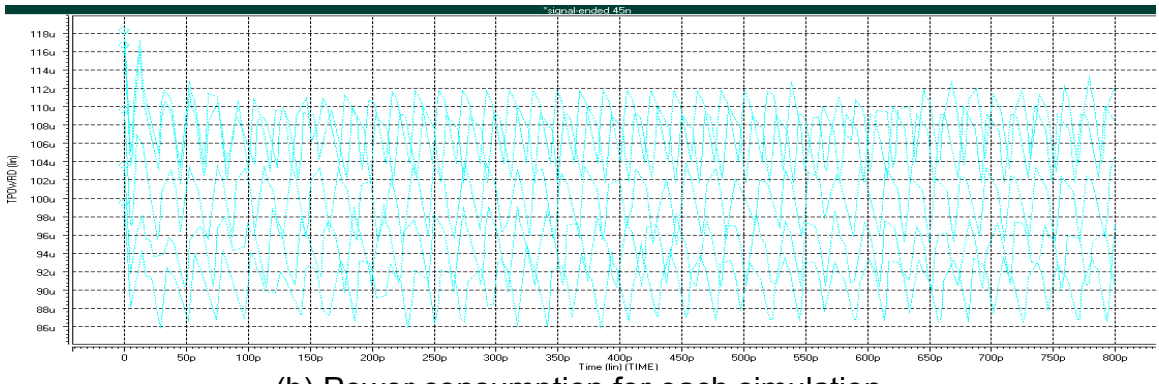


Figure 3.9
Schematic with nodes names of single-ended ring oscillator



(a) Voltage in Node 3 for each simulation



(b) Power consumption for each simulation

Figure 3.10
Simulation waveforms

```
$DATA1 SOURCE='HSPICE' VERSION='Y-2006.03-SP1 MT'
.TITLE '*signal-ended 45n'
 index              nmos@nvt          pmos@pvt          m_power
                    maxval            minval            tdelay
                    temper            alter#
    1.0000             0.4731           -0.4263           9.473e-05
                       0.8082           7.436e-02         6.638e-11
                      25.0000             1.0000
    2.0000             0.4638           -0.4097           1.002e-04
                       0.8144           9.341e-02         6.186e-11
                      25.0000             1.0000
    3.0000             0.4496           -0.4010           1.068e-04
                       0.7810           9.484e-02         5.709e-11
                      25.0000             1.0000
    4.0000             0.4471           -0.3965           1.084e-04
                       0.7777           8.067e-02         5.691e-11
                      25.0000             1.0000
    5.0000             0.4831           -0.4263           9.071e-05
                       0.8021           8.624e-02         6.672e-11
                      25.0000             1.0000
```

Figure 3.11
A section of data in .mt0 file

Matlab is used to deal with the data that saved in .mt0 file. Figure 3.11 shows a piece of data in .mt0. The first two lines are instructions. Line 3~5 shows the names of each parameters, and all the simulation results list below. Here is a piece of code for Matlab, which is used to deal with the data in .mt0 file, including the functions of reading data, processing data and generating graphs:

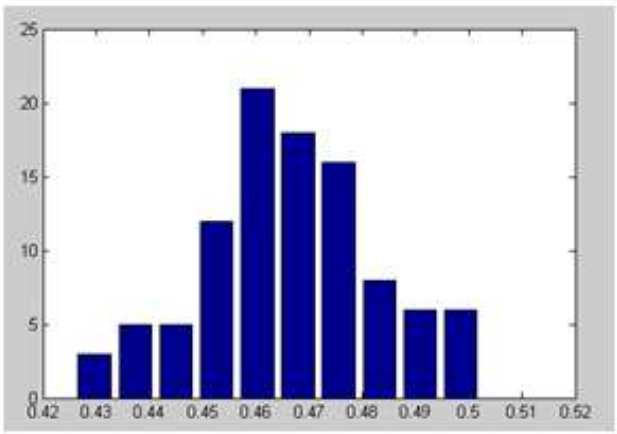
```
1. clear all;
2. clc;
3. fid = fopen('single-ended.mt0','r');
4. line = fgetl(fid);
5. line = fgetl(fid);
6. line = fgetl(fid);
7. line = fgetl(fid);
8. line = fgetl(fid);
9. format('short','e');
10. d = fscanf(fid, '%e %e %e %e %e %e %e %e %e', [9 inf]);
11. T=d';
12. fclose(fid);
13. nvt=T(:,2);
14. pvt=T(:,3);
15. pow=T(:,4);
16. delay=T(:,7);

17. figure(1)
18. bins=linspace(min(nvt), max(nvt), 10);
19. C=hist(nvt,bins);
20. bar(bins,C);
21. figure(2)
22. bins=linspace(min(pvt), max(pvt), 10);
```

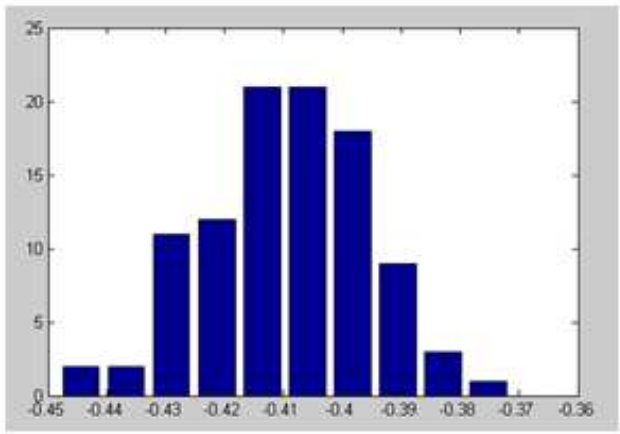
```
23. C=hist(pvt,bins);
24. bar(bins,C);
25. figure(3)
26. bins=linspace(min(pow), max(pow),10);
27. C=hist(pow,bins);
28. bar(bins,C)
29. figure(4)
30. freq=1./delay;
31. bins=linspace(min(freq), max(freq), 10);
32. C=hist(freq,bins);
33. bar(bins,C)
```

The first three lines are used to clear all the variables that used before, and clear all the data and instructions in the screen, then open .mt0 file to ready to begin. The first 5 lines in .mt0 file is not data (see Figure 3.11), which need to be ignored (through Line 4~9). There are 9 parameters in all, and the useful parameters are in second, third, fourth and seventh columns, Line 10~16 are instructions that define 9 parameters and get the objective parameters by row. The rest instructions are used to generate graphs. Using the maximum and minimum values of each parameter as a range, and divide into 10 sections, gets the statistical numbers of the values in every section, and the graph can be generated to reflect the distribution of each line. It should be noticed that Line 30, which is used to calculate the frequency from delay, the dot after 1 cannot be removed or the results will be only integers.

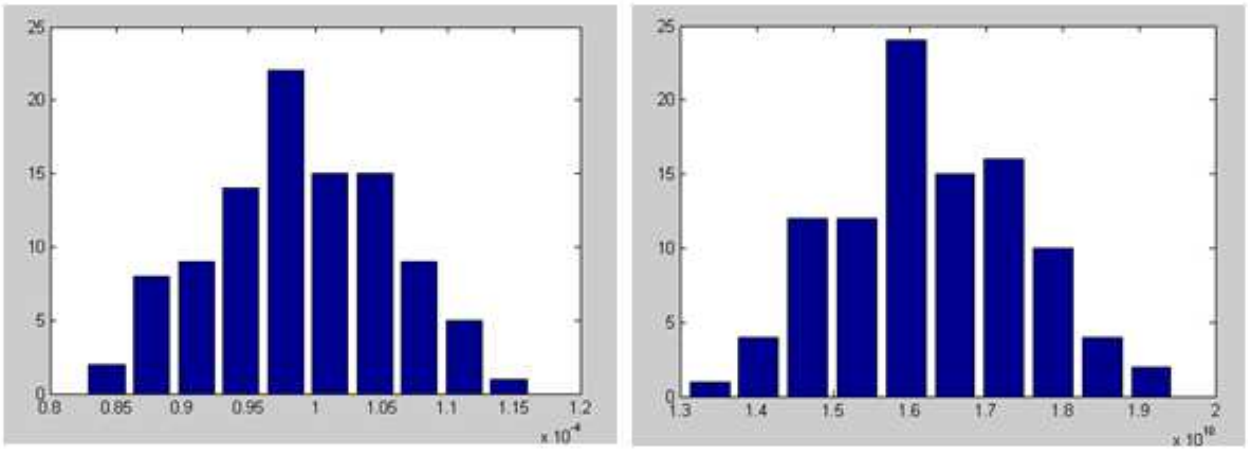
For process variation, 5 times is not enough to show the distributions, so the results of 100 times simulation are showed here in Figure 3.12. As can be seen in the graphs, the threshold voltage has changed by Gaussian distribution, and power consumption and frequency also change with distribution of threshold voltage. According to this experiment, a primary conclusion can be got that the process variation tolerance of single-ended is not quite strong, however, it is not an intuitive way to get a conclusion, and a better way is through comparison. Every graph must have a unique name or the previous graph will be replaced by the latter one.



(a) nvt distribution



(b) pvt distribution



(c) Power distribution (d) Frequency distribution

Figure 3.12
Distributions of each parameter

3.7 Summary

This chapter described the process of this project, including the preparatory work of each experiment, the implementation of the simulation, and the procedures of data processing.

In general, there are two parts of experiments; one is researching some attribute of VCO circuits; the other is used to measure the process variation tolerance ability. All the simulations are completed through Hspice, Monte Carlo simulation with Gaussian distribution can implement the simulation of process variation, and some instructions and syntax of the code are also introduced. Matlab is a tool for calculation and statistics, which are used to generate graphs that make people to get results intuitively.

All the technologies of Nano-CMOS (32n, 45n, 65n, 90n, 130n) are tested in each design to get an exact conclusion of the basic attributes and process variation tolerance of VCO. The next chapter will demonstrate the detailed experiments results and analysis of this project.

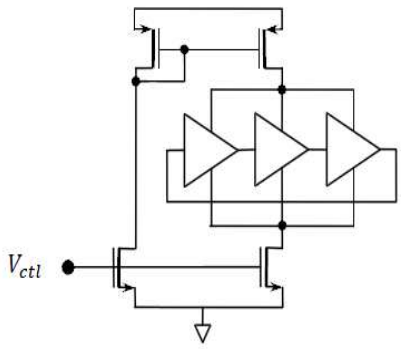
Chapter 4: Experimental Results

4.1 Introduction

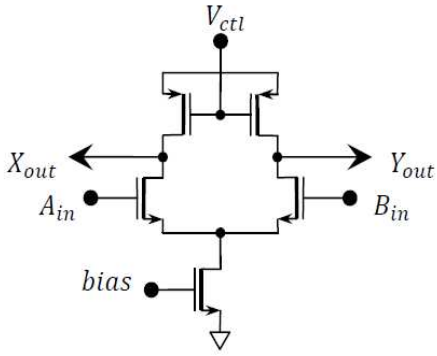
In Chapter 3, all the methods and process of experiments have been described, and in this Chapter, all the experimental data will be analyzed, and a conclusion will be given of each experiment.

As introduced before, all the experiments can be divided into two parts – basic attribute of VCO designs tests and a comparison of process variation tolerance ability.

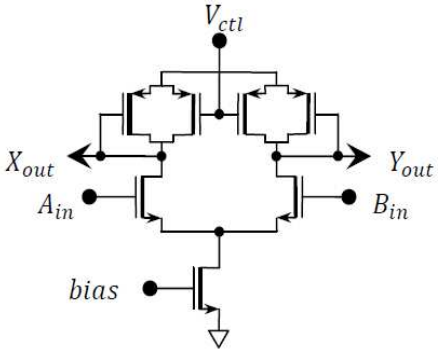
4.2 Frequency Tendency



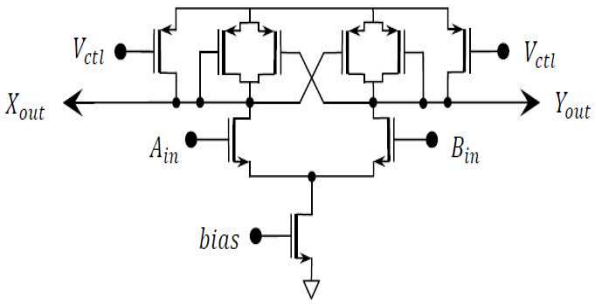
Design 1
Single-ended ring oscillator



Design 2
Triode load



Design 3
Symmetric load



Design 4
Combined cross-coupled differential delay cell with symmetric load

Figure 4.1
Define a short name for each design
(Design 2, 3 and 4 belong to double-ended ring oscillators.)

Firstly, all the schematics of VCO designs will be given. A schematic of single-

ended ring oscillator has shown in Figure 3.8, for convenience, this design will be called Design 1 below, and so are the other designs (see Figure 4.1). The complete circuits of double-ended differential ring oscillators are connected four delay cells (Figure 4.2). All the names of the nodes that will be used are the same in Design 2, 3, 4, so only the schematics of design 2 will be given (Figure 4.3).

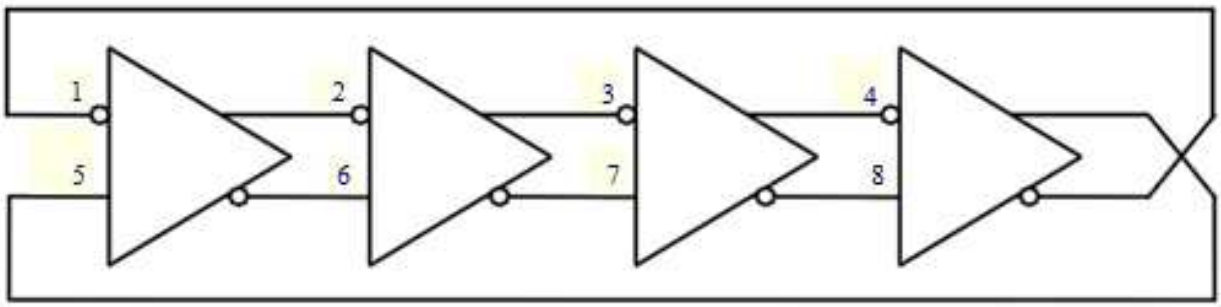


Figure 4.2
Schematic with nodes names of double-ended differential ring oscillators

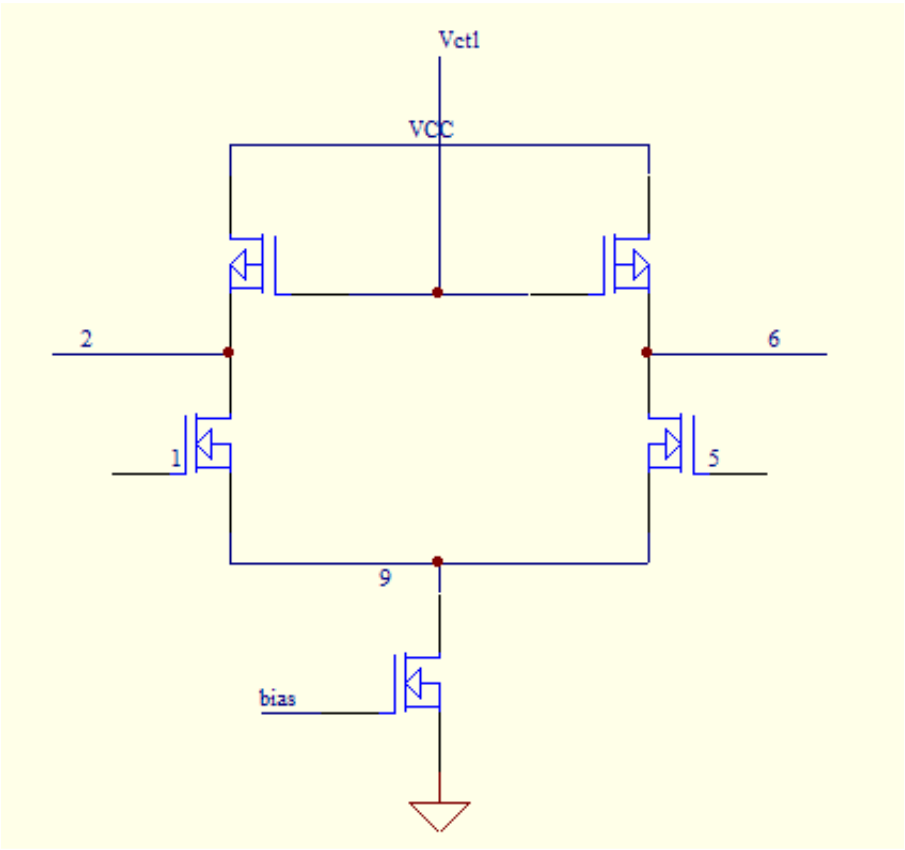
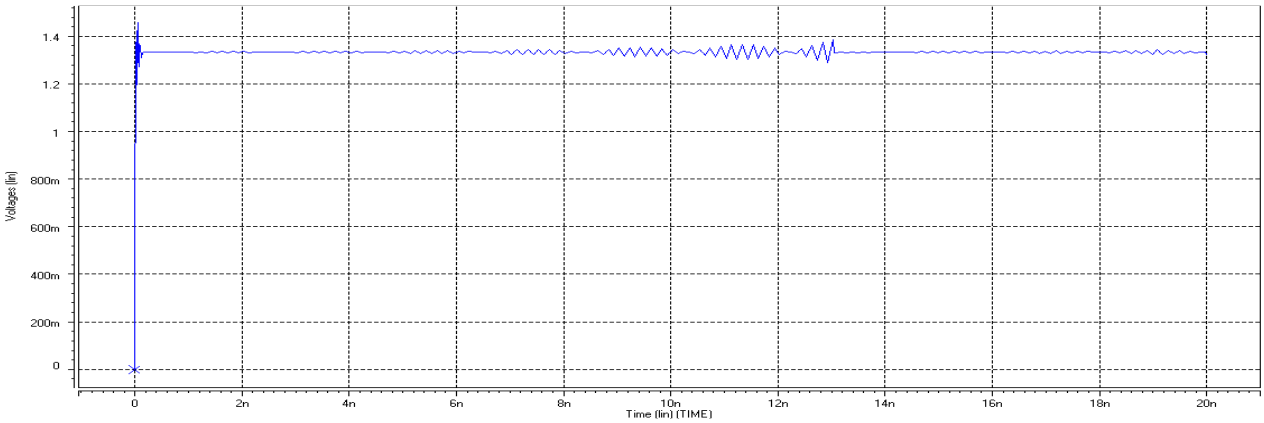


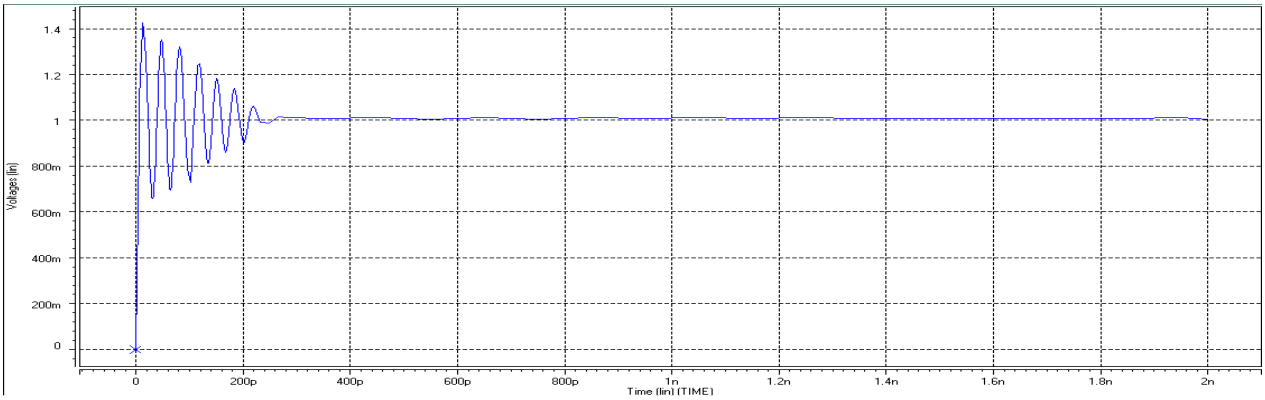
Figure 4.3
Schematic with node names of Design 2

The frequency tendency of each VCO is tested as the first step of this project. The experiments test the frequency that varies with the supply voltage. The voltage will be changed from 0.6 to 2V, and step with 0.1V, then observe the

oscillation voltage range of each design (actually, some designs can work below 0.6V, but the frequency is quite low, so set 0.6V as the minimum voltage).
During the simulations, if a voltage is not suit for oscillating, VCO cannot work or work steadily (Figure 4.4). All the results are shown in Table 4.1. When a design is unsuited to a certain technology, the oscillation voltage range will be quite narrow. Generally, there is no upper limit for oscillation; however, Design 3 has an upper limit, which is different from each other. Design 4 is also not quite suit for 32n technology. In general, Design 1, 2 and 4 all have a satisfactory voltage range for oscillation.



(a) Case 1



(b) Case 2

Figure 4.4
Two kinds of failure cases

Then the frequency tendency that changes with supply voltage will be tested. Use Design 1 as an example, Figure 4.5 shows the tendency of frequency in different technologies, each group represents the data of a technology, and in each group, the voltages are sample values between 0.6 and 2.0 (increasing order). As can be seen from the figure, the frequency of VCO is in proportion to supply voltage.

Table 4.1
Supply voltage range for oscillation

Voltage Scale / Range / Designs	32n	45n	65n	90n	130n
Design 1	0.6~2.0	0.6~2.0	0.6~2.0	0.6~2.0	0.6~2.0
Design 2	1.0~2.0	0.6~2.0	0.6~2.0	0.6~2.0	0.6~2.0
Design 3	1.2~1.3	0.6~1.5	0.6~1.6	0.6~1.7	0.6~1.7
Design 4	0.6~1.7	0.6~2.0	0.6~2.0	0.6~2.0	0.6~2.0

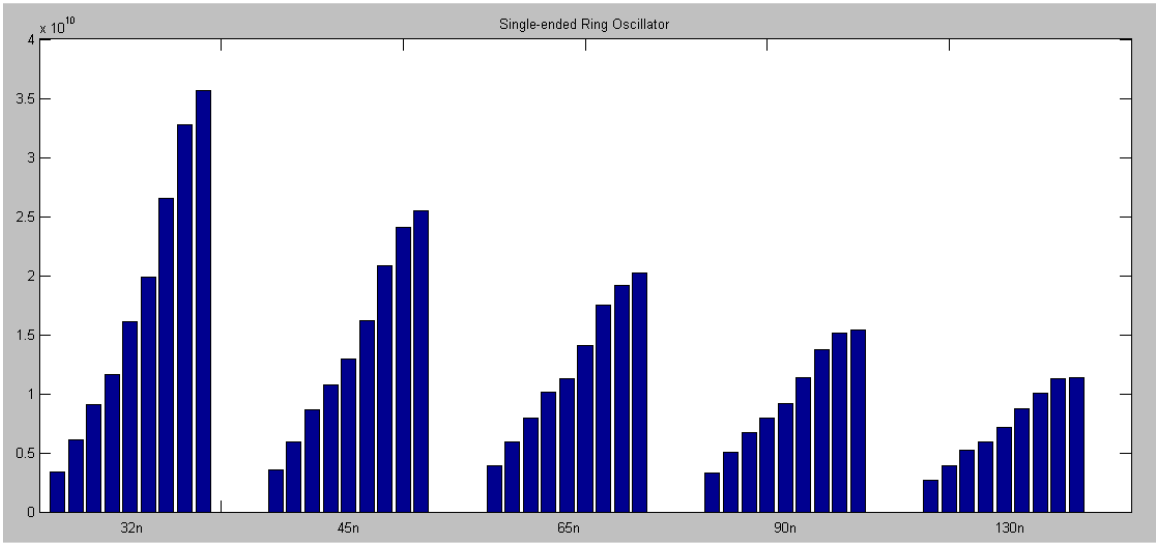


Figure 4.5
Frequency tendency of Design 1(group by scale)

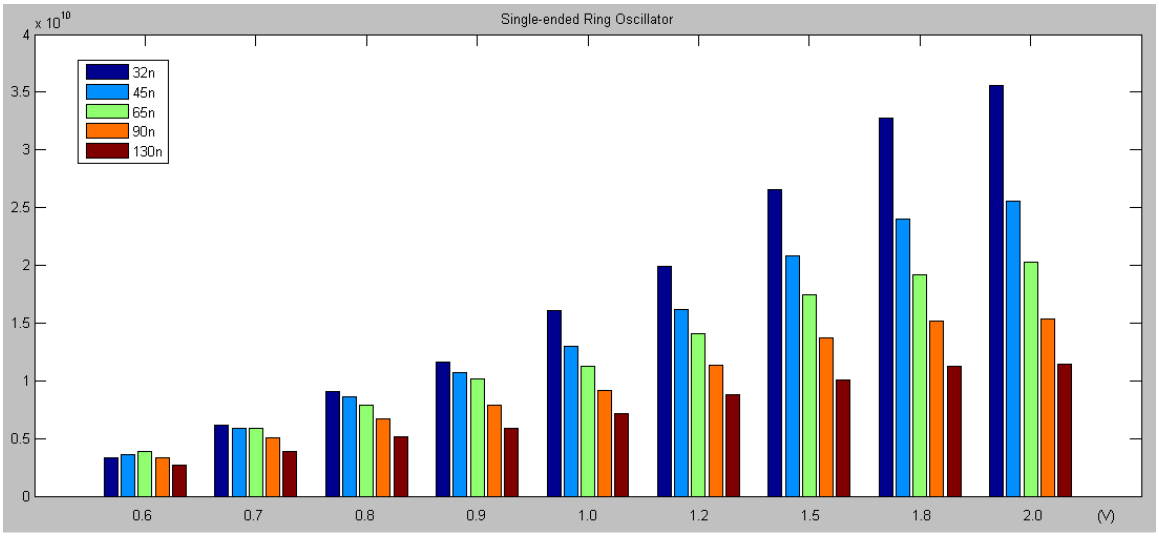


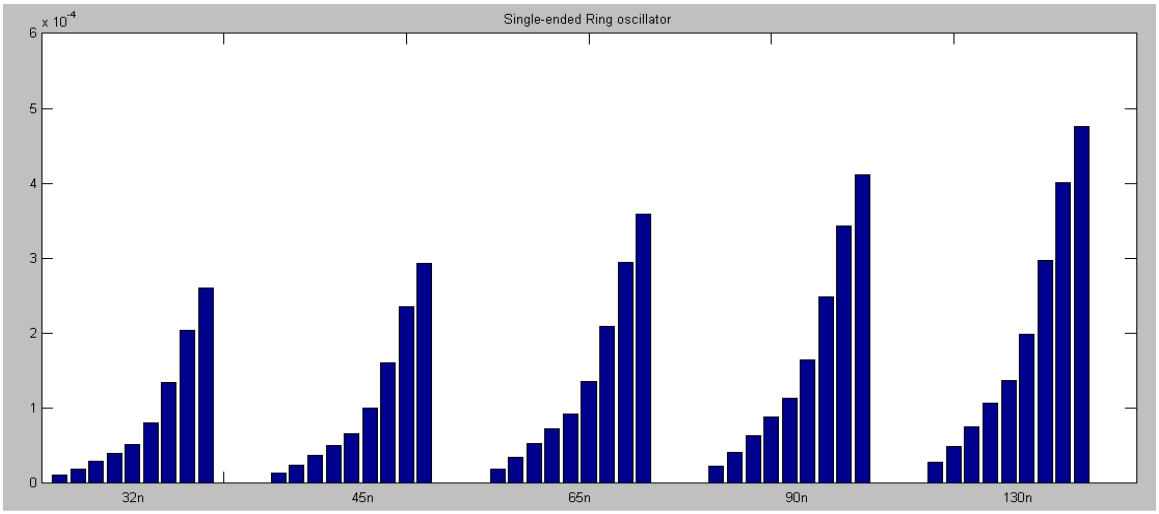
Figure 4.6
Frequency tendency of Design 1(group by supply voltage)

Change an angle to analyze these data again, see Figure 4.6. This figure divides data into 9 groups by supply voltage. Different colours represent different technologies. Because the oscillation is not stable when the voltage is low, so the sample values are dense below 1.0V. It can be seen clearly, frequency is in inverse proportion to the scale of Nano-CMOS. There is an

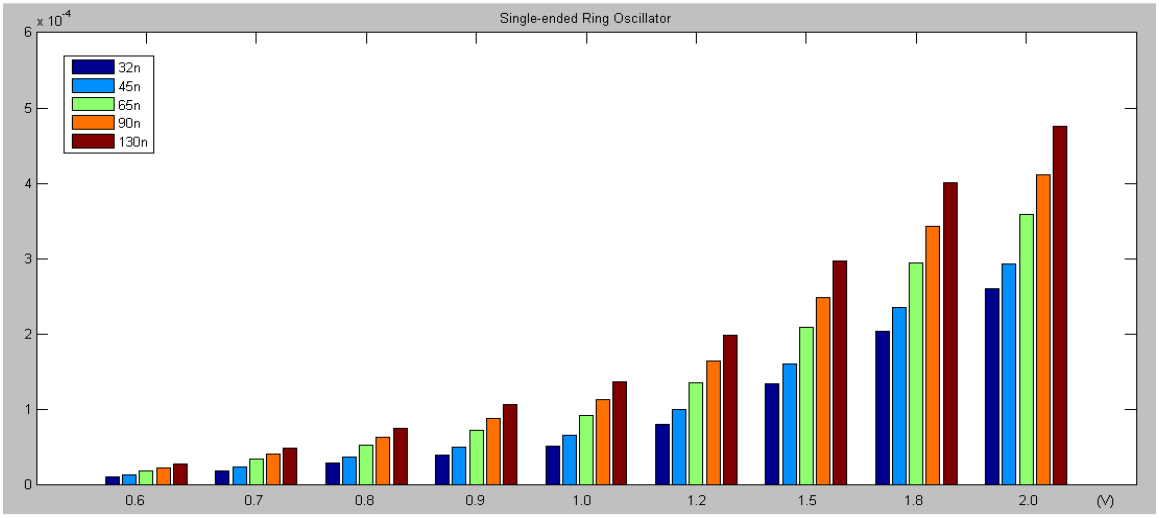
exception at voltage 0.6V group, the frequency tendency is not linear, it is because the oscillation is not stable at this voltage, the frequency is fluctuating during oscillation; therefore, the appropriate supply voltage is above 0.6V, above 0.8V is dependable for Design 1.

4.3 Power Consumption Tendency

Power consumption is also an important attribute not only for VCO, even for nearly all kinds of circuits. The variation of power consumption is well worth to test. Similar experiments with that of frequency tendency, the bar charts that show the tendencies will be given (Figure 4.7). It is not difficult to image that the power consumption is in proportion to supply voltage, higher frequency oscillation needs to take more energy. In addition, smaller scale components are another way to save energy, which is importance to get a Nano-CMOS design, which can be used for portable devices.



(a) Power consumption tendency of Design 1(group by scale)



(b) Power consumption tendency of Design 1(group by supply voltage)

Figure 4.7

Then the comparison among different designs with each technology will be given (Figure 4.8). Use 1.2V as supply voltage. From the figure, it can be seen that due to the complex structure, double-ended differential ring oscillator needs to consume more energy than single-ended ring oscillator, especially Design 4, which use 9 transistors in each delay cell. However, if the complex structure can increase the stability, it will be demonstrated in next section.

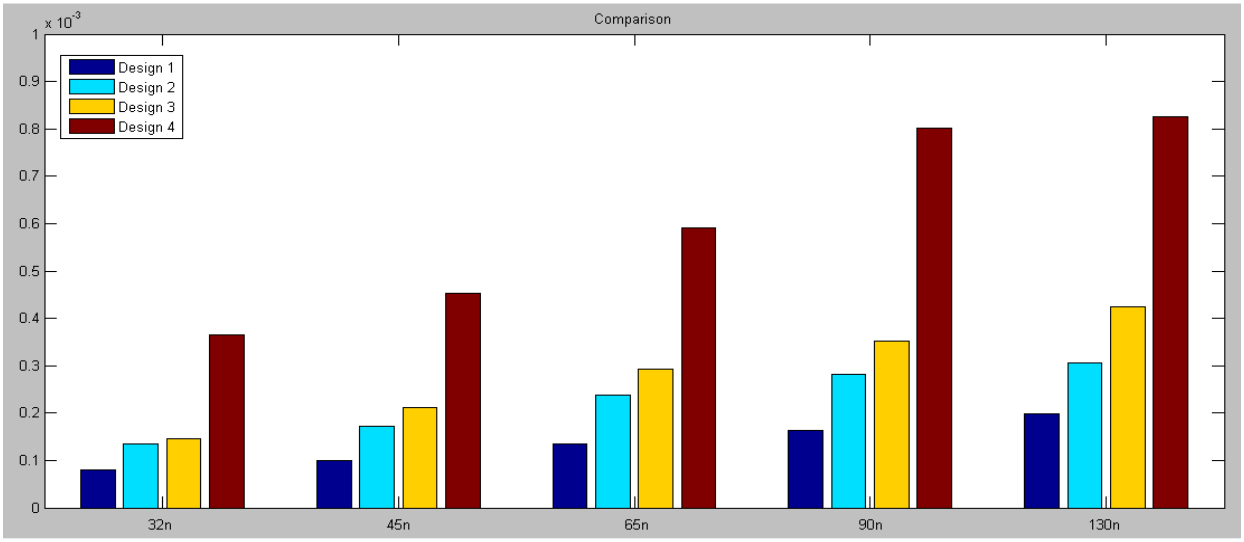


Figure 4.8
Power consumption comparison of each design

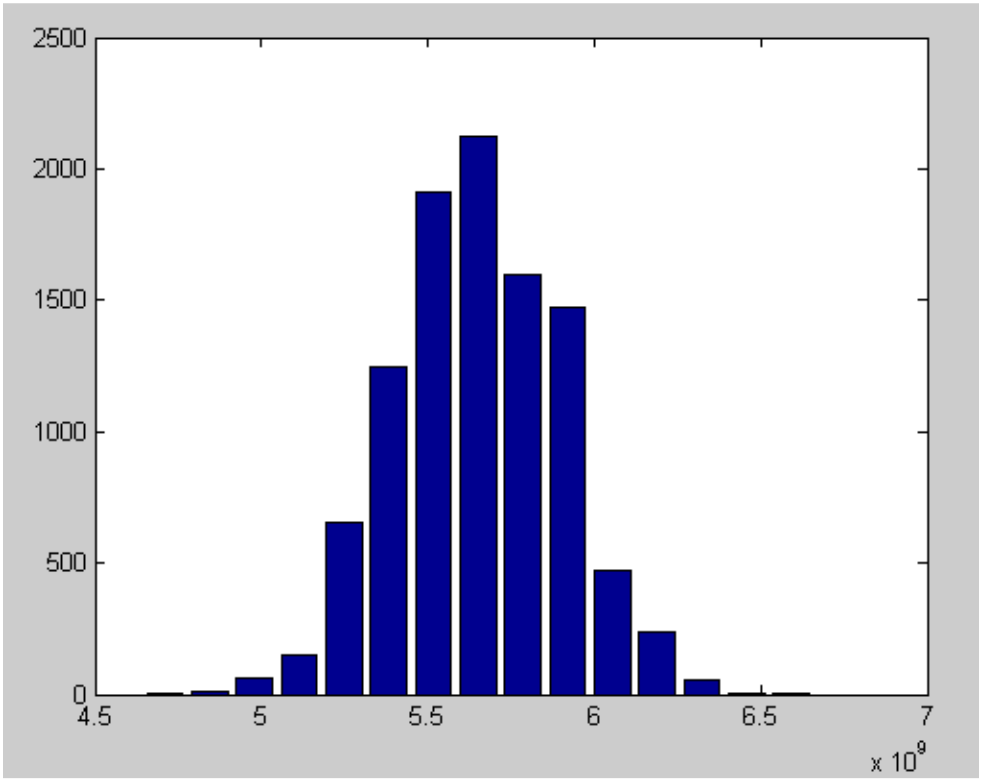
4.4 Frequency Distribution with Process Variation

According to the experiments above, if a design has a smaller volume, great energy conservation can be tested, however, another important factor of a VCO design is the stability of frequency. As introduced before, in Nano-CMOS, the phenomenon of process variation is quite significant that it is important to test the process variation tolerance ability to get a superior performance design.

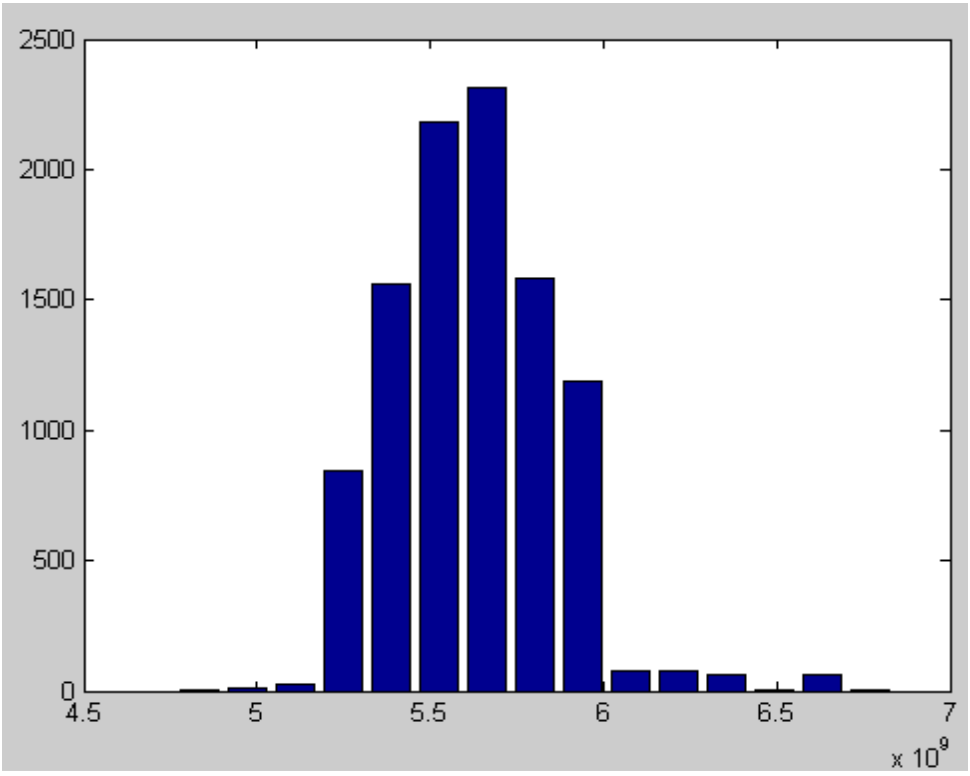
Process variation experiments need to vast amounts of experimental data. In this project, 10 thousand times are used to do the process variation simulation. As describe in Chapter 2, two critical parameters, which have significant affect on process variation, are threshold voltage and gate-oxide thickness.

Firstly, the simulation data with variation of threshold voltage will be given. Figure 4.9 shows the frequency distribution of each design in 130n technology. The distribution method of each design is that get the maximum and minimum value of each design as the range, and divide this range into 15 regions, then calculate the numbers of the case in each region to get the figures above. Before simulation, all the theoretical value of frequency should be adjusted to values close to each other, which is convenient for comparisons. In order to make the frequencies similar, add capacitors is an easy and effective way to implement. The capacitors are added in all the nodes between delay cells,

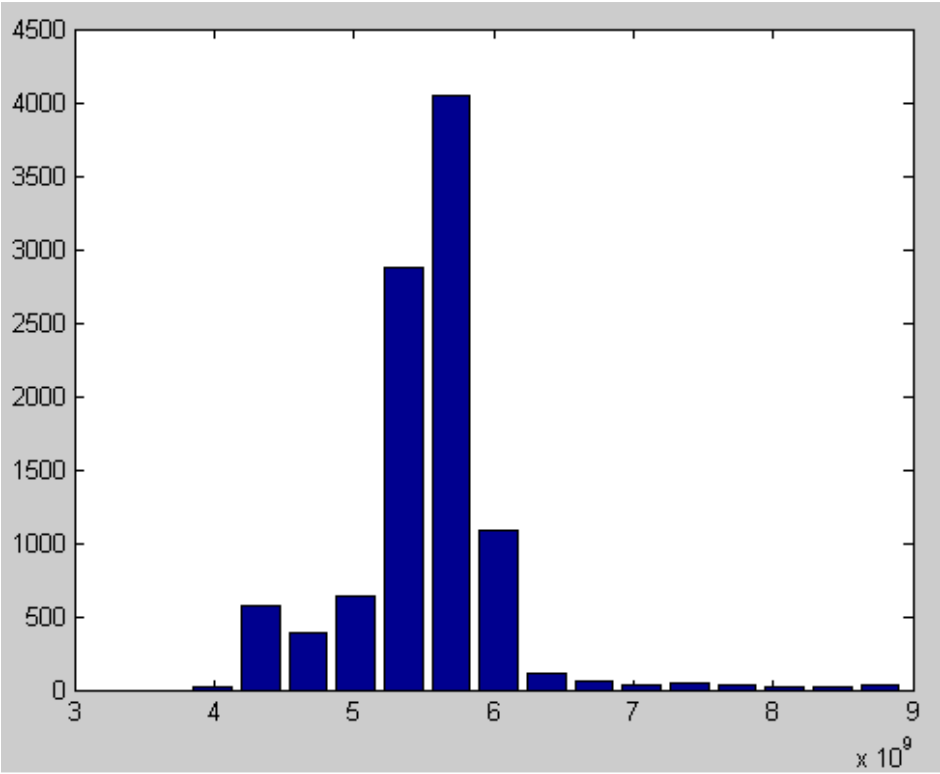
which are Node 3, 4 and 5 for Design 1 (see Figure 3.8), and Node 1 to Node 8 in Design 2, 3 and 4 (see Figure 4.2). The supply voltages of each design also need to similar, make all the designs work in the same conditions.



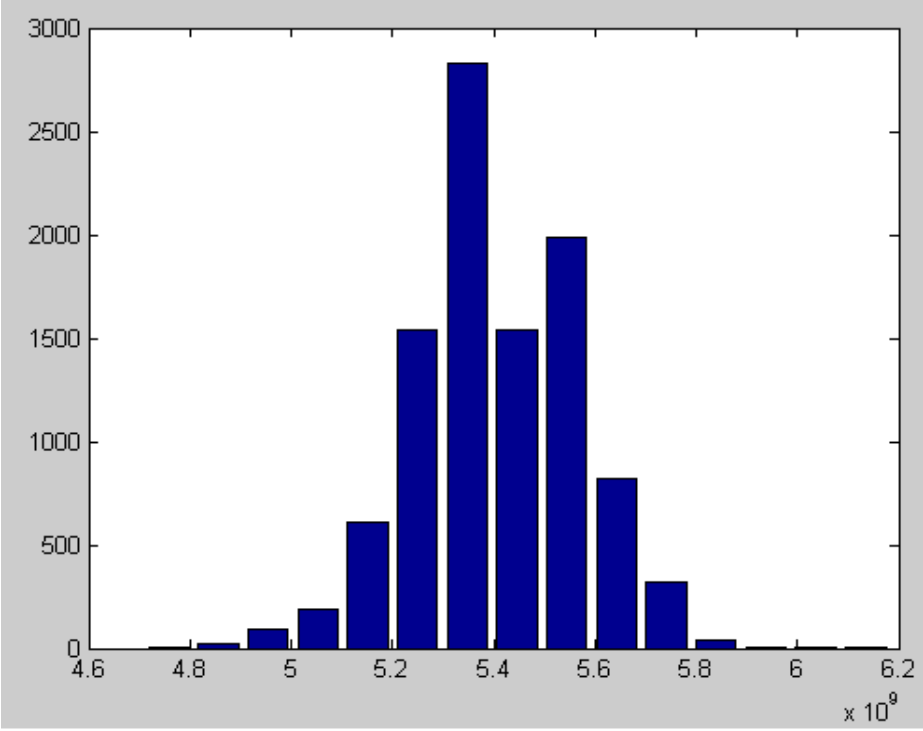
(a) Frequency distribution of Design 1



(b) Frequency distribution of Design 2



(c) Frequency distribution of Design 3



(d) Frequency distribution of Design 4

Figure 4.9

Frequency distributions with variation of Vth

Figure 4.9(a) is the distribution of Design 1, all the data is between 4.5 and 7× 10^9Hz, and most cases are between 5.4 and 6. The range of Design 2 and Design 3 are larger than Design 1, however, their distributions are more

concentrated than Design 1. For design 4, it seems that the distribution is not quite concentrated, however, the value range is fairly narrow, and nearly all the cases are concentrated between 5.2 and 5.8× 10^9Hz, which means that actually, the distribution of Design 4 is quite concentrated. Consider these factors together; Design 4 should be a best design of these four designs.

It is not intuitive to get a result through the figures above; there is a better way to do the comparison that is put all the data in the same coordinate (see Figure 4.10).

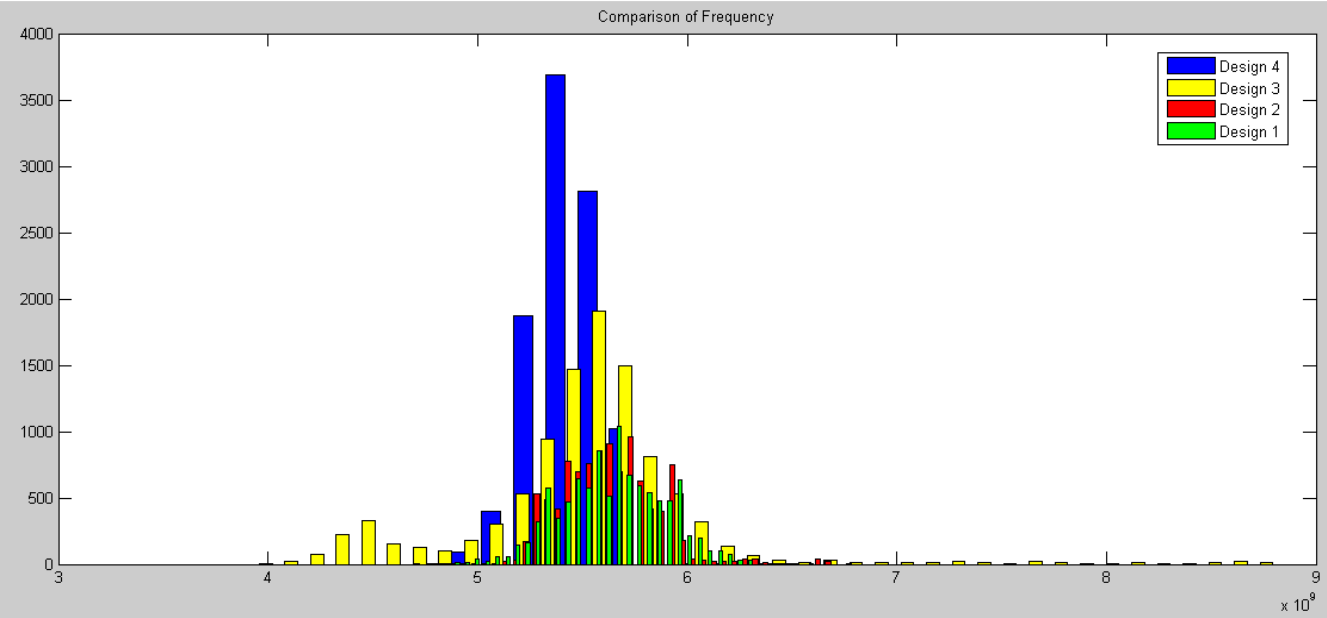


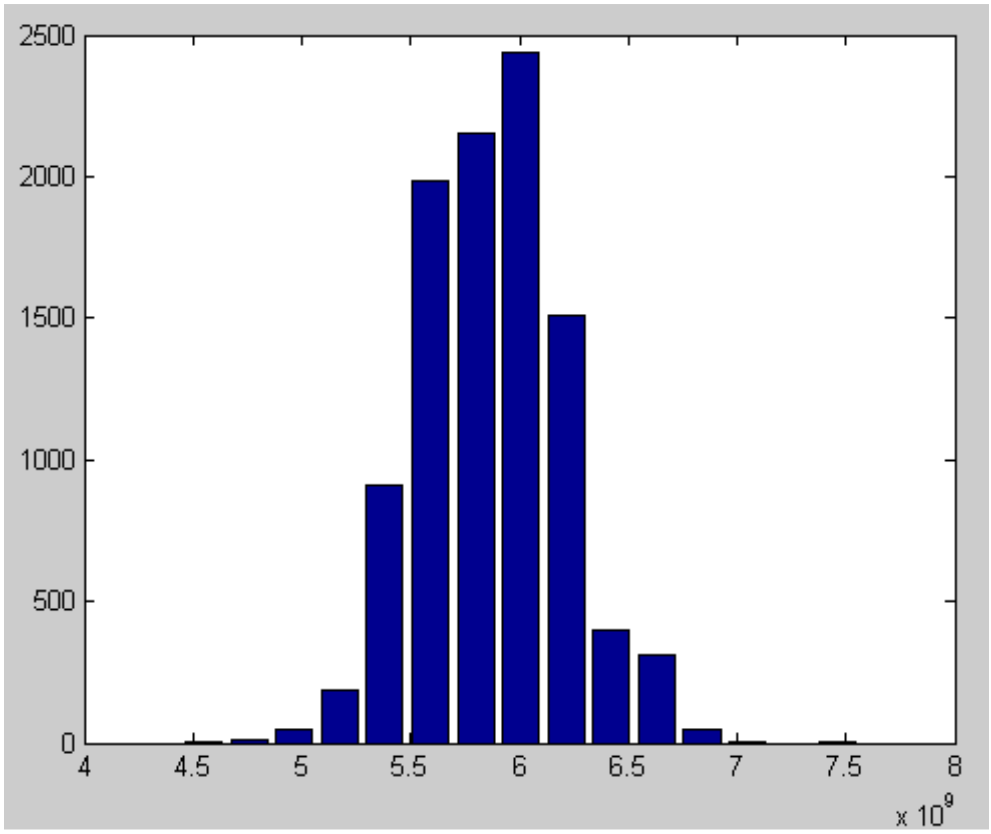
Figure 4.10
Comparison for 130n technology (Vth)

In Figure 4.9, it is obviously that Design 4 is the best one of all; nearly all the cases are much more concentrated than the other designs. Design 3 is also has a nice distribution, however, the range of values is too wide. Design 1 is the worst one, which has a poor distribution.

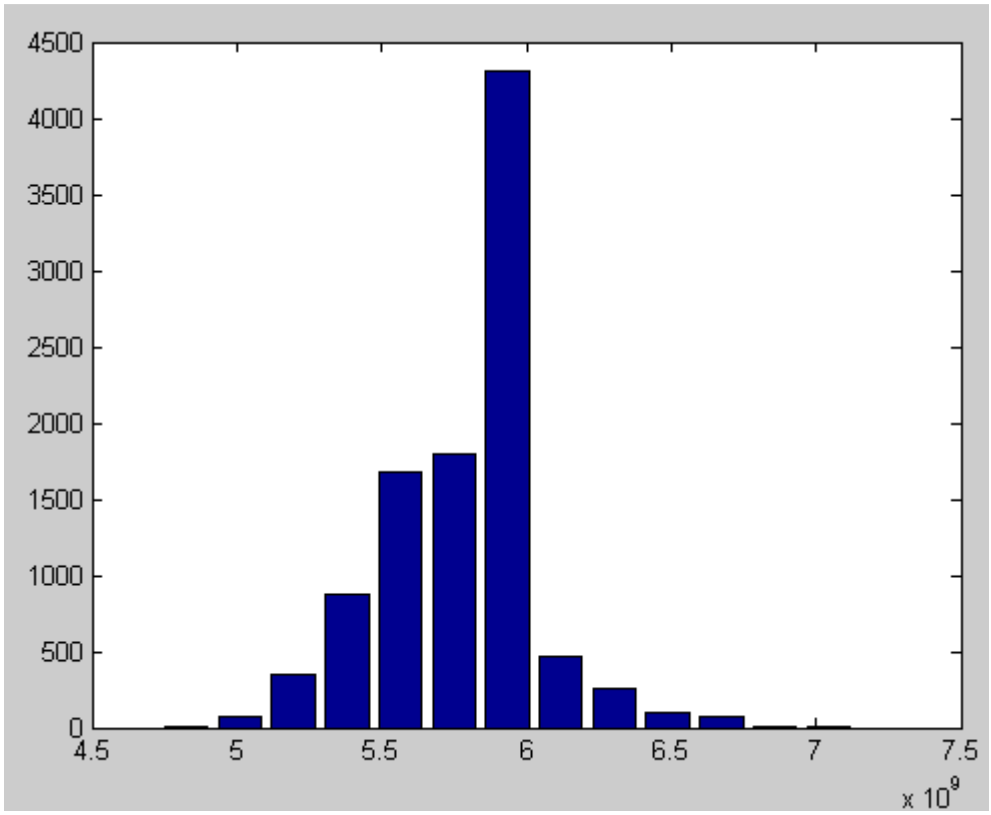
Gate-oxide thickness is another critical parameter for process variation. The next experiments use both threshold voltage and gate-oxide thickness as the variables. See Figure 4.11. Compare Figure 4.11 with Figure 4.9, every design is influenced to various extents. The value ranges of each design are increased and so are the distributions.

Then see Figure 4.12 to get the comparison, Design 4 is still the most stable one, and the deviation extents of other designs' distribution are similar as that in Figure 4.10. Thus, it unnecessary to gives more details.

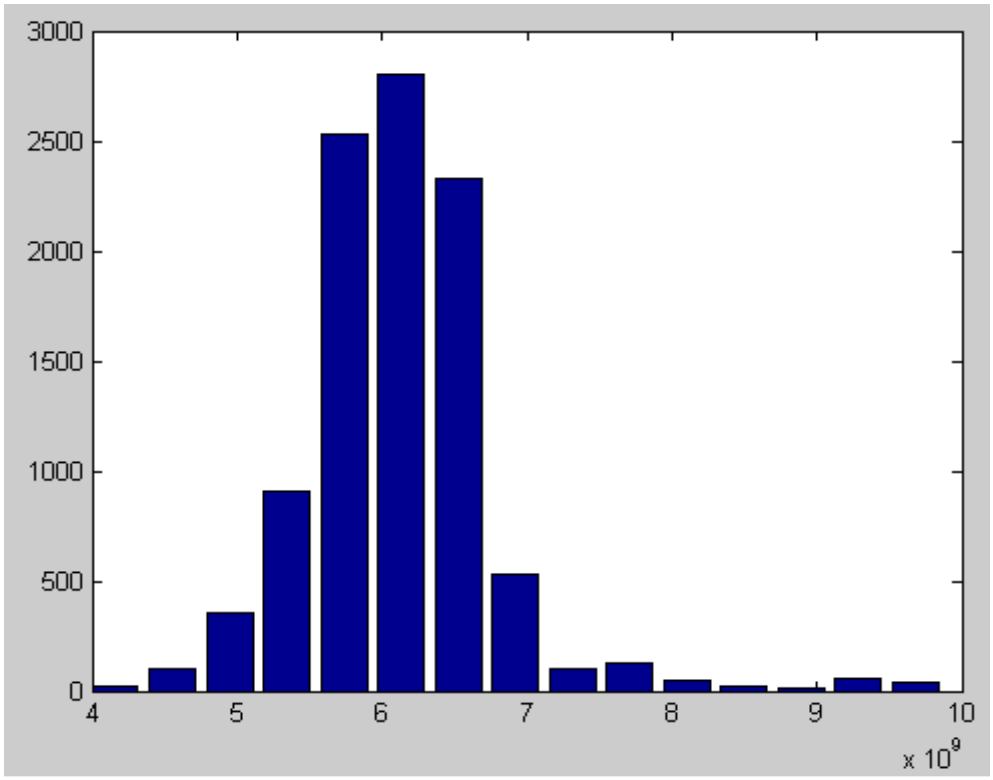
More experimental results of process variation are given in Appendix B.



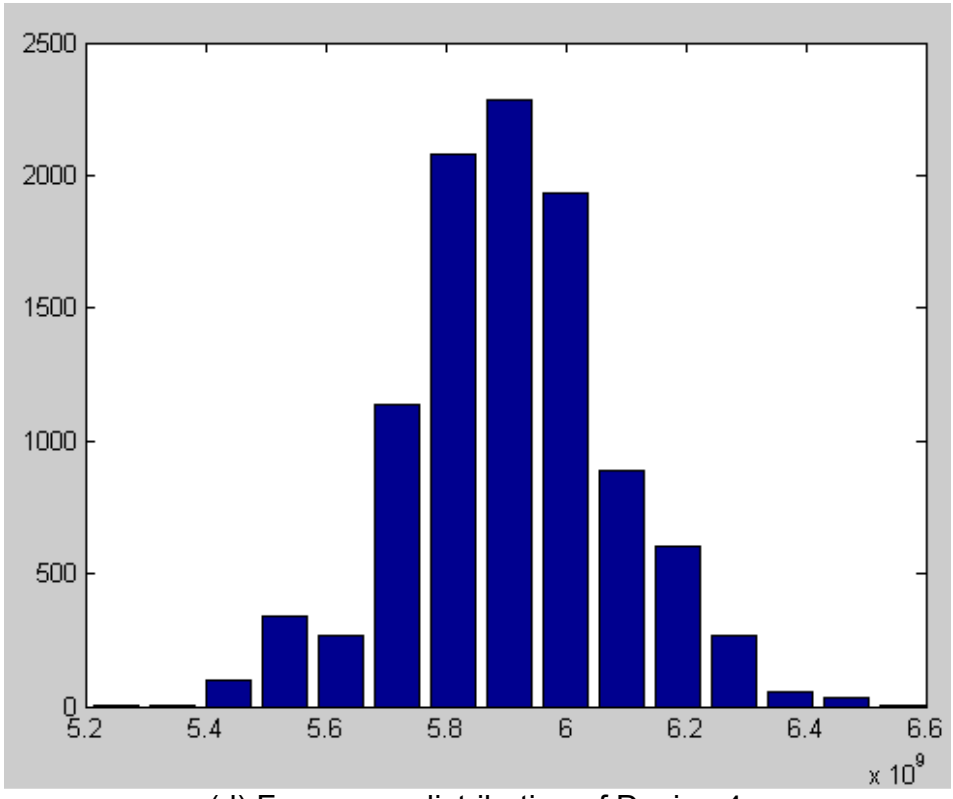
(a) Frequency distribution of Design 1



(b) Frequency distribution of Design 2



(c) Frequency distribution of Design 3



(d) Frequency distribution of Design 4

Figure 4.11
Frequency distributions with variation of Vth and Toxe

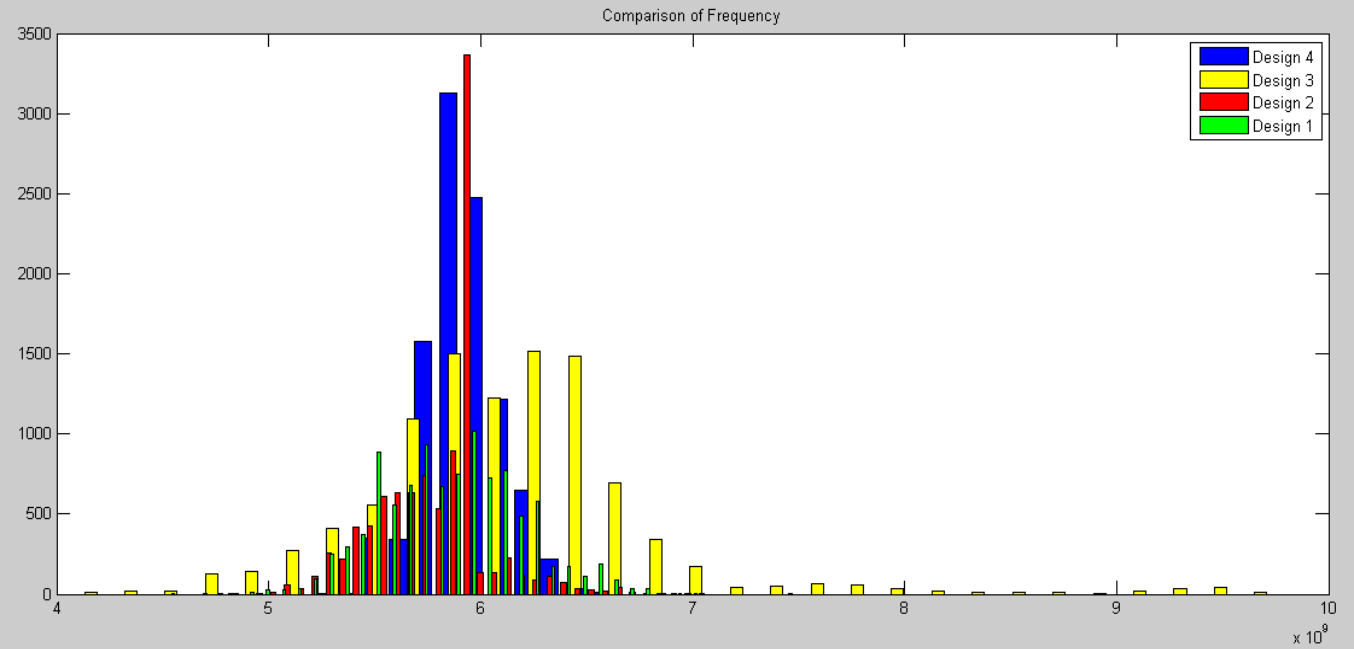


Figure 4.12
Comparison for 130n technology (Vth and Toxe)

Table 4.2
Comparison of standard deviation

Standard Deviation / Design Parameter	Design 1	Design 2	Design 3	Design 4
Vth	2.4852e+008	2.3108e+008	5.3824e+008	1.6593e+008
Vth & Toxe	3.3284e+008	2.6293e+008	6.5322e+008	1.7190e+008

Then the standard deviation of each design will be discussed (Table 4.2). As can be seen from the table, the two standard deviation values of Design 4 have a minimum difference. It is not useful to compare the stability by absolute value, which is because some design has a small part of bad values, which is too far from the mean value, and then these values have far more influences than other values because of the square calculation, especial for Design 3. So a more appropriate way is through comparisons to test the stability.

Synthesize all experimental data of frequency; Design 4 is the best design of all, According to the factors above, Design 3 is not quite excellent, Design 2 is a little better that Design 1. Generally, it seems that double-ended differential structure has better process variation tolerance ability than single-ended structure. The main factor is that double-ended differential structure uses differential amplifier, which is less sensitive to variations of common-mode voltage that caused by sources (such as the supply voltage) and jitter in the circuits.

4.5 Power Consumption Distribution with Process Variation

Power consumption is also changed with process variation, though the influence on VCO that caused by variation of power consumption is not as significant as frequency, it can also research the power preservation ability of each design. Use 90n technology as an example (Figure 4.13, with process variation of Vth). Similar as frequency, the distribution of power consumption is also expressed by an approximate Gaussian distribution. It is obviously that the power consumption of Design 4 is much more than the others, as introduced before, the complex structure and more transistors usage are the main factors cause it.

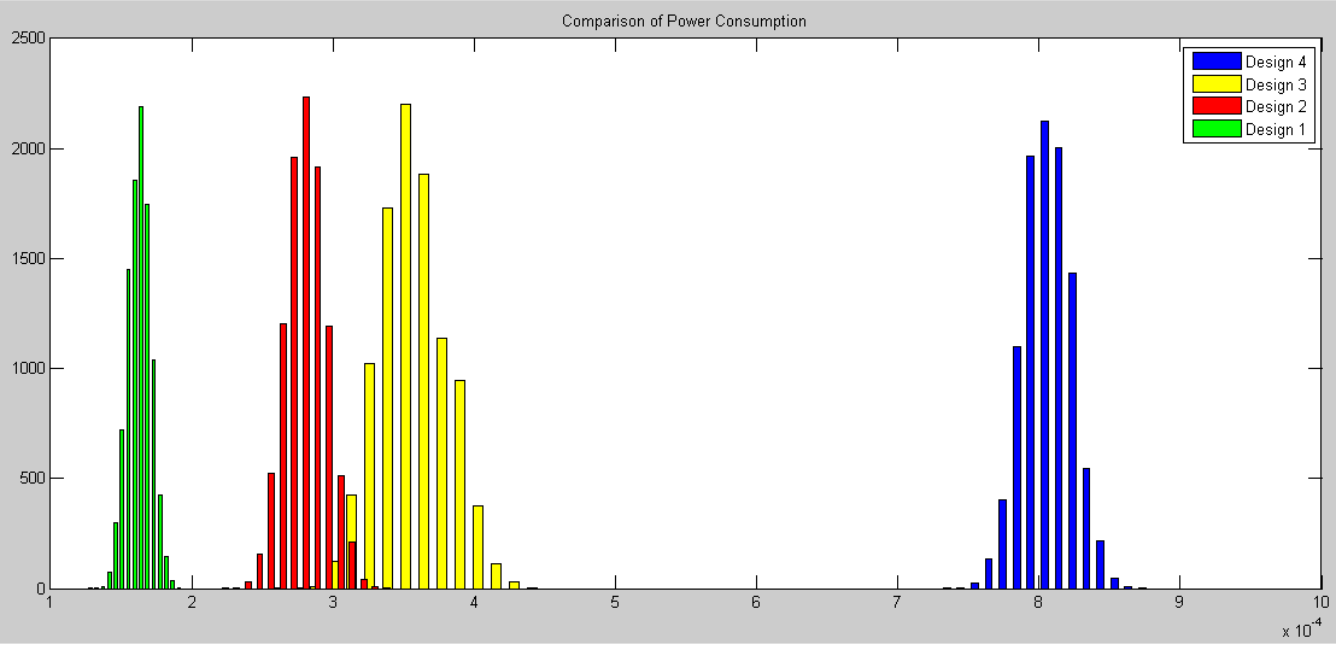


Figure 4.13
Comparison of Power Consumption with process variation

Single-ended ring oscillator has the best power preservation ability, and the deviation of the distribution is also quite small. However, the distribution of power is not the determining factors, so another experiment is count the number of the cases, which have power consumption more than theoretical value. Table 4.3 shows the results of it. As can be seen from the table, Design 1, 2 have the similar number of the more power consumption cases. And the numbers of more power consumption case of all designs have more than half; it indicates that process variation causes more power consumption.

Complex structure is another factor that will cause more power consumption. The structure of load in Design 3 and 4 are important part for process variation tolerance, however, this part also brings unexpected power consumption, especially Design 4 (discussion in next section).

Table 4.3

Designs / Items	Design 1	Design 2	Design 3	Design 4
Theoretical Value	1.626e-04	2.807e-04	3.528e-04	8.020e-04
Number of cases that power more than theoretical Value	5116	5026	6364	5766

4.6 Results Analysis

Synthesize all experimental data; it seems that Design 4 has the best performance except its power consumption. Compared with Design 2 and 3, the feature of Design 4 is the load part and cross-coupled structure. Design 4 uses the cross-coupled loads; the effective resistance of these loads is extremely large. This kind of transistors can generate a negative resistance, and combine with a matched triode resistor, it equals to an infinite resistance. As the Formula 4.1:

$$\frac{R \bullet (-R)}{R + (-R)} = \infty \qquad (4.1)$$

This large resistance reduces the sensitivity of noise at the transitions, and some jitters that generated by the noise. In addition, when status is latched and stable, this structure is quite insensitive to the variations of voltages.

However, because of the infinite resistance, power consumption of Design 4 can be changed by control voltage. The control voltage of Design 2 and 3 needs to be set in a narrow range, which makes the voltage of output in each delay cell, is half of power supply, it is another condition that makes Design 2 and 3 oscillate, and usually, the control voltage is half of the supply voltage. However, in Design 4 the operating point can be controlled by the cross-coupled and symmetric load structure, so the control voltage can be used to control the value of the load (in the experiments above, the control voltage of Design 4 is 2V), so it can be set at any value. In addition, it is one of the most important factors that makes Design 4 has such an excellent ability of process variation tolerance. The more resistance the load is, the more tolerance the design will be, so use greater control voltage can make the circuits more stable. However, the power consumption will be increased by the higher resistance; thus, the control voltage cannot set at too high. It should be indicated that this conclusion is resulted based on that the transistors work in linear region.

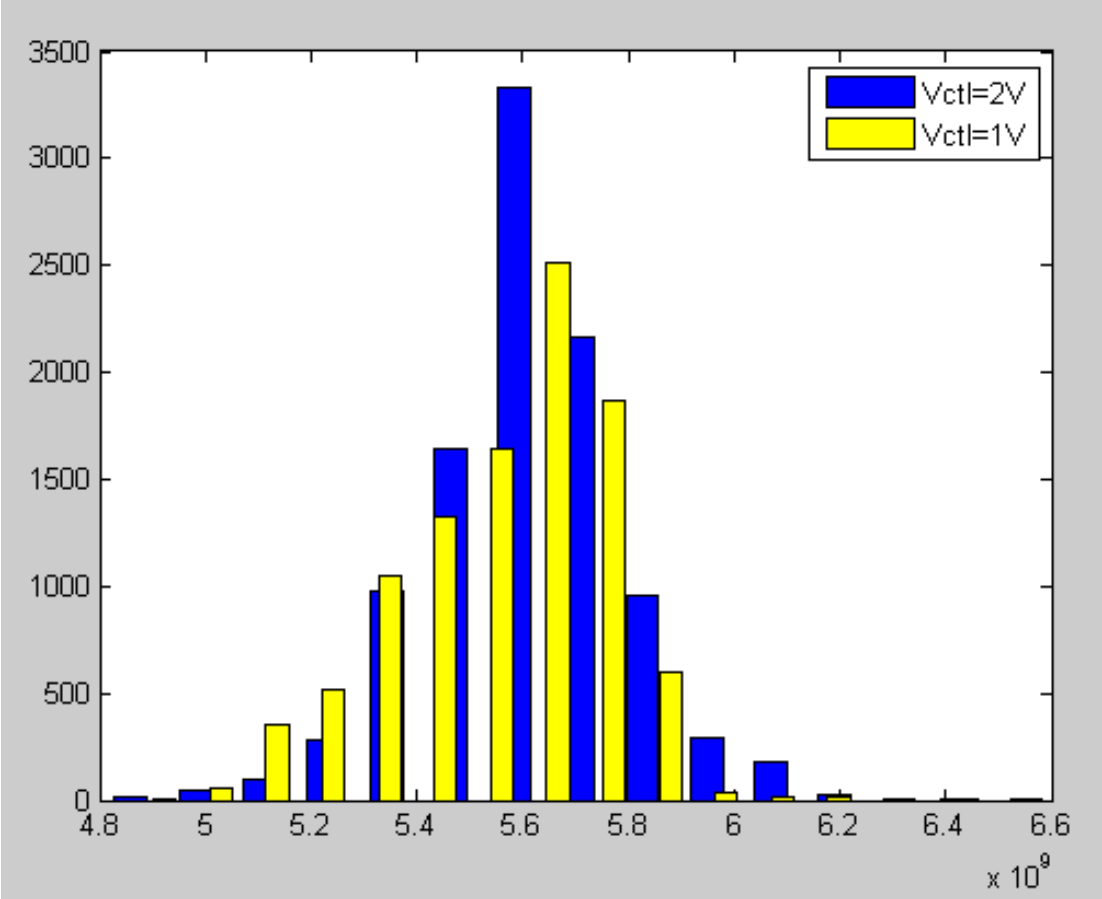


Figure 4.14
Comparison of Design 4 with different Vctl

Then a comparison about the influence of control voltage in Design 4 will be given. Firstly, Figure 4.14 shows the comparison of the frequency distribution with process variation of Vth and Toxe, which use 1V and 2V as control voltage respectively, it can be seen that the stability of greater control voltage case is a litter better than the other one. And through standard deviation also gets the same results, which are 1.9266e+008 and 1.8187e+008 respectively.

Power consumption is also changed with control voltage. For example, when supply power is 1.2V and bias voltage is 0.6V, the power consumption in 90n and 130n technologies is showed as an example in Table 4.4:

It can be seen clearly that power consumption increases by control voltage; however, too large Vth will make the transistor works in nonlinear amplifying region, just as 3V case.

In the applications, getting an equilibrium point that makes the system has satisfactory performance and suitable power consumption is worth studying.

Table 4.4
Power consumption variation with control voltage

Scale / Vctl	90n	130n
1 V	6.504e-04	7.751e-04
1.5 V	6.858e-04	8.140e-04
2 V	6.927e-04	8.258e-04
3 V	6.788e-04	8.155e-04

Another point needs to be noticed is that in 32n and 45n scale Nano-Cmos technology, during the simulation of process variation, failed cases happened in Design 3, which is that the oscillation cannot work in a certain condition. In experiments with process variation, there are 73 failed cases for 32n technology and 65 failed cases for 45n technology. In summary, it seems that Design 3 is not suit for these two technologies.

4.7 Summary

In this chapter, a part of experiential data was given to show the tendency and the distribution of frequency and power consumption, and then gets a conclusion about some properties of VCO and process variation tolerance of each design.

During the experiments, setting control voltage and bias voltage and adjusting the delay of each cell are two critical points, the former one is mainly used to satisfy the condition of oscillation of Design 2 and 3; the latter one can be implemented by using resistance and capacitance, which is used to observe the process variation tolerance ability among different designs, it also a common method in VCO technology.

According to the experimental data, the frequency of VCO is in proportion to supply voltage and in inverse proportion to the scale of Nano-CMOS. A design that uses smaller scale can be used for portable devices; however, the stability of the circuits is also poor in smaller scale design, it will be affected dramatically by process variation. Design 4 is the best design of all designs researched in this project, which has robust process variation tolerance ability, though because of its complex structure, the power consumption is higher. Design 1 is not quite stable, but it has good power conservation due to its simple structure.

The control voltage of Design 4 is different with the other designs of double-ended differential structure; this voltage can be adjusted under requirements. Higher control voltage can promote the process variation tolerance ability; however, it also causes side effects, which will increase power consumption.

To sum up, some cases of experiments have been given and analyzed, through this chapter, some attributes and principle of VCO is resulted. Moreover, the process variation tolerance ability of each design was tested

and compared, and obtained the performance of each design. In the next chapter, conclusions will be given to summarise and synthesise all the experiments and results.

Chapter 5: Conclusion

The first target of this report was to research VCO circuits. Firstly, introduction of motivation and aims of this project were given in Chapter 2, and then background and basic principles of VCO were also discussed. The important principle called process variation was described, and then a set of tools and simulation methods were used to implemented process variation experiments, which combined Monte Carlo simulation and Gaussian distribution and were using in Hspice to simulate. Then, materials are used to introduce that the most important parameters, which affect process variation significantly, are threshold voltage, gate-oxide thickness and supply voltage. In this chapter, the main work of this project is indicated, which is that get a design that has robust process variation tolerance ability through experiments, and analyze its power consumption.

In Chapter 3, the detailed implementation procedures of simulation experiments were demonstrated, mainly including the code of hardware description, the code of simulation, the functions of two kinds of software, the calculation of experimental data and the generation of graphs. The experiments can be divided into two parts, which used to analyze the attributes of VCO and process variation tolerance about designs respectively. In addition, a simple example was given to explain the process of the experiments and data generation, it is useful to explain how to generate the data from Hspice and deal with them in Matlab.

1. Chapter 4 showed some representative experimental data of each experiment. The first part was tested attributes of VCO, which was about the frequency and power consumption that changed with supply power and scale of Nano-CMOS. The second part was the comparison of process variation tolerance ability of designs, and the power consumption as well. During these experiments, the conclusions can be summarized as points below:
2. The frequency of VCO is in proportion to supply voltage, and in inverse proportion to the scale of transistors.
3. The power of VCO is in proportion to both supply voltage and scale of transistors, it is also affected by control voltage and bias voltage.
4. The control and bias voltages in Design 2 and Design 3 need to adjust to make the voltage of output is half of the supply voltage, which is a starting condition for oscillation. However, due to different structure, control voltage in Design 4 can be used to increase the process variation tolerance. The larger control voltage is, the more stable VCO is.
5. Design 4 has the best process variation tolerance ability. Double-ended ring structure is more stable than Single-ended ring structure. Design 1 is the best in power preservation. All designs conditions are showed in Table 5.1.

According the results in this dissertation, double-ended ring oscillator is better to use in VCO designs, and combined cross-coupled differential delay cell with symmetric loads structure will be used with an appropriate control voltage

to avoid more power consumption.

Table 5.1
Experimental results summary

	Design 1	Design 2	Design 3	Design 4
32n	suited	suited	unsuitable	suited
45n	suited	suited	unsuitable	suited
65n	suited	suited	suited	suited
90n	suited	suited	suited	suited
130n	suited	suited	suited	suited
Process variation tolerance	poor	well	quite good	Excellent
Power consumption	Excellent	quite good	good	Poor, but can be adjusted by control voltage

Chapter 6: Future Development

Although lots of works about process variation for VCO system have been implemented, there is still ample room for improvement. In this chapter some drawbacks and problems that existing in the experiments will be discussed.

6.1 Time of Experiments

From the experiments it can be realized that Monte Carlo simulation is based on a large number of simulations to get a distribution. Generally, the number of these simulations is tens of thousands or more, which will need a quite long time to run. It is necessary to find a way to shorten time and increase efficiency.

In my opinion, there are two way to amend this defect. The first one is decrease the simulation time through waveform. For oscillator, it only needs a short time to arrive at a steady state condition, so according to this time to set simulation time can decrease unexpected time wasting. However, it should be considered the variation during the process variation experiments, so some time margin needs to be given.

Another method is using parallel technology, which can make several processes execute synchronously. It should be noticed that parallel streams produced on different processors should be uncorrelated, so it needs to use different random number generator on different processors, and assign different sub streams to different processors. Leapfrog approach is another way to solve it.

6.2 Power and Frequency

According to experimental data, it seems that in order to get a higher stability, it needs to consume more power. It should be have an equilibrium point that has a best cost performance. In addition, if better designs can be obtained to improve the performance of VCO is also worth to research. One method is that continue to decrease the scale of Nano-CMOS, but it demands a more advanced design to increase process variation tolerance ability. During the experiments, the working conditions of each design in the 32n and 45n technologies are obviously worse than that in 130n technology. On the other hand, it should be design different VCO according to different requirements.

6.3 Simulation of PLL

As introduced above, VCO is a main part of PLL, so it is important to simulate with a complete PLL to verify these VCO designs in a complete system, which

will have new variations during the simulations. The effects of loading the output of VCO can also be tested, and the investigation of compensation as well.

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[23] D.j. O’Brien “5 Gbps VCO for USB 3.0”, pp19-20, Sep. 2008.

Appendix A: Source Code

Part A

Source code for each design (use 32n, the others just change the libraries of technologies):

1.Design 1

```
*Design 1: 32n
.option  nopage nomod post

*initial condition
.ic v(3)=0
.param nvt= agauss(0.5088v,0.05088v,3)
.param pvt= agauss(-0.450v,0.045v,3)
.param ntoxe= agauss(1.65e-9v,1.65e-10v,3)
.param ptoxe= agauss(1.75e-9v,1.75e-10v,3)
.param l=32n
.tran 20p 0.7n sweep monte=10000

*voltage sources
v1 vcc  0 1.2
v2 vcc2 0 0.6
.enddata

*Components
m1 vcc 1 1 vcc pmos l='l' w='4*l'
m2 vcc 1 2 vcc pmos l='l' w='4*l'
m3 1  vcc2 0 0 nmos l='l' w='4*l'
m4 6  vcc2 0 0 nmos l='l' w='4*l'

Xinv1 3 4 2 6 inv
Xinv2 4 5 2 6 inv
Xinv3 5 3 2 6 inv

.subckt inv in out vdd gnd
m5 vdd in out vcc pmos l='l' w='4*l'
m6 out in gnd 0   nmos l='l' w='4*l'
.ends inv

*measure
.meas m_power rms power
.meas tran maxval MAX v(1) from=0.5ns to=0.7n
.meas tran minval MIN v(1) from=0.5ns to=0.7n
.meas tran tdelay trig v(1) val='(maxval + minval)*0.5' fall=4
+targ v(1) val='(maxval + minval)*0.5' fall=5
```

(Library of each Nano-CMOS technology is added here, too long so ignore here, relevant information in *http://ptm.asu.edu/*, version: BSIM4 model card for bulk CMOS: V1.0)

2. Design 2

```
*Design 2: 32n
*.option  nopage nomod post
*initial condition

.ic v(1)=0 v(5)=0.9

.param l=32n
.param nvt= agauss(0.5088v,0.05088v,3)
.param pvt= agauss(-0.450v,0.045v,3)
.param ntoxe= agauss(1.65e-9v,1.65e-10v,3)

.param ptoxe= agauss(1.75e-9v,1.75e-10v,3)
.tran 20p 0.7n sweep monte=10000

*voltage sources
vdd   vcc  0 1.2
vct   vcc2 0 0.56
vbias vcc3 0 0.62

*Components
```

Part B

Data processing code in Matlab
This is the code for process variation simulations, change open file name to get graph for different designs.

```
clear all;
clc;
fid = fopen('single-ended.mt0','r');
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);

format('short','e');
d                    =                    fscanf(fid,
'%e %e %e %e %e %e %e %e', [9 inf]);
T=d';
fclose(fid);
delay=T(:,3);

figure(1)
fre=1./delay;
bins=linspace(min(fre), max(fre),15);
C=hist(fre,bins);
bar(bins,C)
```

This is the code for frequency comparison among each technology.

```
clear all;
clc;
blank=[0,0,0];
fid = fopen('single-ended-32.mt0','r');
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
format('short','e');
d                    =                    fscanf(fid,
'%e %e %e %e %e %e %e %e', [8 inf]);
T=d';
fclose(fid);
delay=T(:,6);
freq1=1./delay;

fid = fopen('single-ended-45.mt0','r');
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
format('short','e');
d                    =                    fscanf(fid,
'%e %e %e %e %e %e %e %e', [8 inf]);
T=d';
fclose(fid);
delay=T(:,6);
freq2=1./delay;

fid = fopen('single-ended-65.mt0','r');
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
format('short','e');
d                    =                    fscanf(fid,
'%e %e %e %e %e %e %e %e', [8 inf]);
T=d';
```

```
xdif1 1 5 2 6 vcc vcc3 9  dif
xdif2 2 6 3 7 vcc vcc3 10 dif
xdif3 3 7 4 8 vcc vcc3 11 dif
xdif4 4 8 5 1 vcc vcc3 12 dif

m5 9  vcc2 0 0 nmos l='l' w='4*l'
m6 10 vcc2 0 0 nmos l='l' w='4*l'
m7 11 vcc2 0 0 nmos l='l' w='4*l'
m8 12 vcc2 0 0 nmos l='l' w='4*l'

.subckt dif in1 in2 out1 out2 vdd vdd2 gnd
m1 vdd  vdd2 out1 vdd pmos l='l' w='4*l'
m2 vdd  vdd2 out2 vdd pmos l='l' w='4*l'
m3 out1 in1  gnd  0   nmos l='l' w='4*l'
m4 out2 in2  gnd  0   nmos l='l' w='4*l'
.ends dif

*measure
.meas m_power rms power
.meas tran maxval MAX v(1) from=0.5ns
to=0.7n
.meas tran minval MIN v(1) from=0.5ns to=0.7n
.meas tran tdelay trig v(1) val='(maxval +
minval)*0.5' fall=4
+targ v(1) val='(maxval + minval)*0.5' fall=5
```

3. Design 3

```
*Design 3: 32n
.option  nopage nomod post
*initial condition
.ic v(1)=0

.param l=32n
.param nvt= agauss(0.5088v,0.05088v,3)
.param pvt= agauss(-0.450v,0.045v,3)
.param ntoxe= agauss(1.65e-9v,1.65e-10v,3)
.param ptoxe= agauss(1.75e-9v,1.75e-10v,3)


.tran 20p 0.7n sweep monte=10000

*voltage sources
vdd   vcc  0 1.2
vct   vcc2 0 0.53
vbias vcc3 0 0.67

*Components
xdif1 1 5 2 6 vcc vcc2 9  dif
xdif2 2 6 3 7 vcc vcc2 10 dif
xdif3 3 7 4 8 vcc vcc2 11 dif
xdif4 4 8 5 1 vcc vcc2 12 dif

m7  9  vcc2 0 0 nmos l='l' w='4*l'
m8  10 vcc2 0 0 nmos l='l' w='4*l'
m9  11 vcc2 0 0 nmos l='l' w='4*l'
m10 12 vcc2 0 0 nmos l='l' w='4*l'

.subckt dif in1 in2 out1 out2 vdd vdd2 gnd
m1 vdd  out1 out1 vdd pmos l='l' w='4*l'
m2 vdd  vdd2 out1 vdd pmos l='l' w='4*l'
m3 vdd  vdd2 out2 vdd pmos l='l' w='4*l'
m4 vdd  out2 out2 vdd pmos l='l' w='4*l'
m5 out1 in1  gnd  0   nmos l='l' w='4*l'
m6 out2 in2  gnd  0   nmos l='l' w='4*l'
.ends dif

*measure
.meas m_power rms power
.meas tran maxval MAX v(1) from=0.5ns
to=0.7n
.meas tran minval MIN v(1) from=0.5ns to=0.7n
.meas tran tdelay trig v(1) val='(maxval +
minval)*0.5' fall=4
+targ v(1) val='(maxval + minval)*0.5' fall=5
```

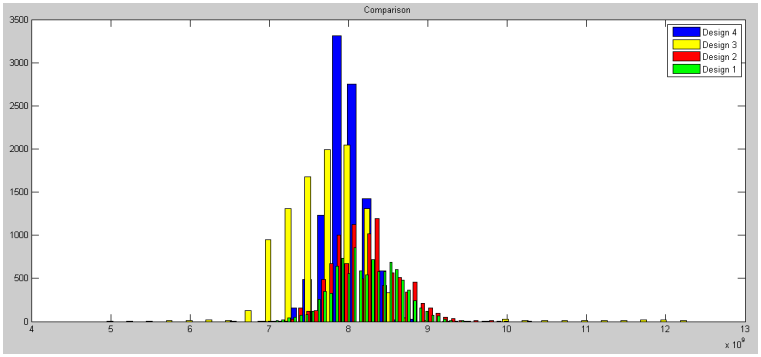
```
fclose(fid);
delay=T(:,6);
freq3=1./delay;

fid = fopen('single-ended-90.mt0','r');
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
format('short','e');
d                    =                    fscanf(fid,
'%e %e %e %e %e %e %e %e', [8 inf]);
T=d';
fclose(fid);
delay=T(:,6);
freq4=1./delay;

fid = fopen('single-ended-130.mt0','r');
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
line = fgetl(fid);
format('short','e');
d                    =                    fscanf(fid,
'%e %e %e %e %e %e %e', [8 inf]);
T=d';
fclose(fid);
delay=T(:,6);
freq5=1./delay;

freq=[freq1',blank,freq2',blank,freq3',blank,fre
q4',blank,freq5'];
figure(1);
bar(freq);
```

4. Design 4

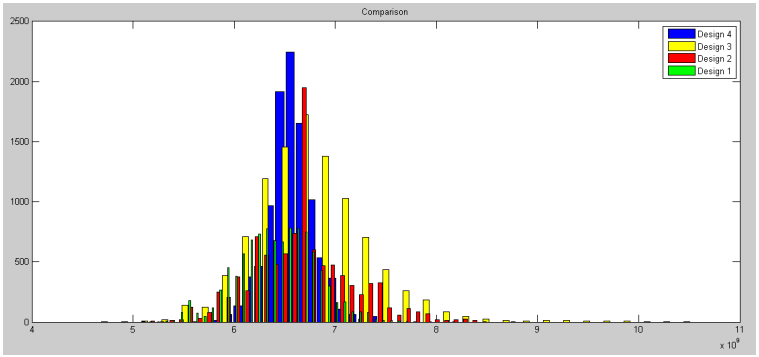
```
*Design 4: 32n
.option  nopage nomod post
*initial condition
.ic v(1)=0

.param l=32n
.param nvt= agauss(0.5088v,0.05088v,3)
.param pvt= agauss(-0.450v,0.045v,3)
.param ntoxe= agauss(1.65e-9v,1.65e-10v,3)
.param ptoxe= agauss(1.75e-9v,1.75e-10v,3)
.tran 20p 0.7n sweep monte=10000

*voltage sources
vdd   vcc  0 1.2
vct   vcc2 0 2
vbias vcc3 0 0.6

*Components
xdif1 1 5 2 6 vcc vcc2 9  dif
xdif2 2 6 3 7 vcc vcc2 10 dif
xdif3 3 7 4 8 vcc vcc2 11 dif
xdif4 4 8 5 1 vcc vcc2 12 dif

m9  9  vcc2 0 0 nmos l='l' w='4*l'
m10 10 vcc2 0 0 nmos l='l' w='4*l'
m11 11 vcc2 0 0 nmos l='l' w='4*l'
m12 12 vcc2 0 0 nmos l='l' w='4*l'

.subckt dif in1 in2 out1 out2 vdd vdd2 gnd
m1 vdd  vdd2 out1 vdd pmos l='l' w='4*l'
m2 vdd  out1 out1 vdd pmos l='l' w='4*l'
m3 vdd  out2 out1 vdd pmos l='l' w='4*l'
m4 vdd  out1 out2 vdd pmos l='l' w='4*l'
m5 vdd  out2 out2 vdd pmos l='l' w='4*l'
m6 vdd  vdd2 out2 vdd pmos l='l' w='4*l'
m7 out1 in1  gnd  0   nmos l='l' w='4*l'
m8 out2 in2  gnd  0   nmos l='l' w='4*l'
.ends dif

*measure
.meas m_power rms power
.meas tran maxval MAX v(1) from 0.5n to 0.7n
.meas tran minval MIN v(1) from 0.5n to 0.7n
.meas tran tdelay trig v(1) val='(maxval +
minval)*0.5' fall=4
+targ v(1) val='(maxval + minval)*0.5' fall=5
```

Appendix B: Experimental Data Graph

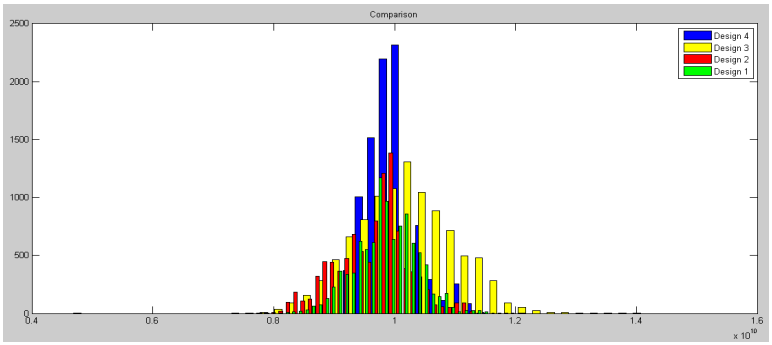
All the process variation data are given in Appendix B.



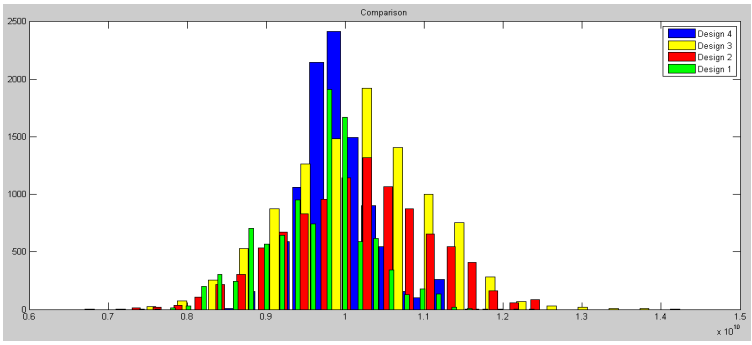
Vth, 90n



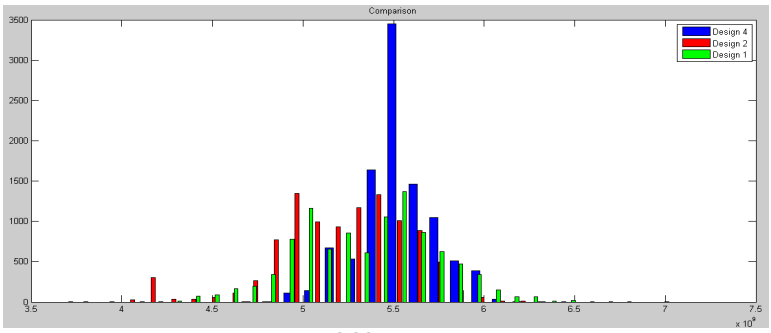
Vth and Toxe, 90n



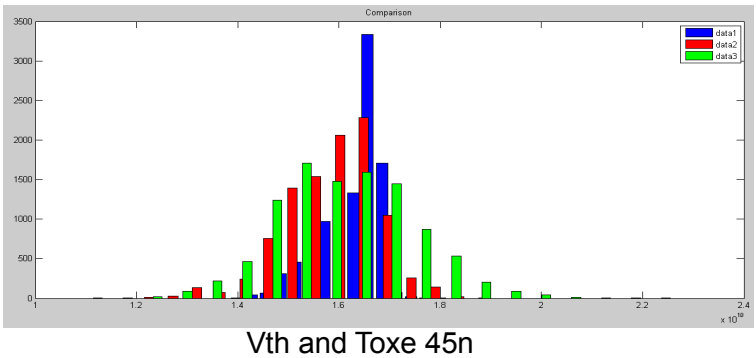
Vth, 65n



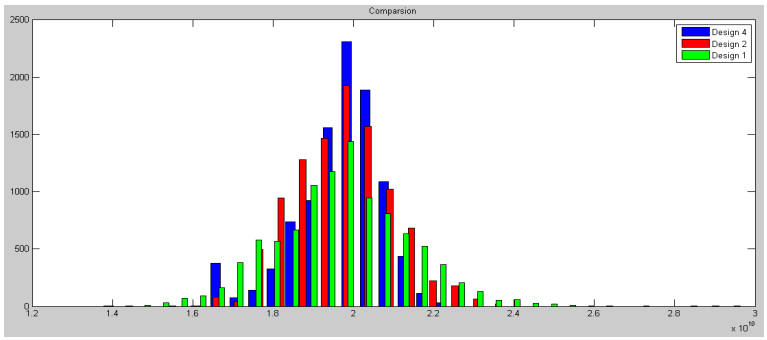
Vth and Toxe 65n



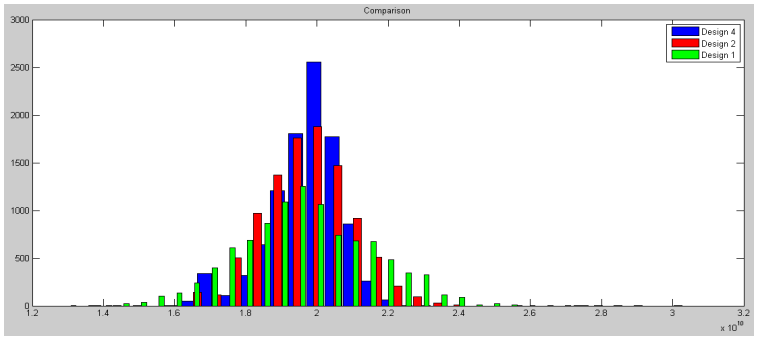
Vth 45n



Vth and Toxe 45n



Vth 32n



Vth and Toxe 32n

Due to poor stability in 32n and 45n technologies, the data of Design 2 have not added in these two technologies.