Abstract

This project is devoted to investigate an integrated circuit topology of feedforward technique. Unlike feedback technique, feedforward does not need a high gain forward amplifier, thus theoretically the system applying feedforward technique should not suffer from a relatively narrow bandwidth. The aim of this project is going to explore and establish a circuit design using gdpk180 technique. Comparison with feedback loop is also being carried out in this project.

Acknowledgements

This paper is dedicated to my class mates of MS55 2009/2010 whose optimism and assistance was a great help to me through the tough times. I would like to express my thanks to my parents who provide me such a good opportunity to study abroad. I also wish to thank my girl friend Chen Zhang to help me keep confident when I was depressed.

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Contents:

Chapter1. Objectives and Organization

1.1 Aims and objectives

The project objective in general is to explore and design an integrated circuit topology using feedforward technique to achieve linearised large signal transferring. Feedforward technique is used to compensate the distortion and keep the system linear. This technique is not based on a negative feedback controlled loop, the concept and principle of this technique is to work out the distortion signal first and then to eliminate it from the system. And theoretically, this circuit should have a good performance at high frequencies. In analogue design, a linear voltage control current source is the most valuable and hard to design, thus in this project, the aim is to design a voltage input and current output transformation block, and both input and output should have a wide range.

The objectives can be specified in the following items,

- The input voltage is required to be 0 ∽ 1V, and output current is required to be 0 ∽ 200uA, the input resistance is required to be low and output resistance is required to be high,
- Splitting up the overall circuit into several functional units,
- Deciding the signal format of each stage,
- Choosing suitable circuit topology to build up each functional units,
- Sizing the FETs of each functional units to make sure they work in the correct mode,
- Improving the performance of each units by using some advanced topology,
- Overall analysis and justifying the circuit according to the simulation result,
- PVT analysis
- Comparison with feedback technique

1.2 Organization of this dissertation

This dissertation consists of six main parts.

Firstly, the next chapter introduces the background knowledge of the feedforward loop.

Secondly, chapter 3 explores the circuit implementation of the feedforward loop, from the top level design down to the basic functional unit design and transistor sizing topics.

Thirdly, the overall performance of the feedforward circuit and PVT analysis will be given in chapter 4,

In the following chapter, a comparison between feedforward loop and feedback loop is also presented.

Then, a review of all the work being carried out in this project is presented in the following chapter and a reasonable conclusion is drawn after this.

Finally, some suggestions which could improve the performance of the feedforward loop will be given on the Future Work in chapter 6.

Chapter2. Background and Context

2.1 Feedforward introduction and application

Feedforward is a relatively new technology of keeping an electronic system stable and keeping the signal transferring without distortion. It is first used in communication system. Linearised components are becoming more and more important in modern communication system and microelectronics system. There are several kinds of linearization technologies. Beside feedforward, feedback and predistortion are major techniques. Among these three, Feedforward has some obvious advantages compared to others. Since the main idea of feedforward is to separate and subtract the distortion signal from the non-Linearised amplified signal, the high gain which main amplifier provides will not degrade, and as long as the phase shift and gain are precisely controlled, the power amplifier will be unconditional linear. [1]

2.2 Feedforward system

The basic feedforward system contains those elements: two amplifiers, which are main amplifier and error amplifier, four couplers, two delay components. [1] The main amplifier generates amplified output signal, as long as distortion part. The error amplifier is to adjust the amplitude and phase of the error signal to generate the cancellation signal. Those couplers work as signal splitter and signal combiner. Delay components are designed to generate a small delay in time domain, or in other words, generate a phase shift.

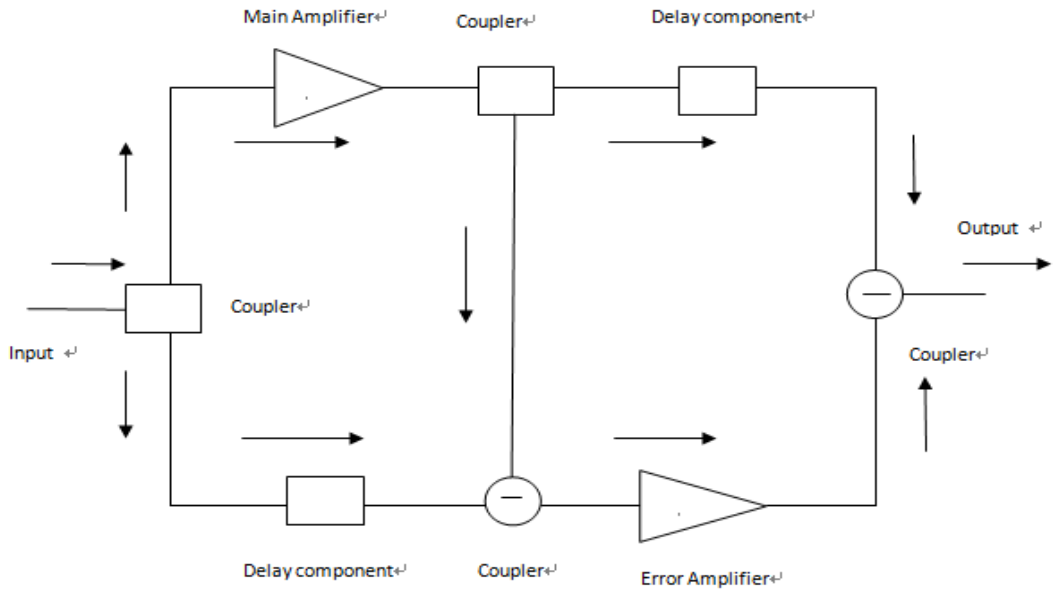

Figure 1. Feedforward topology

2.2.1 Main amplifier

Main amplifier generates the output signal with distortion part. There are some reasons why distortion part is introduced into the system. If the main amplifier works in class AB, or class B, or even class C mode, harmonic signal will be added in. Noises can also be added into this system forming the distortion under different temperature and pressure situation. The analysis of distortion signal depends on specific real scenario.

2.2.2 Error amplifier

The requirement for error amplifier in a feedforward system is that it should have better linearity, more broadband performance, and lower average and peak power capability.

The gain and phase flatness requirements on the error amplifier depend upon the required loop suppression, which is a function of intermodulation performance of the main amplifier and the desired feedforward output linearity. Another important feature of the circuit is that the bandwidth of distortion cancellation loop is much larger than carrier cancellation loop.

2.2.3 Couplers

Couplers are used as a power divider or combiner in the feedforward system. Power

is divided in two streams before flows into the main amplifier and after amplified by the main amplifier, and power is combined for carrier cancellation and distortion cancellation in the first loop and second loop respectively. A simple implementation of this component is to use resistive dividers (provided that the transferring signal is voltage, not current). But it suffers from the disadvantage of being sensitive to mismatching errors. Some research need to done to find proper signal couplers under specific circumstance.

Feedforward input coupler. This power splitter at the input of feedforward separates the input signal into two paths: one going to the main amplifier, the other to the delay component.

Main amplifier output coupler. The high power separates at the output of the main amplifier to generate a carrier cancellation signal for the first feedforward loop.
Carrier cancellation coupler, it performs a function of power combiner here. The delayed signal and sampled output signal of the main amplifier have a phase difference of π. Thus actually this coupler works as a subtractor.
Distortion cancellation coupler, the cancellation coupler in loop2 also works as a combiner and has the functionality of a subtractor. This time, the distortion component is canceled rather than the carriers.

2.2.4 Delay component

Introduce a certain delay and gain into the system to ensure that two signals have the opposite phase and same amplitude in the cancellation point.

2.3 Feedforward features

2.3.1 Distortion performance

Since the non ideal input signal consists of many carriers with uniform carrier spacing Δf, the distortion component will appear on frequencies which have a space of Δf to its neighbor according to the intermodulation effect. At the same time, certain noise is introduced into the main amplifier. Separation the distortion component and noise of first amplifier and then subtract them in the second loop is an advantageous method to keep the amplified signal linear.

2.3.2 Signal cancellation

Feedforward depends on two important elements, which are separation of the distortion error signal and cancellation of this distortion component from the

amplified signal. Signal cancellation at a single frequency is achieved by the subtraction of two signals with same amplitude, which means it can also be achieved by addition of these two signals, with same amplitude and opposite phase. Thus there are three basic requirements for perfect cancellation:

Equal amplitude
180 degree phase difference
Equal delay

2.3.3 Loop cancellation bandwidth

In the first loop, the cancellation signal is the difference between delayed input signal and the sample of amplified distorted signal, thus this cancellation signal equals to the original input signal. And the cancellation bandwidth equals to the bandwidth of input signal, which is the system transmitter bandwidth.

In the second loop, the cancellation signal is the distortion signal which appears at frequencies outside the transmitter band, and therefore this cancellation bandwidth is larger than that of first loop. The cancellation bandwidth of second loop depends on the distortion signal, which in turn depends on the which mode the first amplifier works in, is it a class A amplifier, a class B amplifier ,or a class AB amplifier.

2.3.4 Loop control

Feedforward system theoretically allows operations over a finite bandwidth. But as a disadvantage of open loop structure, the above circuit design lacks of stability, which means any changes in characteristics, such as temperature, voltage, frequencies are not compensated. Therefore the feedforward loop needs a loop control function unit in order to detect the unwanted distortion and adjust the amplitude and phase of the input signal as compensation. First information at the output of feedforward system is gathered to judge how well the circuit is working and then adjust the phase and amplitude of the input signal using a feedback loop until the system performs well.

2.3.5 Some advanced feedforward designs

There are some advanced feedforward designs that can achieve a better performance theoretically. One of these designs is called dual-loop feedforward. In this design the main amplifier of the feedforward amplifier is another feedforward system, as shown below. There are two carrier cancellation loops and two distortion cancellation in the system. The performance of the dual-loop feedforward system should be better because of two feedforward loops. Figure 2 shows the advanced

structure:

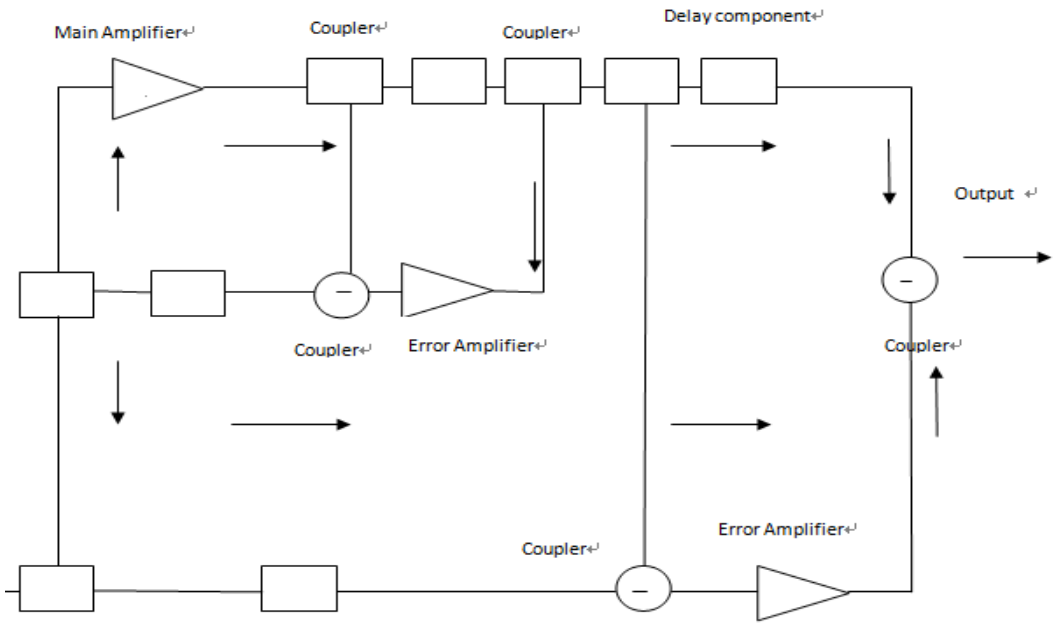

Figure 2. Advanced feedforward topology 1

Another advance feedforward loop introduces a feedback from the output of error amplifier to the input of the main amplifier. [6] This kind of method means to reduce the distortion part of output signal. The input of main amplifier equals to the difference of the main signal and the distortion part. The output distortion level is considerably less than the basic feedforward system. [6] Figure 3 shows the structure of this system

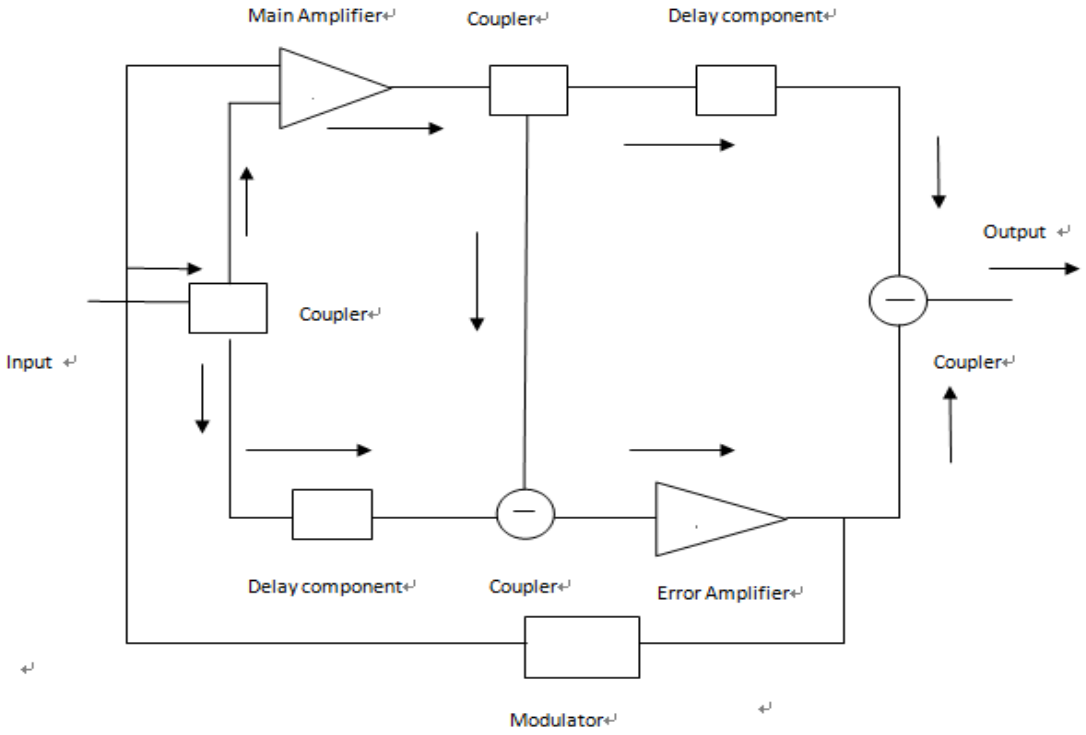

Figure 3. Advanced feedforward topology 2

2.4 The context of this project

As described above, the feedforward technology is mainly used as RF power amplifier as far as for now. And feedforward systems are focused on generate undistorted power. The idea of this project is try to use this concept in integrated CMOS design to build a computational block, focusing on analog signal transferring, and to use basic IC structures to design such a feedforward topology. This computational block aims to perform voltage to current transformation, without distortion. And the expected design should have a wide input range and output range, representing a good ability of tolerating distortion.

MOSFETs are nonlinear equipments, when work in triode mode, the characteristic formula is (length modulation effect is neglected here for convenience): [4]

$$i_D = \mu_n C_{ox} \frac{W}{L} [(v_{GS} - V_t)v_{DS} - \frac{1}{2} {v_{DS}}^2] \quad (1)$$

When work in saturation region, the characteristic formula is represented as:

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2 \quad (2)$$

The relationship between i_D and v_{GS} is not linear, thus results in a $i_D - v_{GS}$ characteristic graph shown as below:

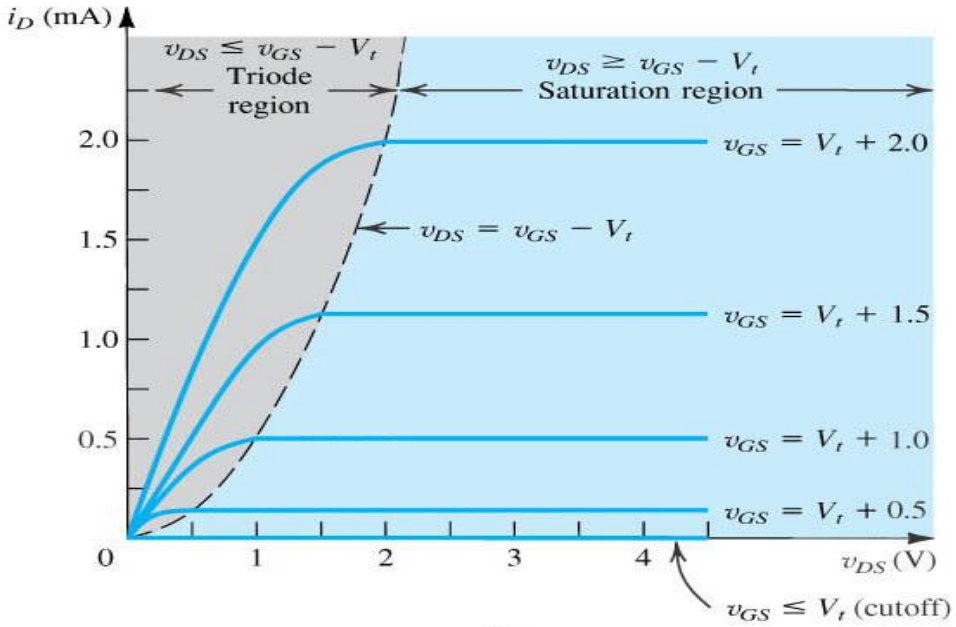

Figure 4. FET characteristic graph [4]

Usually, when MOSFETs are used as amplifiers, they work in saturation mode, and amplify a relatively small input signal to achieve linearity. Over a small region, the relation can be considered linear since the non-linear portion is very small compared to the amplified signal, as described in the load line $i_D - v_{GS}$ characteristics and transfer characteristics graph:

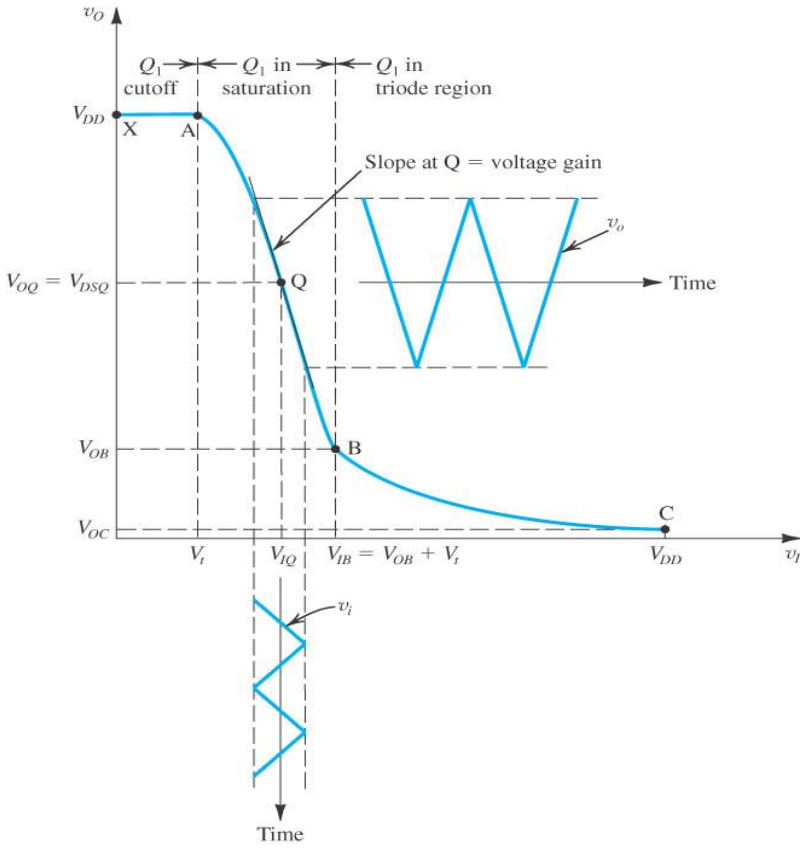

Figure 5. Transfer characteristic of FET [4]

But when fed with a large signal, a considerable distortion is introduced into the system. The load line crosses the saturation region and triode region. In saturation region, spaces between the $i_D - v_{DS}$ lines at a fixed interval of v_{GS} are not a fixed value. As inferred from the formula (1), relationship between i_D and v_{GS} is not linear. In cutoff region and triode region, distortion is very serious as can be seen from the transfer characteristic graph, when the signal swing reaches the cutoff region and triode region, the exceeding part of signal is almost cut off. Thus, when a large signal is introduced into the MOSFET amplifier, system meets a serious linear problem. The idea to fix this problem is to use feedforward technique.

The basic topology of this analog computation block should be similar with that used in RF power amplifier. Here is one different point that should be noticed, in a CMOS computation block, the delay component can be neglected because of the high speed , and possibly this block should be replaced by a function block aiming to transform the signal from one type to the other, i.e. , from current to voltage or from voltage to current. This question will be solved in the later chapters.

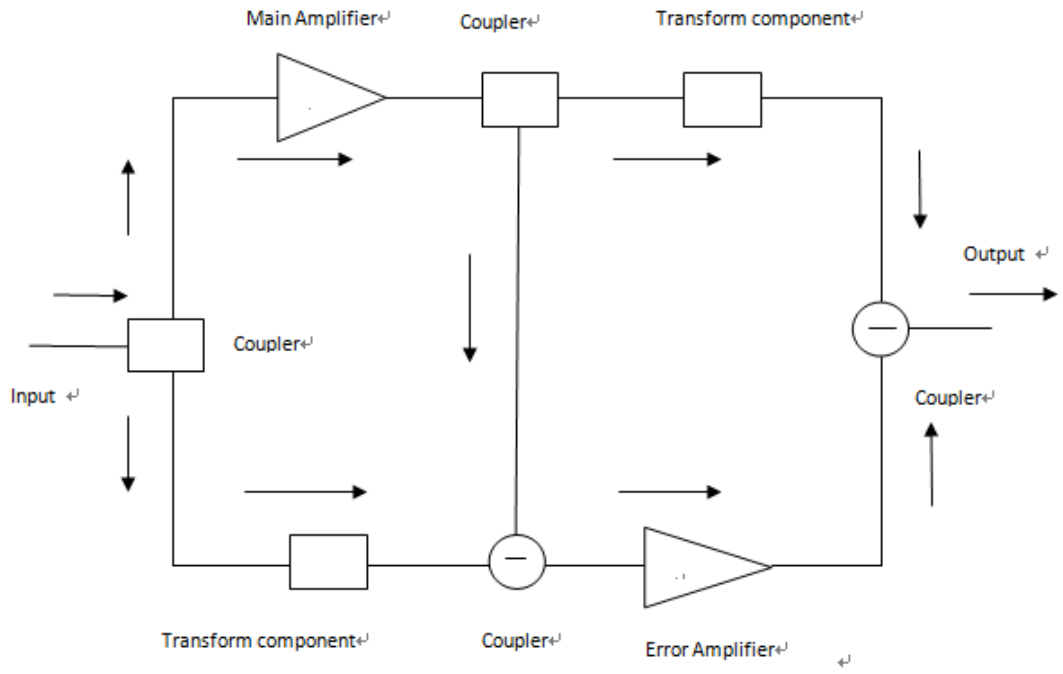

Figure 6. Feedforward topology in IC design

The output of this computation block should have no distortion .The system is expected to have the following features:

1. Large linear region
2. Wider transferring bandwidth

Chapter3. Feedforward Loop Implementation

3.1 Top level design

It's very important to study and to decide the signal format in every part of the whole topology, whether it is voltage or current. Because this has a great influence on the circuit performance and is the key point that determines the circuit elements. It determines whether a voltage controlled voltage source or a voltage controlled current source will be used, and whether current adder will be used or voltage adder will be used, etc.

3.1.1 Topology with voltage computational block

In general, there are two different methods to design the top level circuit. The first one is relatively easy to think of, which is to keep every output signal of circuit elements to be voltage, thus the signal don't have to be transformed to current, and that means transformation block is not needed in this design. To build up the whole circuit, we need voltage amplifiers, voltage adders and voltage subtractor, as shown below:

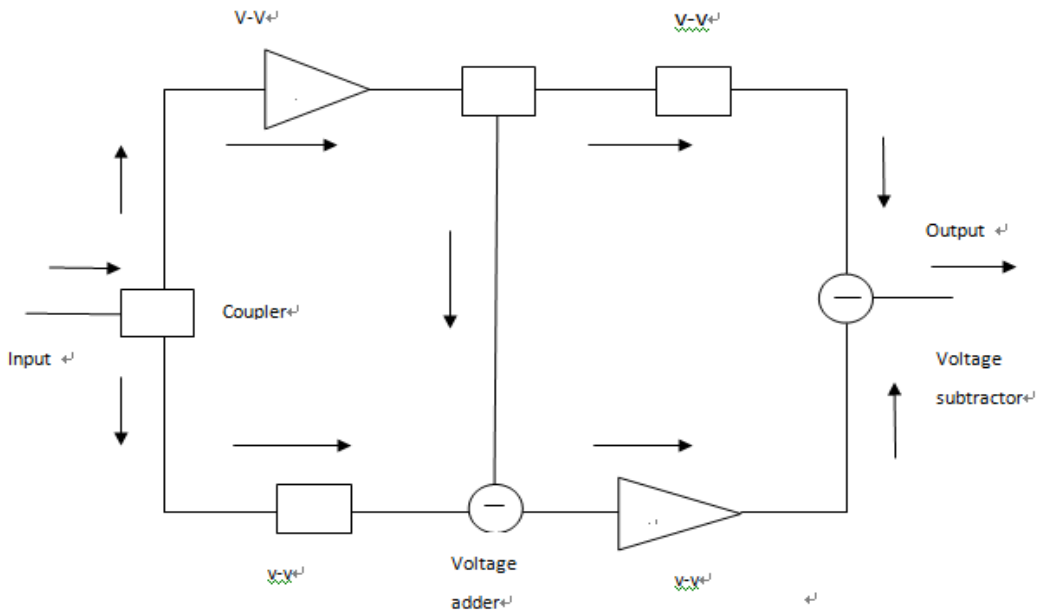

Figure 7. Voltage implementation of feedforward loop

In order to test the performance of this design, it is necessary to build up the circuit with ideal components, and run the simulation to see whether the result is what we expected.

Since the aim of this project is to design a large signal computation block, the input voltage range is wide, specified to be 0~1 v (top rail power supply is 1.25v), and the main amplifier should have a unit gain.

A polynomial voltage controlled voltage source can be used to model the main amplifier, with its poly coefficients set as: c0=-0.5, c1=1, c2=-0.1, this PVCVS has a 0.5 volts threshold voltage and the Vi-Vo characteristic line is a little curve as Vi becomes bigger, generating the distorted output voltage. Another PVCVS as well as a voltage subtractor is used to separate the distortion part by subtracting the distorted voltage from the original voltage, of course, this step will bring new distortion into the system, which is distortion part of the "distortion signal", that is because PVCVS is not linear, but this distortion has a much smaller scale compared to the first distortion. These two blocks are mentioned together because perfect linear voltage subtractor cannot be built without using feedback, PVCVS here is to describe the nonlinear characteristic of voltage subtractor. And a voltage adder has to be used as to add distortion part to the distorted signal to get a linear output. This can be achieved by using a voltage controlled voltage source. The circuit is shown below:

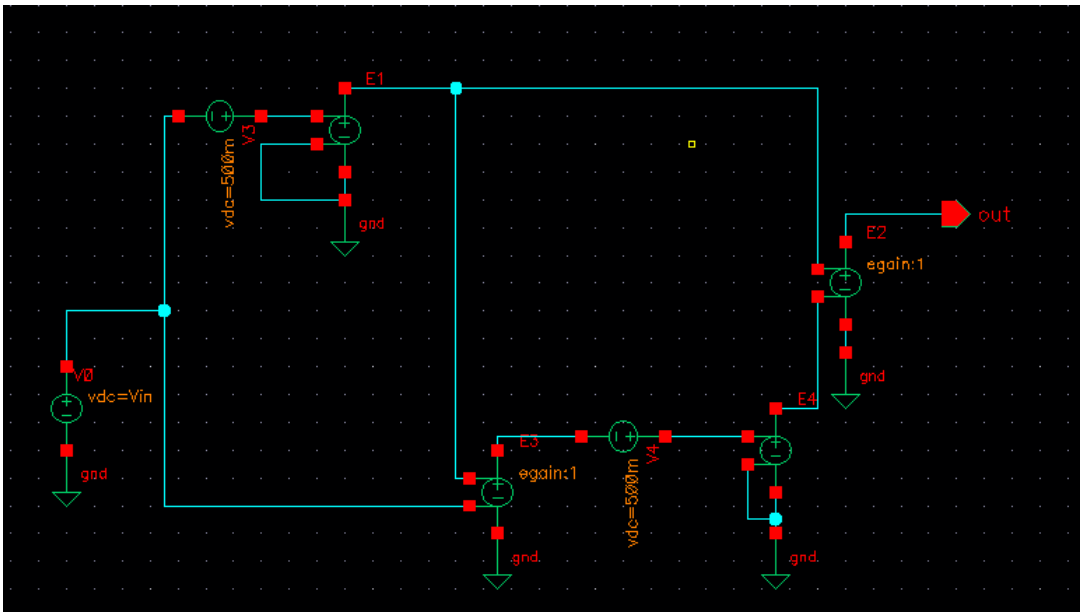

Figure 8. Voltage implementation using ideal components

The simulation result is shown below:

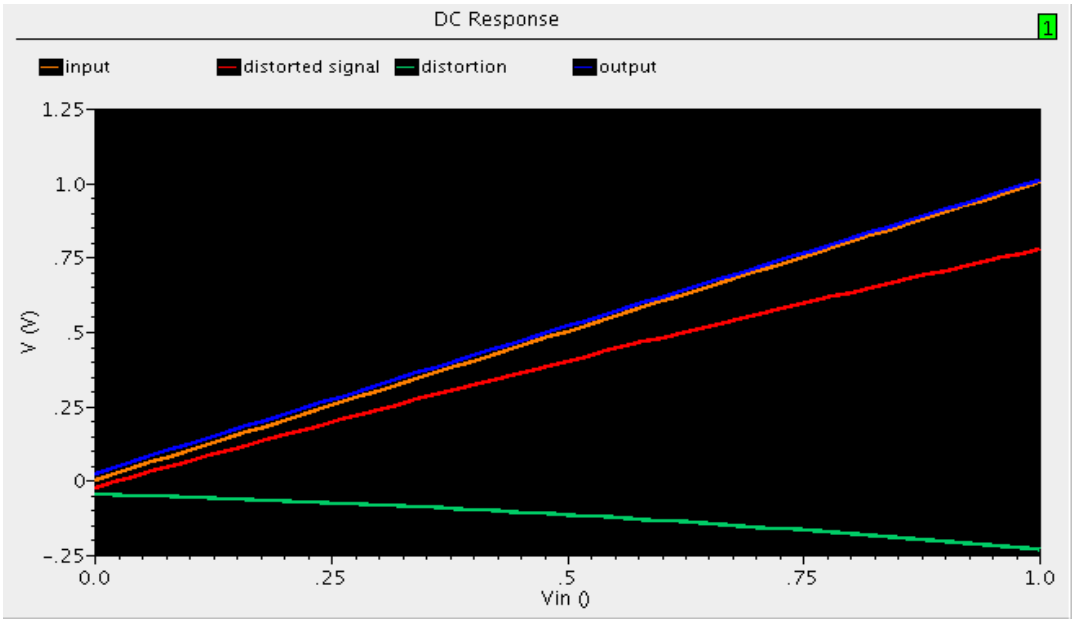

Figure 9.Simulation result of voltage implementation with ideal components

As shown in figure***, the red line represents the distorted signal while the green line shows the distortion part, they can be added up to form the blue line, which represents the output voltage, and that is quite linear and close to the input voltage. This circuit can achieve the expected result. But this design can be realized only if all the circuit elements can be implemented. Unfortunately, a perfect linear voltage adder at the end of the circuit is difficult to be designed without feedback under the wide input range circumstance. The voltage adder or subtractor we can build will have the same scale of distortion as the main amplifier. That means we eliminate the most distortion brought in by main amplifier, but will introduce new distortion into the system, and the new distortion is in the same scale as the old one. To identify this conclusion, the linear VCVS at the output node of the circuit is substituted by a nonlinear PVCVS. The new circuit is shown below:

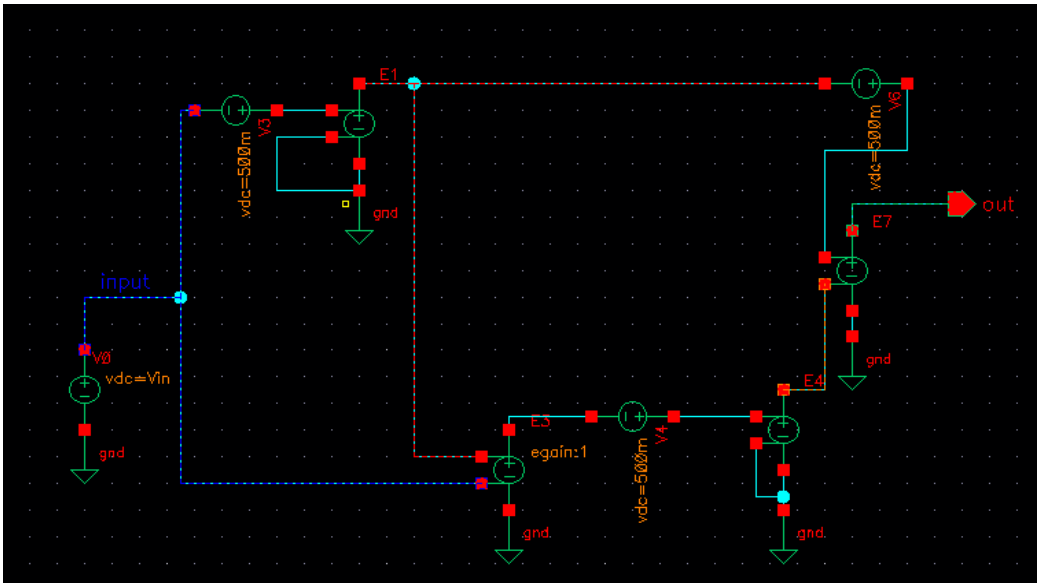

Figure 10. Modified voltage implementation with ideal components

And the simulation result is shown:

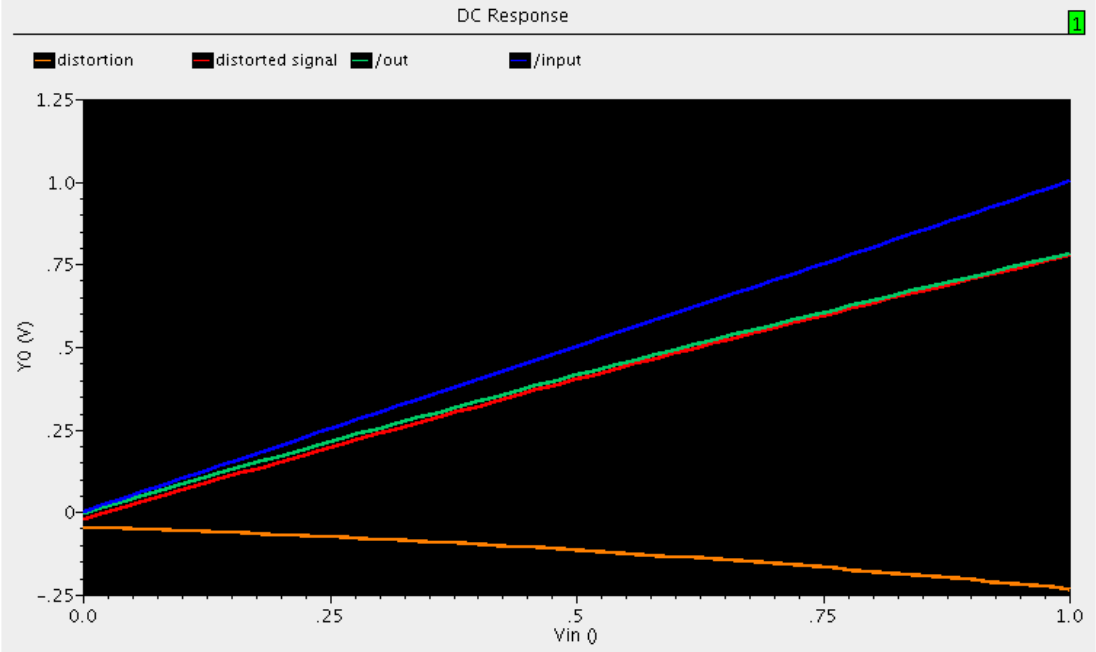

Figure 11.Simulation result of modified voltage implementation with ideal components

The final output signal is no better than the distorted signal, as we discussed earlier. Thus we move on to the second circuit design idea.

3.1.2 Topology with current computational block

Because it is relatively difficult to perform voltage addition and subtraction linearly, the second circuit design focus on doing the signal computation in the current mode, since current computation can be implemented perfectly using current mirrors. Thus in this design, signal transformation block is needed, and the format of signal in every step is important to design.

In the whole circuit, we need voltage controlled current source, current control voltage source, current adder and current subtractor.

To model the nonlinear voltage control current source, a polynomial voltage controlled current source is used with its coefficients set as: c0=0, c1=1, c2=-0.1, and a resistor is used as the simplest linear current control voltage source, current adder and current subtractor are built up by current mirrors. The circuit topology is shown below:

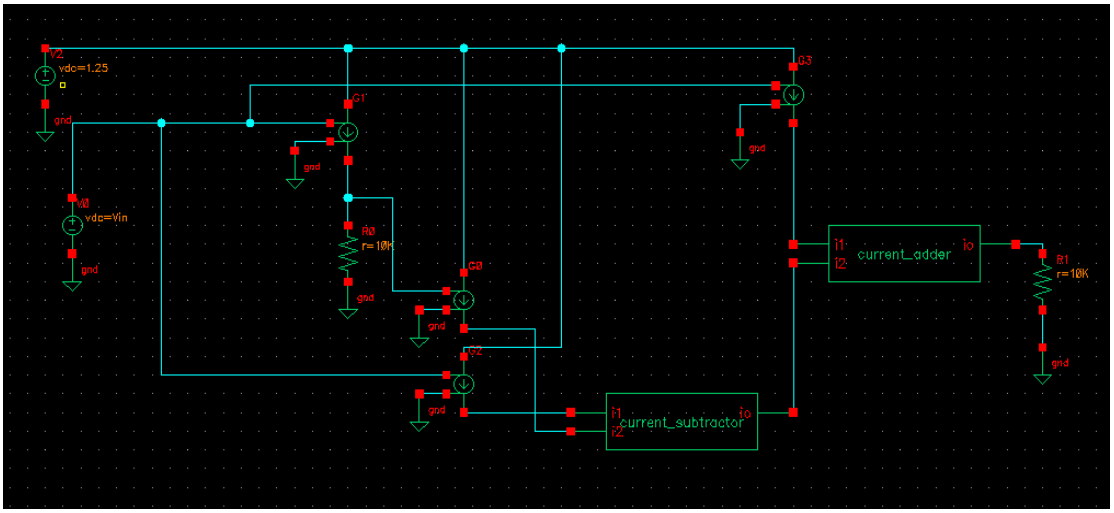

Figure 12. Current implementation with ideal components

As seen from figure12, this circuit is more complicate than the first design. In the first step, input voltage signal goes through a non linear voltage control currents source to produce a distorted current signal. To calculate the distortion part, this non linear current signal should be converted back to voltage signal through a linear current control voltage source, which is implemented as a single resistor, then both this distorted voltage signal and original voltage signal flow into the PVCCS to change their format to current mode, after this step, the difference between original signal and distorted signal can be calculated through a current subtractor, and thus, this distortion part can be eliminated by adding this distortion part to the distorted current signal by a current adder.

Of course, this method does not have the ability to generate a highly linear output because the PVCCSs which used to convert distorted voltage and original voltage are also non linear components, but even these components are not linear; a huge improvement can be achieved since the distortion part captured by the circuit is close to the real value.

This can be proved by a simple calculation, suppose the PVCCS has a transconductance as 1k, so when fed with 1V, the output should be 1mA, since it is non linear, the output current is 0.9mA, then this signal changes to voltage through a 1k resistor to make 0.9V voltage. Then the currents converted from the original voltage and distorted voltage should be 0.9mA and 0.83mA respectively, and then after some linear operation carried out by current adder and current subtractor, the final output current should be around 0.97mA, which is a better result compared to 0.9mA. The simulation result is shown as below,

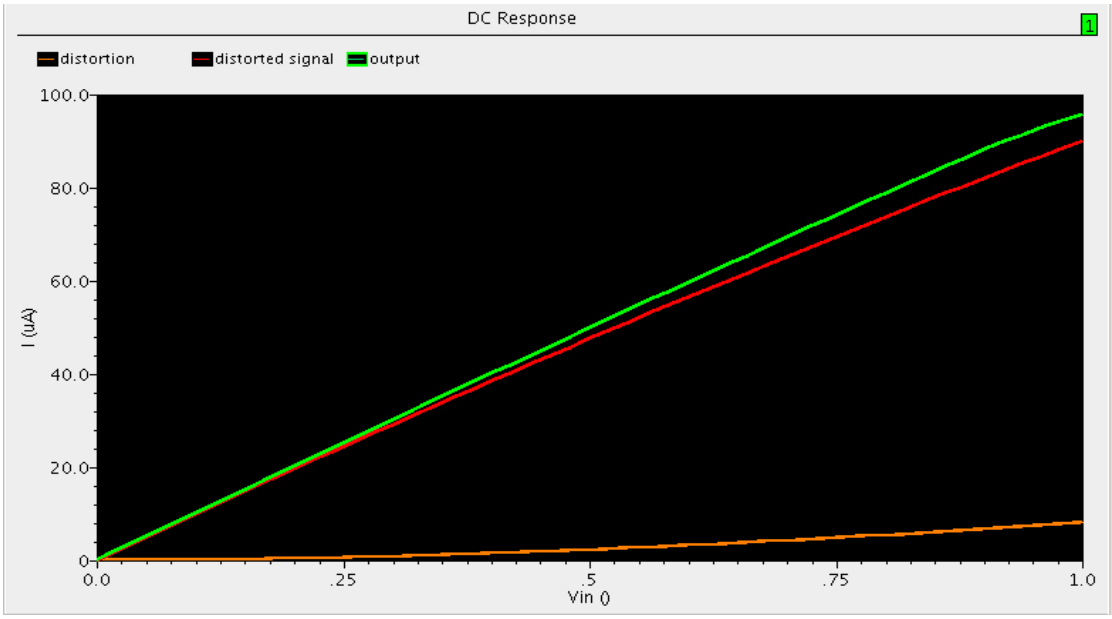

Figure 13. Simulation result 1 of current implementation

The green line represents output current, the red line represents distorted signal, and the yellow line represents the distortion part. As we can seen directly, the output signal equals to the sum of distortion signal and distorted signal, and it is more linear with a small scale of distortion in the high end. This distortion tolerance can be seen more clearly from the voltage comparison below,

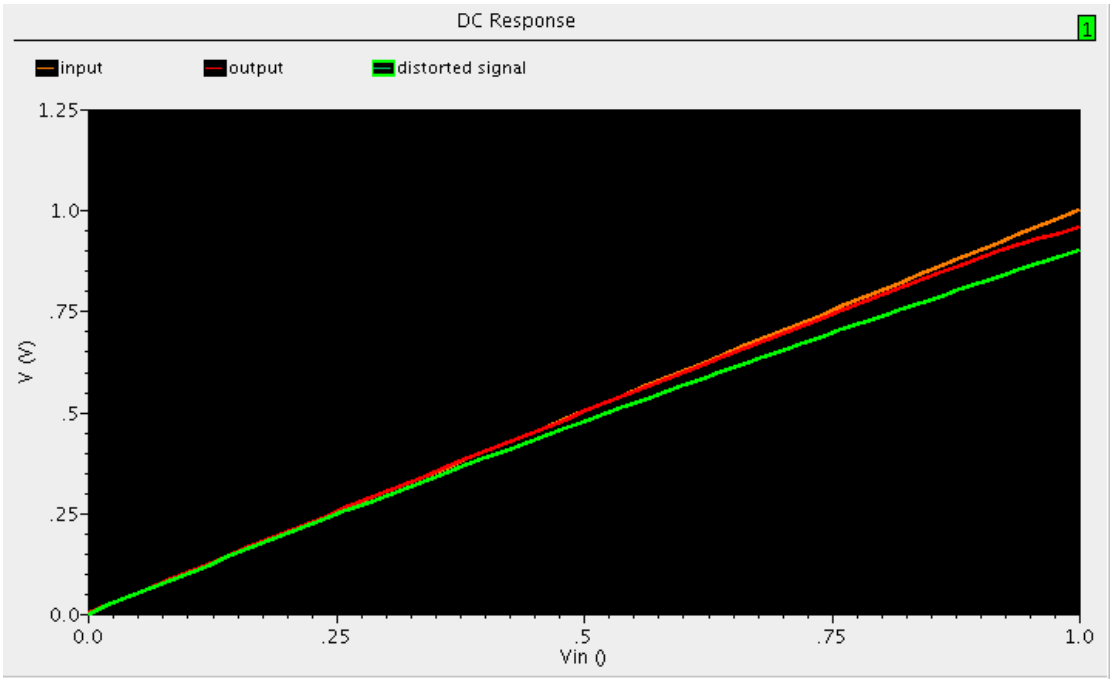

Figure 14. Simulation result 2 of current implementation

The red line shows a large improvement in linearity compared to the first output of VCCS, and all the functional units in this design can be achieved without feedback loop (except for the inner feedback loop of the current mirror, which has a very high operation bandwidth, it will not affect the design principles), thus suggest us a good idea to implement feedforward circuit.

3.2 Voltage controlled current source design

This circuit aims to transform the large input voltage to output current with distortion.

3.2.1 Design requirement

1. Wide range input voltage(0-500mV)
2. Wide range output current(0-200uA)
3. Non linear output
4. High input impedance
5. High output impedance
6. Function well over PVT variation

3.2.2 Basic principles and Design idea

The basic idea to build up the voltage control current source is to use a differential amplifier. This method can make a voltage mapping to current from zero easily, and the mapping is linear when the input is relatively small, and becomes non linear as the input grows.
Here is a simple differential amplifier,

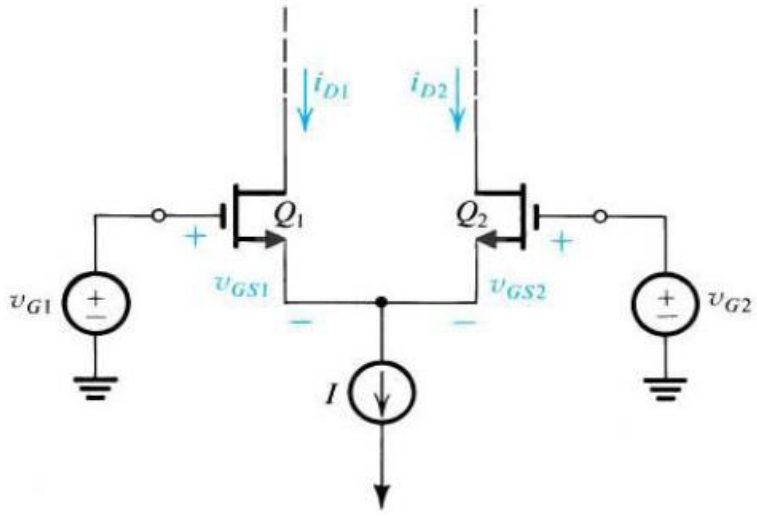

Figure 15. Differential pair[4]

The drain current of Q1 and Q2 can be expressed as

$$i_{D1} = \frac{1}{2} k_n \frac{W}{L} (v_{GS1} - V_t)^2$$
$$i_{D2} = \frac{1}{2} k_n \frac{W}{L} (v_{GS2} - V_t)^2$$

Taking the square roots of both sides of each equation above, we obtain

$$\sqrt{i_{D1}} = \sqrt{\frac{1}{2} k_n \frac{W}{L}} (v_{GS1} - V_t)$$
$$\sqrt{i_{D2}} = \sqrt{\frac{1}{2} k_n \frac{W}{L}} (v_{GS2} - V_t)$$

Subtracting the above two equations, and replace $v_{GS1} - V_{GS2}$ with V_{id} results in

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2} k_n \frac{W}{L}} v_{id}$$

The constant current bias impose the constraint

$$i_{D1} + i_{D2} = I$$

Use above two equations, $i_{D1}$and i_{D2}can be solved as

$$i_{D1} = \frac{I}{2} + \sqrt{k_n \frac{W}{L} I} \left(\frac{v_{id}}{2}\right) \sqrt{1 - \frac{\left(\frac{v_{id}}{2}\right)^2}{I \Big/ k_n \frac{W}{L}}}$$
$$i_{D2} = \frac{I}{2} - \sqrt{k_n \frac{W}{L} I} \left(\frac{v_{id}}{2}\right) \sqrt{1 - \frac{\left(\frac{v_{id}}{2}\right)^2}{I \Big/ k_n \frac{W}{L}}}$$

When V_{id} equals to zero,

$$i_{D1} = i_{D2} = \frac{I}{2}$$

These equations describe the effect of applying a differential input signal V_{id} on the current i_{D1} and i_{D2}. When V_{id} is small enough, i_{D1} and i_{D2} can be seen as linear. As V_{id} grows bigger, this relationship is not linear anymore, as shown in the figure below,

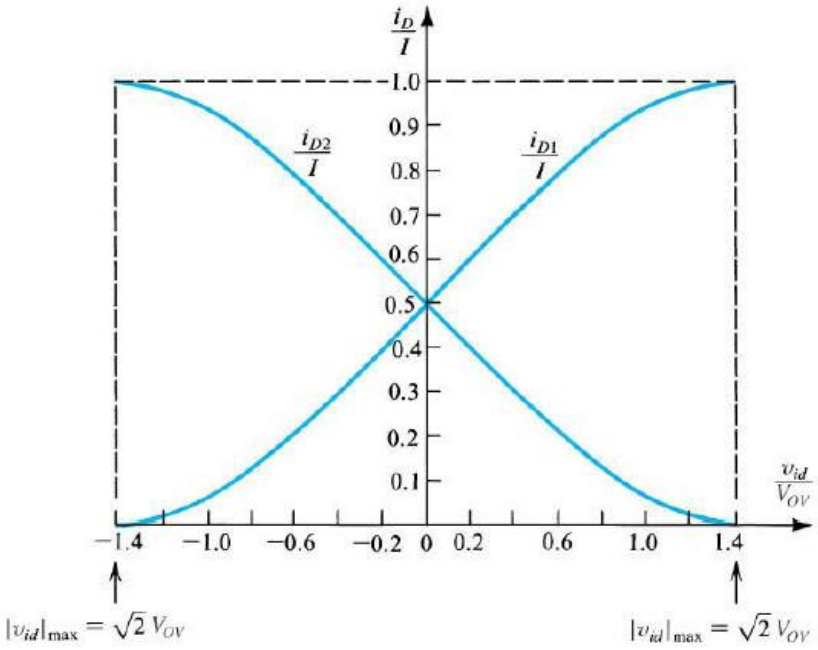

Figure 16.Nomarlised plots of the current in a MOSFET differential pair [4]

If the output current subtracts$\frac{I}{2}$, a voltage range from 0 to 1.4 is mapped to a current range from 0 to 0.5, and this is idea to build this voltage controlled current source.

3.2.3 Circuit implementation with basic function units

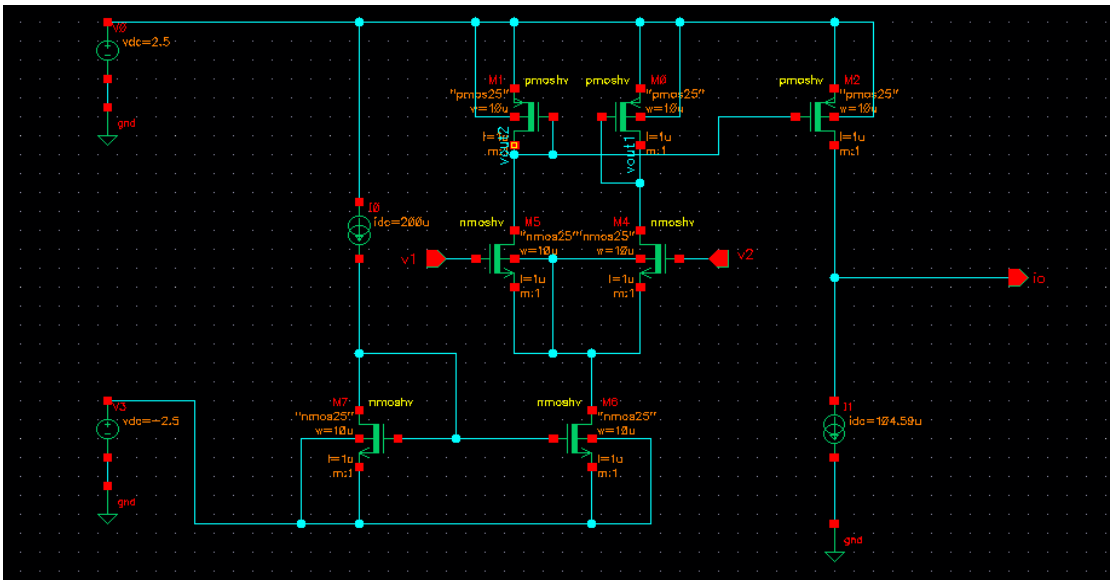

Figure 17. Simple implementation of VCCS

As shown above, the basic functional units in this circuit are different amplifiers, current mirrors, diode loaded transistors, voltage sources and current sources.

A current mirror is used to copy the M1 drain current to M2 drain current, and this current subtract $\frac{I}{2}$ provided by another current course, and the subtraction result forms the output current.

Circuit built up by these basic functional units only shows a way to establish the relationship between input voltage and output current, but still don not performs well. The output impedance is not very large, the current mirror cannot copy current with enough accuracy, and the input voltage swing is limited by small voltage headroom. These problems need to be solved with some more complicated functional units.

3.2.4 Cascode current mirror and Wide swing current mirror

1. Cascode current mirror

To improve the characteristic of current mirrors, cascode current mirror is used. The output impedance of cascode current mirror is

$$R_o = r_{o3} + [1 + (g_{m3} + g_{mb3})r_{o3}]r_{o2} \approx g_{m3}r_{o3}r_{o2}$$

The output impedance is raised by a factor of $g_{m3}r_{o3}$ compared to simple current mirror. Thus the output current will not be sensitive to the voltage at drain node of Q3, as long as Q3 works in saturation region. Cascode has better current copy ability with high accuracy, but it brings some disadvantage because of the cascode current mirror. It consumes relatively large portion of the power supply voltage. While the simple MOS mirror operates properly with a voltage as low as V_{ov} across its output transistor, the cascode circuit requires a minimum voltage of $V_t + 2V_{ov}$.[4]

That is a bad news for the situation where rail to rail power supply is limited to a small range and a wide voltage swing have to achieve in the circuit. The voltage headroom has to be calculated carefully and use another advanced approach for accurate current mirror.

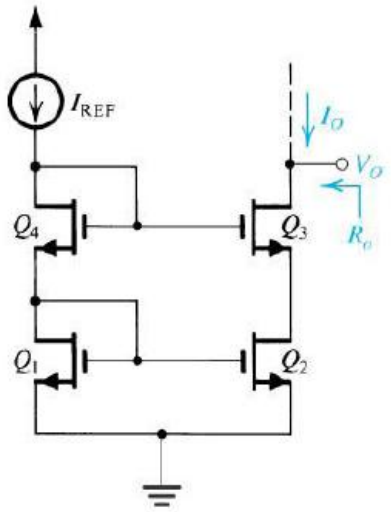

Figure 18. Cascode current mirror[4]

2. Wide swing current mirror

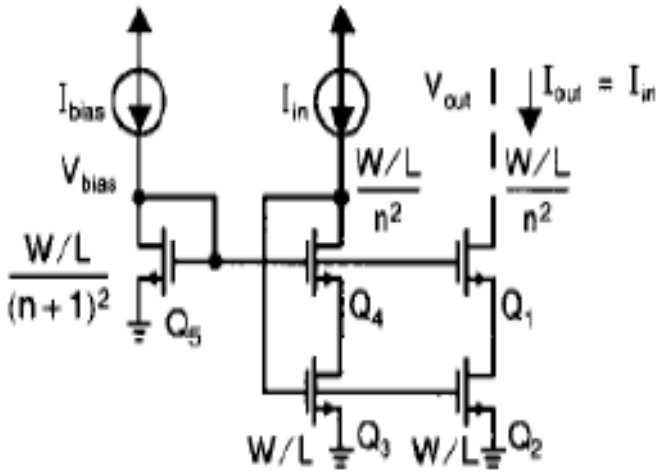

Figure 19. Wide swing current mirror[2]

As shown above, the basic idea of this current mirror is to bias the drain-source voltages of transistors Q2 and Q3 to be close to the minimum possible without them going into the triode region. If the sizes shown in figure 19 are used, Q2 and Q3 will be biased right at the edge of the triode region.

To determine the bias voltage for the circuit, let V_{OV} be effective gate source voltage of Q2 and Q3, and assume all of the drain currents are equal. Thus, we get,

$$V_{OV} = V_{OV2} = V_{OV3} = \sqrt{\frac{2I_{D2}}{u_n C_{OX}(W/L)}}$$

Furthermore, since Q5 has the same drain current but is $(n+1)^2$ times smaller, we have,

$$v_{OV5} = (n+1)V_{OV}$$

Similar reasoning results in the effective gate-source voltages of Q1 and Q4 being given by,

$$v_{OV1} = V_{OV4} = nV_{OV}$$

Thus,

$$V_{G5} = V_{G4} = V_{G1} = (n+1)V_{OV} + V_t$$

Furthermore,

$$V_{DS2} = V_{DS3} = V_{G5} - V_{GS1} = V_{G5} - (nV_{OV} + V_t) = V_{OV}$$

This drain-source voltage puts both Q2 and Q3 right at the edge of the triode region. Thus, the minimum allowable output voltage is now

$$V_{out} > v_{OV1} + v_{OV2} = (n+1)v_{OV}$$

A common choice for **n** might be simply unity, in which case the current mirror operates correctly as long as

$$V_{out} > 2v_{OV}$$

With a typical value of v_{OV} between 0.2V and 0.25V, the wide swing current mirror can guarantee that all of all the transistors in active region even when the voltage drop across the mirror is as small as 0.4V and 0.5V.

Another requirement that must be satisfied to ensure that all transistors are in the saturation region is

$$v_{DS4} > V_{OV4} = nV_{OV}$$

to guarantee that Q4 is in the saturation region. We also have

$$V_{DS4} = V_{G3} - V_{DS3} = (V_{OV} + V_t) - V_{OV} = V_t$$

Thus we only need ensure that V_t is greater than nV_{OV} for Q4 to remain in saturation, which is not a difficult problem.

Since the input current may vary over a certain range, the bias current should be set as the maximum value of the input current to make sure all the transistor works in saturation in all the situations, though the drain source voltage of Q2 and Q3 will be larger than necessary except when largest current is applied. As a result, some voltage swing will be lost.[2]

In the real applications, the dimension of Q5 is set a little smaller than the calculation result to bias Q2 and Q3 with slightly larger drain-source voltage than minimum required. Because the fact that practical transistors do not have a sharp transition between the triode and active region.

Figures below show a wide swing current mirror schematic to test the output voltage swing and the simulation result,

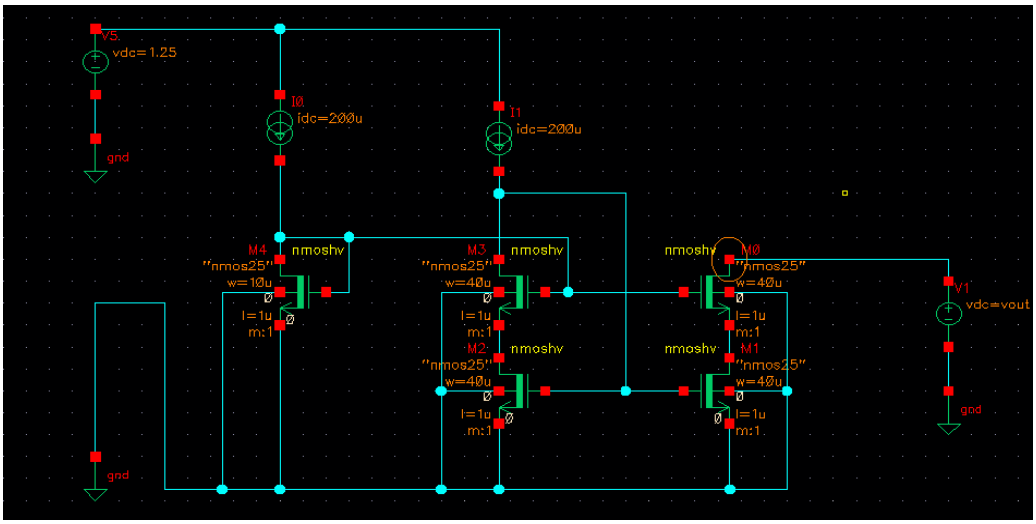

Figure 20. Schematic of wide swing current mirror

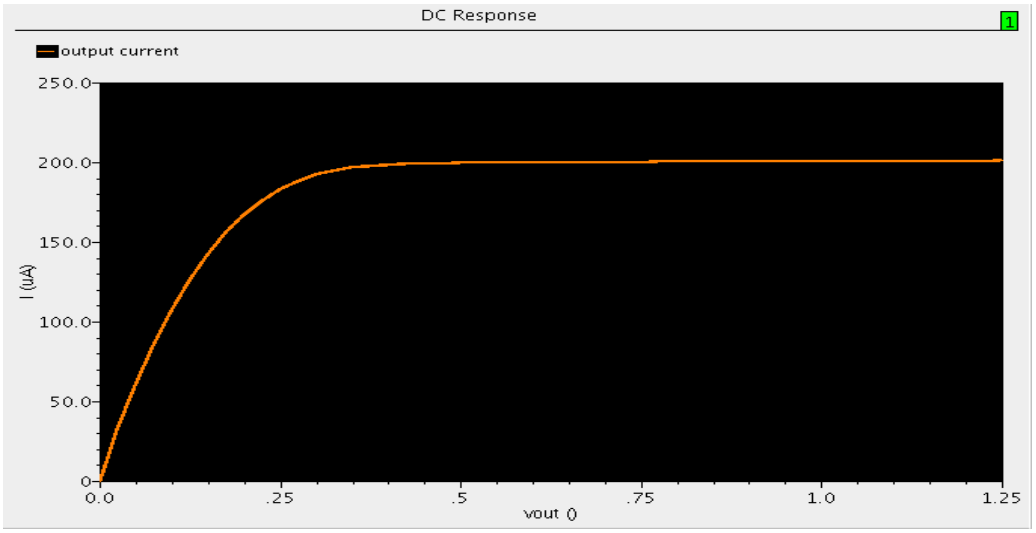

Figure 21.Performance of wide swing current mirror when fed with varying output voltage

As can be seen from the picture, when the output voltage reaches around 0.4V the current mirror works in saturation region and has a good performance. The output current keeps quite stable when the current mirror goes into saturation region. That is due to the large output impedance.

This current mirror will be applied in VCCS design where needs a wide swing output voltage range as well as high output impedance.

3.2.5 Transistor dimension sizing considerations

1. Wide input voltage range

According to the design requirement, this VCCS should have a minimum input voltage range from 0 to 0.5V. The differential amplifier $i_D - v_{GS}$ characteristic is shown,

$$i_D = \frac{I}{2} \pm \sqrt{k_n \frac{W}{L}} I\left(\frac{v_{id}}{2}\right) \sqrt{1 - \frac{\left(\frac{v_{id}}{2}\right)^2}{I \Big/ k_n \frac{W}{L}}}$$

From this equation we can make a conclusion that if we want to expand the input voltage range at the same time to keep the drain current varying over same range, $\frac{W}{L}$ should be changed to a smaller value.

2. High accuracy current mirrors

Current mirrors behave more accurate as the output impedance grows, because this will make the output current not sensitive to the output voltage swing. Thus one consideration to determine the transistor dimension is to make relatively large impedance at the output node of current mirrors

The output resistance of MOSFET in saturation region is

$$r_o = \frac{1}{\lambda I_D} = \frac{L}{\lambda' I_D}$$

Where λ' is a process-technology parameter, thus for a fixed drain current, a longer transistor has a larger output impedance.

And current mirror should always works in saturation region, and that requires a

sufficient drain-source voltage,

$$V_{DS} > V_{GS} - V_t$$

Thus current mirror with smaller V_{GS} tends to have a better performance to work in a low output voltage supply environment,

$$i_D = \frac{1}{2} k_n \frac{W}{L} (v_{GS} - V_t)^2$$

As seen from the above equation, for a fixed drain current, transistors with larger $\frac{W}{L}$ has a smaller v_{GS}.

3. Wide voltage swing

The rail to rail power supply is a fixed value, in order to satisfy a differential MOSFET pair's v_{DS} variation, current mirrors output voltage requirement, and an active loaded voltage consuming, all transistor dimension should be carefully determined to make sure that there is enough voltage headroom to accommodate all the functional blocks. The method to keep every transistor works in saturation region is to make them have a relatively small v_{GS}, and that means all the transistors except for the differential pair tend to have a small $\frac{W}{L}$ to maintain working in saturation. For the differential amplifier, $\frac{W}{L}$should not be too small to go into triode region and should not be too large to shrink the voltage swing.

4. Performance under PVT variation

Circuit should function well under PVT variation. That means all the transistor should work in saturation region in all corners.

The voltage supply varies $\pm$10% under PVT. Thus the circuit meets a challenge when rail to rail supply voltage shrinks by 10%. There must be enough voltage headroom to ensure all the components work well in this corner. The method to tolerate supply voltage variation is to resize all the transistors to make sure they function well under the worst situation.

3.2.6 Final circuits and simulation results

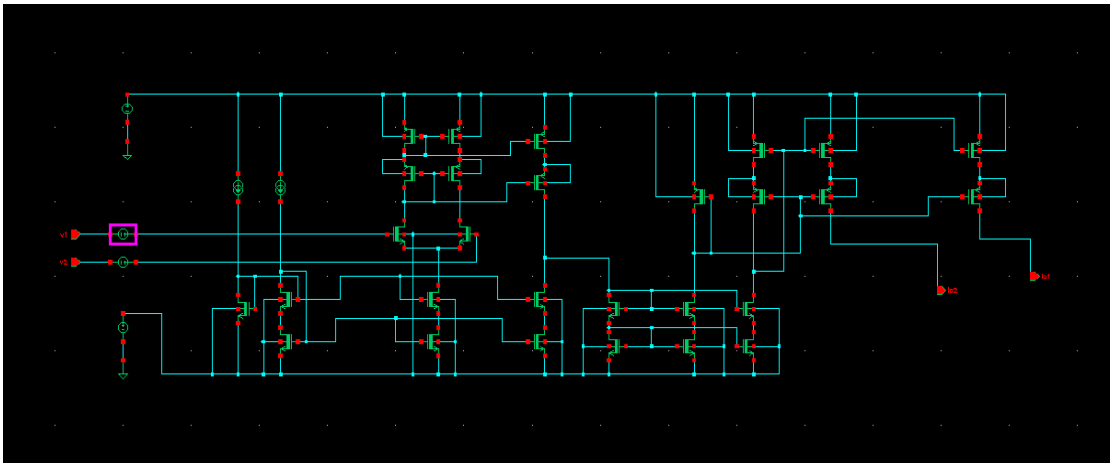

Figure 22. Final schematic of VCCS

1. Some important features

1.
Dimension of differential pair is set to be W=8u, L=1u to allow a wide swing input voltage.

2.
Wide swing current mirror is used to provide a current bias to the differential amplifier. Since when the input voltage is zero, equal currents flow through both differential transistors, thus

$$v_{GS} = V_t + V_{ov} \approx 1.0V$$

And

$$v_G = 0V$$

Makes

$$v_S = v_G - v_{GS} = -1.0V$$

The bottom rail power supply under worst voltage corner is

$$\text{-}1.25V * 0.9 = -1.125V$$

Thus $-1.0V - (-1.125V) = 0.125V$ headroom is left for the current mirror, then wide swing current mirror is the best choice here to provide a accurate current copy and do not need high output voltage.

An improvement can be made here to add bias voltage to both of the input of the differential amplifier. By doing this, a larger voltage headroom can be produced for the current mirror to work in the saturation mode. The bias voltage is set to be 0.6V; thus, the minimum drain voltage of differential amplifier can be calculated as,

$$v_D = v_G - v_{GD} = 0.5V - 0.6V = -0.1V$$

The voltage headroom for the active loaded current mirrors in the worst case is,

$$V_+ * 0.9 - (-0.1) = 1.225V$$

This is still enough to accommodate a cascode current mirror.

Thus the voltage headroom for the wide swing current mirror becomes

$$0.125V + 0.5V = 0.625V$$

This value is larger than that needed by a wide swing current mirror, which is around 0.3V theoretically. But it is helpful to provide bigger voltage headroom, since this can make the wide swing current mirror work in a deeper saturation region and have a better performance according to the simulation result.

As discussed above the, the dimensions of transistors of wide swing current mirrors equal to $\frac{W}{L(n+1)^2}$, $\frac{W}{Ln^2}$,$\frac{W}{L}$, respectively. The parameter n is set to be unit in this design, thus the dimensions become $\frac{W}{4L}$, $\frac{W}{L}$,$\frac{W}{L}$.

The dimension of bias setting transistor is set as: W= 18u, L=200n, a shorter width is chosen to keep current mirrors works in a slightly deeper saturation region to achieve linear mapping.

The dimensions of other 4 transistors are as: W=80u, L=200n

3.
Wide swing current mirror is also used in the output node to provide high output impedance and wider voltage variation.

The dimension is the same as the bias current mirror.

4.
A wide swing current mirror is used to get half value of current source, with a dimension: W=42u, L=200n, which is supposed to be, W=40u, L=200n by theoretically calculation. This slightly justification will compensate for some offset

caused by output voltage swing, to ensure that the output current varies from 0 to 100uA. This is shown in the figure below:

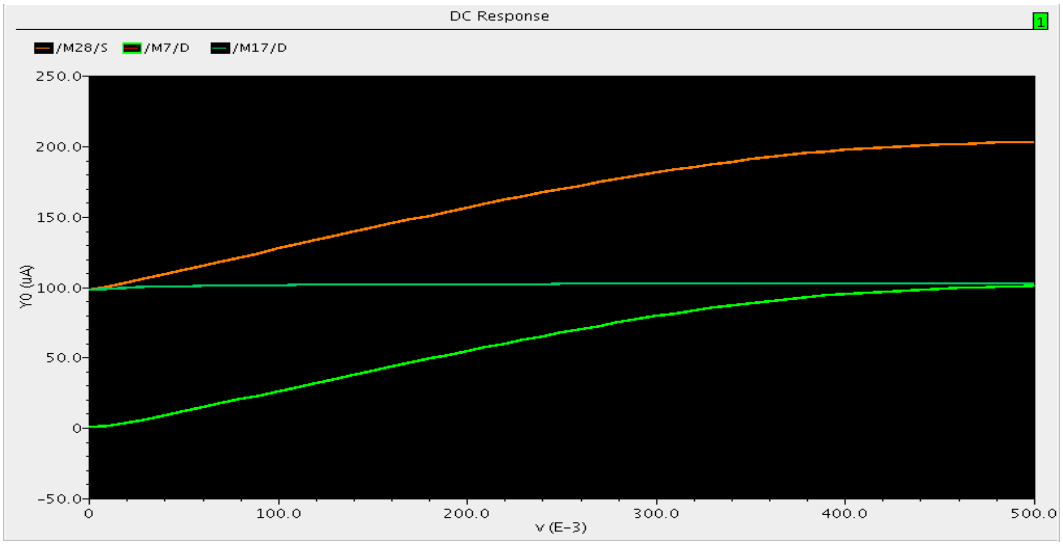

Figure 23. Expected current obtained by subtraction

5.

Cascode current mirror is used as the active load to provide high output impedance and an accurate copying of the drain current. Since the maximum input voltage is 0.5V, the maximum drain voltage of differential pair is

$$0.5 + 0.5 - \mathrm{V_t} \approx 0.4\mathrm{v}$$

For the worst case of voltage variation, voltage headroom for the active load is

$$1.25\mathrm{V} * 0.9 - (0.4) = 0.7125\mathrm{V}$$

Thus cascode current mirror can meet the design requirement, and just work in the saturation region in the worst case.

The dimension of transistors in the cascode current mirror is: W=40u, L=200n, $\frac{\mathrm{W}}{\mathrm{L}}$ is large to keep all the transistors works in the saturation region.

6.

Cascode current mirror is used to double the output current, as a result, this current will range from 0 to 200 uA.

2. Simulation result

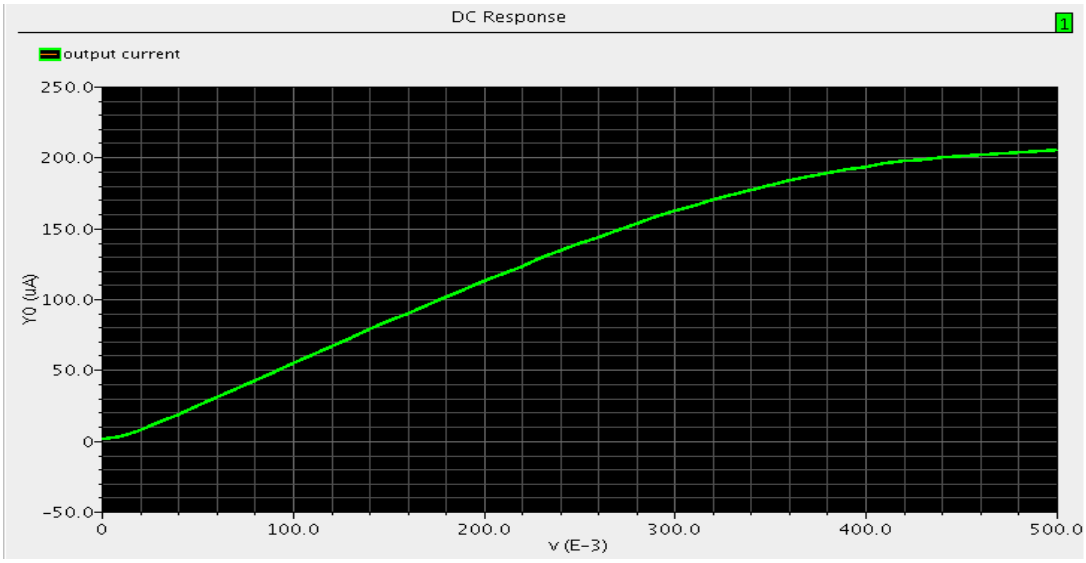

Figure 24. Output current of VCCS

The figure shows the output current, as we can seen from the picture, the current is linear and when the voltage is relatively low, and becomes distorted as input voltage grows bigger.

It can be measured from the linear part of transmission line that the transconductance is $\frac{1}{1{,}9\text{k}}$, thus when connected the output current to a 1.9k resistor, a distorted voltage signal is formed and the comparison with the input voltage is more clear to identify,

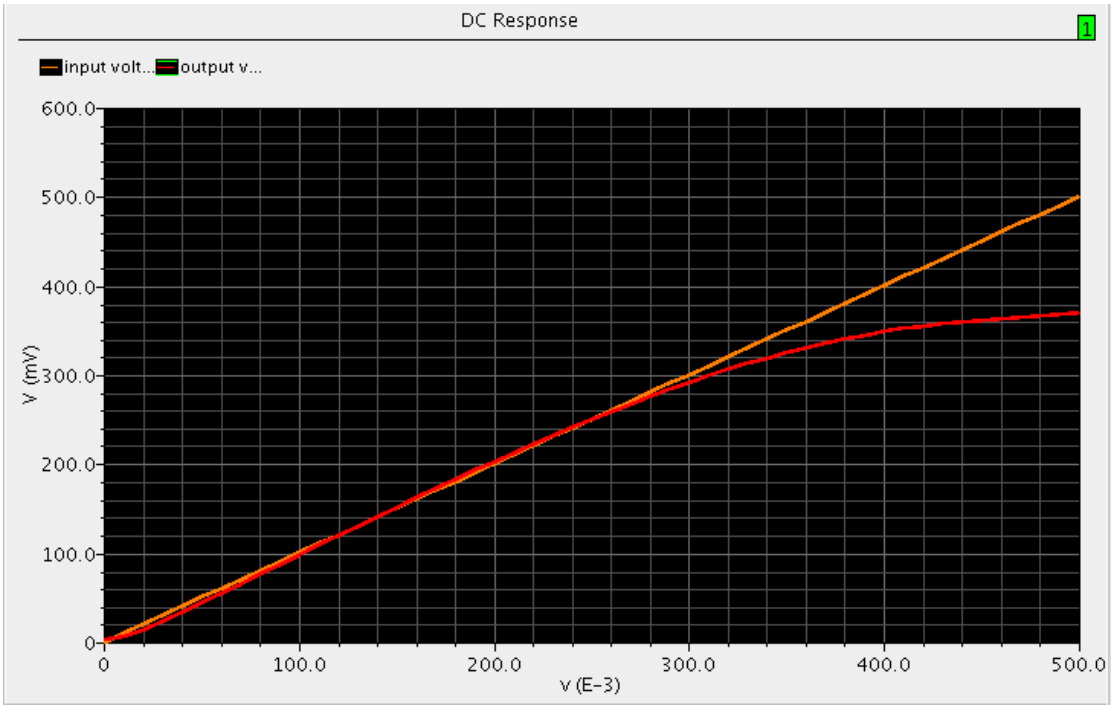

Figure 25. Comparison between input and output

3.3 Current adder design

3.3.1 Design requirement

1. Linear operation
2. High output resistance
3. Function well over a large range input current (0-200uA)

3.3.2 Basic principle and design idea

The current adder is based on the current mirror technique. Two current mirrors are fed with different currents, and the output node of these two current mirror is connected together to perform the current addition. The basic circuit topology is shown below:

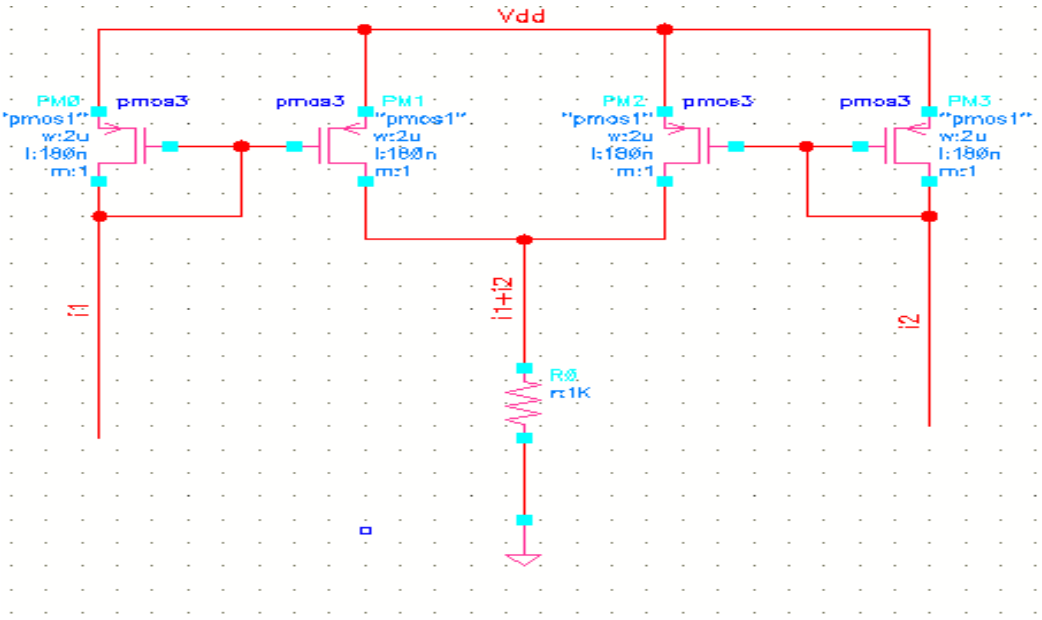

Figure 26. Simple current adder

3.3.3 Wide swing current mirror implementation

The figure below shows the circuit topology of the current adder,

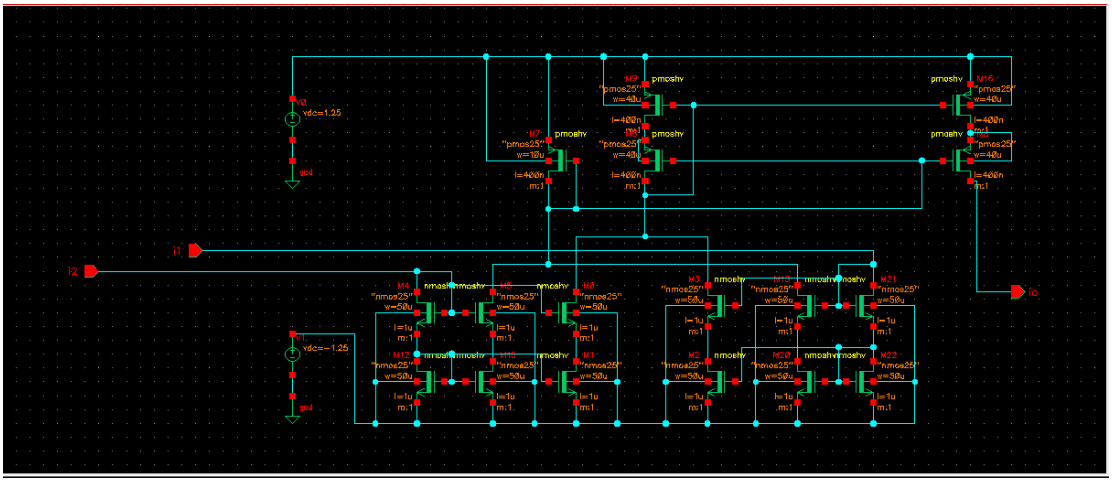

Figure 27. Final schematic of current adder

1. Wide swing current mirror is used as the output stage to provide a large output impedance as well as wide output voltage swing.

2. Cascode current mirror are used as the input stage to improve the current performance by raise the output impedance. And cascode current mirror provide the bias current for the wide swing current mirror.

3.3.4 Transistor dimension sizing

As the input current range is wide, specifically from 0 to 200uA, and cascode current mirrors are used, which do not have large output voltage range; the transistors should have a large $\frac{W}{L}$ ratio to keep every transistor works in saturation.

The dimensions of transistors in cascode current mirrors are set as, W=50u, L=1u

The parameter **n** wide swing current mirror is set to be unit

The dimensions of transistors in wide swing current mirrors are set as, W=9u, L=400n

W=40u, L=400n, W=400u, L=400n, respectively.

3.3.5 Simulation result

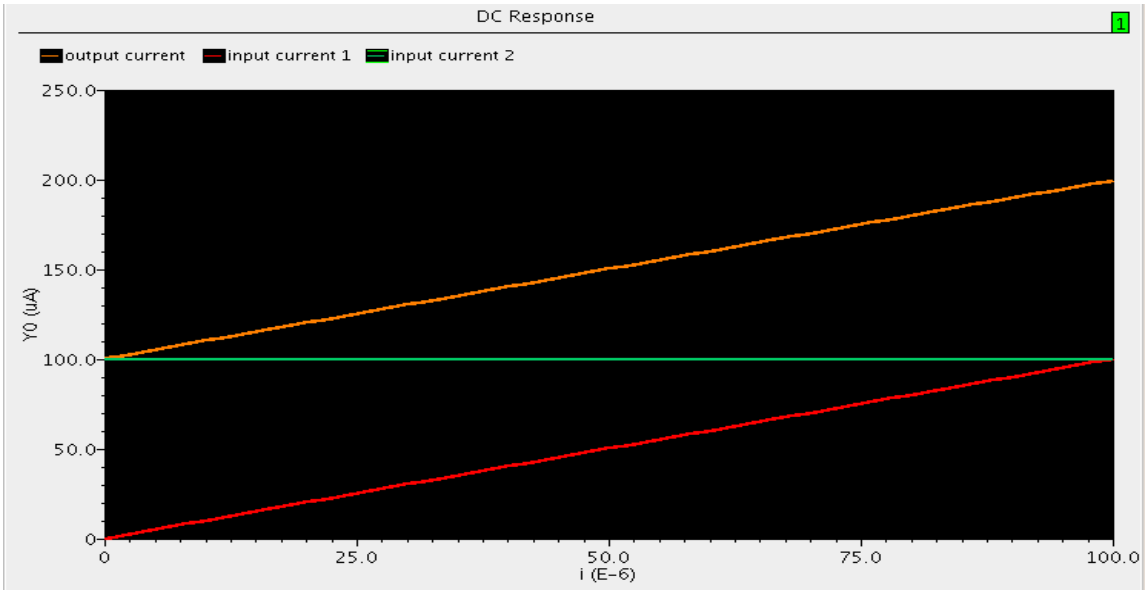

Figure 28. Simulation result of current adder

This current adder is fed with 2 currents; one is fixed at 100uA, the other ranges from 0 to 100uA. The output node is connected to a 3.8k resistor to see whether the current adder has such an ability to drive this load.

As can seen from the picture above, the output current has a perfect linear characteristic and ranges from 100uA to 200uA, as expected.

3.4 Current subtractor design

3.4.1 Design requirement

1. Linear operation

2. High output resistance

3. Function well over a large range input current (0-200uA)

3.4.2 Design idea and circuit topology

Current subtractor also based on the current mirror technique. The mechanism is similar to the current adder; the difference is how to combine these two input current mirrors together to perform certain logic.

The figure below shows the topology of current subtractor,

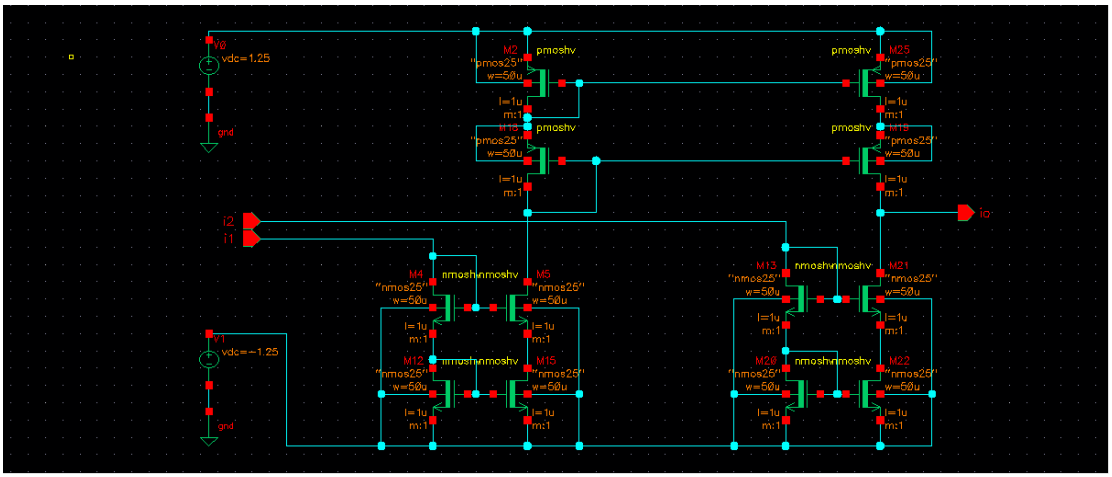

Figure 29. Final schematic of current subtractor

Three cascode current mirrors are used to perform the function. Wide swing current mirror is not applied in this design, because in the overall topology, the output of current subtractor is connected to the input stage of current adder, which can varies over a large range. Thus it is not necessary to use wide swing current mirror here.

3.4.3 Transistor dimension sizing

The dimensions of all transistors are set to be W=50u, L=1u, in order to ensure all the transistor works in saturation region.

3.4.4 Simulation result

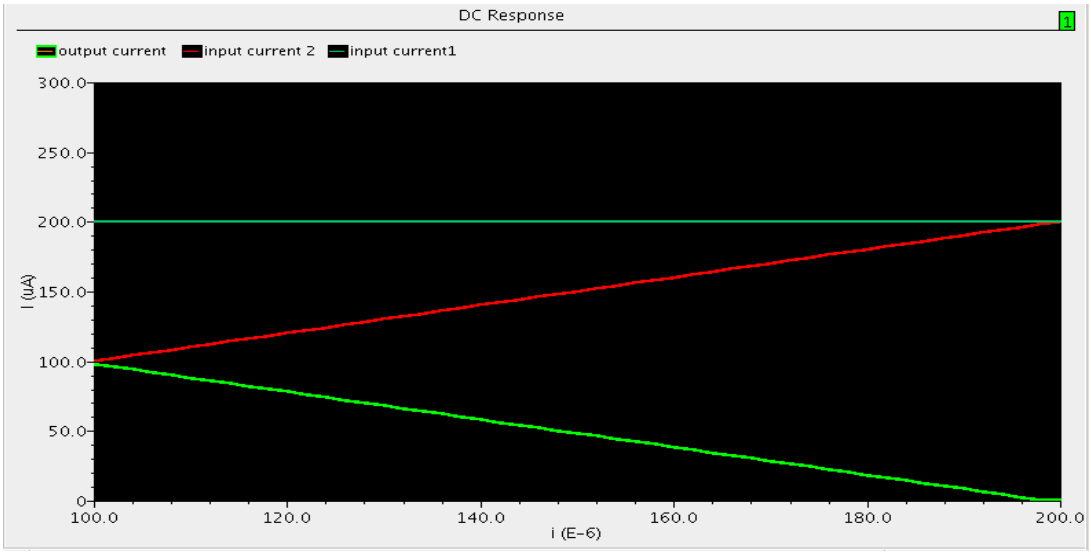

Figure 30. Simulation result of current subtractor

Before simulation, the output node of this current subtractor is connected to the

input stage of current adder to test how this current subtractor behaves in the real circuit connection.

As we can see from the figure above, this current subtractor has a quite linear performance.

3.5 Current controlled voltage source design

This circuit aims to build a linear conversion functional block to transform current to voltage.

3.5.1 Design requirement

1. Linear relationship between input current and output voltage

2. Low output resistance

3.5.2 Circuit implementation

A single resistor here is used as a CCVS to convert current to voltage. The transfer characteristic is quite linear by a fixed transconductance which determined by the resistor.

Since in the overall topology, the output of CCVS is connected to the input stage of VCCS, which has an infinite input resistance, the output resistance of CCVS can be seen as quite low.

This implementation suffers from some drawback under PVT variation, since the resistor value will change 20% percent in the temperature corners; the transconductance will also varies with the resistor value, and cannot be controlled precisely. Furthermore works need to be carried out to find a noble way to build up the current control voltage source which has a fixed and accurate transconductance under different PVT corners.

3.6 Voltage divider design

The input range of VCCS is designed to be 0-0.5V, which still does not satisfy design requirement (0-1V).There is one method to solve this problem, which is to make the input voltage shrink first before it flows into VCCS. Thus a voltage divider is needed in the overall circuit.

To design a simple voltage divider, two resistors of same value will achieve the

expected result easily; the circuit is shown below,

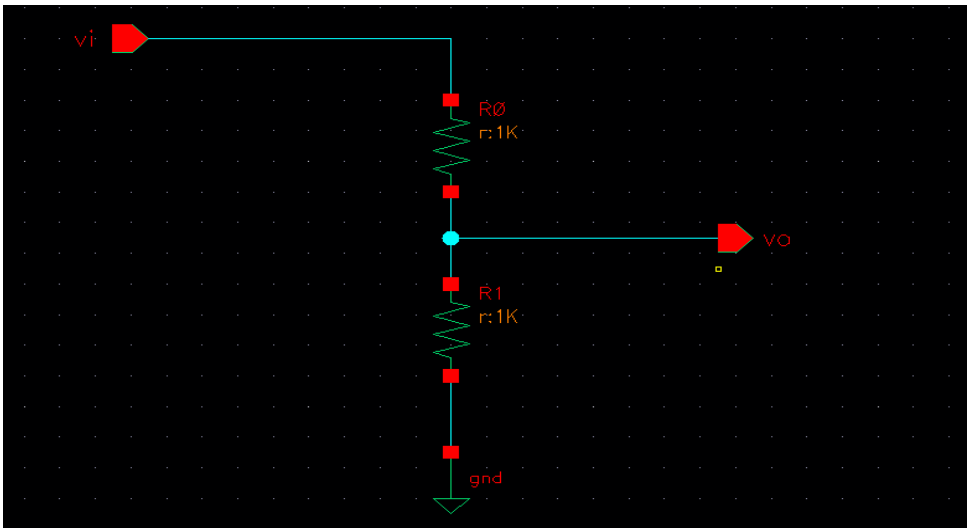

Figure 31. Schematic of voltage divider

Simulation result is shown,

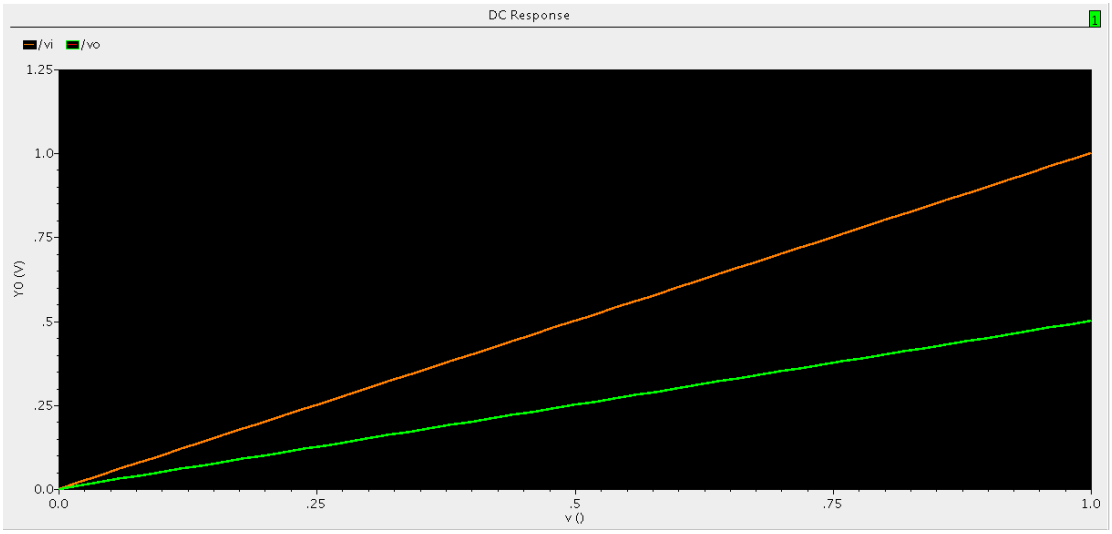

Figure 32. Simulation result of voltage divider

As seen from Figure32,when input voltage varies over the range 0 ∽ 1V, the output voltage is exactly half of the input voltage.

This design has a good performance over PVT variation since temperature changing or process changing will have the same effect on the both resistors, and the changing on each resistor will balance each other. Thus, output voltage has a perfect stable value which equals to half input voltage.

The input resistance of this voltage divider should be small while the output resistance should be large. Since a ideal voltage source, which has a zero output resistance, is connected to the input stage of this voltage divider, and gate node of NMOS, which has infinite input resistance, is connected to the output node of this voltage divider, there is no strict limitation on these two resistors. And they are chosen to be 1k.

3.7 Overall topology implementation

3.7.1 Top level topology

To connect all the components, we get a overall topology as below,

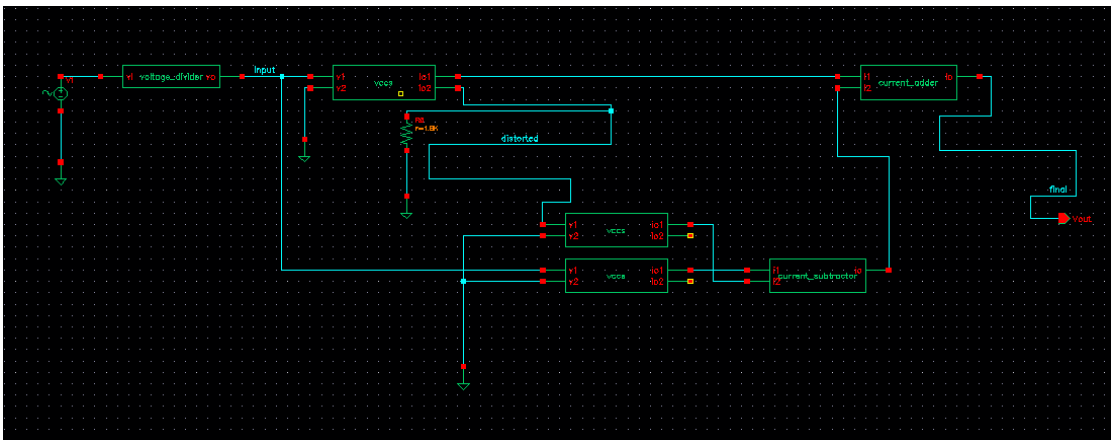

Figure 33. Overall circuit implementation

3.7.2 Simulation result

The final output current is shown below,

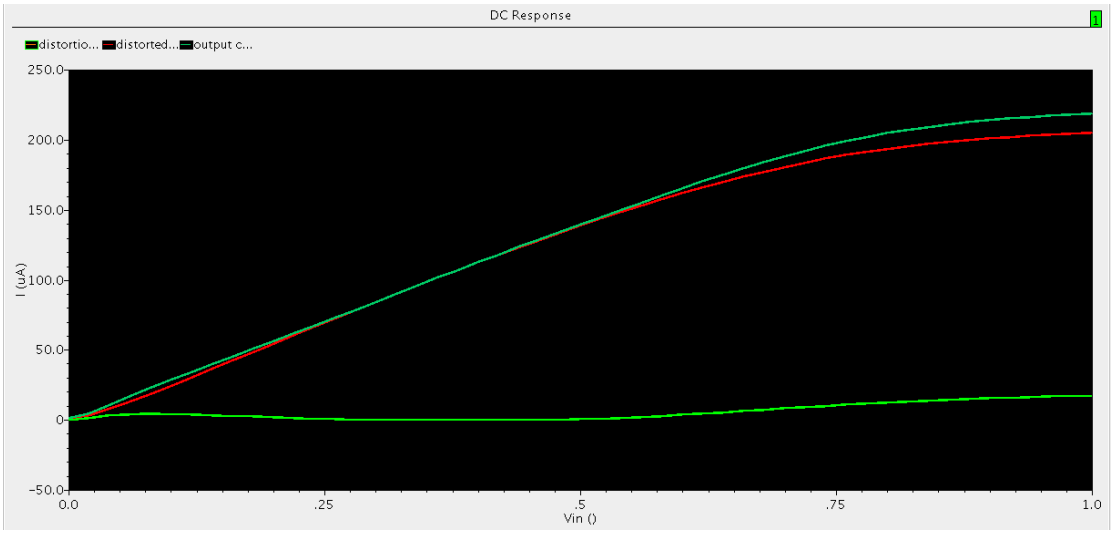

Figure 34. Simulation result 1 of overall circuit

The output current equals to the addition of the distorted current and distortion signal. The output current is more linear than the first output of the VCCS. If connect the output stage to a 3.8k resistor, input voltage and output voltage comparison can be seen in the simulation result below,(the reason why choose 3.8k is because the transconductance of VCCS is $\frac{1}{1.9\text{k}}$, and the input voltage shrinks to a half before flowing into the VCCS, thus 3.8k resistor is need here to achieve a unit gain)

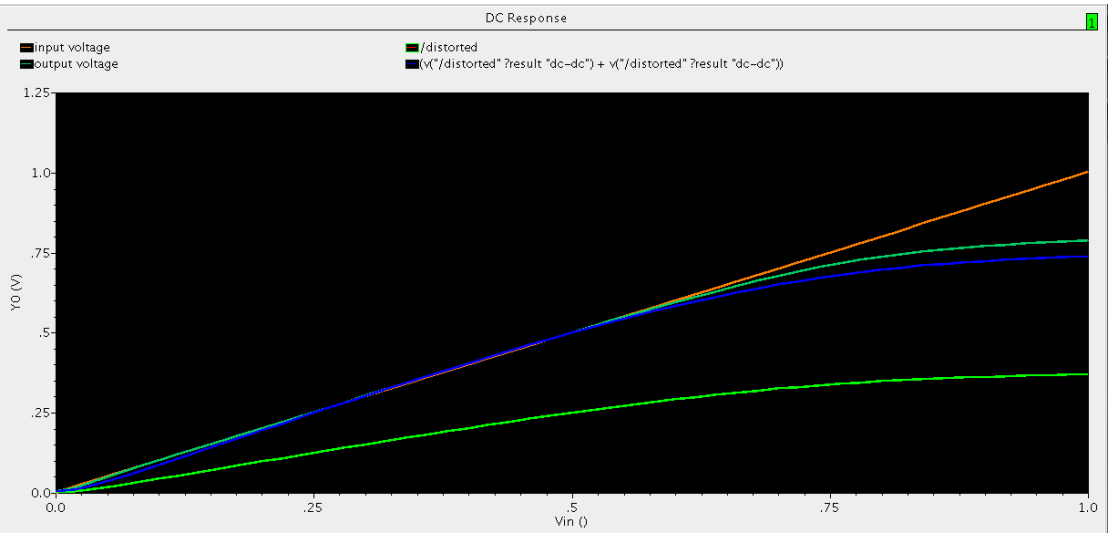

Figure 35. Simulation result 2 of overall circuit

The light green line represents the distorted signal comes from first VCCS, to compare with the input and output voltage, it has to extend to two times as before.
As seen from the figure above, the output voltage becomes more linear than the distorted signal.

Chapter4. Analysis of Results Obtained

4.1 Overall performance

4.1.1 Linearity

As shown in figure35, a single feedforward loop has improvement on the output signal linearity, yet still has distortion compared to the ideal linear output. But this result can be further improved to use nested feedforward circuit, that is to use the overall feedforward circuit as the first VCCS in the circuit, and the result should be better than what we get now. And if we build this nested feedforward circuit several times, a considerably results will be achieved.

4.1.2 Input and output signal range

Input signal range varies from 0 to 1 V.

Output signal range varies from 0 to 200uA.

4.1.3 Transconductance

The transconductance of overall circuit is $\frac{1}{3.8\text{k}}$, since the transconductance of VCCS is $\frac{1}{1.9\text{k}}$, and the voltage divider shrinks the input voltage.

4.1.4 Input impedance

Input impedance of overall circuit equals to the input impedance of voltage divider, which equals to 2k.

4.1.5 Output impedance

Output impedance is quite high, since the output stage is a wide swing current mirror which has high output impedance.

4.2 PVT analysis

4.2.1 PVT corners

PVT represents Process, Voltage and Temperature, which is very important for the corner analysis of a CMOS design. The PVT analysis is suitable for both analog and mix signal circuit.

Process Corner

Different process parameters and photolithography cause different Transconductance. For CMOS process corners, the extremes of operation for devices need to be considered. Normally there are two extremes for both NFET and PFET: "'fast' implying greatest Small Signal Transconductance, and 'Slow' implying least Small Signal Transconductance." [7]Furthermore, NFETs and PFETs should be considered separately, because when a NFET (or PFET) is driven by the process and realization parameters to 'fast' (or 'slow') state, the PFET (or NFET) can be driven to 'slow' (or fast) at the same moment. Thus there will be four extreme conditions: SS, SF, FS, FF. which mean,

SS: Slow NFET and Slow PFET
SF: Slow NFET and Fast PFET
FS: Fast NFET and Slow PFET
FF: Fast NFET and Fast NFET
NN: Normal NFET and Normal PFET

Voltage Corners

In practice, it is impossible to provide an ideal power supply for a circuit. The DC terms of power supply voltage will varied, thus the circuit should be considered and simulated at extreme situations which are specified supply voltage ± 10%. In this project, extreme situations are 1.25V-1.25V*10%, -1.25V+1.25*10% and 1.25V+1.25V*10%, -1.25-1.25 *10%which are 1.125V∽-1.125V and 1.375V∽-1.375V.

Temperature Corners

The normally junction temperature that assumed in design is 60℃, but, however, it is hard to make a circuit operates at the ideal temperature in practice. The real operation temperature for a design is varied due to the ambient temperature, operation time, and thermal energy dissipation in the die and so on. There are two extreme situations needed to be simulated which are -40℃ and +125℃.

PVT corner space is shown below,

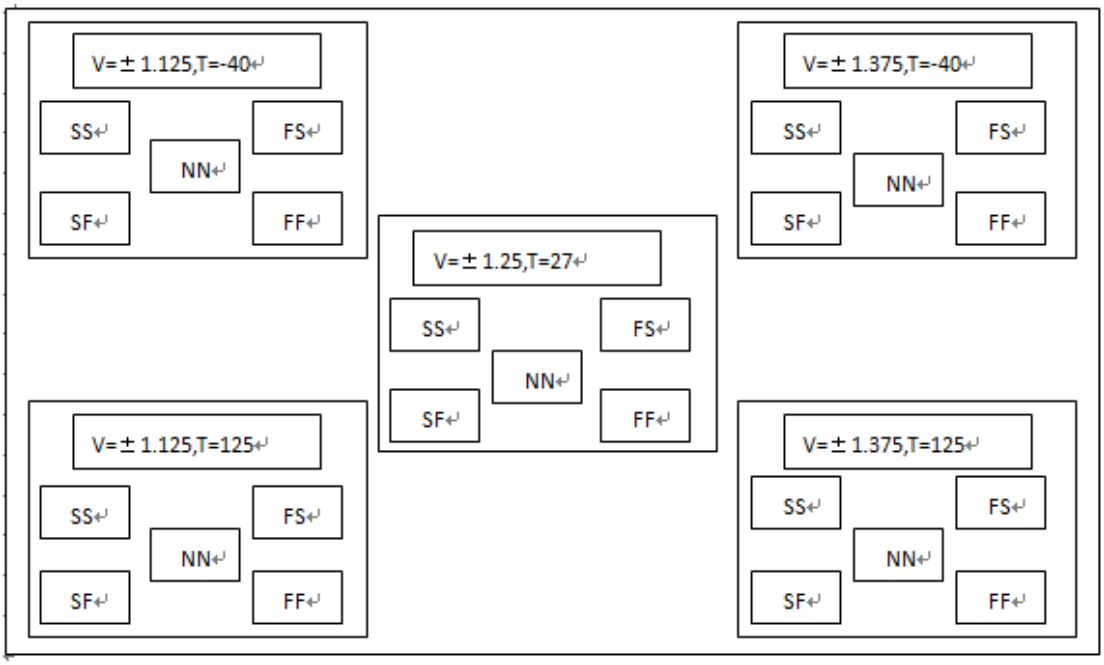

Figure 36. PVT corners

There are two temperature corners, two voltage corners and 4 process corners, thus the amount of all combinations of corner cases add up to 2*2*4=16.If taking the nominal situations into account, we have 5*5=25 situations to be simulated all together, as shown in the figure.

4.2.2 Simulation result

To test the circuit performance under different PVT corners, the voltage signal obtained at the output node of voltage divider and the voltage signal obtained at the output node of the first CCVS are to be examined. Let the output current go through a CCVS which will convert the current signal to voltage signal, and make sure that this output voltage is in the same scale with those two voltage signals just mentioned before. This final output voltage signal will also be examined and compared with other two voltage signals to see whether the whole circuit can make improvement on signal linearity. These three voltage signals are referred as 'input', 'distorted' and 'final' in the simulation. The simulation result is shown below,

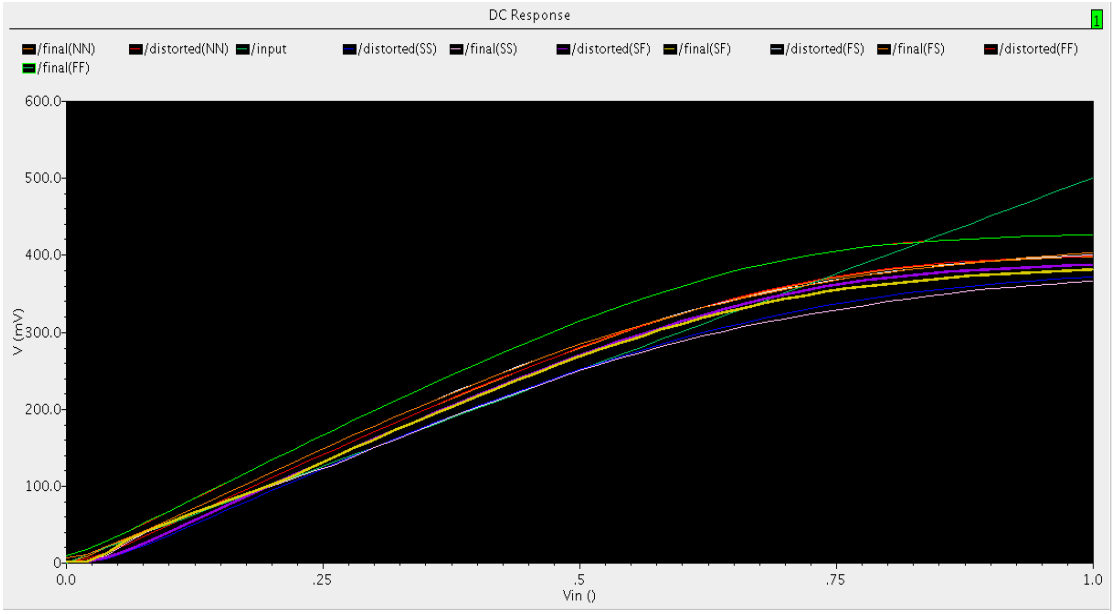

Figure 37. Simulation result on V=±1.125, T= -40

(a)

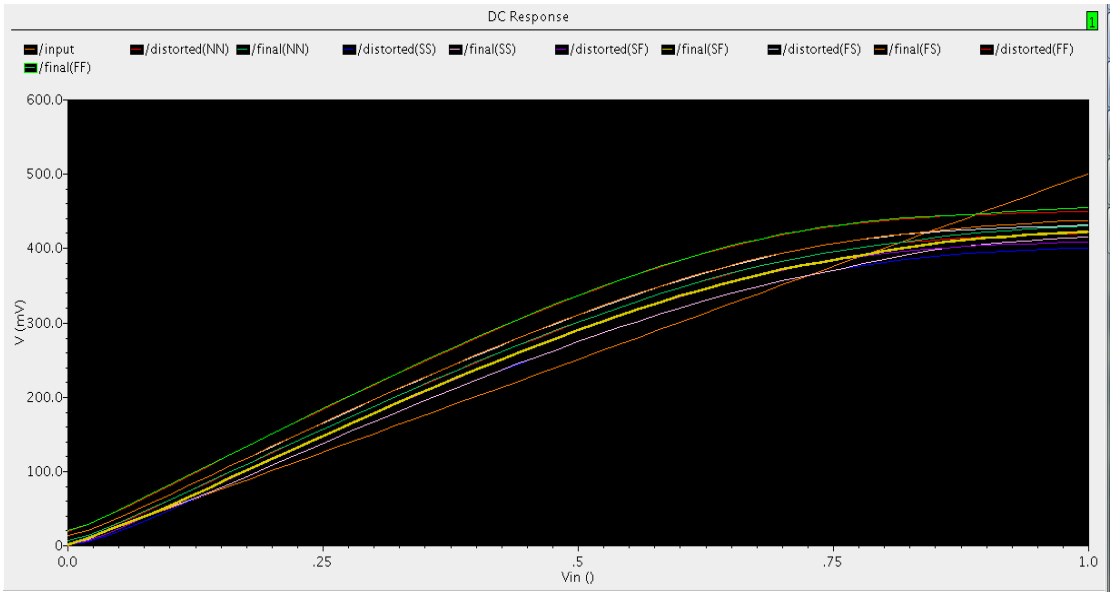

Figure 38. Simulation result on V=±1.375, T= -40

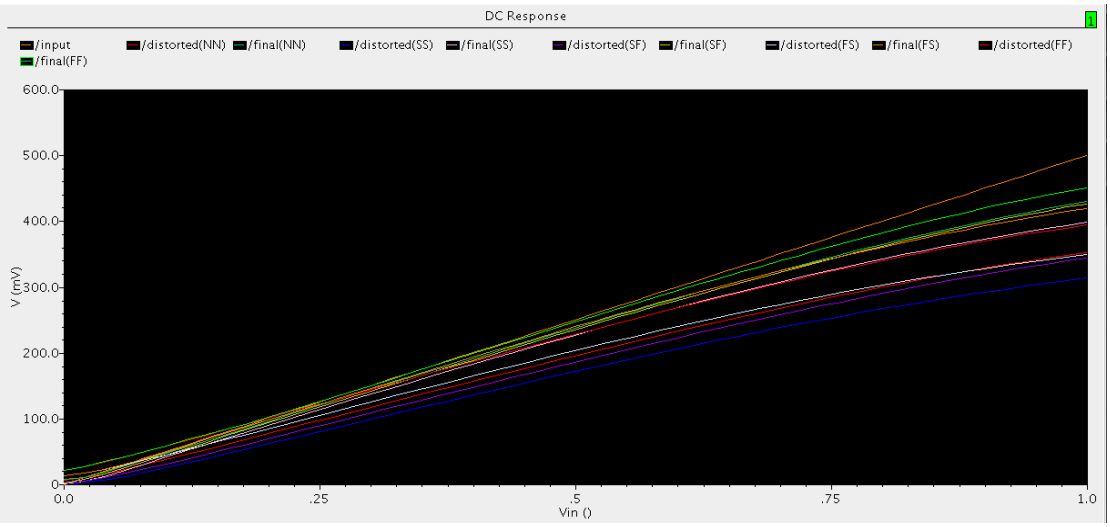

Figure 39. Simulation result on V=±1.125, T= 125

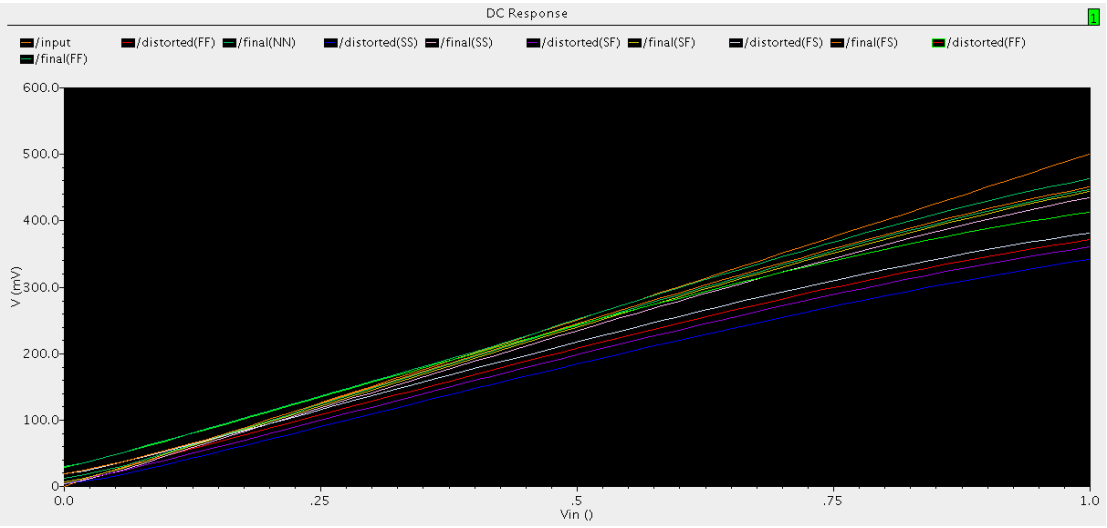

Figure 40. Simulation result on V=±1.3755, T= 125

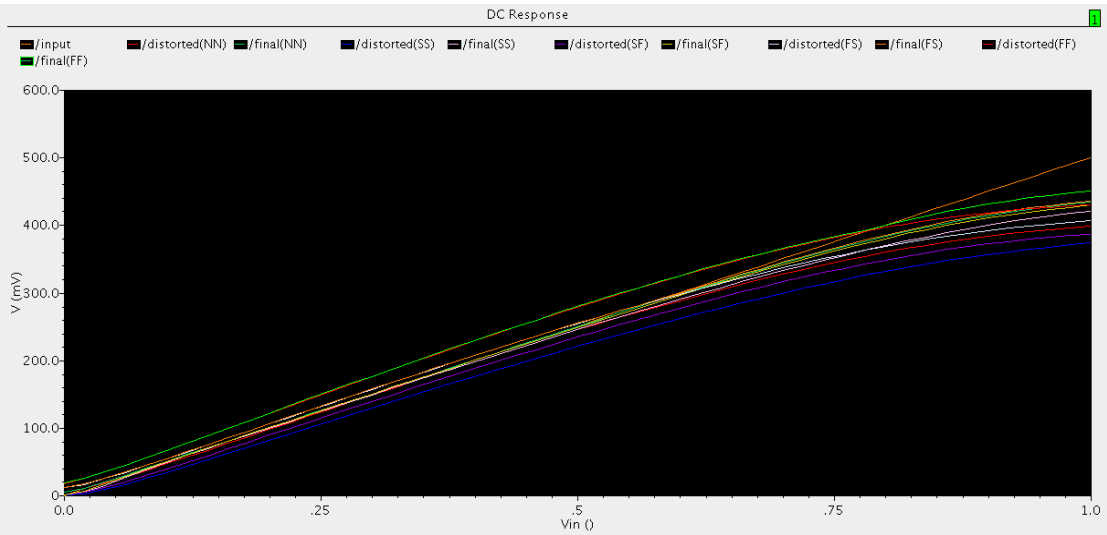

Figure 41. Simulation result on V=±1.3755, T= 125

As seen from the figures above, there is a small variation in the ‘distorted’ signal when the temperature changes. As temperature increases, the ‘distorted’ signal shrinks a little and the corresponding line always stays below the ‘input’ line (shown in figure 39 and 40); when the temperature decreases, the ‘distorted’ signal exaggerate a little and the corresponding line will surpass the ‘signal’ line when the input voltage is under a certain value(shown in figure 37 and 38).Figure 39 and 40 show us that every ‘final’ signal is between the ‘input’ signal and corresponding ‘distorted’ signal. That means in these situations, the output signals approach linearity compared to the inner distorted signal and it proves the whole system do make certain progress on signal linearity. Figure 37 and 38 show us that the ‘final’ line and the ‘distorted’ signal overlap when the ‘distorted’ line surpasses the ‘signal’ line; otherwise the ‘final’ line is between the ‘distorted’ line and the ‘signal’ line. This feature indicates that the system can function well only when the distorted signal is below the input signal, and does not have the justification ability when the distorted signal goes beyond the input signal, or this system can only get rid of negative distortion, but cannot handle positive distortion. The reason for this disadvantage is that the whole circuit is designed as a uni-polar system; the VCCS, the current adder and the current subtractor do not have the ability to deal with negative voltage or current. Further improvement will be made to overcome this disadvantage. One good method is to build a bipolar circuit which has the ability to operate both negative and positive signals. Another method is to justify the CCVS to make sure that even in the worst case, every ‘distorted’ line is below the ‘input’ line, but of course this is not a good solution, because this method will decrease the performance under nominal situation and high temperature situation.

The simulation result also shows a good ability of voltage tolerance. The circuit functions the same under different voltage corners. That is because all the FET works in the saturation region even in the worst case.

The same problem exists in the process variation simulation. The circuit loses its function under the situation when the ‘distorted’ signal surpasses the ‘input’ signal caused by different process parameters. The solution is the same as discussed in the temperature variation case.

Chapter5. Comparison with Feedback Technique

5.1 Feedback principle

Feedback technique is a common method to keep system linear in IC design. The basic principle of feedback technique is illustrated in the following figure and equations, the output of the main amplifier is connected back to its input to establish a feedback loop, as shown below,

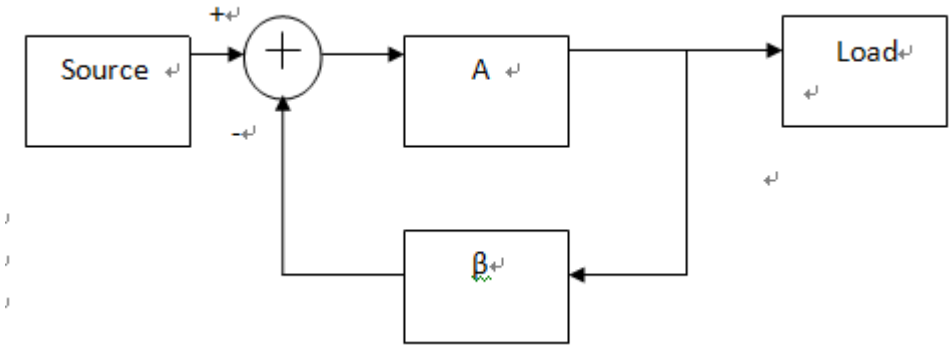

Figure 42. Circuit topology of feedback

A represents the gain of the main amplifier while β represents the gain of the amplifier connected back to the input stage. The loop gain is then calculated as below:

$$A_f = \frac{A}{1+A\beta} = \frac{1}{\frac{1}{A}+\beta}$$

Since the main amplifier is a high gain amplifier $\frac{1}{A}$ is very close to zero and can be neglected, thus the formula above can be written as:

$$A_f = \frac{1}{\beta}$$

The output signal is quite linear with the input signal provided that the main amplifier has a high enough gain. If the output signal is directly connected back to the input stage, β equals to 1 and the overall gain is unit.

The fundamental requirement of feedback loop is that the main amplifier has a super high gain. As we know, if the gain of an amplifier is raised up, then the bandwidth of the circuit will decrease, since the product of gain and bandwidth is a fixed value. Thus, the system is linearised by feedback technique on the disadvantage of working in a narrower bandwidth than before.

5.2 VCCS based on feedback

It is a common method to build a large signal voltage controlled current source using feedback. This circuit will have highly linear characteristics because of the high gain the main amplifier has. But this kind of method will not perform so excellent over a wide bandwidth, because as frequency rises, the gain becomes lower, and this will affect the linearity of the overall circuit.

5.2.1 Circuit design

The first step is to build up an operation amplifier with high gain. A two stage operational amplifier with differential amplifier as the first stage and a common source PMOS transistor as the second stage is shown as below, with the output node connect to a resistor to change the output voltage to current.

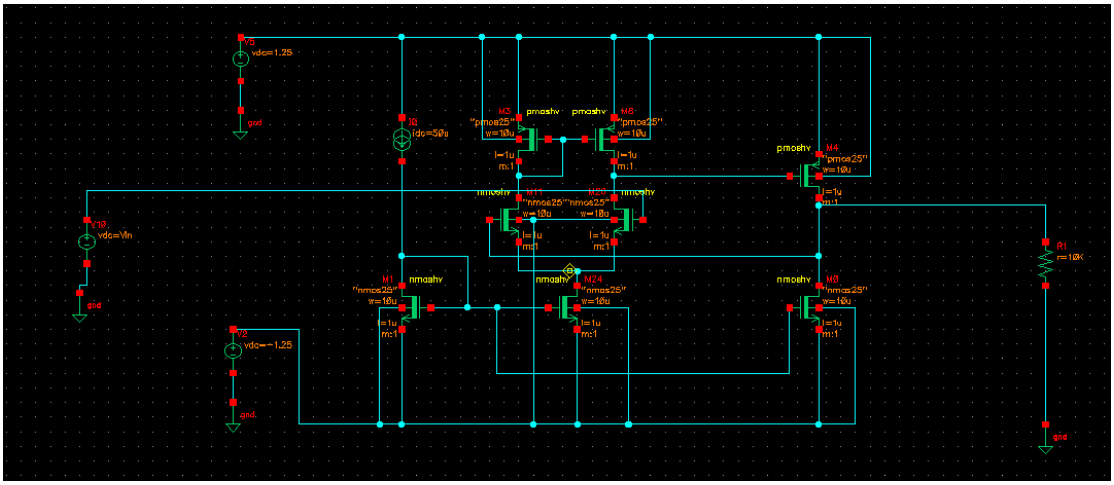

Figure 43. Feedback loop by a two stage OPAMP

Connect the output of the OPAMP to the positive input, and feed an input voltage into the negative input of the OPAMP. Then a negative feedback loop is built up.

5.2.2 Compensation for stabilization problems

In order to make feedback loop stable, sufficient phase margin and gain margin have to be maintained. Do a stability simulation, the gain margin and phase margin is shown below，

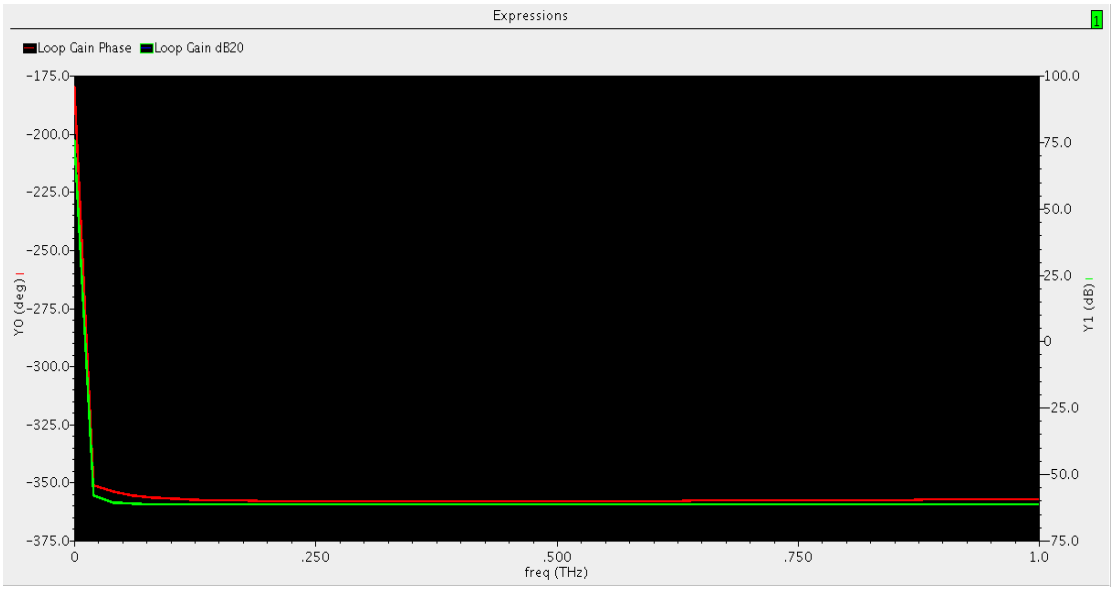

Figure 44. Stabilization analysis

This shows there is not enough phase margins to keep the feedback loop stable. To change the phase margin, compensation capacitor and resistor are added into feedback loop to compensate for the stability problems. A 10k resistor and 10p capacitor are added, the new circuit is shown，

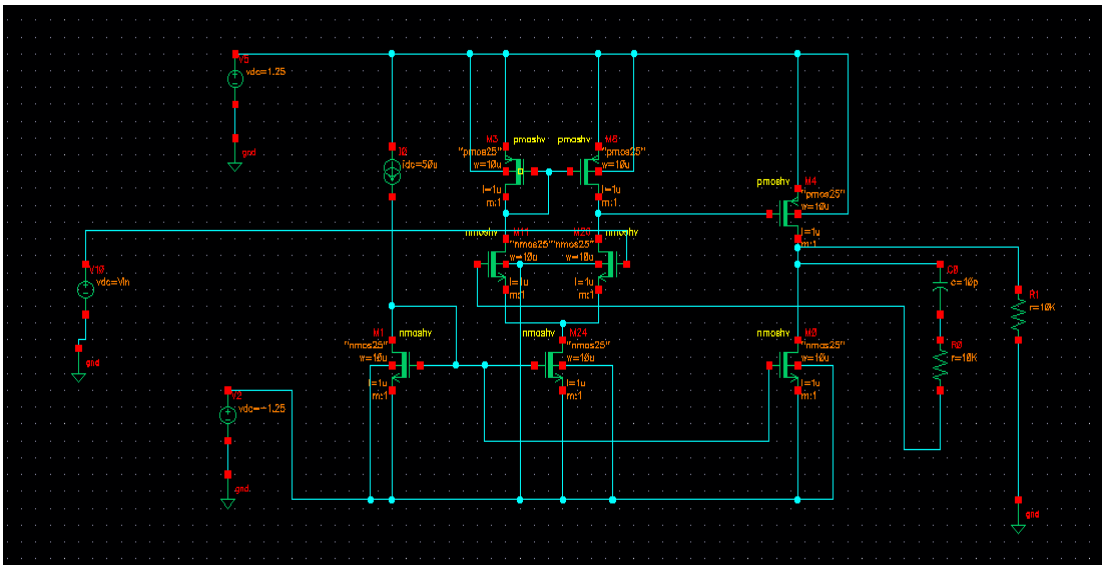

Figure 45. Modified feedback loop with compensation

And the stability simulation result is,

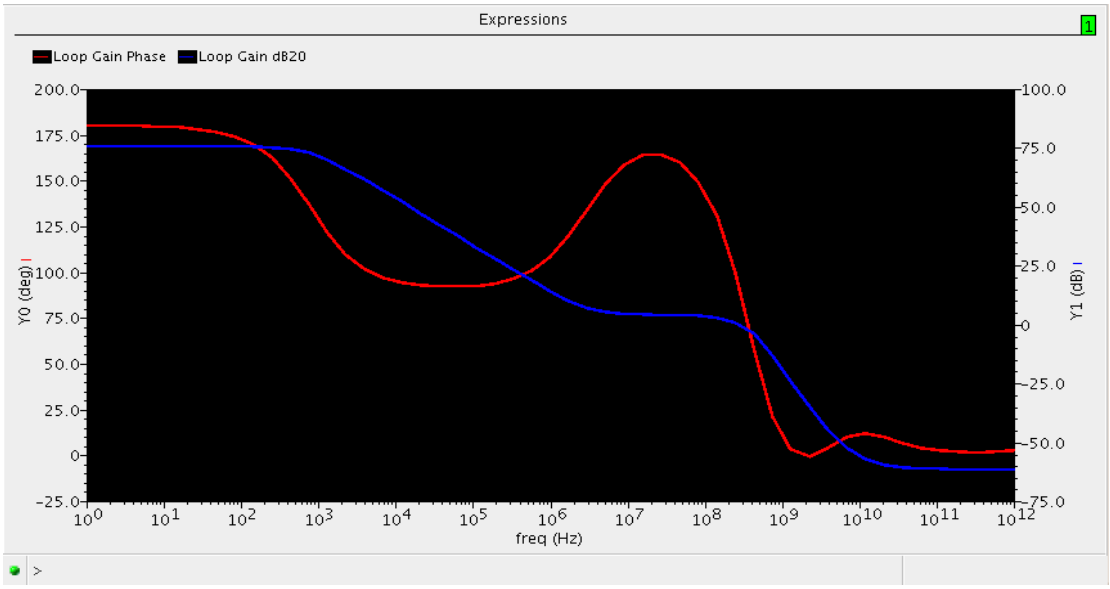

Figure 46. Stabilization analysis of the modified loop

As seen from the picture above, when loop again approaches 0db, the phase is around 70 degree, which means there is enough phase margins and this OPAMP is stable.

5.3 Linearity comparison

Feedback circuit has a better linearity because of the high gain amplifier; this will force the output to follow the input signal closely.

As shown in the figures below,

1. Feedback

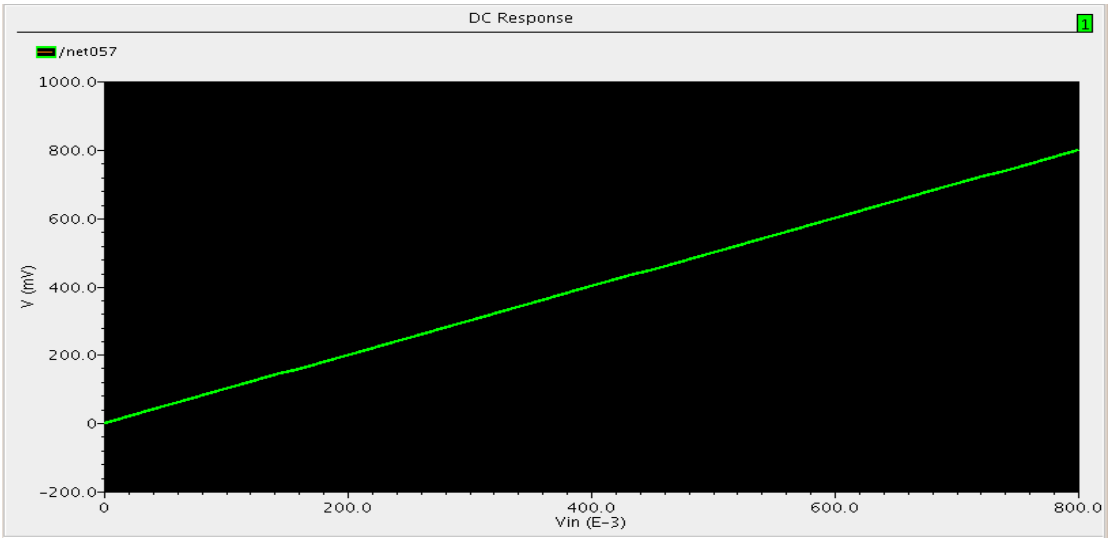

Figure 47. Simulation result of feedback loop

2. Feedforward

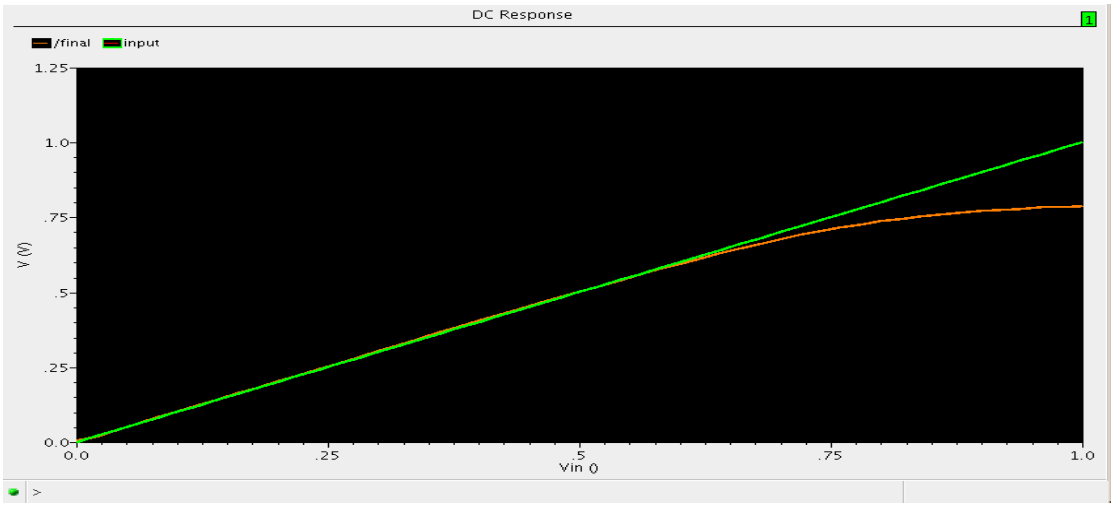

Figure 48. Simulation result of feedforward loop

As seen from the figure, feedback has a much better linearity compared to a single feedforward block. But the output linearity of feedforward can be improved to use nested feedforward circuit. Theoretically, this improvement can be significant and the output signal can be quite linear provided enough nested feedforward is used. But delay of the circuit will increase and the cost of design will be considerably high.

5.4 Bandwidth comparison

Although feedforward does not have good linearity as feedback technique, but it has a better working bandwidth. As shown in the figure below，

1. Feedback

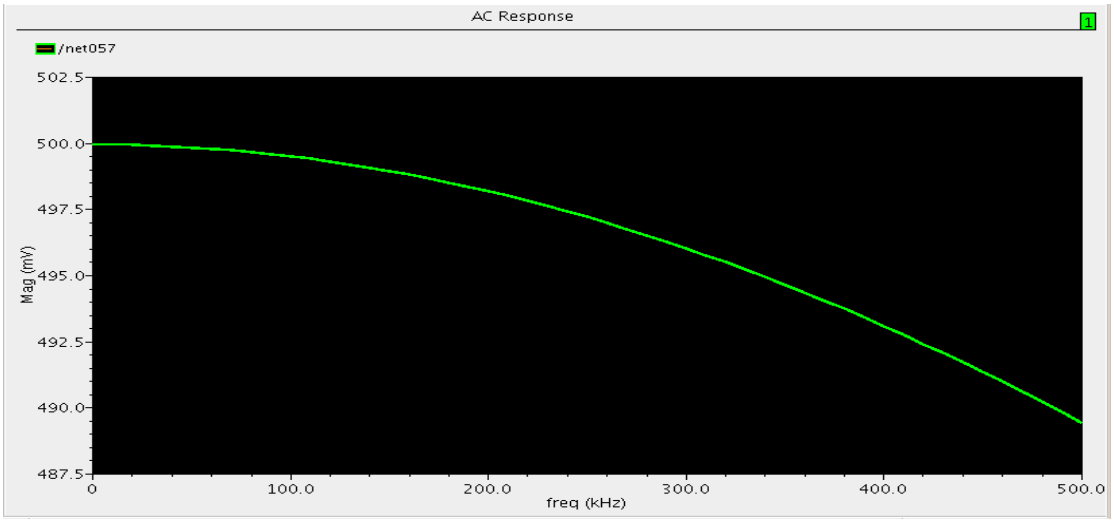

Figure 49. Frequency analysis of feedback loop

2. Feedforward

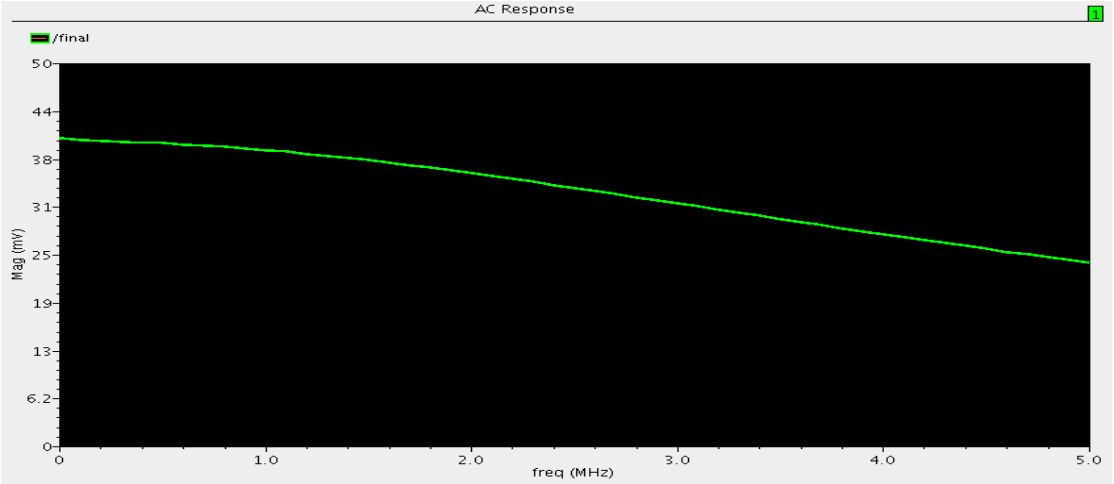

Figure 50. Frequency analysis of feedforward loop

As seen from the figure above, when fed with an input voltage of 0.5V, the output of feedback circuit will be 0.5V over a small bandwidth ranging from approximate 0 to 50 KHz, and the output of feedforward circuit is 0.41 V and holds that value for a relatively broad bind. Since compensation capacitor must be added into the feedback loop to maintain stable, at the same time, a new pole is introduced into the system, which will decrease the OPAMP gain faster when the frequency rises. For feedforward circuit, since there is no obvious feedback loop existing in the circuit, and only the inner feedback in the current mirror can decrease the gain over extraordinary high frequencies, it has a better bandwidth performance compared to feedback.

Chapter6. Review and Conclusions

Feedforward technique has been implemented in this project. The aim was to design a linearised large signal wideband transconductance block with an input voltage ranging from 0 to 1V and an output current ranging from 0 to 200uA, which was achieved at the end of the project.

A large signal voltage control current source is established in this project using feedforward. There are innovations in this project; the mechanism of how feedforward technique can be used in the CMOS circuit is carefully designed and researched. The signal is designed firstly converted from voltage to current, generating distortion part, and then do subtraction and addition in the current mode. Much more energy is focused on how to make each functional block works well under different situations and improve the overall performance of the whole circuit. Since this project is under large signal environment, a considerable amount of work is to make full use of the limited voltage supply and make every part of circuit works well under the voltage boundaries. And second innovation lies in how to build a relationship between voltage and current in the VCCS. To map a voltage ranging from 0 to 0.5v to a current ranging from 0 to 200uA, a differential amplifier is used, the current flows through one of the differential pair is subtracted by half the bias current, and the result is taken as the output current.

To obtain a good understanding of feedforward technique, chapter 2 give a detailed introduction of feedforward system and feedforward features.

Chapter 3 first gives a better suggestion of implementing feedforward loop, and then discuss in detail how each functional block should be built up. Some advanced circuit topology is introduced to make the circuit function well under limited power supply. And the FET dimension is carefully sized to balance all the requirements such as voltage swing, wide input range, voltage headroom, current accurate, etc.

Chapter 4 delivers overall features of the whole circuit and then makes a PVT analysis for the circuit. The overall parameters for this feedforward circuit meet the design requirements. And this circuit has a good performance under most PVT corners. But it still has some disadvantages under certain PVT corner, which remains to be further improved.

A comparison with feedback technique is performed in chapter 5. The comparison based on two points: linearity and bandwidth. It is clear to make a conclusion from the simulation result that feedforward technique has a better bandwidth but does not perform as good as feedback loop in the low frequency domain.

Chapter7. Further Work

6.1 Transistor based current control voltage source

A better design for the current control voltage source is expected in the future work. Since the value of resistor will vary 20% under temperature variation, it is not a good design to use r resistor to perform a highly linear conversion from current to voltage. An advanced method should be researched so that it can function well under PVT variation.

6.2 Make the circuit works in bipolar mode

A further improvement of this project should be focused on the bipolar working mode of this circuit, which means the input voltage range can vary from -1v to 1v， and the output current ranges from -200uA to 200uA. This is a challenging design, since a self compensating circuit should be designed in which half circuit works on the positive input, half circuit works on the negative input.

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