Contents

Executive summary

The modern digital communication systems especially the receivers, invariably employ a high frequency clock essentially free of jitter. Hence extensive researches undertake the study and design of new topologies for such systems.

A system is developed in this project whose output is digitally controlled by the action of feedback. The system regularly compare the output with a reference clock, minimise the noise and produce a stabilised clock. Phase locked loop is such a system, however it is modified to suit the specifications.

A high resolution converter, delta sigma modulator is employed for digital control frequency modulation which replace the conventional voltage controlled oscillator of phase locked loop to achieve clock free of jitter. This is a contemporary topology which was brought into the form after the preliminary investigation of noise sources in PLL being that of noisy input reference, quantization error noise and the noise associated with analogue components.

This project is in collaboration with Xintronix who specialize in high speed communications for data centre, telecommunications infrastructure and consumer applications.

Introduction

With the emergence of powerful digital signal processors for telecommunication, the use of clock signals (of various frequencies) for synchronization and synthesis has become inevitable. The generation of a clock signal can be considered as the key element for any telecommunication system. Thus the application of phase-locked loops (PLL) is significant. The idea of phase locked loop was first conceived by H. D. Bellescize in 1932. Since then it has found many applications in control system, measurements and instrumentation. PLL's are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to recover a signal from a noisy communication channel, generate stable frequencies at a multiple of an input frequency (frequency synthesis), or distribute clock timing pulses in digital logic designs. Since a single integrated circuit can provide a complete phase-locked loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a Hertz up to many gigahertz.

Although the concept of PLL was introduced in 1932, the realization was found to be difficult until the development of IC's in 1980. Since then, the realization of PLL using integrated circuit (IC) technology for improvement in performance and for reliability has become more important than ever. Hence the study and design of PLL is of prime importance for any CMOS analogue designer.

Chapter 1

Objective

The project eventually aims to generate a high frequency signal (2.5GHz) essentially free of jitter using a phase locked loop(PLL). The classic structure of PLL which is modified to suit the specifications of the project(being to obtain a jitter free clock) is extensively studies and implemented.

The fundamental approach undertaken in this system is to identify sources of jitter at various points in the PLL and incorporate solutions to eliminate it. The sources of noise and the associated preliminary solutions are discussed as follows.

The input reference signal which might have been impaired by jitter(inherent of clock generation) is filtered out using anti-aliasing filter before the signal is processed by delta-sigma modulators. Since noise avoidance is the critical part, delta-sigma modulators is incorporated which gracefully shape the noise out of the signal bandwidth to a much higher frequency range . This high frequency noise can be subsequently filtered out using an analogue low-pass filter. The filtered signal now is combined with quadrature frequency converter which again is another source of noise. The feedback of the PLL compensates for any noise introduced here.

Although, the PLL is a classic system, the use of sigma-delta modulators in the PLL for noise avoidance is a contemporary topology. Apart from the classical components of PLL, being the phase detector and low-pass filter, the system implemented here comprises of delta-sigma modulator and quadrature frequency converter. Cadence is adopted to create the schematics for the block analogue low-pass filter(implemented at transistor level) while all other components are implemented using VerilogA(hardware descriptive language). The main added value is obtaining jitter free clock which is used for frequency synthesizers which find applications in radio receivers, mobile telephones, radio-telephones, walkie-talkies, CB radios, satellite receivers, GPS systems.

Chapter 2

Phase locked loop

The generation of a high frequency signal essentially requires a feedback system to compare the output regularly with a reference signal. Phase locked loop is one such system. To get an insight how a phase locked loop functions, a exhaustive literature review of the subject has been undertaken and presented below.

2.1 Fundamentals of Phase locked loop

A PLL is a device which causes one signal to track another signal. It keeps an output signal synchronizing with a reference input signal in frequency with help of a feedback path. The general block diagram of a PLL is as shown in figure 2.1.

The elements of the system are phase detector (PD), loop filter (LP) and voltage-controlled oscillator (VCO). The VCO is an oscillator whose frequency is proportional to an externally applied voltage. When the loop is locked on to an incoming periodic signal, the VCO frequency is exactly equal to that of the incoming signal. The phase detector is a non-linear device whose output contains the phase difference between the input reference and the VCO signal.

This signal is utilized by the loop filter to produce a dc voltage corresponding to the phase difference.

To further the explanation, if the frequency of the incoming signal shifts slightly, the phase difference between the VCO signal and the incoming signal will begin to increase with time. This will change the control voltage in such a way as to bring the VCO frequency back to the same value as the incoming signal. Thus the loop can maintain lock when the input signal frequency changes and the VCO input voltage is proportional to the frequency of the incoming signal. The range of input signal frequencies over which the loop can maintain lock is called "*lockrange*". [3]

An important aspect of the PLL performance is the capture process, by which the loop

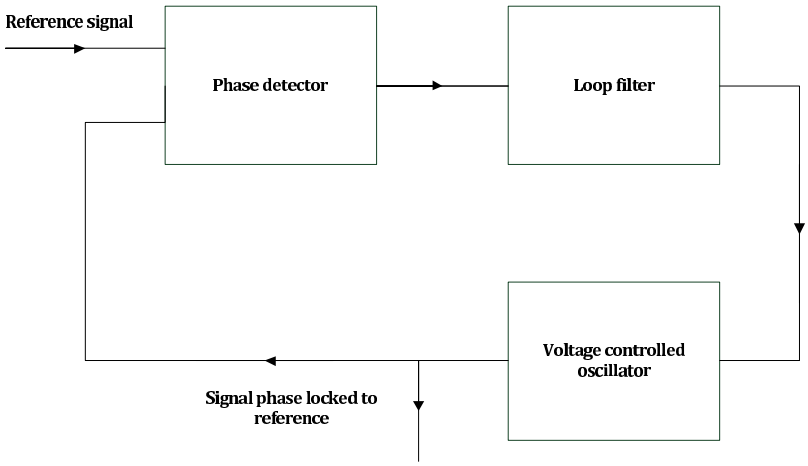

Figure 2.1: General PLL block diagram

goes from the unlocked, free-running condition to that of being locked on a signal. In the locked condition, the VCO runs at the frequency corresponding to zero applied dc voltage at its control input. This frequency is called the center frequency of free-running frequency.

The PLL is a highly non-linear system due to two of its indispensable non-linear components i.e. the phase detector and the voltage-controlled oscillator which translate the problem from signal response to phase response and back again.

2.2 Mathematical analysis of PLL

Consider vin(t) and vout(t) to be the input reference and output of oscillator signals with ω_i and ω_o as their angular frequencies and θ_i and θ_o as their phase constants. The vin(t) and vout(t) can be written as,

$$vin(t) = ACos(\omega_i t + \theta_i t) \tag{2.1}$$
$$vout(t) = BCos(\omega_o t + \theta_o t) \tag{2.2}$$

where A and B are constants.
The PD acts as a signal multiplier and hence the output of the PD can be written as,

$$v_{pd}(t) = K_{pd}Cos[(\omega_i - \omega_o)t + \theta_i - \theta_o] + Cos[(\omega_i + \omega_o)t + \theta_i + \theta_o] \tag{2.3}$$

where K_{pd} is the PD constant.

$$\text{Using, } CosuCosv = \frac{1}{2}[Cos(u - v) + Cos(u + v)]$$

The higher frequency component $(\omega_i + \omega_o)$ is eliminated by the low pass filter(LPF) and hence its output can be given as,

$$v_{lpf}(t) = K_{pd}Cos\left[(\omega_i - \omega_o)t + \theta_i - \theta_o\right] \tag{2.4}$$

After sufficient period of time, allowing the VCO output to synchronize with the input signal, it can be shown that,

$$vout(t) = Bsin(\omega_i t + \phi_0) \tag{2.5}$$

Comparing 2.2 and 2.5,

$$\theta_o = (\omega_i - \omega_o)t + \phi_o \tag{2.6}$$

and LPF output signal $v_c(t)$ becomes,

$$v_c(t) = K_d cos(\theta_i - \phi_{o)} \tag{2.7}$$

The VCO is a frequency-modulated oscillator, whose instantaneous angular frequency is a linear function of the controlled signal $v_c(t)$, around the central angular frequency

$$w_{inst} = \frac{d}{dt}(\omega_o t + \theta_0) = \omega_o = K_v V_c t \tag{2.8}$$

Taking derivative of Eq. 2.6,

$$\frac{d\theta_o}{dt} = K_c v_c(t) \tag{2.9}$$

$$\omega_i - \omega_o = K_d K_v cos(\theta_i - \phi_o) \tag{2.10}$$

It can be derived that,

$$\phi_o = \theta_i - cos^{-1}\frac{\omega_i - \omega_o}{K_d K_v} \tag{2.11}$$

Yielding,

$$v_c(t) = \frac{\omega_i - \omega_o}{K_v} \tag{2.12}$$

Equation 2.12 clearly shows that it is the dc signal v_c, that changes the VCO frequency from its central value ω_o, to the input signal angular frequency ω_i [4].This is the underlying concept of PLL.

Chapter 3

Phase locked loop using digitally controlled frequency modulator

The prototypal system of PLL is prone to signal noise and interference which becomes a major impediment where high frequency signals are involved. Another main drawback of the conventional PLL is the use of considerable amount of analogue circuitry. The analogue complexities significantly slow down the operation of PLL mainly due to the VCO and hence a faster oscillating VCO would be expensive. Due to the PLL being sensitive to noise, the VCO and the loop filter would have to be isolated from the high speed digital circuitry adding to increased complexity of design.

In order to achieve a robust signal, the VCO of the classic PLL is been replaced by a digitally controlled frequency modulator(DCFM) and a frequency converter. The DCFM employs a digital-to-analogue delta-sigma modulator to generate a control signal and the frequency converter to translate the input reference signal(of lower frequency) to a higher frequency signal basically performs frequency multiplication. The figure 3.1 shows the topology of the modified PLL to achieve a jitter free high frequency clock.

It is required to detect and suppress side-band frequencies of the input reference signal and thereby achieve a "*clean*" output from a "*noisy*" input signal. As in a conventional PLL, the output signal is regularly compared with the input reference signal, generate a "*correction*" and employ it to steer the output signal towards the required frequency.

3.1 Noise injector

To simulate the "*real*" environment in which a circuit operates, noise is generated in order to verify the side-band suppression. For this, white Gaussian synchronous jitter is induced to input reference signal. The verilogA code generates random numbers using a function $rdist_normal(seed, mean, stddev)$ which takes parameters a seed i.e. the start range, mean and the standard deviation values. The magnitude of the noise can be scaled by multiplying

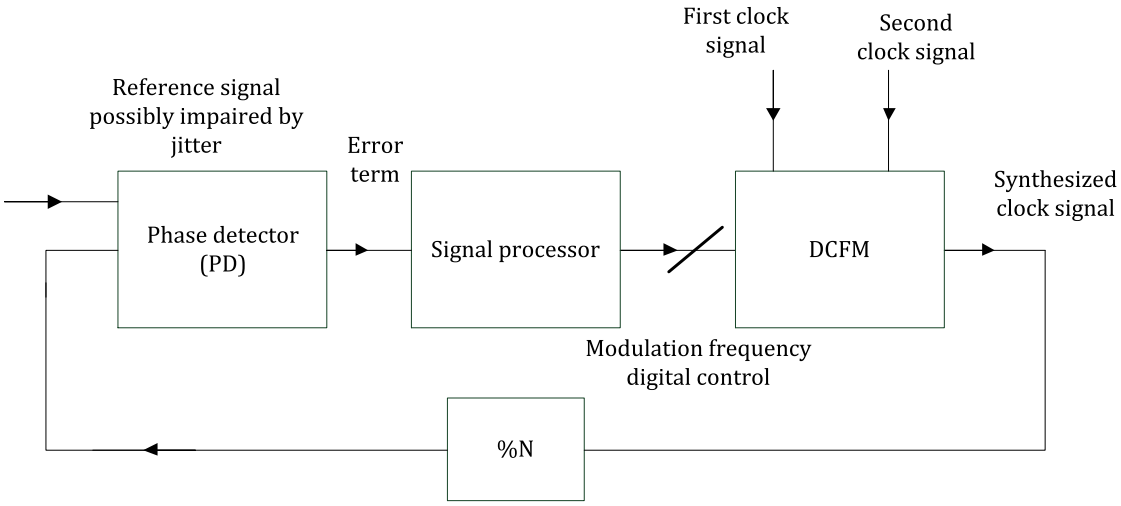

Figure 3.1: Clock synthesis PLL

this factor by the desired amount.

3.2 Phase detector

The comparison of the input reference signal and the output of the PLL is achieved by incorporating an XOR gate(figure 3.2). The phase detector detects any phase differences in input reference and the feedback signal and then generates an error signal. The non-linearity feature of the phase detector brings about the correction of phase error in the loop.

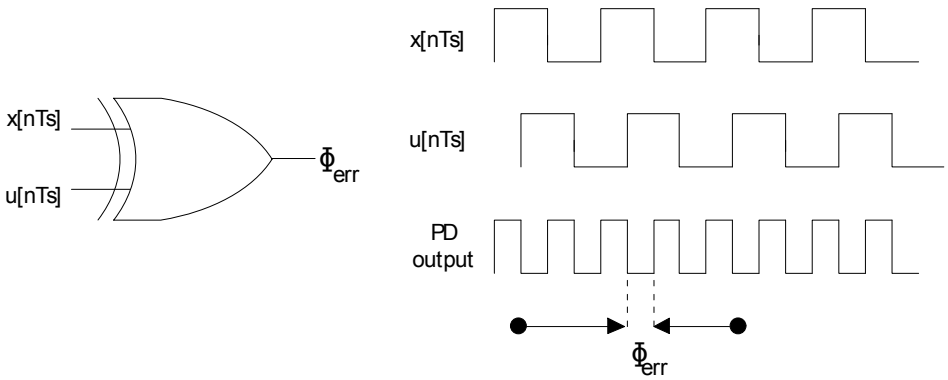

Figure 3.2: Phase detector using XOR logic

Although the XOR gate successfully determines the magnitude of correction required, it fails to convey whether the feedback signal has to lead or lag the input reference signal. This is the main disadvantage of XOR gate. Hence in order to determine the direction

towards which the feedback signal has to be steered, subtraction of the two signals is carried out which is dealt in later section.

3.3 Signal processor

A signal processor is employed in conjunction with the phase detector to determine the phase error between the input reference and the feedback signal. It basically acts as a low pass filter computing the average of the phase error over a period of time. The phase error is sampled at a rate of 2^n times the input reference signal where "n" is the bit resolution which is computed so as to determine the phase error w.r.t one cycle of reference signal. This block is analogous to the charge pump of a conventional PLL determining the amount by which the feedback signal has to be steered to lock onto the input reference signal.

The "n" is chosen as to procure a realizable clock frequency signal. The input reference signal being 5MHz, which has to be sampled at a rate of 2^n, i.e. 32 times the 5MHz is 160MHz. Hence the the sampling rate of the phase error is largely constrained by the clock signal.

The signal processor is followed by a loop filter which is used to suppress the noise and high-frequency signal components from the phase detector and provide a dc-controlled signal for the VCO. The phase error voltage is filtered by the loop filter.

The type of the loop of the PLL is determined by the number of integrators within the loop. The VCO essentially consists of a integrator and inclusion of loop filter contributes to another added integrator. Such a loop comprising two integrators is called as second-order PLL[4]. The loop filter essentially determines the limit frequency which can be detected by the loop for correction. Frequencies which are outside the range are not captured for correction.

The loop filter implemented in this system is digital and realized using an adder and a latch.

3.4 Digitally controlled frequency modulation

The block diagram of DCFM is as shown in figure 3.3. The digital control inputs from the signal processor is utilised to generate a sinusoidal corresponding to the difference of frequency between the input reference and the output signal. This sinusoidal generated is quantized at a very high frequency and the converted to digital input which is utilised by the delta-sigma modulator for pulse width modulation driven by a clock signal. The pulse width modulated signal is low pass filtered to derive an analogue sinusoidal wave and passed into a quadrature frequency converter where it is processed by an analogue mixer

driven by an LC oscillator yielding the desired high frequency output signal. Hence this block acts as VCO which has the feature that its oscillating frequency is controlled by the input control bits.

The delta-sigma converter and its associated low-pass filtering form the main part of this specific project. The details of the blocks making up DCFM is explained in the next coming sections.

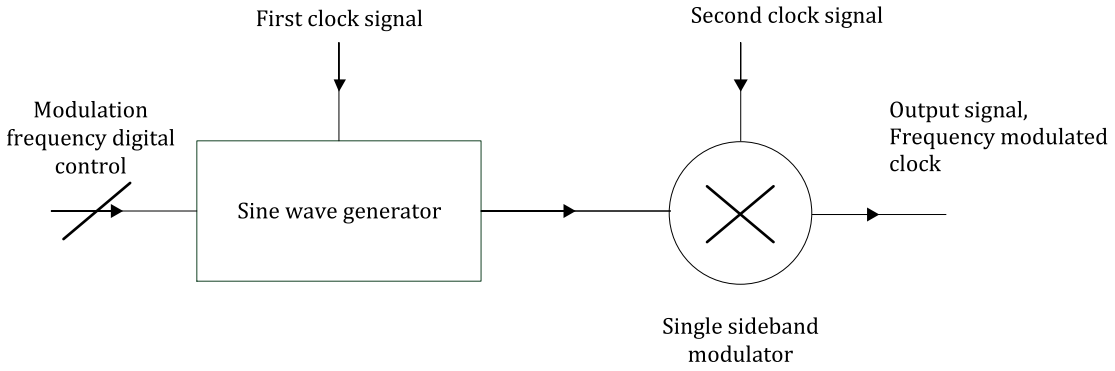

Figure 3.3: Digitally controlled frequency modulator

3.4.1 Sine wave generator

The phase error coded as digital bits is utilized for the sinusoidal generation. Sine wave generator (figure 3.4) generates sinusoidal by consulting and regenerating from a look-up-table in memory. However for simulation purpose a sinusoidal is actually generated whose frequency is determined by the output bits of signal processor. The minimum frequency resolution is 10Hz and hence a 5 bit digital input will correspond to a maximum of 320Hz of difference between the input reference and the fed-back signal. In-phase and the corresponding quadrature phase sinusoidal is generated for the inputs of the quadrature frequency converter. The correction frequency i.e. whether the output sine wave has to be added to or subtracted from the local oscillator frequency of frequency converter is conveyed by swapping the in-phase and the quadrature phase signals.

3.4.2 Quantizer

The delta-sigma modulator essentially requires the input signal to be quantized at a much higher rate than the Nyquist frequency which can be as high as 64, 128 times. To obtain high resolution bit pattern of sinusoidal a high frequency signal of 2MHz is used to quantize the sine generated.

3.4.3 Encoder

The quantized output is now encoded onto a 10 bit digital number which will act as the input to the delta-Sigma DAC.

3.4.4 Delta-Sigma digital-to-analogue modulator

The digital-to-analogue conversion is performed by the delta-sigma modulator required for high resolution conversion and is of second-order, with a 1-bit quantizer and oversampling ratio(M) 128. The digital components being the subtracter, integrator, comparator and the digital-to-digital converter are of 24 bits wide. It employs a clock signal whose frequency is much higher than the Nyquist rate, generally 64 or 128 times the baseband signal. It performs the DAC operation by utilising the input digital bits and generating a high frequency pulse width modulated wave. It essentially shapes the quantization noise to higher frequencies which can be subsequently filtered out of the baseband signal yielding a jitter free signal.

3.4.5 Low pass filter

The modulated wave is low-pass-filtered to eliminate the quantization noise, shaped to higher frequencies and also accomplishes analogue regeneration of sinusoidal wave. Sallen-Key topology is incorporated to achieve low-pass filtering which implements second-order active filters. This circuit acts a unity gain amplifier which has a very high input impedance and low output impedance.

3.4.6 Quadrature frequency converter

In several applications, frequency multiplication is employed where in an output signal is generated whose frequency is harmonic of the input signal. In this specific PLL, apart from frequency multiplying the input reference signal to 2.5 GHz, the frequency multiplier has to also "*mix*" the correction frequency with the input signal. Hence a quadrature

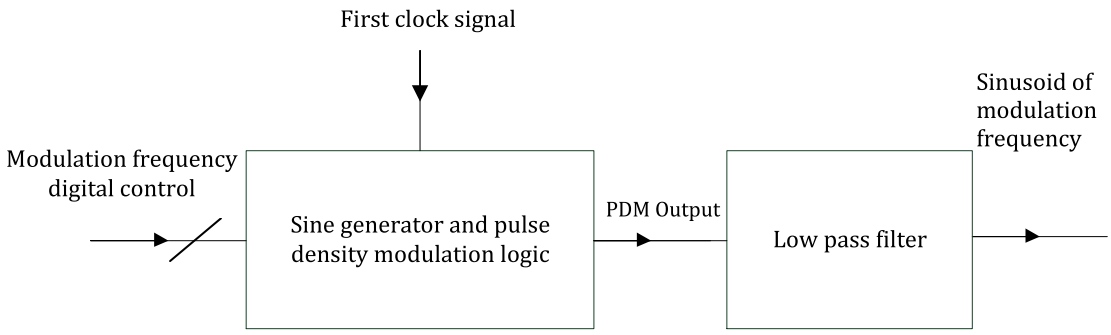

Figure 3.4: Sine wave generator using pulse width modulation

frequency converter is employed to accomplish this functionality.

The quadrature frequency converter uses two mixers for frequency synthesis. One of the frequency is the desired output frequency (2.5GHz in this specific system) and the other is the error frequency to be either added or subtracted.

A mixer is a non-linear device, which performs a frequency conversion, either up or down, of two input frequencies to one mixed output. They are a class of multipliers because they can multiply their two inputs. One of these inputs is a local oscillator (LO), which usually has a fixed frequency. The other input and output frequency names depend on the way the conversion is performed. For up-conversion the second input is the intermediate frequency (IF) that can vary in a given range. The mixed output signal is then called the radio frequency (RF). For down-conversion the two names are the other way round, as then the second input has a higher frequency than the output, which is also usually in the RF region.

Given the LO and IF inputs of an up-converting multiplier are sinusoidal signals. Then they can be described by,

$$v_{LO}(t) = V_{LO}.Cos(\omega_1 t) \tag{3.1}$$
$$v_{IF}(t) = V_{IF}.Cos(\omega_s t) \tag{3.2}$$
$$\tag{3.3}$$

The resulting signal on the RF port is then,

$$v_{RF}(t) = V_{LO}.V_{IF}Cos(\omega_1 t + \phi_1).Cos(\omega_2 t + \phi_2) \tag{3.4}$$
$$v_{RF}(t) = \frac{V_{LO}.V_{IF}}{2}(Cos(\omega_1 t - \omega_2 t) + Cos(\omega_1 t + \omega_2 t) \tag{3.5}$$

The result term includes a difference frequency and a sum frequency. These terms are responsible for either down-conversion or up-conversion.

3.5 Analogue-to-digital converter

The output derived from the frequency converter is analogous in nature and hence to facilitate comparison with the input reference signal which is a digital clock, a analogue-to-digital converter is incorporated.It compares the input voltage to a reference value and outputs either a digital ”1” or ”0”.

3.6 Frequency divider

In case the desired output signal needs to be much higher than the input reference signal, a frequency divider is added in the feedback path which divides the output frequency by

the quantity(500 in this system) to be compared with that of the input reference signal.

The key design technique in the whole system of PLL is to keep the loop bandwidth as low as possible to minimise noise interference.

The analogue low-pass filter is implemented using 180nm CMOS process(at transistor level) in Cadence whereas the remaining blocks are implemented in VerilogA(hardware descriptive language).

The verilogA offers several advantages being, the simulation of system-level designs and complex mixed signal circuits can be accomplished with great ease and great speed. It also offers easy debugging and reusable ability. [10]

Chapter 4

Delta-sigma modulators

The powerful digital signal processors used for telecommunications require high-resolution A/D or D/A converters. However, the quantizer introduces error which shows up as noise in the resulting signal. Furthermore they are heavily constrained by higher frequency sampling rates, required for improved performance (maximum sampling rate till then was Nyquist rate). To overcome such drawbacks, the concept of oversampling was introduced which reduced in-band quantization noise to achieve a high degree of resolution.

How is it achieved? The delta sigma modulator translates a N-bit PCM signal into a 1-bit fast data stream with few parallel bits. Fundamentally, $\Delta\Sigma$ modulators re-quantize high resolution input to a lower resolution. Because a 1-bit output is extremely easy to implement in hardware and there are ways to make that one-bit output have the SNR of an N-bit converter. This calls for oversampling the input data stream. The output 1-bit data stream encodes the input value within its average
[12].

In the oversampling converters, the sampling frequency is kept much higher than the Nyquist rate called as the oversampling ratio (M),typically higher by a factor between 8 to 512 and generate each output utilizing all preceding input values. This gives the extra dynamic range (due to extra bits of resolution). Furthermore, this same extra bit of resolution can be obtained at lower sampling rates by spectrally shaping the quantization noise over a larger frequency range through the use of negative feedback.

Definitions:
f_B = analog signal bandwidth
f_N = Nyquist frequency (two times f_B)
f_S = sampling frequency
$M = \frac{f_S}{f_N} = \frac{f_S}{2f_B}$ = oversampling ratio

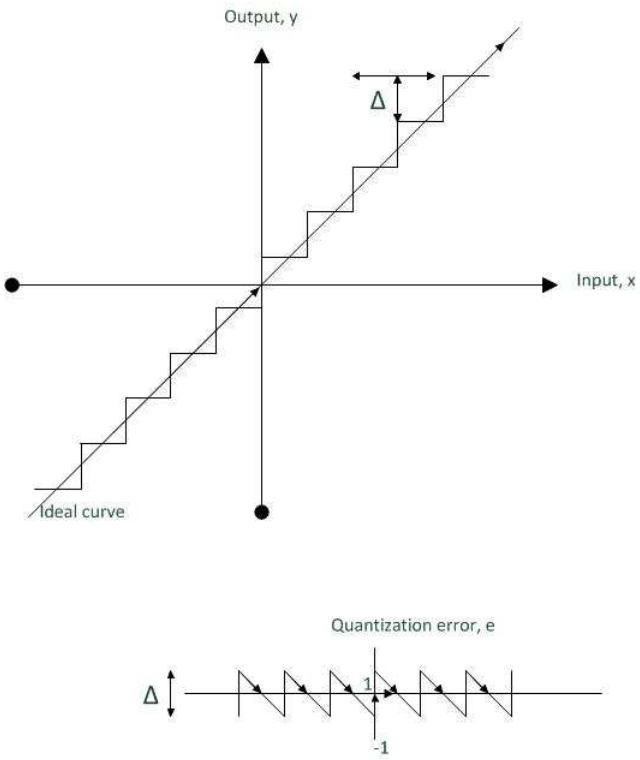

Figure 4.1: Quantization error graph

4.1 Quantization noise

A quantizer can be modelled as adding quantization error e(n) to input x(n) to generate output y(n), i.e., y(n) = x(n) + e(n), where n refers to n-th sample. The output signal is equal to the closest quantization level value. The quantization error is the difference between the input and output values, which is bounded by $\pm\Delta/2, where\Delta$ equals the difference between two adjacent quantization levels. The quantization levels and quantization error are shown in figure 4.1.

The mean square value of the quantization error is,

$$e_{rms}^2 = S_Q = \frac{1}{\Delta}\int_{\frac{-\Delta}{2}}^{\frac{\Delta}{2}} e(x)^2\,\mathrm{d}x = \frac{\Delta^2}{12} \tag{4.1}$$

From equation 4.1, it can be seen that the quantization noise power is independent of sampling frequency and hence our noise assumption and the subsequent analysis holds good.

The spectral density of the sampled noise is,

$$E(f) = e_{rms}\sqrt{\frac{2}{f_S}} = e_{rms}\sqrt{2\tau} \tag{4.2}$$

where $\tau = 1/f_S$
The in-band noise energy n_0 is

$$n_0^2 = \int_0^{f_B} E^2(f)\mathrm{d}f \tag{4.3}$$

$$n_0^2 = e_{rms}^2(\frac{2f_B}{f_S}) = \frac{e_{rms}^2}{M} \tag{4.4}$$

$$n_0 = \frac{e_{rms}^2}{\sqrt{M}} \tag{4.5}$$

It can be shown that maximum SNR can be given by,

$$SNR_{max} = 10log(\frac{P_s}{P_e}) = 6.02N + 1.76 - 5.7 + 30log(M) \tag{4.6}$$

Hence it can be observed that doubling the oversampling ratio M, decreases in-band noise by a factor of only $\sqrt{2}$ which corresponds to -3dB. This property is exploited by oversampling converters, since when an oversampled signal is quantized, the spectral components of the quantization error are distributed in a larger frequency band[7].To obtain much higher dynamic range, noise shaping through the use of feedback can be used [6].

Since the total in-band noise power is reduced, the number of "$effective$" bits is increased from the actual bits.

While the most types of converters result in quantization noise of white spectrum, delta-sigma converters shape the noise to higher frequencies which can be easily filtered out. This is the main advantage of $\Sigma\Delta$ converters.

The oversampling converters requires considerable amount of digital circuitry in addition to some analogue stages. The accuracy requirements on the analogue components are relaxed which considerably reduces the cost. The inclusion of digital circuitry tends to make system faster and cheaper.

4.2 First-order, Delta-sigma modulator

It can be recalled that oversampling alone is not an efficient way to modulate, rather a more efficient way is to adopt a noise-shaping sigma-delta modulator. Such a system incorporates a negative feedback. Furthermore, it is also essential to develop a system which should act as a amplifier for the baseband signal (devoid of noise in that range of frequency) and ignore the noise at higher frequencies where its gain is low[5]. The two linear inputs being the signal and the noise can be defined as,

Signal transfer function = STF $=\frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)}$
Noise transfer function = NTF $= \frac{Y(z)}{X(z)} = \frac{1}{1+H(z)}$

The filter which shapes the quantization error to higher frequency band is called NTF whose transfer function is given by equation 4.2 which can be either a low-pass or band-pass[7].

From above equations it can be observed that when H(z) goes to infinity, NTF will go to zero. To noise-shape the quantization noise in a useful manner, H(z) is chosen such that its magnitude is large from 0 to f_B and also STF will tend to unity in the frequency band of interest. The NTF will tend to zero in the same band of frequency. Thus the quantization noise is reduced over the frequency band of interest while signal remains unaffected[6].

The maximum level of input signal should be well within the feedback signal, otherwise the large signal will saturate the input signal.

The H(z) for first order noise-shaping modulator can be defined as,

$$H(z) = \frac{1}{z-1} \tag{4.7}$$

A block diagram for such a transfer function is as shown in figure 4.2.

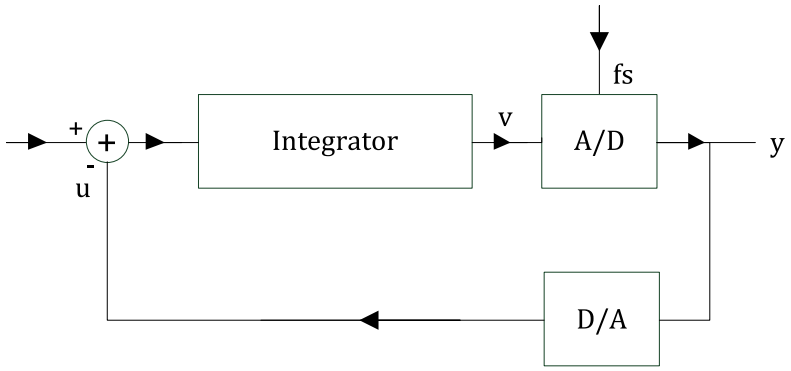

Figure 4.2: Block diagram of First Order Sigma Delta modulator

4.3 Sampled-Data model of a First-order ΣΔ Modulator

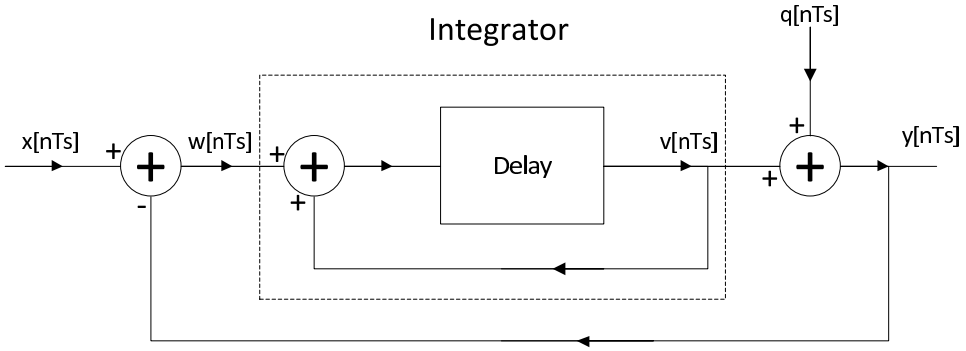

Figure 4.3: Detailed block diagram of First-Order Delta Sigma modulator

The qualitative understanding of the delta-sigma operation can be explained referring to the figure 4.3. Quantization noise is added to the input for the better comprehension. The output of the delta-sigma modulator depends not only on the present value of the input but also of the previous values and it produces a bit stream, the average level of which represents the input signal level. The integrator (comprising of a delay element with a feedback) acts as a comparator between the present values and the previous and outputs a low if present value is lower than the previous value. The quantizer is a 1-bit quantizer which brings about the linearity between the two levels [2]. The feedback reduces the effect of noise in the closed loop at low frequencies (ideally the signal bandwidth). To analyse the functionality of the block the signal and noise transfer functions is derived.

From the figure 4.3, the relationship between output and the input is derived as,

$$y[nT_s] = q[nT_s] + v[nT_s]$$
$$v[nT_s] = w[(n-1)T_s] + v[(n-1)T_s]$$

Therefore,

$$y[nT_s] = q[nT_s] + w[(n-1)T_s] + v[(n-1)T_s]$$
$$= q[nT_s] + x[(n-1)T_s] - y[(n-1)T_s] + v[(n-1)T_s]$$

But the first equation can be written as,

$$y[(n-1)T_s] = q[(n-1)T_s] + v[(n-1)T_s]$$

Substituting this relationship into the above gives,

$$y[nT_s] = x[(n-1)T_s] + q[nT_s] - q[(n-1)T_s] \tag{4.8}$$

From the equation 4.8, it can be observed that the output is the delayed version of the input and a differentiated version of the quantization error. This structure does not require a demodulation filter(since the input remains unaffected by the modulation process), the amplification of the in-band noise is prevented. Furthermore the differentiation of error is further suppressed by the high sampling rate frequency. If the integrator has high gain(compared to feedback path consisting of quantization noise), the in-band noise is strongly attenuated thereby delivering the noise to be shaped out to higher frequencies[8].

Converting the equation 4.8 into Z domain,

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z) \tag{4.9}$$

It is clear from equation 4.9 that the signal $X(z)$ passes through unmodified while the quantization noise $Q(z)$ is modified by the term $1 - z^{-1}$.

The two terms can be now re-defined as,

$$Signaltransferfunction = STF = \frac{Y(z)}{X(z)} = z^{-1} \tag{4.10}$$

$$Noisetransferfunction = NTF = \frac{Y(z)}{X(z)} = 1 - z^{-1} \tag{4.11}$$

$$\tag{4.12}$$

From the equations 4.11 and 4.12 it can be observed that, the NTF has now indeed zeros at the origin resulting in high-pass transfer function. This high-pass characteristics reduces the noise at low frequencies which is the key to obtain extra dynamic range within the bandwidth of converter[1].

The feedback forces the average value of the quantized output y(n) to equal the average value of input x(n) so that the integrator's input x(n)- y(n) equals zero (otherwise, the infinite dc gain will amplify the difference to infinity).

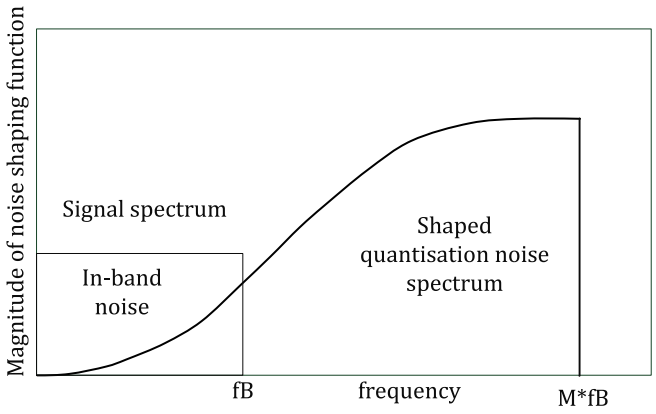

Figure 4.4: Spectrum of "shaped" noise

The figure 4.4 shows how the noise is "*spectrally*" shaped out of frequency band of interest.

4.4 Delta-Sigma Digital-to-Analogue Converter

Before proceeding to the architecture of delta-sigma DAC, the simple process of delta-sigma modulation of 1st order is explained with the help of table 4.1,

The table 4.1 shows the simple operation of a sigma-delta 1st order modulator. Assuming the input ranges from "0" or "16", the input signal along with the output of subtracter(shown in column 1) is subtracted by either lowest or highest number of the range i.e. by either "0" or "16" according to the output of the comparator. The integrator which comprises of an adder and a latch integrates the previous value with the present input. The output of the comparator is either "0" or "15" when compared with mid-range value i.e. less than or more than "8". This can be verified from column 3 of the table. The pattern of the comparator output has an amazing property. Its average value is equal to the value at the input of the modulator! i.e. "13". Hence by devising a circuit which can compute the average value of the delta-sigma modulator output, the input signal can be

Table 4.1: Simple operation of 1st order delta-sigma modulator

Input signal					Integrator				Comparator
13	-	0	=	13	0	+ 13	=	13	1
13	-	16	=	-3	13	+ -3	=	10	1
13	-	16	=	-3	10	+ -3	=	7	0
13	-	0	=	13	7	+ 13	=	20	1
13	-	16	=	-3	20	+ -3	=	17	1
13	-	16	=	-3	17	+ -3	=	14	1
13	-	16	=	-3	14	+ -3	=	11	1
13	-	16	=	-3	11	+ -3	=	8	1
13	-	16	=	-3	8	+ -3	=	5	0
13	-	0	=	13	5	+ 13	=	18	1
13	-	16	=	-3	18	+ -3	=	15	1
13	-	16	=	-3	15	+ -3	=	12	1
13	-	16	=	-3	12	+ -3	=	9	1
13	-	16	=	-3	9	+ -3	=	6	0
13	-	0	=	13	6	+ 13	=	19	1
13	-	16	=	-3	19	+ -3	=	16	1

reproduced without any undesired modification.

It can be observed that although the input signal range from ”0” to ”16” the output of the integrator stretches itself outside the range. Hence while designing the bus width of the digital sigma-delta system it has to be ensured that the number of bits should accommodate the integrator output.

The delta-sigma modulator implemented in this project is a DAC and is as shown in the figure 4.5. It is a first order loop containing an integrator, 1 bit comparator and digital-to-digital converter.

The DAC implemented comprises of a subtracter, digital integrator comprising an adder and latch, a comparator and a digital-to-digital converter, all of which are 15 bits wide i.e. ranging from $0 : 14$. However, the input is restricted to 10 bits to accommodate the integrator output. As observed from the table 4.1, the process of sigma-delta modulation involves negative numbers also, hence a suitable signed number representation has to be chosen. Simple sign-and-magnitude method is adopted for ease of implementation. The 15th bit is the sign bit where a $'1'$ represents a negative number and a ’0’ positive number. Also observed from the table 4.1 is that the output of the integrator can go beyond the actual range of input due to the inherent property of integration, hence additional 4 bits are provided. Hence the input signal will be restricted to 10 bits ranging from 0 to $1023(2^9)$.

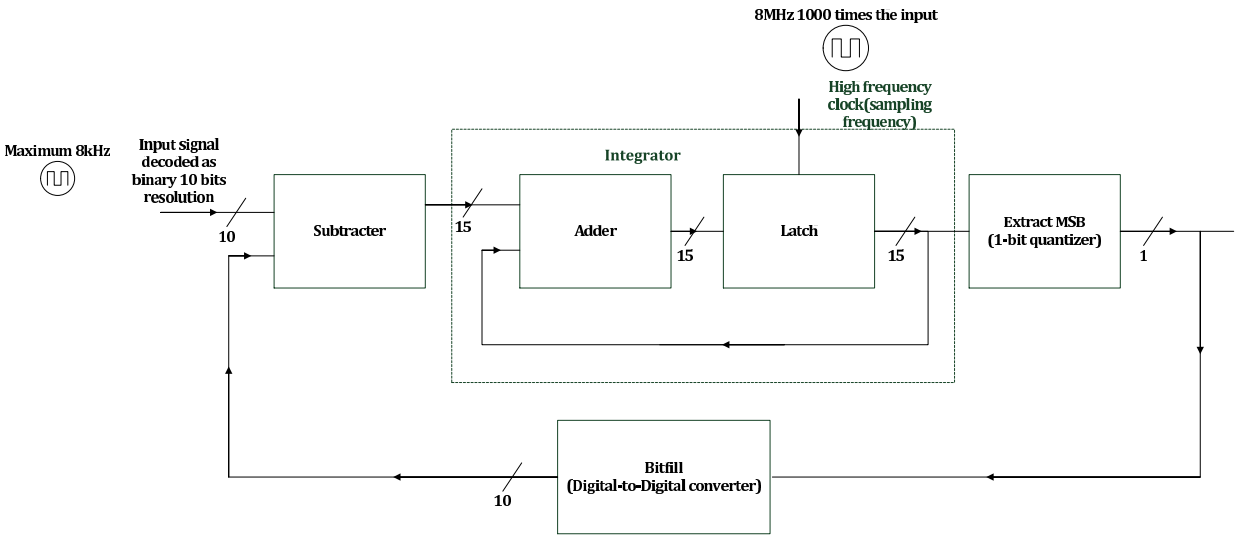

Figure 4.5: Block diagram of first order sigma-delta modulator for DCFM

The subtracter either subtracts a $'0'$ or $'1023'$ from the input number. Two's complement is employed to undertake the subtraction. The sign bit is updated accordingly.

The adder also employs two's complement for addition of a negative number to a positive number or vice-versa, otherwise the two positive numbers are added using digital logic.

The latch clocks the previous input to the adder to implement an integrator.

The comparison of the integrator output with the mid-range value is realized by extracting the MSB bit of the 10 bit numbers. The output is '1' if any bit above 8th bit is high and sign bit is low. Its a '0' if sign bit is high or MSB bits are low.

The digital-to-digital converter performs bit-fill operation i.e. a '1' on MSB bit of PWM signal appends all the 10 bits of input signal to '11111111' and same as for a '0'.

A DAC converts the digital logic to Vmax and -Vmax, which in this case is 2.5 V to 0 V.

The simulation results are as shown in figure 4.6. The trace named "*sine*" is the 8KHz sine wave representation, which utilises a clock signal of frequency 8.192 MHz for modulation(in green trace) whose PWM output is shown in trace named "$PDMOut$" and which is low-pass filtered(LPF2). The first trace is the plot of Nyquist converter output for the same given input signal to enable comparison.

Conventional converters sample the input signal at Nyquist rate. Essentially this sampling frequency is 4 to 5 times the input signal. To enable comparison of the Nyquist converters and the delta-sigma modulators, both are fed on their inputs identical frequency signals and conversion carried out. Such a simulation results is as shown in the figure 4.7.

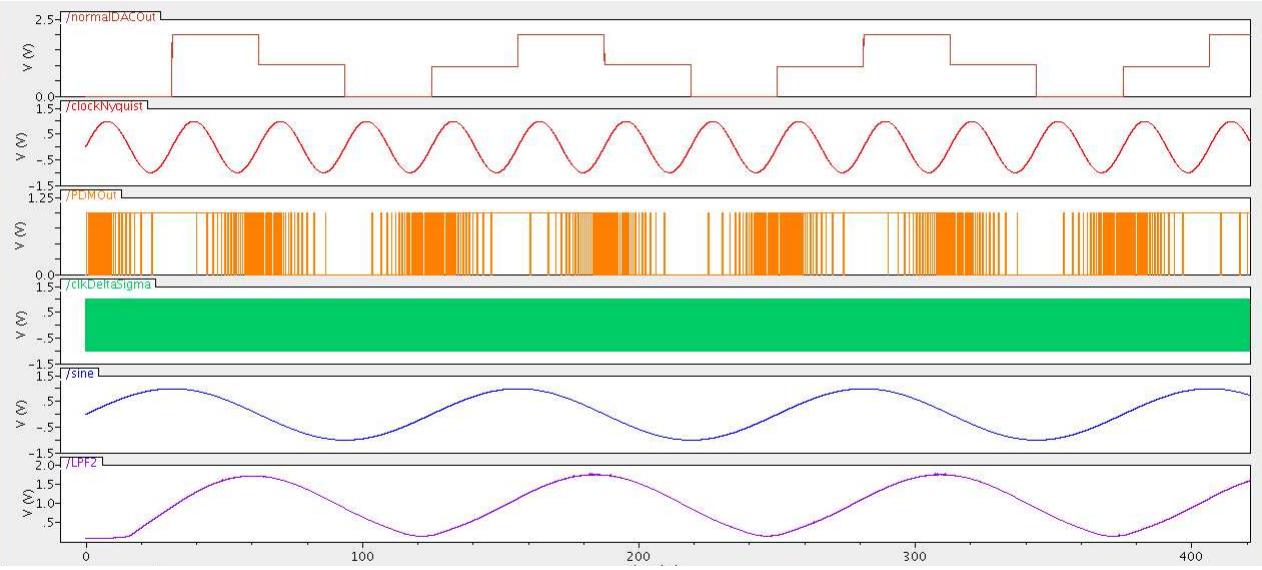

Figure 4.6: First order delta-sigma DAC simulation results

The blue trace shows the frequency plot of the delta-sigma modulator and it can be seen that the noise shaping is evident upto the sampling frequency. The frequency components in the vicinity of the baseband signal(8 kHz) are attenuated by shaping out the noise frequency components to higher frequencies. The red trace shows the frequency spectrum plot of the Nyquist converter and it can be seen that visible frequency components present in the vicinity of the baseband signal. The frequency spectrum of subsequent low-pass filtering of the PWM wave is as shown in the figure 4.8 and as pointed on the trace, lower-left corner shows that frequency components above 10KH are filtered out.

4.5 Classification of delta sigma modulators

The performance of the $\Delta\Sigma$ modulators can be improved by adopting various strategies which can be listed as,

- Increasing order(L) of the integrator thus the order of the modulator.
- Increasing the oversampling ratio(M).
- Increasing the number of bits.

Various factors affect the choice of strategy employed. These depend on the nature of signals handled whether low pass or band pass(figure 4.9)), number of bits and levels of quantizer[7].

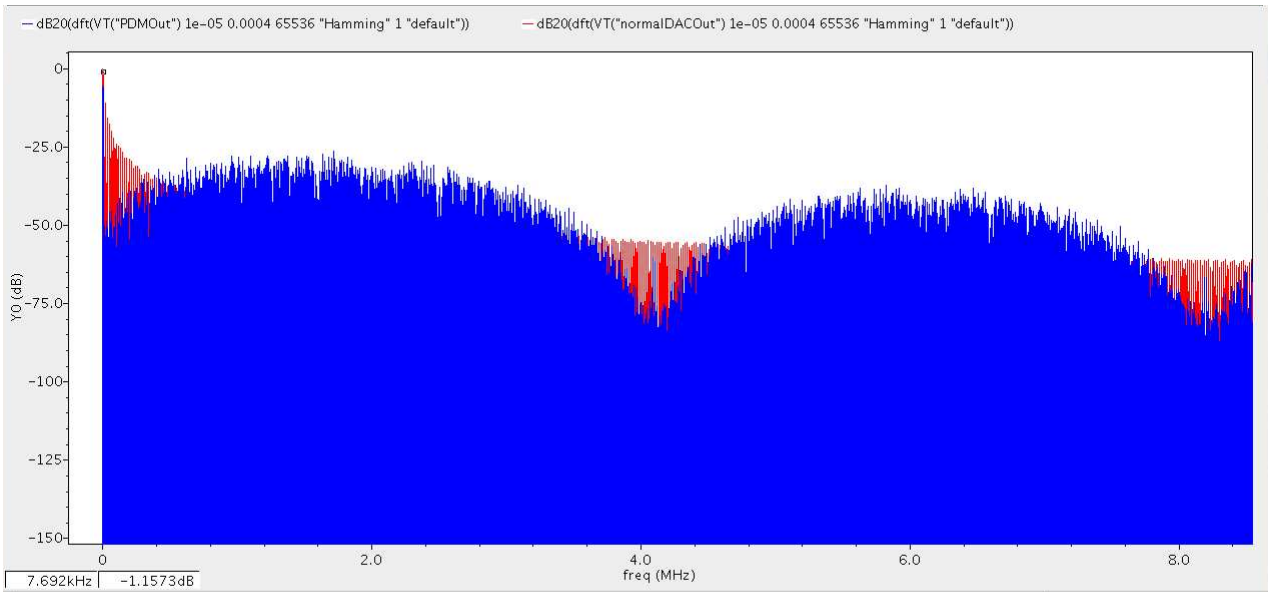

Figure 4.7: Comparison results of delta-sigma and the Nyquist converters

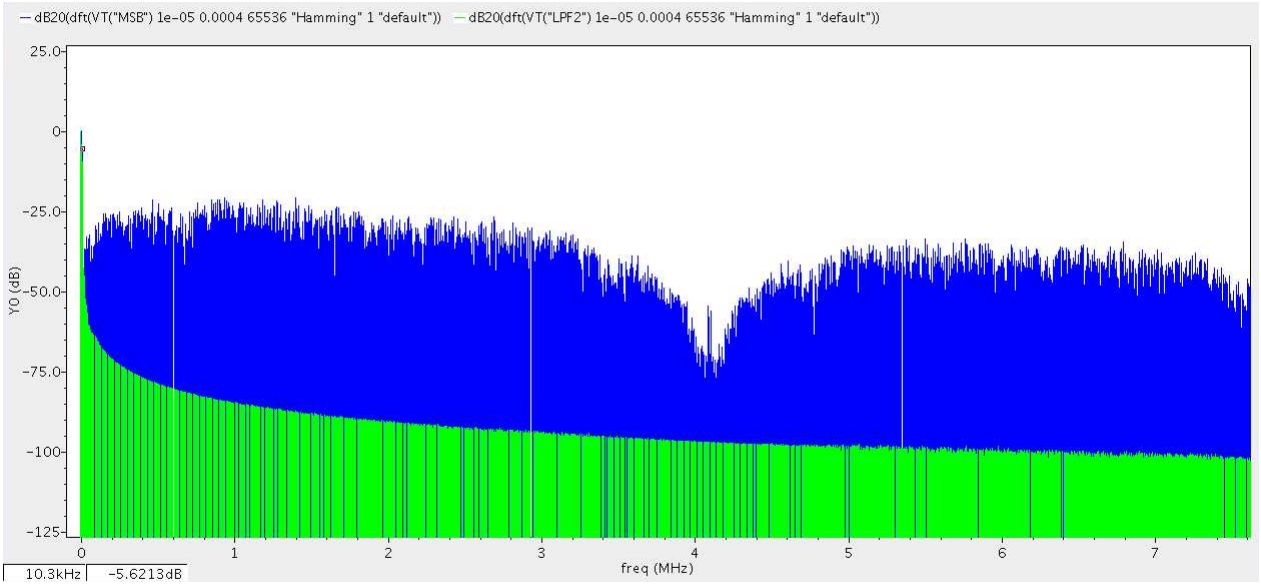

Figure 4.8: Low-pass filtering of the delta-sigma modulated wave

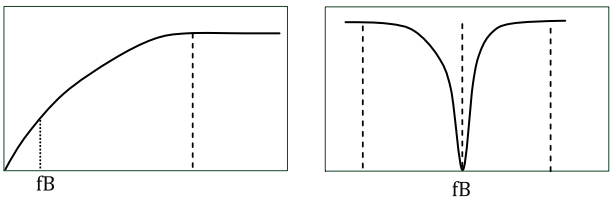

Figure 4.9: Low pass and band pass $\Delta\Sigma$ modulators

Since the input generated for $\Delta\Sigma$ modulator is of frequency down to 0Hz, a low pass $\Delta\Sigma$ modulator is employed. A 1-bit quantizer is used since it is easily implemented in hardware and a second order integrator serves as compromise between accuracy and increased complexity.

4.6 Higher order Sigma-Delta Modulators

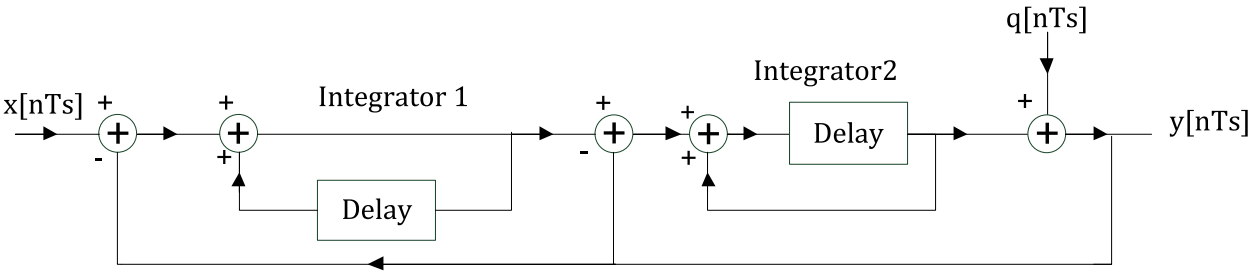

Figure 4.10: Second order sigma delta modulator

The figure 4.10 shows the second order sigma delta modulator, so called due to its two integrators connected in series. Its STF and NTF can be given as,

$$STF = z^{-1} \tag{4.13}$$

$$NTF = (1 - z^{-1})^2 \tag{4.14}$$

And the modulator output is given by,

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 Q(z) \tag{4.15}$$

In general, L-th order $\Sigma\Delta$ modulator has the following form,

$$Y(z) = z^{-K}X(z) + (1 - z^{-1})^L Q(z) \tag{4.16}$$

K, depends on the architecture where K<L.

The noise transfer function can be written as,

$$NTF_Q(z) = (1 - z^{-1}) \tag{4.17}$$

By replacing z by $e^{j\omega T_s}$ it can be shown that,

$$Magnitude of NTF = (2sin\Pi f T_s) \tag{4.18}$$

The equation 4.18 is magnitude of noise transfer function.

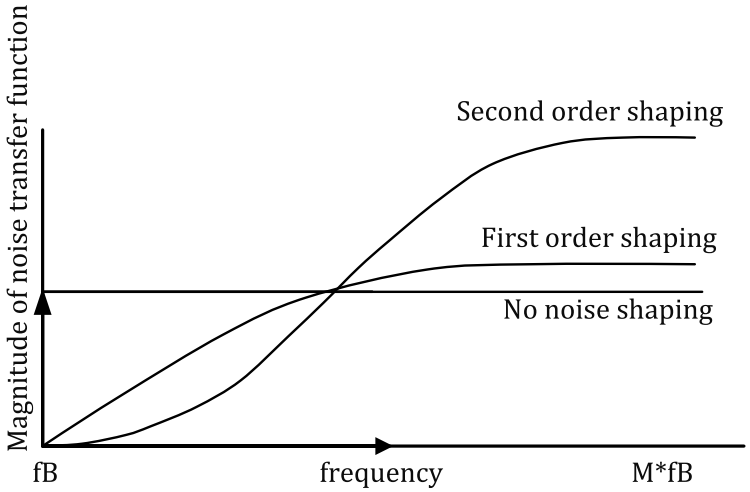

Figure 4.11: Noise power comparison of higher order modulators

The maximum SNR for second order sigma-delta modulator can be given by,

$$SNR_{max} = 10log(\frac{P_s}{P_e}) = 6.02N + 1.76 - 12.9 + 50log(M) \tag{4.19}$$

The graph 4.11 is the qualitative analysis of the equation 4.18. It can be observed from equation 4.19 and from the figure 4.11 that doubling of M improves the SNR for a second-order modulator by 15 dB[1].

As discussed in section 4.1, we have assumed the noise to be white and the power spectral density of the modulator $S_E(f)$ is,

$$S_E(f) = NTF_Q(f)^2 \frac{S_Q(f)}{f_S} \tag{4.20}$$

Integrating $S_E(f)$ over the signal band to get the inband noise power using $S_Q = \frac{\Delta^2}{12}$,

$$S_B = \frac{1}{f_S} \int_{f_B}^{-f_B} (2 \sin \Pi F T_S) 2L \frac{\Delta^2}{12} \tag{4.21}$$

Evaluating the above equation, in-band rms noise is given by,

$$n_0 = \sqrt{S_B} = \Big(\frac{\Pi^L}{\sqrt{2L+1}}\Big)\Big(\frac{1}{M^{L+0.5}}\Big) e_{rms} \tag{4.22}$$

where L = order of the modulator.
Hence $n_0 \propto \frac{e_{rms}}{M^{L+0.5}}$.

Doubling of M leads to a $2^{L+0.5}$ decrease of in-band noise resulting in an extra L+0.5 bits of resolution![1]

The second order delta-sigma digital-to-analogue comprises two integrators as shown in figure 4.12. Due to double integration, the output of the last integrator can go far beyond the input range and hence to accommodate such extensive calculations 24 bit wide bus is adopted. A clock signal of frequency, same as that used in the first order(8MHz) is utilised to enable comparison between the modulators of two orders.

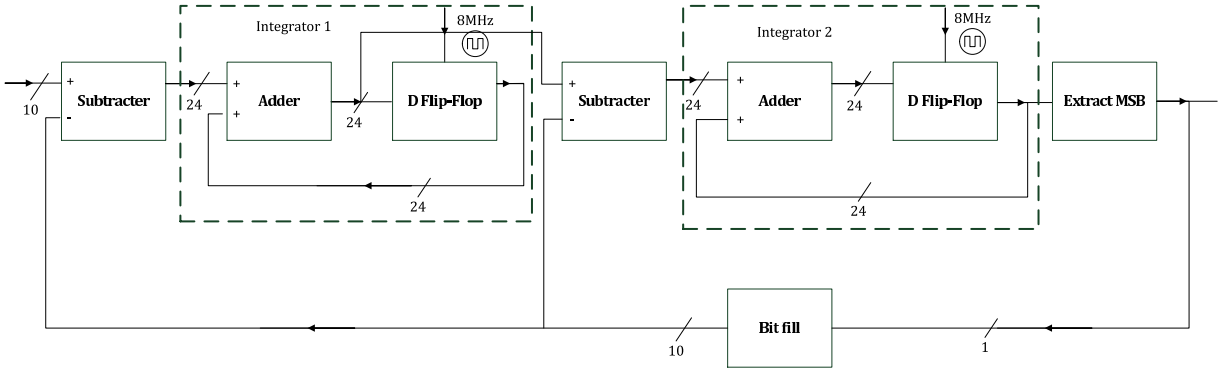

Figure 4.12: Comparison of first and the second order delta-sigma modulator

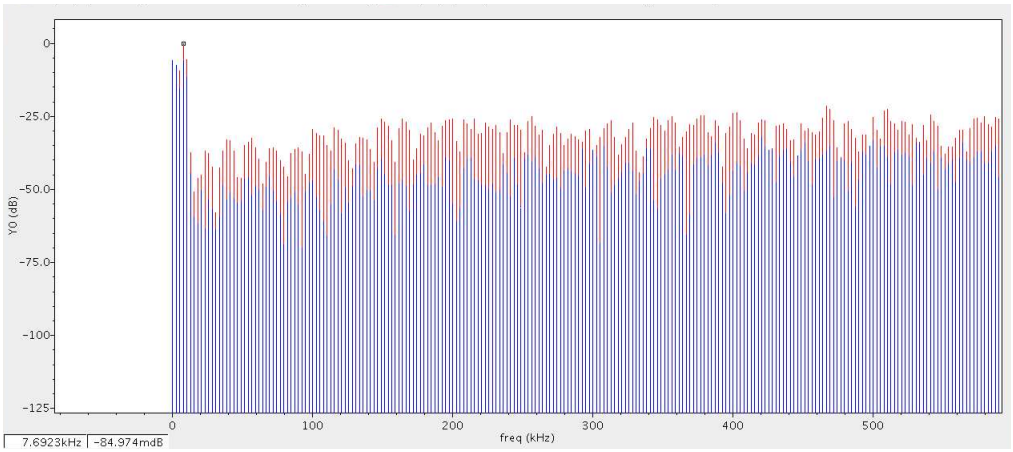

Figure 4.13: Comparison of first and the second order delta-sigma modulator

The figure 4.13 shows the comparison between the first and the second order delta-sigma modulators. The red and the blue trace shows the frequency components of the second and the first order delta-sigma modulators. It can be seen that second order modulator shapes larger number of noise frequencies to higher frequencies for the same clock frequency.

The comparison results of different oversampling ratios is as shown in the figure 4.14. The blue trace(frequency spectrum of PWM wave using M value as 8MHz) suppresses side-

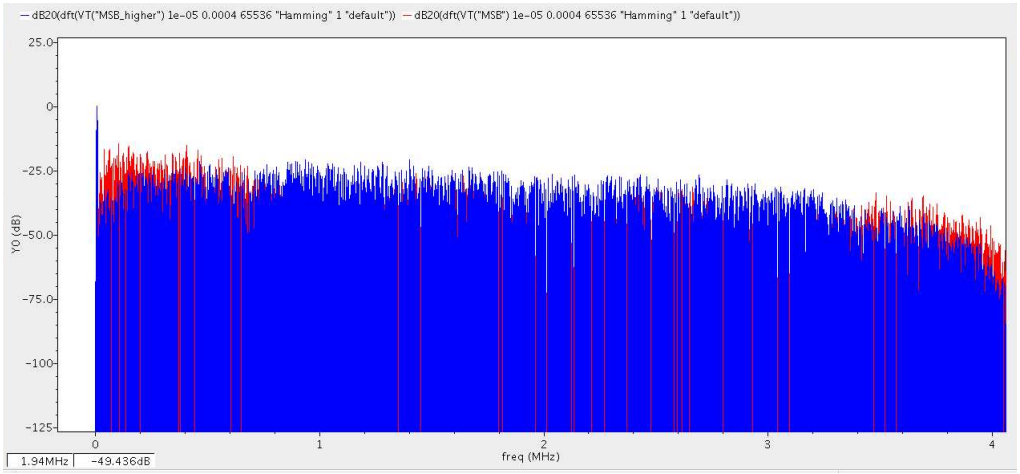

Figure 4.14: Comparison of modulators employing 1MHz and 8MHz clock as oversampling ratio

band frequencies better than that of modulator using 1MHz as oversampling ration(red trace).

Hence it can be concluded that $\Delta\Sigma$ modulators constitutes best technique for conversion and also offers several features from which the performance can be further improved.

Chapter 5

Active low pass filter

The pulse width modulated signal derived from the delta-sigma modulator is converted to a sinusoidal using an analogue low pass filter. Furthermore the low-pass filter also remove the undesired higher frequencies for which an active low-pass filter is used. The advantage of using an active low pass filter with a unity buffer operational amplifier is that the op-amps has high input impedance preventing excessive loading on the filters output while its low output impedance prevents the filters cut-off frequency point from being affected by changes in the impedance of the load. More specifically a second-order filter is used to attain a steeper stop-band roll-off as compared to first order filters.

A Sallen-Key topology is incorporated which implements second-order active filter. This circuit acts a unity gain amplifier which has a very high input impedance and low output impedance.

The key advantage of this circuit which is especially relevant to obtaining low-noise signal is that it has sharp "*knee*" transition. This topology implements a 2-pole filter and this inherent property aids to reduce the interfering signal without degrading the desired signal. Further, cascading several stages can offer a steep attenuation curve with a very sharp knee. Also, since it is a unity gain amplifier the power consumption is drastically reduced due to absence of resistors in the feedback path.

5.1 Design of Sallen-Key low-pass filter

The transfer function of the circuit in the figure 5.1 is given by,

$$\frac{vout}{vin} = \frac{Z_3 Z_4}{Z_1 Z_2 + Z_3(Z_1 + Z_2) + Z_3 Z_4} \tag{5.1}$$

Equation 5.1 is the form of second order filter.

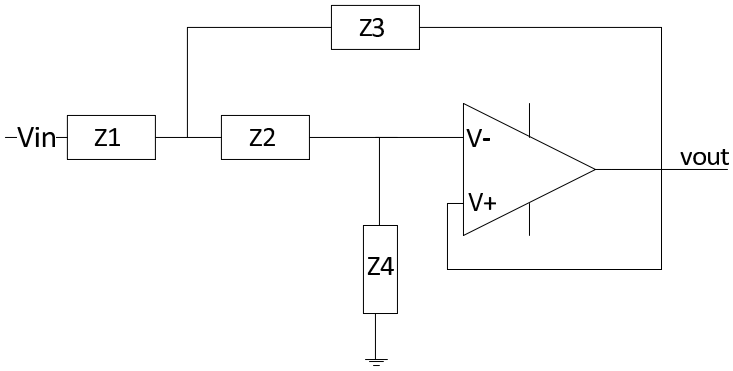

Figure 5.1: Sallen-key generic circuit

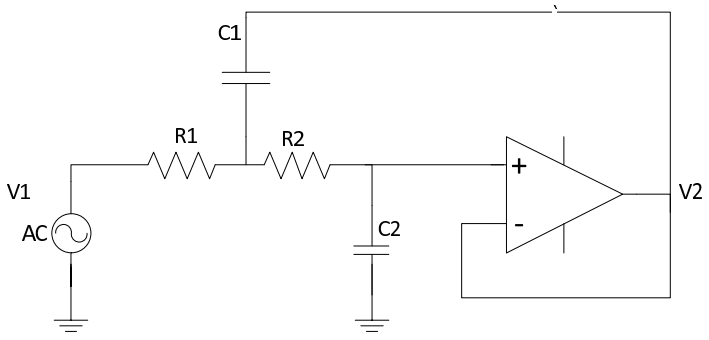

Figure 5.2: Sallen-Key topology

The Sallen-Key low pass filter has components R1, R2, C1 and C2 configured as shown in the figure 5.2.

The operation can be described qualitatively as follows:
At low frequencies,C1 and C2 act as open circuits and the signal is simply buffered to the output.
At high frequencies, C1 and C2 act as short circuits and the signal is shunted to ground at the amplifiers input, the amplifier amplifies this input to its output, and the signal does not appear at Vo. Near the cut-off frequency, where the impedance of C1 and C2 is on the same order as R1 and R2, positive feedback through C2 provides Q enhancement of the signal.

This circuit is a non-inverting op-amp, the ratio of output and input voltages always remaining a constant K which is,

By applying Kirchoff's law it can shown that the transfer function in terms of circuit elements is given by,

$$\frac{V_2}{V_1} = \frac{1/R_1R_2C_1C_2}{s^2 + (1/R_1C_1 + 1/R_2C_1 + 1/R_2C_2 - K/R_2C_2)s + 1/R_1R_2C_1C_2} \tag{5.2}$$

Equation 5.2 can be compared to the second order transfer function of a low-pass filter given by,

$$H(s) = \frac{\omega_0^2}{s^2 + s(\frac{\omega}{Q}) + \omega_0^2} \tag{5.3}$$

Comparing equation 5.2 and 5.3, equations for ω_0 and "Q" can be derived as,

$$\omega_0^2 = \frac{1}{R_1R_2C_1C_2} Q = \frac{\omega_0 R_1R_2C_1C_2}{(R_1 + R_2)C_2} \tag{5.4}$$

Given ω_0, setting $R_1 = R_2 =$ R and choosing a convenient C_1, C_2 can be calculated [9].

For a cut-off frequency 15kHz, the value of design parameters derived are $R_1 = R_2 =$ 50K ohms and $C_1 = C_2 =$ 213 pF yielding the schematic as shown in the figure 5.3.

Low-pass filtering of 8kHz is achieved and is shown in the figure 5.4 after undertaking AC analysis.

The transient response of the two analogue low-pass filters connected in series is shown in the figure 5.5. The blue trace is the output of first low-pass filter which converts the PWM wave to a sinusoidal and the second low-pass pass filter(output of which is shown in purple trace) smooths the output of the first low-pass filter. Owing to the RC circuit in

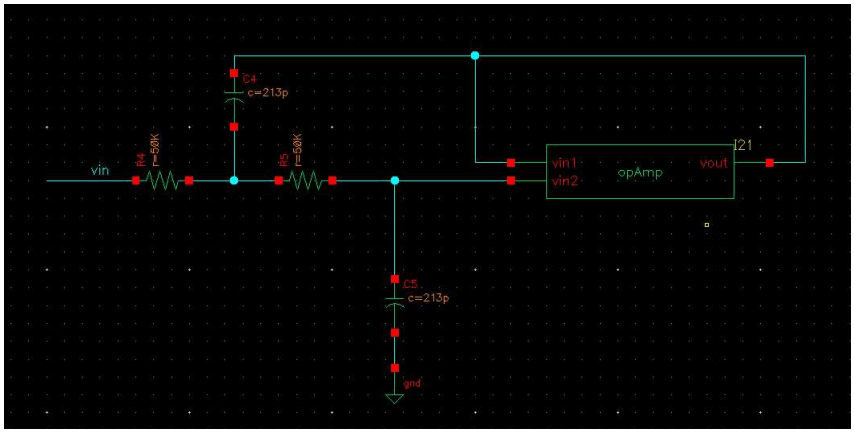

Figure 5.3: Sallan-Key topology

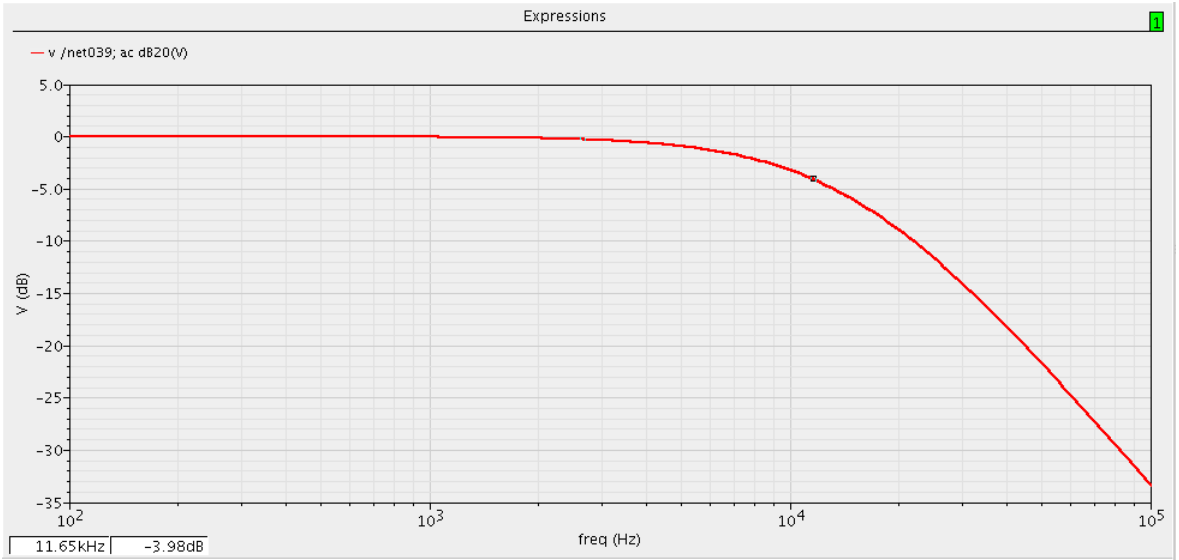

Figure 5.4: AC simulations of Sallen-Key topology

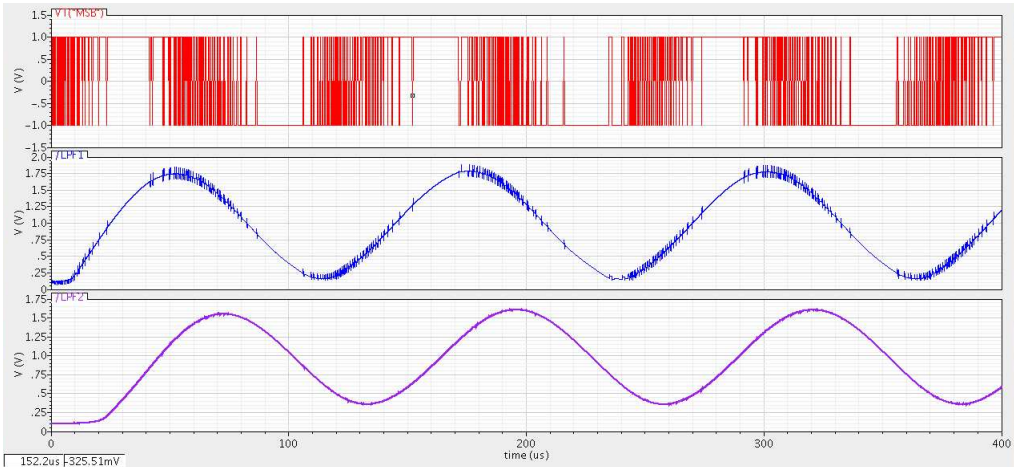

Figure 5.5: Transient response of the analogue low-pass filter

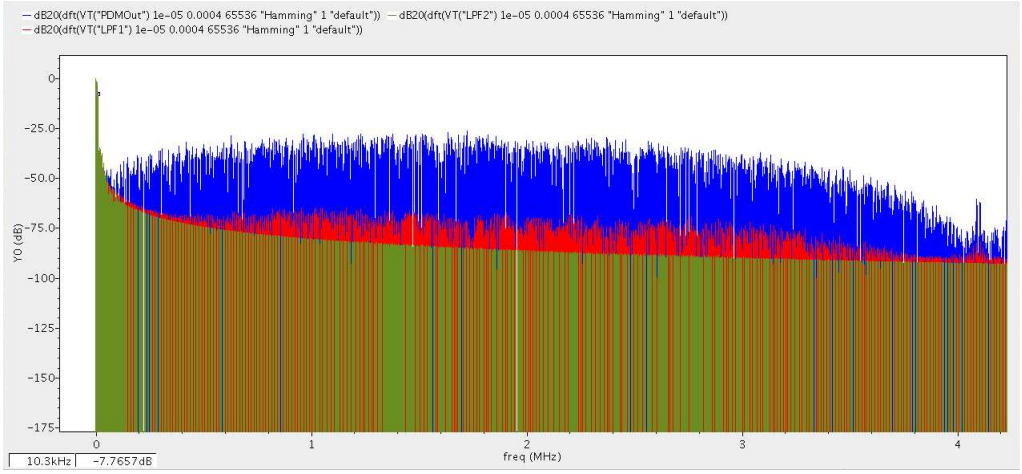

Figure 5.6: Frequency spectrum of the delta sigma modulated signal and the low-pass filter

the path a delay is observed between the input and the output sine waves.

The figure 5.6 shows the frequency spectrum of the delta sigma modulated signal and the two low-pass filters connected in series(blue trace - PWM wave, red - output of first LPF, green - output of second LPF).

5.2 Design of operational amplifier

The amplifier used in the low-pass filter is a two-stage amplifier with differential inputs as shown in the figure 5.7 with a capacitor C_c connected in the feedback path. The noise in an operational amplifier is dominated by that of input stage. Hence this operational amplifier specifically realizes PFET differential inputs, since PFET devices offer less noise and have better component matching by placing the input pair in a floating n-well[11]. The Miller capacitor (capacitor connected between the output of the second stage to the input of first stage) facilitates the "*splitting*" of the poles so that one of the two poles becomes dominant and thereby achieve stability. Figure 5.7 also shows the device dimensions calculated for a given gain bandwidth given by the equation 5.5.

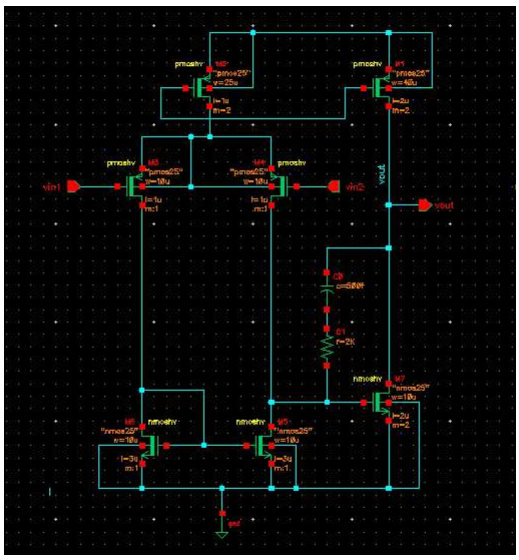

Figure 5.7: Schematic of OpAmp with device dimensions

$$GB = \frac{g_{mI}}{C_c} \tag{5.5}$$

where g_{mI} = Transconductance of the first stage and C_c = Miller capacitance.

For a $C_c \geq 0.22C_L$ where C_L 10pF, the device sizes of the differential input pair is determined.

The dimensions of the current mirror load devices is chosen to be W/L = 1, if the CMR is not a concern.

For a given 60^0 phase margin, the second stage transconductance is determined using the equation 5.6,

$$g_{mII} = 2.2 g_{mI}(\frac{CII}{C_c}) \tag{5.6}$$

The dimensions of the second stage devices are calculated utilising the transconductance of the first and the second stages as given by the equation 5.7,

$$S_{II} = S_{current_mirror_mosfet}\frac{g_{mI}}{g_{mII}} \tag{5.7}$$

The DC analysis is carried out with worst case varying differential inputs as shown in figure 5.8. As seen the offset voltage is zero and the amplifier behaves expectedly for the maximum voltage swing on the inputs.

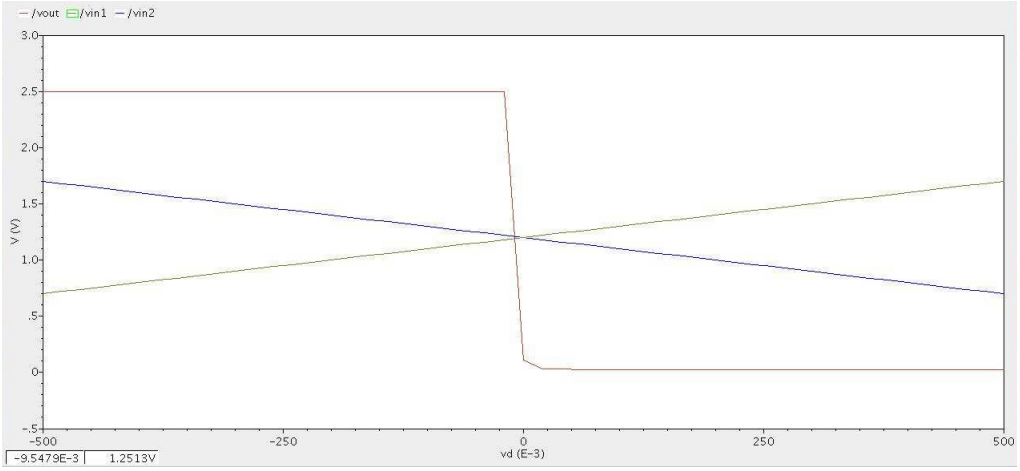

Figure 5.8: DC analysis with differential inputs and output

For frequency varying from 10Hz to 1GHz, the opamp has an AC gain of 34dB upto 400KHz (figure 5.9).

The opamp in this case is used as a closed system hence stability is of main concern. Therefore a maximum negative feedback is applied while designing the opamp i.e. output of the second stage short circuited to the inverting input of the first stage. The stability of the operational amplifier is determined by stability analysis and as shown in figure 5.10 and whose gain and the phase margin are as shown in the figure 5.11.

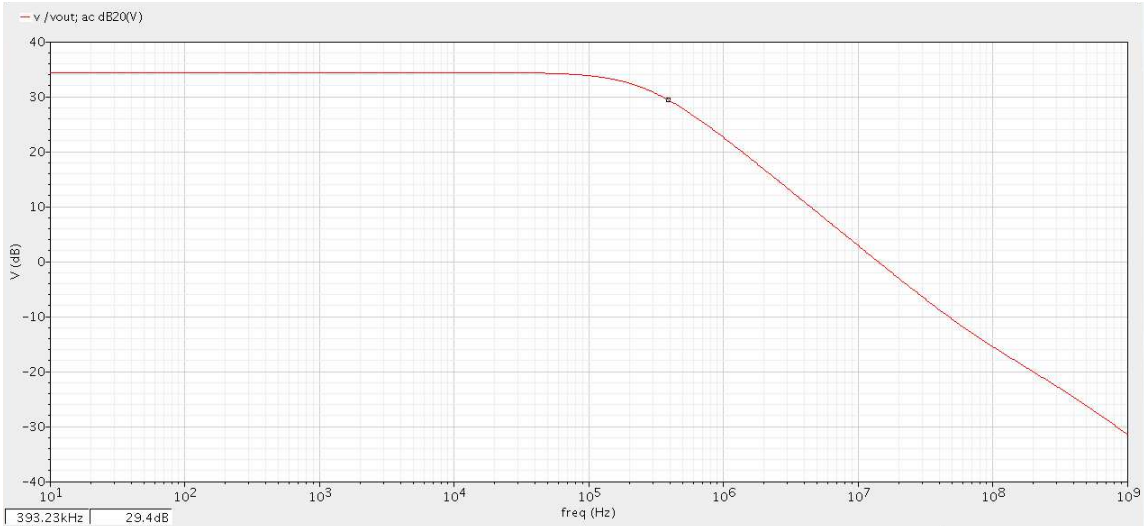

Figure 5.9: AC analysis of OpAmp

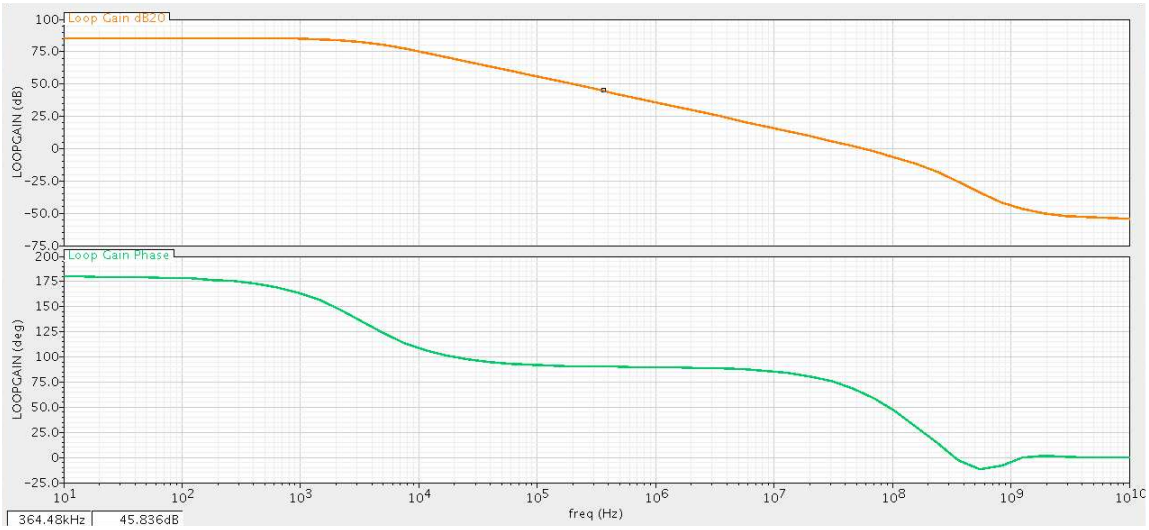

Figure 5.10: Stability analysis of OpAmp

Figure 5.11: Stability summary with phase and gain margin

Chapter 6

Phase locked loop simulations

As discussed earlier, the two mixers in the quadrature frequency converter require a same frequency signal but differ in their phase by a quadrature. The other input are also in quadrature but who derive the signal from a local oscillator. This topology of the mixer gives rise to the possibility of two architecture of DCFM controlled PLL which are discussed below,

- Access the sine generated at two locations to generate quadrature PCM streams and use two sigma-delta modulators to generate two quadrature PWM outputs.
- Access the sine generated at one location and generate a PCM input to a single sigma-delta modulator which generates a single PWM stream. Split the stream into two and delay one by the number of delta-sigma output samples equivalent to the $\frac{\lambda}{4}$ at the current frequency.

In the latter of the two architectures discussed, the split has to be done for the phase error analogue sinusoid which has a very low bandwidth feeding the mixer. The splitting and subsequent generating of quadrature signal would require a capacitor of very high order(in nF) and limits the drive of the mixer. Furthermore, this would also need feedback to avoid undesired frequency components to overcome PVT variations and mismatch. However, splitting the sinusoid in digital domain before being given as input to delta sigma modulator would require few latches and no feedback. Hence it is preferred to operate two sigma-delta modulators in quadrature and mix using the quadrature frequency converter.

Incorporating this architecture, the phase locked loop using digitally controlled frequency modulation block diagram is as shown in the figure 6.1. The output of the PLL is locked to a input reference signal of 5MHz impaired with jitter. The loop filter utilises a clock multiple of of the input reference signal and specifically in this system it is 32 times 5MHz.

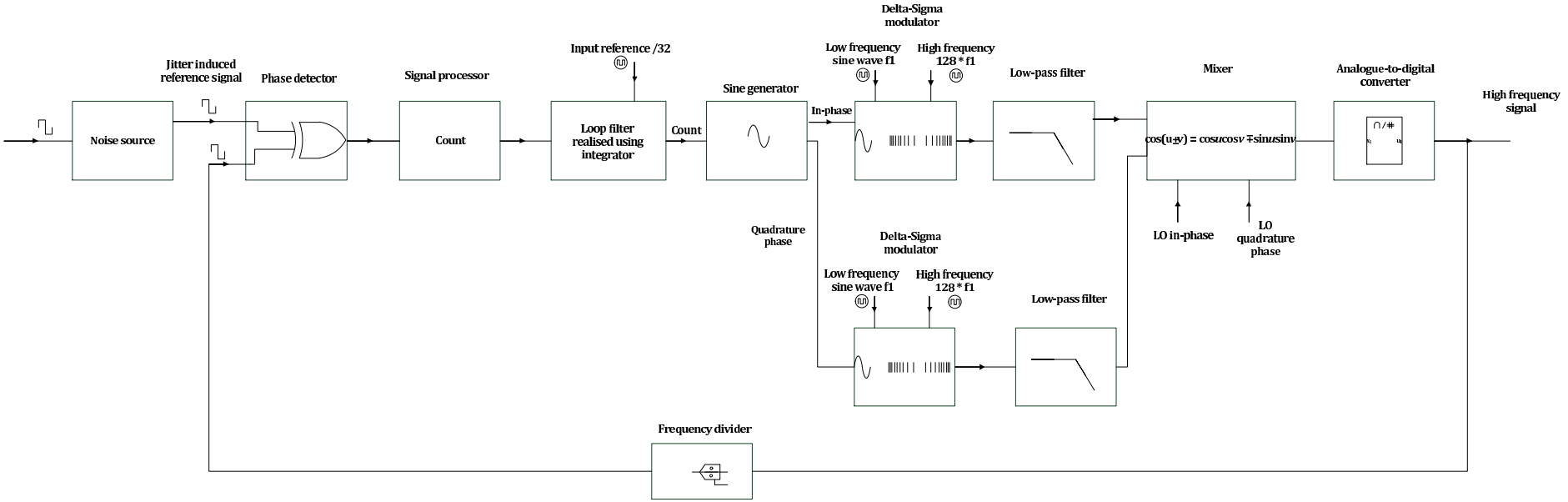

Figure 6.1: Phase locked loop using digitally controlled frequency modulation

The frequency spectrum of the ideal reference signal and that of the induced with jitter is as shown in the figure 6.2. It can be seen that significant undesired energy is present in side-band frequencies and which has to removed by the action of PLL to achieve a stable clock.

Figure 6.2: Frequency spectrum of white noise

The figure 6.3 shows the phase error detection using XOR gate and it can be observed that it fails to convey the direction in which the VCO has to steer itself to correct the phase error. However, phase error detection using subtraction outputs three levels as shown in the figure 6.4. A positive value corresponds to a negative correction and vice versa. A zero level corresponds to a nil correction. It can also be observed that this three levels of phase error is responsible for the non-linearity.

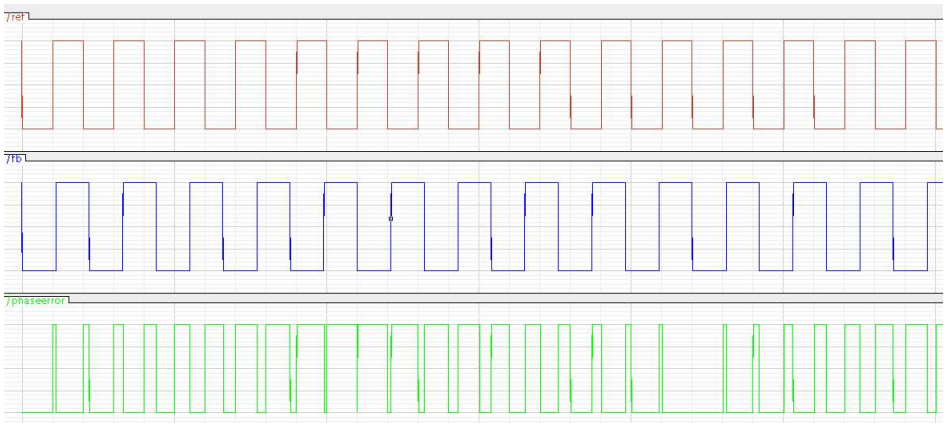

Figure 6.3: Output of the phase detector using XOR gate

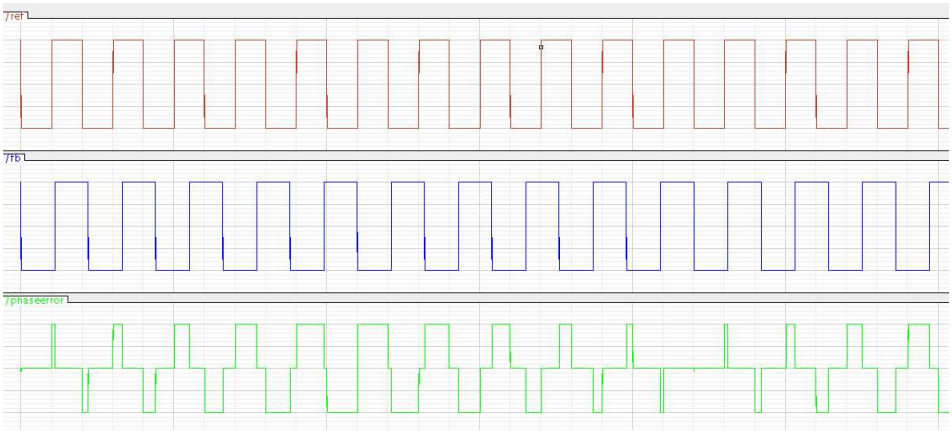

Figure 6.4: Output of the phase detector using Subtraction

The blue trace in the figure 6.5 is the phase error count corresponding to one cycle of the input signal for a unit time which generates corresponding sinusoidal for subsequent modulation. The loop filter low-pass filters this output (green trace) to produce the averaged sum. The corresponding frequency spectrum is shown in figure 6.6 and it can be seen that the cut-off frequency is 20kHz. Hence it can be concluded that the PLL will detect and correct frequencies in the range ±20kHz of input reference signal. The main advantage of DCFM PLL lies in the fact that it is able to track high frequency components slowly without much constraints on components i.e. if the same functionality would had to implemented using an analogue block. it would require huge amount of capacitances. The digital counterpart needs few digital latches to accomplish this complex task.

Figure 6.5: Output of the signal processor

The figure 6.7 and figure 6.8 shows the output at various points in the PLL. The corresponding labels in figure are self-explanatory.

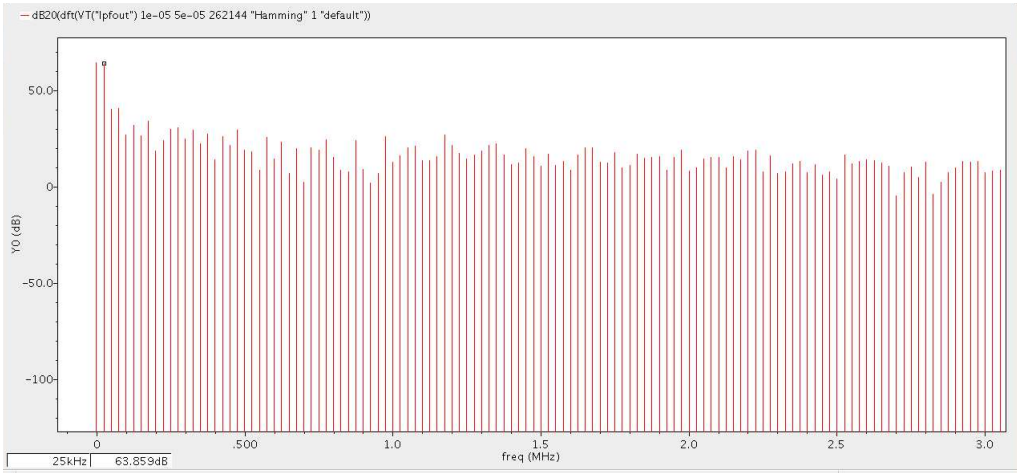

Figure 6.6: Frequency spectrum of signal processor

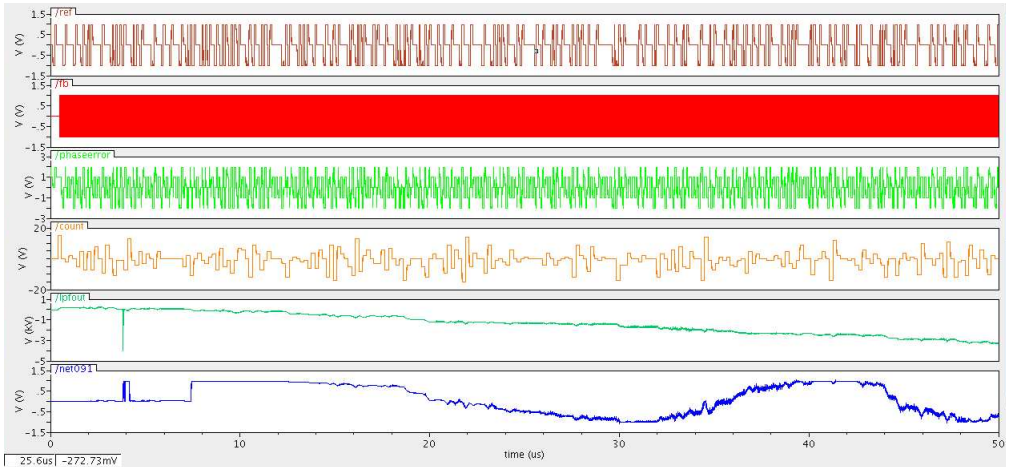

Figure 6.7: Simulation results of PLL 1-2

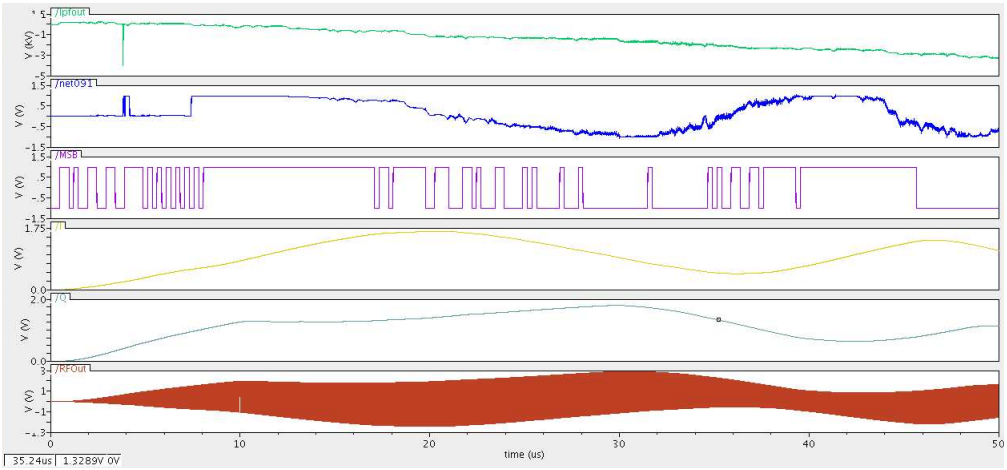

Figure 6.8: Simulation results of PLL 2-2

Figure 6.9: Frequency spectrum of output signal locked to input reference signal of 5MHz

Although the feedback signal is 2.5GHz, the figure 6.9 shows the frequency spectrum of the input reference signal and the feedback signal which is divided by a factor corresponding to the frequency multiplied to observe the noise suppression. It can be seen that the reference signal (shown in red trace) contains frequency components of significant energy in the side-band. However, the output of the PLL(shown in green trace) has suppressed side-band frequencies thereby "*cleaning*" the input clock impaired by jitter.

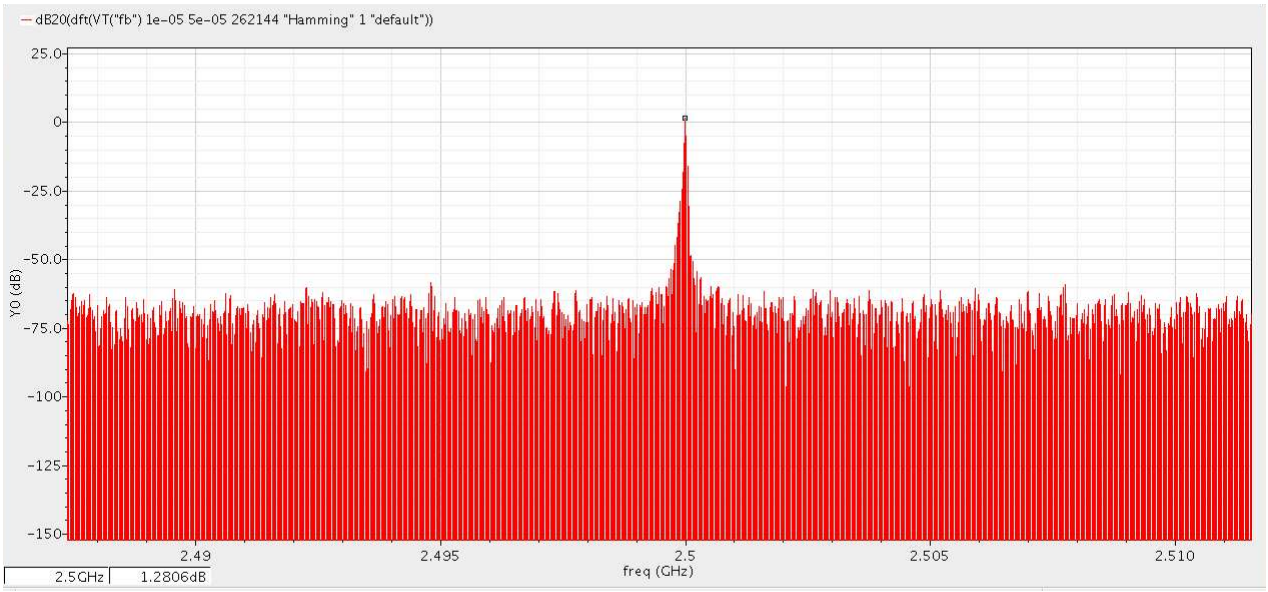

Figure 6.10: Frequency spectrum of output signal

The figure 6.10 shows the 2.5GHz signal free of noise components. The presence of immediate side-band frequencies depends on the resolution of the digitally coded signal processor.

Chapter 7

Evaluation

As is desired, the noise in the simulated PLL is calculated using spectreRF tool of cadence. However, owing to blocks coded in verilogA, the spectreRF could not be employed to calculate because of the tool's drawback to identify "*hidden*" states in verilogA codes seen in memory elements like flip-flops. Hence a frequency spectrum is used to verify the desired functionality.

The active low-pass filter employ a very high values of capacitors of 212pF which is not realizable easily. Hence either a higher gain of opAmp or higher cut-off frequency could compensate for the high values of capacitances. And also a better stability of opAmp could ensure a steeper cut-off frequency.

A second active low-pass filter was used to cut-off the noise shaped high frequency signals of the PWM wave. This second filter is redundant, however is included to meet the high gain requirement of the operational amplifier. Hence to design the first opamp with high gain would be a future effort.

Chapter 8

Conclusion and future work

To overcome the drawbacks of a conventional PLL, digitally controlled frequency modulator is employed to "*lock*" the output signal to input reference. This PLL successfully locks the output to 2.5GHz derived from the input reference of 5MHz. The simulation results show that the noise (inherent of the input reference signal) in the side-band frequencies is suppressed. The loop filter suppresses the high frequency components to provide binary coded DC voltage to the DCFM. The delta sigma modulators facilitate noise shaping and thereby is mainly responsible for removal of quantization noise and subsequently obtain the clock free from jitter. Since most of the circuitry of delta sigma modulators is digital, the complexities of analogue components is refrained and also much cheaper and faster. The clock used by the delta sigma modulators is of reasonable frequency and hence the realisation of whole PLL in this topology is quite feasible. The noise caused by analogue components of active low-pass filter is taken care by the feedback of the PLL. The only high frequency signal required is the one of the input to quadrature frequency converter and which can be obtained from a local oscillator. The generated output clock of the PLL can be further utilised to synchronize the local oscillator signal(required for quadrature frequency converter). The synchronisation is mutual which benefit both the signals and thereby achieve a stable clock.

The main advantage of the DCFM PLL is that it can track frequency components slowly around the centre frequency which otherwise would require very large capacitances to track by analogue blocks.

Higher order delta-sigma modulators could be incorporated for further noise shaping. As discussed in the evaluation section, the second low-pass filter is redundant and which can avoided by designing opamp of higher gain.

Most of the blocks of the PLL is coded in verilogA and the next step would be to physically realize all the blocks in cadence. Such a system would offer "real" jitter and hence the capability of the PLL using DCFM would be completely exploited and it would also facilitate calculation of noise using spectreRF.

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