Abstract

The increasing popularity of Automatic identification procedures (Auto ID) in recent years has generated a widespread interest in Radio Frequency Identification (RFID) and its applications. A lot of research is being done on its efficient design and implementation. The aim of this project is to study a passive RFID tag system, its building blocks and implement the whole system design. The design is implemented on a schematic level on the Cadence Analog Virtuoso Simulator tool. The system is implemented in a hierarchical manner wherein, the individual blocks are first designed as per their requirements and later all of them are merged to achieve the overall system functionality.

Three of these building blocks, the rectifier ,demodulator and oscillator are first implemented in their conventional way. Their experimental results are studied and it is found that some design modifications are required to overcome some problems. The circuits are accordingly modified and the experimental results show better results.

The secondary aim of the project is to introduce security measure within the tag so that tag data can be protected from un-authorised access. This feature has been successfully implemented by embedding a decision making block within the tag structure in such a way that it will authenticate the reader and act accordingly.

Overall, the main contributions of this design project are,

- Improving the efficiency of the conventional HF rectifier as it is the main source of power to the other tag circuitry
- Solving the issue faced during demodulator design and achieving more stable results
- Frequency variations occurring in the ring oscillator due to supply changes have been reported and a slightly different approach for the oscillator design is presented thereby minimising the frequency variations to a large extent.
- Additional data security measure in the form of GO/NO-GO logic has been implemented using a stream of CMOS logic gates to validate the reader identity

Table of Contents

1. Introduction

In recent years, with the advancement in wireless electronics and the chip design techniques, automatic identification technology (Auto-ID) [1] has been growing rapidly and become a key component in manufacturing and distribution industry. RFID, which stands for Radio Frequency Identification is one such automatic identification technology which is widely used in areas such as supply chain management, public transportation and access control. It is a wireless electronic tagging technology [2] to uniquely identify a person or object using radio waves. The system consists of an Interrogator, often called as a Reader and a transponder, often called as a Tag. Modulated RF signal from the reader activates the tag, which then transmits the data stored in its memory back to the reader. The tag can be Active or Passive in nature. Active tags have internal battery to power its circuitry and offer long read ranges. Passive tags on the other end, do not have any internal battery and draw power from the received reader signal. This however reduces tag size and its cost compared to active tags thereby making them popular.

As no internal power supply is used in passive tags, the reading range between reader and the tag is limited to a small distance which varies from few centimetres to only few meters. However, this limitation is very useful in security of data from tag to the reader. The low power operation also limits the data stored in tag to only few tens of bits which is sufficient in pure identification applications. The demand for more energy and high efficiency for passive RFID arise when used to transmit data in the range of few 100's of bits to few 1000's of bits.

The principal work of the project is to meet this high efficiency demand and design a passive RFID tag to transmit a large data, around 512 bits. We have here proposed a new application of RFID in Medical and Health-care sector wherein a person's medical record can be stored in the tag, which can be easily retrieved in case of medical emergencies thereby enabling prompt medical attention and treatment. Considering the scope of this project, the work has been limited to design of Analog Front End [3] of the tag, the details of which are discussed in section 2.1.

1.1 Aims and Objectives

The primary aim of this project is to design a High Frequency(HF) passive RFID tag capable of transmitting large data (around 500 bits or more). The secondary aim of the project is to implement a reader authentication mechanism enabling data transfer only when reader will be identified correctly.

The objectives to meet this aim are as follows :

- Divide the whole system into individual function blocks and study their requirements so as to implement them in a suitable manner

- Efficient design of rectifier, as it is the source of power to the other circuit elements. Here, I began with a basic rectifier design which was later improved to achieve better results
- Design an On-Off Keying (OOK) demodulator circuit to extract the data out of the reader signal. The design of this block is a combination of the demodulator design in [18] and the OPAMP design presented in my interim report
- Design of a GO/NO-GO block which will output a positive pulse only when the data in the reader signal has been authenticated. This is one of the important aspects of the tag design as in most of the cases, tags don't feature reader authentication mechanism
- Implement a ring oscillator design to generate a HF periodic signal of frequency 14.28MHz.

  A 14.34 MHz ring oscillator also has been proposed whose frequency is relatively independent of the supply voltage variations
- Integration of all the individual circuit blocks and make them work as a system able to transmit an Amplitude modulated tag's data at 14.28MHz

1.2 Organisation of this dissertation

The dissertation is divided into following sections,

Section 2 discusses the background of the RFID system and gives the overview of a conventional tag structure and briefly talks about the analog front-end of the transponder system.

Section 3 explains the choice of the technical parameters like frequency, modulation type, inputs to the system and the design tool being used.

Section 4 is about the tag design implemented for this project. A brief working of the whole design will also be presented.

Section 5 gives the detailed explanation of the individual blocks of the design. Experimental results have been given for a better understanding.

Section 6 shows the schematic level implementation of the proposed RFID tag design

Section 7 demonstrates the results achieved after the whole system implementation

Finally, in Section 8, the conclusion for this project is presented and I have given some suggestions on future work which can improve the overall functionality of the design and add new features.

2. Background

With RFID finding a large number of applications in the field of supply chain management, access control and passive sensors, passive tag design has generated a lot of interest, as it is the tag that stores the data and accomplishes communication with the reader. Figure 1 shows the blocks of a basic RFID System.

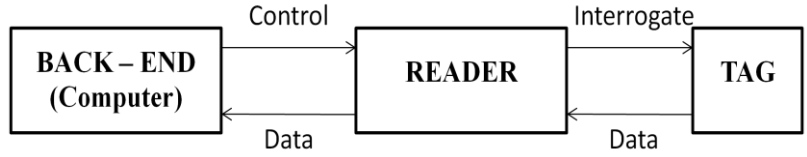


Figure 1 :- RFID System block

The reader (Interrogator) is continuously transmitting the RF signal in its neighbouring area setting up an electromagnetic field. When the Transponder (Tag) enters the field, it gets activated and extracts energy from the received signal and transmits back the data stored in its memory to the reader. The reader then sends the received data to the back-end system (computer) which will manipulate or work on the data and accordingly generate a control signal to the reader indicating whether the tag has been recognised and data has been received.

Out of these system blocks, it is the tag which holds the criteria for the design of a RFID system. Over the years, passive tag design has evolved a lot giving better efficiency and flexibility to the use of RFID for different applications. Reduction in tag size and cost has triggered a wide interest in the design and development of integrated circuits for passive tags.

2.1 Basic RFID Transponder

Figure 2 shows the structure of a basic RFID transponder [3].

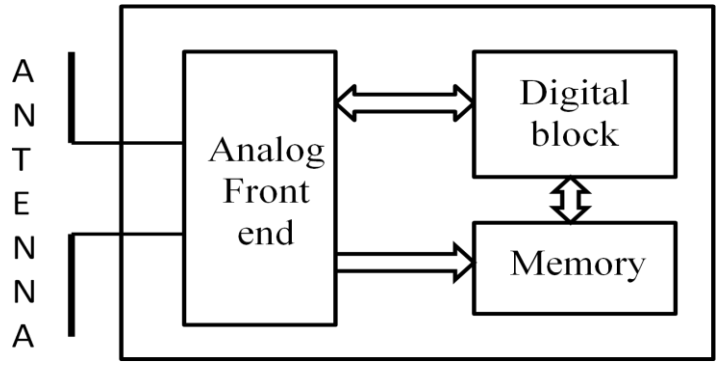


Figure 2 :- Basic RFID transponder structure[3]

As passive tags do not have any internal source of power supply, all the power required to drive the tag circuitry has to be obtained from the electrical/magnetic field generated by the reader. The tag antenna couples the reader signal and makes it available to the Analog Front-End, whose structure is as follows,

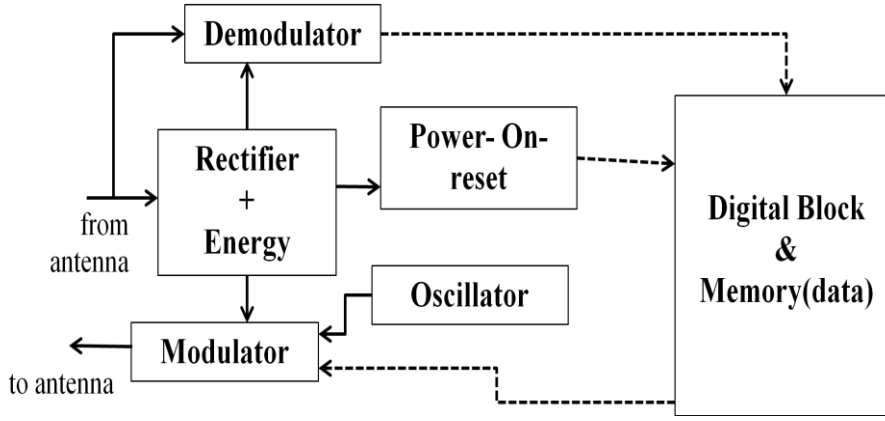


Figure 3 :- Basic Analog Front-End structure

The most important circuit in the above figure is the Rectifier, as it converts the coupled AC electro/magnetic signal to a DC voltage, which serves as a source of power to the other tag circuits. During passive tag design, the focus is more on the optimisation of the Antenna and the rectifier structure because of the following reasons,

- The efficient transfer of energy from reader to tag depends on how precisely the antenna has been designed. Proper coupling with the reader antenna will ensure that maximum power is drawn and made available at the rectifier input.
- Good efficiency of rectifier will result in less power loss and thereby enabling sufficient and regulated DC supply to the other tag circuits.

For my project, I have worked on the optimisation of the rectifier, and for antenna, I have used its electrical equivalent circuit as an input to the rectifier which will be discussed in detail in Section 5.2 . Some of the previous work done on HF Antenna design can be found in [6][7].

3. The choice of Technical parameters

3.1 Frequency

RFID being a wireless communication between a reader and a tag, uses radio waves. These radio waves fall in the electromagnetic spectrum. Frequencies from 300kHz to 3GHz fall in this spectrum. Though RFID operates in an unlicensed spectrum space, the 4 most common unlicensed frequency bands in which RFID operates are[8],

a) low-frequency (30 - 300kHz)
b) high-frequency (3 - 30MHz)
c) ultrahigh-frequency (300MHz – 3GHz) and
d) Microwave (2G – 30GHz)

However, the most commonly used bands are the HF and UHF, while the microwave range is used in only few applications. The below table shows a comparison between the various frequency bands[9] [10].

	LF	HF	UHF	Microwave
RFID frequencies	125 – 135kHz	13.56MHz	860 – 930MHz	2.35GHz
Typical read range	Less than 0.3m	Approx 0.5m	Approx 3 – 5m	Approx 1m
Characteristics	No radiation and Reflection problem. Works well near metal or fluids	Tolerant to metals and fluid surfaces	Read reliability issues with metals and fluids as UHF are easily reflected or get absorbed	Read reliability issues with metals and fluids as Microwave are easily reflected or get absorbed. They also possess health issues
Memory storage	Few hundreds of bits	256 bits – 8Kb	64b – 256bytes	64b – 256bytes

Table 1 :- Comparison between RFID frequency bands

Though UHF offer good read ranges compared to HF, the HF range of 13.56MHz has the following advantages over UHF,

a) good immunity to electrical interference and environmental noise

b) No reflections from metal and fluid surfaces as compared to UHF which get easily absorbed resulting in signal attenuation

c) better data transfer rate than UHF

d) UHF systems require high power RF transmission compared to HF due to long read ranges. This requires readers with high sensitivity and also demands for

sophisticated techniques to extract information from tag data. This makes the system complex as compared to a HF RFID system

For this reason, I am operating my system in the HF range.

3.2 Modulation types

Different modulation schemes have been implemented for forward link communication and return link communication. This has been done keeping in mind the complexity of the designed circuitry within the tag. So, for forward link (from reader to tag), a simple circuit has been implemented for decoding the reader information. This has been achieved using ON-OFF-KEY (OOK) modulation for reader signal. The advantage of this modulation is that it simply requires an envelope detector and a comparator circuit to successfully extract the information from the reader signal.

For return link communication (from tag to reader), Amplitude modulation (AM) of the tag's data has been chosen. The advantage is that it is easy to implement the logic with the use of CMOS gates. The details of both the modulation schemes have been discussed in section 5.1 and section 5.7 respectively.

3.3 Source of Input

As discussed in [1] - table 3.6, the minimum supply voltage required for the operation of the tag microchip keeping in mind the power consumption is 1.8V and the maximum up to 10V. My input signal to the tag is a 3V – OOK modulated reader signal which is fed to the rectifier, which then delivers a supply of around 2.25V to the rest of the tag circuitry. The generation of the 3V – OOK modulated signal is discussed in section 5.1 in detail.

3.4 Why CMOS?

CMOS is widely used technology today for the design and construction of analog Integrated circuits. The reasons are however as follows,

a) Noise immunity and power consumption are two important IC design criteria to be taken care during circuit design. CMOS devices compared to TTL and NMOS devices have better noise immunity and low static power consumption.

b) CMOS technology has the highest device count and circuit density compared to other technologies. Due to this reason, CMOS devices are the optimum choice to be used in wireless system.

c) Inherently, CMOS have a lower manufacturing cost compared to SiGe-BiCMOS by over 30% [12].

Overall, CMOS devices offer better reliability and performance and hence are the obvious choice to be used in IC's design and construction.

3.5 Design Tool

The EDA package that has been used for this project is the Cadence Virtuoso.

The Virtuoso analog design environment is specially designed to provide advanced simulation in order to facilitate fast and accurate verification. The tool also provides easy manipulation of the various analog quantities like the current, voltage, resistance and capacitance providing a basis of a full custom design. [11].

The Cadence Virtuoso Schematic Editor provides fast and easy creation of design entries. The tool provides well defined component libraries which allows faster simulation at transistor level and gate level. The ADE editor provides option for specifying the analysis (Transient, DC or AC and many more) to be done on the circuit. It also gives option for setting up constraints and selecting node points in the circuit to view the output of the simulation. The tool also facilitates creation of our own symbol entries for a circuit so that it can be used directly at different places without the need of designing the whole circuit again.

The above mentioned feature of creating symbols is very important in hierarchical system design wherein symbols of commonly used circuits can be created and used when required in different circuits thereby building a hierarchy, starting from a circuit at a bottom level and ending up with a system made up of the respective circuit symbols.

4. System Design

The architecture of my proposed passive RFID tag is as shown,

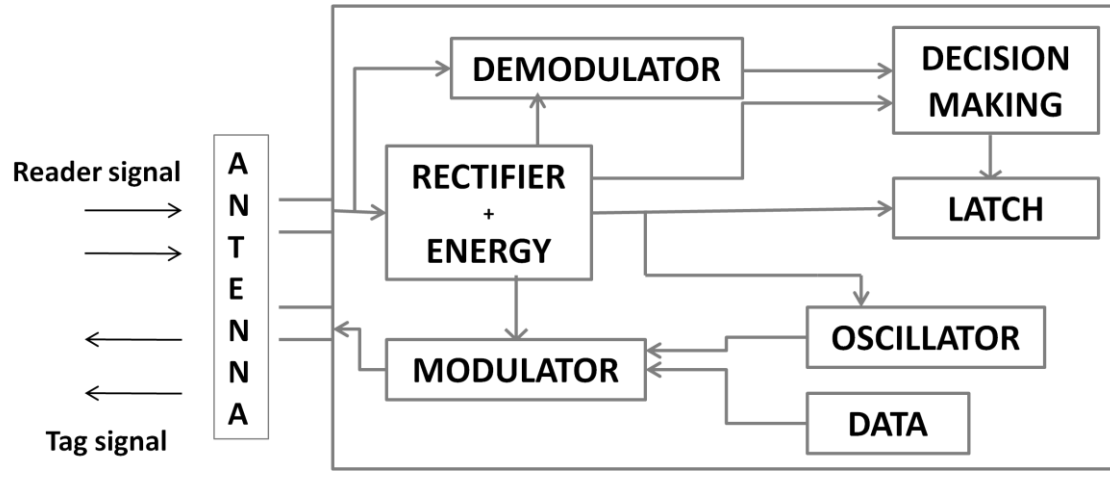


Fig 4 :- Proposed Transponder architecture

- OOK modulated reader signal generates an electro/magnetic field which energises the tag antenna. This signal is a 3V RF wave at the frequency 13.33MHz

- The antenna couples the RF signal to the rectifier which than converts into a DC signal used to power all the other tag circuitry

- Demodulator extracts the information from the received reader RF signal. This information is an important aspect of my design which forms the basis of the decision making logic.

- The Decision making circuit processes the demodulator output, which is the reader information extracted from the RF signal and outputs a positive pulse if the reader is authenticated.

- The latch circuit, latches the output to an appropriate state of authentication (which is either true or a false)

- The oscillator circuit generates a RF carrier wave of frequency 14.28MHz which is then modulated with the tag's data. The modulation is amplitude modulation which is done by the modulator circuit.

- The modulated tag's data is then sent to the antenna circuit for transmission back to the reader

5. Modules of the RFID Tag system

5.1 Reader signal

As mentioned in section 3.3, the input for the tag is an OOK modulated 3V RF signal of frequency 13,33MHz. In the tool, the multiplier logic is used to implement the OOK modulation and generate the required signal.

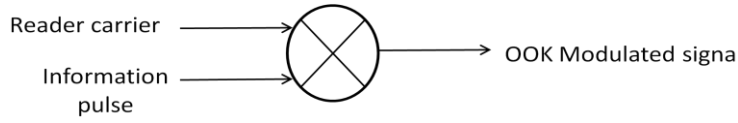


Fig 5 :- Multiplier logic symbol implementation

The reader carrier is a 3V RF periodic signal, while the Information pulse is the modulating signal. The respective signal representations are as follows,

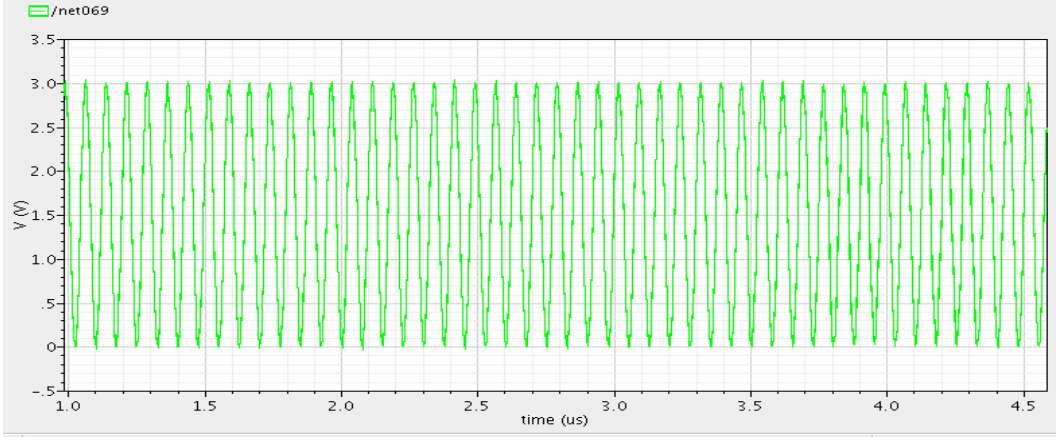


Fig 6 :- Reader carrier

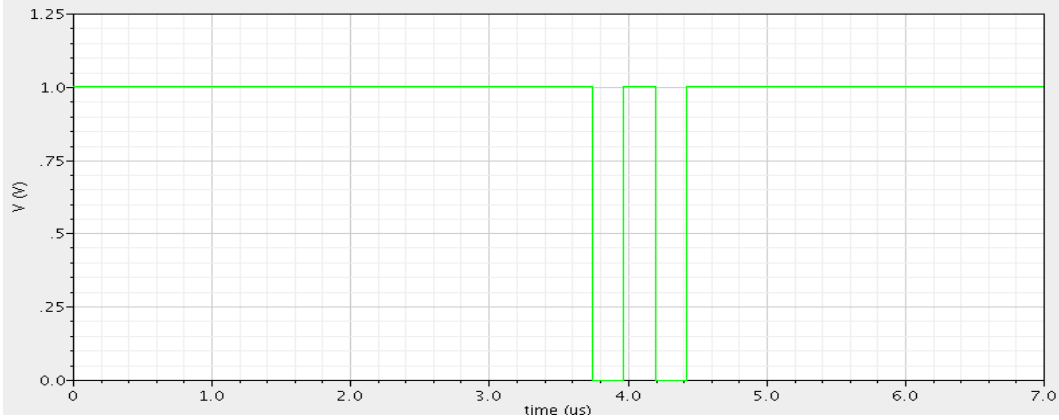


Fig 7 :- Information pulse

As seen in Fig 7, the continuous stream of 1's represent no information, while the bit pattern of **010** is the actual reader information to be sent with the RF signal.

The multiplier logic is implemented in **veriloga** and a symbolic representation of the multiplier is used in the design system. The logic used is as below,

```
analog begin
    V(out) <+ (V(in1) * V(in2));
end
```

The cell view implementation of this code using the Verilоga – editor generates the multiplier symbol with the whole code, updated as follows,

```
module simple_mult(out, in1, in2);          --- start multiplication module
output out;                                 --- OOK output
electrical out;
input in1;                                  --- reader carrier
electrical in1;
input in2;                                  --- Information pulse
electrical in2
analog begin
    V(out) <+ (V(in1) * V(in2));            --- multiplication logic
end
end module                                  --- end multiplication module
```

The output of this multiplication block is,

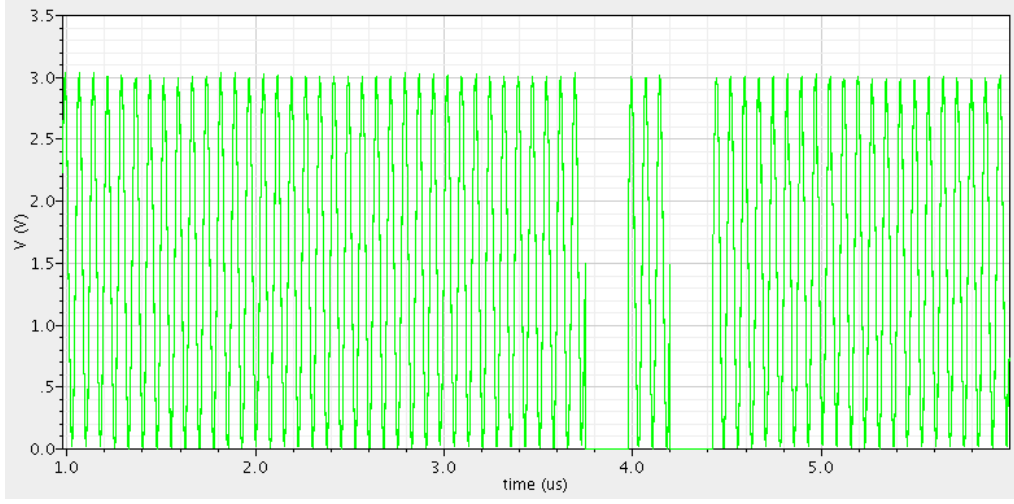


Fig 8 :- OOK modulated 13.33MHz RF reader signal

5.2 Transponder antenna

At high frequencies around 13.56MHz, loop antennas are used for communication. The coupling between the reader and tag is through the mutual inductance of these two loop antennas. The reliability of the system and the read range depends on the efficient transfer of energy from the reader to the tag and for that, parallel resonant LC loop antennas are used which are tuned to the communicating carrier frequency [13].

In this project, the electrical equivalent circuit of the antenna system has been implemented and used.

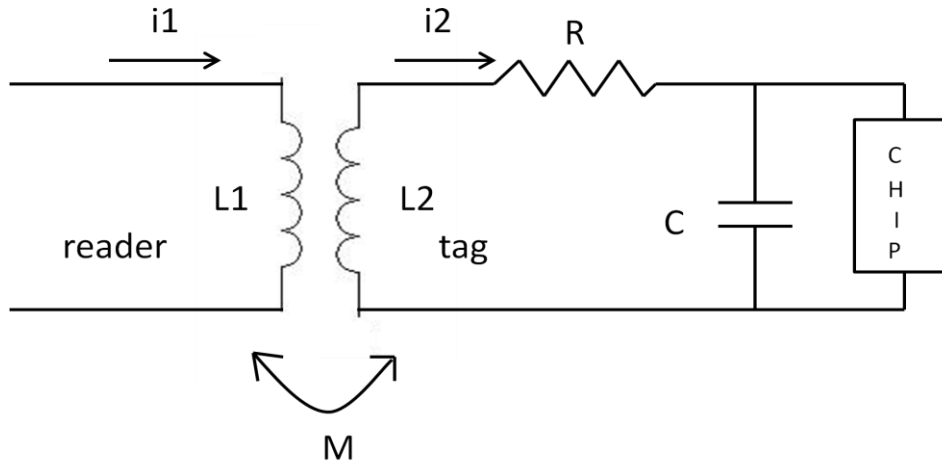


Fig 9 :- Transponder tag equivalent circuit [13]

L1 = reader antenna inductance
L2 = tag antenna inductance
i1 = current flowing through reader inductance
i2 = current induced in tag antenna
R = antenna resistance
C = parallel resonating capacitance for tuning
M = mutual inductance between the two antenna coils

One of the key design parameter for an antennas is the *Q – factor,* known as the *Quality factor*. For a higher energy range, a higher Q is desirable [1]. Also, the bandwidth of the transponder resonant circuit is inversely proportional to the Q factor and is given by [1],

$$B = \frac{f}{Q} \quad \text{..... (1)}$$

where,

B = bandwidth
f = resonating frequency
Q = quality factor

Considering Q = 30, f = 13.33MHz for transfer from reader to tag, we get the bandwidth as 444 kHz. This means that, the modulation sidebands of the signal around the frequency of 13.33 MHz, will be damped due to the influence of this bandwidth.

This is highly desirable for our system, as for transmission of data from tag to reader, we are operating at 14.28 MHz and this damping phenomena will make sure that the signals at 13.33 MHz and 14.28 MHz do not interfere with each other in any manner.

The Voltage vs the Frequency graph will make things more clear,

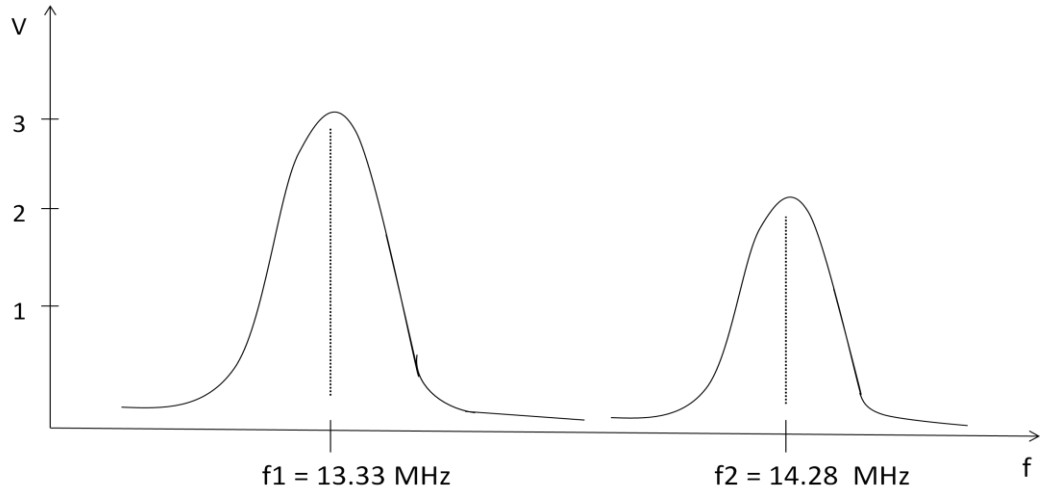


Fig 10 :- Voltage vs Frequency graph for a resonant circuit

This selection of Q-factor ensures that the forward link and return link signals will be separated in frequency domain and at the same time, the system will have a good energy range.

5.2.1 Design of L and C

The quality factor is also given by [14],

$$Q = \frac{\text{Energy Stored in the System per One Cycle}}{\text{Energy Dissipated in the System per One Cycle}} \quad \text{..... (2)}$$

$$= \frac{\text{reactance}}{\text{resistance}} \quad \text{..... (3)}$$

$$= \frac{\omega L}{r} \quad \text{..... (4)}$$

$$= \frac{1}{\omega C r} \quad \text{..... (5)}$$

where,

ω = angular frequency = 2πf
L = inductance
C = capacitance
r = DC ohmic resistance

substituting *Q = 30, r = 5 ohm, f = 13.33 MHz* in eq. (4) and (5), we get

L = 1.79 µH
C = 79.6 pF

when *f = 14.28 MHz*, the second antenna will have L and C as

L = 1.67 µH
C = 74 pF

Using the above calculated values, the electrical equivalent of the antennas was implemented in the design tool.

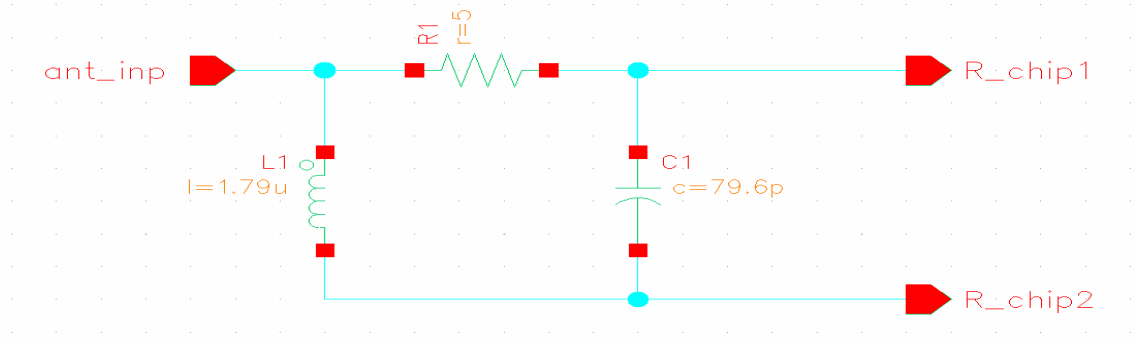


Fig 11 :- Antenna electrical equivalent for 13.33 MHz signal

In the above circuit, ant_inp is the input pins to which the OOK modulated reader signal will be fed. R_chip1 and R_chip2 refer to the internal tag circuitry which will provide an impedance R_{chip} to the antenna and are connected to the rectifier.

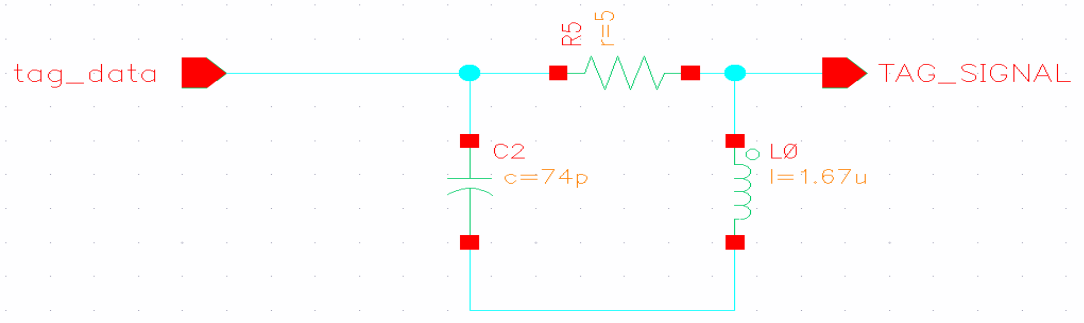


Fig 12 :- Antenna electrical equivalent for 14.28 MHz signal

The tag data which is amplitude modulated is the input to the above shown parallel LC resonant circuit. The antenna2 forms a mutual inductance with its respective reader antenna, which on receiving the tag data, will send it to its internal circuitry for demodulation and other processing.

5.2.2 Interrogation field strength (H_{min}) and Energy range (d)

The maximum HF input voltage (V1) at the tag antenna before rectification is 3V.

The Interrogation field strength (H_{min}) according to [1] is defined as the minimum field strength between the reader and tag at which the supply voltage (V1) is just high enough for normal operation. When the field strength will be at its minimum strength, the operating distance between the reader and tag will be at its maximum.

The details of the field strength and energy range equations can be found in [1], however, for the purpose of my project, I am mentioning only the final equations for the Interrogation field strength [1] and the Energy range [1].

$$H_{min} = \frac{V1}{\omega \mu_0 A N} \sqrt{\omega^2 \left(\frac{L}{R} + \frac{r}{\omega_0^2 L}\right)^2 + \left(\frac{\omega_0^2 - \omega^2}{\omega_0^2} + \frac{r}{R}\right)^2} \quad \text{..... (6)}$$

where,

V1 = antenna1 induced voltage
ω = angular frequency (2πf)
L = antenna inductance
R = load resistance as seen by the antenna (chip resistance)
r = ohmic resistance
A = antenna area
N = number of windings of the tag coil
ω_0 = resonant frequency of the LC circuit

As in reality, the L and C values will not be ideal as calculated and hence will show some variations from the desired values. This will deviate the resonant frequency of the LC circuit from the transmission frequency of the reader.

$\omega_0 = 2\pi f_0$ and $f_0 = (2\pi\sqrt{LC})^{-1}$

Substituting, V1 = 3V, f = 13.33 MHz, L = 1.79 µH, R = 1.5 kΩ, r = 5Ω, C = 79.6 pF, N = 4 and A = 0.05 × 0.08 m^2 in eq. (6), we get

H_{min} = 0.2374 A/m

Now that we have the value of H_{min}, energy range of the tag system is given by [1],

$$x = \sqrt{\sqrt[3]{\left(\frac{i N R^2}{2 H_{min}}\right)^2} - R^2} \qquad \text{..... (7)}$$

where,

x = energy range

R = transmitter antenna radius

i = transmitter antenna current

N = number of windings of transmitter antenna

Reader range can be increased by minimizing the difference between the transmitted reader frequency and the LC resonant frequency, such that H_{min} is reduced, or by increasing the transmitter antenna current.

Ideally from [1], N = 1, R = 40 cm

i = 290 mA (for our system)

H_{min} = 0.2374 A/m, as calculated above

x = 23 cm

This is the typical value of the read range for the implemented RFID system which is ideal for proximity applications where we intend to use. Actual results may be shorter or longer depending upon the following criteria's ,

- Performance of antenna coil
- Q of the antenna (higher the Q, more the read range)
- Operating environment
- Transmitting antenna current

5.3 Rectifier

For a passive RFID tag system, rectifier is very important as it converts the coupled AC electro-magnetic RF carrier to a DC voltage which serves as a source of power supply to the analog front-end circuit, digital block and the memory. To make sure that enough power is made available and the tag circuits operate properly, power transmission has to be efficient. In this project, I have worked on the efficient design of the rectifier circuit such that power losses are minimised and more power is available to be supplied to the other circuits.

The rectifier circuit design was implemented as a Full-wave Bridge Rectifier circuit using 4 diode connected MOSFETs [16].

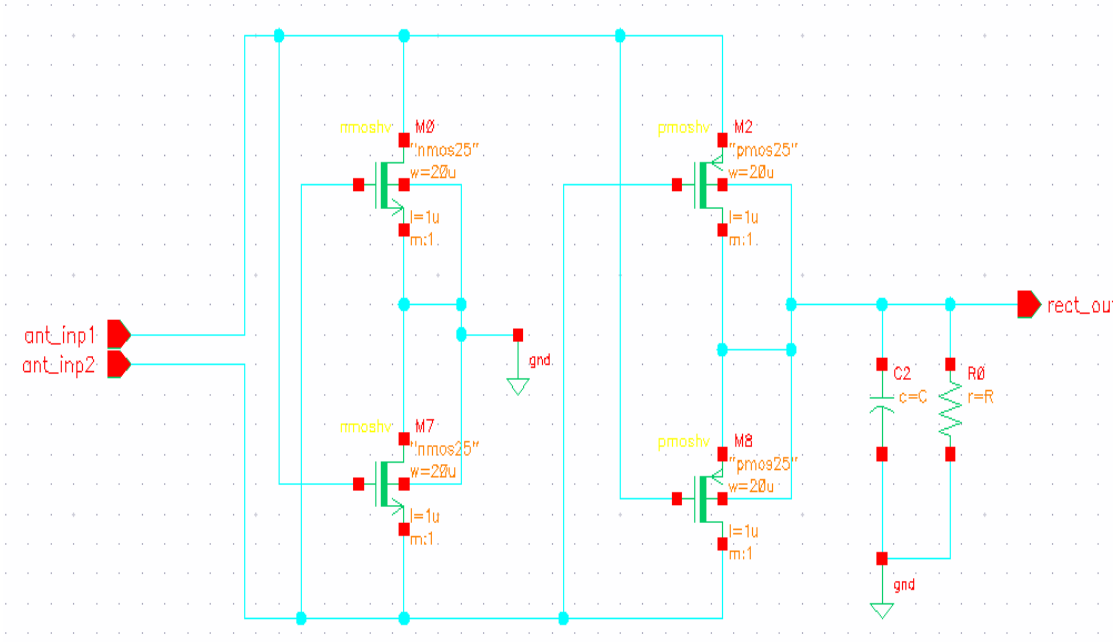


Fig 13 :- Gate cross-connection bridge rectifier circuit

The above structure uses NMOS (N1 and N2) and PMOS (P1 and P2) devices while the gates are cross connected.

- When ant_inp1 is a high voltage and ant_inp2 is a low voltage, N2 (lower NMOS) and P1 (upper PMOS) become conductive. This will charge up the load capacitor C.
- When ant_inp2 is a high voltage and ant_inp1 is a low voltage, N1 and P2 become conductive and will charge up the load capacitor C.
- Conventional rectifier circuits , where NMOS (N3 and N4) are used instead of PMOS (P1 and P2) and the gates are not cross-connected, suffer from threshold voltage drop problems thereby reducing their efficiency. However, the above

circuit does eliminate the problem of threshold voltage drop as it uses cross-connected gates for PMOS.

Fig 14. and Fig 15 show the available voltage and current at the output of the above circuit.

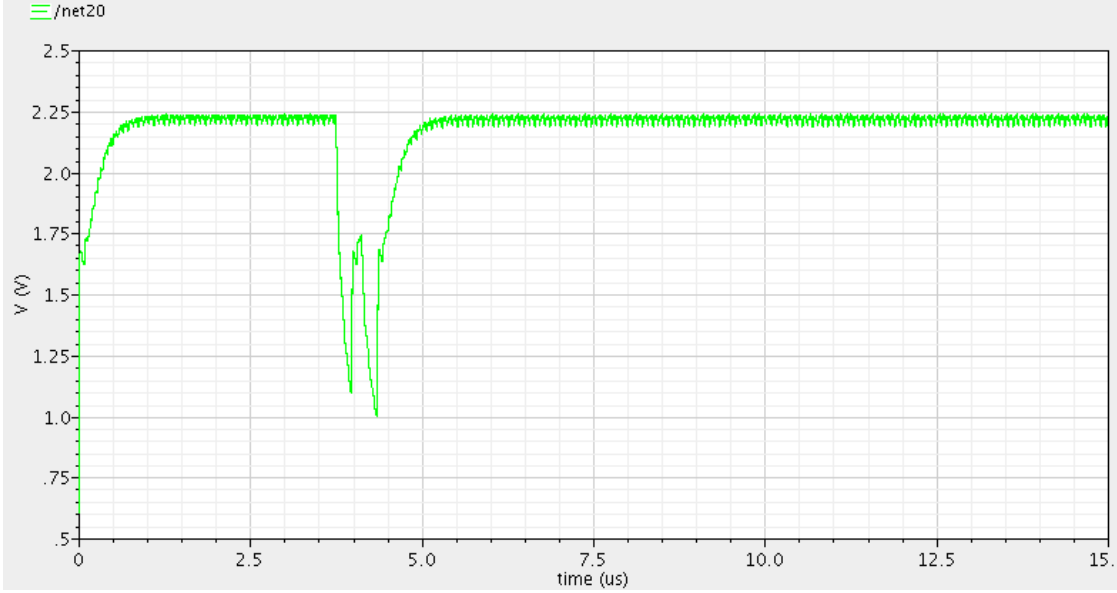


Fig 14 :- Output voltage for conventional rectifier circuit

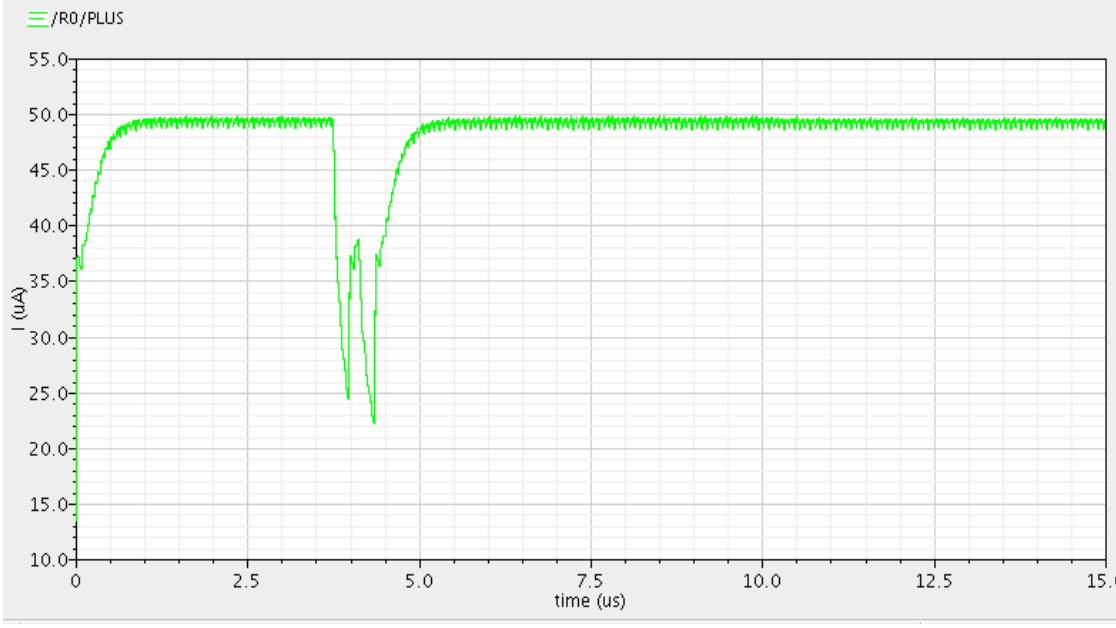


Fig 15 :- Output current for conventional rectifier circuit

From the above two results, we see that the conventional rectifier circuit provides an output rectified voltage of around 2.2V and a current of around 48 µA.

The circuit shown in Fig 13. though overcomes the threshold voltage drop problems, however faces another issue [16]. When the voltage of the antenna is smaller than the voltage present on C, the charge stored in the output capacitor C will flow back to the antenna through the PMOS devices. Consider the below example,

The signal voltage levels at the antenna terminals are as follows:

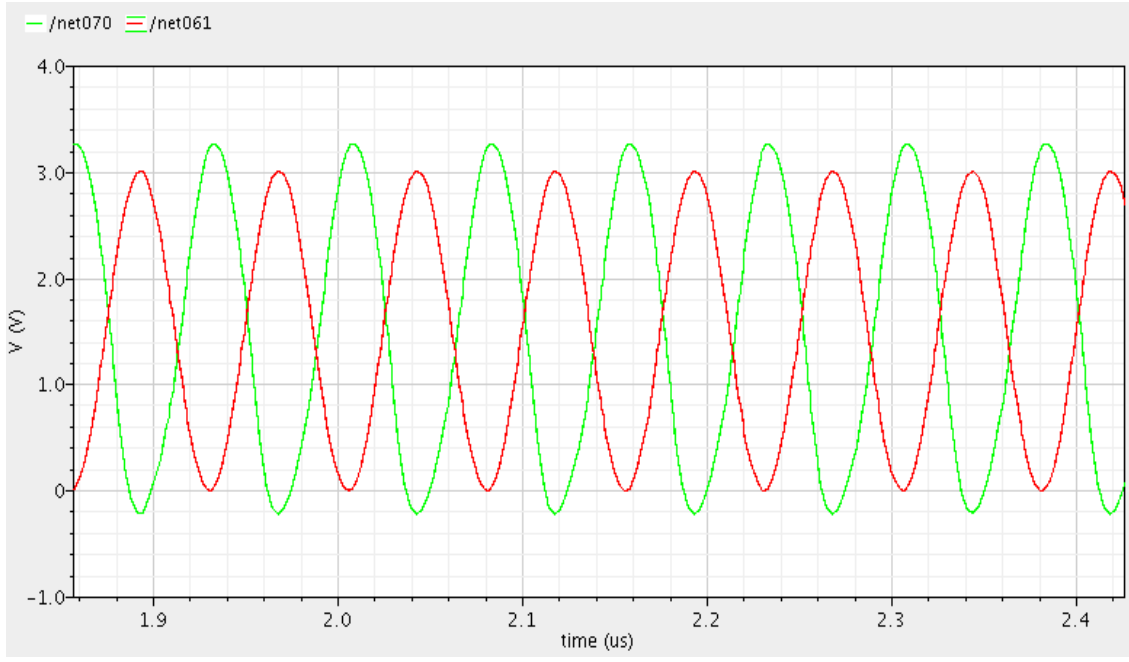


Fig 16 :- Antenna terminals RF signal voltage levels

The signal in red is the one at the antenna terminal ant_inp1. While the other is at the terminal ant_inp2. Considering the scenario when ant_inp2 is low voltage, and ant_inp1 voltage is rising and falling. During this period, PMOS (P1), will always be ON. As soon as voltage at ant_inp1 becomes less than that on capacitor C, the charge on C will flow back to the antenna terminal ant_inp1 through the PMOS (P1).

This feedback to the antenna will give rise to power losses in the circuit reducing its overall efficiency and producing voltage variations at the output.

In [16], a modification to this rectifier circuit is discussed which uses the bootstrap circuit technique to eliminate the threshold voltage drop problem and improve the overall efficiency of the rectifier circuit. However, the circuit discussed is more complex and would end up using more chip area. For this project, I have slightly modified the earlier rectifier circuit in such a manner that overall efficiency of my

rectifier circuit is improved and at the same time, the circuit would use less chip area compared to the one mentioned in [16].

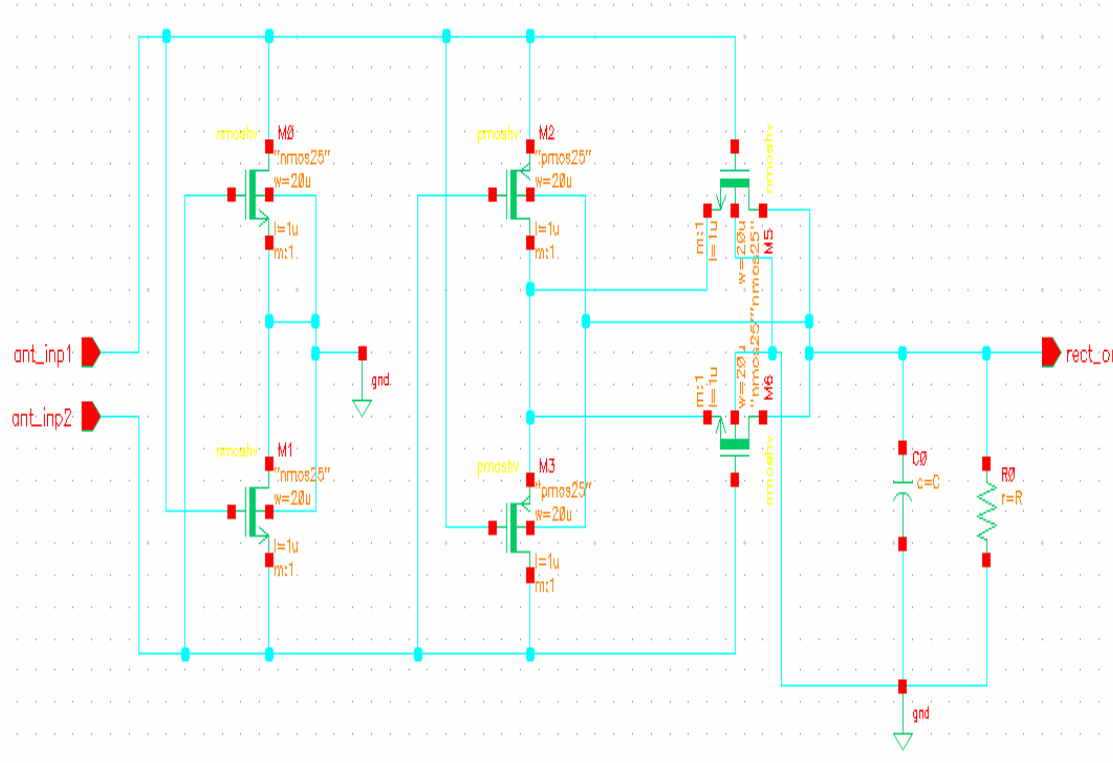


Fig 17 :- Modified rectifier circuit

Two additional NMOS (N3 and N4) have been added in front of the capacitor C. Here, a simple application of MOSFET as resistor switch is used. N3 and N4 act as MOSFET switches which turn ON and OFF depending on the voltage available at their respective gates.

Thus, when the voltage at the ant_inp1 is momentarily less than that stored on capacitor C, N3 (upper NMOS) will be ON and N4 (lower NMOS) will be OFF. N3 works as a resistive switch which will suppress the feedback flow of charge. The simulation results of the voltage and current at the output are as shown.

Here, the DC output voltage available at the output of the rectifier circuit is around 2.5V, while the current is around 56 µA. We can see that compared to the earlier mentioned rectifier circuit, better results are achieved in the terms of more power being available at the output in the form of more voltage and more current. Also, the voltage variations at the output are reduced. This additional power is very useful in our application where we need to transmit large data (around 512 bits) compared to the conventional passive tags where only few bits (30 – 50) are transmitted.

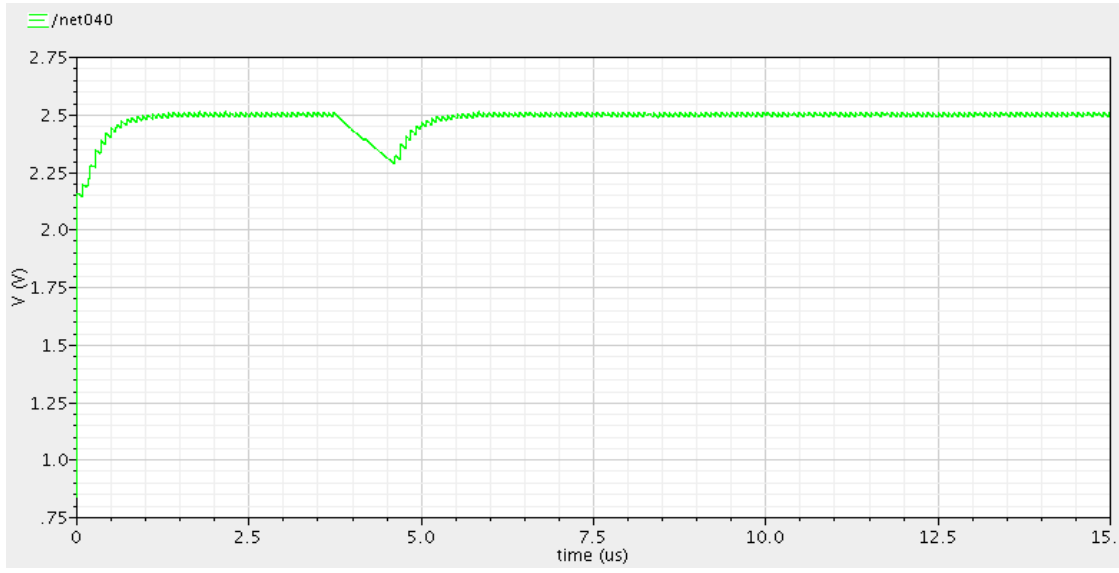


Fig 18 :- Output voltage for modified rectifier circuit

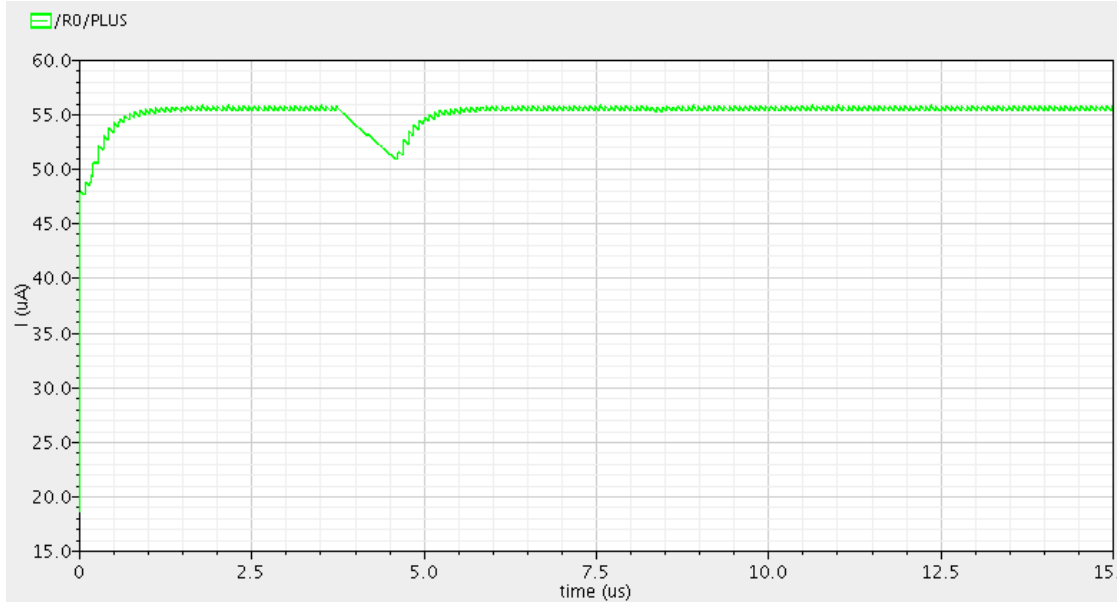


Fig 19 :- Output voltage for modified rectifier circuit

5.4 Demodulator

In conventional passive RFID applications, demodulator circuits are not employed as the only purpose of the tag is to transmit its data once it is energised by the reader signal. Applications which require data to be written/read to and from the tag use demodulators. The function of the demodulator is to efficiently recover the information from an input RF signal and pass it to the digital block to carry out the required operation.

In this project, the role of the demodulator is to extract the reader information which is being sent with the reader signal. This binary representation of this information is 3 bits long, **010**. The output of the demodulator circuit forms the basis of the decision making feature of the tag which authenticates this information pattern and makes a decision whether tag data should be transmitted or not.

For the project, I basically started with the demodulator circuit design in [18] and then combined instances from my previous work to get the final design.

The demodulator design in for this project consists of 2 parts,

- Envelope detector circuit
- Demodulator circuit

The envelope detector actually is a peak rectifier circuit, which gives a DC signal corresponding to the RF signal applied to it. The circuit is implemented as follows,

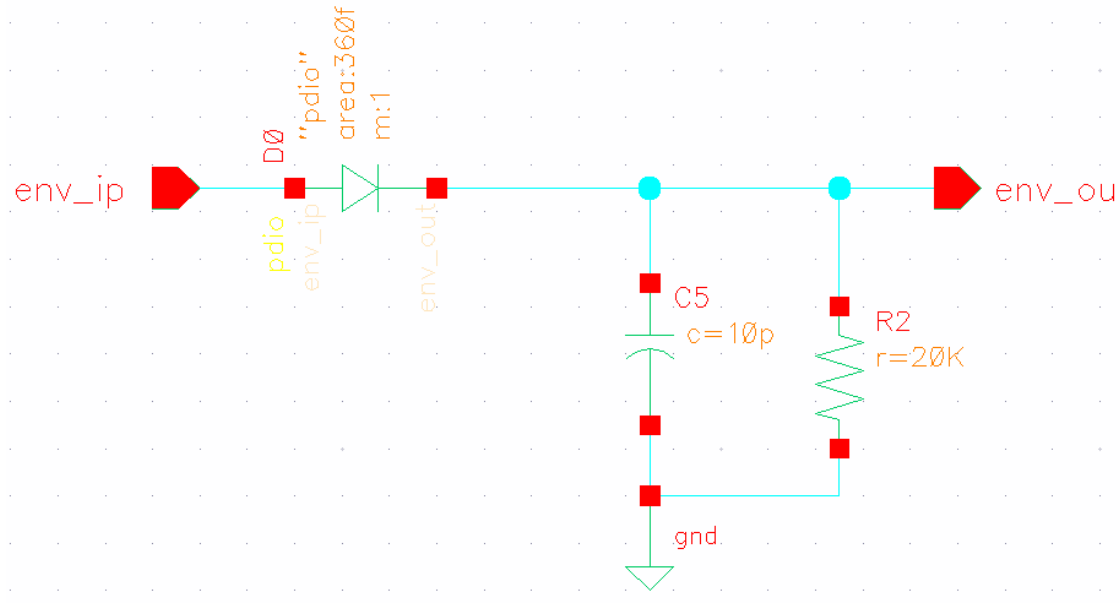


Fig 20 :- Peak detector circuit

When C = 10 pF and R = 500 kΩ, the output is as shown below,

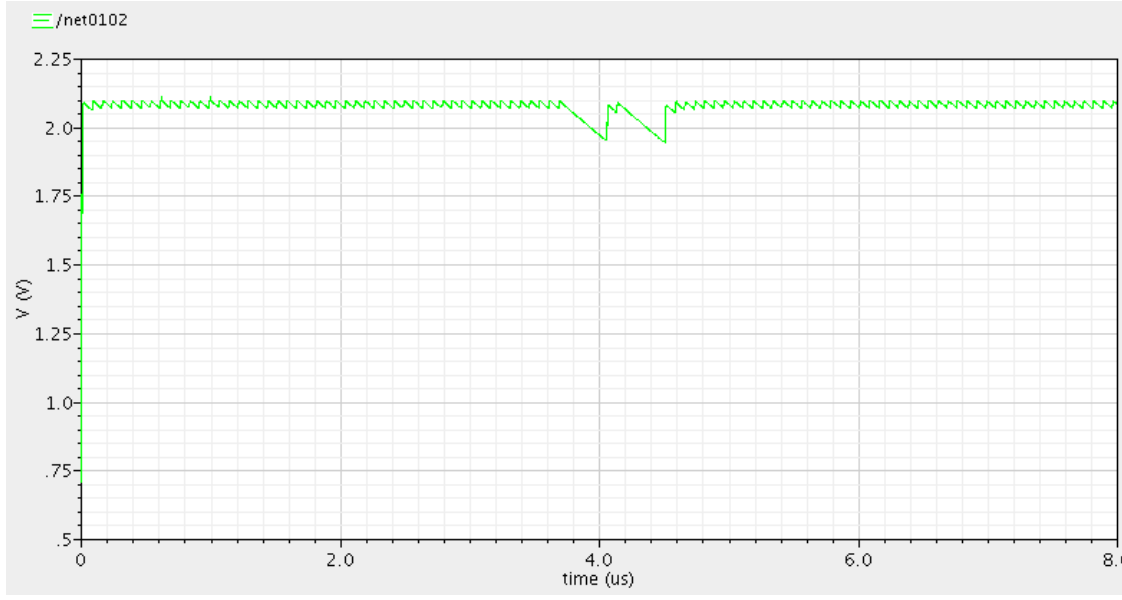


Fig 21 :- Peak detector circuit output

We see from the output that the time constant **RC** is so high then the capacitor discharge interval, that, the detected output follows an almost constant pattern and doesn't really differentiate a 0 (low voltage) or a 1 (high voltage) which represents reader information. However, to detect the varying patterns in the input signal, we need distinguished pattern for a 0 and a 1. For that, the value of the resistor was modified to 20 kΩ and it showed better results,

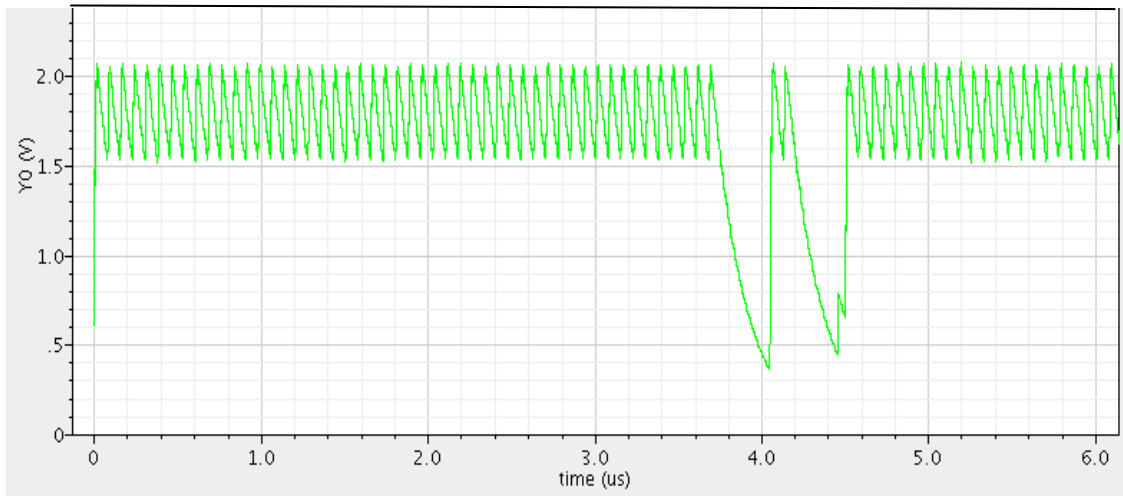


Fig 22 :- Peak detector circuit output for R = 20 kΩ

Referring to Fig 22, although the output voltage does not follow a constant pattern, we can easily distinguish the 0 (low voltage) and the 1 (high voltage) representing the reader information. Also, the resistor value for this implementation is only 20 kΩ as compared to 500 kΩ in the earlier implementation. A NMOS transistor can be used to replace the 20 kΩ resistance thereby saving a lot of circuit space which is very important in IC fabrication. The demodulator circuit began with the implementation given in [18].

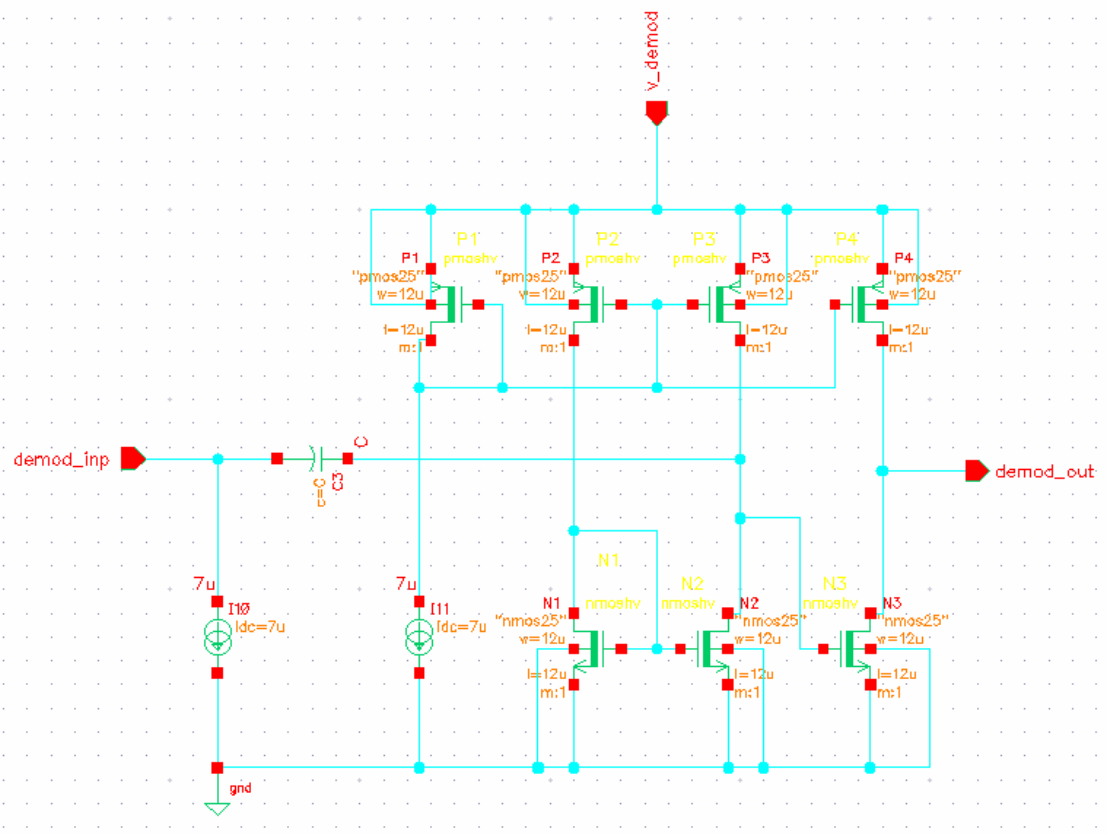


Fig 23 :- Initial Demodulator circuit

The circuit consists of 2 current sources, **I1** (left) and **I2** (right) and a capacitor **C** between them. Transistor **P1** with current source **I2**, provide the bias to the transistors **P2**, **P3** and **P4**. **N1** and **N2** have their gates connected to each other and the common node is connected to the drain of **N1**. Due to this, the amount of current flowing through P2 and N1 is same as that flowing **P3** and **N2**.Thus, we can notice that, **P2** and **P3**, and **N1** and **N2** form a current mirror. Let's assume that current flowing through **P2-N1** is **I3** and that through **P3-N2** is **I4**. Under proper matched conditions,

$$I3 = I4$$

That means, current through **P2-N1**will always try to make current through **P3-N2** as identical as possible. P3 and N2 are two transistors acting as resistors connected between **Vdd** and **gnd**.

The detected RF waveform is connected to the intermediate node connecting **N2** and **N3** through the capacitor **C**. The voltage at this intermediate node varies according to the detected waveform applied through **C**. This signal with voltage variations is applied to the gate of **N3** which turns **ON**/**OFF** the transistor. When **N3** is **ON**, the output **demod_out** is connected to ground through **N3**. When **N3** is **OFF**, demod_out is connected to supply voltage **Vdd** through **P4**.

The output is as shown in Fig 24.

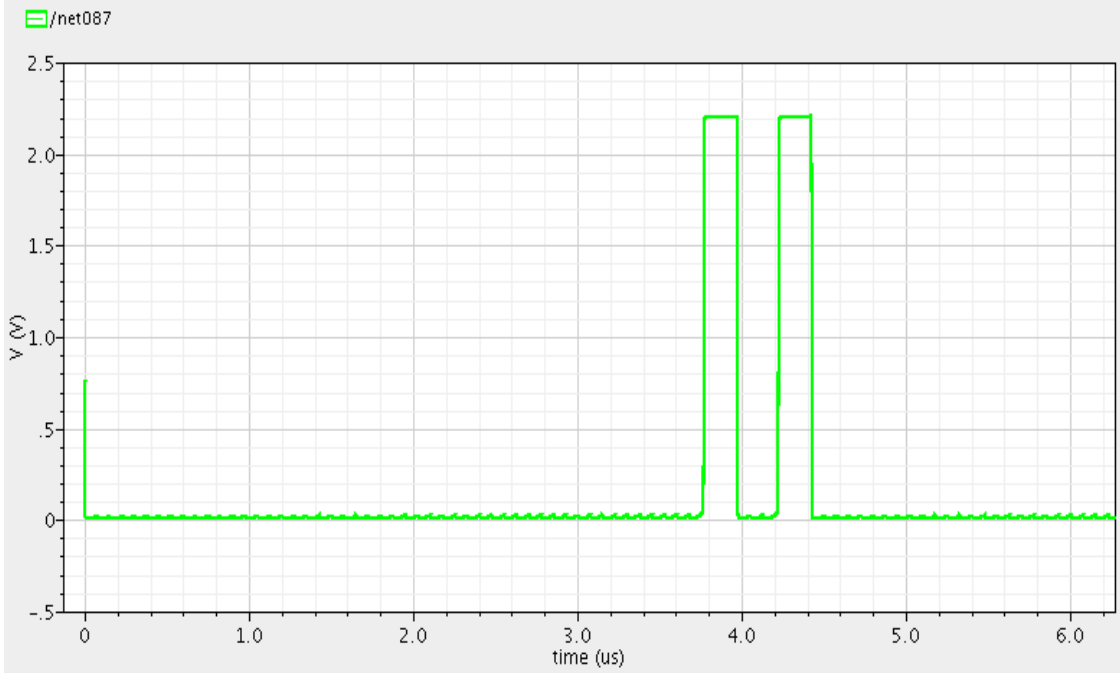


Fig 24 :- Initial demodulator output

This output is the logical representation of the received RF signal.

In this, the RF signal variations are converted into a logical waveform where a **0**, is represented by a high-voltage and a **1** by a low-voltage.

However, the said demodulator design has a disadvantage.

If we closely look at the demodulator circuit in Fig 23, we can see that the capacitor **C** and the equivalent representation of **P3** and **N2** as resistors form a filter network. As the resistor values are high in the order of kΩ's, the filter network formed acts as a High pass filter (HPF). Now, the when the capacitor C discharges, the voltage will decrease which will depend on the time constant **RC**, where **R** is the equivalent resistance seen. If the RC time constant is very high then the discharge interval of C, the voltage decrease will be less.

Fig 25. shows the signal voltage at the intermediate node which is applied to the gate of N3.

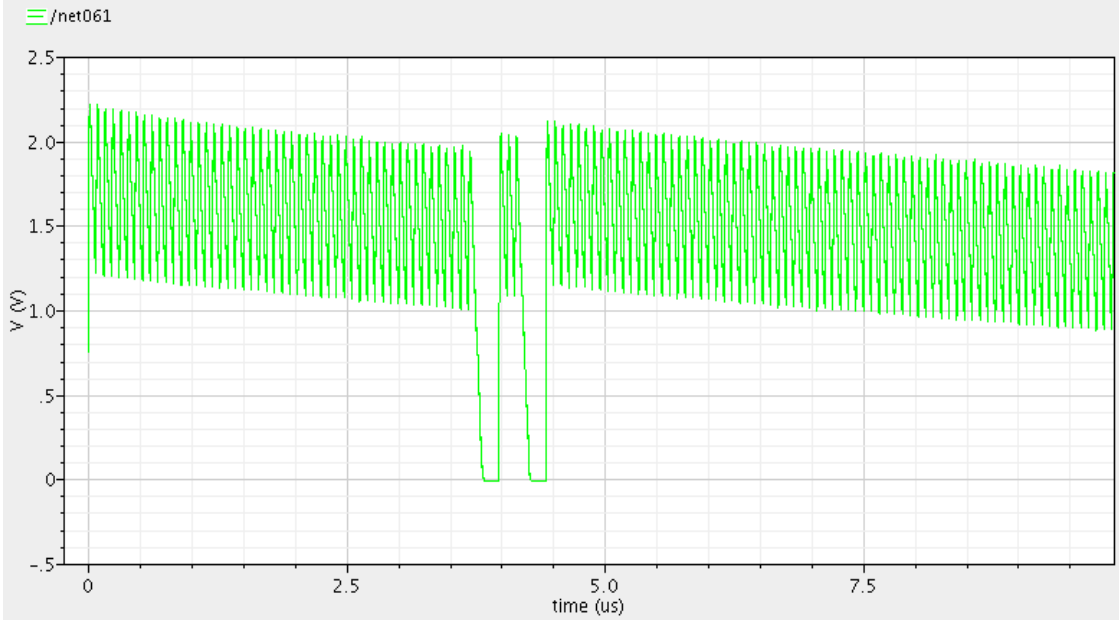


Fig 25 :- Signal variations at the intermediate node connecting P4 and N3

We observe that the intermediate node voltage goes on decreasing as time progresses. As this is the same signal being applied to the gate of N3, the transistor turns OFF again when the gate voltage drops below the threshold voltage of the NMOS. Due to this, the output **demod_out** rise again to Vdd through the PMOS (P4). This gives rise to un-required variations in the demodulator output which is a drawback of this design.

Fig 26 shows the demodulator output following the node voltage variations.

Now, this voltage variations can be reduced if we increase the RC time constant by a big margin. This can be done either by increasing **R** or **C** or both. However, there are limitations on the value of **R** as the equivalent MOS resistance can be increased to only few tens of kilo-ohms considering the design constraints. The formulae for output resistance calculation for MOS is [17],

$$R_0 = V_A / I_D \quad \text{..... (8)}$$

where,

I_D = drain current

V_A = early voltage, which is a process technology parameter

$= V_A' * L$

L = channel length

V_A' = process technology dependent (typically 5 V/µm – 50 V/ µm)

Fig 26, 27 and 28 show node voltage variations for different values for capacitor **C**.

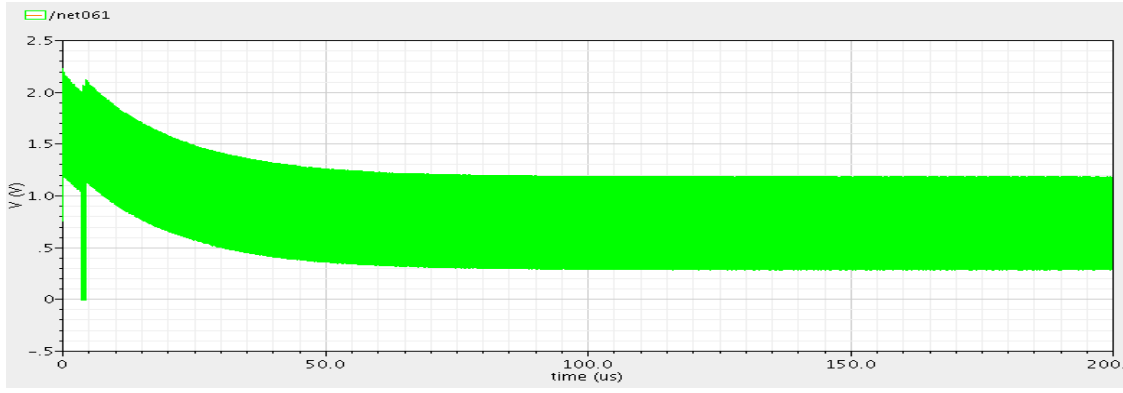


Fig 26 :- Node voltage variations for C = 10 pF

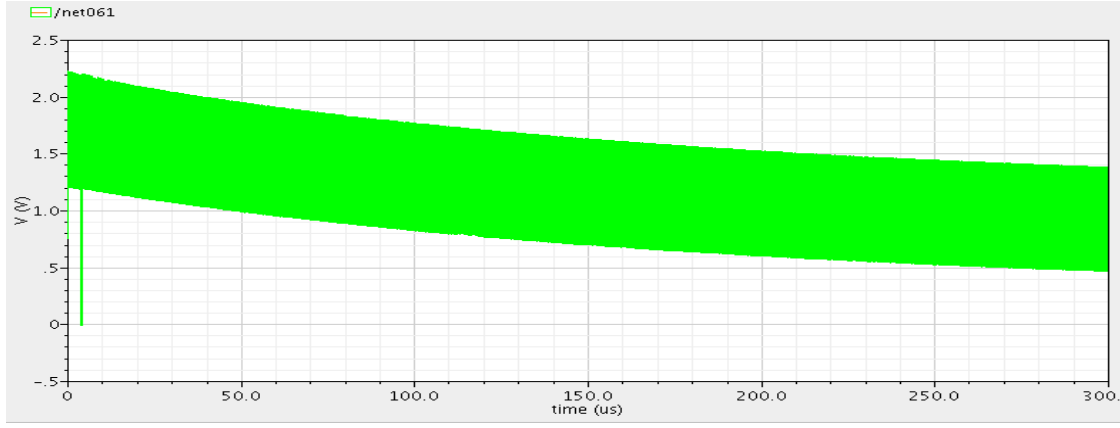


Fig 27 :- Node voltage variations for C = 100 pF

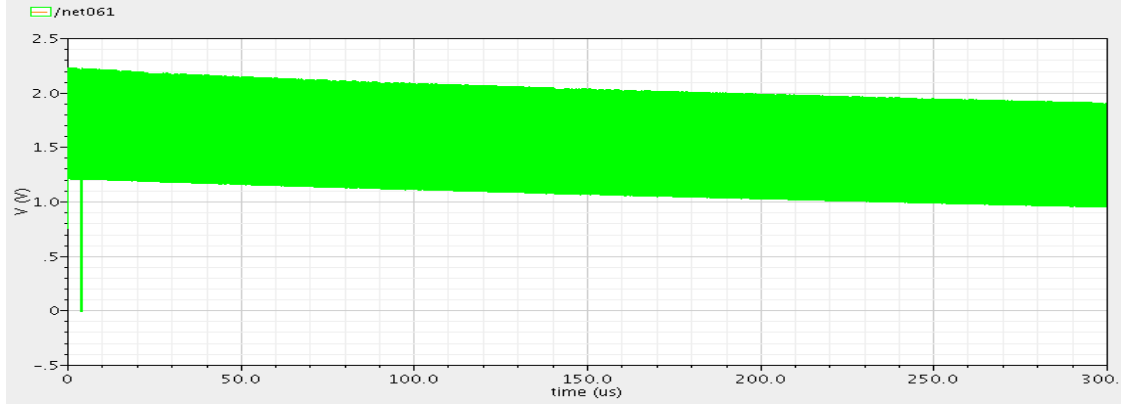


Fig 28 :- Node voltage variations for C = 500 pF

The threshold voltage for N3 is around 730 mV.

Looking at Fig's 26, 27 and 28, we can notice that as soon as the node voltage falls below the threshold voltage of N3, N3 will turn OFF and the demod_out rises to **Vdd**. This rise is highly undesirable as a high voltage in demod_out indicates a **0** in the reader signal which is not true as, apart from the 3 bit reader information, the signal actually never goes low.

Fig 29 and 30 show the demodulator output at the output pin demod_out.

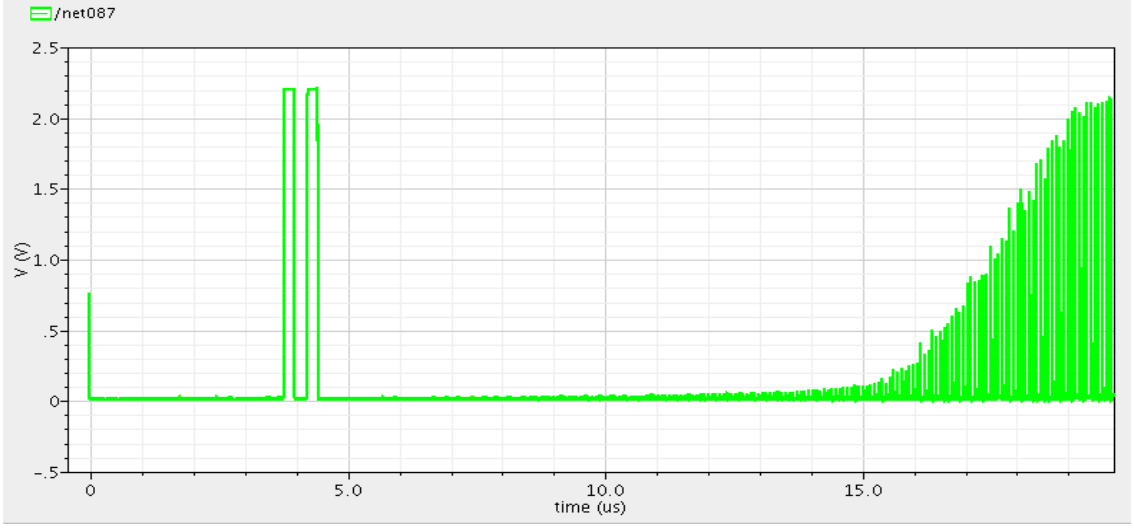


Fig 29 :- Demodulator output for C = 10 pF

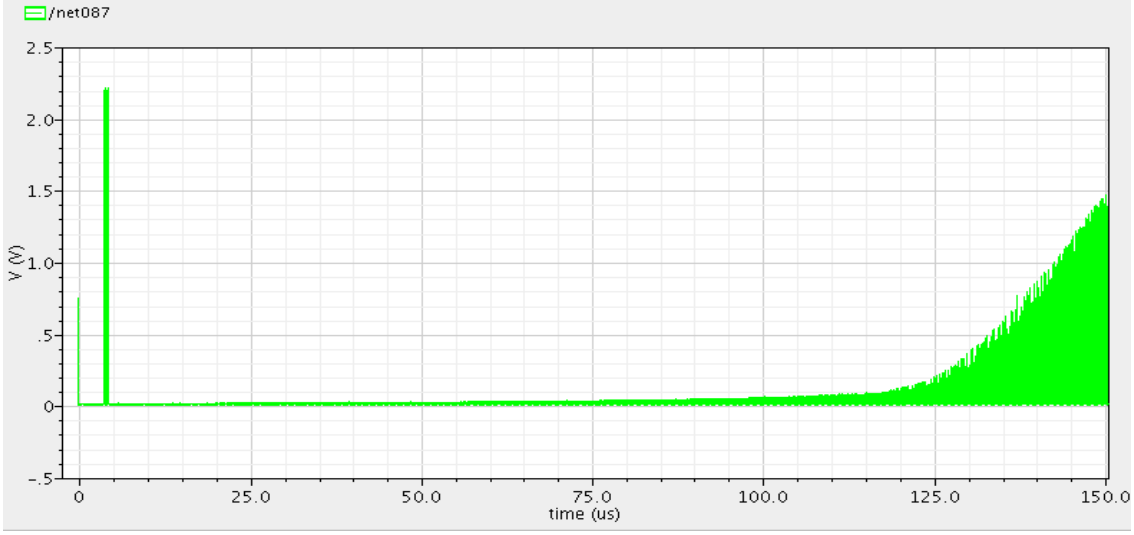


Fig 30 :- Demodulator output for C = 100 pF

When C = 10 pF, the demodulator output again starts rising after 15 µs and when C = 100 pF, output starts rising after 125 µs. The voltage variations can be avoided or greatly reduced by increasing the value of the capacitor C to a very large value around 400 pF – 500 pF. However, the more the value of capacitor, more the space it takes and for IC fabrication, there are limitations on the amount of capacitor value and sizes which can be embedded. And also as we are targeting large transmission of data from tag (at least 500 bits), the wrong demodulator output would make decoding difficult, thereby affecting the decision making ability of the tag.

The demodulator circuit of Fig 23 was then modified and the drawback of the design was corrected. Fig 31 shows the modified demodulator circuit,

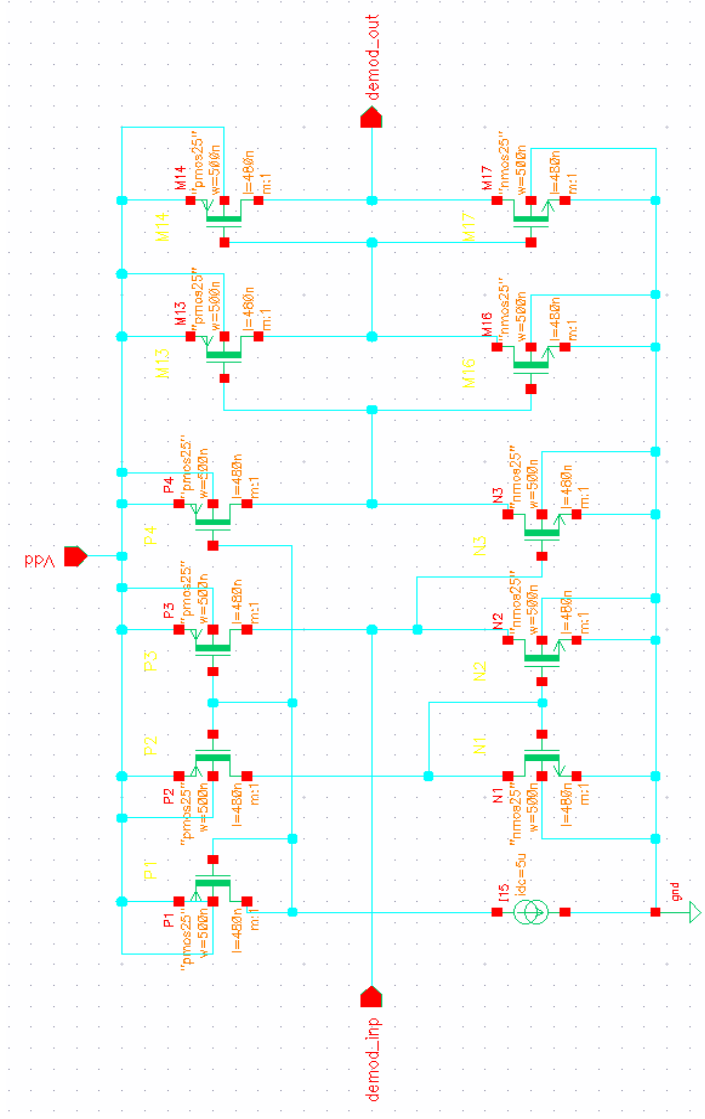


Fig 31 :- Modified demodulator circuit

The biasing for the transistors **P1**, **P2**, **P3** and **P4** is done by a constant current source **I1**. Here only one current source is used compared to the earlier one. The current source biasing is the same that was used in the **OPAMP** design shown in my interim report. The capacitor **C** is removed and the detector output is directly connected to the intermediate node. The overall circuit functions in the same manner as the earlier one. As, currents through **P2-N1** and **P3-N2** are almost identical and very small , the voltage variations at the node are easily picked up by the gate of **N3** which turns **ON**/**OFF** depending upon gate voltage.

Fig 32 and 33 show the node voltage and the demodulator output for the modified circuit.

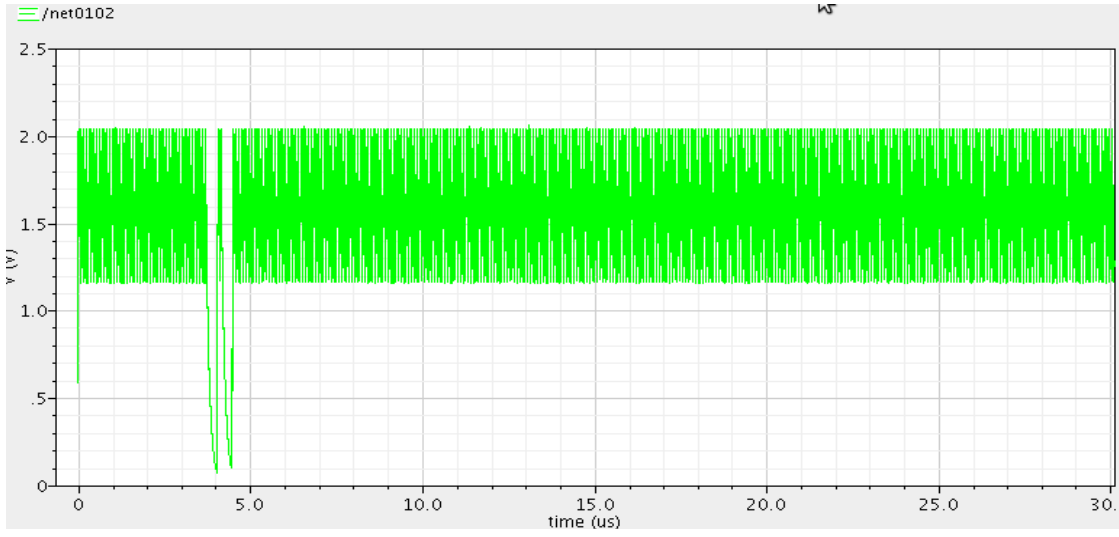


Fig 32 :- Node voltage variations for modified circuit

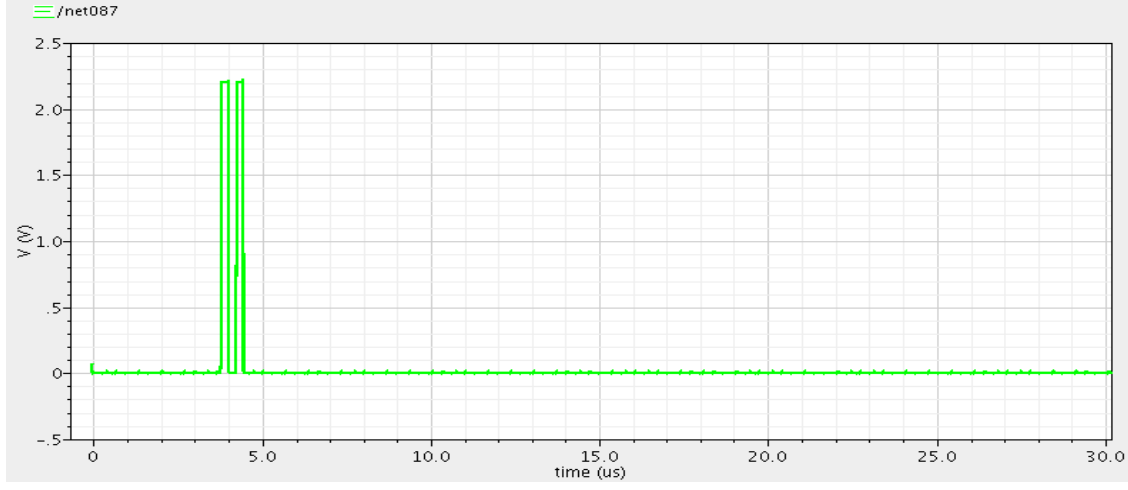


Fig 33 :- demodulator output for modified circuit

Here, we can clearly observe that the node voltage maintains its nature as expected and hence we get a proper demodulated output waveform for our reader signal. This gives us the final demodulator module as shown in Fig 34.

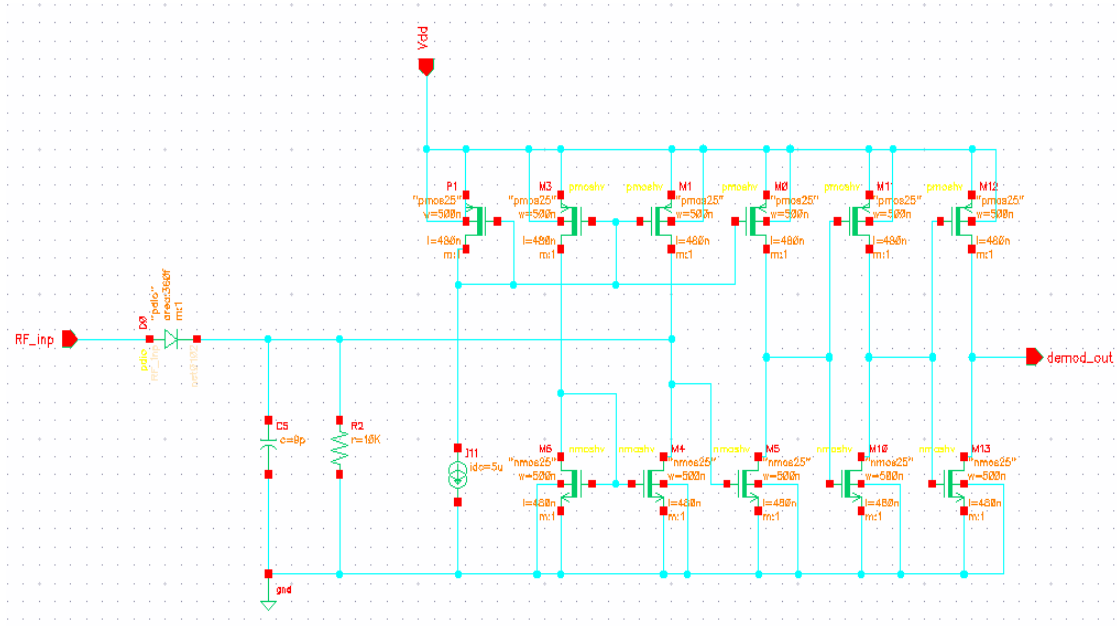


Fig 34 :- Demodulator module implementation

Two additional inverting stages have been added to smoothen the demodulator output. This output is now made available to the decision making module to authenticate the reader.

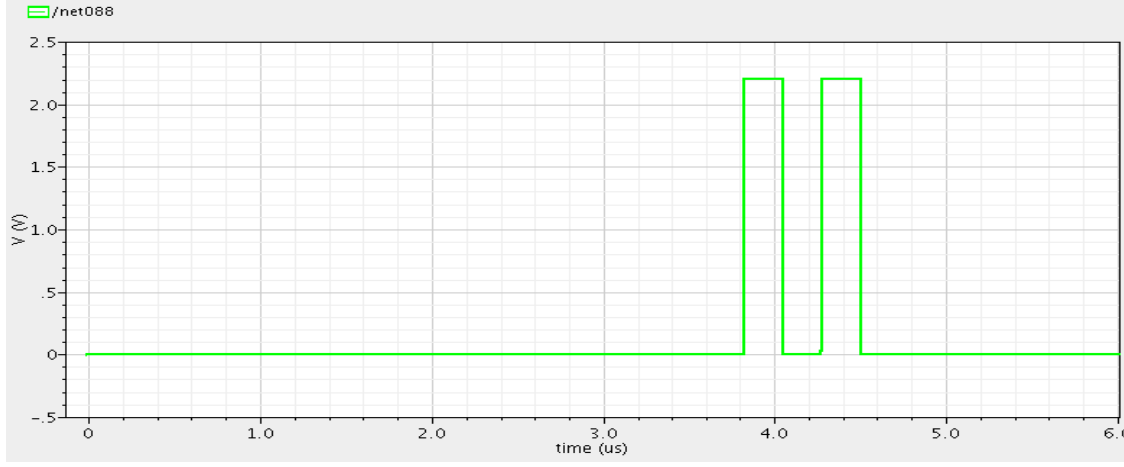


Fig 35 :- Final demodulator module output

5.5 Decision making

This is the most important feature of the project. Conventional passive RFID do not embed this block as their basic function is just to transmit data when energised. In cases, where data has to be written / read to and from the tag, reader signal contains the appropriate information so that tag can accordingly make a decision. However, security and authentication are two factors that have to been taken care when transmitting information wireless. A lot of effort is put in to achieve privacy of data against unauthorised readers.

Fig 36 gives a general view of transfer of the tag data,

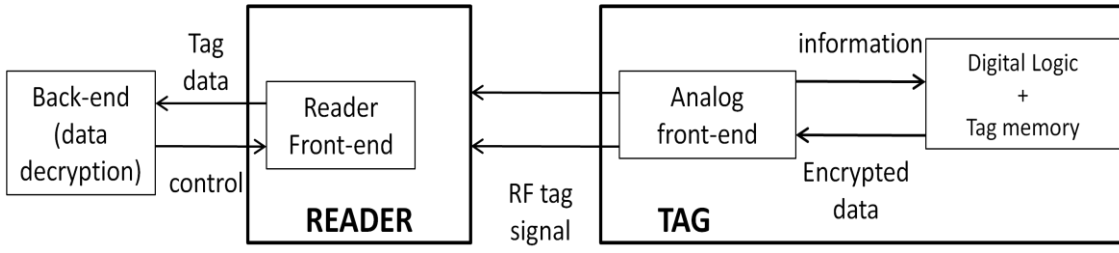


Fig 36 :- General flow of tag data within a RFID system

Various Cryptographic methods are implemented on the tag data before it is loaded in its memory. When the tag's analog front-end interrupts the digital logic block, the data flows from the tag memory which is actually the encrypted version of the actual data. This data is then modulated on a carrier signal and transmitted. Reader on receiving the tag signal, extracts the data from it and sends it to the back-end (computer in most cases), which decrypts the tag data to make it readable. The back-end then sends an appropriate control signal to the reader after processing the data. This encryption and decryption of tag's data ensures that only authorised readers can get access to the actual data stored in the tag and accordingly use it.

This data protection is very necessary in applications where the tag stores sensitive information, like a person's identity, access code. Additional security measures like reader authentication can be implemented to stop the tag from sending data and thereby avoiding illicit tracking.

In this project, I have worked on reader authentication by embedding a simple decision making logic within my design. This block will have the tag demodulator output as its input and will work on the data to output a GO/ NO-GO signal. Depending on the nature of this signal, the system will decide whether tag data should be transmitted or not.

Before talking about the decision making block in detail, let me first explain how the tag data is generated within the tool.

Tag data

As the system is being designed using a tool, the source of data that I have used is an element from the **analogLib** library within the tool. This design element is called **vpulse**. vpulse outputs a pulsed waveform. The properties of vpulse has been set such that it will transmit data wherein a **0** in the tag data will be represented by a low-voltage (0V) and a **1** will be represented by a high-voltage (1V).

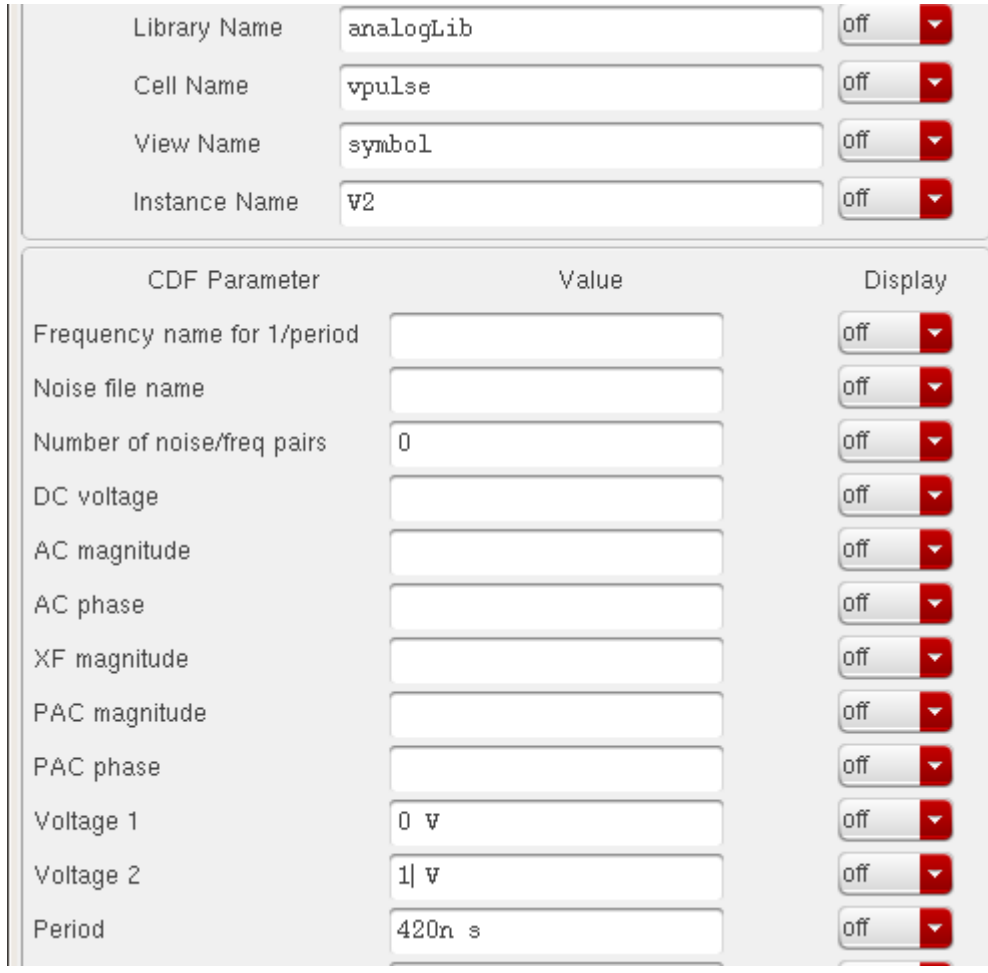


Fig 37 :- vpulse property settings

Here, each pulse has been set with a width of 420 ns. The return link frequency is 14.28 MHz, whose time duration is 70 ns. Care has taken in choosing an appropriate pulse width for tag data so that the backscattered data can be distinguished easily by the reader. In real scenario, the vpulse will be an actual memory block which will transmit data only when the digital block issues a GO ahead signal. However, from the design point of view, I have delayed the pulse transmission by 4 µs. When vpulse starts transmitting data, the decision making logic will interact with the data to **continue** or **stop** its transfer to the modulation block depending on the GO / NO-GO signal status.

The output of vpulse element is as shown in Fig 38.

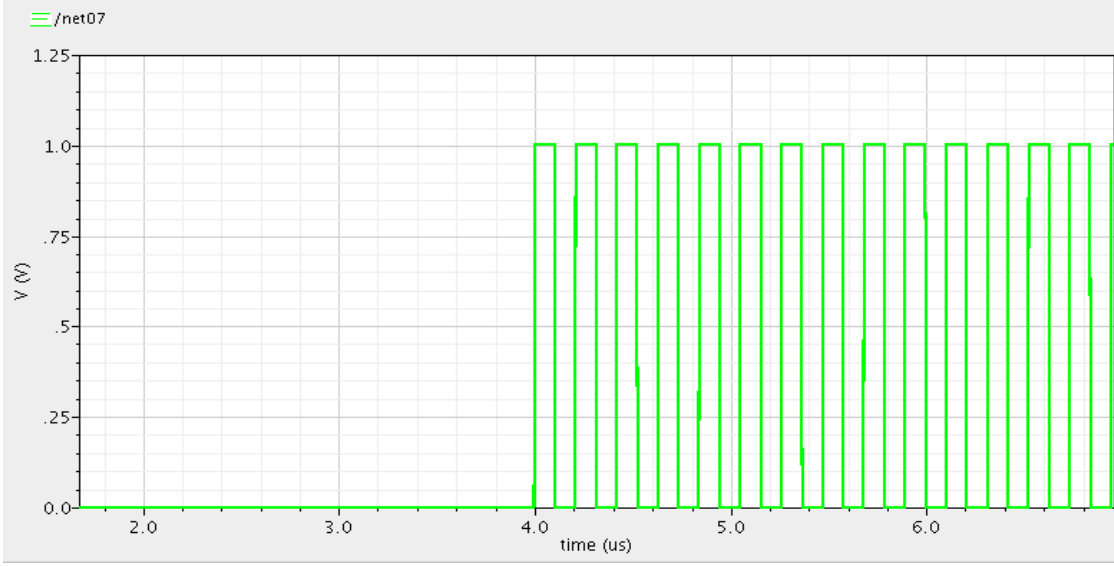


Fig 38 :- vpulse element output data

Now, let's continue with the decision making logic.

The decision making logic consists of 2 parts,

1. Reader data authentication
2. Latch circuit and GO / NO-GO decision

The reader data authentication block works on the demodulator output and outputs a positive pulse when the data is authenticated. In case if the reader authentication fails, we do not see any positive pulse. Instead, it outputs a constant zero signal indicating failed reader authentication.

The latch circuit will latch on the data from the reader authentication block. The output will go high as soon as the reader authentication is done. During the fail scenario, the latch output will remain low thereby preventing the tag data to flow. Keeping in mind the complexity of the tag structure, the decision making circuit has been designed using simple logic gates which are implemented in analog form using CMOS logic.

5.5.1 Reader authentication

The reader authentication is done in two stages. The first stage is the data processing stage and the next stage is the decision making stage.

Fig 39 shows the block view of reader authentication logic.

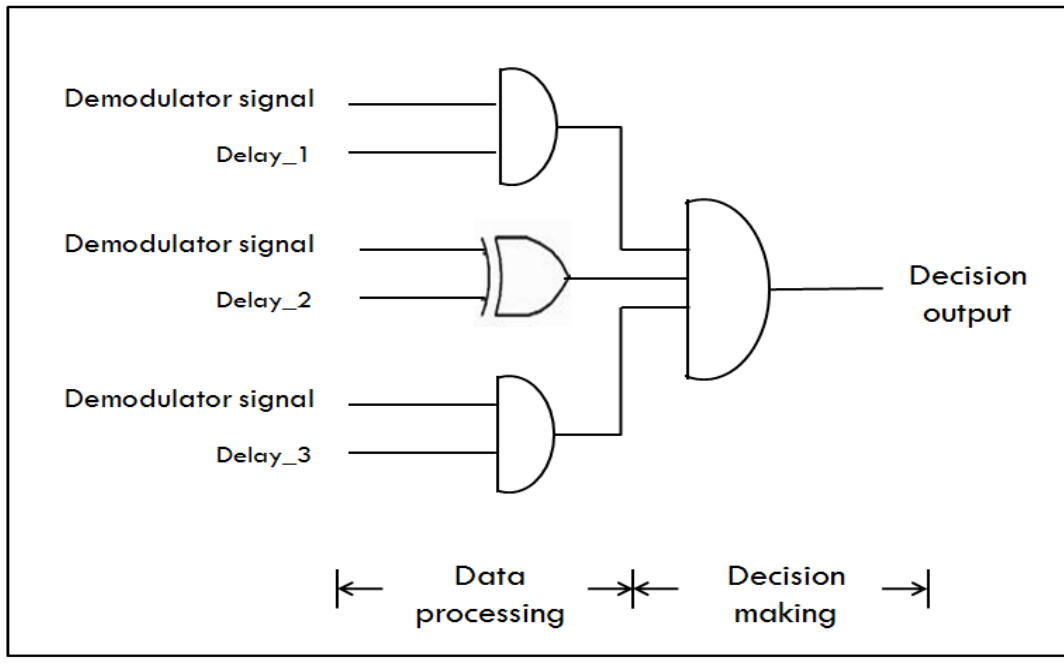


Fig 39 :- Block view of reader authentication logic

The **Delay_1**, **Delay_2** and **Delay_3** are the delayed versions of the demodulator signal. The signal representations are as shown below,

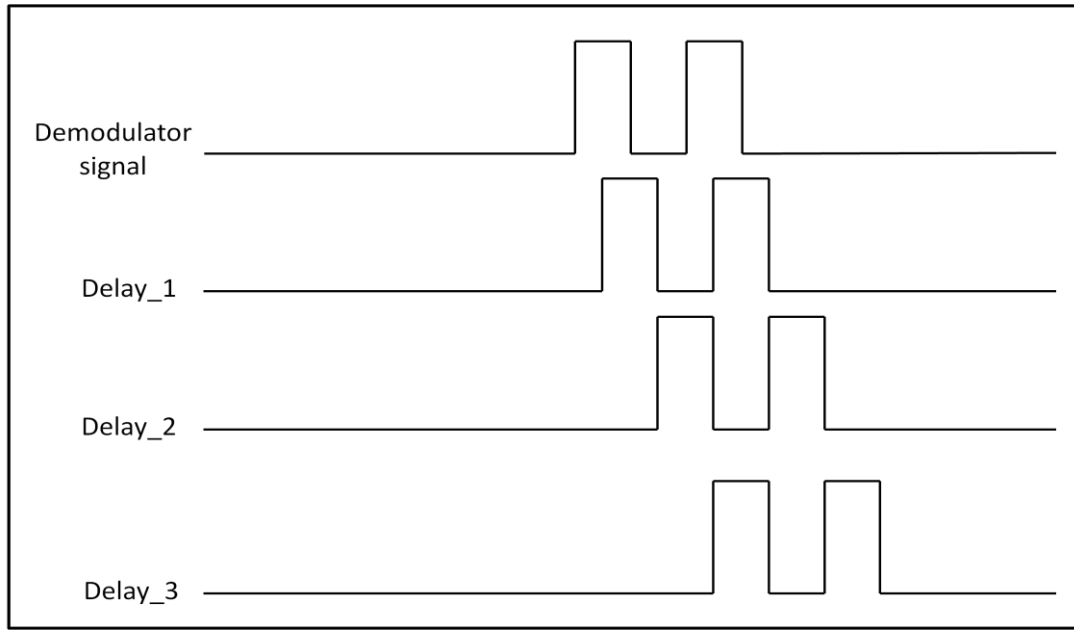


Fig 40 :- Demodulator signal, Delay_1, Delay_2 and Delay_3 representation

The simplest way to delay a signal is by using CMOS logic Inverters. Here as well, I have used inverters with capacitor at its output and generated 3 delayed versions of the demodulator signal. The basic CMOS logic inverter has the following advantages [17],

- They can present a symmetrical voltage-transfer characteristics, which results in wide noise margins
- The static power dissipation in both its states is zero. Though we see dissipation due to leakage currents
- They have low output resistance which makes them less sensitive to noise effects and other occurring disturbances

Fig 41 shows a single inverter stage with a capacitor C between its output node and the ground.

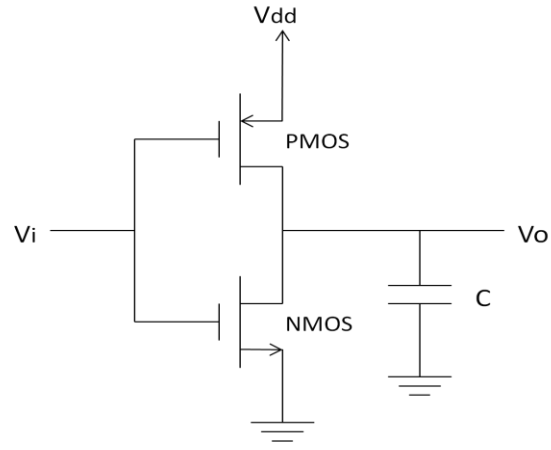


Fig 41 :- Capacitive loaded CMOS inverter

To get the 3 delay signals, multiple stages of the above circuit have been implemented. As, in general, input resistance of the inverter is infinite as ($I_G = 0$), one single inverter can drive a large number of similar stages with no loss in the transferred signal. However, with addition of every inverter stage, the load capacitance on the driving inverter increases and this slows down the operation.

It is this slowing down in the switching time of the inverter that introduces a propagation delay and we get the signals Delay_1, Delay_2 and Delay_3.

Now let's see the delay equations in detail,

Fig 42 shows the input and output waveform of the discussed inverter circuit,

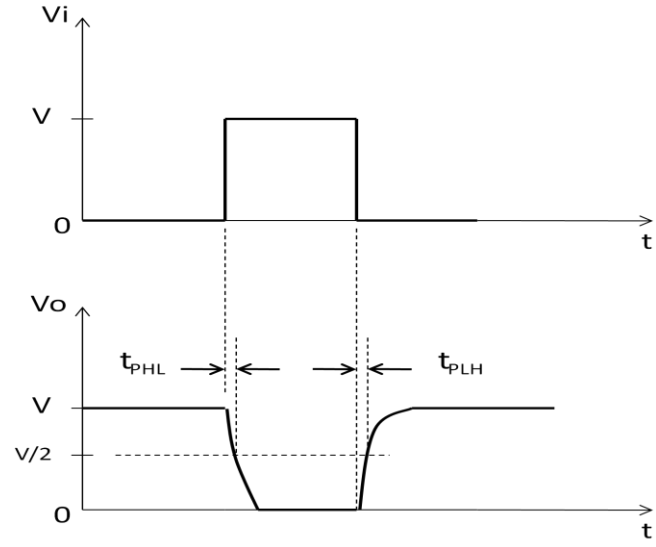


Fig 42 :- Input and output waveforms of a capacitive loaded CMOS inverter

where, HL indicates the high-to-low output transition
LH indicates the low-to-high output transition

The equations for $\mathbf{t_{PHL}}$ and $\mathbf{t_{PLH}}$ are [17]:-

$$t_{PHL} = \frac{2C}{K_n' (W/L)_n (V_{DD} - V_t)} \left[\frac{V_t}{(V_{DD} - V_t)} + \frac{1}{2} \ln \left(\frac{(3V_{DD} - 4V_t)}{V_{DD}} \right) \right] \quad \text{..... (9)}$$

t_{PLH} is identical to t_{PHL} expect for $\mathbf{k_n' (W/L)_n}$ is replaced with $\mathbf{k_p' (W/L)_p}$.

The propagation delay t_P is given by,

$$t_P = (t_{PHL} + t_{PLH}) / 2 \quad \text{..... (10)}$$

Lets us calculate $\mathbf{t_{PHL}}$ for standard values which are used in VLSI circuits for our case,

Substituting C = 7.2 pF, $(W/L)_n = 2$, $(W/L)_p = 4$, $V_{DD} = 2.25$ V, $V_{tn} = V_{tp} = 0.725$ V, $k_n' = \mu_n C_{ox} = 20\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 10\ \mu A/V^2$, we get

$\mathbf{t_{PHL}} = \mathbf{t_{PLH}} = 30.14$ ns

hence, $\mathbf{t_P} = (t_{PHL} + t_{PLH}) / 2 = 30.14$ ns

This is the value of propagation delay for one stage of a capacitive loaded CMOS inverter. With the addition of more stages, t_p increases and hence the overall delay of the signal at the output of the final stage. We can change the value of C according to our convenience to get a particular delay.

Fig 43 shows the circuit implementation to generate the delay signals Delay_1, Delay_2 and Delay_3.

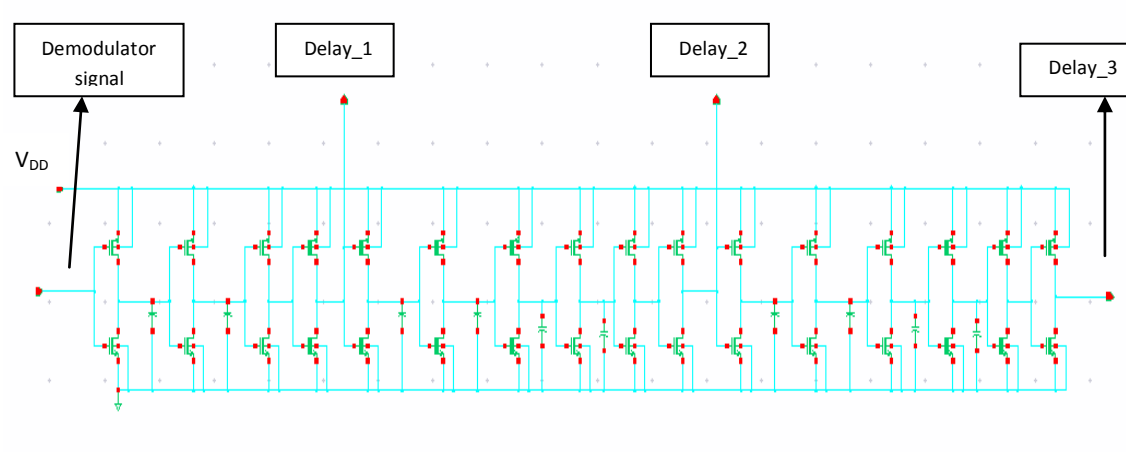


Fig 43 :- circuit to generate delay signals

The delay signals are individually processed with the demodulator output signal as per shown in Fig 39. The output of the data processing stage is,

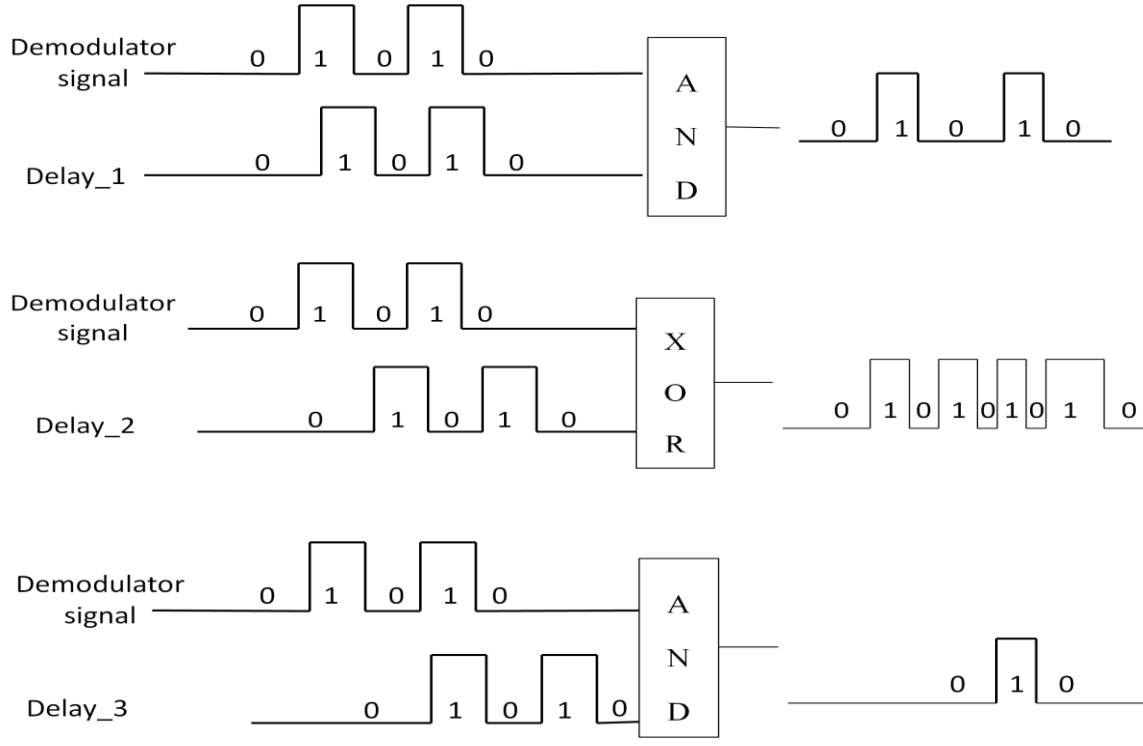


Fig 44 :- Data processing stage outputs

The output signals of the data processing stage are fed to next stage which is a 3-input AND gate.

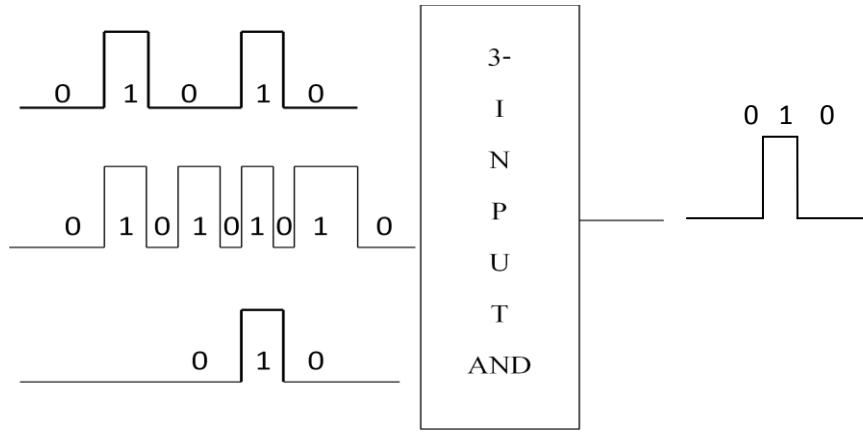


Fig 45 :- stage 2 output of reader authentication block

The output of the second stage is a short positive pulse indicating that the reader data embedded in the reader RF signal is **010**. Any other 3-bit combination apart from **010**, will show no result in the second stage indicating that the reader is not a valid reader and hence, data from tag should not be transmitted.

Fig 46 and 47 show the circuit level implementation of the data processing (AND gate) and decision making stage of the reader authentication block,

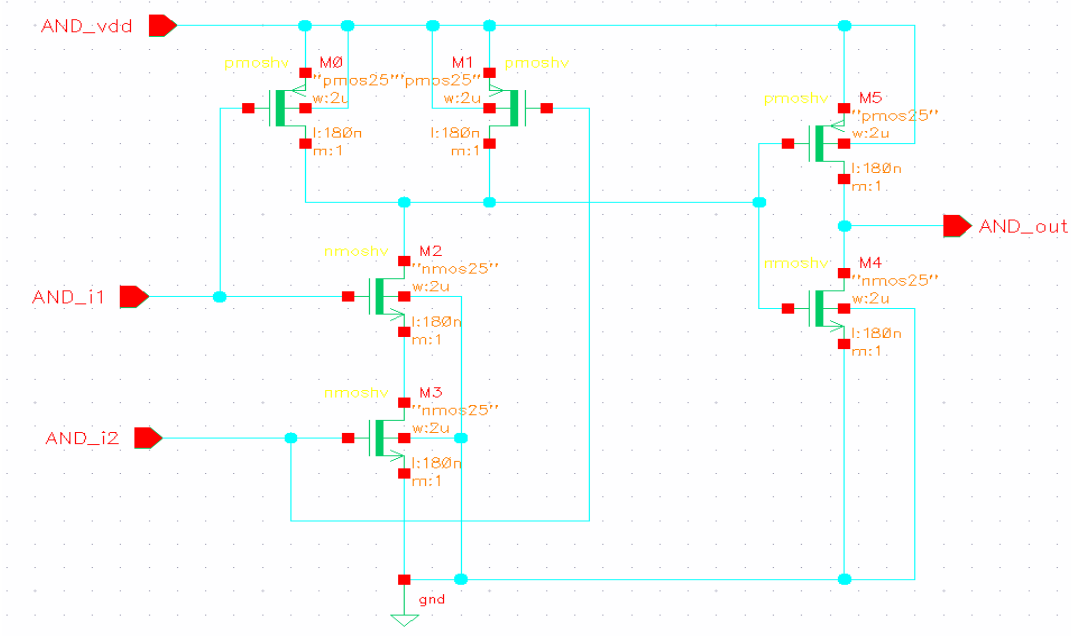


Fig 46 :- AND gate implementation

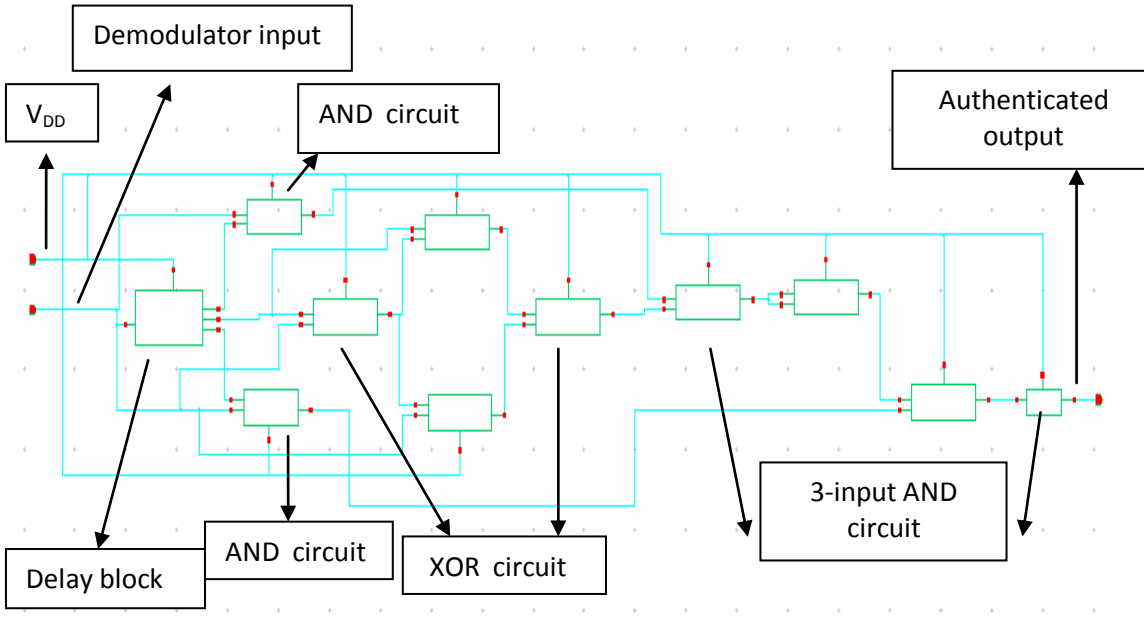


Fig 47 :- Symbol level implementation of the reader data authentication block

The XOR gate is implemented as,

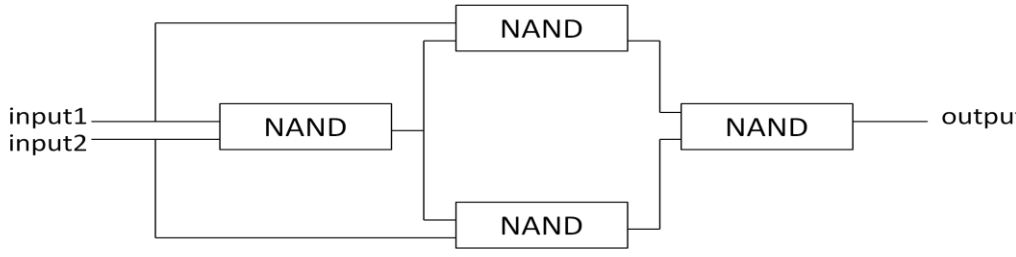


Fig 48 :- XOR gate implementation

The 3-input AND gate is implemented as,

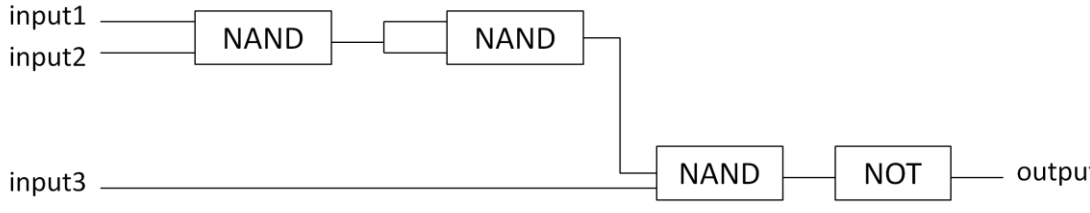


Fig 49 :- 3-input AND gate implementation

The final output which is the authenticated reader output obtained from the circuit implementation shown in Fig 47 is as shown,

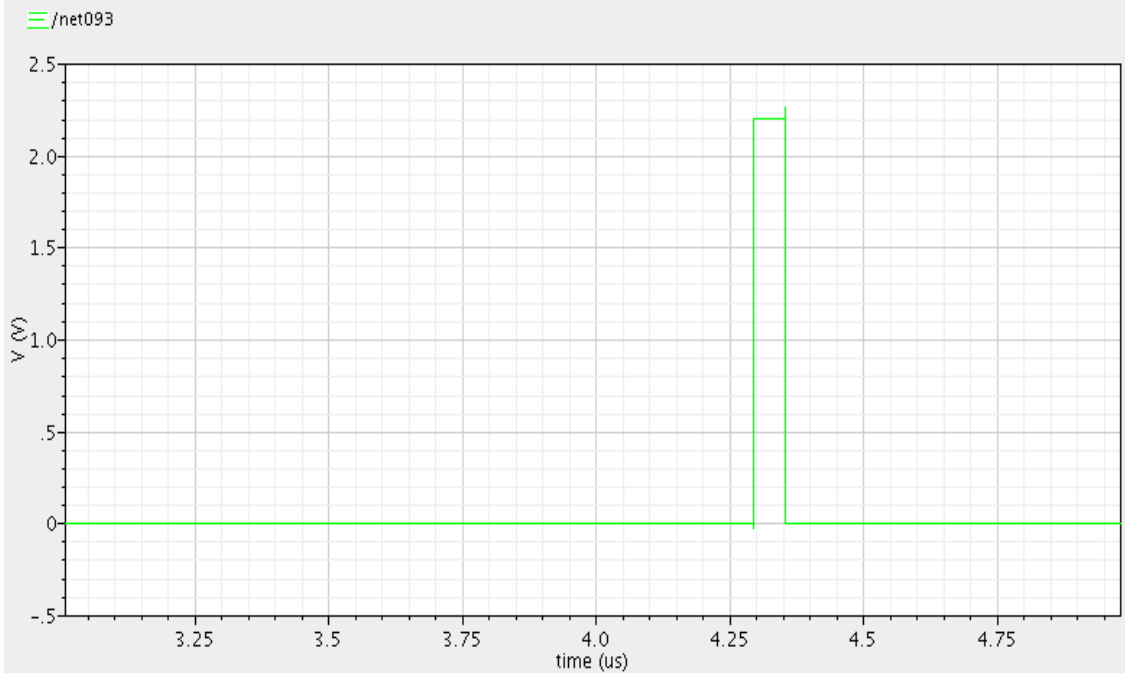


Fig 50 :- Reader authentication block output

It can be seen that when the reader information is **010**, we get the above output from the first block of decision making unit. This output is the one expected for correct reader authentication and is the same as seen in Fig 45.

Reader authentication block output for other reader information bits 000, 001, 011, 100, 101, 110 and 111 are shown in section 7. On comparing the output of Fig 50, and then one in section 7, we can see that the tag in our design will generate this positive pulsed wave only when it finds the correct reader. Also, the transistor level implementation for NAND and NOT gates are shown in the APPENDIX.

Now that we have got the reader authenticated, we need to start the transmission of tag data. For this, the output first will be sent to the second module of the decision making block, which is the **Latch circuit and GO / NO-GO decision**, the details of which are given in section 5.5.2.

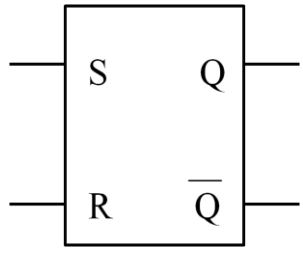
5.5.2 Latch circuit and GO / NO-GO decision

Here, the output obtained from reader authentication block is latched to a particular state whose nature will indicate whether the authentication was successful or not.

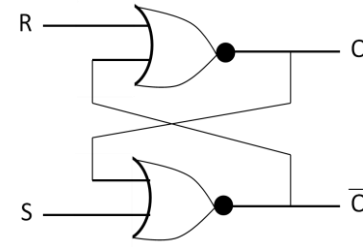
The output of the AND circuit indicates one of the following 2 scenarios,

- Authenticates fails
  Here, data is present but latch is zero(false). Therefore output is a zero. This means that the data is not allowed to pass through.
- Authenticated passed
  Here, data is present and latch is true. Therefore output is the tag data. This means that data is allowed to pass through.

To latch the reader authenticated output, I have used a simple Ser-Reset latch (SR latch). It has been implemented using cross-coupled NOR gates. Fig 51 shows the symbol of SR latch, circuit implementation and truth table.



a)



b)

S	R	OUTPUT
0	0	current state = previous state
0	1	Q = 0
1	0	Q = 1
1	1	race condition

c)

Fig 51 :- a) SR Latch symbol, **b)** SR Latch circuit, **c)** truth table

SR Latch working is as follows,

- When S = R = 0 (low), the feedback mechanism makes outputs Q and Q' maintain their current state. Here Q' is a complement of Q.
- When S = 0, R = 1 (high), the output Q is forced to 0 (low state). Q will maintain its state even when R turns to low state.
- When S = 1 (high), R = 0, the output Q is forced to 1 (high state). Q will maintain its state even when S turns to low state.

- When S = 1, R = 1, a race condition occurs and the outputs of NOR gates go to zero. This is a condition which is inappropriate and should be avoided. Here the logical equation Q = **not** Q' no longer holds true. In certain applications before the output settles, the race condition gives rise to damped oscillations resulting in errors in high frequency digital circuit.

For out project, we are interested in the third scenario (S = 1 and R = 0). For this, the SR circuit is implemented as follows,

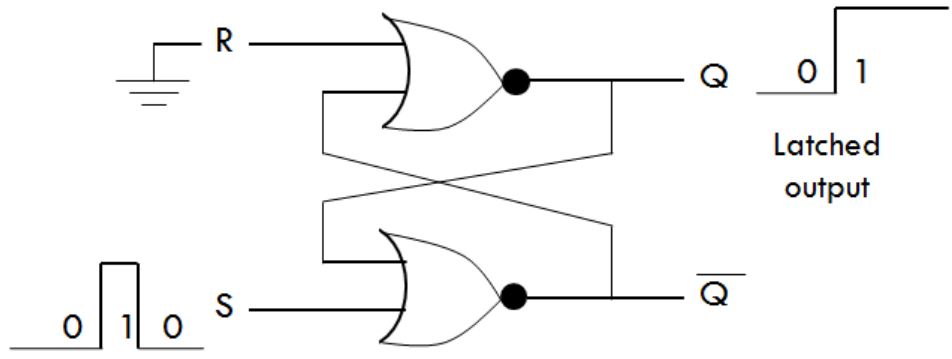


Fig 52 :- Our SR latch implementation

Here, the authenticated output obtained from the Reader authentication module is applied to the S pin. The R pin is grounded. So, R will always be 0 (low).

When we hit the condition S = 1 and R = 0, Q goes high. When S returns to low stage, we have the condition S = 0, R = 0 and hence, Q maintains its output which was high. In this manner, the signal is latched to its positive state.

In the case when the reader was not authenticated, the S pin will always be 0 (low). Referring to truth table, when S = 0, R = 0, the output will maintain its state, which will be zero as in our case, the initial state of Q is always low (0).

Fig 53 shows the transistor level implementation of **Fig 52**. While **Fig 54**. shows the input and **Fig 55** shows the simulated output for the latch circuit when reader is authenticated. **Fig 56**. shows the simulated output when the authentication fails. Comparing the two outputs, we can conclude that the **GO / NO-GO** decision making is successfully implemented using the design presented.

In real scenario, this latched signal will then be passed to the digital block of the tag system, which will then interrupt the memory to start transmitting data bits. As, from the system design point of view, we do not have any digital block or memory element, I have directly used the **vpulse** element of the AnalogLib in the design tool to go ahead and complete the remaining process.

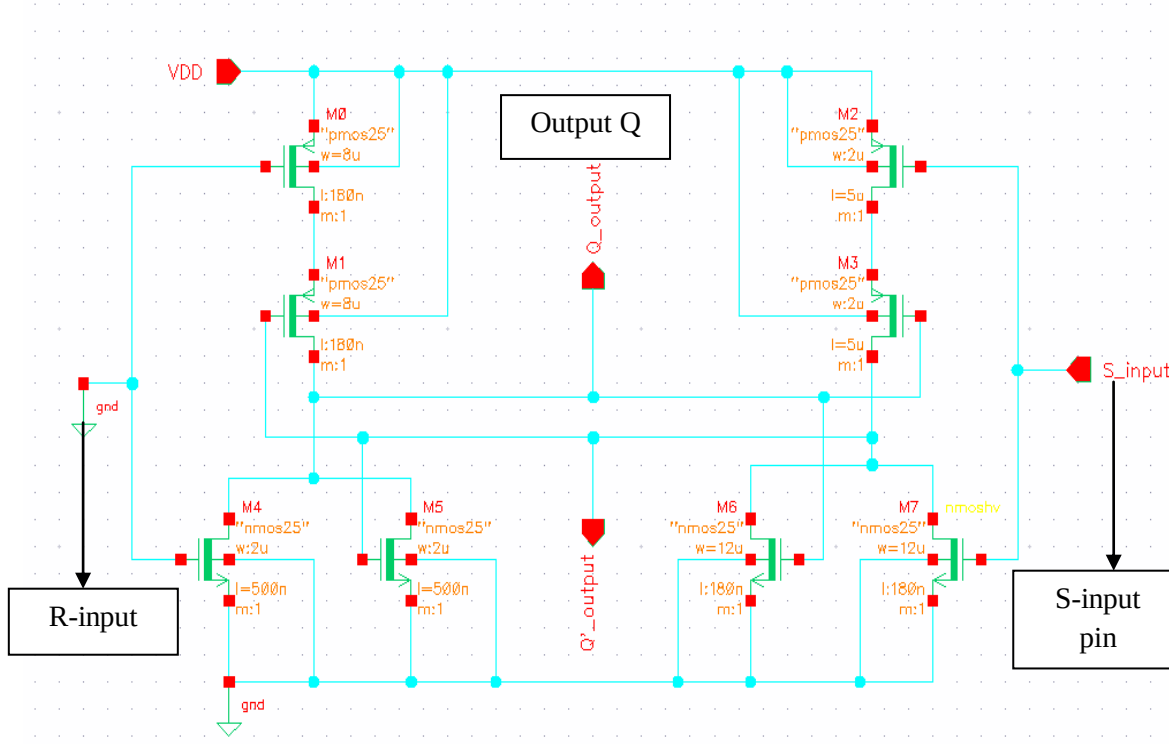


Fig 53 :- Transistor level implementation of SR Latch

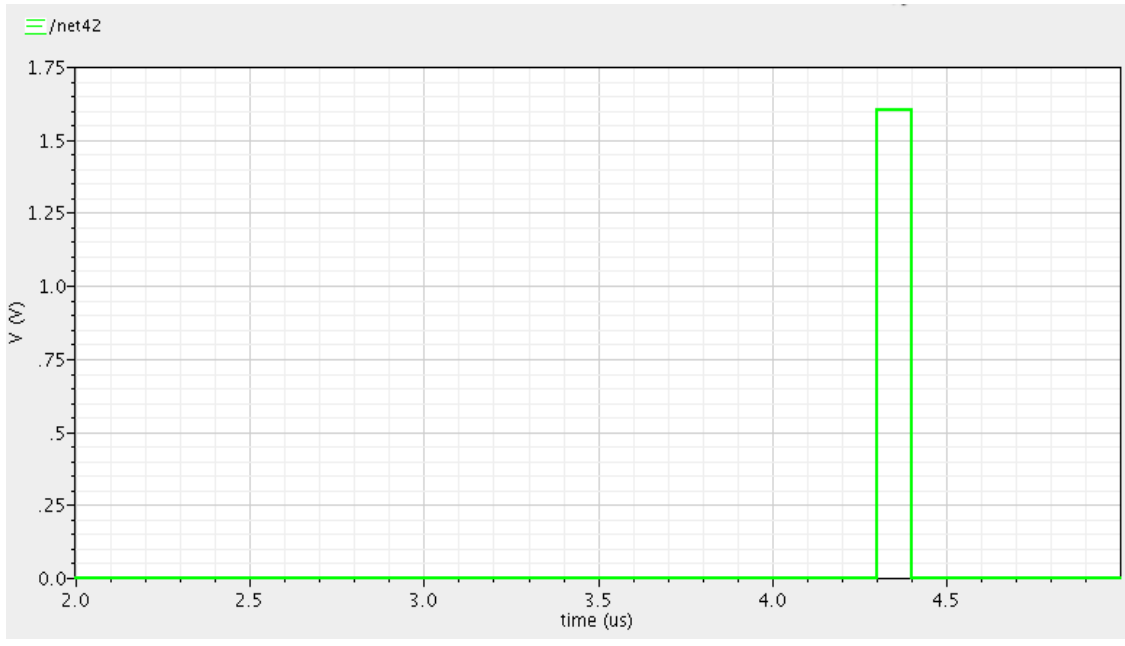


Fig 54 :- S input to SR latch

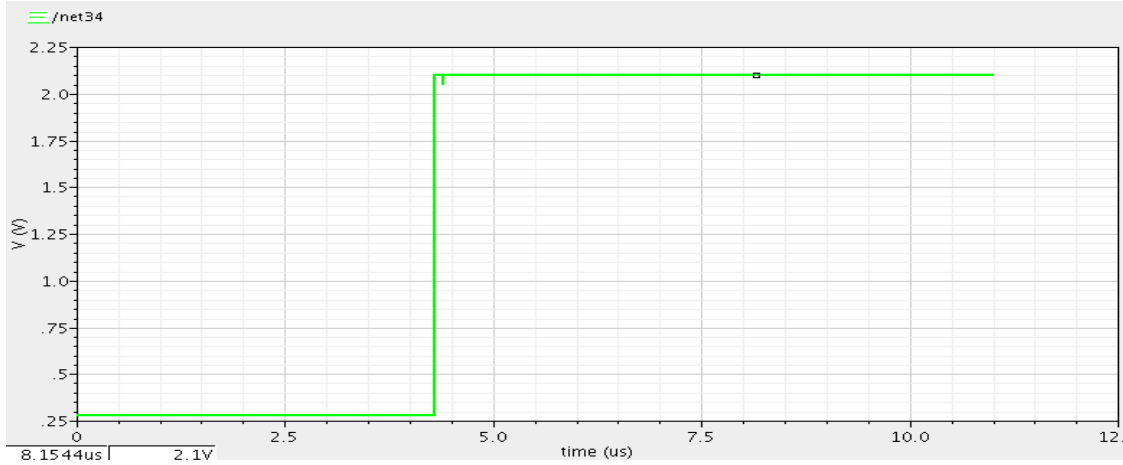


Fig 55 :- SR latch output

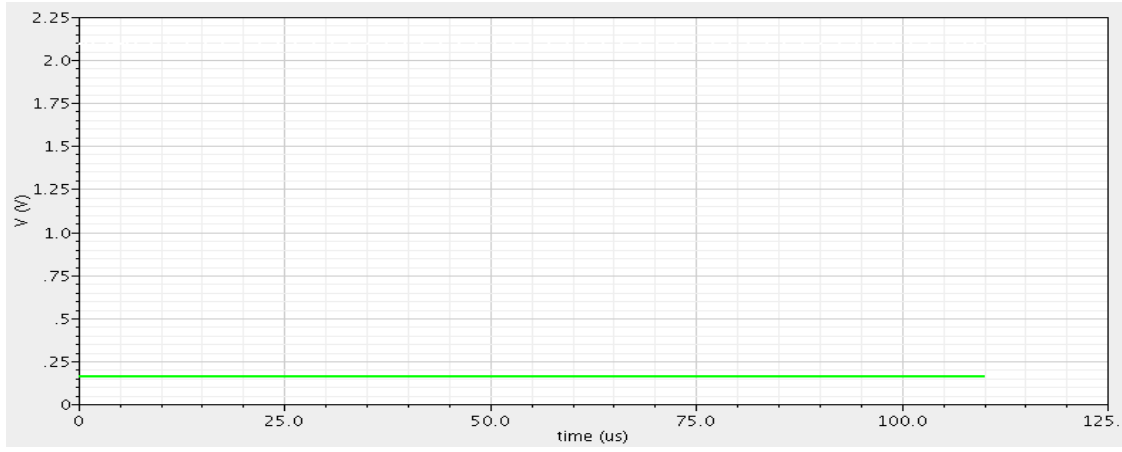


Fig 56 :- Latch output for failed authentication

In case of failed authentication, the memory won't be triggered and hence, no data will be thrown out thereby protecting the sensitive tag from unauthorised access.

5.6 Oscillator

In RFID system, the tag data has to be loaded on a carrier waveform so that it can transmitted. This carrier waveform can be a Low-frequency, High – frequency, UHF or Microwave depending the application and the need. Oscillators are used for this purpose. An Oscillator can be a LC – oscillator, Crystal oscillator or a Ring oscillator. Out of these, ring oscillators are simple to design and easy to implement in RFIC design, and hence find their role in several fields of application. For the project, I have designed a ring oscillator to generate a HF carrier signal of frequency 14.28 MHz.

Ring Oscillator

The basic circuit is shown in Fig 57 [19].

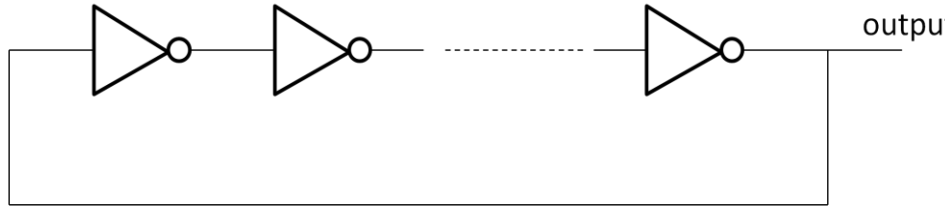


Fig 57 :- NOT-based ring oscillator

The ring oscillator is a closed loop which consists of N- identical NOT gates (odd number). The stages of NOT gates, **N** is chosen such that we get the signal with the desired frequency. This is because, every stage adds a delay due to the presence of the transistor gate capacitance (C_g) which affects the signal propagation and hence its frequency.

The structure of the basic building block of the ring oscillator is as shown,

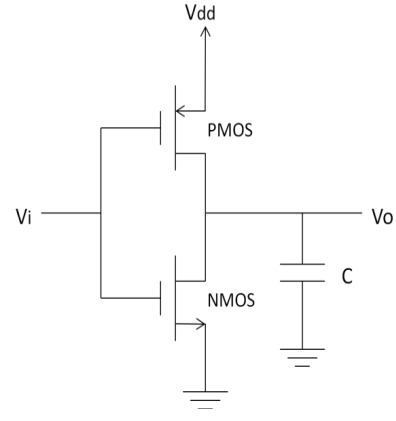


Fig 58 :- CMOS inverter

Odd number of the CMOS inverter stages with the output of a stage connecting the input of the following stage and the output of the last stage connecting the input of the first stage forms a ring oscillator.

The frequency of oscillation is given as [20],

$$f = \frac{1}{2 N \tau} \qquad \text{..... (11)}$$

where,

f = frequency of oscillation
N = number of stages
τ = delay for one stage = $R_{eq} C_p$
R_{eq} = is the equivalent resistance at the inverter toggle point

At the toggle point, the inverter drives its maximum current. Also, an additional capacitor C is also added at the output of each inverter stage and hence the frequency equation now looks,

$$f = \frac{1}{2 N (Cp+C)} \cdot \frac{I}{Vdd} \qquad \text{..... (12)}$$

where,

I = maximum current at the toggle point
V_{dd} = supply voltage

The load capacitor at each inverter output will charge and discharge as the output changes (V_o) which depends on the equivalent resistance of the tied drains of the two transistors (PMOS and NMOS).

For the project, I have simulated a 7-stage ring oscillator to generate the required carrier signal. The circuit implementation is as shown,

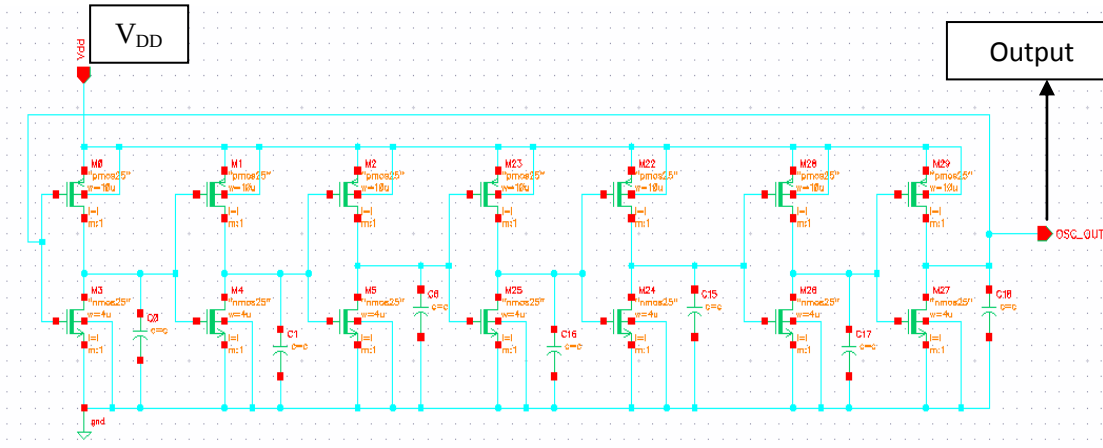


Fig 59 :- 7-stage ring oscillator

The load capacitor value used is **1 pF**.

PMOS transistor dimensions are **W = 10u, L = 1.4u** and NMOS transistor dimensions are **W = 4u, L = 1.4u**.

The output carrier signal generated is as shown,

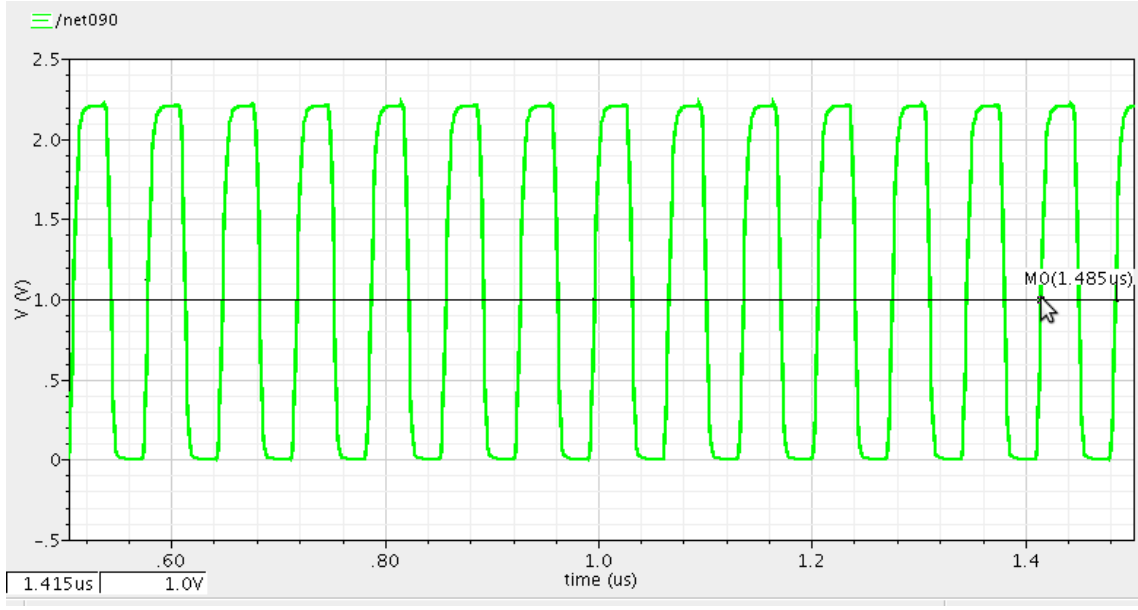


Fig 60 :- 7-stage oscillator output

The time values have been shown in the output figure to indicate the frequency of the signal generated.

The frequency of the above signal generated is **14.2857 MHz**. However, in real life scenario, small variations in the fabricated transistor sizes or the capacitor value can slightly alter the frequency. The above shown frequency is for an ideal case.

Now lets look at the frequency response of the signal when the voltage supply is varied. If we carefully look at the equation (12), we notice that N is a fixed parameter once decided by the designer. The value of C after fabrication is a constant as well. The value of C_p is so small that it has negligible effects and hence can be ignored. If the supply voltage changes, current I changes and hence the oscillator frequency.

Ideally, if V_{DD} increases, the current I increases. However, the current increase corresponding to the voltage rise is not same. Current rises comparatively more than the voltage and hence the ratio $\mathbf{I/V_{DD}}$ is non-linear. That means, when supply increases, the ratio I/V_{DD} also increases thereby increasing the frequency of operation. In applications where, the oscillator is used as a VCO to offer a wide frequency range, this frequency variations is an advantage.

However, in applications where the frequency variations can be tolerated to only a certain extent, care has to be taken that the supply voltage doesn't change. This can be done by using a Voltage regulator circuit to regulate the power supply to all the other circuit.

In this project, I am not using any voltage regulator. However, I have tried to minimise the frequency variations with respect to supply voltage variations by modifying the oscillator circuit. Now, before moving on to the new circuit, let me show the effects of voltage rise on the frequency.

Case 1:- $\underline{V_{DD} = 2.42\ V}$ (an increase of 10% from 2.2 V)

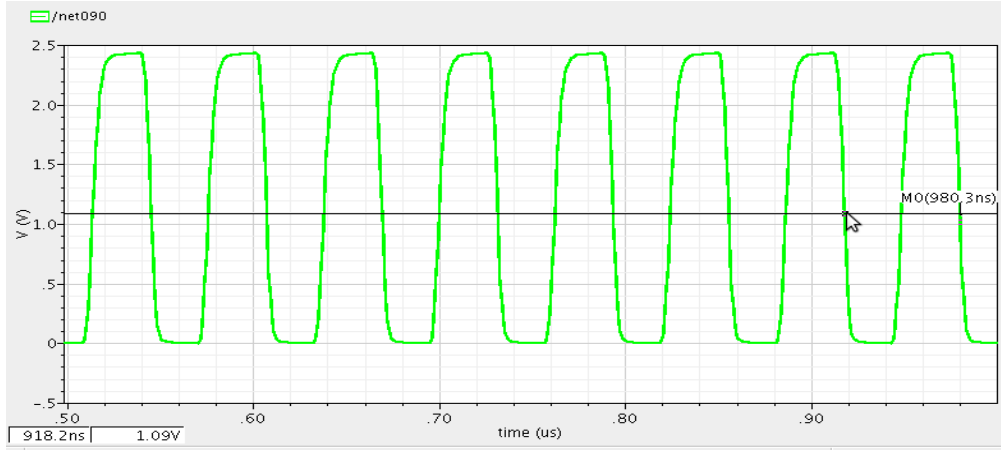


Fig 61 :- Oscillator output when V_{DD} = 2.42 V

Looking at the time period in the above output, the new frequency is **16.103 MHz**. This is a drastic change of **12.72 %** in the frequency.

Case 2:- $\underline{V_{DD} = 2.64\ V}$ (an increase of 20% from 2.2 V)

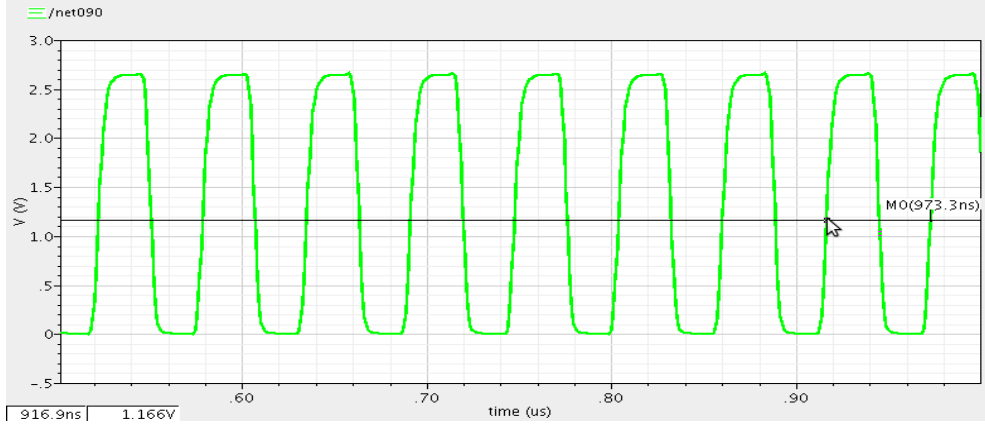


Fig 62 :- Oscillator output when V_{DD} = 2.64 V

The new frequency is **17.73 MHz**. This is a again drastic change of **24.11 %** in the frequency.

To minimise the frequency variations, the circuit shown in Fig 59 was modified such that the new oscillator is a 9-stage and the basic building block which is an inverter with a load capacitor is also modified.

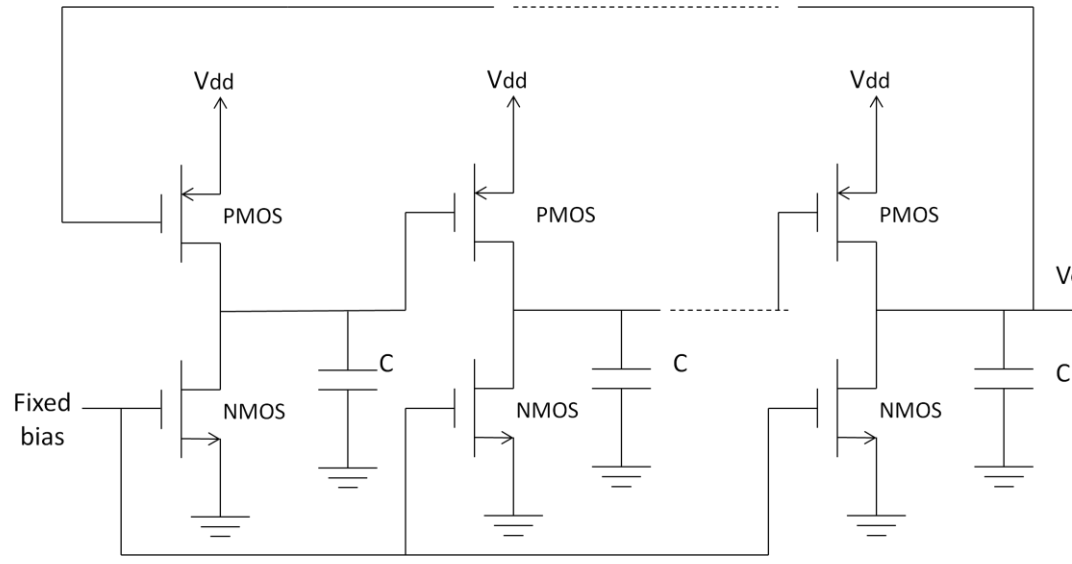


Fig 63 :- Modified Ring oscillator

Here, the output of each inverter stage is applied to the gate of the PMOS, while a fixed reference voltage (V_{ref}) is applied at the gate of the NMOS. Here as well, the capacitor C gets charged from the supply through the PMOS and discharges the voltage through the NMOS to the ground terminal. It is after the discharge of the capacitor C that the PMOS of the next stage turns ON and starts conducting.

In the earlier oscillator implementation, when the voltage supply rises, the charge on the capacitor also increases accordingly. As, the increase in the supply also affects the lower NMOS transistor, the discharge of C through NMOS now varies, giving rise to frequency variations.

In the modified circuit, the capacitor new value now is **165 fF**, which means that it has a lower charge holding capacity compared to the 1 pF capacitor used in the earlier implementation. So, when the supply increases, the drain current of PMOS also rises. However, this time the operation is more like a small signal one wherein now the charge on the capacitor rises by a very small amount. Also, as the NMOS transistor is supplied with a fixed gate voltage, the discharge of the capacitor through the NMOS becomes comparatively independent of the supply voltage. Hence in this case, the frequency variations are minimised to a great extent.

Fig. 64 shows the schematic implementation of the modified oscillator circuit.

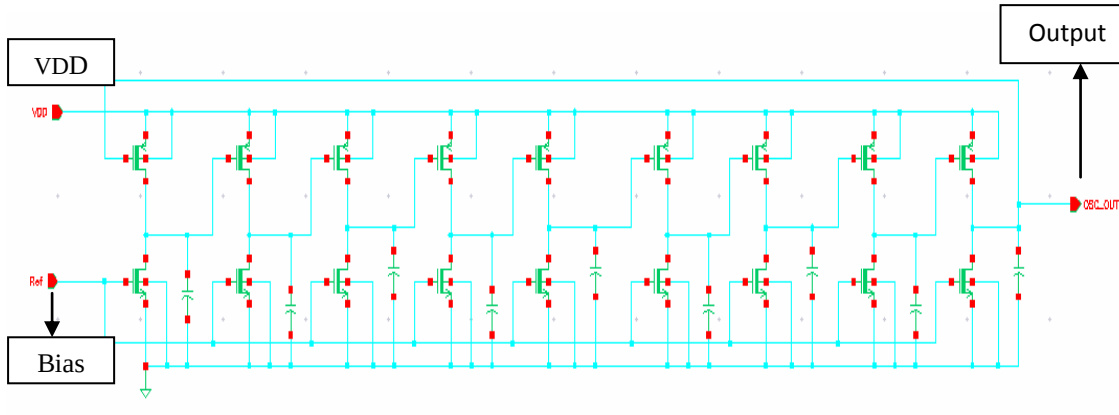


Fig 64 :- 9-stage modified ring oscillator schematic

The output signal plot is as shown,

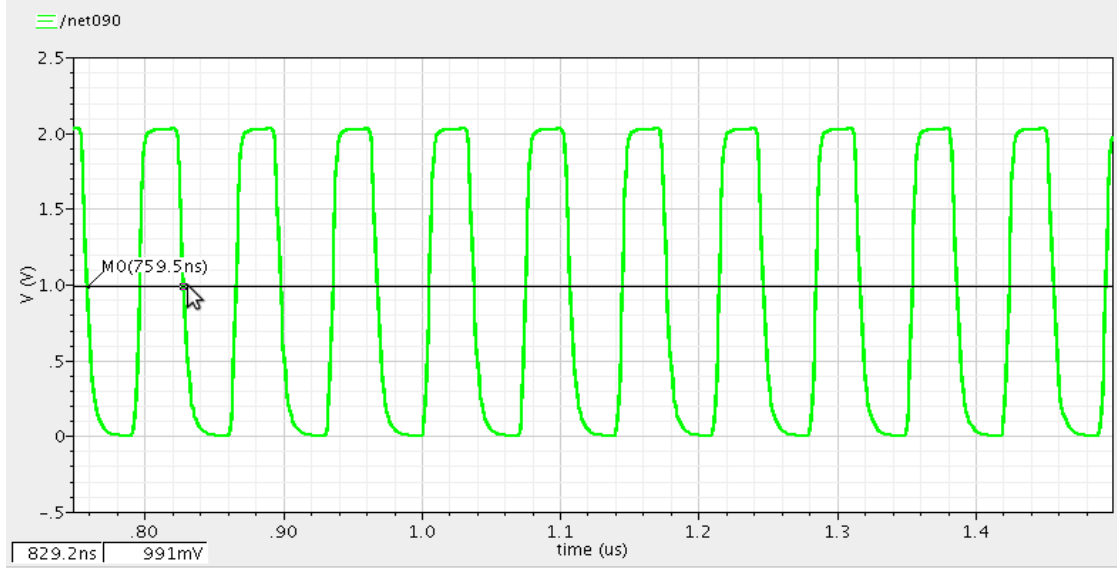


Fig 65 :- Modified oscillator output carrier signal

Here, the frequency of the carrier wave generated is **14.34 MHz**.

The frequency response for the voltage rise is much improved than before.

Case 1:- $\underline{V_{DD} = 2.42\ V}$ (an increase of 10% from 2.2 V)

The generated wave is of frequency **13.992 MHz (**refer Fig. 66). This means that the frequency variation in this case is **2.44 %** which is very less when compared to the earlier implementation.

Case 2:- $\underline{V_{DD} = 2.64\ V}$ (an increase of 20% from 2.2 V)

The generated wave is of frequency **13.572 MHz**. This means that the frequency variation in this case is **5.37 %.**

So, if we compare the results obtained from the two ring oscillator circuit implementation, we notice that the modified circuit offers better results for supply voltage variations.

The parameter values for the new circuit are as follows,

V_{bias} = 2.2 V. This bias voltage can be any voltage between the NMOS threshold voltage and the minimum value of supply voltage.

L_p = 2u, W_p = 12u, --- for PMOS
L_n = 5u, W_n = 2u, --- for NMOS

The above values have been chosen for optimised results.

The frequency variations can still be improved by increasing the number of inverter stages. However, the power dissipation also increases with that. So, its a trade off between better frequency results and power loss.

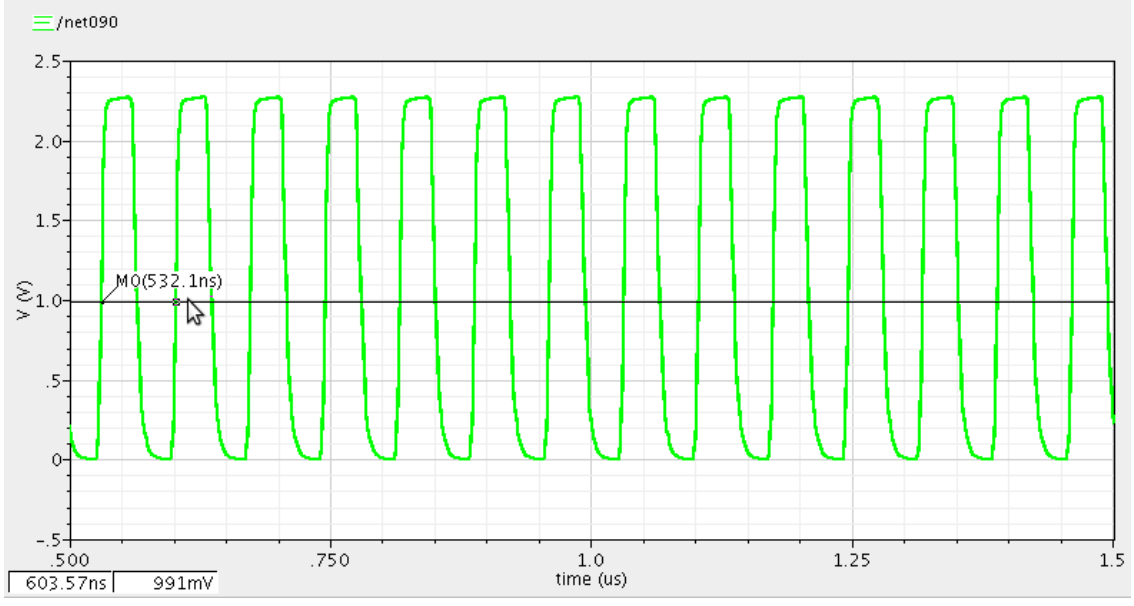


Fig 66 :- Oscillator output when V_{DD} = 2.42 V

5.7 Modulator

This is the last block in the tag system before the tag information is made available to the antenna for transmission. Modulation in simple words is a technique to alter one or more properties of a HF periodic signal with respect to a modulating signal. The HF periodic signal is often termed as a carrier signal. The properties of the carrier waveform that can be altered are either amplitude, frequency or phase. The modulation scheme used in this project for back-scattering the tag data is Amplitude Modulation.

In Amplitude modulation, the amplitude the carrier waveform, which is a 14.28 MHz periodic signal is varied with respect to the instantaneous amplitude of the modulating signal, which is the tag data in our case. The advantage of using amplitude modulation for our design is it's less design complexity compared to frequency and phase modulation. Secondly, demodulation of the final signal is less complex at the receiver end.

Reader antennas have capacity to transmit strong signals in terms of energy (power) over a fairly large distance as there are less constraints on their size and cost as compared to the antennas used in tags. Also, for high frequencies, as the communication between the reader and the tag is in near field and through electro-magnetic coupling, inductors are used. As tags are constrained by their size and cost, antenna size is limited and hence its radiation power and the energy range. Amplitude modulation on the carrier signal is done in such a way that data bits **0 and1** are represented with distinguishable voltage levels, which means that even a bit **0** in the tag data has power (voltage) associated with it when transmitted on the carrier waveform. This ensures that when the receiver receives tag data over a distance of few centimetres (roughly 5-10 cm), both the bits positions **0** and **1** will have energy associated with them (voltage levels) to facilitate their reception and further demodulation.

There are many ways to implement amplitude modulation, however, for the project, I have used a NOR circuit to implement amplitude modulation. The NOR gate implemented is a CMOS 2-input NOR gate, with oscillator signal and the tag as its input. It is a very simple circuit and the CMOS implementation reduces static power dissipation. The transistor sizes have been chosen in a manner to get the desired modulated output.

The circuit implementation is as shown in **Fig 67**, while the modulated output signal is shown in **Fig 68**.

Looking carefully at the modulated output, we can see that till the time tag data doesn't arrive, the modulator just outputs the same oscillator waveform, which is just a periodic waveform without any information. When the tag data arrives, we start getting a modulated waveform. During the scenario when the reader is not authenticated, the modulator just outputs the HF periodic waveform as no data arrives in that case.

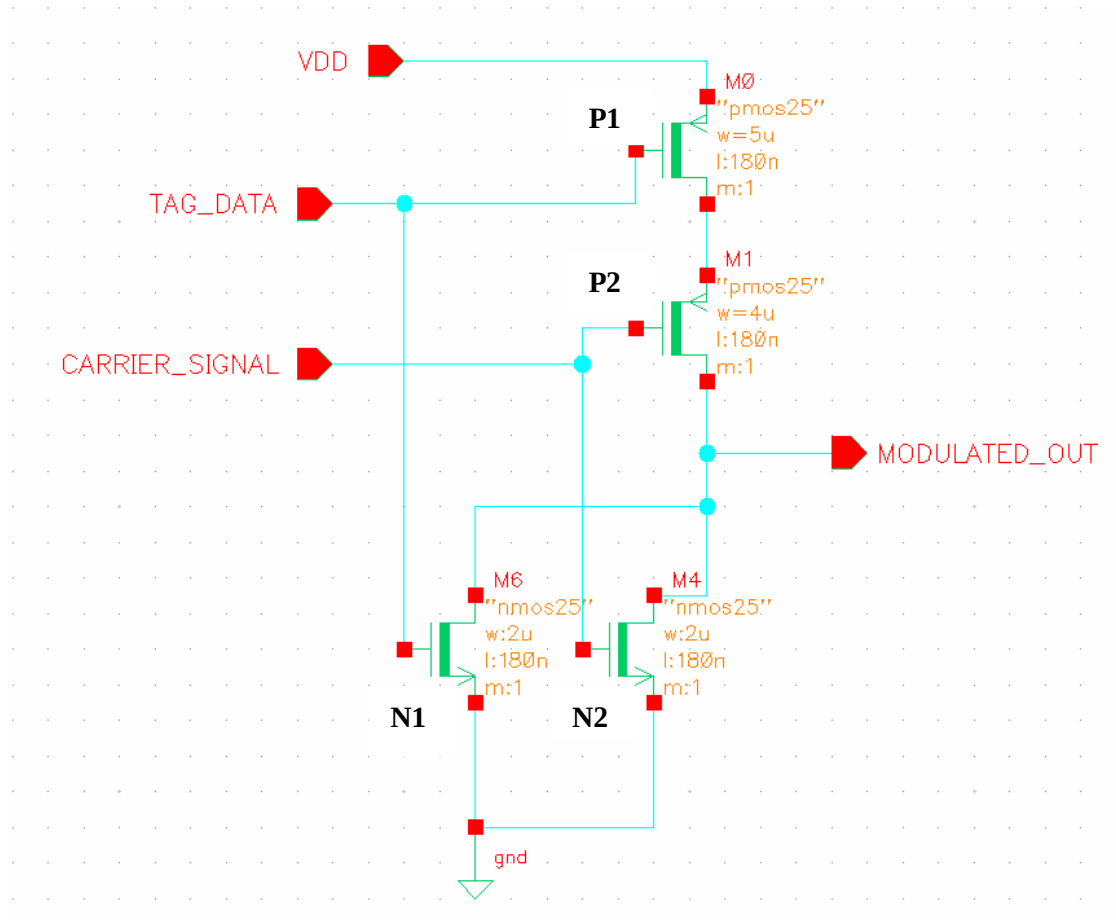


Fig 67 :- Modulator circuit (2-input CMOS NOR)

The circuit functioning is as follows,

- When TAG_DATA = 0

  For P1. $V_g = 0$. So, $V_{SG} >= |V_t|$ and the P1 turns ON. However, N1 is OFF. Hence, less current from the upper circuit is drained down through the two NMOS's thereby delivering more current at the output and resulting in output periodic signal of voltage 2 V

- When TAG_DATA = 1

  P1 is still ON. However, N1 also turns ON. Now the current flowing through P2 finds a additional path to flow through N1 to ground. These results in less current available at the output node and the output signal voltage falls to 1.5 V

Also, for PMOS,

$$I_D \alpha (V_{SG} - |V_t|)^2 .$$

So, when TAG_DATA = 0, $(V_{SG} - |V_t|)^2$ rises thereby increasing the drain current, since $V_G = 0$.

When TAG_DATA = 1, $(V_{SG} - |V_t|)^2$ decreases thereby reducing the current flow and hence the output.

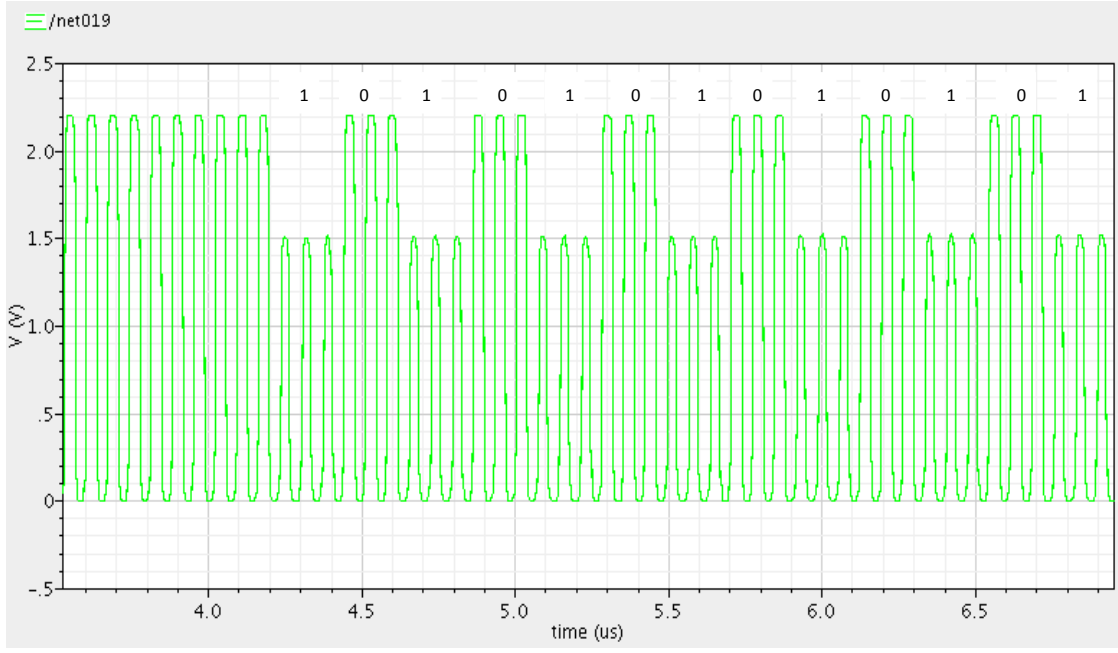


Fig 68 :- Modulator output

Here, tag data bit **0** is represented by a periodic waveform of voltage **2.2 V** and a bit **1** is represented by **1.5 V**. Refer **Fig. 56** for tag data. This output is now ready to be sent to the other tag antenna for transmission to the reader.

6. Final Design Implementation

After successfully completing individual block functions of the tag circuitry, the whole circuit was simulated to co-ordinate the working between the individual system blocks. Here, in the final design, the circuits have been replaced with their corresponding symbols generated within the tool.

The whole system view is as follows,

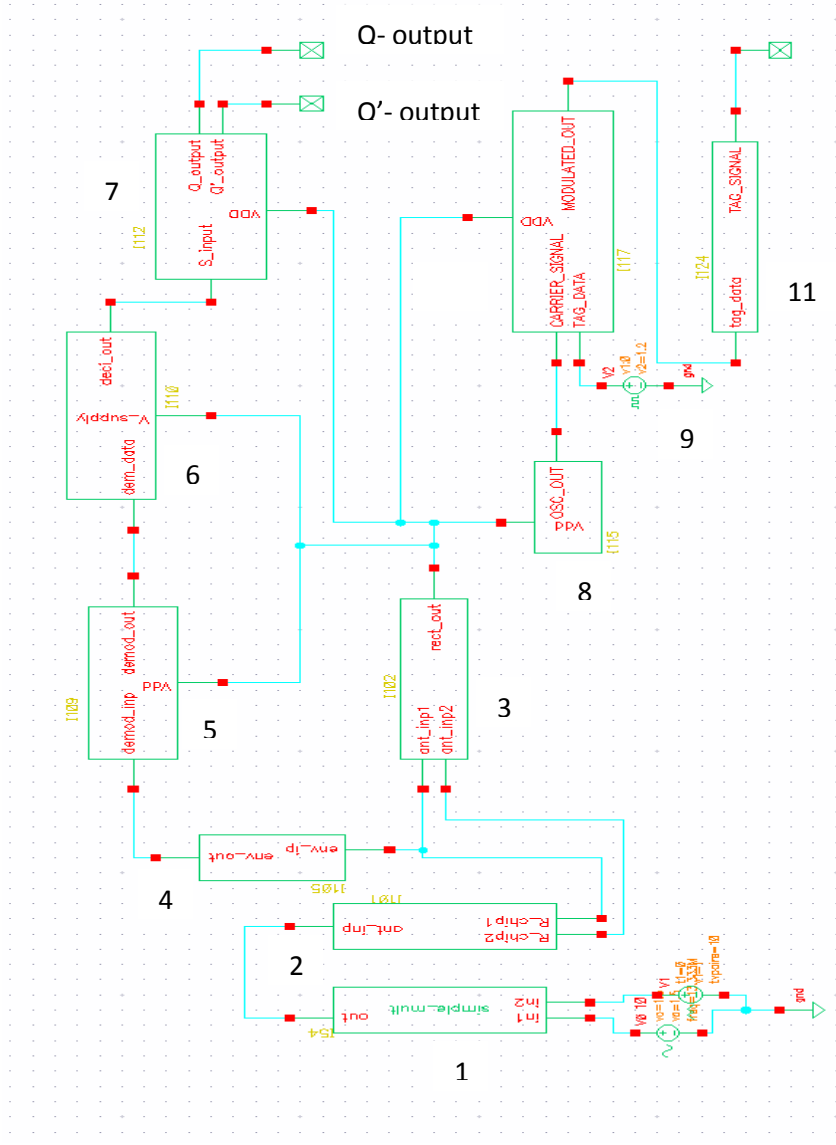


Fig 69 :- Final circuit schematic implementation

where,

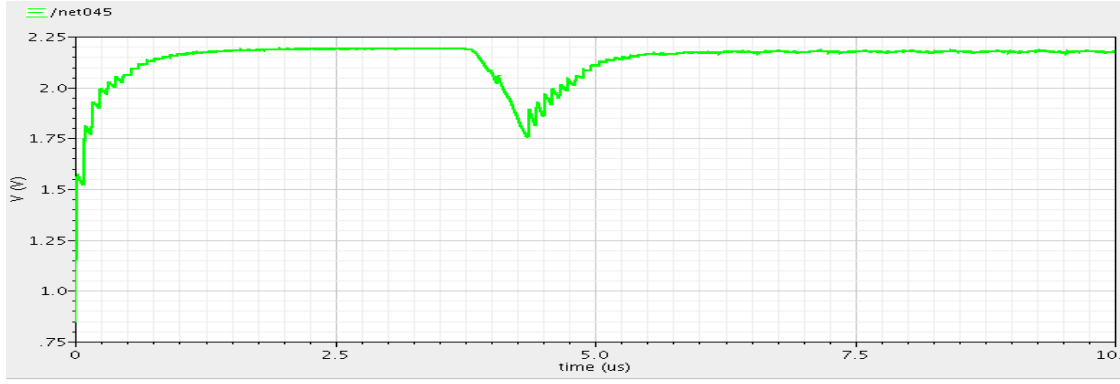
1 = multiplier block (the OOK-modulated reader signal generator)
2 = Tag antenna1 (for reception of the receiver signal)
3 = rectifier
4 = Envelope detector
5 = Demodulator
6 = Reader authentication
7 = SR latch
8 = Oscillator
9 = Tag data (which is generated by **vpulse** within the tool)
10 = Modulator
11 = Tag antenna2 (for data transmission)

In the next section, I have presented the final results of all the individual blocks when used together in the whole system.

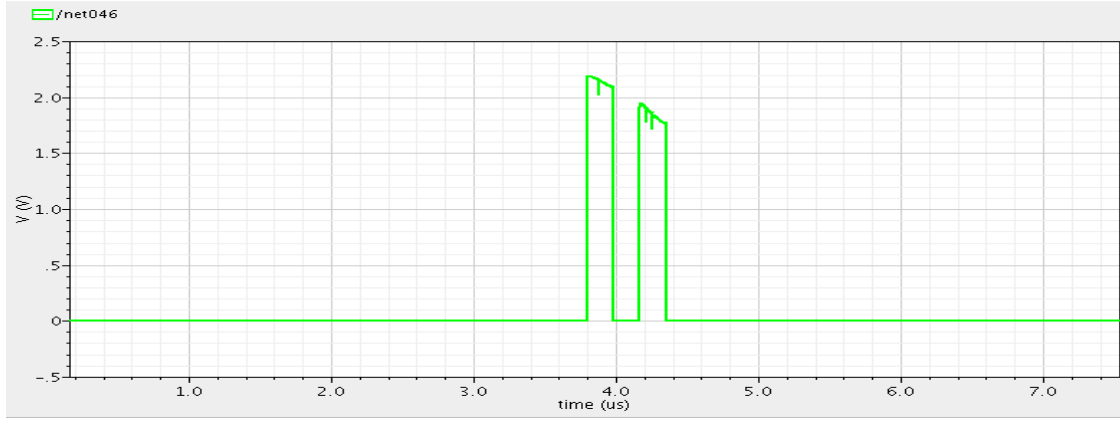
Also, the Reader authentication block output is shown for the un-authorised reader information bits (000, 001, 011, 100, 101, 110, 111).

7. Results

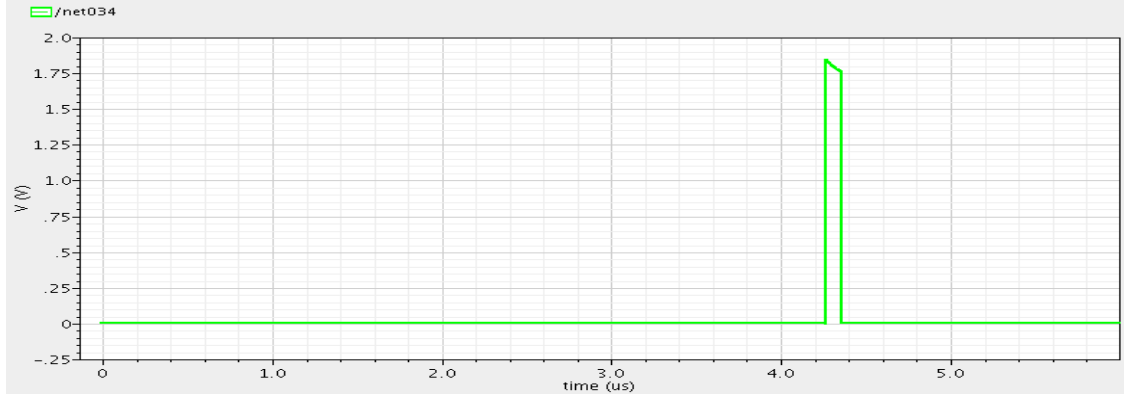
The simulation results for all the system blocks are as shown,



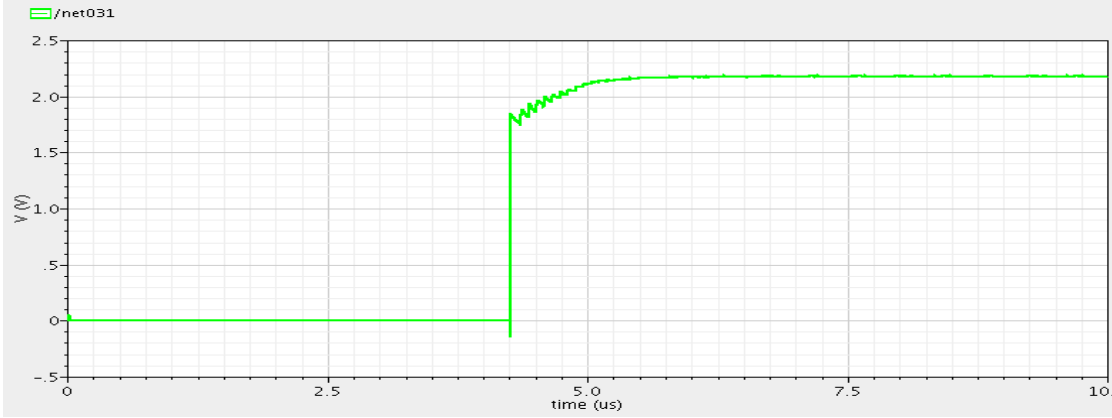
a)



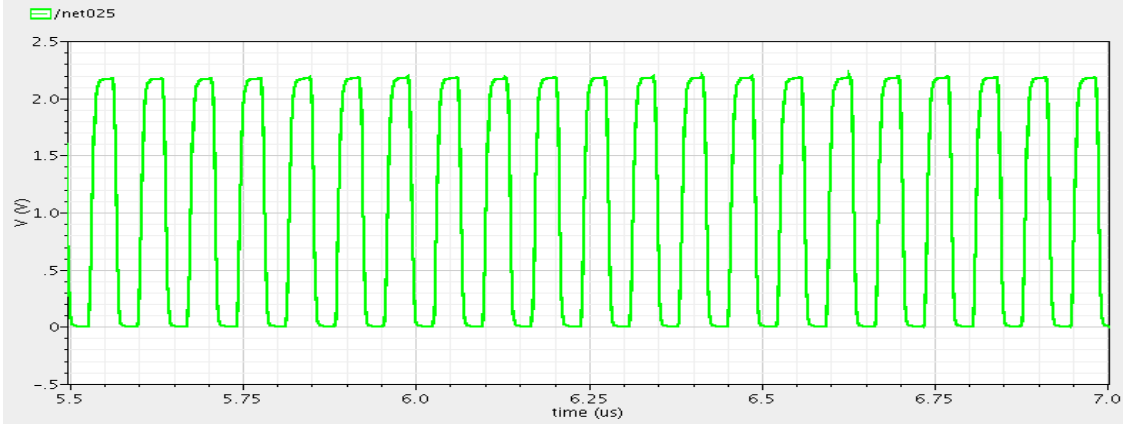
b)



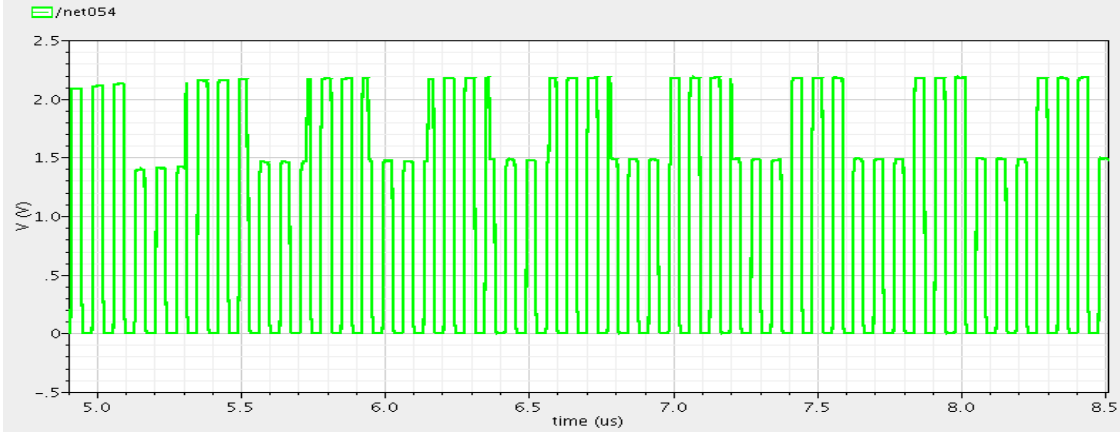
c)



d)



e)



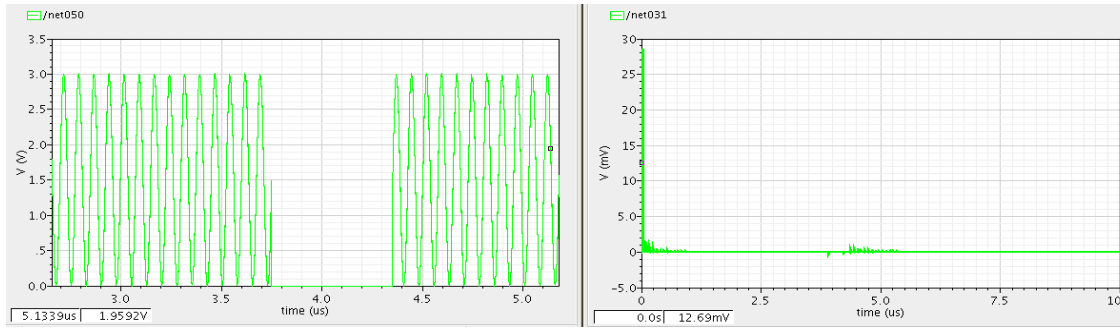
f)

Fig 70 :- a) Rectifier output, **b)** Demodulator output, **c)** Reader authentication **d)** SR Latch output, **e)** Oscillator output, **f)** Modulator output

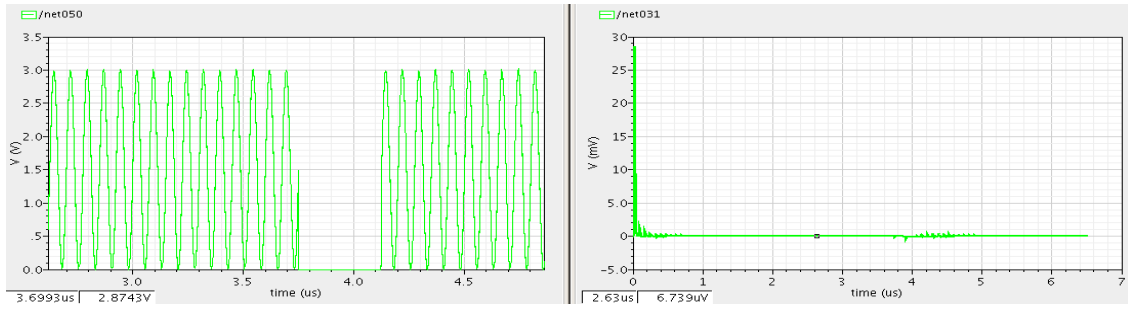
When, an un-authorised reader tries to read tag data, the system design for the tag will come to know the reader status and will accordingly generate a different latch output indicating that the authentication has failed.

Now, let's have a look at the design response for other reader information. The information bits in the reader signal between the time **3.75 µs – 4.35 µs**. Here, the left signal is the reader signal with its information embedded which is on a V (voltage) scale on Y-axis, while the latch output on the right is one a mV (milli-volt) scale.

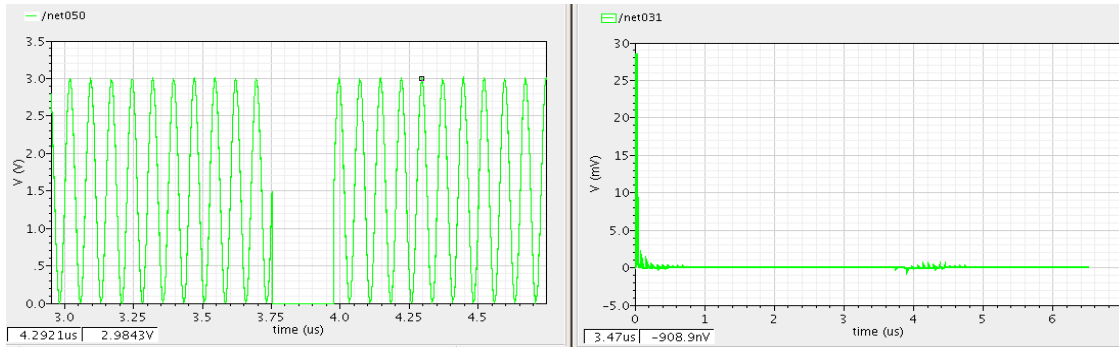
1) **reader bits = 000**



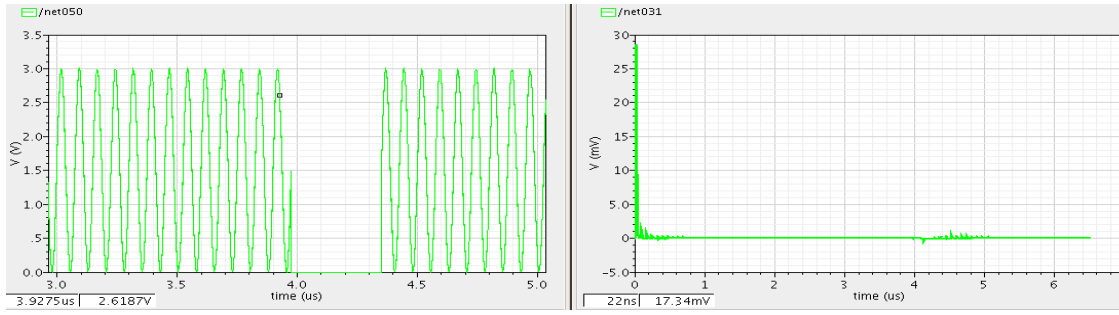
2) **reader bits = 001**



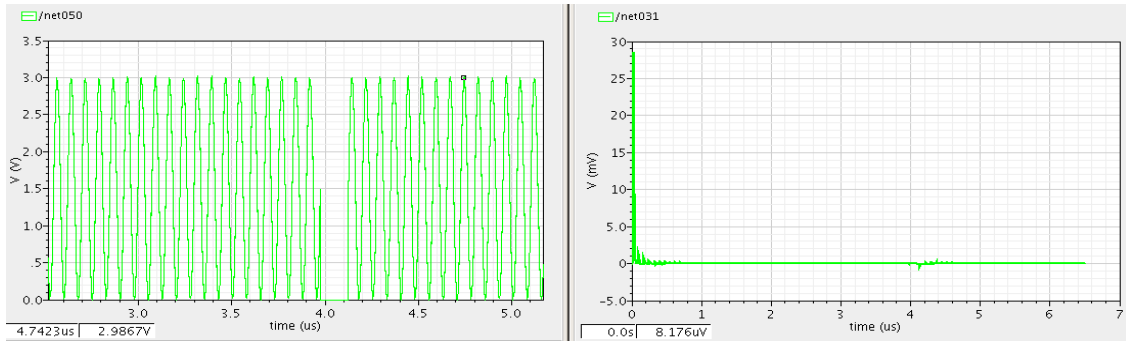
3) **reader bits = 011**



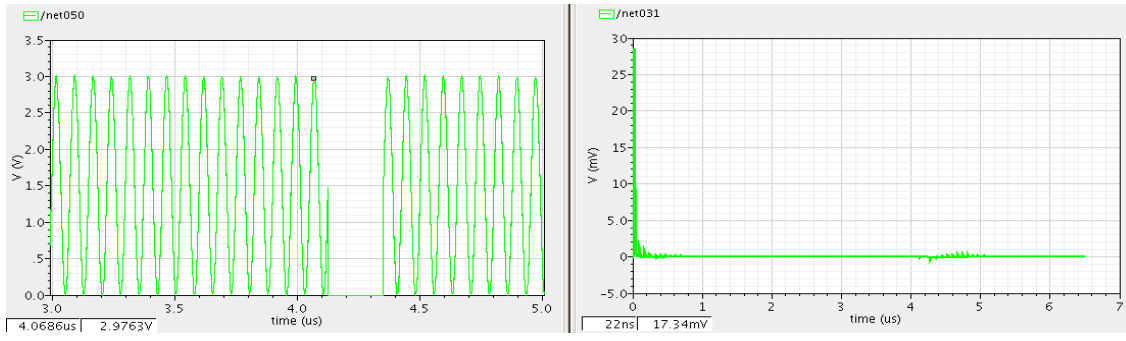
4) **reader bits = 100**



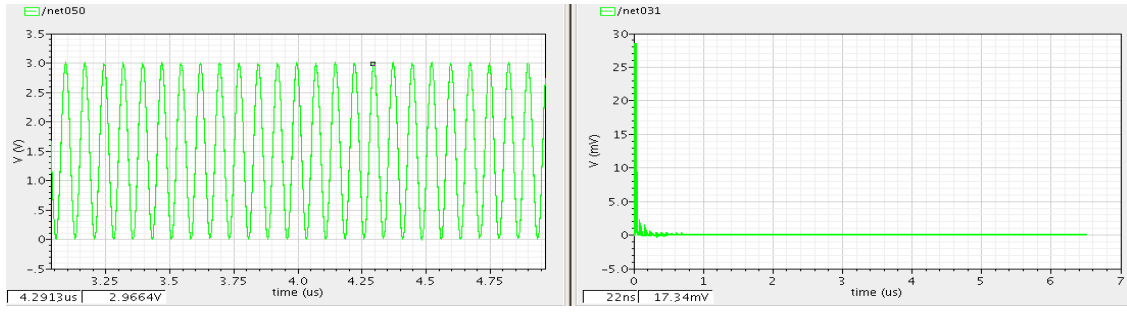
5) **reader bits = 101**



6) **reader bits = 110**



7) **reader bits = 111**



8. Conclusion and Future work

Looking at the results obtained in **Fig 70**, it can be concluded that the proposed design for the high frequency passive tag has been successfully simulated. The primary objective of the project was to first design the individual system blocks and then integrate them to carry out tag data transmission. Secondly, as power efficiency is a key factor in a passive RFID system, emphasis was given on the rectifier design. The rectifier design was first carried out for a conventional structure and results obtained were shown. To overcome the shortcomings of the conventional rectifier structure, the design was modified and better results were achieved.

For demodulator design, I first started with the design presented in [18]. When the results were studied, a major design flaw was encountered. Analysis was then done on the circuit to find out the root cause and then the design was modified and again simulated. This time, I found that the demodulator did overcome the previous problems, giving better results.

The secondary aim of the project was to add security feature in the tag such that the tag will transmit data only to its authorised readers. For this, the Decision Making logic was implemented and designed to generate a GO / NO-GO response. The basic idea of the design is to work on the demodulated reader data and figure out its authenticity. A good part of the design was that it was implemented using basic CMOS logic gates designed on an Analog platform. Experimental results show that during reader authentication, this block outputs a positive pulse, while failed authentication results in zero output. This output was then latched to a particular state. (0 – for fail and a low-high signal for pass).

The carrier signal for data transmission was generated using a 7-stage ring oscillator. However, experimental results showed that the frequency of the oscillator varies by a very large amount when the supply voltage varies. Accordingly, a different way of ring oscillator design was presented. This new oscillator is a 9-stage ring oscillator, where the output of a previous Inverter stage is applied to the gate of the next p-type transistor, while the n-type transistor in all stages was supplied by a fixed bias. The design resulted in comparatively very less frequency variations compared to the earlier one. Though, more better results can be achieved by increasing the inverter stages. However, this leads to more power dissipation and hence it’s a design trade-off.

Lastly, the design was run for other combinations of the reader input bits to see the design response. Referring to the figures shown above, it can be seen that for any other reader information other than 010, the decision making block outputs a low signal (practically zero) indicating un-authorised access.

Future work

Although, a lot of essential work has been done for the proposed design implementation and including the new features, there is much more that can be done. The suggestions for future development are,

- In the current version of the design, I have only used 3 bits for reader information. However, more bits can be included. Though this may require the re-designing of the Decision-making block, addition of the bits will lead in more flexibility and more imparted security.

- As energy is a key in passive tag system, sufficient efforts can be spent on just an optimised rectifier design. This is very important as rectifier is the energy source to the other tag components. A highly efficient rectifier would mean that more power is made available and hence additional features can be implemented within the tag and at the same time, more information can be stored and transferred in and out of the tag.

- Looking at the rectifier output in Fig 70, we can see that the supply varies when the reader information bits arrive. To overcome this supply variations or minimise them, voltage regulators can be designed and implemented in such a manner that they will carry a more or less constant supply to the other tag components.

- Also, important work can be done on tag antenna design. Different ways of optimising tag antenna should be found out. Detailed work can be carried out on the type of antenna to be used, their sizes, the material to be used for their manufacturing and bandwidth to improve the communication distance and energy transfer.

- After optimisation of all the individual blocks for a better performance, a Layout Structure for the schematic design can be implemented.

Bibliography

[1] Klaus Finkenzeller, "RFID Handbook - Fundamentals and Applications in Contactless Smart Cards and Identification", 2nd Edition. John Wiley & Sons, 2003. ISBN 0-470-84402-7

[2] RFID Journal, "The basics of RFID Technology", 2005

[3] Jianyun HU and Hao MIN, "A Low Power and High Performance Analog Front End for Passive RFID Transponder", IEEE

[4] Jim Williams, "The Art and Science of Analog Circuit Design", Butterworth-Heinemann. 1998. ISBN: 0-7506-7062-2

[5] Christian Reinhold, Peter Scholz, Werner John and Ulrich Hilleringmann, "Efficient Antenna Design of Inductive Coupled RFID-Systems with High Power Demand", JOURNAL OF COMMUNICATIONS, VOL. 2, NO. 6, NOVEMBER 2007

[6] S. Serkan Basat, Kyutae Lim, Joy Laskar and Manos M. Tentzeris, "Design and Modelling of Embedded 13.56 MHz RFID Antennas", IEEE. 2005

[7] "HF Antenna Design Notes: Technical Application Report", 3rd Edition. TEXAS INSTRUMENTS, Literature Number: 11-08-26-003, Sept 2003

[8] Patrick J. Sweeney II, "RFID for Dummies", Wiley Publishing, Inc. 2005, ISBN: 0-7645-7910-X

[9] Matt Ward and Rob van Kranenburg, "RFID: Frequency, standards, adoption and innovation", JISC Technology and Standards Watch, May 2006.

[10] Laran RFID - White paper, A Basic Introduction to RFID Technology and its use in the supply chain", January 2004.

[11] CADENCE, "Cadence Virtuoso Custom Design Platform"

[12] "The CMOS Advantage", SiBEAM, November 2005

[13] "Tag Tuning/RFID – Application Note", Atmel Corporation, Rev. 2055A–RFID–07/02

[14] Youbok Lee, "Antenna Circuit Design for RFID Applications", Microchip Technology Inc. DS00710C, 2003.

[15] Changming Ma, Chun Zhang and Zhihua Wang, "A Low-Power AC/DC Rectifier for Passive UHF RFID Transponders", IEEE International Symposium on Microwave, Antenna, Propagation, and EMC Technologies For Wireless Communications, 2007.

[16] Hu Jianyun, He Yan and Min Hao, "High Efficient Rectifier Circuit Eliminating Threshold Voltage Drop for RFID Transponders", Project supported by National High Technology Research and Development Program of China (No.2003AA1Z1280)

[17] A S. Smith and K C. Sedra, "Microelectronic Circuits", 5th Edition, Oxford University Press, 2004, ISBN: 978-0-19-533883-6

[18] Tae Young Kang, Kyung Hwan Park and Seong Su Park, "Demodulator Circuit of RFID System", United States Patent 7417496 , 08/26/2008.

[19] F. Sandoval-Ibarra and E. S. Hernández-Bernal, "Ring CMOS NOT-based Oscillators: Analysis and Design", Journal of Applied Research and Technology, ISSN : 1665-6423, Vol. 6, Num. 1. 2008

[20] R. chebli, X. Zhao and M. Sawan, "A Wide Tuning Range Voltage-Controlled Ring Oscillator dedicated to Ultrasound Transmitter", PolySTIM Neurotechnologies Laboratory.

[21] Zheng Zhu, Behnam Jamali, Peter H. Cole, "An HF/UHF RFID Analogue Front-end Design and Analysis", AUTOIDLABS-WP-HARDWARE-012, September 2005

APPENDIX:- Logic gates circuit implementation

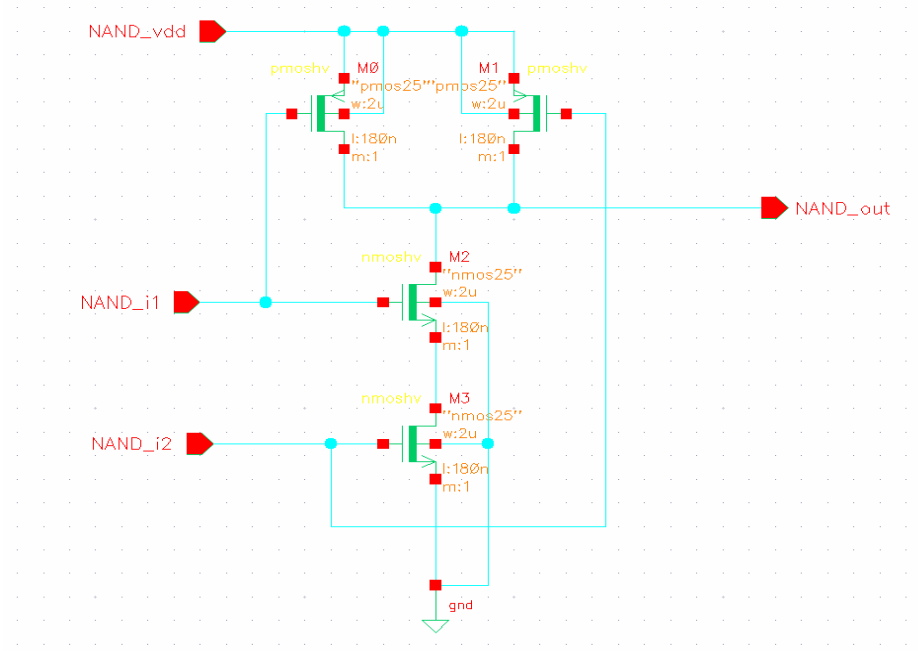


Fig 71 :- NAND gate circuit implementation

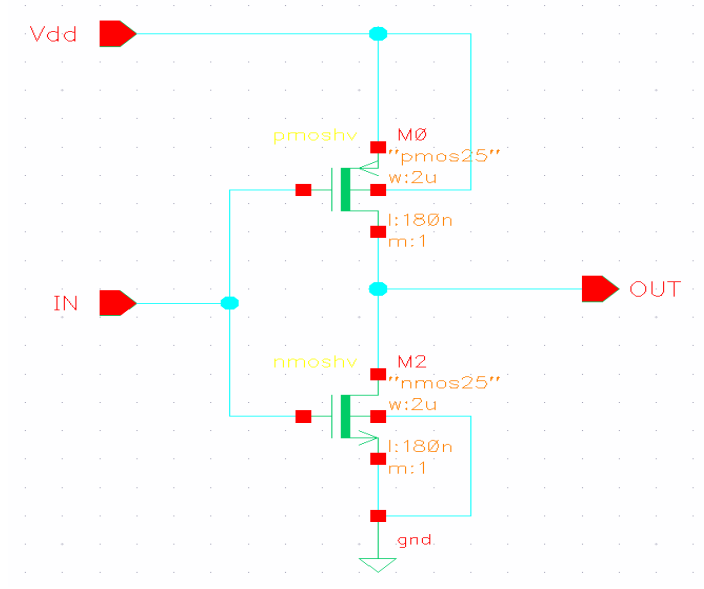


Fig 72 :- NOT gate circuit implementation