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1 EXECUTIVE SUMMARY

Over the past decades semiconductors technologies has suffered an extreme scale down, fact that continues nowadays, recently the scale down has reached the impressive number of 22 nm process node (critical dimensions of transistor). CMOS technology has been used to reach such a reduction in technology size, combined with the added benefit of low power consumption, but it is obvious that as devices are becoming smaller new problems arise in the manufacturing process; a major problem is the so called process variations.

Process variations means the random deviation of parameters such as oxide thickness, width and length in the fabrication process of any transistor, these deviations are arising from the simple fact that fabrication process is not a perfect process, changes in temperature or process steps duration causes deviations in the device performance. It is evident that a deviation in the oxide thickness of x will cause less electrical variations in a technology of 600 nm. than in a technology of 45 nm. therefore, as the scale down decreases the effect of process variations on performance increases.

Process variations can be a highly important issue to be solved at any given design that is required to be manufactured in a nano-scale, one possible solution is to consider this problem while the design process, in other words, to design a system that is process variation aware and consequently the system performance will be affected as less as possible due to process variations. Many techniques have been implemented over the past decade as process variation tolerant systems design is highly important in order to produce quality and reliable systems.

This project tries first to investigate the effects that process variations can cause on the performance of different VCO designs, through the project different VCO topologies are explained, design and simulated, different technologies are used in order to compare the problems that process variations can cause on them.

The second part of this project is related to the design of a system that can be aware of any process variations that could happen and adapt the VCO in order to reduce as much as possible the VCO dependency to process variations.

This project has achieved:

- The correct design of 4 different VCO topologies, all these design achieve the appropriate performance characteristics in order for all of the designs to be implemented on USB 3.0
- The correct simulation of these 4 designs under corner cases, temperature variations, power supply variations and a considerably huge amount of random process variations.
- The deep investigation of how process variations affect the VCO performance.
- Two solutions that are able to mitigate the VCO performance degradation due to process variations are presented in this project.

2 AIMS, OBJECTIVES AND THESIS ORGANIZATION.

For the appropriate completion of this project two main aims need to be achieved:

1. The correct design of a VCO that can be implemented on a USB 3.0, but it must be mentioned that the time is not sufficient to achieve all the specific characteristics for a USB 3.0 implementation and achieve aim two as well, but the VCO must achieve a frequency of 5 GHz and possess low noise

2. The investigation of this VCO under process variations and a possible solution that would make the VCO aware of process variations and therefore its performance would be unaffected as much as possible due to process variations that might occur.

In order to achieve these aims 4 objectives must be achieved

2.1 OBJECTIVE 1: RESEARCH ON VCOs AND PROCESS VARIATIONS

Research must be done in these two areas before starting to design or simulate any system. There are different ways to implement a VCO, consequently as many as possible must be studied. Not too much knowledge is known about process variations therefore a deep understanding of this area must be achieved as is a key element in this project.

2.2 OBJECTIVE 2: VCO DESIGN

Many VCO topologies must be investigated in this project, the software design and simulation is highly important in this project, all the VCOs must be design properly so they can be implemented in a USB 3.0.

2.3 OBJECTIVE 3: PROCESS VARIATIONS EFFECTS ON DIFFERENT VCO

It is required to understand the effects that process variations can cause on different VCOs, for this objective every VCO that was design in objective 2 must be stressed under random process variations and the degradation on their performance must be observed.

2.4 OBJECTIVE 4: DESIGN A VCO THAT IS AWARE OF PROCESS VARIATIONS

A VCO that can detect what process variations are happening and in what level needs to be design, after detecting the process variations the VCO must be able to adapt itself so the performance degradation due to process variations can be reduced as much as possible.

2.5 THESIS ORGANIZATION:

Chapter 3 is dedicated to basic knowledge on VCO parameters and characteristics, in this chapter the different VCO topologies are explained with their respective parameters and characteristics. This chapter also includes a summary of process variations including their main sources.

Chapter 4 discusses different VCO design methodologies that need to be known before attempting to design a physical VCO, it includes necessary information in order to understand the simulations that are being performed in this project.

Chapter 5 presents the two main design concepts that are used for the design of VCOs.

Chapter 6 shows all the VCOs that were design in this project, their respective simulation and results are included as well, this chapter includes as well the design's results of the VCOs under process variations, this chapter is very important to understand the effects that process variations can cause on different VCO.

Chapter 7 combined with chapter 6 are the most important chapters in this project, chapter 7 presents 2 different solutions to the process variation problem, two different solutions that can be attached to different VCOs and produce a small but important improvement in the process variation area.

Chapter 8 and 9 present a conclusion and possible future work

3 BACKGROUND

3.1 VCO

A VCO is an electronic oscillator whose oscillatory frequency is controlled by an input DC voltage V_{tune}, VCOs are used in application such as PLL, frequency synthesizers or function generators, in figure 3.1 it can be observe this concept, the output V_{out} is a non-perfect periodic sinusoidal signal, V_{out} can be expressed in equation 3.1, where p is a fixed phase and V_o is the amplitude, W_c is the angular carrier frequency that can be expressed in equation 3.2, where f_c is the center frequency, all this parameters (V_o, p and f_c) are dependent on many design parameters that can involve active and passive devices, by configuring these parameters the VCO performance can be configure as well.

$$V_{out}(t) = V_o \sin(W_c\, t + p) \quad (3.1) \qquad W_c(V_{tune}) = 2\pi f_c(V_{tune}) \quad (3.2)$$

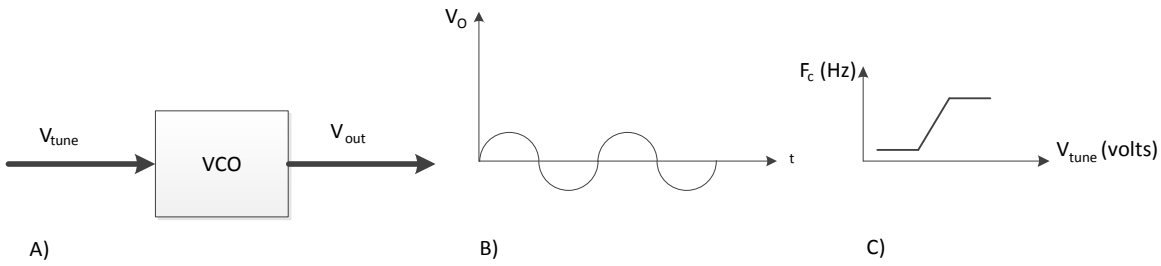


Figure 3--0-1: Illustration of VCO concept

Table 3-0-1: VCO parameters performance

parameter	Unit
Center frequency	MHz or GHz
Tuning range	GHz or MHz
jitter	Seconds @ frequency
Phase noise	dBc/Hz @offset [KHz]
VCO-Gain	MHz/V
area	μm^2
Supply voltage	V
Power consumption	mW

There are many parameters that are consider at the time of designing a VCO, these can be summarize in table 3.1, the main parameters are center frequency, tuning range, phase noise, power consumption and area.

3.2 VCO TYPES

VCOs can be categorized in 2 major groups, these two categories can be distinguished simple by the way that oscillation is achieved, one is called LC oscillators and the other is ring oscillators.

3.2.1 LC oscillators

LC oscillators achieve a signal oscillation through a resonant tank composed by passive devices (inductor and capacitor) building a parallel resonant tank; this is symbolized in figure 3.2. The carrier frequency can be calculated by equation 3.3, where L is the inductance and C is the capacitance.

$$W_c = \frac{1}{\sqrt{LC}} \tag{3.3}$$

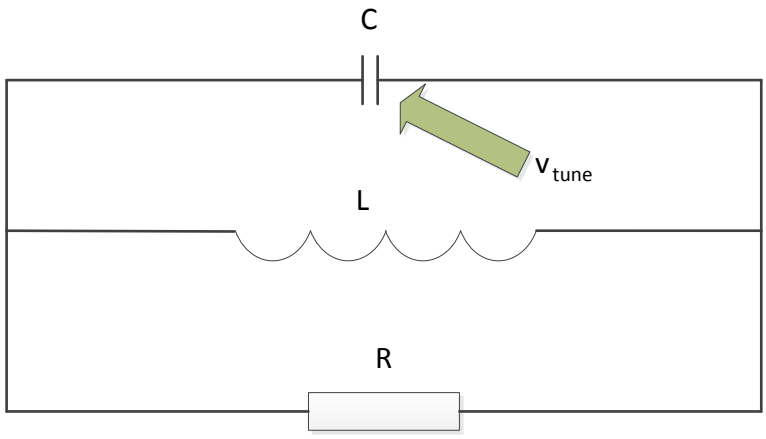


Figure 3-0-2: LC tank schematic

The capacitance C is proportional to the input voltage V_{tune} and as expressed in equation 3.3 the carrier frequency W_c is dependent on the capacitance, this way a voltage control oscillator can be achieved, it must be mentioned that not only the variable capacitance C tunes the oscillation frequency but also the parasitic and inductor capacitances. LC oscillators can achieve high center frequencies, low phase noise and low power consumption, on the other hand, their tuning range is quite limited, and in order to implement them a high area is required.

Before process variations are discussed in this type of VCO, it must be clear that capacitance C and inductance L are not implemented with passive components due to their high area and parasitic problems and it needs to be explained how they are implemented in order for a proper understanding on how process variations affect them.

3.2.1.1 CAPACITANCE INMPLEMENTATION THROUGH VARACTORS

MOS inversion mode varactors are voltage-controlled capacitors which are widely used to create on chip capacitances [3] and have been used for a long time [4]. Varactors are implemented by shorting the source and drain regions and applying a tuning voltage V_{tune} to them (figure 3.3b), this tuning voltage varies the depletion region, which at the same time varies the depletion region capacitance C_d which is in series with the gate oxide capacitance C_{ox}, observe figure 3.3.a for a graphical representation of this. The varactor capacitance C_v can be calculated with equation 3.4, it is clear the importance of the parameter C_{ox}.

$$\frac{1}{C_v} = \frac{1}{C_{ox}} + \frac{1}{C_d} \tag{3.4}$$

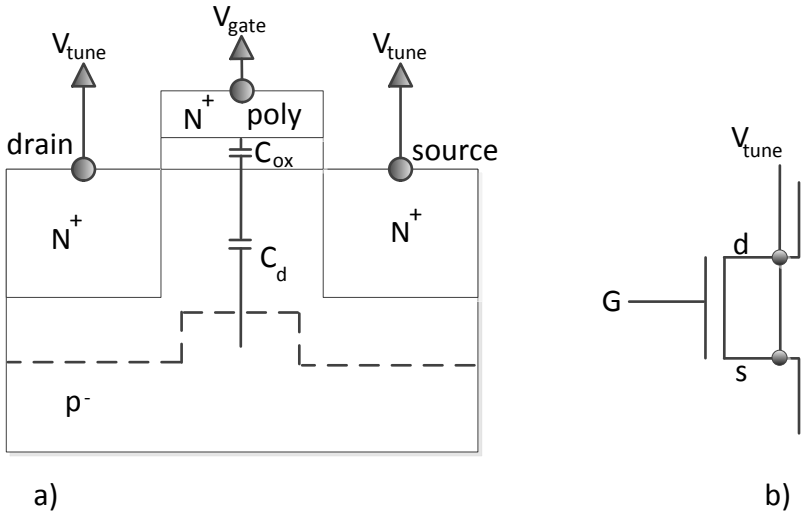


Figure 3-0-3: Varactor representation

3.2.1.2 PLANAR INDUCTORS

External inductors are discarded due to their high area, cost and parasitic capacitance, best way to produce integrated inductors is by planar inductors. Planar inductors are built by the circuit metalization process, in modern IC technologies 4 to 9 metal layers (cooper or aluminium) are available to the designer for circuit wiring, besides circuit wiring, these metal layers can be used for inductor design, these are referred as monolithic planar inductors, in figure 3.4a it can be observe a graphical representation of this concept. The inductance is characterized by the magnetic field induced by the alternating current flowing through the conducting metal layers, the magnetic flux density B is the responsible for this magnetic field.

In spiral inductors, the distinction between fabrication process parameters and design parameters must be made.

- Process parameters:
    1. Oxide thickness
    2. Substrate resistivity
    3. Number of metal layers
    4. Thickness t and composition of metal layers.
- Design parameters:
    1. Number of turns, n
    2. Metal width, w
    3. Edge to edge spacing between adjacent metal, s
    4. Outer or inner diameter, d_{out} and d_{in}
    5. Number of sides, N

Spiral inductors can be implemented in different geometries, on figure 3.4b it can be seen the most used one, square or "Manhattan", due to its layout simplicity and low cost, there are more efficient geometries such as hexagonal or octagonal, or circular which is the most effective one.

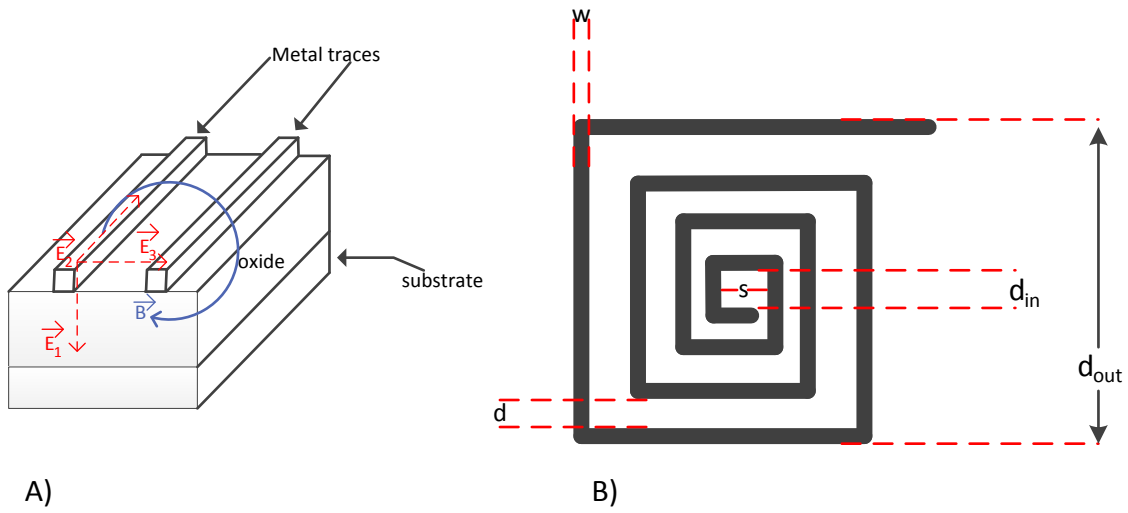


Figure 3-0-4

From equation 3.5 it can be calculated the inductance of a square spiral inductance [7] with an error margin of 8%, from this equation it is clear that the inductance is highly dependent on process parameter t (metal thickness), which can suffer a variation of ± 30 % on the fabrication process due to chemical – mechanical polishing [7].

$$L = \frac{\mu_o}{2\pi} l \left(ln\left(\frac{l}{n(w+t)} - 0.2\right)\right) \quad (3.5)$$

$$l = (4n+1)d_{in} + (4N+1)N(w+s) \quad (3.6)$$

3.2.2 RING OSCILLATORS

Another way to implement an oscillation signal is by cascading individual N delay cells creating a delay path with a negative feedback of 180°, this can be seen in figure 3.5, the frequency f_o is calculated by the total time of the delay path, with equation 3.7 this can be done were t_d is the delay of each individual cell, and N is the number of delay cells.

$$f_o = \frac{1}{2 \times N \times t_d} \qquad (3.7)$$

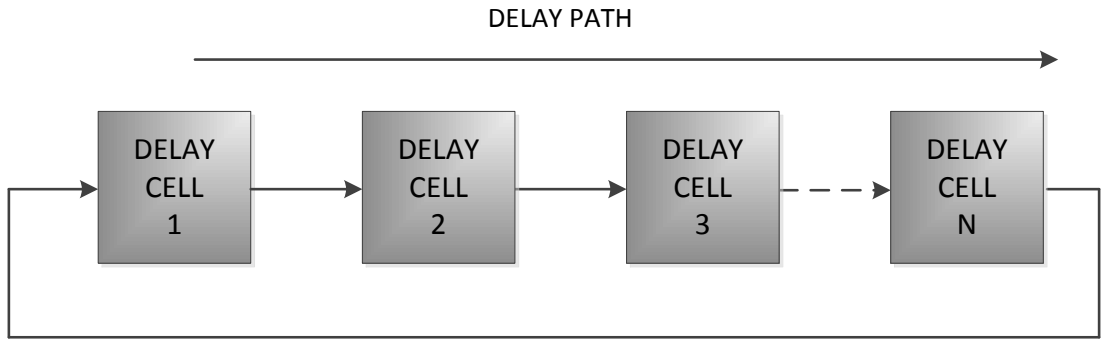


Figure 3--0-5: Ring oscillator schematic

As every VCO, the frequency needs to be tuned, in ring oscillators the delay of each individual cell can be tuned by an input voltage, delay cells can be implemented on different ways offering different characteristics in terms of tuning range, power consumption or area, but comparing them with LC oscillators in most cases they suffer from higher phase noise and power consumption, but on the other hand they have wider tuning range and can be implemented in smaller areas as only transistors are required for their implementation, apart from the fact of avoiding many parasitic effects that appear in LC tanks.

3.3 PROCESS VARIATION

A highly complex fabrication process is required In order to be able to reach such impressive scales in semiconductors, this combined with the atomistic and quatum-mechanical limitations, the probability of any variations has increased considerable, this fact simply introduces the concept that nowadays is not only required to model a nano-scale system for worst case process corners scenarios, but to be tolerant to different process variation that may occur during fabrication, process variations can be categorized in two categories.

1. Inter-die variations: these come from lot-to-lot, wafer-to-wafer and within the wafer, these variations affects every device in the system by equal, such problems can be random residuals or wafer die interactions, these problems are described in detail in [5]
2. Intra die variations: these affect the device dopant density, geometry, circuit timing or gate oxide thickness, these vary from device to device within the same die, and these are the major contributor to mislead behaviour of the system due to process variations.

Both variations are well described in [5], an important detail is that these variations may occur on a random position, this creates the impossibility of reducing them by control fabrication methods, main sources for these variations are:

1. RDF (Random Dopant Fluctuations): The decrease of the number of dopant atoms in the channel due to scaling down has reached the impressive figure of less than 100 atoms in a 32 nm technology, figure 3.6a shows how the number of dopants atoms has decreased considerably with technology scaling , MOS threshold voltage variations due to variations in the number and location of dopants is considered to be the principal issue in threshold voltage variations, in [7] it has been found that 65% of voltage threshold variations are due to RDF in 65nm technology.

2. Line edge and Line width roughness (LER and LWR): these are just a simple deviation of an ideal straight line structure which is created in the lithography step, this concept is illustrated in figure 3.6b, in [8] it has been proved that this problem only starts when the gate length is 80 nm or below, this problem affects directly V_T.

3. Gate dielectric variations: these are variations on the metal gate used for MOS devices, variations in gate oxide thickness, fixed charge or interface traps, physical variations of these parameters causes the variations in threshold voltage, gate tunnelling current or electron mobility degradation.

Nowadays it can be seen a variation of 30% in VCO operating frequencies and 5 to 10 times variation in leakage power due to process variations [9]. It can be summarize that the most important parameters that are affected by process variations are threshold voltage and gate oxide thickness, this and the fact that the VCO performance is highly dependent of these two parameters makes the necessity of this project to focus on the variation of these two parameters.

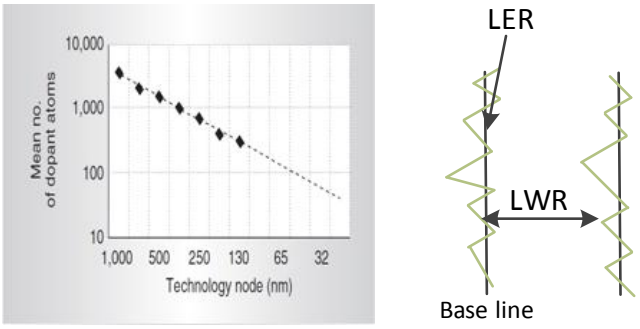


Figure 3-0-6: a) the decrement of the number of dopants [5], b)LER and LWR illustration

3.3.1 PROCESS VARIATION ON LC OSCILLATORS

Process variations in this case can be separated 2 categories:

1. capacitance: the varactor capacitance C_v (equation 3.4) is highly dependent on the gate oxide capacitance C_{ox}, which is dependent on the oxide thickness as equation 3.8 shows

   $$C_{OX} = \frac{\epsilon_{ox}}{t_{ox}} \quad (3.8)$$

   Oxide thickness t_{ox} is dependent on the gate length which can suffer a variation of $\pm 35\%$, [6], looking back at equation 3.3 it can be seen the importance of this variation.

2. Planar inductor: The inductance produce by a planar inductor can vary up to $\pm 25\%$ [7] due to process variations, another problem is that as this device suffers from process variations the parasitic also vary, as it will be seen later, In terms of minimizing the process variations effects, the LC tank is not a good approach mainly to the inductance.

3.3.2 PROCESS VARIATIONS ON RING OSCILLATORS

As ring oscillators are created only with MOS transistors two main parameters are the major contributors to VCO performance degradation, this is easily seen from equation 3.9, this is the drain current of any MOS device, clear is the dependency to the parameters t_{ox} and V_T, which as described before suffer a huge variation due to process variations.

$$I_D = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_T)^2 \quad (3.9)$$

$$K' = \frac{\mu_n \epsilon_{ox}}{t_{ox}} \quad (3.10)$$

4 DESIGN METHODOLOGY

4.1 VCO DESIGN THEORY

4.1.1 BARKHAUSEN OSCILLATOR THEORY

Barkhausen model [11], treats a VCO as a feedback system, refer to figure 4.1, where there is an amplifier A and a feedback network F, the amplifier A is characterize by the transfer function $A(V, jw)$ were V represents the input amplitude and jw the angular frequency, on the same way the feedback network transfer function is $F(V, jw)$.

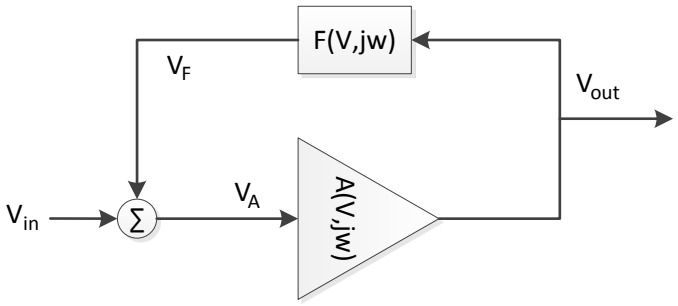


Figure 4-0-1: Barkhausen feedback model

If both parts, amplifier and feedback network, are linear systems, both expressions can be simplified to $A(jw)$ and $F(jw)$, then we find

$$V_{out} = A(jw)V_A \tag{4.1}$$

and

$$V_F = F(jw) \times V_{out} \tag{4.2}$$

where

$$V_A = V_{in} + V_F \tag{4.3}$$

the complete transfer function of the system is

$$\frac{V_{out}}{V_{in}} = \frac{A(jw)}{1 - F(jw)A(jw)} \tag{4.4}$$

This system is unstable if

$$|A(jw)||(F(jw)| \geq 1 \tag{4.5}$$

Barkhausen criteria states that long as the system is unstable the oscillation amplitude will grow[11], this specifies that if the gain Is greater 1 the output amplitude of the system will grow indefinitely, in reality this amplitude will reach a saturation at some point and it will become stable.

The conclusion of this analysis is that two conditions need to be met for the system to oscillate.

1. The open loop amplitude gain of the system should be equal or greater than 1.
2. The feedback network needs to create a phase change of 180°.

4.1.2 N STAGE RING OSCILLATOR

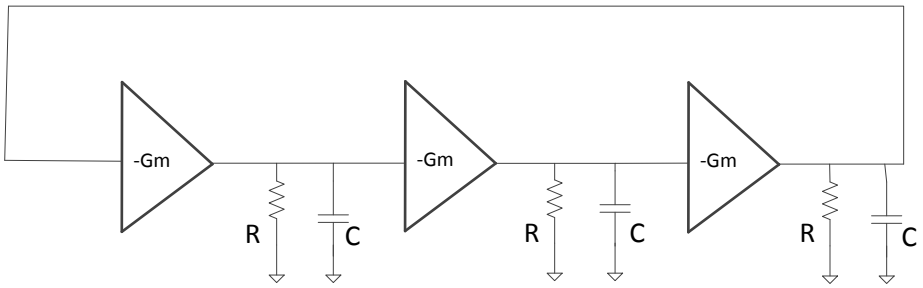


Figure 4-0-2: 3 stage ring oscillator

Looking at figure 4.2 it can be seen a 3 stage ring oscillator where the total delay line is the sum of each delay stage where each stage delay can be found by

$$T_{stage} = -Gm \times (R//C)$$

Where the – represent a phase shift of 180° of the input,

$$T_{stage} = -Gm \times \frac{R \times \frac{1}{jwC}}{R + \frac{1}{jwC}} = -\frac{Gm \times R}{1 + jwRC}$$

As an open loop transfer function

$$T_{total} = T_{stage1} \times T_{stage2} \times T_{stage3}$$

$$T_{total} = -\left(\frac{Gm \times R}{1 + jwRC}\right)^3$$

From this we can see that an N stage ring oscillator will have a delay of

$$T_{total} = -\left(\frac{Gm \times R}{1 + jwRC}\right)^N$$

The condition above is satisfied if the number of stages is odd, in case of even number of stages the total delay would be

$$T_{total} = \left(\frac{Gm \times R}{1 + jwRC}\right)^N$$

As stated before the phase change of the entire loop needs to be 180°, this states the next two facts:

1. If single ended stages are used then it is required for the number of stages to be odd.
2. If double ended stages are used then the number of stages can be either odd or even.

4.1.4 NON IDEAL OSCILLATORS

The theories presented before are only for ideal oscillators, in reality physical design has to account for distortions on the output, because of these distortions different effects need to be analyse and minimize through the design process.

4.1.4.1 PHASE NOISE AND JITTER

A perfect oscillator will have a perfect sinusoidal output that can be described as

$$V_{out} = V_0 cos[2\pi f_c t + \phi]$$

where V_0 is the amplitude, f_c is the center frequency and ϕ is a fixed phase, but in reality the output signal is

$$V_{out} = V_0(t) y[2\pi f_c t + \phi(t)]$$

where y is a periodic function and there are fluctuations in the parameters $V_0(t)$ and $\phi(t)$, in terms of frequency domain this will create a symmetrical distribution of f_c [12] this is called phase noise, observe figure 4.3a for frequency domain representation and 4.3b for time domain, the Jitter is the phase noise in terms of time domain. The lower the jitter the better the performance of a VCO.

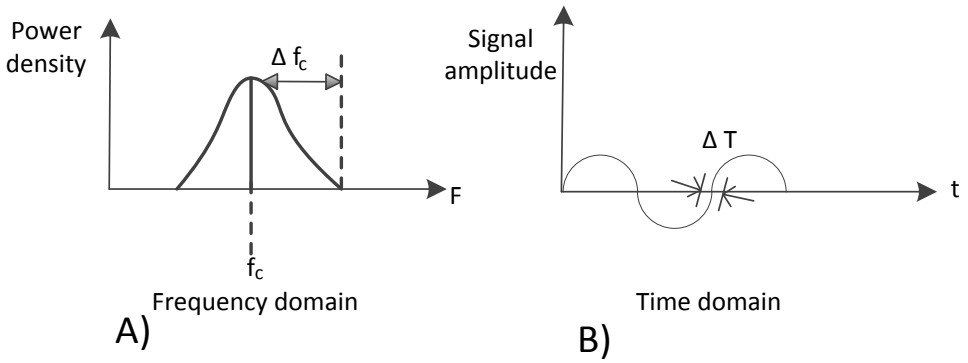


Figure 4-0-3

There are two types of sources for noise, internal and external:

- INTERNAL: Thermal variations can cause effects on the charge carries of a MOS device which can be a source for noise. Another source is the so called, flicker noise, this noise is created due to imperfection in the silicon lattice, imperfections that can be attributed to process variations and as devices get smaller this source of noise becomes more important.
- EXTERNAL: The dynamic noise created by the switching activity of MOS devices is the major contributor to the noise [13].

4.2 VCO PERFORMANCE MEASUREMENT

Various VCO designs are presented in this dissertation, it is important that all of them reach a practical performance, for this reason a practical performance of a USB 3.0 was chosen for this thesis, below are the specifications that must be meet.

1. Frequency: 5GHz.
2. Maximum Jitter: 1.5 Pico seconds.
3. Supply: 1.2 volts.

4.3 SOFWARE TOOLS

Cadence Virtuoso Design Suite is used for this project, three tools need to be used for the complete investigation and design of the different VCOs.

1. Virtuoso Schematic editor.
2. ADE (Analogue Design Environment): tool used for the AC, DC, and noise analysis.
3. ADE XL: As it´s name emphasizes this is a bigger version of the ADE, this tool is capable of performing monte carlo simulations.

4.5 PROCESS VARIATION TESTBENCH

All the designs need to be tested not only for corner cases, but for multiple process variations and the effects that these variations have on different technologies, it has been explained that performance degradation of a system due to process variations is mostly due to the random variations of oxide thickness t_{ox} and threshold voltage V_T, therefore, this project focuses on the manipulation of these two parameters. Every device in Cadence Virtuoso has a technology file, this file contains up to 40 parameters for CMOs technologies, these parameters dictate the behaviour of the device, by having access to these technology files a Monte Carlo simulation can be written and performed where parameters t_{ox} and V_T are varied through a Gaussian distribution, on figure 4.4 it can be seen a flow chart of this procedure.

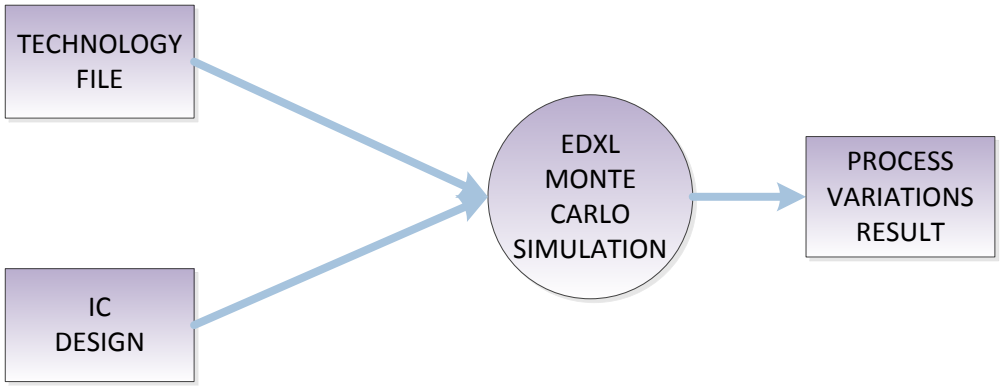


Figure 4.-0-4: process variations simulation flow chart

Process variations is a wide area to investigate, plus this project is also trying to design a system that is aware of them, therefore, this project is focusing only in inter-die variations, in other words, variations that occur by the same proportion to all the devices in the system, from now on every time that is mentioned process variations, these variations are happening equally to all devices.

5 DESIGNS

Multiple designs are investigated on papers and are implemented in the industry, each one giving different performance characteristics, in this thesis multiple designs are tested, in this section different designs are explained describing their performance.

5.1 RING OSCILLATORS

Ring oscillators can be divided in 2 sections, single ended or double ended.

5.1.1 SINGLE ENDED

The inverter is the simplest form of delay cell, schematic can be seen in figure 8a, is composed of a simple CMOS inverter, the delay of each cell is determined by the charging and discharging of the RC network where this RC network is a function of the parasitic capacitance and resistance of the MOS technology, figure 5.1b, this delay is calculated by equation 5.1, where the total capacitance is dependent on the variant parameter gate oxide capacitance C_{ox} .

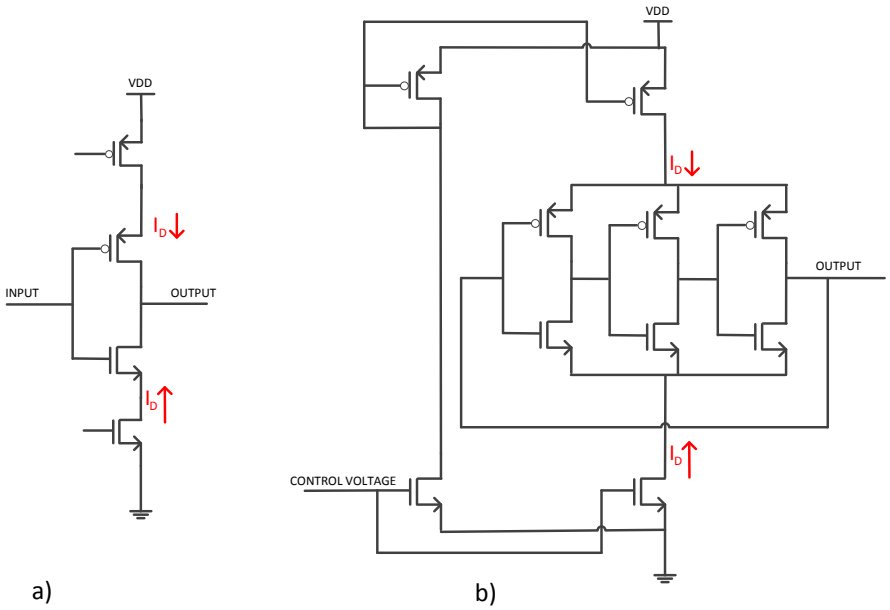
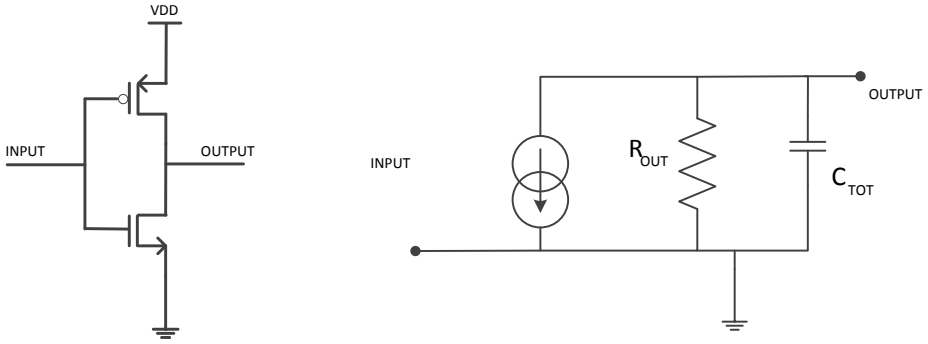


Figure 5-0-1: a) simple inverter schematic. b) single stage VCO



a) b)

Figure 5-0-2: a) inverter schematic b) small signal representation of the output node

$$t_d = C_{TOT} \times R_{out} \tag{5.1}$$

$$R_{out} = \frac{V_{DD}}{I_D}$$

$$C_{TOT} = C_{out} + C_{in} = \left(\frac{5}{2}\right) \times C_{ox} \times \left(W_p L_p + W_n L_n\right)$$

Going back to equation 3.7 where

$$f_o = \frac{1}{2 \times N \times t_d}$$

by rearranging we obtain

$$f_o = \frac{I_D}{N \times C_{TOT} \times V_{DD}}$$

Where I_D

$$I_D = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

$$K' = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$$

It is clear the dependency of the oscillation frequency to supply voltage V_{DD}, the oxide thickness t_{ox}, and threshold voltage V_T, this particular VCO design is called starved VCO because the inverters are starved for current.

It is required to have an odd number of stages in order to obtain a phase change of 180° in all the delay path.

5.1.2 DOUBLE ENDED OR DIFFERENTIAL CELLS

Another way to implement delay cells is by differential op amps (figure 5.3) with different configurations, where each delay cell must have a gain of 1 or greater, the total phase change across the delay path must be 180°, with this configuration it is possible to have even and odd number of stages, this is due to the fact that each differential delay cell can produce a phase shift of the input of 180° and 360°.

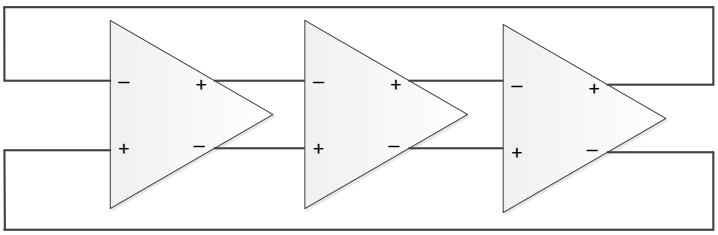


Figure 5-0-3: differential amplifier schematic

As the single ended ring oscillator, the time delay of each stage is dependent on parasitic capacitance and resistance, where the resistance is controlled by the current applied to the cell, this way of creating time delays is called resistive loads, figure 5.4a there are different ways of creating resistive loads, in figure 5.4b it can be seen what is called the triode load, this load is very sensitive to power supply variations V_{DD}, the resistance in this case is determined by the size of the MOS devices and the control voltage.

Another way is by is shown in figure 5.4C, these are called symmetric loads, as it can be seen this configuration is no more than a two current sources with resistive loads, symmetric loads are less sensitive to power supply changes due to their high impedance, on the other hand their frequency range is shorter as the devices need to be in saturation in order to function correctly.

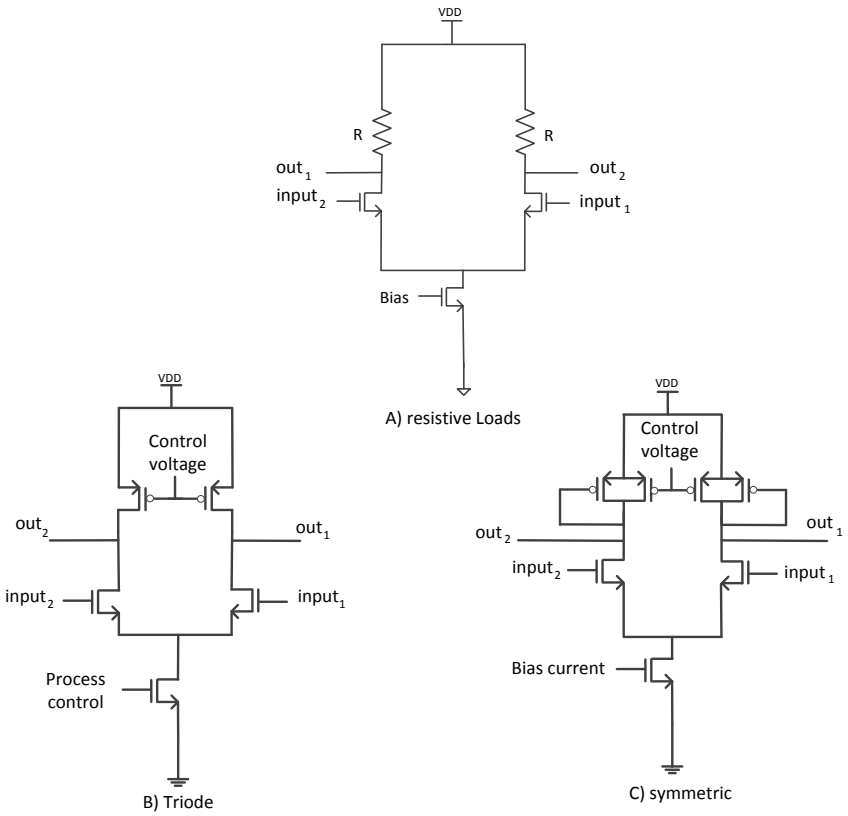


Figure 5-0-1: different ways of performing resistive loads

6 DESIGNS UNDER PROCESS VARIATIONS

In this section, all the described designs in the previous section are tested under corner cases and different process variations, every design was performed in 90, 180 and 350 nm technology so a comparison between these 3 technologies could be made, however the results for 350 nm are not presented as the oscillation frequencies that were achieved were very low in the range of 300 to 800 MHz, but the designs for these are in the submitted design files. The results for 180 nm can be found in the appendix A unfortunately there was not sufficient time to perform monte carlo simulation on this technology, but comparing the corner cases for 90 and 180 nm it can be observe that the performance degradation due to corner cases is quite similar.

6.1 INVERTER RING OSCILLATORS

This is the first design to be investigated; the complete schematic can be seen in figure 6.1, this design has a good voltage swing from V_{DD} to ground due to the last stage, in table 6.1, it is listed a performance summary of this design, the frequency range in this design is considerably high, this can be seen in figure 6.2 where the oscillation frequency response to the control voltage is plotted, the response is significantly linear. The cycle to cycle jitter is more than acceptable with a 0.1265% standard deviation. This design can be achieved with a low amount of transistors (only 12) compared with the other designs.

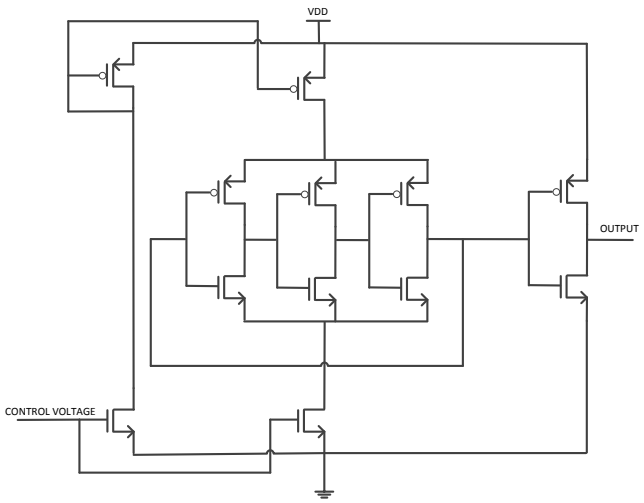


Figure 6-0-1: starved current VCO

Table 6-0-1: starved inverter performance

Frequency range	0.21 – 5GHz
Voltage range	0.2 – 1.5 Volts
current	120 µA
Supply voltage	1.2 Volts
Jcc	253 fsec. @ 5.1GHz
Phase noise @ 100KHz offset	-54 dBc
Phase noise @ 100MHz offset	-114 dBc
transistors	12

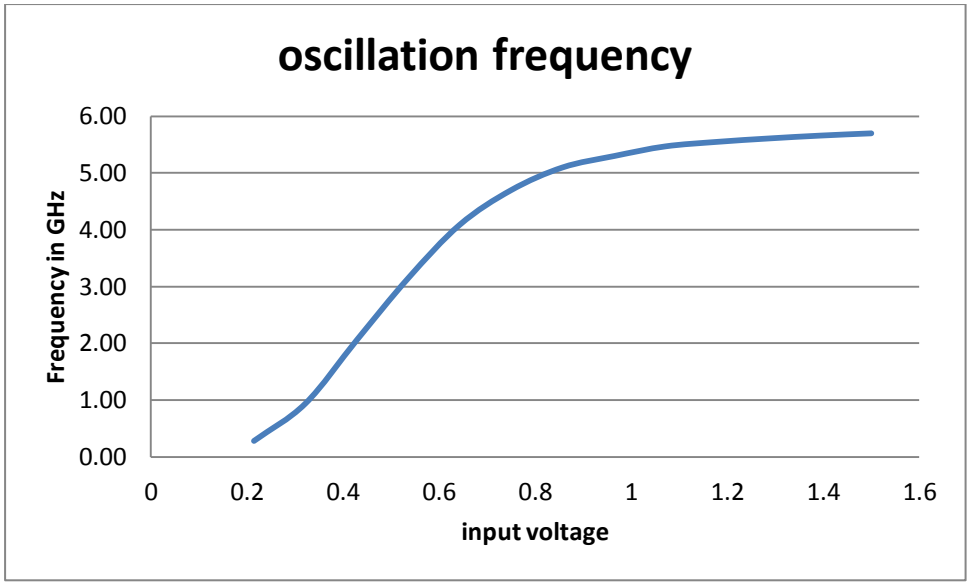


Figure 6-0-2: starved inverter frequency response

The investigation of this design under process corners can be seen in table 6.2, it is clear the degradation in terms of frequency range, all the other parameters are acceptable.

The design was also investigated under the variations of gate oxide thickness and voltage threshold, performing monte carlo simulation with 100 samples, and the variations in the oscillation frequency were observe, results are summarized in table 6.3, these tables are common on this report and the parameters need to be explain once, as the proper understanding of these tables is essential in this project.

- Oxide thickness and threshold voltage variations: this is the maximum percentage variation of these 2 parameters from their established values in the technology files, the variations are performed with a Gaussian distribution.
- Average frequency: the average VCO oscillation frequency from the 100 sample test run.
- Frequency variations in percentage: this is the average deviation of the VCO oscillation frequency from the average frequency due to the t_{ox} and V_{th} variations.

As an example, in table 6.3, when t_{ox} and V_{th} are varied 30% with a Gaussian distribution, we can see an average frequency of 3.99 GHz, where this frequency can suffer a deviation of $\pm 22.2\%$.

Table 6-0-2: starved current VCO under corner cases

	90 nm.			
Corner case	SS	SF	FS	FF
Frequency range	0.21 – 3.4GHz	0.21 – 5GHz	0.2 – 4.2GHz	0.21 – 6.5GHz
Voltage range	0.2 – 1.5 Volts	0.2 – 1.5 Volts	0.2 – 1.5 Volts	0.2 – 1.5 Volts
current	88 µA	135 µA	100 µA	171 µA
Supply voltage	1.2 Volts	1.2 Volts	1.2 Volts	1.2 Volts
Jcc	360 fsec. @ 3.4GHz	261 fsec. @ 5GHz	285 fsec. @ 4.1GHz	193 fsec. @ 6.5GHz
Phase noise @ 100KHz offset	-65 dBc	-64 dBc	-54 dBc	-52 dBc
Phase noise @ 100MHz offset	-125 dBc	-124 dBc	-114 dBc	-112 dBc
transistors	12	12	12	12

Table 6-0-3: starved current VCO under process variations simulation.

STARVED INVERTER 90 NM TECHNOLOGY

Oxide thickness and threshold voltage variations	5%	10%	20%	30%
Frequency variations in percentage	± 2.5 %	± 5.2%	± 11.34%	± 22.2%
Mean frequency	4.4	4.3	4.23	3.99

Apart from the process variations, the deviation of the oscillation frequency due variations in temperature and voltage supply V_{dd} was experimented, temperature was varied from -40° to 120° and voltage supply $\pm 10\%$, the results can be seen in figure 6.3 for temperature variation and in figure 6.4 for voltage variation. It is clear from these results that the VCO performance is highly dependent on these 2 parameters, specially to temperature variations.

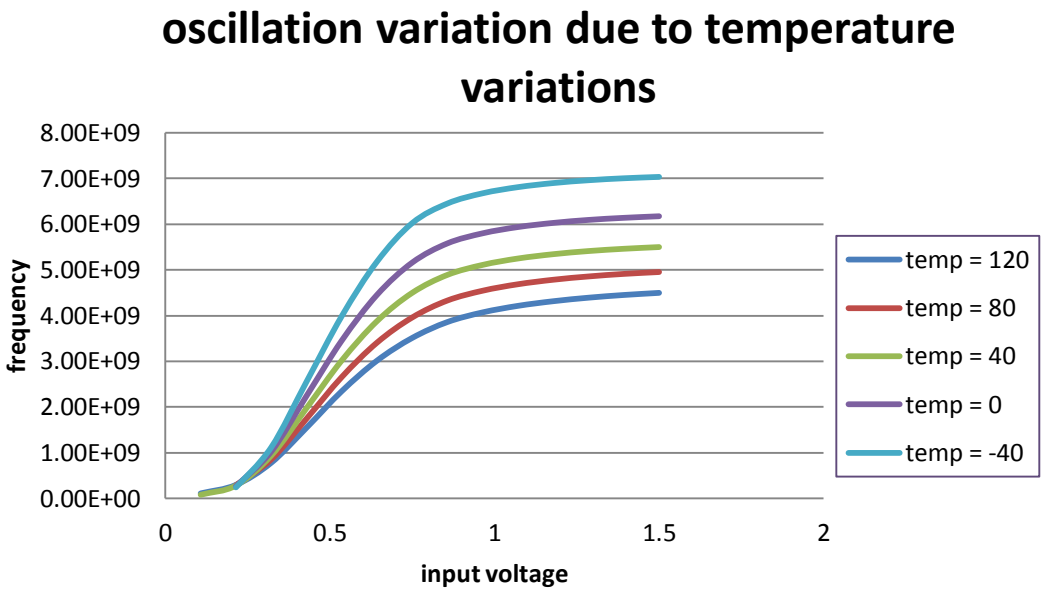


Figure 6-0-3: starved current VCO frequency response at different temperatures.

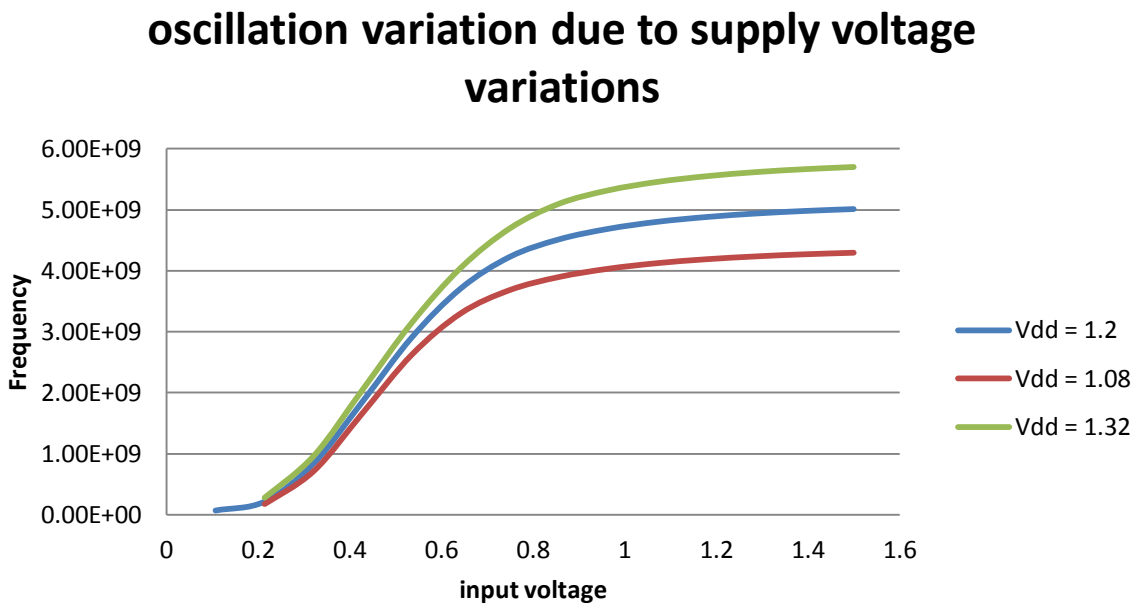


Figure 6-0-4: starved current VCO frequency response under different power supply voltages

Because of the single ended nature of this design, the DC component on the output is quite high, due to this fact, the harmonic 0 is higher than other designs.

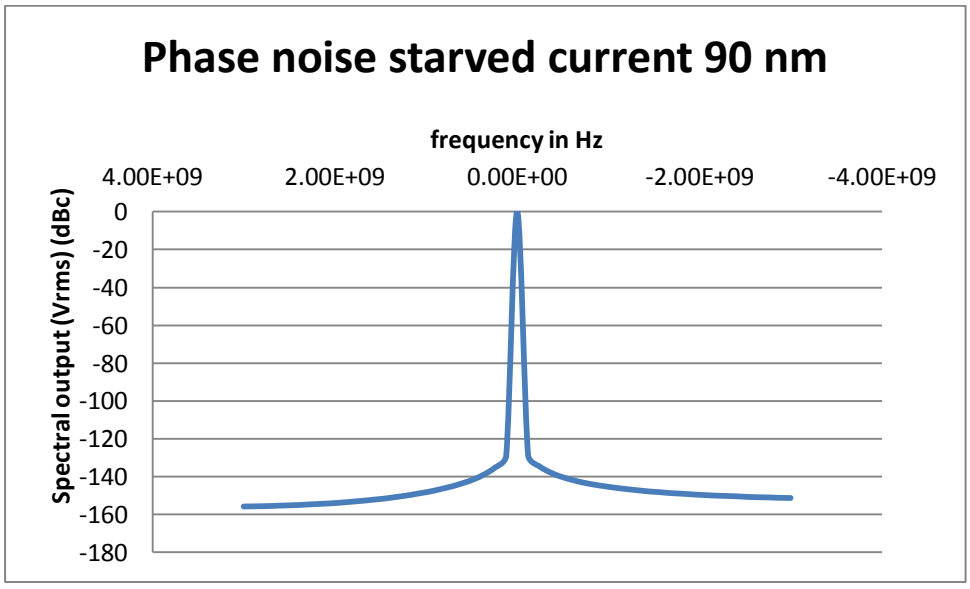


Figure 6-0-5: phase noise analysis of starved current VCO

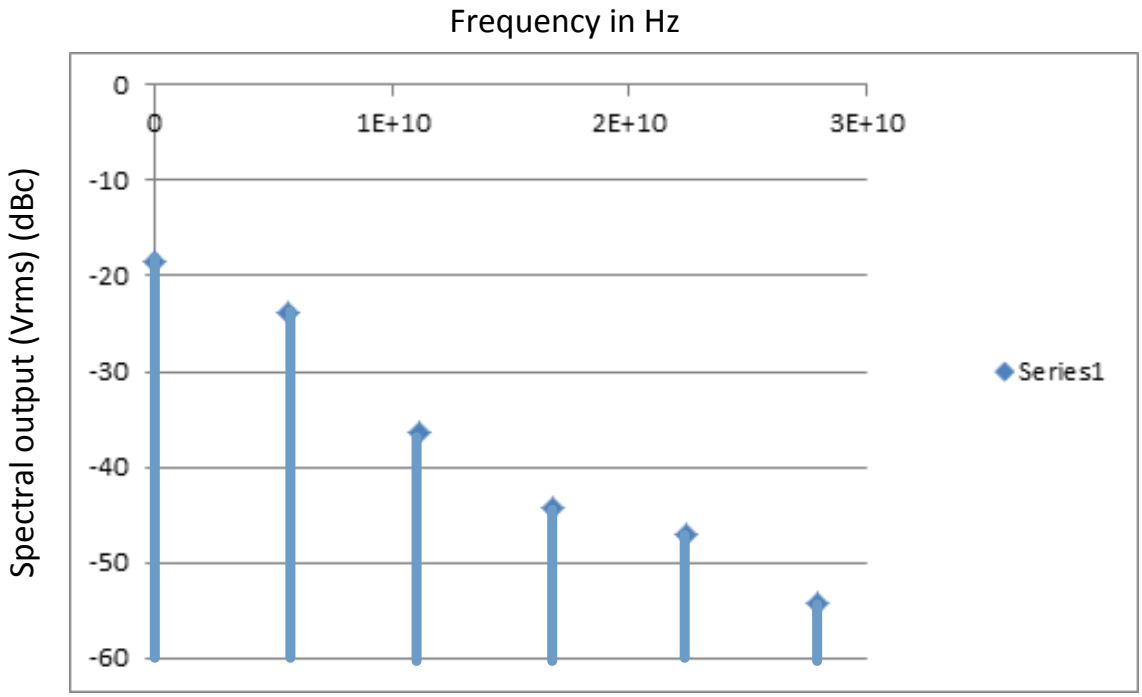


Figure 6-0-6: harmonics of starved current VCO

6.2 TRIODE CELL

This design needs to be implemented with 5 delays cells in 90 nm technology and 3 delay cells in 180 nm. Appendix A This design has proven to be successful in frequency range and specially in phase noise and cycle to cycle jitter. The results for the design under corner cases can be seen in table 6.5, these results are similar to the previous design the starved ring oscillator, where the frequency range suffers considerably. An advantage of this design over the starved inverter is the more linear frequency response to the control voltage, figure 6.8 , another advantage that can be seen is the lower jitter in all corner cases. As explained before the frequency response of this design is very sensitive to variations in supply voltage, figure 6.8 shows this. In terms of monte carlo simulations of process variations the frequency degradation is very similar to the one in the starved inverter design, table 6.6 shows these results. The results for the noise analysis under normal conditions can be seen in figures 6.10 and 6.11.

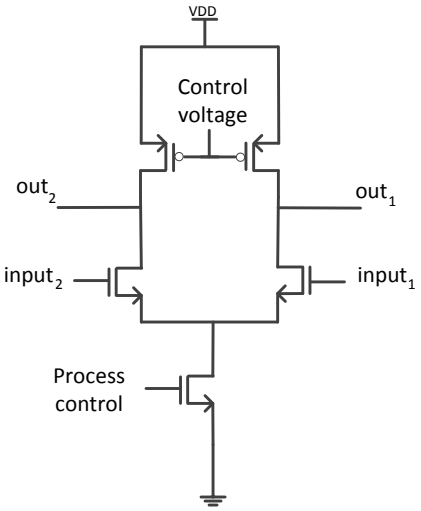


Figure 6-0-7: triode delay cell

Table 6-0-4: triode VCO performance parameters

90 nm	
triode	
Frequency range	5 – 0.46GHz
Voltage range	0 – 0.85 Volts
current	250 µA
Supply voltage	1.2 Volts
Jcc	232 fsec. @ 5.1GHz
Phase noise @ 100KHz offset	-64 dBc
Phase noise @ 100MHz offset	-124 dBc
transistors	36

	triode			
	90 nm.			
Corner case	SS	SF	FS	FF
Frequency range	3.7 – 0.27GHz	5.5 – 0.55GHz	4.25 – 0.34GHz	6.2 – 0.67GHz
Voltage range	0 – 0.85 Volts	0 – 0.85 Volts	0 – 0.85 Volts	0 – 0.85 Volts
current	250 µA	250 µA	150 µA	150 µA
Supply voltage	1.2 Volts	1.2 Volts	1.2 Volts	1.2 Volts
Jcc	137 fsec. @ 3.6GHz	264 fsec. @ 5.4GHz	128 fsec. @ 4.3GHz	98 fsec. @ 6.2GHz
Phase noise @ 100KHz offset	-66dBc	-66 dBc	-64 dBc	-64 dBc
Phase noise @ 100MHz offset	-126 dBc	-127	-125 dBc	-124 dBc
transistors	26	36	36	36

Table 6-0-5: triode VCO under corner cases

Table 6-0-6: triode VCO under process variations results.

TRIODE CELL 90 NM TECHNOLOGY

Oxide thickness and threshold voltage variations	5%	10%	20%	30%
Frequency variations in percentage	± 1.8 %	± 3.7%	± 10.04%	± 22.08%
Center frequency in GHz	5	5.036	4.87	4.5

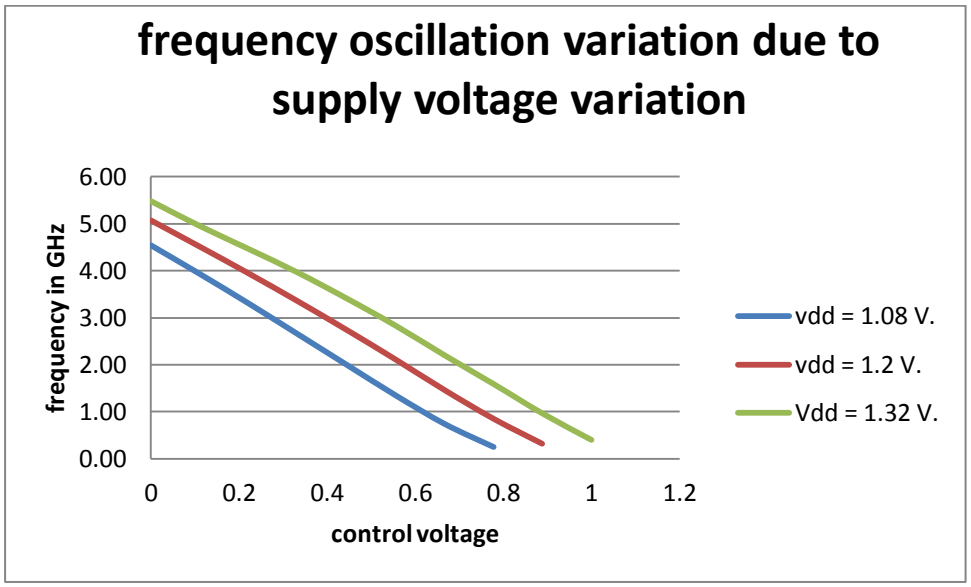


Figure 6-0-8: triode frequency response at different voltage supply.

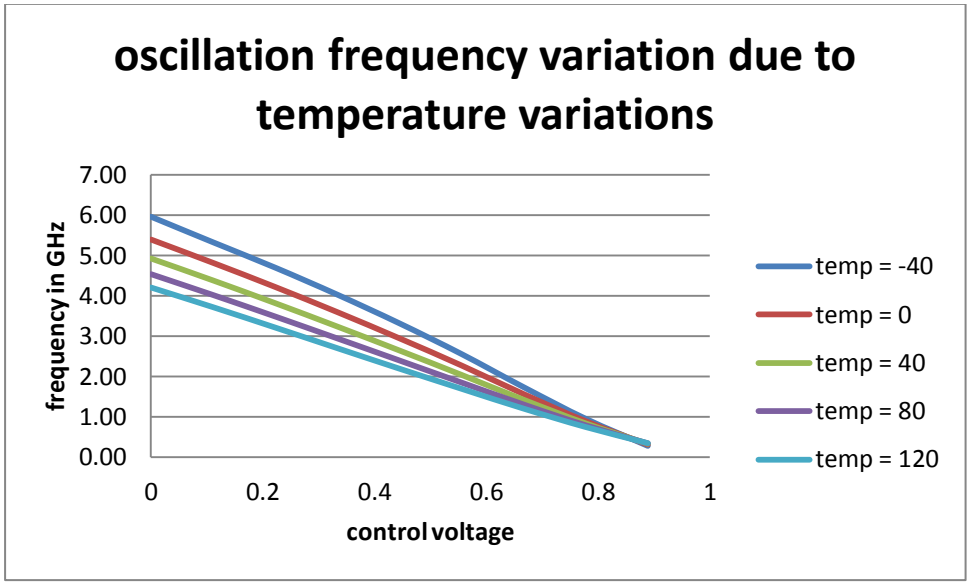


Figure 6-0-9: triode VCO frequency response at different temperatures

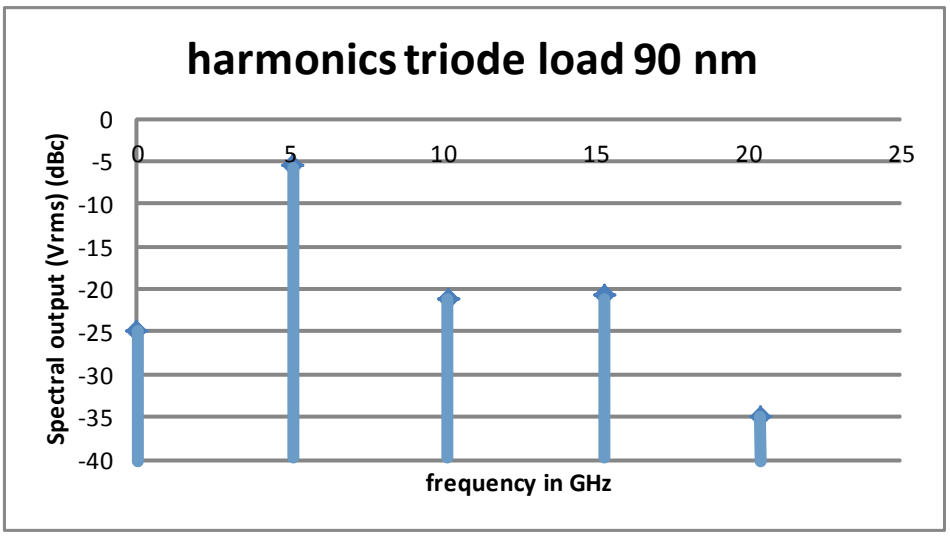


Figure 6-0-10: Triode VCO harmonics.

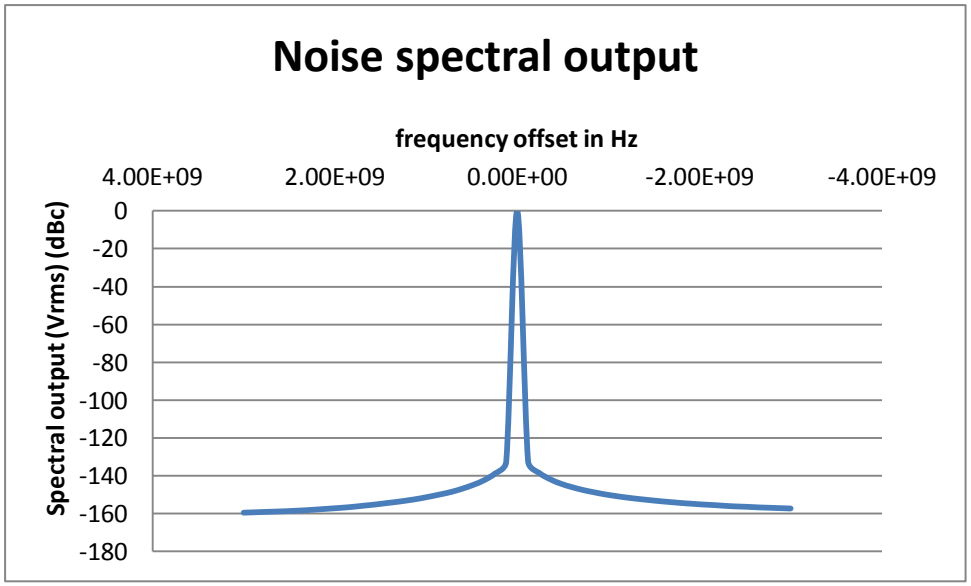


Figure 6-0-11: Triode VCO phase noise analysis.

6.3 SYMMETRIC LOAD DIFFERENTIAL RING OSCILLATORS

This design was chosen for investigation due to its known high quality [10], this design achieves a lower frequency range compared with previous designs; this is translated into a more linear frequency response, as it can be observe in figure 6.13. This design needs to be implemented with 5 delay cells for 90 nm. Technology and 3 delay cells for 180 nm, it is required a high number of transistor for it´s implementation, and a voltage supply of 1.5 is needed, all this means a higher power consumption compared with the other designs. Table 6.7 summarizes this design performance. Table 6.8 shows the performance of this design under corner cases, similar degradation as in the previous designs can be observe, the phase noise analysis shows appropriate results for this matter.

Table 6.9 shows the results of this design under monte carlo simulations for process variations, variations of the frequency range due to process variations showed to be minor in this design. In the previous two designs, when process variations of $\pm 30\%$ were done, both cases showed a frequency variation $\pm 22\%$ when in this case a variation of $\pm 17\%$ is achieved, this means a reduction of 5%, this reduction is achieved as well for process variations of $\pm 20\% \; and \; \pm 10\%$.

In terms of power supply and temperature variations, results can be seen in figures 6.13 and 6.14, as explained before this design suffers less degradation in terms of power supply variations.

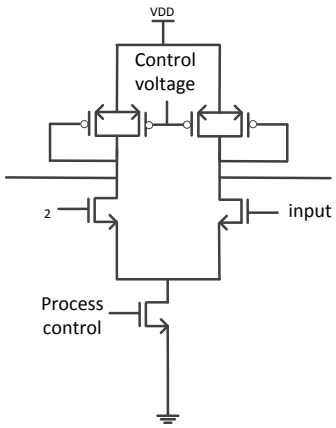


Figure 6-0-12: symmetric delay cell

Table 6-0-7: Symmetric VCO performance parameters

Frequency range	5 – 2.4GHz
Voltage range	0 – 0.85 Volts
current	150 µA
Supply voltage	1.5 Volts
Jcc	197 fsec. @ 5GHz
Phase noise @ 100KHz offset	-60 dBc
Phase noise @ 100MHz offset	-120 dBc
transistors	36

Table 6-0-8: Symmetric VCO under corner cases

	symmetric			
	90 nm.			
Corner case	SS	SF	FS	FF
Frequency range	3.6 – 2.8GHz	5.6 – 2.6GHz	4 – 2.6GHz	6.3 – 3.5GHz
Voltage range	0 – 0.85 Volts	0 – 0.85 Volts	0 – 0.85 Volts	0 – 0.85 Volts
current	150 µA	150 µA	150 µA	150 µA
Supply voltage	1.5 Volts	1.5 Volts	1.5 Volts	1.5 Volts
Jcc	245 fsec. @ 3.8GHz	256 fsec. @ 5.4GHz	210 fsec. @ 3.9GHz	98 fsec. @ 6.2GHz
Phase noise @ 100KHz offset	-62dBc	-40 dBc	-66 dBc	-64 dBc
Phase noise @ 100MHz offset	-122 dBc	-100 dBc	-120 dBc	-124 dBc
transistors	36	36	36	36

Table 6-0-9: symmetric VCO under process variations analysis

SYMMETRIC CELL 90 NM TECHNOLOGY

Oxide thickness and threshold voltage variations	5%	10%	20%	30%
Frequency variations in percentage	± 1.36 %	± 2.9%	± 7.6%	± 17.08%
Center frequency in GHz	5.14	5.1	4.1	4.8

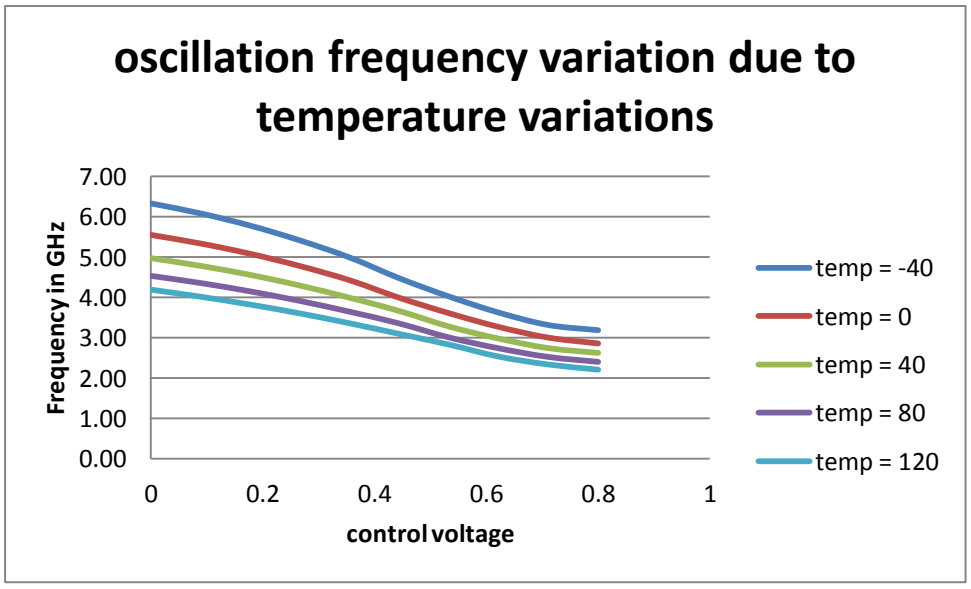


Figure 6-0-13: symmetric VCO frequency response at different temperatures

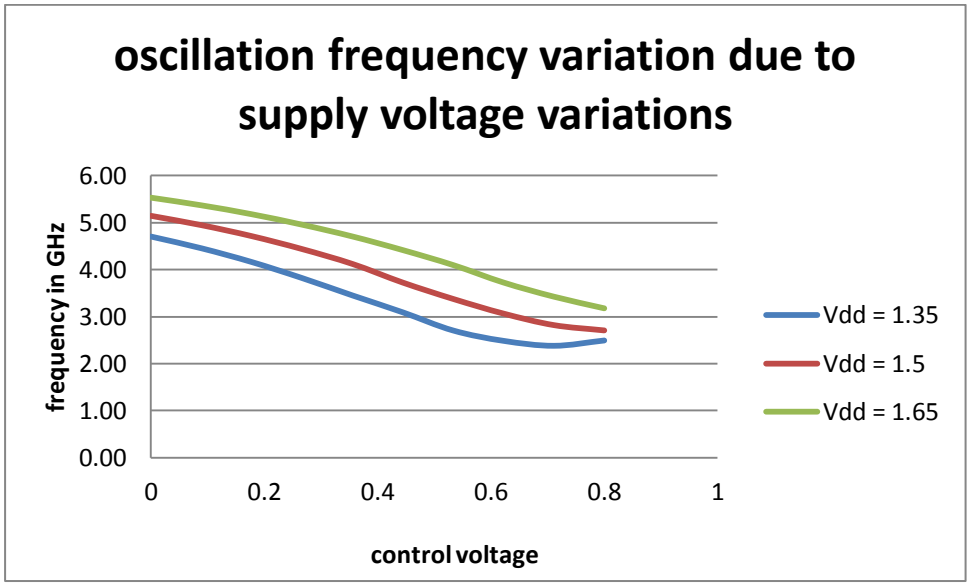


Figure 6-0-14: symmetric VCO frequency response under different power supply voltages

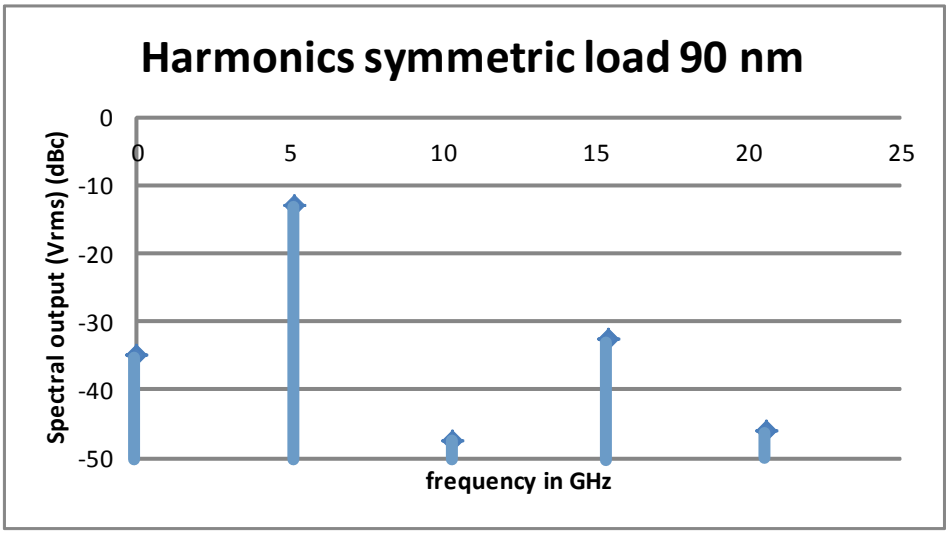


Figure 6-0-15: symmetric VCO harmonics

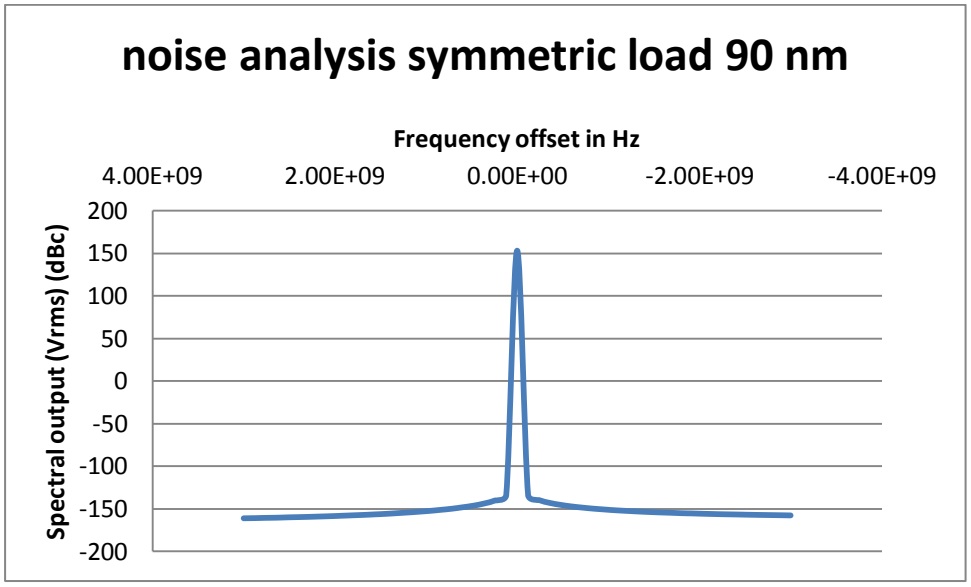


Figure 6-0-16: symmetric VCO phase noise analysis

6.4 LC VCO

This design is based on an LC tank, in contrast with all the previous ones that were ring oscillators. In figure 6.17 it can be seen the schematic for this design, the capacitance is formed by PMOS varactors, for simulation simplicity the inductance is not spiral. Table 6.10 shows the performance characteristics of this design, this design can achieve a practical frequency 4.7 GHz, but the frequency range is low, it can only be tuned 100 MHz by the current control, this can be seen in figure 6.18, on the other hand this design holds some advantages over the ring oscillators, the phase noise is extremely low in this design, fact that is emphasize on the extremely low cycle to cycle jitter achieving the incredible figure of 11 fseconds in a high frequency of almost 5 GHz.

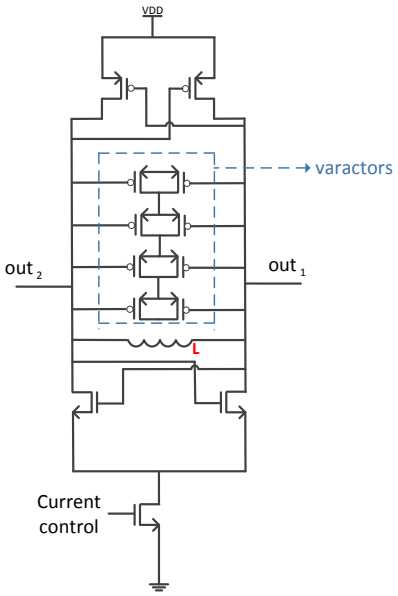


Figure 6-0-17: LC oscillator schematic

Table 6-0-10: LC performance parameters

LC tank oscillator

Frequency range	4.73 – 4.63GHz
current range	10 – 75uA
Supply voltage	1.2 Volts
Jcc	11.48 fsec. @ 4.7GHz
Phase noise @ 100KHz offset	-84 dBc
Phase noise @ 100MHz offset	-144 dBc
transistors	13

Table 6-0-11: LC tank under process variations

LC tank 90 NM

Oxide thickness and threshold voltage variations	10%	20%	30%
Frequency variations in percentage	± 0.05%	± 0.93%	± 2.3%
Center frequency in GHz	4.6	4.6	4.6

In table 6.11 it can be seen the results of the LC tank under monte carlo simulations for process variations, at a first look it shocks how low the frequency variations are, this is because there is a problem with the inductor technology file, from the University files is only possible to use ideal inductors, the technology file of an ideal component cannot be manipulated for a monte carlo analysis, this means that during the monte carlo simulation the inductor is not suffering any process variation, remembering equation 3.3 (page 6) where it states that the carrier frequency of this design is highly dependent on the inductance we can see the why of these results. In order to simulate process variations correctly in this design, a non-ideal inductor would have to be created, including its own technology file, this is a very difficult task, and due to the lack of time it was decided to manipulate the inductance parameter on a manual fashion, as explained before, in [7] states that metal thickness variations of the spiral inductors can cause $\pm 30\%$ variation in the inductance value, by knowing this, the inductance was varied $\pm 30\%$ of its stated value, the results of this simulation are shown in figure 6.19, where it can be seen how dependent is this design to process variations in the inductance.

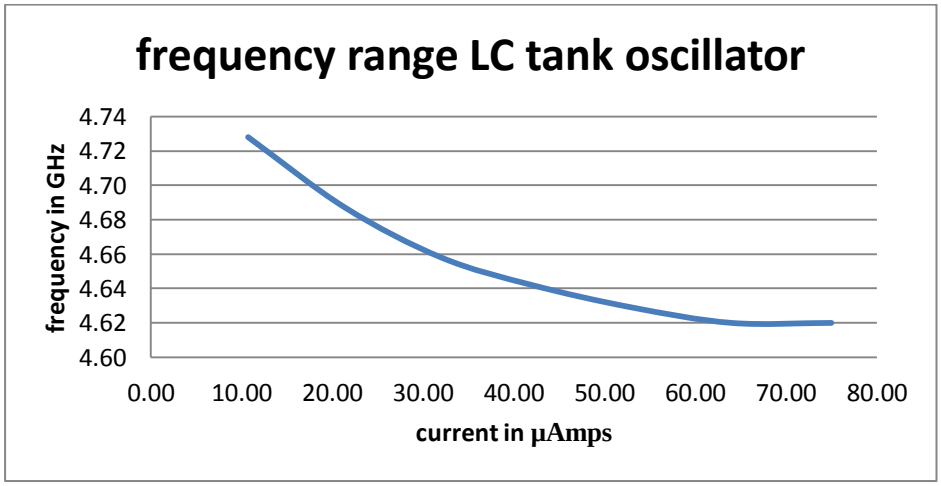


Figure 6-0-18: LC tank frequency response

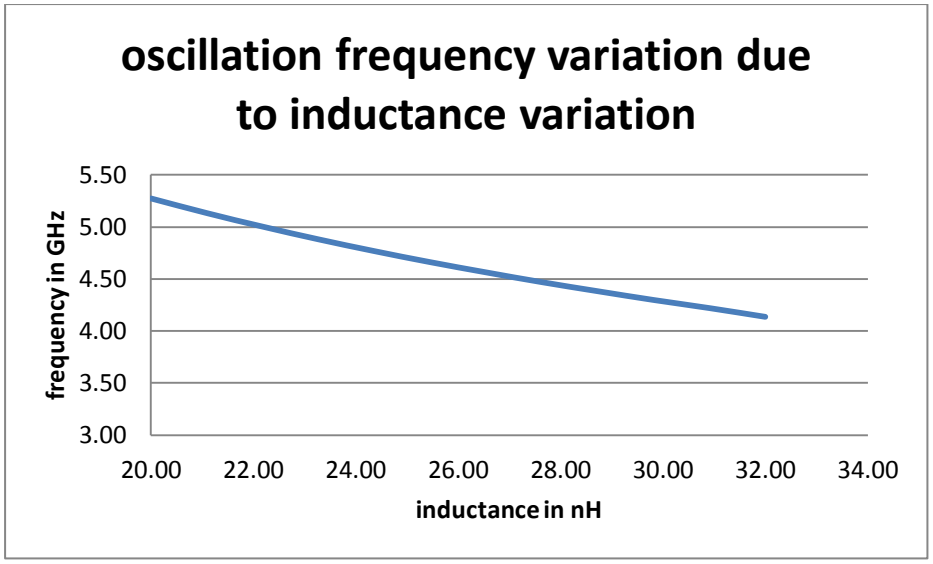


Figure 6-0-19: frequency response dependency to inductance L

6.5 CHAPTER CONCLUSION

Four different designs were investigated in this chapter, each one offering different advantages and disadvantages, below there is a summary of all.

1. Inverter (current starved): few transistors are required for the implementation of this design therefore this design offers the best performance in terms of power consumption, the system degradation due to process variations is severe and the system behaves with low noise.
2. Triode Load: this design suffers the most performance degradation due to process variations, apart is very sensitive to any temperature or power supply degradation, on the other hand is the best design in terms of low noise.
3. Symmetric design: this design has shown to be the most successful of all in terms of process variations, with a considerably low jitter and is the least sensitive to power supply variations, but it requires a high number of transistors plus it needs a power supply of 1.5 volts, this makes this design the worst for power consumption.
4. LC tank: this design shows an extremely low phase noise and low power due to the small amount of MOS transistors required for its implementation, the disadvantages are the extremely low frequency tuning range and the huge performance degradation that is created due to the inductance variation.

From the four designs above it was taken the decision to discard the triode load and LC tank for future work, in the next section improvements are performed to reduce the performance degradation of the other 2 designs due to random process variations

7 PROCESS VARIATION AWARE VCO

In the previous chapter it was observed the dependency of VCO's oscillation frequency to process variations, voltage supply and temperature. This project focuses on process variations; therefore, this chapter presents two solutions that minimize the degradation of the oscillation frequency due to process variations, the two solutions are:

1. Increase the current: In the previous chapters it was seen that every VCO investigated for this project is dependent on a bias current (starved inverter, triode and symmetric), if we increase the number of currents being applied to the VCO, this is illustrated in figure 7.1, the VCO is more dependent on these currents and is less dependent on the process parameters, this idea will be explained deeper later, but it must be mentioned that is not a good idea as it introduces more power consumption to every VCO, fact that is obviously not practical for any system.

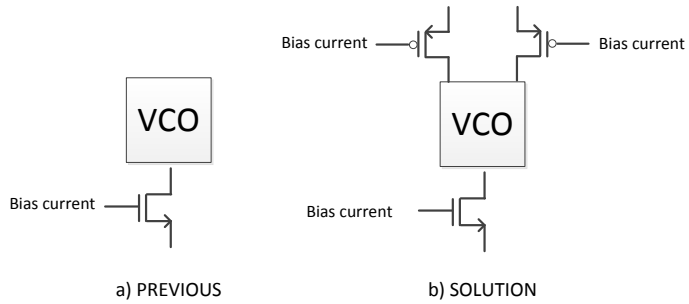


Figure 7-0-1

2. Process variation aware control voltage: A much better idea than the previous one is to create a system that is capable of sensing the process variations that occur to all devices by equal amount and combine this information with the control voltage through a differential amplifier. This way the control voltage will slightly increase or decrease depending on process variations and due to the linear frequency response of every VCO to the control voltage this can be achieve.

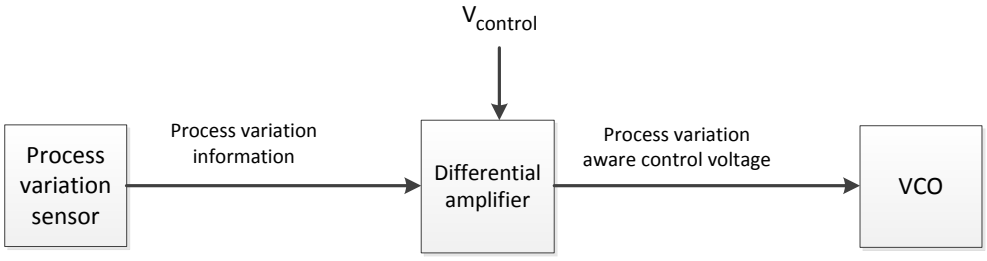


Figure 7-0-2

7.1 PROCESS VARIATION AWARE CONTROL VOLTAGE

In order to implement this solution, the flowchart presented in figure 7.3 had to be followed.

1. It is required to perform a deeper investigation about the effects of process variations on the VCO performance, especially on the oscillation frequency, in order to create a solution it was necessary a deeper understanding of the process variations problem.
2. It was required to design a sensor capable of sensing the random process variations that could happen to all devices by equal amount.
3. A differential amplifier whose performance is not affected by any process variations needed to be design. The differential amplifier output can be simplified by the equation below

$$Diff_{out} = V_{control} - process\ variation\ sensor$$

It is essential for the correct functionality of the differential amplifier that the values of the 2 inputs, control voltage and process variation sensor, are not corrupted by any process variation that may occur in the differential amplifier.

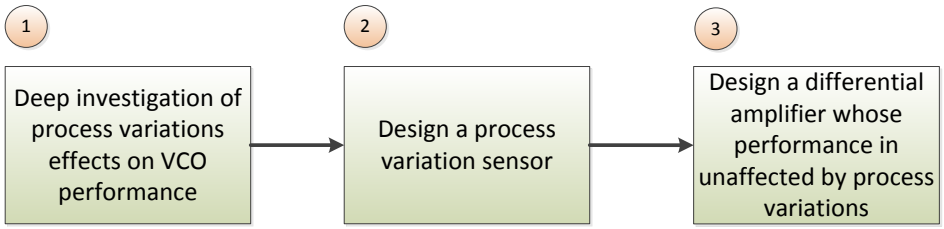


Figure 7-0-3: flow chart to achieve process variation aware VCO

7.1.1 DEEPER INVESTIGATION OF PROCESS VARIATIONS.

In order to implement the explained designs in chapter 6, it is required the usage of NMOS and PMOS devices, the behaviour of these devices is different and therefore it requires the investigation of process variations to be separated into 2 parts:

1. It is necessary to know in what degree the VCO performance is tied to the process variations that occur to NMOS and PMOS separately.
2. As the project focuses on the variations of t_{ox} and V_{th}, it is necessary to know which one of these two contributes more to the VCO performance degradation.

In tables 7.1 and 7.2 it can be seen these investigations in two designs, starved inverter and symmetric, here we can see 2 important facts:

1. When t_{ox} and V_{th} are varied at the same time, but first these variations only affecting to NMOS devices and after affecting only to PMOS devices, we can observe that the degradation caused by PMOS to the oscillation frequency is much higher than the one caused by NMOS, specially note when the process variations are 30% for the inverter case table 7.1 and 7.2, for NMOS the oscillation frequency varies ±11.3%, but in the PMOS case is ±17.7%.
2. Since it was discovered that process variations on PMOS affects more to the degradation of the oscillation frequency than process variation on NMOS, it was important to know which

parameter t_{ox} or V_{th} was affecting more to the degradation, both parameters were varied separately and it was found that for both designs, the gate oxide thickness t_{ox} affects much more to the VCO performance degradation, principally in the symmetric design.

Table 7-0-1: Deep investigation of INVERTER or starved current VCO under different process variations

NMOS and PMOS investigation

INVERTER 90 NM (NMOS VARIATION)

Oxide thickness and threshold voltage variations	10%	20%	30%
Frequency variations in percentage	± 3.2%	± 6.6%	± 11.3%
Center frequency in GHz	4.7	4.6	4.6

INVERTER 90 NM (PMOS VARIATION)

Oxide thickness and threshold voltage variations	10%	20%	30%
Frequency variations in percentage	± 4.3%	± 9.5%	± 17.7%
Center frequency in GHz	4.7	4.6	4.48

t_{ox} and V_{th} variation

INVERTER 90 NM (PMOS VARIATION)

Threshold voltage	10%	20%	30%
Frequency variations in percentage	± 3.2%	± 6.5%	± 9.78%
Center frequency in GHz	4.7	4.7	4.7

INVERTER 90 NM (PMOS VARIATION)

Oxide thickness	10%	20%	30%
Frequency variations in percentage	± 3.1%	± 7.8%	± 16.2%
Center frequency in GHz	4.7	4.6	4.5

Table 7-0-2: Deep investigation of symmetric VCO under different process variations

NMOS and PMOS investigation

SYMMETRIC 90 NM (NMOS VARIATION)

Oxide thickness and threshold voltage variations	10%	20%	30%
Frequency variations in percentage	± 0.98%	± 2.69%	± 11.3%
Center frequency in GHz	5.1	5	4.9

SYMMETRIC 90 NM (PMOS VARIATION)

Oxide thickness and threshold voltage variations	10%	20%	30%
Frequency variations in percentage	± 3.03%	± 7.54%	± 15.16%
Center frequency in GHz	5.1	5	4.8

t_{ox} and V_{th} variation

SYMMETRIC 90 NM (PMOS VARIATION)

Threshold voltage	10%	20%	30%
Frequency variations in percentage	± 2.23%	± 4.47%	± 6.8%
Center frequency in GHz	5.1	5.1	5.1

SYMMETRIC 90 NM (PMOS VARIATION)

Oxide thickness	10%	20%	30%
Frequency variations in percentage	± 2.6%	± 8.38%	± 17.4%
Center frequency in GHz	5.1	5	4.8

7.1.2 PROCESS VARIATION SENSOR

As process variations on PMOS devices are the major contributors to oscillation frequency degradation, a sensor capable of sensing PMOS process variations with as much accuracy as possible needs to be design. A special PMOS diode was used for this purpose; the schematic for this can be seen in figure 7.4, where the control voltage is connected directly to this process variation sensor, table 7.3 shows the monte carlo simulations when V_T and t_{ox} are varied separately and the control voltage is kept constant at $1.2\ volts$, again variations are higher due to t_{ox} than to V_T. Table 7.4shows the results when V_T and t_{ox} are varied 30% on the same simulation, but this time the control voltage is varied, the purpose of this simulations is to observe if the sensor behaves on the same manner at different control voltages, as the results show the voltage variations are almost the same for all the control voltages cases.

Table 7-0-4:oxide thickness and threshold voltage variation separately

t_{ox} and V_{th} variation

SENSING 90 NM (PMOS VARIATION)

Oxide thickness	10%	20%	30%
Voltage variation	± 6.48%	± 11.12%	± 18.33%
Average Voltage in Volts	0.987	0.908	0.998

SENSING 90 NM (PMOS VARIATION)

Threshold voltage	10%	20%	30%
Voltage variation	± 5.7%	± 9.35%	± 11.62%
Average Voltage in Volts	0.990	0.994	0.998

Table 7-0-3: PMOS performance under different control voltages

SENSING 90 NM (PMOS VARIATION) under different control votages

Control voltage	1.2	1	0.8	0.6	0.4	0.2
Voltage variation	± 13.05%	± 14.25%	± 13.74%	± 12.76%	± 11.51%	± 10.61%
Average Voltage in Volts	0.987	0.835	0.684	0.525	0.356	0.179

This PMOS diode can sense as accurately as possible the voltage threshold variations, equation 7.1 expresses the drain current

$$I_D = \left(\frac{K'W}{2L}\right)[(V_{GS} - V_T)^2] = \frac{\beta}{2}(V_{GS} - V_T)^2 \qquad 7.1$$

or

where $K' = \mu_p C_{ox}$

$$V = V_T + \sqrt{2I_D/\beta} \quad (7.2)$$

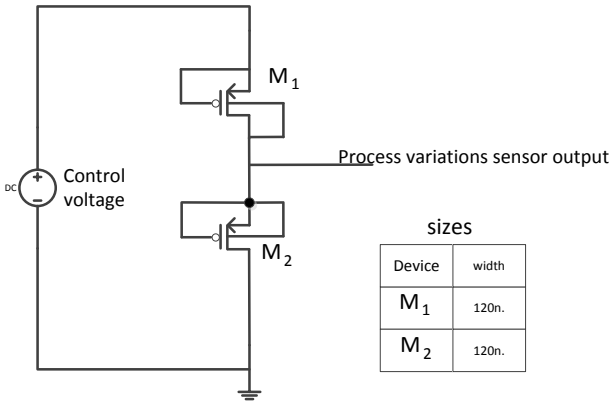


Figure 7-0-4: PMOS proves variation sensor

7.2

It is clear from equation 7.2 that any small change in V_T and t_{ox} will create a variation in the output voltage, the sizes W/L of the PMOS are kept to the minimum so the changes in V_T and t_{ox} are emphasized, figure 7.5 shows the % variation in voltage as the width of both PMOS are increased, as the widths get larger, the % variations in voltage decreases.

The bulk is not connected to the voltage supply, this means that the voltage that is applied to the bulk is not constant, with this configuration we can find 2 transconductances modelling the devices, g_m and g_{mb} (body transconductace), and with two transconductance the process variations can be measure with more accuracy.

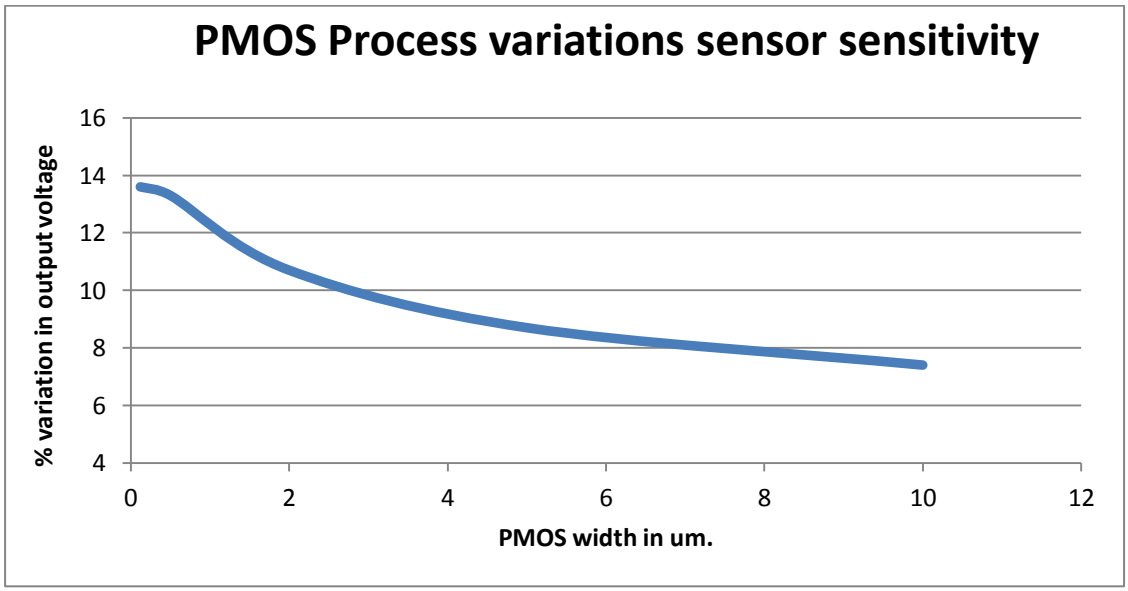


Figure 7-0-5:

In order to measure the V_T and variations on NMOS devices the equivalent circuit can be seen in figure 7-6, as the variations happening in NMOS devices are less it is obvious that the % variations in the sensing voltage is less as well, this can be seen in figure 7.7, where V_T and t_{ox} are varied 30% at different widths values

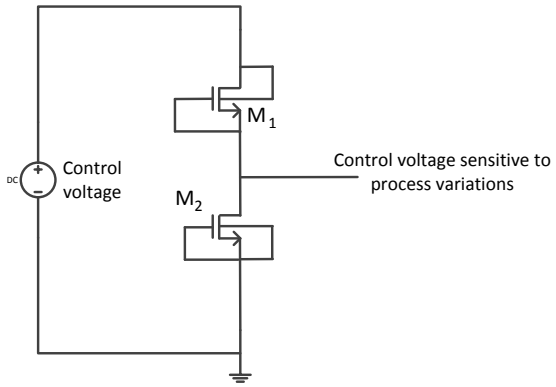


Figure 7-0-6: NMOS process variations sensor

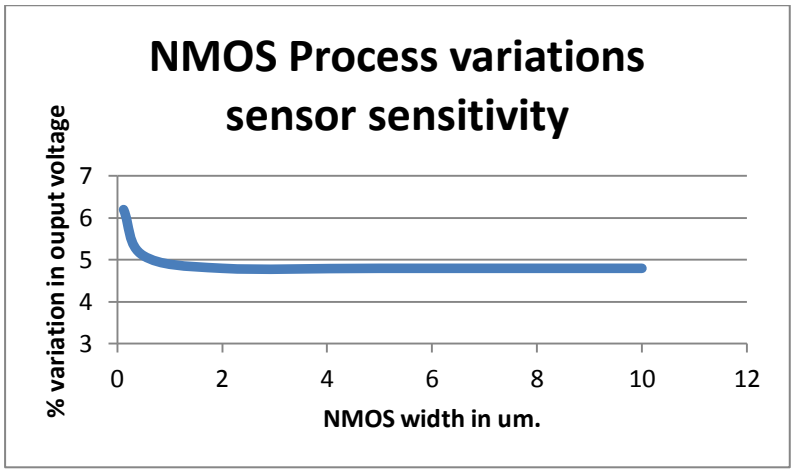


Figure 7-0-7:

From the just presented results it can be summarize two facts:

1. Process variations V_T and t_{ox} can be sense and by varying the width of sensor devices (PMOS), the sensitivity of this sensor can be tuned (figure 7.5).
2. The sensitivity of this sensor is almost the same under different control voltage values (table 7.4)

From these two facts, two different steps were followed next:

1. The VCO was adapted to the process variations sensor: this means that the VCO performance in terms of frequency tuning range was adapted to the process variations sensor, a high level schematic of this is shown on figure 7.8, the disadvantage of this method is the limitations in terms of frequency tuning range, best way to explain this is by an illustration, in figure 7.9a it can be seen the linear response of the VCO starved inverter, when the VCO is design ideally we want to obtain a frequency of 4 GHz with a control voltage of 0.7, but due to process variations we obtain 4.4 GHz with 0.7 (figure 7.9C), but if the frequency range sensitivity to process variations is the same as the process variations sensor, then the system will adapt so a frequency of 4 GHz is achieved.

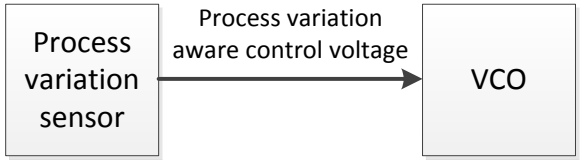


Figure 0-8

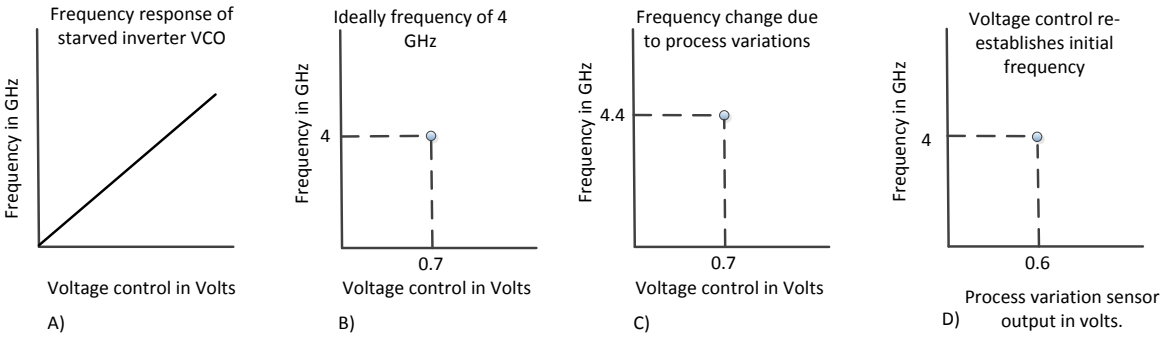


Figure 7-0-9

2. The other method is to adapt the process variation sensor information to the VCO, this idea was explained before figure 7.3 and it will be shown on the next section of this chapter.

Method 1 was tested with the starved inverter configuration, in table 7.5 it can be seen the results when the control voltage was set to 1, comparing this results with table 6.3 it can be seen a 4% improvement in the 20% and 30% process variations cases, this is not a tremendous improvement but it needs to be taken into account the high frequencies that are achieved, around 4 GHz.

Table 7-0-5: method 1 tested on starved current VCO

STARVED INVERTER 90 NM TECHNOLOGY

Oxide thickness and threshold voltage variations	5%	10%	20%	30%
Frequency variations in percentage (Δ)	± 2 %	± 4.3%	± 7.5%	± 18%
Average frequency in GHz	3.9	3.7	3.8	4.1
Variation in process variations sensor output (β)	±15 mV	±19 mV	±45 mV	±83 mV
Average process variations output	0.760 mV.	0.743mV	0.756mV	0.789mV
Control voltage	1	1	1	1

As explained before this method has its limitations and is difficult to configure if it wants to be implemented, in order to implement it we need to follow 3 steps:

1. Observe frequency variations in VCO: As every VCO behaviour to process variations is different from other VCOs, it is required to observe the variations in frequency due to process variations, in figure 7.10a it can be seen an illustration of this, ideally frequency point X will not suffer any variations due to process variations, but unfortunately point X will suffer a variation of $\pm \Delta$.
2. Observe voltage variations in process variations sensor: it was explained that the process variations sensor sensitivity is inversely proportional to the PMOS width, but the output voltage of this sensor is also inversely proportional to the PMOS width, figure 7.11. The process variations sensor output will suffer a variation of $\pm\beta$ from voltage point Y due to process variations, figure 7.10b, this variation β will depend on the PMOS width.
3. Adjust the PMOS width: with the appropriate variation in β, a decrement in Δ variation can be achieved, and this is shown in table 7.5, in this case both PMOS widths were set to 1.25µm. let's take the example when V_T and t_{ox} are varied 30%, the control voltage is 1 volt, as the PMOS width is high, the output of the process variations sensor will drop considerably to 0.789 mV, this creates an average frequency of 4.1 GHz, to keep this frequency as invariant as possible to process variations, β will vary $\pm 83\ mV$.

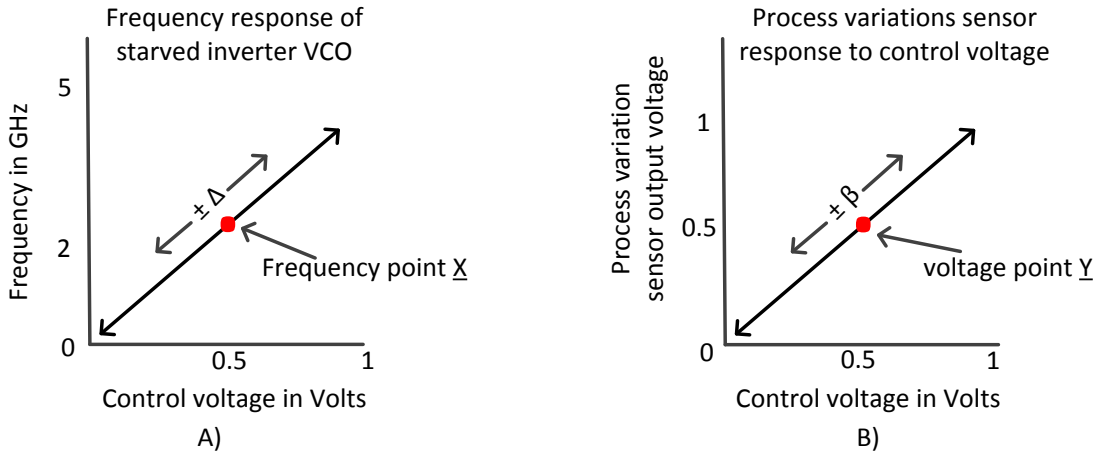


Figure 7-0-10

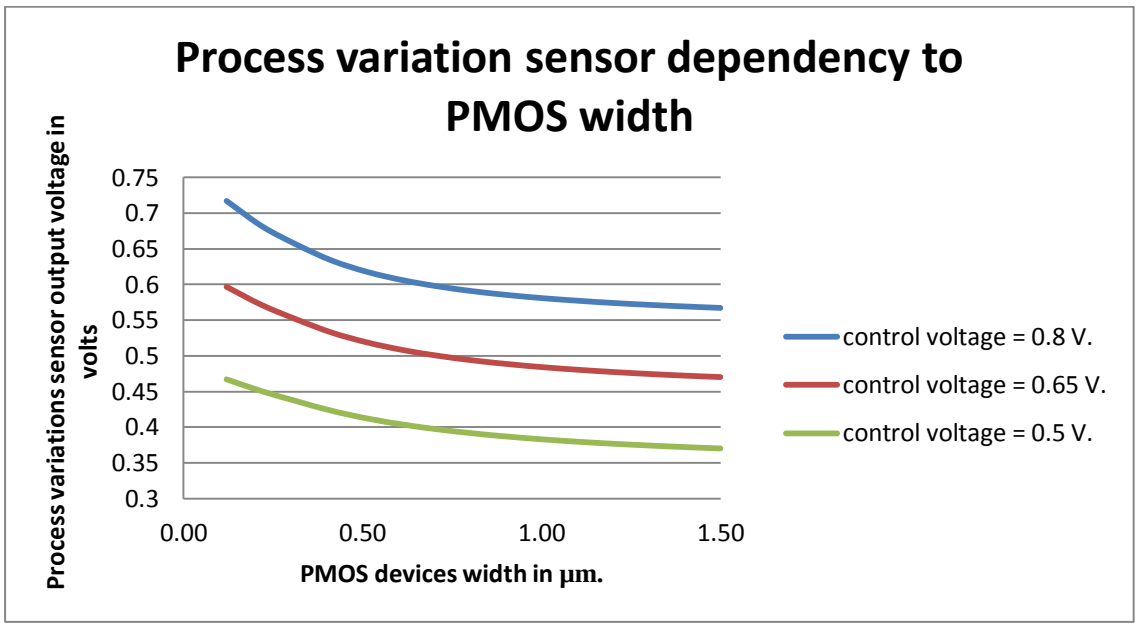


Figure 7-0-11:

It has been shown that method 1 shows improvements, on the other hand is difficult to implement and suffers from huge limitations as the VCO frequency performance is dependent on the width of the PMOS devices that are used in the process variations sensor, because of the widths we can summarize two important facts.

1. As the width is increased the sensor loses sensitivity (figure 7.5), this loss of sensitivity is small but it is desirable to achieve the highest possible sensitivity and this is done with the minimum possible width which is 120 nm.
2. As the width of the PMOS is increased, the output voltage of the process variations sensor decreases, figure 7.11, this is not good, referring again to figure 7.11, in terms of output voltage, if we establish a control voltage of 1 volt, ideally we need a process variations sensor output of 1 volt, with the corresponding β variation, in simple words, figure 7.11 is a major problem, this is also shown in table 7.5, where it can be seen that for a control voltage of 1, we obtain an average voltage of 0.789 volts.

From these two facts it is clear that we need the width of the PMOS devices to be always the minimum, 120nm.

7.1.3 DIFFERENTIAL AMPLIFIER UNAFFECTED BY PROCESS VARIATIONS

Once that the process variations can be sense, this information can be adjusted to the VCO performance characteristics, this way the limitations that were described in the previous method can be overcome, the solution that is presented here is a differential amplifier that can be adjusted to meet different VCO frequency tuning characteristics by simply choosing the correct MOS ratio between width and length. The major challenge in this part was to design a differential amplifier whose performance is affected as less as possible by process variations, with this method extra circuitry is required but the widths of the PMOS devices on the process variations sensor can be kept to the minimum 120nm.

7.1.3.1 TOTAL NMOS DIFFERENTAIL AMPLIFIER

This differential amplifier performance is unaffected by process variations; the schematic to this design can be seen of figure 7.12, is nothing more than a simple differential amplifier but the unique fact about it, is that is design only with NMOS, by using only NMOS and the appropriate W/L ratio sizes, process variations cause almost no effect on the system performance, transistors M_6, M_7 and M_8 are the key elements of this design. The idea of this system is exactly the same as the explained previously; an example of the performance of this design can be seen in figure 7.3, this figure shows a DC analysis of the differential amplifier when the input voltage that is applied to device M_4 is varied from 0 to 1 volt, from this figure it can be described two important facts of this design:

1. The output voltage of the differential op amp (process variation aware control voltage) can achieve a minimum voltage of 0.5 volts, this is due to the special configuration of transistors M_6 and M_7 and M_8 , whose bulk is connected to V_{DD}, this creates the first limitation for this system, the control voltage can never be less than 0.5 volts.
2. With the width manipulation of every transistor different performances can be achieved, as an example figure 7-13 shows two different cases when the devices M_1 to M_3 have different widths values, therefore different drain currents.

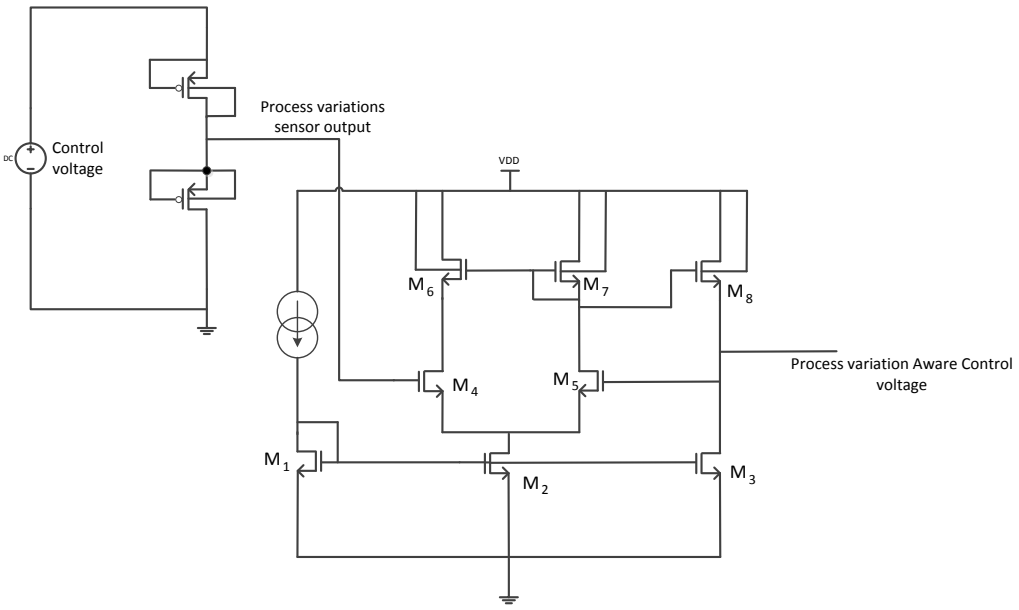


Figure 7-0-12: process variations sensor connected to the differential amplifier

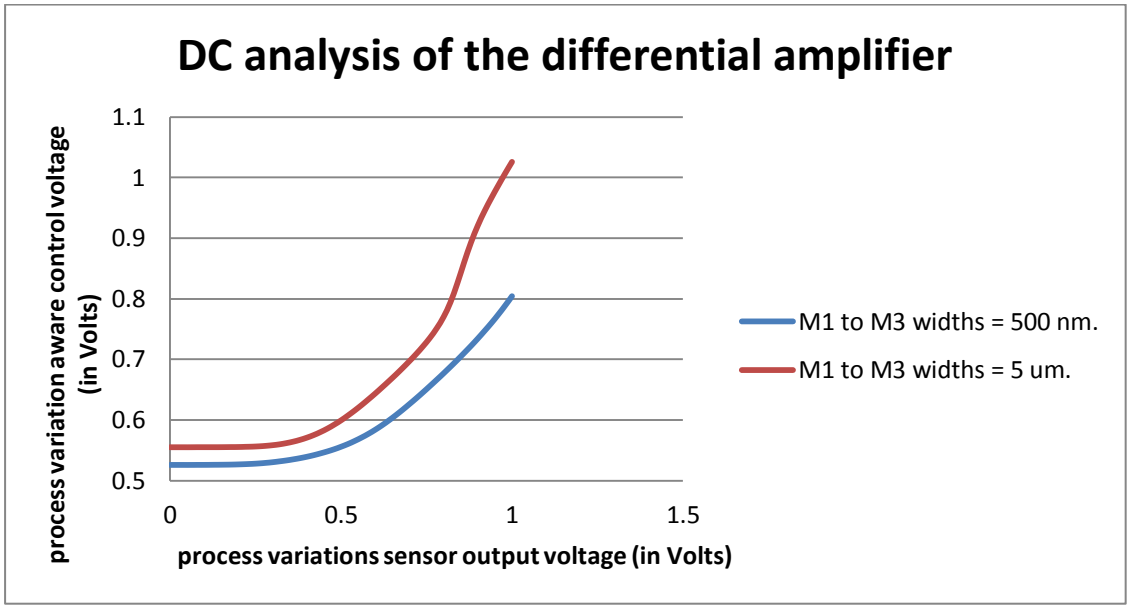


Figure 7-0-13

Figure 7-14 shows the fact that this differential amplifier performance is not affected by process variations, in this graph it can be seen a DC analysis at the 4 process corner cases, there is almost no difference in performance.

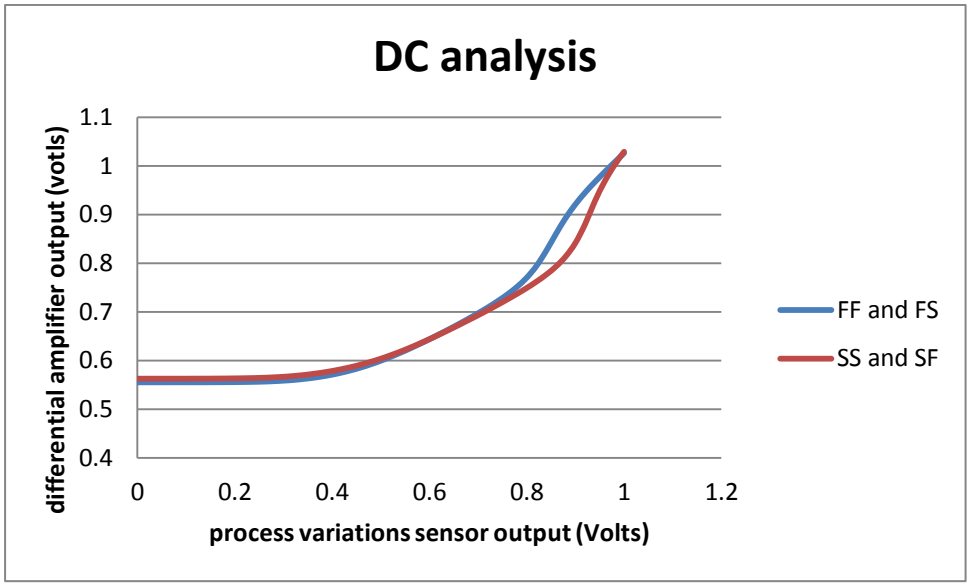


Figure 7-0-14: DC analysis showing that the differential amplifier is unaffected by process variations

As this is a differential amplifier by varying the W/L ratio of the input transistors M_4 to M_5, the gain of the amplifier can be adjusted, this can be seen in figure 7-15, where the width of transistor M_5 is kept constant at 500 nm, the width W of M_4 is varied, the length of both devices are kept constant at 90 nm, it can be observed that as the W/L ratio of M_4 gets higher, the gain of the amplifier increases.

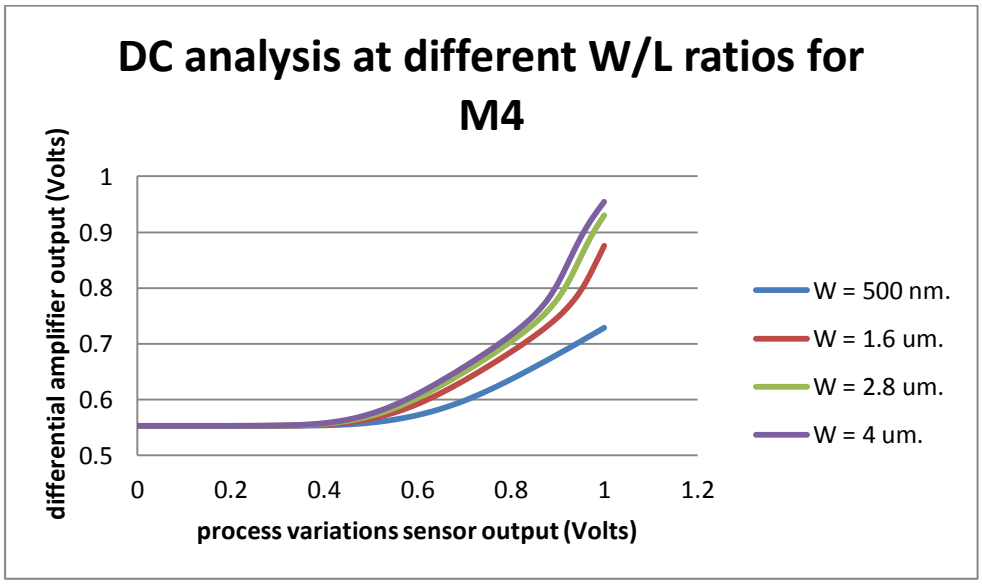
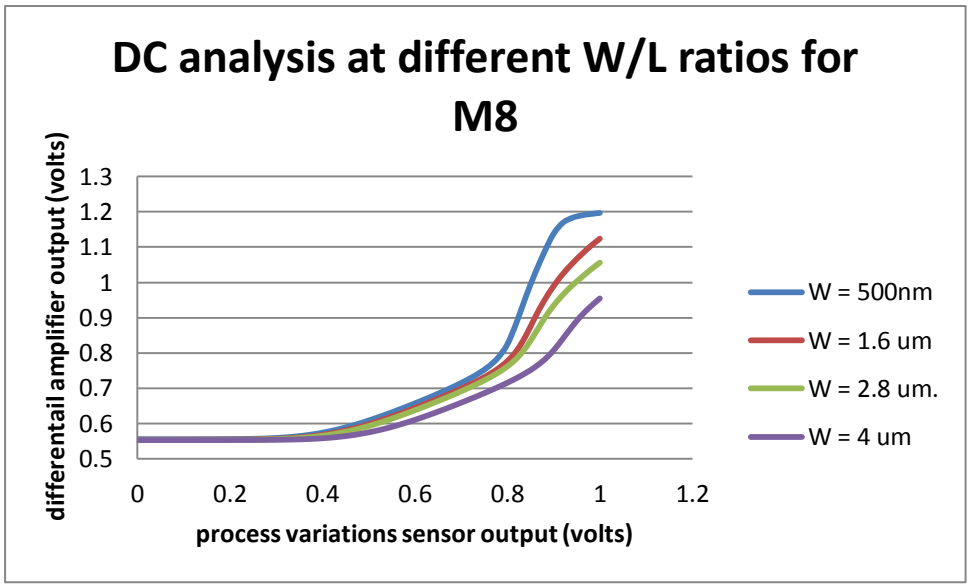


Figure 7-0-15

Another way to control the gain of the differential amplifier is by varying the W/L ratio of transistor M_8 as the width is decreased the gain of the amplifier is reduced.



In table 7.6 it can be seen the results when this design was tested with the inverter design (starved current), it shows less improvement that the previous case when the process variations sensor was connected directly to the device, still results are 2% better than in chapter 6 (table 6.9) when the VCO doesn't have any method of improvement, it is obvious that this design needs future work to obtain a better improvement.

Table 7-0-6: starved current results when the process variations sensor is combined with the differential amplifier

Oxide thickness and threshold voltage variations	5%	10%	20%	30%
Frequency variations in percentage	± 4.3 %	± 6.4%	± 8.3%	± 20%
Mean Frequency in GHz	3.9	3.68	3.73	3.6

7.2 INCREASE CURRENT

This is the most successful method for reducing the VCO performance degradation due to process variation, this method simply consists in adding more and larger currents to the VCO. For ring oscillators the equation below is the most important, this equation states the oscillator frequency is proportional to the drain current I_D of a delay cell, where N is the number of delay cells.

$$f_o = \frac{I_D}{N \times C_{TOT} \times V_{DD}}$$

Where C_{TOT} is highly dependent on C_{ox} of each device, and as the equation below states C_{ox} is highly dependent on the gate oxide thickness t_{ox}

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

If the drain current I_D is made higher the parameter C_{TOT} becomes less important in the equation above, therefore the VCO frequency degradation due to the process variation t_{ox} can be reduce.

This method was tested with the symmetric VCO, in figure 7.16 it can be seen the modifications that were made to each cell, and currents of $250\ \mu Amps$ where input to each cell.

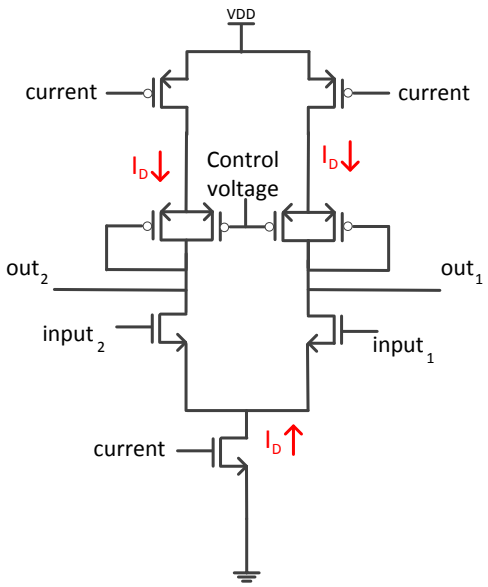


Figure 7-16: schematic of symmetric cell when multiple currents are applied

Table 7-7: symmetric VCO under process variation but when multiple currents are applied to each cell.

Oxide thickness and threshold voltage variations	5%	10%	20%	30%
Frequency variations in percentage	± 2 %	± 4%	± 6.5%	± 14.5%
Mean Frequency in GHz	4.9	4.5	4.8	4.6

The table above, table 7.7, shows the results of this method, in a 90 nm symmetric load design, the frequency variations is only $\pm 14.5\ \%$ when t_{ox} and V_t are varied 30%, this are the best achieved results, and the VCO is still oscillating at a very high frequency of 4.6 GHz.

8. REVIEW AND CONCLUSION

In this project 4 different VCOs have been design, each one of these designs has an appropriate performance for implementation on a PLL system of a USB 3.0, achieving a frequency of 5 GHz and with a low noise performance, each of these designs was investigated under process variations and one technique was developed for achieving the aim of creating a VCO that is aware of process variations.

Before any work was developed it was necessary the understanding of different VCO design possibilities and the advantages and disadvantages that each one of them was offering, apart from this, the project also required the investigation of process variations as one the aims of the projects was the investigation under different process variations.

The behaviour of 3 different ring oscillators under 3 different technologies was investigated (350, 180 and 90 nm), each one of these was design using the software Cadence Virtuoso Design Suite, noise analysis was performed in all of them, it was required to learn to produce these analysis, this was done with [14] and [15].

Technology 350 nm was discarded as it was producing very low frequencies, still the design files are attached to the project, in this thesis the performance of the 3 different ring oscillators is shown for technologies 180 and 90 nm, all of these designs achieve an appropriate frequency tuning range and an appropriate phase noise. Once the designs were functioning correctly the investigation of the effects that process variations would cause on them was investigated, corner cases were analyse where in each of the 4 corner cases a phase noise analysis was carried out as well as it was required to observe not only how process variations would affect the performance of frequency but the performance in noise as well, it was found that even in worst cases, the noise is still low.

More investigation was carried out when the ring oscillators were tested under power supply and temperature variations, observing the degradation that these parameters can cause to the system performance.

But as corner cases investigation is not sufficient when it comes to process variations, monte carlo simulation files were created with the appropriate manipulation of the technology files, this way the effects of random process variations were properly investigated, the results show a high degradation of the VCO operating frequency due to process variations, it was found that the design using symmetric loads was the most unaffected by process variations, where the other two (starved current or inverter and triode load) were affected on the same degree.

A VCO capable of producing an oscillation signal with an LC tank was design, but as problems were encountered with the technology files it was not possible a full investigation of this design under process variations, but it was observe how dependent this design is on the inductance, must be mentioned the extremely low phase noise that this design has.

All the previous tasks were part of the investigation area in this project, the next steps were followed to achieve the main aim of this project, a VCO that is aware of process variations, for this aim a PMOS diode capable of sensing the variations that could happen in the gate oxide thickness and threshold voltage was design, this supported two possible solution but unfortunately both of this solutions suffered from some limitations.

The first solution consisted in the direct connection of the PMOS diode to the VCO, this the PMOS diode, varies the control voltage depending on the variation of parameters t_{ox} and V_t, and as the VCO frequency is highly dependent on the control voltage a less affected VCO to process variations was achieved, this technique could only be tested on the starved current design, the results show a 4% improvement comparing them without this technique, however this technique suffered from the fact that everything was dependent on the PMOS width, therefore this causes some limitations and it was found that the best thing would be to always leave the PMOS width to as minimum as possible.

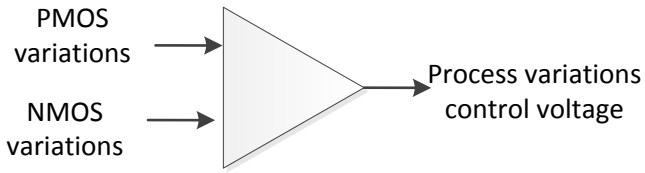
The second solution overcomes the problem of the PMOS width dependency, with this technique the PMOS width can always be on the minimum, and with the special configuration of a differential amplifier a more adaptive technique can be produce, still this solution was not properly completed and tested but it shows a good background for future work.

Finally, a very rudimentary solution was carried out, even though that it was rudimentary this solution showed the best results when it comes to a VCO that is unaffected by process variations, this solution was based on the increment on the number of currents being applied to the VCO, therefore increasing the power consumption, this solution was tested with the symmetric load design achieving a frequency variation of only $\pm 14.5\ \%$ at 4.6 GHz when t_{ox} and V_t are varied up to 30% in the monte carlo simulations.

9. Future work

From the presented solutions in chapter 7 to create a process variation aware VCO, the most promising one is the method that uses the process variations sensor to adapt the control voltage depending on the variations of t_{ox} and V_t, this method has shown huge limitations and it is clear that it has not been completely implemented, as future work I believe that the main path to follow is the improvement of this method as it has shown small improvements in the area of process variation aware VCO, the next points should be follow for this:

1. In the solutions presented only the PMOS variations was taken into account, and as every VCO design requires NMOS and PMOS is obvious that it is required to have into account the process variations that can occur to NMOS devices, therefore for an improvement it would be require to sense the NMOS variations as well, figure xxx illustrates this idea.



2. It would be require to reduce the limitations that the special differential amplifier creates, specially the limitation of only being capable of producing a minimum output voltage of 0.5 Volts.

More future work that could be develop involves the LC tank, as there was problems with the appropriate simulation of this design, it would be good to know exact data about the process variations effects on this design

Another fact is the VCO dependency to temperature variations, this has been shown in all the presented designs, the PMOS diode is sensitive as well to temperature variations, with the appropriate configuration of a system maybe the VCO dependency to temperature could be reduce as well.

A layout of every VCO could be carried out, this way the parasitic capacitances could be extracted, and a more accurate simulation could be performed.

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APPENDIX A 180 NM

	inverter			
	180 nm			
Corner case	SS	SF	FS	FF
Frequency range	2.8 – 0.2GHz	4.2 – 0.5GHz	4.4 – 0.35GHz	5.2 – 0.67GHz
Voltage range	0.6 – 2 Volts	0.6 – 2 Volts	0.6 – 2 Volts	0.6 – 2 Volts
current	50 µA	50 µA	50 µA	50 µA
Supply voltage	1.2 Volts	1.2 Volts	1.2 Volts	1.2 Volts
Jcc	512 fsec. @ 2.4GHz	210 fsec. @ 3.9GHz	256 fsec. @ 4.2GHz	168 fsec. @ 5GHz
Phase noise @ 100KHz offset	-58 dBc	-51 dBc	-37	-36 dBc
Phase noise @ 100MHz offset	-118 dBc	-110 dBc	-97	-121 dBc
transistors	12	12	12	12

	Triode			
	180 nm			
Corner case	SS	SF	FS	FF
Frequency range	2.3 – 0.3GHz	5.9 – 0.2GHz	4.1 – 0.8GHz	9.3 – 0.4GHz
Voltage range	0 – 0.4 Volts	0 – 0.66 Volts	0 – 0.55 Volts	0 – 0.77 Volts
current	150 µA	150 µA	150 µA	150 µA
Supply voltage	1.2 Volts	1.2 Volts	1.2 Volts	1.2 Volts
Jcc	434 fsec. @ 2.2GHz	374 fsec. @ 4.1GHz	311 fsec. @ 4.1GHz	234 fsec. @ 9.3GHz
Phase noise @ 100KHz offset	-45 dBc	-24 dBc	-35 dBc	-30 dBc
Phase noise @ 100MHz offset	-105 dBc	-108 dBc	-117 dBc	-100 dBc
transistors	26	26	26	26

	symmetric			
	180 nm			
Corner case	SS	SF	FS	FF
Frequency range	2.5 – 0.57GHz	4.89 – 1.5GHz	4.1 – 0.8GHz	9.3 – 6.3GHz
Voltage range	0 – 0.35 Volts	0 – 0.5Volts	0 – 0.55 Volts	0 – 0.55 Volts
current	150 µA	150 µA	150 µA	150 µA
Supply voltage	1.2 Volts	1.2 Volts	1.2 Volts	1.2 Volts
Jcc	494 fsec. @ 2.2GHz	293 fsec. @ 4.9GHz	277 fsec. @ 4.1GHz	169 fsec. @ 9GHz
Phase noise @ 100KHz offset	-44 dBc	-39 dBc	-38 dBc	-35 dBc
Phase noise @ 100MHz offset	-122 dBc	-115 dBc	-118 dBc	-110 dBc
transistors	26	26	26	26