Abstract

With the trend that people rely on integrated devices, such as mobiles and computers, low power consumption has become a paramount requirement in recent years. Reducing the supply voltage to sub-threshold region is one of the effective methods to combat low energy dissipation as dynamic power reducing quadratically will supply voltage V_{DD}. However, how to make the device work under sub-threshold region must be figured out and the critical parameters influencing the reliability of the circuit need to be studied.

In order to achieve ultra low power at sub-threshold operation, we did a lot of research on sub-threshold technology and took static random access memory (SRAM) as the first case to study. This thesis is mainly separated into three parts. The first part is the introduction of sub-threshold technology including the previous works on sub-threshold design challenge, the previous sub-threshold SRAM design, and the method of analyzing stability. How to combat the challenge for designing a sub-threshold SRAM system and details of each part of the sub-threshold SRAM design will be introduced in the following chapter. Finally, reliability analysis of static noise margin (SNM) will be carried out to find out critical parameters having an impact on the stability of the SRAM cell.

The main contribution of this thesis project is that we fulfilled two sub-threshold SRAM designs, summarized and analysed the reliability of the sub-threshold design.

Key words---- SRAM, sub-threshold, reliability, static noise margin (SNM)

Declaration

A dissertation is submitted to the University of Bristol in accordance with the requirements of the degree of Master of Science in the Faculty of Engineering. It has not been submitted for any other degree or diploma of any examining body. Except where specifically acknowledged, it is all the work of the Author.

Zhang Yue, September 2012

Contents

List of Figures

List of Tables

List of Abbreviations

ABB	Adaptive Body Biasing
BL & BLB	Bitline & Bitline Bar- the true and the complementary input/output lines of a column of SRAM cells
BTI	Bias Temperature Instability
CMOS	Complementary Metal-Oxide-Semiconductor
CR	Cell Ratio
DRV	Data Retention Voltage
HCI	Hot-Carrier Injection
HP	High Performance
IWL-VC	Improved Word-line Voltage Control
LP	Low Power
M-C	Monte-Carlo
MOSFET	Metal-Oxide-Silicon Field-Effect Transistor
NM	Noise Margin
NMOS & PMOS	N-type Metal-Oxide-Semiconductor & P-type Metal-Oxide-Semiconductor
OUT	Output Signal
OUTB	Opposite Output Signal
PC	Pre-charge
PP	PMOS Pass-transistor
PR	Pullup Ratio
PTMs	Predictive Technology Models
PVT	Process, Voltage, Temperature - a set of conditions affecting the circuit

Q	The point named Q
QB	The opposite point named QB
RAM	Random Access Memory
RBL	Read Bitline
RDF	Random Dopant Fluctuations
RE	Read Enable Signal
ROM	Read Only Memory
RWL	Read Word Line
SA	Sense Amplifier
SAE	Sense Amplifier Enable Signal
SL	Select Line
SNM	Static Noise Margin
SRAM	Static Random Access Memory
Sub-V_{TH}	Sub-threshold Voltage
SVT	Standard V_{TH}
TDDB	Time-Dependent Dielectric Breakdown
ULP	Ultra-Low-Power
VCVS	Voltage Controlled Voltage Sources
WE	Write Enable Signal
WL	Word Line
WWL	Write Word Line
6T or 8T	Six Transistors or Eight Transistors

1. Introduction

1.1 Aims and Objectives

Current trends show that minimizing power consumption is a paramount requirement in the design of integrated circuits (Keller et al. 2011). Power consumption has become a principle design consideration as device sizes decrease and many more devices can be synthesized on a single chip (Calhoun 2002). Many emerging embedded applications require extremely low power compromising real-time performance. These low power devices are generally designed using sub-threshold based design techniques. Such techniques have proven to be useful for ultra-low-power (ULP) and low-energy applications since dynamic energy consumption is reduced exponentially with supply voltage V_{DD} and the minimum energy operation usually occurs in the sub-threshold region (Calhoun et al. 2009).

However, a major challenge in the ultra low power design of circuits, particularly in memory based circuits and systems, is reliable sub-threshold design. This is because low threshold voltage and aggressive technology scaling exacerbate the reliability. Hence, more research is required to evaluate the reliability of sub-threshold circuits and systems. This work will investigate the design and reliability analysis of a sub-threshold memory system. HSPICE simulations will be carried out on various memory circuits to find out critical parameters that affect the circuit reliability. The aim will be to design sub-threshold memory systems, find out critical charges at various threshold voltages and the critical parameters that affect the circuit reliability. Besides, MATLAB will also be used to analyse critical data.

In order to investigate the reliability of a sub-threshold memory system, the background of sub-threshold technology and recent advances are discussed firstly. Then the SRAM sub-threshold design and reliability analysis are stated. Finally, the progress of future work is outlined.

1.2 Reliability of Electronic System

Reliability consists of the availability, capability and safety of a device and is thus an essential component of good product evaluation criteria. The goal of reliability analysis is to evaluate the inherent reliability of a device, find the critical characteristics which influence reliability, and pinpoint potential areas for reliability improvement. After targetable reliability analysis, appropriate actions will be taken to mitigate the effects of those failures. In order to better carry out further research work, we must figure out the importance of reliability first.

Take SRAM as an example, we use it as a significant part of the computer. Lack of

reliability will reflect on circuit instability and design life decrease, which will cause not only extra costs but also reputation problems. There are a number of reasons why reliability is an important product attribute, including:

- Customer Satisfaction. If the device has instability in the performance or has less design life than customers expected, customers will be unsatisfied and may not buy products of this brand again. While a reliable product may not dramatically affect customer satisfaction in a positive manner, an unreliable product will negatively affect customer satisfaction severely. Thus high reliability is a mandatory requirement for customer satisfaction and expectation.

- Repeat Business. Losing the customer's satisfaction and trust, the manufacturer will lose the repeat business at the same time. In order to get repeat business from customers, improving the reliability of products will be the most significant for the manufacturer. And this type of attitude has a positive impact on future business.

- Reputation. Customer satisfaction crisis will cause a loss of company reputation. A company's reputation is the most important method to sell products, which is very closely related to the reliability of its products. The more reliable a product is, the more likely the company will have a favorable reputation.

- Warranty Costs. If a product fails to perform its function within the warranty period, the replacement and repair costs will be additional expenses except production costs, as well as gain unwanted negative attention. The negative effect on profits will be very large.

- Competitive Advantage. Many companies will publish their predicted reliability numbers to help gain an advantage over their competitors who either do not publish their numbers or have lower numbers. Increasing reliability will be the strategy for victory.

From reading papers, we understand the importance of reliability firstly, and furthermore we adopt the unstable factors in the CMOS circuit from different perspectives. And more importantly, these will contribute to our further research on reliability analysis and searching the critical parameters that influence circuit stability and reliability.

1.3 Ultra Low Power (ULP) Design Using Sub-threshold Technology

From reading the papers (Calhoun et al. 2006), (Calhoun et al. 2009), (Keller et al. 2011) etc. corresponding to energy consumption of a circuit, we will always find that designers are expected to explore approaches for the lowest possible power consumption, which is well known as ultra low power (ULP). To combat power consumption issues, lower voltage is expected to be used in devices. Both the static and dynamic power are reduced quadratically as the supply voltage V_{dd} is reduced.

And the relationship between supply voltage and dynamic power dissipation can be seen in equation (1.1) (Wang 2010).

$$P_{dyn} \propto f_{0\to1} \cdot V_{DD}^2 \cdot C_L \tag{1.1}$$

Where, $f_{0\to1}$ represents the frequency of energy consuming transitions, V_{DD} is the supply voltage, and C_L is the load capacitance.

The ultra-low-power performance can be achieved by reducing V_{DD} to sub-threshold region, as V_{DD} has a quadratic effect. And sub-threshold operation as the potential technology for large energy savings is being examined and used in ULP design (Jorgenson 2010).As Keller et al. (2011) mentioned, the minimum-energy operating point generally occurs near the sub-threshold voltage. Low voltage operation can markedly reduce the energy consumption of the circuit. And before we do the research on sub-threshold technology, it is necessary to introduce the thresholding technology. Thresholding is a method of separating objects from the background by selecting an interval (usually in pixel intensity) and setting any points within the interval to 1 and points outside the interval to 0" (Whitaker & Dorf 2005). Sub-threshold voltage is lower than the threshold voltage, and the details of sub-threshold technology will be introduced in chapter two.

1.4 Static Random Access Memory (SRAM)

Memory device, as an essential part of any computation system, can be categorized into read only memory (ROM) and random access memory (RAM) as introduced by Fig.1.1. Static random access memory (SRAM) is named according to storage characteristics of RAM and does not need to be refreshed periodically (Whitaker & Dorf 2005). And the so-called "static" refers to memory that can maintain and constantly store the data as long as this remains energized. However, the stored data will disappear when the power supply is stopped. SRAM is widely used in the digital world because of its faster, low power requirement and easy to control characteristics. We take SRAM as a first case to study in this project. And the details of read and write operation will be introduced later.

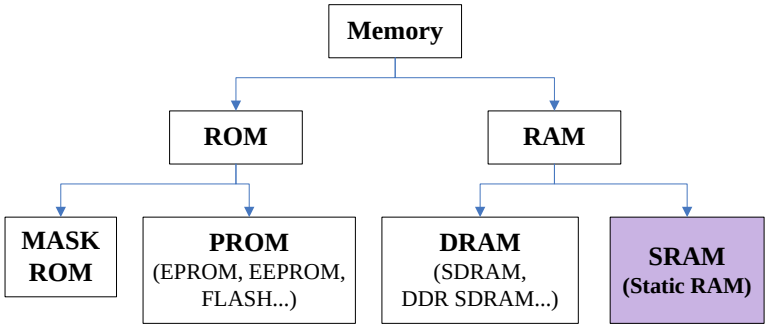


Figure 1.1 Simplified Classification of Memory Unit

The current advance of SRAM has presented the six transistors (6T), eight transistors (8T) and even twelve transistors (12T), and the 6T SRAM cell is commonly used. However, when we use a low voltage operation for traditional 6T SRAM to get lower leakage power and active energy, there exists some limitations. Numerous articles, e.g. (Calhoun et al. 2007), (Kim et al. 2008) etc., have mentioned that using 8T & 10T SRAM can lift these restrictions, which will be presented and discussed in the sub-threshold SRAM section.

1.5 Sub-threshold Design of SRAMs

To reduce energy consumption, numerous researchers focus on sub-threshold technology and explore the limitation and potential of sub-threshold design of SRAMs. What has been examined is that the low voltage operation can indeed realize the energy saving and stability.

SRAMs comprise a significant percentage of the total power for many digital chips. Besides, SRAMs leakage can dominate total chip leakage. Furthermore, SRAMs with lower V_{DD} can reduce leakage power and access energy. Therefore, for system integration, SRAM must become capable of operating at sub-threshold voltage that is compatible with sub-threshold combinational logic (Calhoun et al. 2007). To overcome the difficulties of operating an SRAM in sub-threshold requires both circuit and architectural innovations. Considering the critical parameters affecting the stability of SRAM circuits, such as noise margin and device scale, the new detecting method and innovative SRAM are proposed and will be introduced in detail later.

2. Sub-threshold technology

This chapter is about sub-threshold technology and is divided into five parts. Firstly, the sub-threshold technology will be introduced, and the following parts will correspond to the circuit parameters affecting the sub-threshold circuit. The recent advance and the future challenge of sub-threshold design will be presented later. Finally, the motivation of the proposal research will be expounded.

2.1 Sub-threshold Design

It has been discussed by Calhoun and Khanna (2009) and Kim (2011) that the operation of digital CMOS transistors using sub-threshold technology is the principal method to reduce energy consumption. To learn the sub-threshold technology well, we have read the book *Design of Analog CMOS Integrated Circuit* (Razavi 2011) which introduces the sub-threshold technology clearly.

As the book mentioned (Razavi 2011), when we analyse the MOSFET, we have assumed that the device turns off abruptly as V_{GS} drops below V_{th}. But for $V_{GS} \approx V_{TH}$, some current flows from D to S still exists in reality. Even for $V_{GS} < V_{TH}$, I_D is not infinitely small, but it exhibits an exponential relationship with V_{GS}. We call it "Subthreshold conduction". The region where V_{GS} is higher than the threshold voltage region is known as a strong inversion layer. And the area below the threshold voltage is known as the sub-threshold or weak inversion layer.

For V_{DS} greater than roughly 200mV, its formula can be represented as:

$$I_D = I_0 \exp \frac{V_{GS}}{\text{ב} V_T} \tag{2.1}$$

Where $\text{ב} > 1$ is a no ideality factor. From this formula, we have seen that as V_{GS} falls below V_{TH}, the drain current drops at a finite rate. With typical values of ב and temperature, V_{GS} must decrease by approximately 80mV for I_D to decrease by one decade (Fig. 2.1).

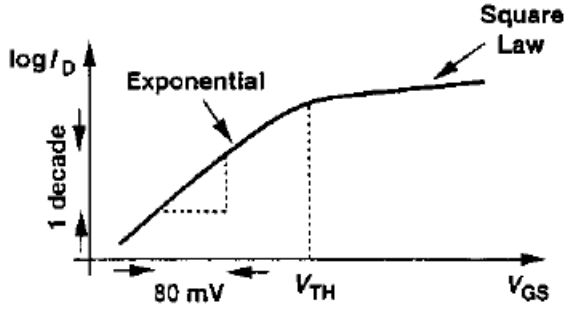


Figure 2.1 MOS sub-threshold characteristics (Razavi 2011)

We can see that using sub-threshold technology in MOS devices can achieve a higher gain, which the exponential dependence of I_D upon V_{GS} in sub-threshold operation suggests. However in order to meet this condition, only a large device width or low drain current happens. And this will be one of the challenges when we try to realize scaling device.

2.2 Circuit Parameters Affecting Sub-threshold Design

Reliability issues of the memory system cannot be ignored. And to find out critical parameters those affecting the circuit reliability will be the first task. From reading the papers introduced below, we studied and summarized the reliability factors including the following:

2.2.1 The Conflict between Low Power and Reliability.

In the digital world, low power (LP) device is an urgent need, and low voltage operation can markedly reduce the energy requirements of digital circuits. But it also causes reliability and yield to greatly reduce (Keller et al. 2011). To maintain LP and reliable stability of the circuit, device dimensions, adaptive body biasing (ABB) and the cost of potentially increasing energy per operation must be considered.

Keller and Bhargav (2011) present a new method for digital CMOS library characterization and a new algorithm for finding the minimum energy operating point of digital CMOS circuits; with precise guarantees on reliability and parametric yield and gate sizing with a guaranteed minimum static noise margin (SNM) for any circuit. From reading this paper, we know that in order to guarantee the reliability of a design, intra-die variation and statistical noise margin data must be considered. After collecting statistical noise margin data and considering total energy per operation, they proposed the search algorithm and the reliable–circuit minimum energy algorithm results for 1M inverter test circuit are shown in Fig. 2.2. P (L, W) and N (L, W) mean PMOS/NMOS sized with length and width. E_{tot} is the total energy per operation in a digital circuit. This figure shows each energy operating point status with P (L, W) and N (L, W) given for each point in nanometers.

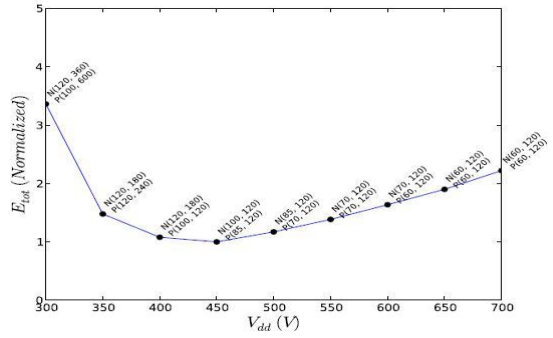


Figure 2.2 Results of the reliable-circuit minimum energy algorithm applied to test circuit (Keller 2011)

Random variation and minimized energy are important components when we research into CMOS circuit reliability. Calhoun and Khanna (2009) also give us the strategies to combat random variation and minimize energy for nodes below 45nm. In this paper, they refine predictive technology models (PTMs) to capture the scaling trends of low-power CMOS technologies and their effect on sub-threshold circuits. They find that there is a net improvement in minimum energy with scaling in the LP technologies. Although I_{off} is increasing with scaling, the improvement in delay results in a net improvement in energy. Variation fundamentally limits logic noise margin (NM) and SRAM data retention voltage (DRV). V_{DD} and L knobs for minimum energy become more useful in scaled technologies generally, but targeted application of voltage knobs to specific circuit contexts are also necessary for maintaining sub-V_T functionality (Calhoun et al. 2009).

2.2.2 Static Noise Margin

From reading the papers, we realized that numerous researchers focus on noise issues. Noise trades with power dissipation, speed, and linearity make it be concerned as circuit parameters when dealing with analog and digital circuit (Razavi 2001).

Keller, S., the author of the paper *Reliable Minimum Energy CMOS Circuit Design*, commits to mitigating the effect of lower voltage operation on reliability and yield of the circuit. He mentioned that he uses quantification and modeling method to calculate the energy per operation of a digital circuit. Besides, quantification of the variation-induced device failure rate is a considerably new issue that requires the use of noise margin. He use static noise margins (SNMs) to analyse memory cells and address the functional yield problem in sub-threshold circuit. The noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'. And the SNM, as the name suggests, corresponds to a static form of analysis.

In their research, SNM is calculated by way of a DC sweep and is independent of output load. Given any two gates G_X, G_Y (Keller et al. 2011), where G_X is driving G_Y, the SNM is defined as:

$$NM_H = V_{OH}(G_X) - V_{IH}(G_Y) \quad (2.2)$$

$$NM_L = V_{IL}(G_Y) - V_{OL}(G_X) \quad (2.3)$$

$$SNM = \min\ (N\,M_H, N\,M_L) \quad (2.4)$$

Keller (2011) also mentioned noise margin in sub-threshold logic circuits when they examined the impact of technology scaling to 22nm on sub-threshold circuit design. To investigate the scaling of LP processes, they incorporated variability into the models, such as local V_{TH} variation due to random dopant fluctuations (RDF). For a large circuit, parameters like delay and leakage current are less affected by RDF. However, due to inadequate SNM, RDF threatens the basic functionality of the circuit. So, in their research, they characterize the SNM for logic gates.

2.2.3 Potential Parameters Affecting the Circuit Reliability.

Introducing reliability analysis is an important step in taking corrective action, ultimately leading to a product that is more reliable. Li and Qin (2006) used a simple SRAM circuit, 1-bit six-transistor cell with a commercial 0.25-μm technology, as an example to demonstrate how to apply SPICE to circuit reliability modeling, simulation, analysis, and design. According to the paper, there are two potential parameters which affect the reliability of the SRAM system:

A. Hot-carrier injection (HCI).

The main effects of HCI on the device electrical characteristics are threshold-voltage drift and transconductance (gm) degradation. They use SPICE simulation to prove that pass transistors in an SRAM cell receive more severe damages because of bidirectional HCI stresses. As this paper mentioned, after SRAM circuit design and device lifetime calculation are prepared, the SRAM circuit with HCI-induced ΔR_d elements was simulated at different stress times to check its functionality. ΔR_d is only one parameter in HCI failure equivalent circuit model, and it characterizes drain current reduction due to mobility degradation resulting from HCI-induced interface charge and oxide charge. They made the conclusion that HCI had significant effects on SRAM-cell stability. Reliability design techniques for HCI including transistor sizing, gate topology transform, and input-signal scheduling are presented in *Hot-Carrier Reliability of MOS VLSI Circuits. Norwell*. (Leblebici & Kang 1993).

B. Time-dependent dielectric breakdown (TDDB).

As Li, X.J. etc. mentioned, there are four topologically distinct oxide breakdown locations in the SRAM cell shown in Fig. 2.3 store-to-stolen, store-to-V_{DD}, store-to-gnd, and gate-to-diffusion of pass transistors. Store-to-Stolen breakdown and gate-to-diffusion breakdown of pass transistors reduce the bias temperature instability (BTI) differential voltage and output swing; whereas breakdowns at Store-to-V_{DD} and Store-to-gnd increase the leakage current at the opposite transistors and degrade the cell stability and static noise margin (SNM). Most SRAM cells become unstable without sufficient SNM.

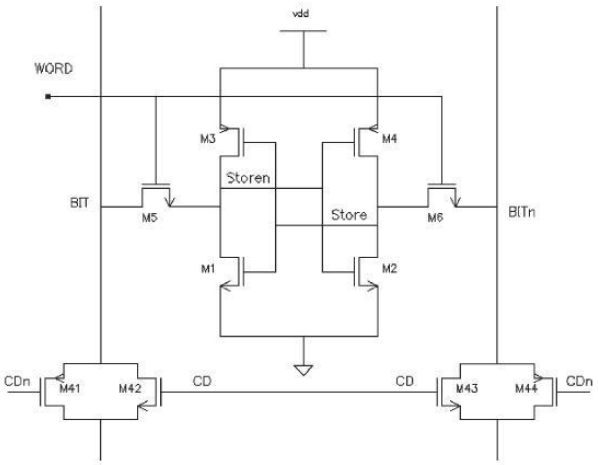


Figure 2.3 Store/Stolen represents the 6T SRAM cell state (Li et al. 2011).

In the paper (Li et al. 2011), they took the second step to simulate SRAM circuit reliability with inclusion of both TDDB and HCI failure equivalent circuit models. And the first step is to test HCI influence separately. The simulation proved that TDDB has the most deleterious effects on SRAM-cell stability.

2.3 Challenges in Sub-threshold Design of SRAMs

After reading the books, we have basic knowledge about MOSFET, SRAM and sub-threshold technology. Besides, the papers give us an overview about the current advance about sub-threshold SRAM design. However, the challenges in sub-threshold design of SRAMs still exist:

2.3.1 Stability of SRAM Cells

Researchers commit themselves to designing more reliable sub-threshold SRAM systems to adapt market demand for low power consumption. Although some new structures of SRAM have been present, researching the more stable and lower power consumption device will always be the significant challenge.

The sub-threshold technology has been proved in ultra-low-power applications. However, the noise margin decreases as the supply voltage is lowered. And the reliability of circuits is facing a challenge due to the issues associated with low voltage and ultra low voltage. The characteristic parameters affecting reliability still need to be found and examined.

2.3.2 Sense Amplifier Problems

The sense amplifier is the critical component in SRAM design. The speed and power dissipation of the whole SRAM design is extremely affected by the performance of

sense amplifier (Wang 2010). Therefore, trying to design the appropriate sense amplifier circuit will be one of the challenges in this project. And the details of examining various sense amplifier circuits will be introduced in chapter3.

2.3.3 Voltage Margin and On-off Current Ratio reduction of Sub-threshold SRAM Design

Both Calhoun (2009) and Kim (2008) have mentioned that facing the ultra low power sub-threshold SRAM design, reduced voltage margin, degraded on-off current ratios and heightened sensitivity to variations are extreme challenges. When we try to reduce voltage for power consumption reduction, the issues introduced above will exist and influence the stability of the circuit.

2.3.4 Reduced Number of Cells per Bitline

As Wang (2010) mentioned, the total number of cells per bitline will be reduced when the conventional SRAM cells are used in sub-threshold design. This is because the ratio between I_{read} (read current of accessed cell) and $I_{leakage}$ (leakage current of un-accessed cell) is reduced. The leakage current in one bitline is shown in Fig. 2.4 (Wang 2010). Besides, as Verma & Chandrakasan mentioned at most 64 cells could be attached to one bitline if no other technique was applied.

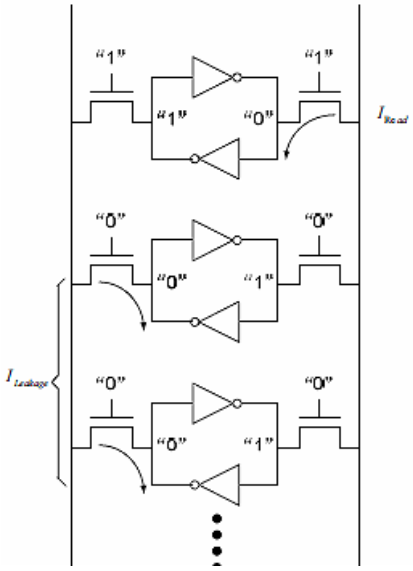


Figure 2.4 Leakage current in one bitline (Wang 2010)

However, in this project, we will focus on only one cell in the column and do research on designing and examining the reliability of a successful sub-threshold SRAM circuit. Other components in SRAM such as pre-charge (PC), write and read sequence generation circuits, etc., are also to be designed properly and these will be introduced

in detail in chapter3.

In conclusion, the design and analysis of sub-threshold SRAM for this project are facing great challenges.

2.4 Recent Advance in Sub-threshold Design of SRAMs

Memory, as the most important part in embedded applications, owns a large family including RAM, ROM, Cache and so on. Static random access memory (SRAM) is a type of semiconductor memory where the word static indicates that, unlike dynamic RAM (DRAM), it does not need to be periodically refreshed. SRAM uses bistable latching circuitry to store each bit. This project will investigate the reliability of a sub-threshold memory system, and SRAM cells will be the basic system to be studied.

2.4.1 The Basic Component in SRAM----NMOS and PMOS

The idea of metal-oxide-silicon field-effect transistors (MOSFETs) was patented by J.E. Lilienfeld in the early1930s, while it has been widely adopted in the digital world since complementary MOS (CMOS) devices were introduced in the mid-1960s. CMOS has the characteristics which can effectively reduce power consumption and fabrication cost as the book (Razavi, 2001) mentioned. Firstly, CMOS gates dissipated power only during switching and required very few devices; secondly, it was also discovered that the dimensions of MOS devices could be scaled down more easily than those of other types of transistors.

With the development of CMOS technologies, it came to dominate the analog world as well. As said above, CMOS devices could be scaled down. And device scaling also continued to improve the speed of MOSFETs. Like Professor Razavi (2001) said, the intrinsic speed of MOS transistors has increased by more than three orders of magnitude in the past 30 years. In this project, NMOS and PMOS will be the basic components in memory system.

A. NMOS

Fig. 2.5 shows the circuit symbols used to represent NMOS and PMOS transistors, which are the basic components to build inverter, word-line enable switch transistor and even to implement a buffer in 10T SRAM.

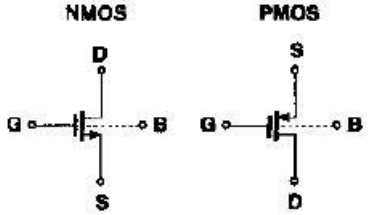


Figure 2.5 MOS symbols

Fig. 2.6 shows a simplified structure of an n-type MOS (NMOS) device. When

$V_{GS} > V_{TH}$ enough, carriers are attracted into the channel region to initiate conduction. The transistor is turned on, and a channel has been created which allows current to flow between the drain and the source. V_{TH} is threshold voltage, and influenced by body voltage drain voltage and channel length and so on. And when $V_{DS} \geq V_{GS} - V_{TH}$, the channel is cut off at the drain end. Further increases in V_{DS} have little effect on the current.

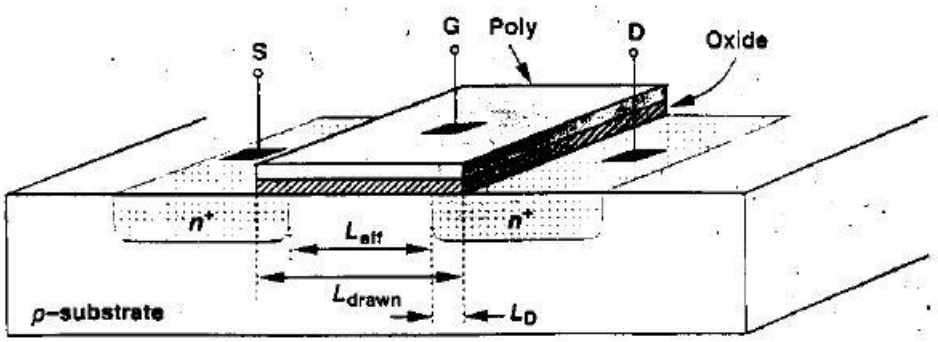


Figure 2.6 Structure of a NMOS device (Razavi 2001)

B. PMOS

P-type metal-oxide-semiconductor logic uses p-type metal-oxide-semiconductor field effect transistors (MOSFETs) to implement logic gates and other digital circuits. PMOS has opposite polarity with NMOS.

2.4.2 Sub-threshold 6T SRAM Design

As the book (Rabaey, Chandrakasan & Nikolic 2003) mentioned, the generic SRAM cell is introduced in Fig. 2.7. It **c**onsists of six transistors per bit. The word line (WL), which replaces the clock and controls the two pass transistors M_5 and M_6, enable access to the cell. Two bit line (BL) transferring both the stored signal and its inverse are required, which improves the noise margins during both read and write operations. The middle of this circuit, which is used as SR latch, structures two pair of inverters through $M_1 - M_4$.

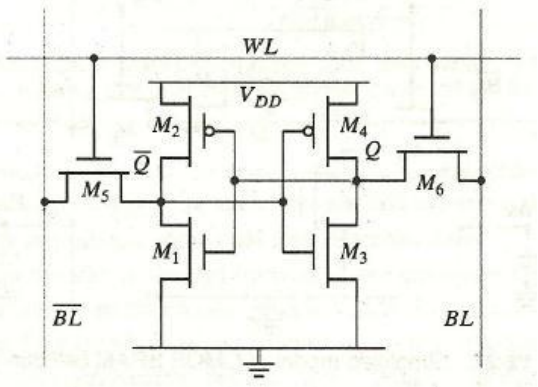


Figure 2.7 Six-transistor CMOS SRAM cell (Rabaey, Chandrakasan & Nikolic 2003)

A. Read Operation

The Electronics Handbook (Whitaker &Dorf 2005) defines the memory read and write operation as:

> *When an address is present to a memory device, and sometimes after a control signal is strobed, the information stored at the specified address is retrieved after a certain delay. This process is called a memory read. Similarly, data can be stored into the memory device by performing a memory write. When SRAM circuit is writing, data and an address are presented to the memory device with the activation of a write control signal.*

Assume that a 1 is stored at Q. Furthermore, both bit lines are precharged to 2.5V before the read operation is initiated. The read cycle is started by asserting the word line, enabling both pass transistors M_5 and M_6 after the initial word-line delay. Then the values stored in Q and Q' are transferred to the bit lines by leaving BL at its precharge value and by discharging BL' through $M_1 - M_5$. This is shown in Fig. 2.8.

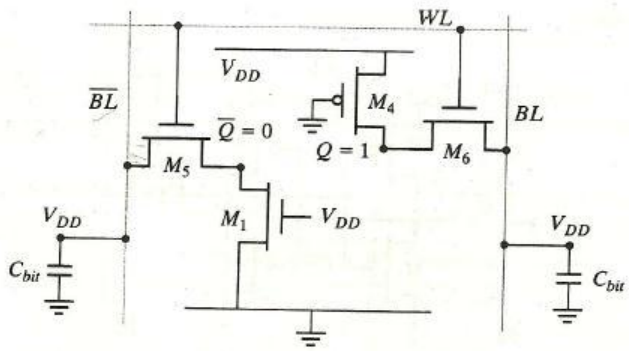


Figure 2.8 Simplified model of SRAM cell during read (Q=1, $V_{precharge} = V_{DD}$)
(Rabaey, Chandrakasan & Nikolic 2003)

B. Write Operation

Assume that a 1 is stored at Q. A 0 is written in the cell by setting BL' to 1 and BL to 0, which apply a reset pulse to an SR latch. During the initiation of a write, the circuit can be simplified to the model shown in Fig. 2.9. And Q' side of the cell cannot be pulled high enough to ensure the writing of 1. The sizing constraint, imposed by the read stability, ensures that this voltage is kept below 0.4V. Therefore, the new value of the cell has to be written through transistor M_6 (Rabaey, Chandrakasan & Nikolic 2003).

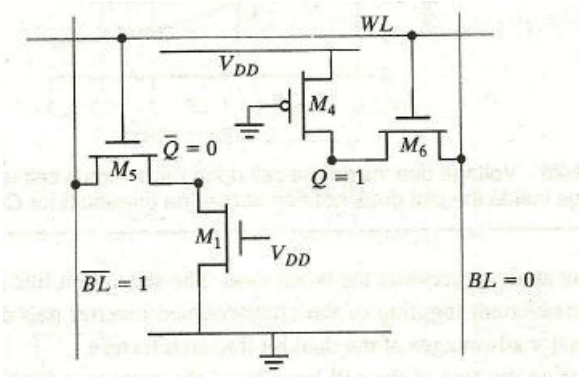


Figure 2.9 Simplified model of SRAM cell during write (Q=1)
(Rabaey, Chandrakasan & Nikolic 2003)

2.4.3 Low Gate Leakage SRAM Cells

Due to the dependence of the leakage power on the number of transistors, and the requirement of large memory content of future system on chip devices, it is important to do research on minimizing the leakage power of SRAM structures. And Anand &Chandra (2011) describe two low gate leakage SRAM cell structures, which are IWL-VC and PP-SRAM cells.

A. Improved Word-line Voltage Control (IWL-VC) SRAM Cell

Based on the conventional 6T SRAM structure, a pass transistor P3 (which is shown and highlighted in a red circle) is added and select line (SL) is used instead of word line (WL). They use this new structure of SRAM (Fig. 2.10) to improve the timing performance. The SL is always activated before WL is activated.

With the two extra NMOS transistors (NC1 and NC2, which are shown and highlighted in a red circle), the static power consumption is not significant. And they estimated that the extra power dissipation for a row of 128 SRAM cells is less than 4% of the total static power dissipation. This method lowered the gate current leakage of the cell up to 58%.

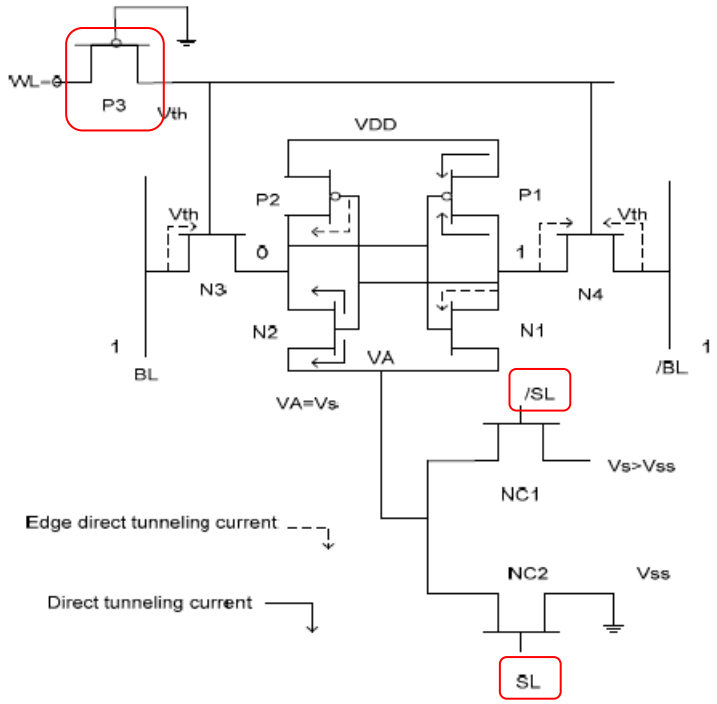


Figure 2.10 IWL-VC SRAM with Gate Leakage Currents when Cell Holds"0"
(Anand &Chandra 2011)

B. PMOS Pass-transistor (PP) SRAM Cell

The second new structure of SRAM they present is illustrated in Fig. 2.11. This is a gate leakage current reduction method based on PMOS Pass-transistor SRAM structure. Compared to the basic 6T SRAM, the PP-SRAM cell has lower gate leakage. In PP-SRAM, two PMOS transistors (P3 and P4, which are shown and highlighted in a red circle) replace the NMOS transistors (N3 and N4). This replacement can decrease the gate leakage currents of the SRAM cell.

PMOS pass transistors with high V_{TH} and forward biasing method in PP-SRAM cell structure were used to reduce both the gate oxide direct tunneling and the sub-threshold currents. And they estimated by circuit simulation that the gate leakage current was reduced by 27% and the total static power up to 45% (Anand &Chandra 2011).

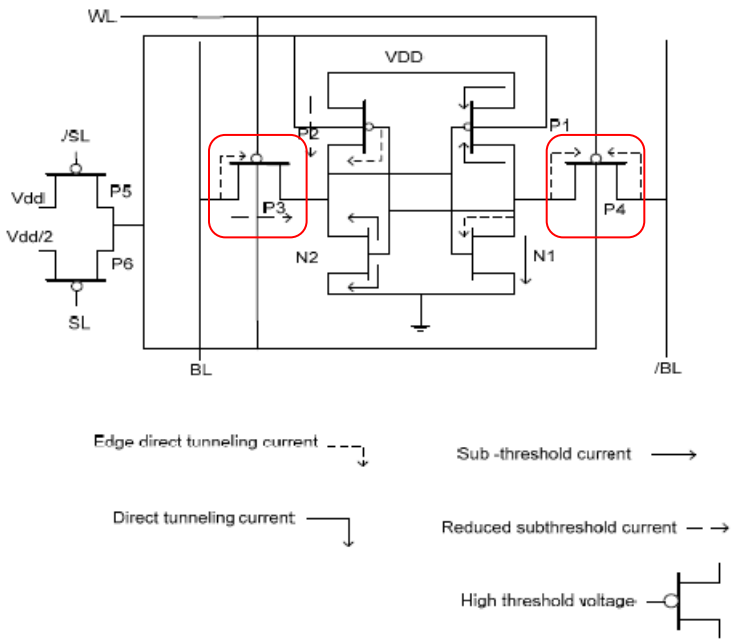


Figure 2.11 Proposed PP-SRAM Cell (Holding"0") with Gate Leakage Currents (Anand &Chandra 2011)

2.4.4 Sub-threshold 10T SRAM Cell Design

When we focus on low voltage operation, the limitation of traditional 6T SRAM cannot be ignored. Calhoun (2007) explores the limits of low voltage operation for traditional 6T SRAM and proposes an alternative bitcell that functions to much lower voltages. Fig. 2.12 shows the schematic of the 10T sub-threshold bitcell. Transistors $M_7 - M_{10}$ implement a buffer used for reading and removing the problem of Read SNM by buffering the stored data during a read access.

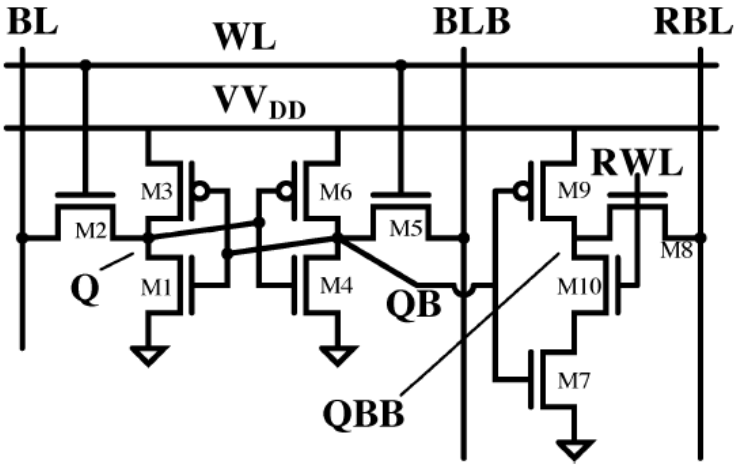


Figure 2.12 Schematic of the 10T Sub-threshold Bitcell (Calhoun 2007)

Because of the Read SNM issues, traditional 6T SRAM fails to write in sub-threshold. Calhoun, etc. tested that the 10T bitcell could solve the Read SNM problem, overcome the write problem and relax the bit-line integration limitation to allow sub-threshold operation.

Kim et al. (2008) also discuss the 10T SRAM techniques. They give an overview of traditional 6T SRAM issues in sub-threshold region .That is: due to the reduced SNM, poor writability, limited number of cells per bit-line, and reduced bit-line sensing margin, 6T SRAMs fail to deliver sufficient density and yield requirements in the sub-threshold region. Furthermore, they present a decoupled 10T SRAM cell (Fig. 2.13) for SNM improvement.

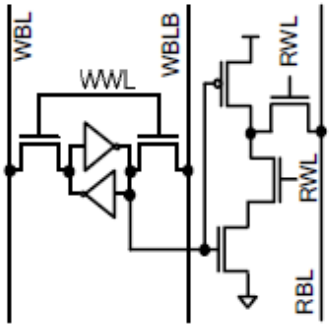


Figure 2.13 Decoupled 10T SRAM cells (Kim et al. 2008)

First, they use 10T SRAM cell to eliminate the read failure caused by data-dependent bit-line leakage. Second, they utilize reverse short channel effect (RSCE) to improve cell writability, reduce power consumption, improve logic performance and enhance circuit immunity to process variations. After circuit simulation and analysis, they realized a sub-threshold SRAM with 1k cells per bit-line operating at 0.2V and 27℃ (Kim et al. 2008).

2.5 Motivation of Proposal Research

From the review of research articles, we know that many emerging embedded applications use extremely low power with compromising real-time performance. These low power devices are generally designed using sub-threshold based design techniques. Besides, these techniques have proven useful for ultralow-power (ULP) and low-energy applications since dynamic energy consumption is reduced quadratically with V_{DD} and minimum energy operation usually occurs in the sub-threshold region (Keller et al. 2011).

However, a major challenge in the ultra low power design of circuits, particularly in memory based circuits and systems, is reliability in the presence of faults induced by electromagnetic radiation. This is because low threshold voltage and aggressive technology scaling exacerbate the reliability. Hence, more research is required to evaluate the reliability of sub-threshold circuits and systems.

3. Sub-threshold SRAM Design

Memory cells can be roughly divided into static and dynamic structures. Static structure form cross-coupled inverters to keep the data (Wang 2010) and they use the regular fast logic process and do not require additional mask steps. Because embedded SRAMs have successfully accelerated the performance of high-end microprocessors, network routers and switches, we take SRAM as the first study case in our project (Pavlov & Sachdev 2008).

The 6-transistors (6T) SRAM is significant in the digital world due to its superior robustness, low power and low-voltage operation. Therefore, we firstly focus on designing and analyzing the 6T sub-threshold SRAM. 8T sub-threshold SRAM design is also proposed to provide future comparisons analysis with 6T and critical reliability analysis.

In this chapter, the 6T and 8T sub-threshold SRAM circuit design implementation and improvement will be introduced in detail.

3.1 Conventional SRAM Block Structure

An example of the basic SRAM block structure is shown in Fig. 3.1. This picture shows an N*M memory SRAM, where N is the number of rows and M is the number of bits. The SRAM blocking diagram mainly contains the row decoder, input data control, memory matrix, and column decoder and sense amplifiers. Their names and functions are listed as follows (Pavlov & Sachdev 2008).

- Row Decoder: The row decoder gated by appropriate timing block signal decodes X row address bits and selects one of the word lines WL_0–WL_{N-1}.
- Column Decoder: Column decoders or column MUXs (YMUXs) addressed by Y address bits allow the sharing of a single sense amplifier among 2, 4 or more columns.
- Sense Amplifier: Dynamic latch-type sense amplifier with differential inputs. Several SRAM cells in one column decoder are sharing a single sense amplifier.
- Timing Block: The majority of modern SRAMs are self-timed, i.e. all the internal timing is generated by the timing block within an SRAM instance.

In the following sections, the detailed design for each sub-threshold SRAM part will be introduced.

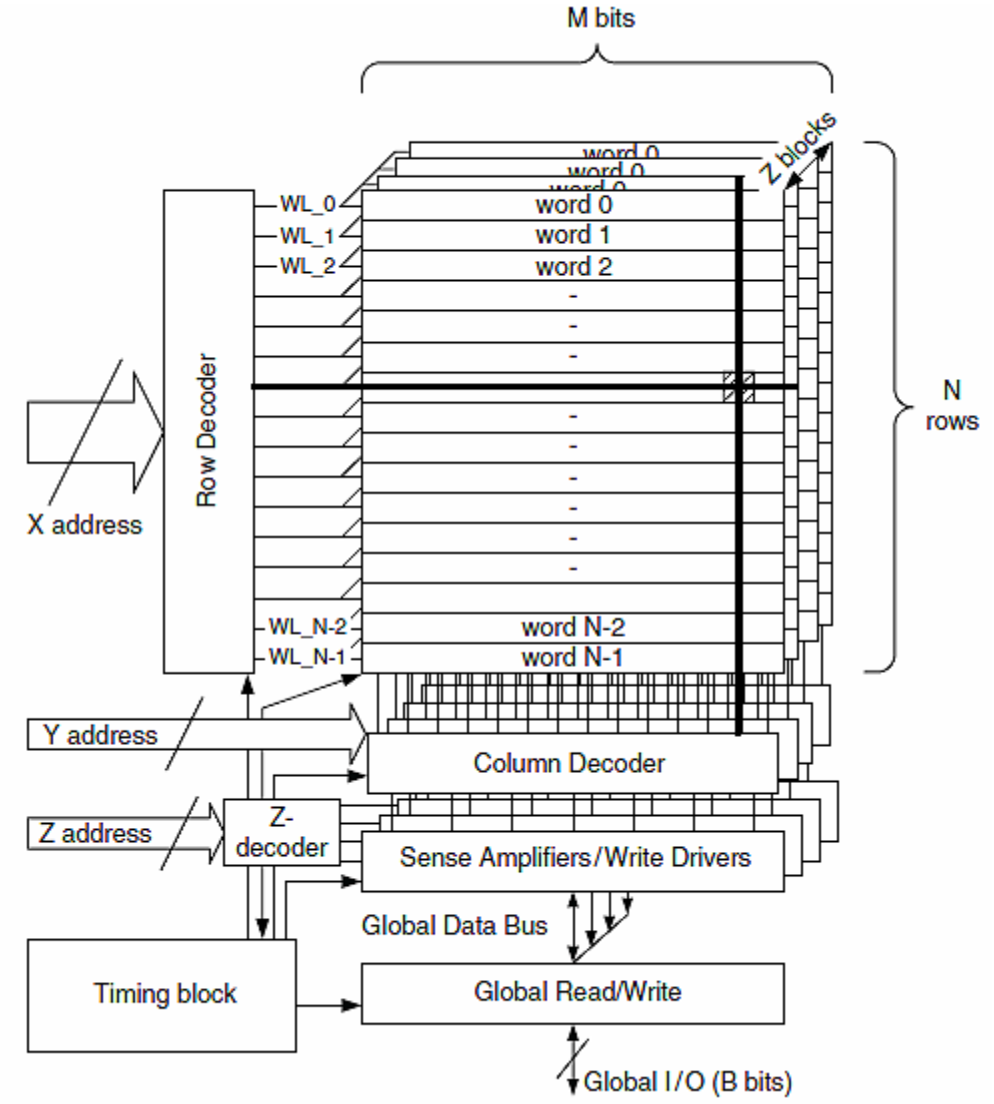


Figure 3.1 SRAM structure (Pavlov & Sachdev 2008)

3.2 Detailed 6T Sub-threshold SRAM Design

3.2.1 Conventional 6T SRAM

The conventional 6-transistors (6T) SRAM cell is widely used in digital systems and the cell structure is shown in Fig. 3.2. It uses six transistors to store and access one bit, and the four transistors in the center (M1-M4) form two cross-coupled inverters. The cross-coupled inverter pair is the foundation of the static storage elements (Wang 2010).

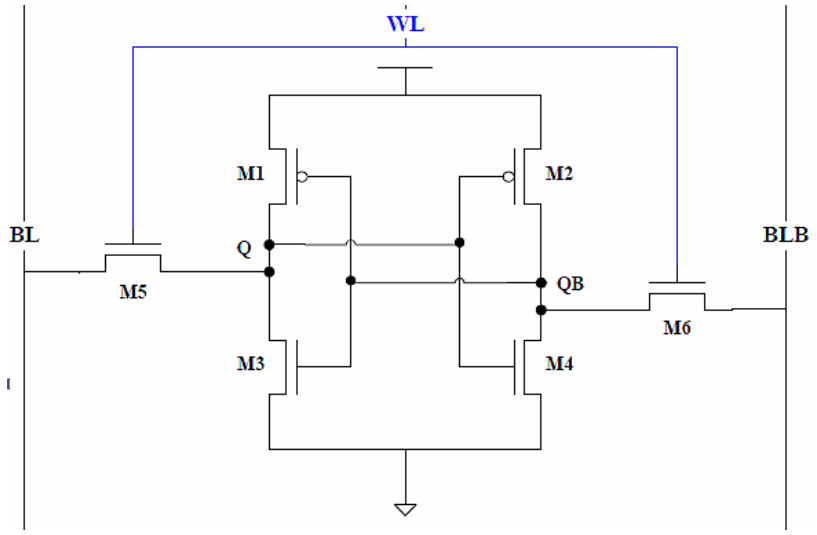


Figure 3.2 the conventional 6T SRAM cell

As Seevinck (1987) describe, the cell area and the stability are two important aspects in SRAM design. The dimension can be reduced by fabrication technology scaling down, while the stability is always a significant issue. To evaluate the stability of an SRAM cell, SNM is widely used.

As shown in Fig. 3.3, the SNM is defined as the maximum value of V_n that can be tolerated by the SRAM cell before changing states (Wang 2010). We added two voltage controlled voltage sources (VCVS) into the SRAM cell to detect the maximum value of V_n not flipping cell state.

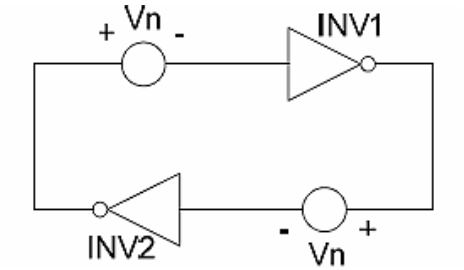


Figure 3.3 The cross-coupled inverter with noise source included (Wang 2010)

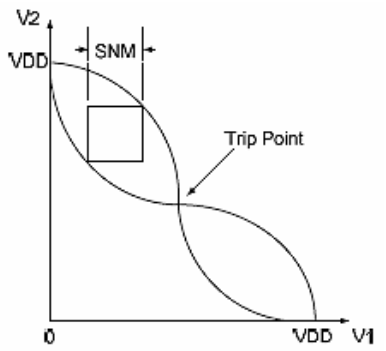


Figure 3.4 SNM estimation based on maximum square (Wang 2010)

As Wang (2010) indicated, read SNM and hold SNM can be found respectively

during read operation and at standby mode of SRAM cells. Besides, read SNM is much more critical than hold SNM in studying the stability of the SRAM cell because the former is much smaller than the latter. From the butterfly picture (Fig. 3.4), the SNM can be estimated according to the maximum squared inside the two I-V curves. The higher SNM, which means the higher stability of the cell, is always pursued when designing SRAM cells.

3.2.2 Overview of the 6T Sub-threshold SRAM Cell Design

The basic 6T sub-threshold SRAM design mainly includes SRAM cell, pre-charge, write driver, input/output, read-enable and sense amplifier circuit, shown in Fig. 3.5. To implement successful read and write operation at sub-threshold region, the SRAM cell transistor sizing must be calculated appropriately.

As Rabaey, Chandrakasan, & Nikolic (2003) mentioned, when we analyse this 6T sub-threshold SRAM read operation, assume that a '1' is stored at 'Q' point and this is the data we need to read. Firstly, both bitlines (BL and BLB) are pre-charged to V_{DD}. Then the word line is asserted, and both pass transistors M5 and M6 turn on. Because a '1' is stored in the cell, BL stays charged. However, BLB discharges through M6 and M4. It must be ensured that the QB point doesn't rise too high before C_{blb} is discharged or M1 might turn off (the inverter defined by M1/M3 switches), and the memory cell will change state. The appropriate sizing of the transistors can efficiently avoid accidentally writing a '1' into the cell. This is called a read upset. To prevent this, the voltage on QB will be dictated by the equivalent on resistances of M6 and M4. Think of them as simple resistors, which form a voltage divider. So, the resistance of M6 must be larger than M4 (there is a stronger connection from QB to ground rather than to the precharged bit line). The way to control the relative on-resistances is to have appropriate Width/Length ratios. In other words, W_{M6}/L_{M6} has to be less than W_{M4}/L_{M4}. Here, we define the Cell Ratio (CR) as equation (3.1).

$$CR = \frac{PD}{PG} = \frac{W_{M3}/L_{M3}}{W_{M5}/L_{M5}} = \frac{W_{M4}/L_{M4}}{W_{M6}/L_{M6}} \quad (3.1)$$

To avoid a read upset, the voltage on node QB should remain below the trip point of the inverter pair for all process, noise, and operating conditions. CRs are usually greater than 1.2 (most microprocessor fabrications use a minimum CR of 1.25 to 2.5). We define the CR = 2.5 in this project.

Another way to ensure the cell doesn't toggle accidentally is to precharge the bit lines to say Vdd/2 so QB could never reach the switching threshold of M4 (remember, M4 is only one half of an inverter and hence M4 actually won't switch that easily). This has performance benefits as well, since the voltage swing is now halved, and the operation is hence faster (Rabaey, Chandrakasan, & Nikolic 2003).

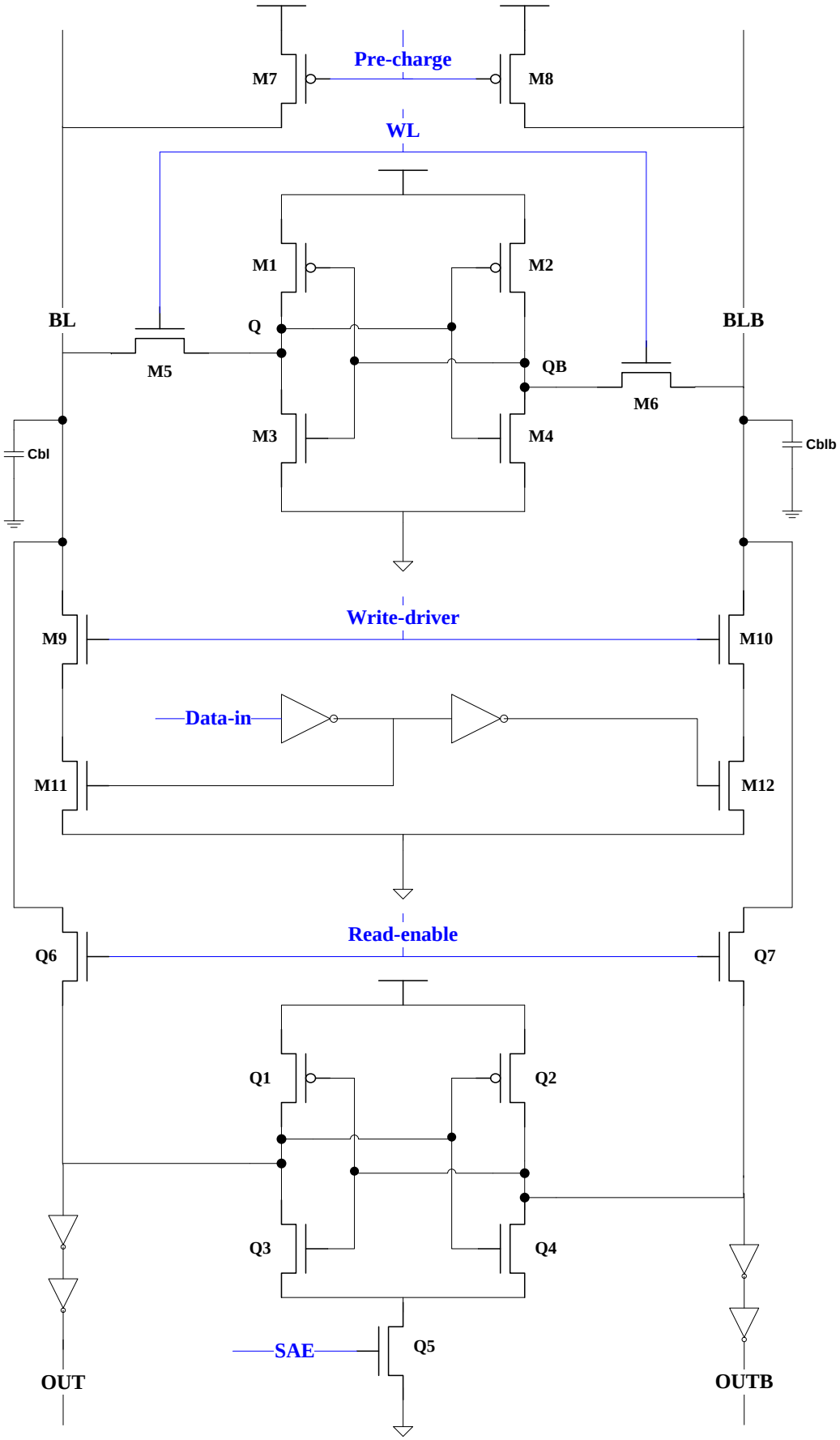


Figure 3.5 6T sub-threshold SRAM structure

For the write cycle, assume that a '1' is stored in the cell (Q = 1), and a '0' is the data needing to be written in the cell. When write enable signal (WE) is asserted, BL will discharge to '0' through M9 and M11, while BLB is still charged to '1'. And this causes the cell to change state if the devices are sized properly.

The procedure here is to put the appropriate value on the bit line pair ('0' on BL and '1' on BLB in our example of writing a zero, which is identical to applying a reset pulse to an SR latch, which is what this circuit really is), and assert the word line. From our analysis on reading the cell, we know that the value on BLB is not sufficient to toggle the cell, because we explicitly designed M4 and M6 to ensure that didn't happen. Hence the new value has to propagate through the other pass transistor M5.

In order to write to the cell, the pass transistor M5 must be more conductive than M1 to allow node Q to be pulled to a value low enough for the inverter pair (M4/M2) to begin amplifying the new data. This is the same principle we used to size M4 and M6. Now however, the bit line needs to remain constant, and the stored value to change. Therefore, M5 should have the lower on-resistance than M1.

The writing operation of the cell is reliable if Q point can be pulled low enough, and the pullup ratio (PR) of the cell is defined as the size ratio between the PMOS pullup and the NMOS pass transistor (Rabaey, Chandrakasan, & Nikolic 2003):

$$\mathrm{PR} = \frac{\mathrm{PU}}{\mathrm{PG}} = \frac{W_{M1}/L_{M1}}{W_{M5}/L_{M5}} = \frac{W_{M2}/L_{M2}}{W_{M6}/L_{M6}} \tag{3.2}$$

We can write the transistor equations (M5 is in linear, M1 in saturation regimes), and solve for the voltage at Q in terms of the W/L ratio of the devices. Because M5 is an NMOS (higher mobility and hence lower resistance) and M1 is a PMOS, using minimum sized devices for both should easily satisfy the condition.

Typically, the widths of the pullup devices are sized at or near the process minimum. Longer than minimum channel lengths may also be employed to further reduce the pullup ratio. This is necessary since the read sizing of the SRAM cell dictates that the pass gate sizing should be minimized to prevent read disturbance. According to Rabaey (2003), the PR should be less than 1.8. We define PR = 1 in this project.

In addition, the bit line capacitances C_{bl} and C_{blb} are in the pF range. Therefore, the size of the transistor connected directly with bitline will be 10 times larger than PMOS (M1 and M2) in the SRAM cell.

3.2.3 Pre-Charge Circuit Design

Before write and read operation are initiated, both BL and BLB should be pre-charged firstly. In this project, we use PMOS as PC switch, shown as Fig. 3.6. When PC signal is '0', M7 and M8 turns on, then BL and BLB will be charged to V_{DD}. Before write-enable and read-enable signals are asserted, the PC will turn off.

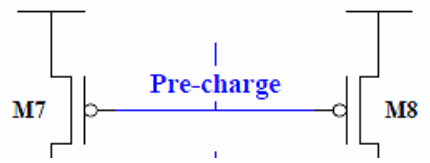


Figure 3.6 Pre-charge circuit for 6T

3.2.4 Write-Enable and Read-Enable Circuit Design

A. Write-driver

In this project, we use M9 and M10 to implement the write-driver function. When write operation signal is enabled, M9 and M10 turns on. If a '1' is waiting to be written into the cell, M11 turns off while M12 turns on. BLB will discharge through M10 and M12, and then QB point was pulled down to make M1 turn on, which makes Q point voltage increase to V_{DD}. Therefore, a '1' is written into the cell successfully.

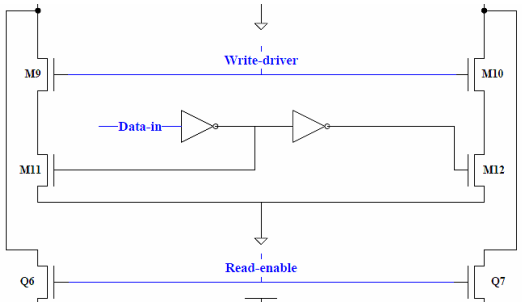


Figure 3.7 Write and read-driver circuit

B. Read-enable circuit

Pavlov and Sachdev use PMOS as YMUX signal switch, shown as Fig. 3.8. When the word line (WL) is asserted, the bit lines (BL and BLB) have discharged to a sufficient voltage differential, and then the SA is enabled by a high-to-low transition of SAE pulse. Shortly after that, the column MUX/isolation transistors Q6 and Q7 are turned off by YMUX signal changing low to high, isolating the highly capacitive bit lines from the SA parts and preventing the complete discharge of C_{BL} and C_{BLB}. Then the positive feedback of the cross-coupled inverters Q1 − Q3 and Q2 − Q4 quickly drives the low-capacitance outputs 'OUT' and 'OUTB' to the full swing complementary voltages.

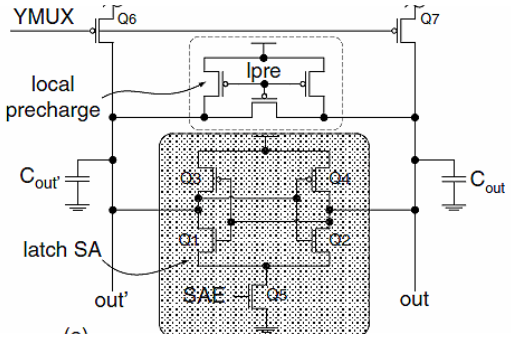


Figure 3.8 YMUX circuit with a latch-type sense amplifier (Pavlov & Sachdev 2008)

However, Pavlov and Sachdev's circuit output will not be stable, because the output line is connected directly with the bitline during the whole operation except the short isolation moment. Therefore, we have improved the YMUX switch to read-enable switch with NMOS Q6 and Q7, shown in Fig. 3.7. Additionally, because the read-enable switch is used to switch on or off the read operation, the improved circuit can be understood more clearly. When the operator needs to read data from the SRAM cell, the read-enable signal will change from low to high.

3.2.5 Sense Amplifier Design

There are various sense amplifiers (SA) used in previous SRAM designs (Wang 2010). The conventional current mirror SA is widely used as it has high sensitivity, shown as Fig. 3.9(a) (Seevinck, van Beers, & Ontrop 1991). Assume that a '1' is stored in the SRAM cell, Q3 will turn on shortly after read-enable (RE) and sense amplifier enable (SAE) signal assert. And then the current of left side of SA flows to ground through Q3 and Q5, which enable Q1 and Q2 to turn on. The output will be '1' as current flows from V_{DD} through Q2. However, the current flowing from V_{DD} through Q1 will influence the gate (G) current of Q1 and Q2, which even changes the state of the Q2 switch during one read operation. To improve this SA, we separate the gate current control of Q1 and Q3, and the improved SA is shown as Fig. 3.9(b).

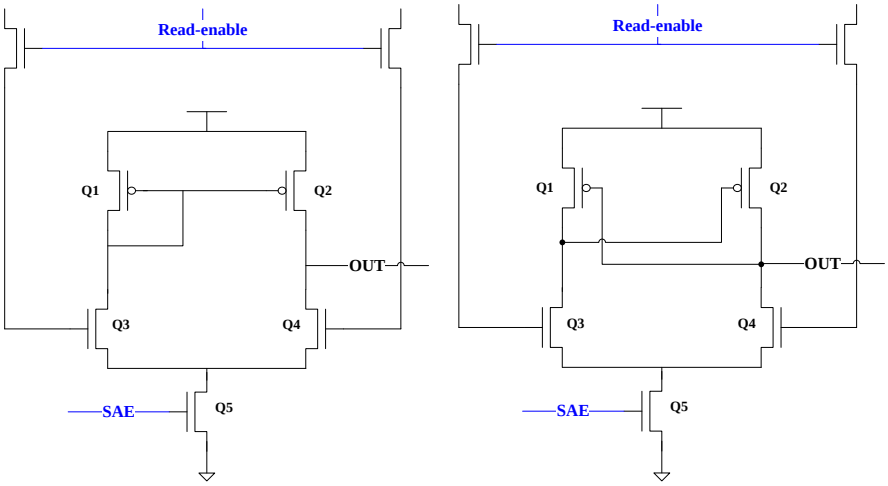


Figure 3.9 Conventional current mirror SA circuit

However, because the current mirror SA has high sensitivity, some error signal may be amplified and produce the unstable output signal. This is difficult to control and will be markedly aggravated when it works at the sub-threshold region. Assume that a '1' is stored in SRAM cell which needs to be read, and the supply voltage of the SRAM cell is lower than threshold voltage. In sub-threshold region, the Q point voltage is sub-threshold voltage which cannot keep M4 turned on enough. At read cycle, WL is asserted firstly, meanwhile, the QB point's voltage will pullup abruptly as BLB presents a positive strong voltage. And then, the current will flow from BLB to ground through M6 and M4. However, the differential voltage value between Q and QB is not so obvious. Additionally, the switch fluctuation of CMOS which is caused

by voltage fluctuation also can be amplified by current mirror SA, which is not expected.

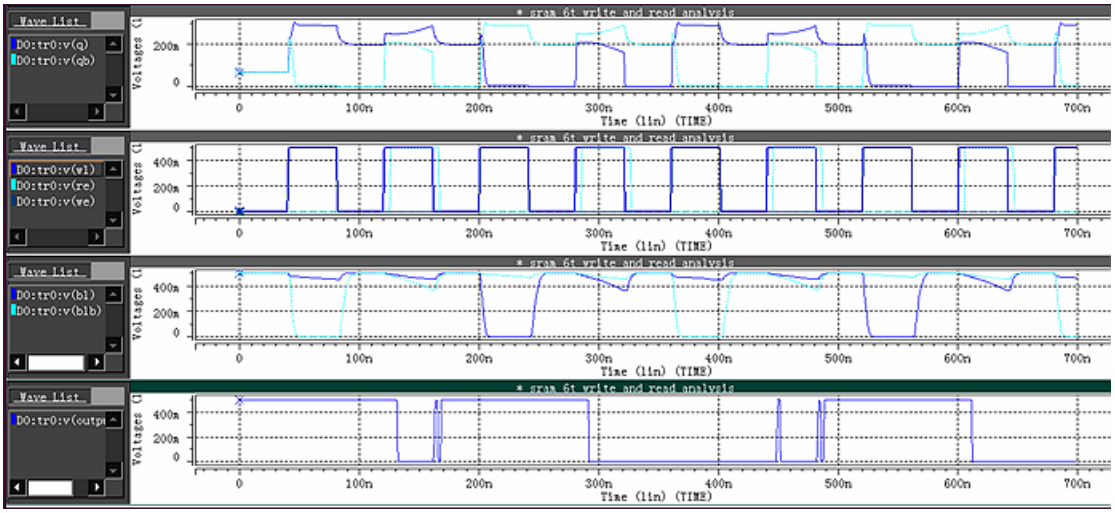


Figure 3.10 Unstable output signals with current mirror SA

Figure 3.10, which is simulated by HSPICE, is divided into four rows: state of Q and QB point, WL/RE/WE signal, state of BL and BLB, and the output signal. It is obvious that the output signal is not stable. Therefore, we improved the SA with the latch type SA, shown as Fig. 3.11. This type of SA is formed by a pair of cross-coupled inverters, much like a 6T SRAM cell.

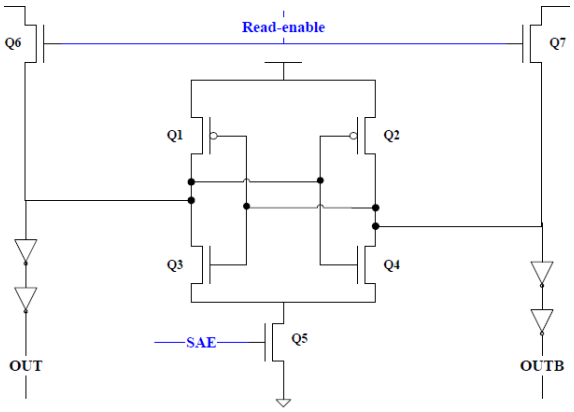


Figure 3.11 Latch type SA

When SAE is set to high, Q5 will turn on and SA begins to work, the output is stable. Fig. 3.12 shows the RE and output signal, and it can be seen that the read operation is successful, the data we collect are ‘1’, ‘0’, ‘1’ and ‘0’ as expected.

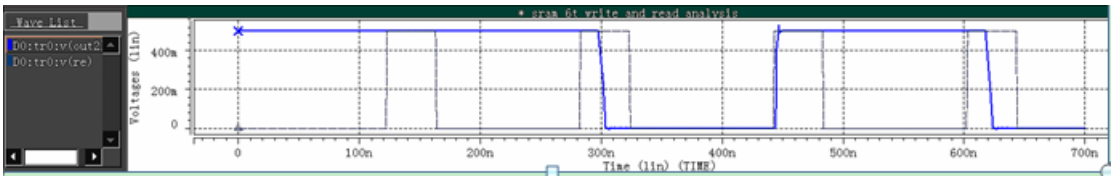


Figure 3.12 Stable outputs with latch type SA

3.2.6 Input / Output Buffer Design

Inverter type read buffers are often applied in sub-threshold design, as it can satisfy the speed requirement. The inverter type buffers are also used as data buffer and read buffer in our project.

3.2.7 Write and Read Control Sequences

After describing the whole architecture of the 6T sub-threshold SRAM and the design of each part, the read and write sequences need to be explained for future analysis.

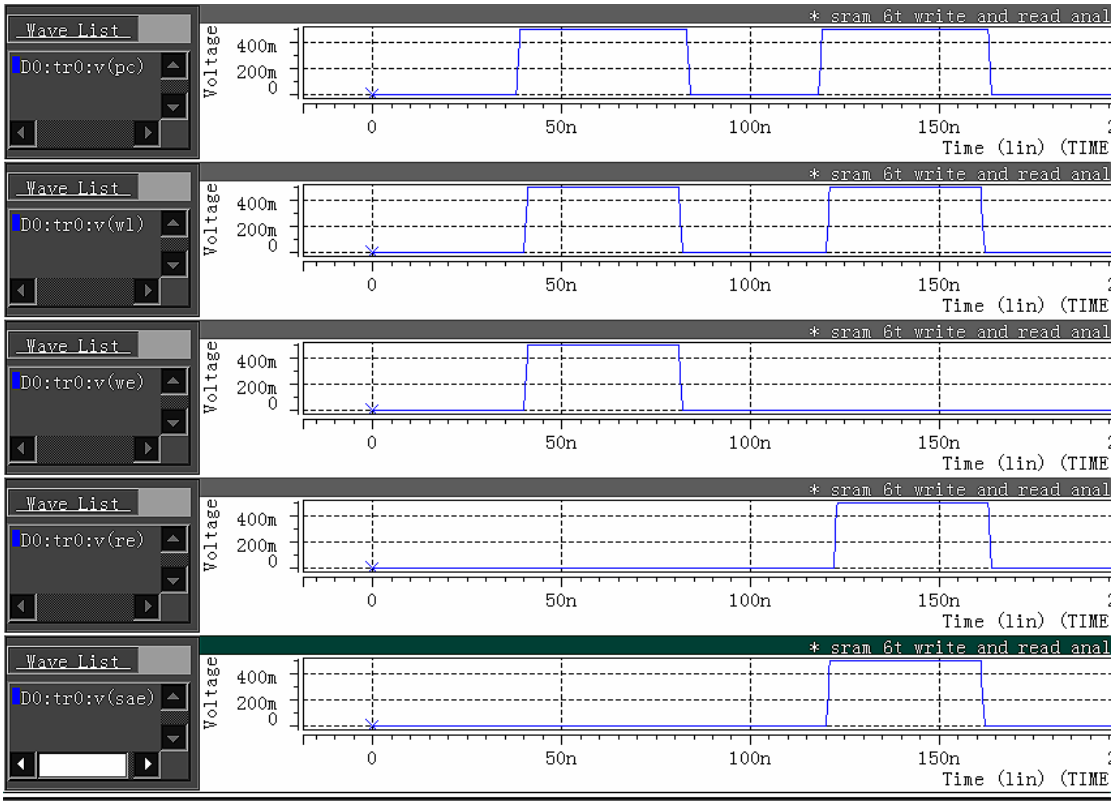


Figure 3.13 Write and read operation timing sequence for 6T

To make the write and read operation timing sequence clear, we assume that first write and then read. The period of PC and WL signal are the same, however PC signal needs to be set slightly faster than WL signal from low to high, and lower at the state of high to low. This is because pre-charge operation needs to be stopped earlier than WL is asserted. When write operation is set, the WE signal is synchronous with WL, which is the same for read operation. However, SA needs to be set a little faster than read operation; therefore, it can be seen as little nuances between the SA and RE signal.

3.3 Detailed 8T Sub-threshold SRAM Design

After designing the 6T sub-threshold, we realized that more research needs to be done on 8T sub-threshold SRAM design. And then more reliability analysis on 8T sub-threshold SRAM design and the contrastive analysis between 6T and 8T sub-threshold will be examined and introduced.

3.3.1 Overview of the 8T Sub-threshold SRAM Cell Design

The 8T sub-threshold SRAM design mainly including SRAM cell, pre-charge, write driver, input/output, and read operation circuit, and the schematic of the cell is shown in Fig. 3.14. To combat the challenges of sub-threshold SRAM design, this cell has a 6T storage cell and a 2T read-buffer cell. Because the write operation and read operation for 8T are separated and isolated, the WL signal does not need to be set during read-accesses. In other words, the BL charge will not influence the data in the cell. Therefore, the SA circuit is no longer needed at 8T design (Wang 2010). The details of how write and read operation operate will be introduced in the following section.

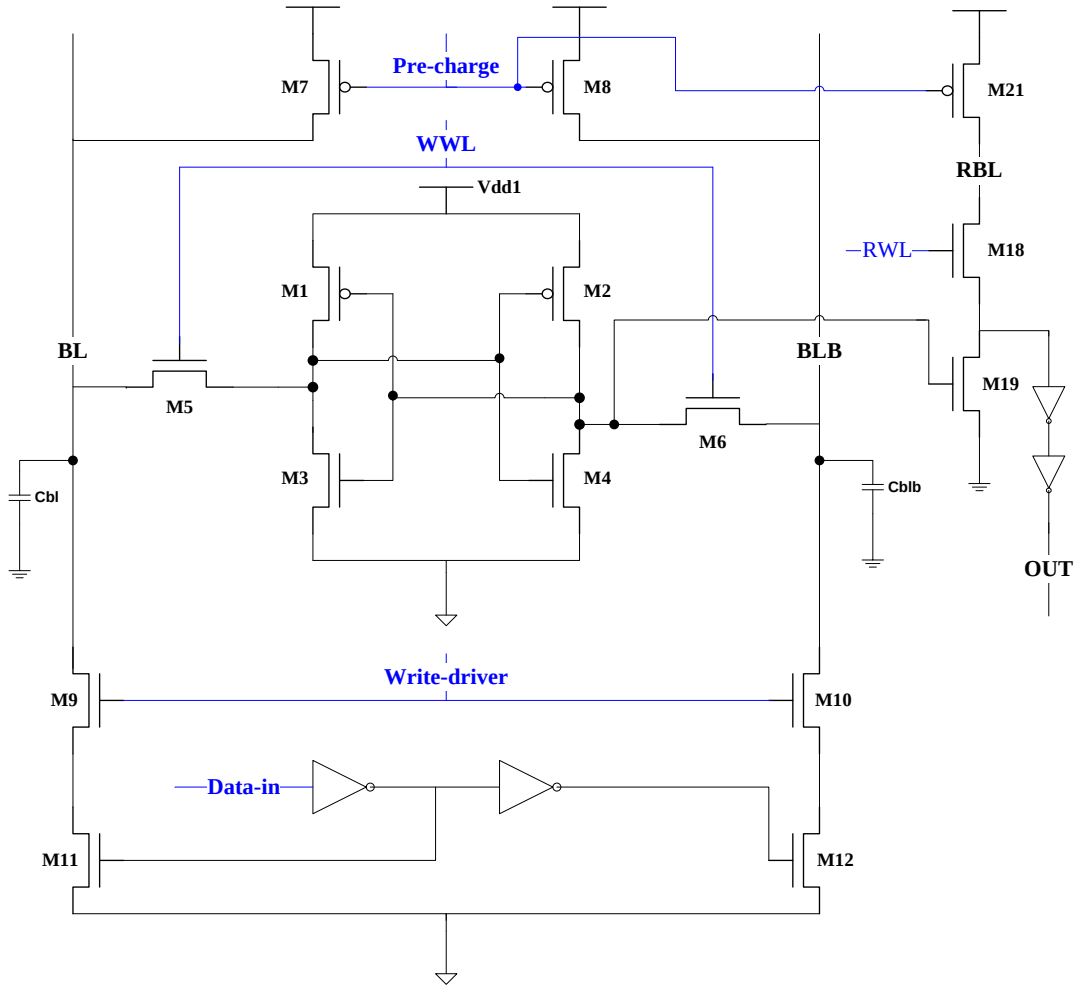


Figure 3.14 8T sub-threshold SRAM structure

To implement successful read and write operation at sub-threshold region, the SRAM cell transistor sizing are also needs to be calculated appropriately. Based on CR and PR calculation discussed before, the 8T sub-threshold SRAM cell has similarly sizing with 6T sub-threshold SRAM design. The CR is also 2.5, and PR is 1.

3.3.2 Pre-Charge Circuit Design

Different from 6T, a new line named read bitline (RBL) is added into the 8T sub-threshold circuit. Therefore, PC needs to charge RBL as well before write and read operation, shown in Fig.3.15.

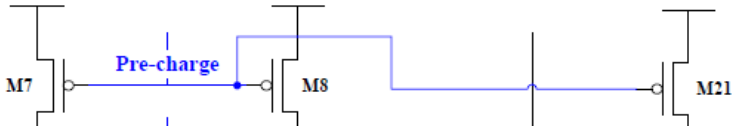


Figure 3.15 Pre-charge circuit for 8T

3.3.3 Write Operation and Read Operation

A. Write Operation

Write operation of 8T cell is the same as 6T design. Write access to the bitcell occurs through the write access transistors (M5 and M6) from BL and BLB. Here, we call BL and BLB as write bitline. When write data goes into the cell, write word line (WWL) signal and write driver (WE) signal are set to '1' together. And then, M5, M6, M9 and M10 are turned on, which allows data to be stored into the SRAM cell (Calhoun et al. 2007).

B. Read Operation

Different from 6T, the read operation is isolated from WWL and bitline. Read operation for 8T sub-threshold design is controlled by read word line (RWL) signal. Assume that a '1' is stored in Q point, and QB = '0'. When RWL is set to '1', read-buffer reads data directly from QB point, and low voltage signal at QB makes M19 turn off. Meanwhile, the current flows from RBL to output through M18 and export the value '1' as expected.

3.3.4 Write and Read Control Sequences

After describing the whole architecture of the 8T sub-threshold SRAM and the design of each part, the read and write sequences need to be explained for future analysis.

To make the write and read operation timing sequence clear, we also assume write firstly and then read. Fig. 3.16 shows write and read operation timing sequence, divided into four rows, PC, WWL, WE and RWL. The WWL signal and RWL signal are separate to implement write operation control and read operation control. The period of PC is set the same as 6T sub-threshold design. During write operation set, the WE signal is synchronous with WWL. Different from 6T control sequences, read operation has no relationship with WWL.

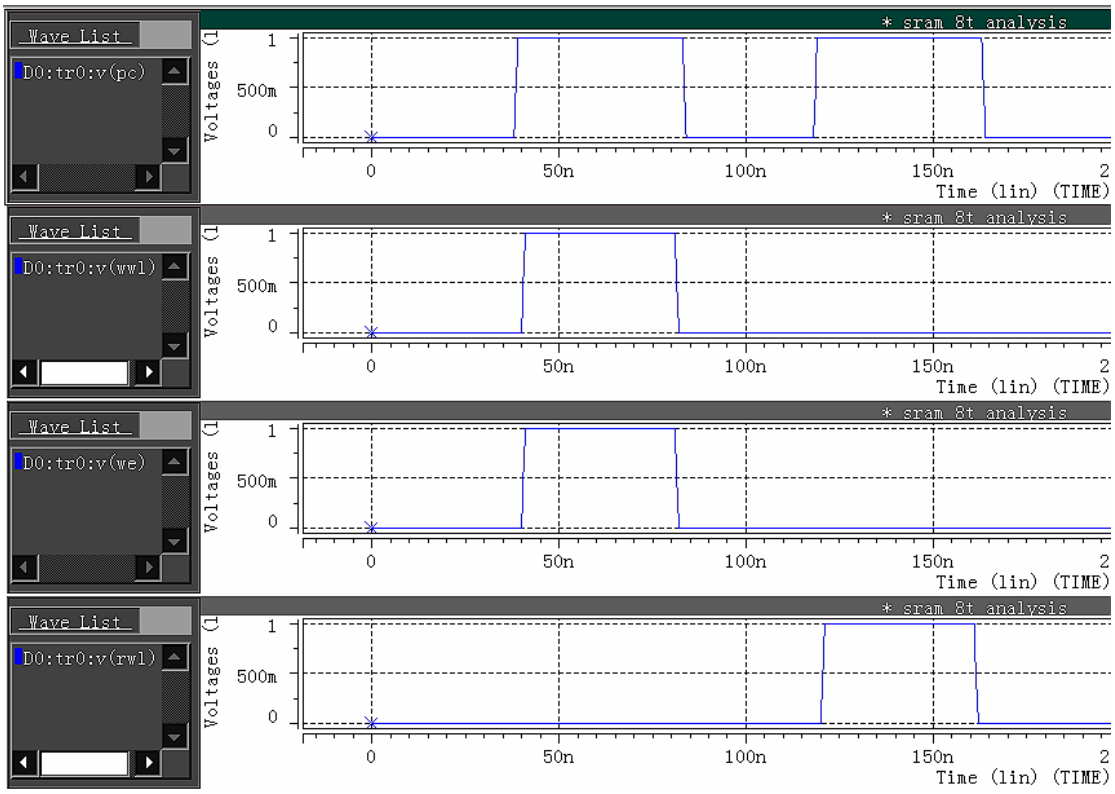


Figure 3.16 Write and read operation timing sequence for 8T

4. Software Introduction and Design Simulation

The purpose of design simulation is to check whether the designed circuits work as expected or not before fabrication. And the circuit will be corrected considering the feedback from simulation once there is any error, which will prevent the failure of the fabricated chip to some extent (Wang 2010). The schematic of the sub-threshold SRAM design in this project was firstly simulated in Hspice with the newest predictive technology model in low power (LP) 45nm technology provided by ptm.asu.edu PTM website. And more size, such as 16nm, 22nm, and 32nm PTM LP model will also be simulated and analysed in later work.

In this chapter, the introduction of Hspice and simulation of successful sub-threshold design has been described in detail.

4.1 Introduction of HSPICE

As simulation software, Hspice operation interface is introduced in Fig. 4.1. After importing the file, the basic two operations (which are shown and highlighted in red circle) are Simulation and Avanwaves. Using Hspice, we can simulate, check the correctness of our sub-threshold design, and calculate the power consumption, time delay etc. Besides, based on the data collected by Hspice simulation, the critical characters influencing the reliability of a sub-threshold memory system will be analysed.

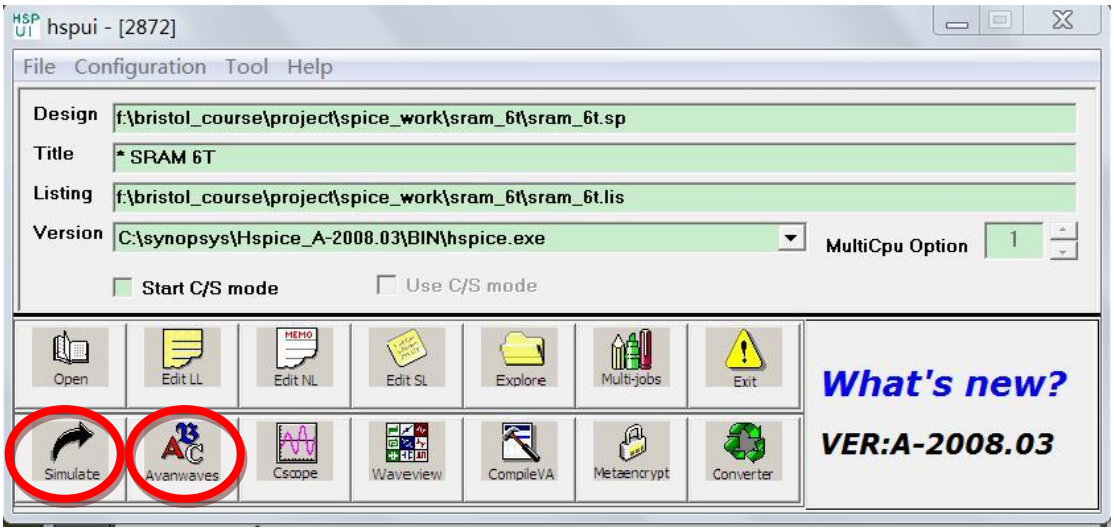


Figure 4.1 Hspice operation interface

Fig. 4.2 shows the content for basic AND_gate.sp file. The Hspice file mainly includes file title, parameter setting for PMOS and NMOS (which is shown and highlighted in a red circle); pulses form (which is shown and highlighted in a blue circle), CMOS circuit model building (which is shown and highlighted in a yellow circle). Besides, the setting for clock, delay and power are also needed. Considering

different needs and research, other functions such as power consumption, time delay and etc. are written in the Hspice file. Finally, the predictive technology model (PTM) for CMOS should be added.

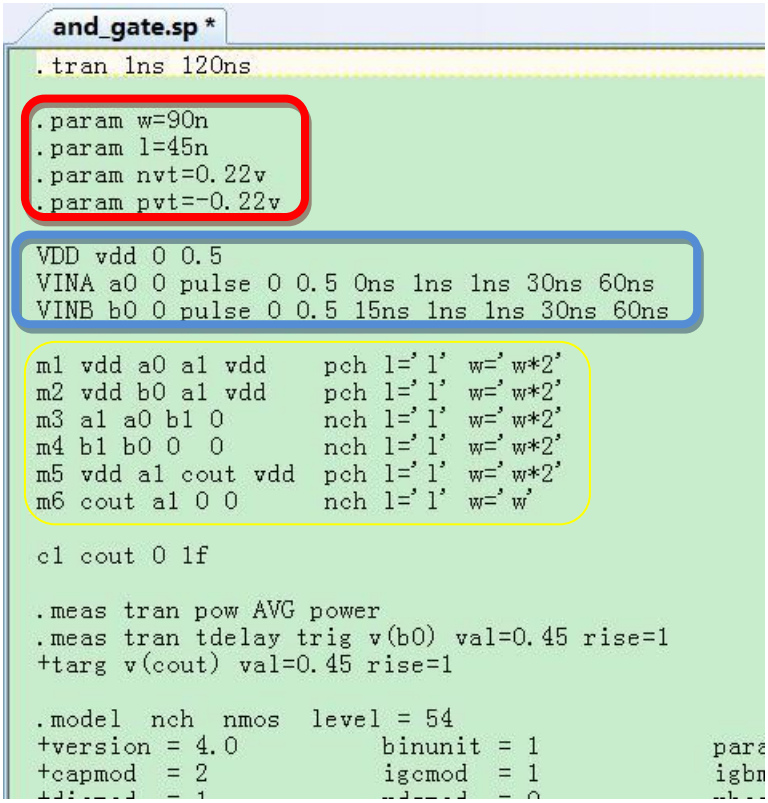
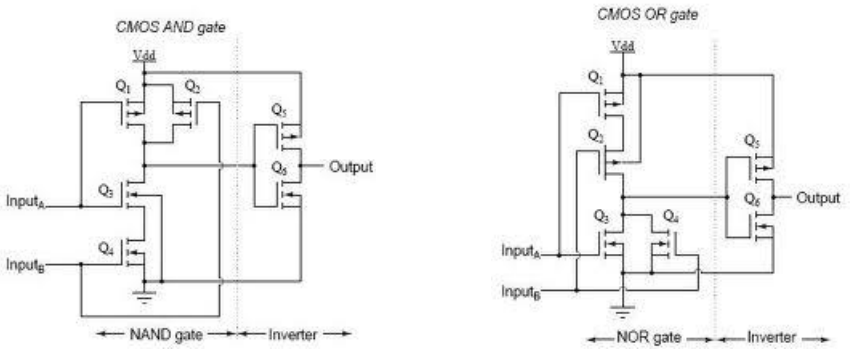


Figure 4.2 AND_gate.sp file

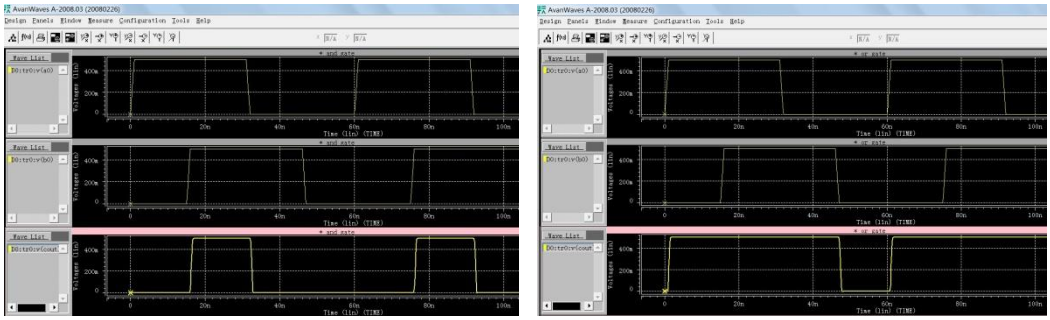
In order to grasp the application of Hspice, we model two simple gate circuits as previous work: AND_gate and OR_gate. The schematic of these two circuits are introduced in Fig. 4.3.



(a) AND gate (b) OR gate

Figure 4.3 CMOS AND gate and OR gate circuits

After building the model that corresponds to the CMOS circuits with Hspice language, the simulation waveforms are shown in Fig. 4.4. V (a0) and V (b0) are input signals and shown in first two row sub-windows, and V (cout) is the output signal.



(a) AND_gate waveform (b) OR_gate waveform

Figure 4.4 AND gate and OR gate Hspice simulation waveform

From the waveform we can get correct signal feedback, which is an important basis for later analysis. The detailed simulation and analysis for 6T and 8T sub-threshold design will be introduced in the following section and the corresponding final code will be given in the APPENDIX chapter.

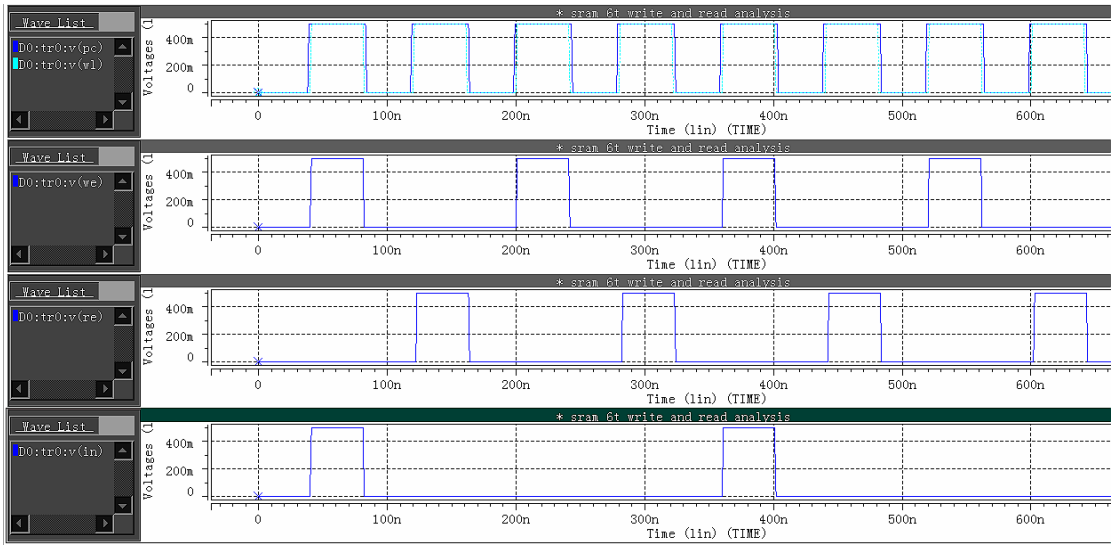
4.2 Design Simulation

We mainly work on 45nm LP model in our project, and the simulation results for successful sub-threshold design are shown in the following sections after the Hspice file programming work.

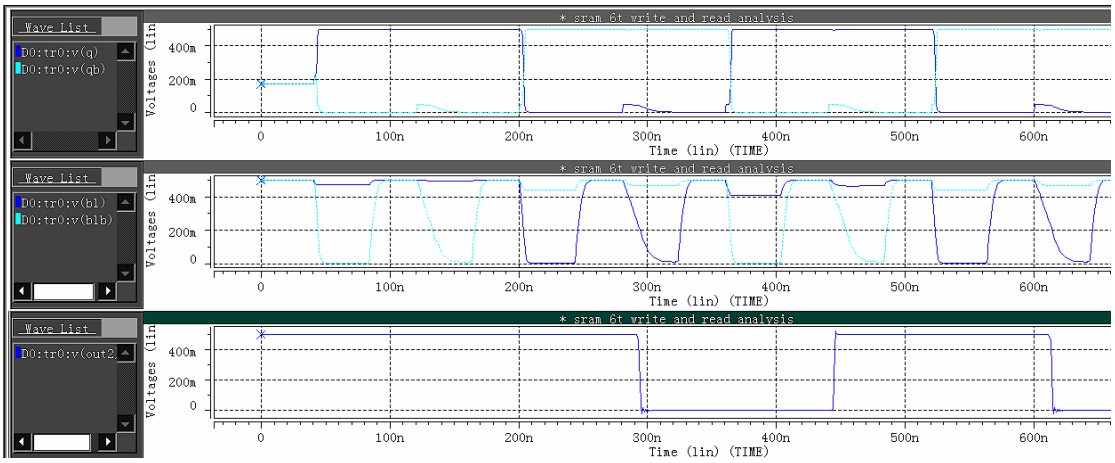
4.2.1 6T Sub-threshold Design Simulation

After thinking and solving the challenges, and designing each part of the circuit as introduced before, the 6T sub-threshold design with 0.22v as threshold voltage can work successfully under sub-threshold voltage equaling 0.2v (which is the supply voltage for the SRAM cell). The simulation results for both normal threshold ($V_{DD} = 0.5V$) and sub-threshold ($V_{DD} = 0.2V$) are shown as Fig. 4.5. The input data are ‘1’, ‘0’, ‘1’ and then ‘0’. Write operation has been set firstly, and then read. The PC, WL, WE and RE signals are set as introduced in chapter3 and shown in the first four rows in the screenshot as Fig. 4.5(a). The next rows present the state of Q/QB and BL/BLB, then the output results. When first read operation begins, a ‘1’ should be read from output at 120ns, and a ‘0’ for second read operation at about 280ns, and then ‘1’, and ‘0’. Besides, the output waveform for normal supply voltage, which is 0.5v, is also simulated as Fig. 4.5(b), and the sub-threshold result shown in Fig. 4.5(c).

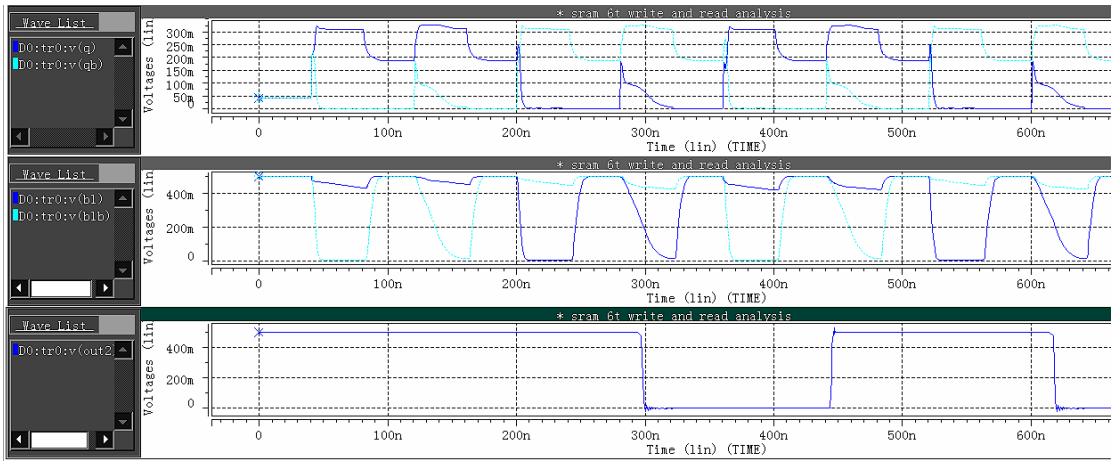
As the screen shows, the final simulation exports the results as expected.



(a) PC, WL, WE, RE, data_in signal



(b) Normal threshold design simulation



(c) Sub-threshold design simulation

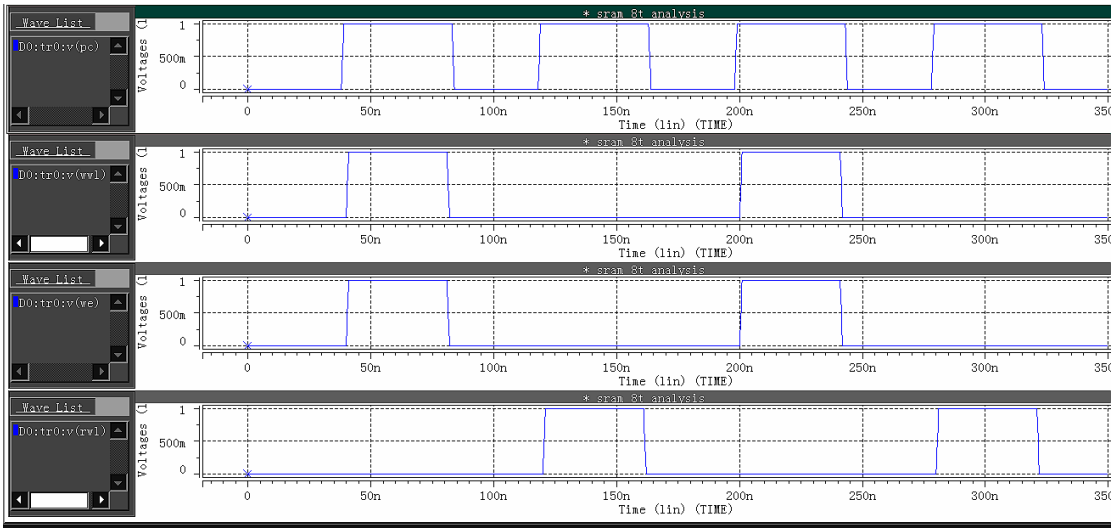
Figure 4.5 Simulation of 6T SRAM design

4.2.2 8T Sub-threshold Design Simulation

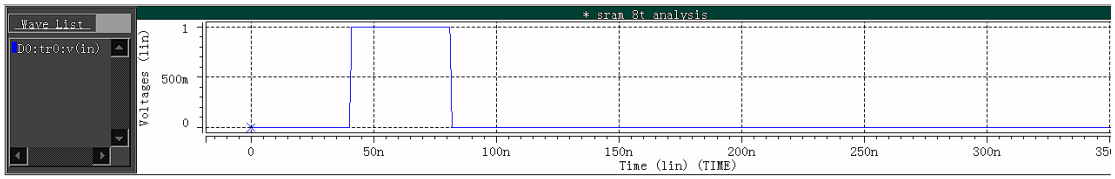
The 8T sub-threshold design with 0.587v as threshold voltage can work successfully under sub-threshold voltage equaling 0.4v (which is the supply voltage for the SRAM cell). The simulation results for both normal threshold ($V_{DD} = 0.8V$) and sub-threshold ($V_{DD} = 0.4V$) are shown as Fig. 4.6. The input data are '1' and'0', shown as Fig. 4.6(b). Write operation has been set firstly, and then read.

Different from 6T sub-threshold SRAM design, the 8T read operation connected with a new word line named read word line (RWL). The PC, WWL, WE and RWL signal are set as introduced in chapter3 and shown in the first four rows in the screenshot as Fig. 4.6(a). The next rows present the state of Q/QB, BL/BLB and RBL (read bitline), then the output results. When first read operation begins, a '1' should be read from output at 120ns, and a '0' for second read operation at about 280ns. Besides, the output waveform for normal supply voltage, which is 0.8v, is simulated as Fig. 4.6(c), and the sub-threshold result shown in Fig. 4.6(d).

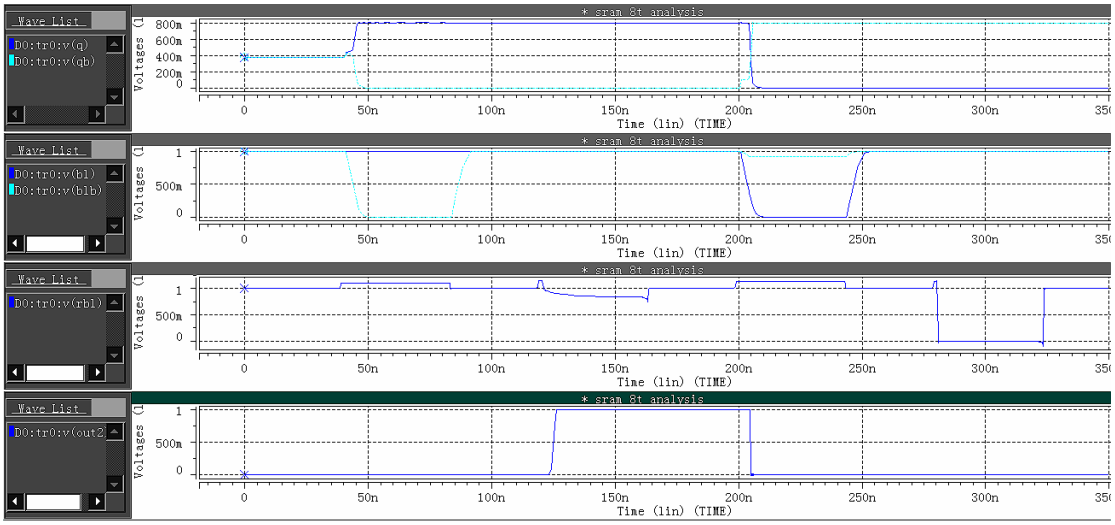
As the screen shows, the final simulation exports the results, which is a '1' and then a '0', as expected.



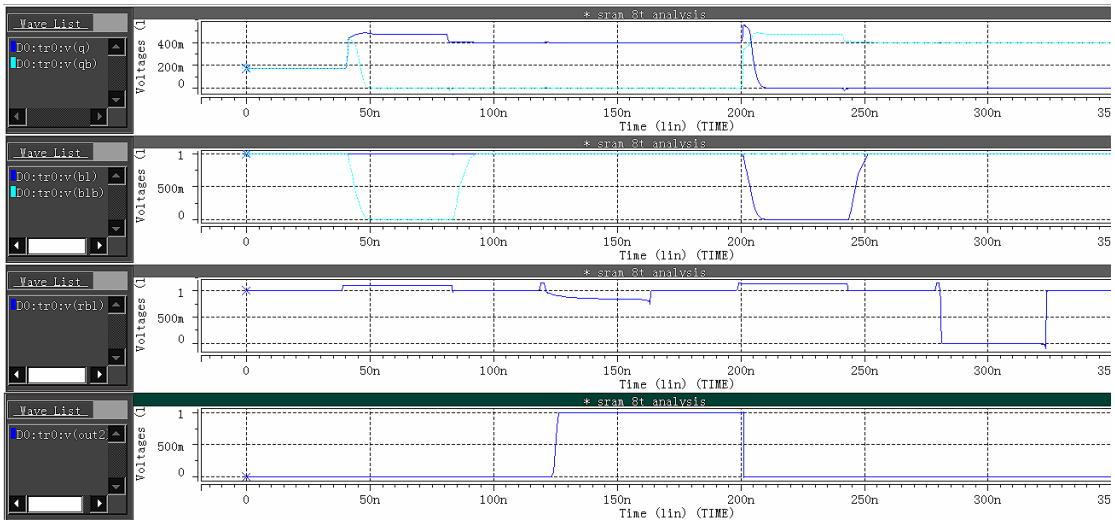
(a) PC, WWL, WE, RWL signal



(b) Input signal (first '1', and then '0')



(c) Normal threshold design simulation



(d) Sub-threshold design simulation

Figure 4.6 Simulation of 6T SRAM design

5. Reliability Analysis of Sub-threshold Design

In order to evaluate the inherent reliability of a device, find the critical characteristics which influence reliability, and pinpoint potential areas for reliability improvement, the reliability analysis is significant. SNM as the paramount method to evaluate the stability of the system will be calculated in Hspice and MATLAB when we analyse the reliability of the circuit.

In this chapter, reliability analysis of not only comparison between different designs, same design under different critical parameters, but also various predictive technology models (PTMs) technology will be introduced. And then, the critical parameters affecting reliability of sub-threshold design will be carried out.

5.1 Comparison Near-threshold and Sub-threshold Design

As Keller (2011) mentioned, to implement ultra-low energy operation, reducing the supply voltage below the process nominal V_{DD} is necessary. Additionally, the power consumption and reliability comparison between near-threshold and sub-threshold design is significant. Before the reliability analysis of sub-threshold SRAM design, some research on near-threshold also has been introduced in the following sections.

5.1.1 Power Consumption

Energy reduction usually motivates sub-threshold design (Calhoun et al. 2009). This section shows the energy variety with supply voltage V_{DD} decreasing. Take 8T sub-threshold as an example, dynamic and leakage energy consumption and total energy reduction for per operation are shown in Fig 5.1 with Hspice simulation. The threshold voltage for 8T sub-threshold design is 0.587v. To see reducing V_{DD} effects on energy, we changed the supply voltage for the SRAM cell from 0.8v (which is normal voltage) to 0.4v (which is sub-threshold voltage). And 0.57v~0.6v can be considered as a near-threshold region. As the bar chart shows, the dynamic energy reduced quadratically with V_{DD} decreasing, while the leakage energy increased slowly. As Calhoun (2009) and Keller (2011) mentioned the minimum energy operating point always occurs at the sub-threshold region, and the minimum-energy operating point depends largely upon the ratio of dynamic to leakage energy.

As Keller (2011) mentioned, the issue of reliability is critical when facing the random parameter variation and CMOS circuits become less reliable as V_{DD} is reducing. Therefore, it is necessary for the comparison of reliability analysis with changing V_{DD}.

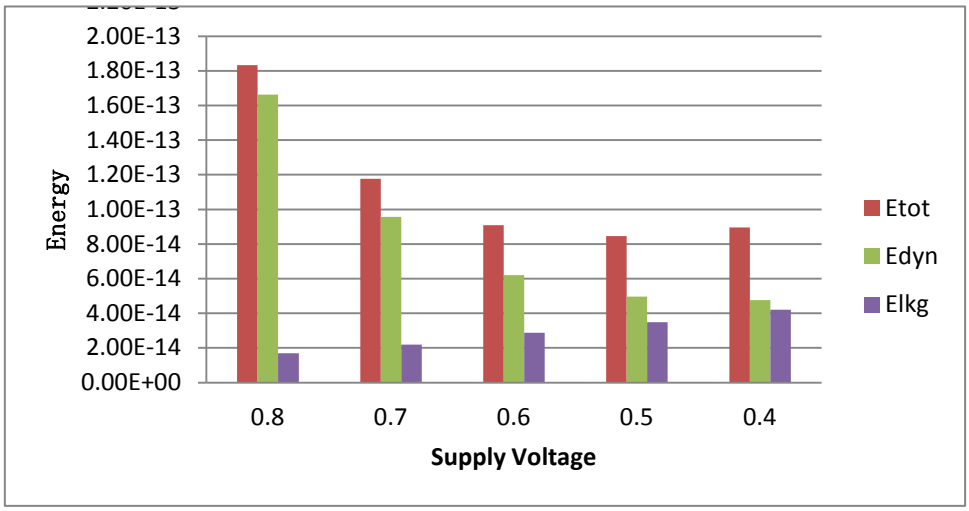


Figure 5.1 Energy drawn for 8T sub-threshold design

5.1.2 SNM Comparison Analysis between Near-threshold and Sub-threshold

As mentioned before, static noise margin (SNM) is the paramount factor used to evaluate the stability of the SRAM cell. Drawing and mirroring the inverter characteristics and finding the maximum possible square between them is the basic understanding of the SNM (Seevinck et al. 1987). During read operation, M5 and M6 are turned on, while in hold mode, M5 and M6 are turned off. Therefore, the read SNM is more critical than hold SNM in studying the stability of the SRAM cell as the former is much smaller than the latter (Wang 2010), as shown in Fig. 5.2. In the following part, SNM is always referred to as read SNM unless specified.

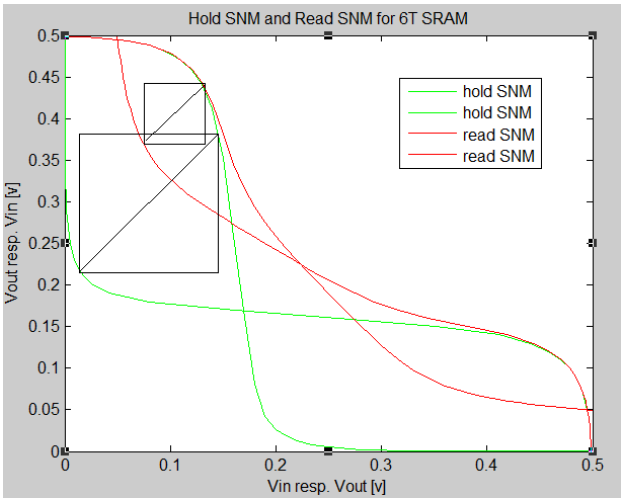
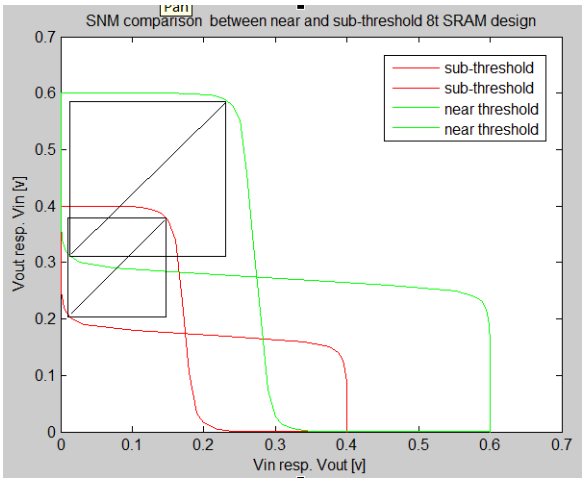


Figure 5.2 Simulated SNM for 6T read/hold

Take 8T SRAM cell as an example, as Fig. 5.3 shows, it can be seen obviously that the SNM of sub-threshold design (V_{DD} = 0.4v) is much lower than near threshold design (V_{DD} = 0.6v). And the table (5.1) shows the value of SNM varying with V_{DD}. Obviously, the SNM will decrease with supply voltage drop. However, the power consumption is still the paramount requirement factor in the digital world (Keller et al.

2011). In the following parts of this thesis, Seecinck's (1987) method is applied when comparing the stability of different cell designs and same design under different critical parameters.



V_{DD} (v)	read SNM (v)
0.8	0.2953
0.7	0.2910
0.6	0.2561
0.5	0.2093
0.4	0.1581

Table 5.1 8T Read SNM variety

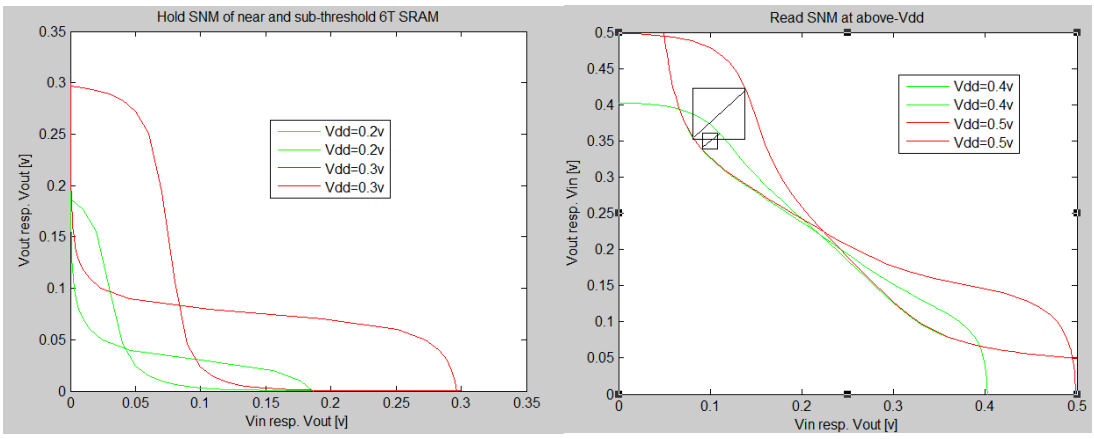
Figure 5.3 Simulated SNM of 8T near and sub-threshold

5.2 Reliability Analysis of Sub-threshold Design

To find the critical parameters affecting the reliability of sub-threshold design, it is significant to do some comparing analysis of different cell designs and same design under different critical parameters.

5.2.1 SNM Analysis of 6T Sub-threshold Design

As we mentioned before, the read SNM is much lower than hold SNM; the hold SNM for 6T sub-threshold design is decreasing as supply voltage drops, shown as Fig. 5.4 (a). However, the read SNM fails (Calhoun et al. 2006) at sub-threshold region and is very small even at near threshold, shown as Fig.5.4 (b).



(a) Hold SNM at near and sub-threshold region (b) Read SNM at above-threshold region

Figure 5.4 Simulated SNM for 6T read/hold under near and sub-threshold region.

As Calhoun (2006) described, many techniques have been reported to mitigate the low-voltage SRAM read SNM problems described above. To reduce bit-line precharge voltages and negative word line bias for unaccessed cells are two ways to increase the read SNM. However, forming a read buffer to isolate the internal storage nodes, Q and QB, will make read upset problem not happen (Calhoun et al. 2006). This method is the 8T sub-threshold design and the SNM for 8T is obviously larger than 6T, which means that 8T sub-threshold design will give us a more clearer and more accurate simulation feedback.

5.2.2 SNM Analysis of 8T Sub-threshold Design

8T sub-threshold design eliminates the read SNM problem of Fig. 5.4 (b), and SNM is always referred to read SNM unless specified in the following parts. As mentioned above, the SNM for 8T sub-threshold design is larger than 6T. And more reliability analysis for same design under different critical parameters will be introduced in the following sections.

A. V_{DD} Varying

As shown in Fig. 5.3, the values of SNM decrease apparently as supply voltages drop and limited to $V_{DD}/2$ because of the two sides of the butterfly curve. Therefore, the upper limit on the change in SNM with V_{DD} is 1/2 (Calhoun et al. 2006). Fig. 5.5 shows the butterfly curves at different supply voltages from 0.4v to 0.8v, which indicates the impact of supply voltage on SNM is significant.

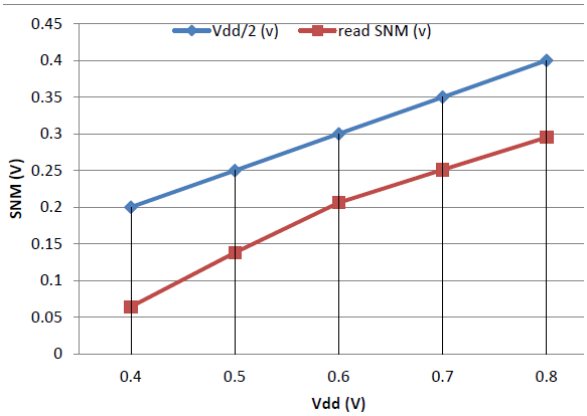


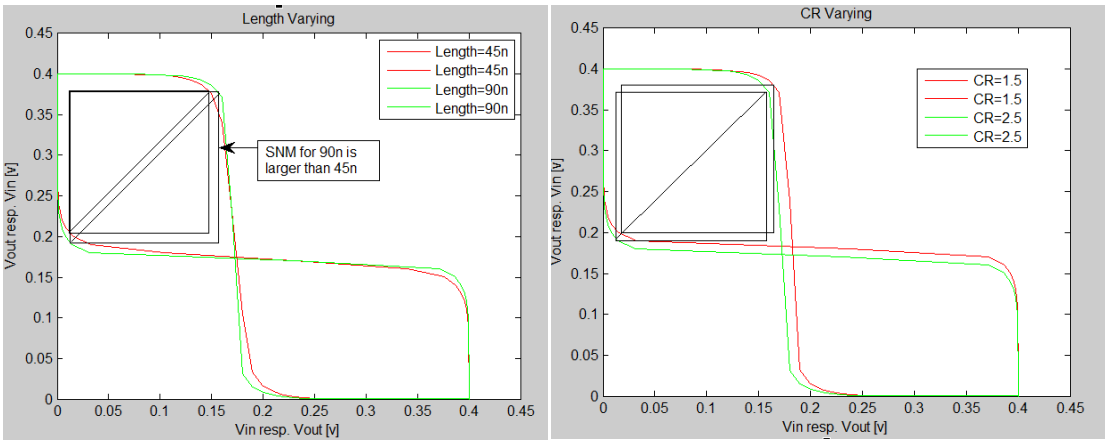
Figure 5.5 SNM versus V_{DD}

B. Length Varying

We investigate some critical parameters to improve SNM. As Calhoun (2009) introduced, increasing length (L) with constant width (W) as one powerful way to improve NM, can be seen in Fig. 5.6 (a). However, considering the size of chip, the value of L must be set appropriately. Table 5.2 shows the SNM varying with L and CR changing.

Table 5.2: SNM varying with L and CR changing

L		CR	
Length	**SNM (vdd=0.8)**	**Cell Ratio**	**SNM (vdd=0.8)**
45	**0.1455**	**1**	**0.1487**
60	**0.1500**	**1.5**	**0.1489**
75	**0.1521**	**2**	**0.1496**
90	**0.1532**	**2.5**	**0.1504**
		3	**0.1509**



(a) L changing (b) CR changing

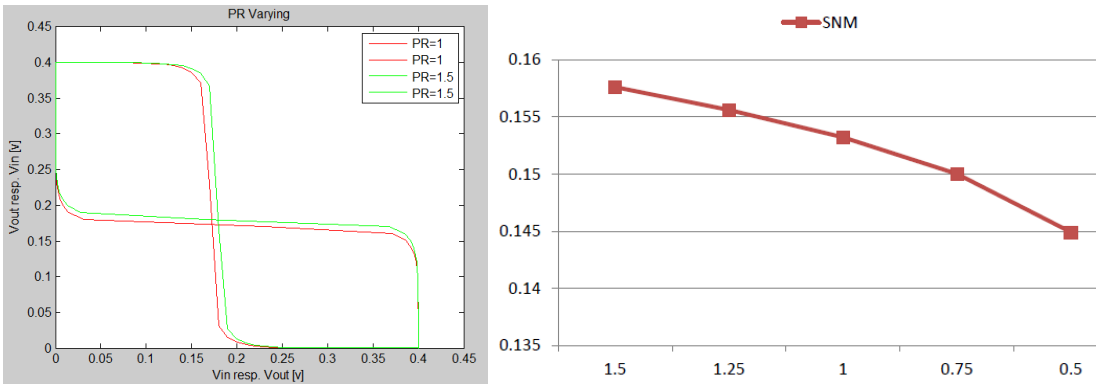
Figure 5.6 Simulated SNM with L and CR varying

C. Cell Ratio (CR) Varying

In contrast to V_{DD} and L, CR has very little impact on SNM during sub-threshold read operation (Calhoun et al. 2006), shown as Fig. 5.6 (b).

D. Pullup Ratio (PR) Varying

The impact of PR on SNM in sub-threshold is also not large. Fig.5.7 (a) shows SNM versus PR in sub-threshold. Additionally, as Calhoun (2006) mentioned in the paper, Static Noise Margin Variation for Sub-threshold SRAM in 65-nm CMOS, the sub-threshold SNM sensitivity to any sizing changes is reduced, shown as Fig. 5.7 (b).



(a) Simulated SNM with PR varying (b) PR affects on SNM

Figure 5.7 SNM versus PR

E. Size Varying

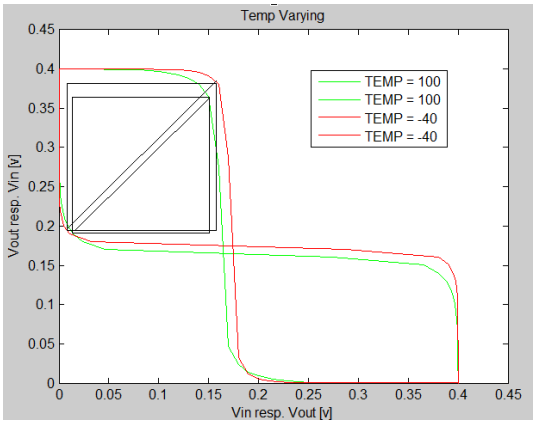
The project we introduced before is based on 45nm LPPTM technology, and in this section, we try to use different technology to evaluate the SNM of the SRAM cell. When the supply voltage is lowered, the noise margin decreases significantly. Table 5.3 shows the read SNM under normal and sub-threshold voltage in 45nm, 32nm, 22nm, and 16nm LPPTM technology. As the table below shows, the SNM is decreased as CMOS is scaling down.

Table 5.3: SNM varying with size changing

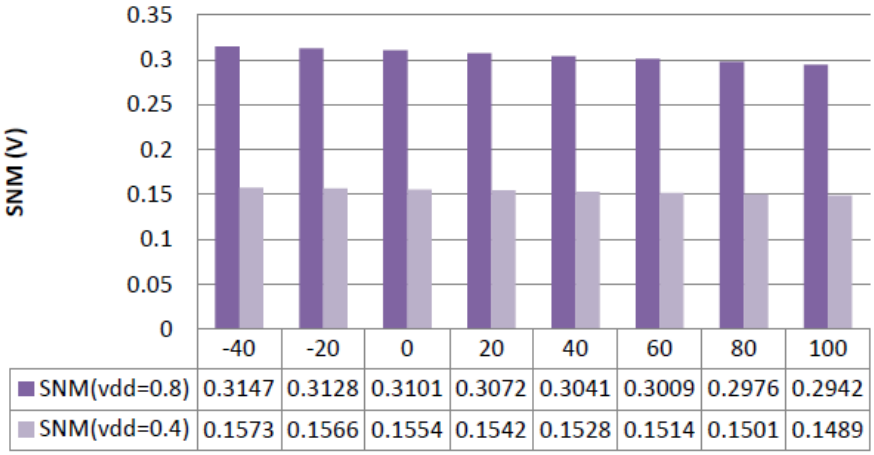
Technology	Vdd (V)	SNM (V)
45nm	0.8	0.2953
	0.4	0.1476
32nm	0.8	0.2950
	0.4	0.1471
22nm	0.8	0.2943
	0.4	0.1467
16nm	0.8	0.2932
	0.4	0.1415

F. Temperature Varying

Although the impact of temperature on SNM is not as large as V_{DD}, the SNM reduced with temperature increasing from -40℃to 100℃. The reason why the higher temperatures have lower SNM in sub-threshold is that the degraded gain in the inverters that results from worse sub-threshold slope and PMOS devices weaken relative to NMOS at higher temperatures (Calhoun et al. 2006). Fig. 5.8 (a) shows SNM versus temperature in sub-threshold, and Fig. 5.8 (b) gives us the SNM vary comparison between V_{DD}=0.8v and V_{DD}=0.4v. It can be seen that the SNM of above-V_{th} (above threshold voltage) varies a little faster than sub-V_{th} as the temperature changes.



(a) Simulated SNM with TEMP varying



(b) SNM varying of V_{DD}=0.8v and V_{DD}=0.4v as TEMP varying

Figure 5.8 SNM versus temperature

5.2.3 Conclusion of Circuit Parameters Affection Sub-threshold Design

・8T sub-threshold design solved the read upset problem and has larger SNM than 6T sub-threshold design.

・Supply voltage V_{DD} and length have a significant impact on SNM. SNM will be larger with supply voltage higher.

・SNM drops as size decreases in the real digital world; we should try to set appropriate CR to ensure SNM is large enough.

・SNM decreases as temperature increases. Therefore, the temperature has an impact on reliability of sub-threshold design.

5. Conclusion

In this thesis, an overview of sub-threshold technology has been introduced firstly, and then the 6T and 8T sub-threshold design to overcome the challenges as mentioned in chapter2 have been improved. The details of 6T and 8T sub-threshold SRAM design including the cell ratio and pullup ration calculation, sense amplifier improvement etc. and working sub-threshold model also have been produced in this thesis. These two sub-thresholds SRAM systems were designed and simulated in 45nm CMOS technology. To compare different LPPTM technology on reliability of sub-threshold SRAM design, 32nm, 22nm and 16nm are also simulated and analysed for calculating Static noise margin (SNM).

SNM as the paramount method to evaluate the stability of the system has been calculated in Hspice and plotted using MATLAB for not only different designs, but also same design under different critical parameters and various predictive technology models (PTMs) technology. We find that SNM will decrease as supply voltage and size of CMOS drops, which means the cell ratio (CR), pullup ratio (CR) and length have an impact on reliability of sub-threshold design. However, when we set the CR and L large enough to meet the maximum SNM, it is necessary to consider fabrication space at the same time. Besides, temperature also influences the stability of the design; higher temperature will contribute lower SNM. In addition, 8T sub-threshold SRAM design solved the read upset problems of 6T sub-threshold SRAM. These critical parameters will have a significant impact on designing a sub-threshold system.

In summary, designing the sub-threshold design and anaysing the reliability of these systems will have significant impact on future research and fabrication. The future work will be introduced in the following chapter.

6. Future Work

Since the read SNM and hold SNM have already been simulated and analysed, the write margin of sub-threshold SRAM design could be tested in the future as write margin also can be used to evaluate the stability of the system.

Besides, this project mainly focuses on one bit SRAM cell design and analysis in one column, and the whole SRAM system can be integrated and simulated for more practical simulation and fabrication. The targeted device for this project is sub-threshold SRAM design and reliability analysis. However, after the sub-threshold SRAM design, the fabrication of a sub-threshold device is one of the main research topics in the future.

Moreover, the design of the sub-threshold SRAM device with larger memory capacity can also be a part of future work.

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Appendix

Part Hspice and MATLAB code have been shown as follows:

1. Hspice Code for 6T Sub-threshold SRAM Design

```
* SRAM 6T WRITE AND READ ANALYSIS
.option nopage nomod post
.tran 1ns 700ns
.param w=90n
.param wn=225n
.param l=45n
.param nvt=0.22v
.param pvt=-0.22v
.param nvt1=0.18v
.param pvt1=-0.22v
VDD1 vdd1 0 0.2
VDD vdd 0 0.5
VPC pc 0 pulse 0 0.5 38ns 1ns 1ns 44ns 80ns
VWL wl 0 pulse 0 0.5 40ns 1ns 1ns 40ns 80ns
VWE we 0 pulse 0 0.5 40ns 1ns 1ns 40ns 160ns
VSAE sae 0 pulse 0 0.5 120ns 1ns 1ns 40ns 160ns
VRE re 0 pulse 0 0.5 122ns 1ns 1ns 40ns 160ns
VIN in 0 pulse 0 0.5 40ns 1ns 1ns 40ns 320ns
**********6T SRAM cell********
M1 vdd1 qb q vdd1       pch1 l='l' w='w'
M2 vdd1 q qb vdd1       pch1 l='l' w='w'
M3 q qb 0 0             nch1 l='l' w='wn'
M4 qb q 0 0             nch1 l='l' w='wn'
M5 bl wl q 0            nch1 l='l' w='w'
M6 blb wl qb 0          nch1 l='l' w='w'
**********Pre-Charge********
M7 vdd pc bl vdd        pch l='l' w='w*10'
M8 vdd pc blb vdd       pch l='l' w='w*10'
**********write driver********
M9 bl we a 0            nch l='l' w='w*10'
M10 blb we b 0          nch l='l' w='w*10'
M11 a in1 0 0           nch l='l' w='w*10'
M12 b in2 0 0           nch l='l' w='w*10'
M13 vdd in in1 vdd      pch l='l' w='w*2'
M14 in1 in 0 0          nch l='l' w='w'
M15 vdd in1 in2 vdd pch l='l' w='w*2'
M16 in2 in1 0 0         nch l='l' w='w'
```

```
**********SA********
M17 vdd outb out vdd    pch l='l' w='w'
M18 vdd out outb vdd    pch l='l' w='w'
M19 out outb e 0        nch l='l' w='w'
M20 outb out e 0        nch l='l' w='w'
M21 e sae 0 0            nch l='l' w='w'
M22 bl re out vdd       nch l='l' w='w*10'
M23 blb re outb vdd     nch l='l' w='w*10'
**********Buffer*********
M24 vdd out out1 vdd    pch l='l' w='w*2'
M25 out1 out 0 0        nch l='l' w='w'
M26 vdd out1 out2 vdd pch l='l' w='w*2'
M27 out2 out1 0 0       nch l='l' w='w'
M28 vdd outb outb1 vdd    pch l='l' w='w*2'
M29 outb1 outb 0 0        nch l='l' w='w'
M30 vdd outb1 outb2 vdd pch l='l' w='w*2'
M31 outb2 outb1 0 0       nch l='l' w='w'
Cblb    blb    0    1pf
Cbl     bl     0    1pf
**********Caculation********
.meas tran Pw1 AVG P(M1) from=40ns to=80ns
.meas tran Pr1 AVG P(M1) from=120ns to=160ns
.meas tran Pw AVG power from=40ns to=80ns
.meas tran Pr AVG power from=120ns to=160ns
*.print tran P(M1) power
*.meas tran tdelay trig v(re) val=0.25 rise=1
*+targ v(out2) val=0.25 rise=1
*.meas tran tread trig v(bl) val=0.45 fall=1
*.+targ v(out2) val=0.45 fall=1
**********Library**********
.model    nch1    nmos    level = 54
+version = 4.0          binunit = 1             paramchk= 1             mobmod    = 0
+capmod = 2            igcmod = 1              igbmod = 1              geomod    = 1
+diomod = 1            rdsmod = 0              rbodymod= 1             rgatemod= 1
+permod = 1            acnqsmod= 0             trnqsmod= 0
+tnom = 27             toxe = 1.4e-009         toxp = 7e-010           toxm = 1.4e-009
+dtox    = 0           epsrox    = 3.9         wint = 5e-009           lint = 1.2e-008
+ll = 0                wl = 0                  lln = 1                 wln = 1
+lw = 0                ww = 0                  lwn = 1                 wwn = 1
+lwl = 0               wwl = 0                 xpart = 0               toxref = 1.4e-009
+vth0 = 'nvt1'         k1 = 0.35               k2 = 0.05               k3 = 0
+k3b = 0               w0 = 2.5e-006           dvt0 = 2.8              dvt1 = 0.52
+dvt2 = -0.032         dvt0w = 0               dvt1w = 0               dvt2w = 0
+dsub = 2              minv = 0.05             voffl = 0               dvtp0 = 1e-007
```

+dvtp1 = 0.05 lpe0 = 5.75e-008 lpeb = 2.3e-010 xj = 2e-008
+ngate = 5e+020 ndep = 2.8e+018 nsd = 1e+020 phin = 0
+cdsc = 0.0002 cdscb = 0 cdscd = 0 cit = 0
+voff = -0.15 nfactor = 1.2 eta0 = 0.15 etab = 0
+vfb = -0.55 u0 = 0.032 ua = 1.6e-010 ub = 1.1e-017
+uc = -3e-011 vsat = 1.1e+005 a0 = 2 ags = 1e-020
+a1 = 0 a2 = 1 b0 = -1e-020 b1 = 0
+keta = 0.04 dwg = 0 dwb = 0 pclm = 0.18
+pdiblc1 = 0.028 pdiblc2 = 0.022 pdiblcb = -0.005 drout = 0.45
+pvag = 1e-020 delta = 0.01 pscbe1 = 8.14e+008 pscbe2 = 1e-007
+fprout = 0.2 pdits = 0.2 pditsd = 0.23 pditsl = 2.3e+006
+rsh = 3 rdsw = 150 rsw = 150 rdw = 150
+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 0
+prwb = 6.8e-011 wr = 1 alpha0 = 0.074 alpha1 = 0.005
+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002
+egidl = 0.8
+aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002
+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004
+eigbinv = 1.1 nigbinv = 3 aigc = 0.012 bigc = 0.0028
+cigc = 0.002 aigsd = 0.012 bigsd = 0.0028 cigsd = 0.002
+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1
+xrcrg1 = 12 xrcrg2 = 5
+cgso = 6.238e-010 cgdo = 6.238e-010 cgbo = 2.56e-011 cgdl = 2.495e-10
+cgsl = 2.495e-10 ckappas = 0.02 ckappad = 0.02 acde = 1
+moin = 15 noff = 0.9 voffcv = 0.02
+kt1 = -0.37 kt1l = 0.0 kt2 = -0.042 ute = -1.5
+ua1 = 1e-009 ub1 = -3.5e-019 uc1 = 0 prt = 0
+at = 53000
+fnoimod = 1 tnoimod = 0
+jss = 0.0001 jsws = 1e-011 jswgs = 1e-010 njs = 1
+ijthsfwd= 0.01 ijthsrev= 0.001 bvs = 10 xjbvs = 1
+jsd = 0.0001 jswd = 1e-011 jswgd = 1e-010 njd = 1
+ijthdfwd= 0.01 ijthdrev= 0.001 bvd = 10 xjbvd = 1
+pbs = 1 cjs = 0.0005 mjs = 0.5 pbsws = 1
+cjsws = 5e-010 mjsws = 0.33 pbswgs = 1 cjswgs = 3e-010
+mjswgs = 0.33 pbd = 1 cjd = 0.0005 mjd = 0.5
+pbswd = 1 cjswd = 5e-010 mjswd = 0.33 pbswgd = 1
+cjswgd = 5e-010 mjswgd = 0.33 tpb = 0.005 tcj = 0.001
+tpbsw = 0.005 tcjsw = 0.001 tpbswg = 0.005 tcjswg = 0.001
+xtis = 3 xtid = 3
…
(Considering the pages, the library of nch and pch are elided here)
…
.end

2. Hspice Code for 8T Sub-threshold SRAM Design

```
* SRAM 8T ANALYSIS
.option nopage nomod post
*.tran 1ns 700ns sweep data=vddtest
*.data vddtest vdd1value
*0.8
*0.7
*0.5
*0.4
*.enddata
.tran 1ns 350ns
.param w=90n
.param wn=225n
.param l=45n
.param nvt=0.62261v
.param pvt=-0.587v
.param nvt1=0.4v
*.param vdd1value=0.8v
VDD1 vdd1 0 0.4
VDD vdd 0 1
VPC pc 0 pulse 0 1 38ns 1ns 1ns 44ns 80ns
VWL wwl 0 pulse 0 1 40ns 1ns 1ns 40ns 160ns
VWE we 0 pulse 0 1 40ns 1ns 1ns 40ns 160ns
VIN in 0 pulse 0 1 40ns 1ns 1ns 40ns 320ns
VRWL rwl 0 pulse 0 1 120ns 1ns 1ns 40ns 160ns
**********8T SRAM cell********
M1 vdd1 qb q vdd1       pch l='l' w='w'
M2 vdd1 q qb vdd1       pch l='l' w='w'
M3 q qb 0 0             nch l='l' w='wn'
M4 qb q 0 0             nch l='l' w='wn'
M5 bl wwl q 0           nch l='l' w='w'
M6 blb wwl qb 0         nch l='l' w='w'
**********Read bit********
M18 rbl rwl out 0       nch l='l' w='w'
M19 out qb 0 0          nch1 l='l' w='w'
**********Pre-Charge********
M7 vdd pc bl vdd        pch l='l' w='w*10'
M8 vdd pc blb vdd       pch l='l' w='w*10'
M21 vdd pc rbl vdd      pch l='l' w='w*10'
**********write driver********
M9 bl we a 0            nch l='l' w='w*10'
M10 blb we b 0          nch l='l' w='w*10'
M11 a in1 0 0           nch l='l' w='w*10'
```

```
M12 b in2 0 0              nch l='l' w='w*10'
M13 vdd in in1 vdd    pch l='l' w='w*2'
M14 in1 in 0 0            nch l='l' w='w'
M15 vdd in1 in2 vdd pch l='l' w='w*2'
M16 in2 in1 0 0          nch l='l' w='w'
*************Inverter*********
M22 vdd out out1 vdd    pch l='l' w='w*2'
M23 out1 out 0 0           nch l='l' w='w'
M24 vdd out1 out2 vdd    pch l='l' w='w*2'
M25 out2 out1 0 0           nch l='l' w='w'
Cblb    blb    0    1pf
Cbl      bl      0    1pf
.meas tran write AVG P(M1) from=40ns to=45ns
.meas tran read AVG P(M1) from=120ns to=125ns
.meas tran leakage AVG I(vdd1) from=80ns to=120ns
*.meas tran tdelay trig v(re) val=0.25 rise=1
*+targ v(out2) val=0.25 rise=1
*.meas tran tread trig v(bl) val=0.45 fall=1
*+targ v(out2) val=0.45 fall=1
***************library*********
…
```

(Considering the pages, the library model for nch,pch and nch1 are elided here)

```
…
.end
```

3. Hspice Code for Calculating 6T Read SNM

```
* SRAM 6T READ SNM ANALYSIS
.option nopage nomod post
.TEMP 20
.param U = 0
.param UL = '-VDD/sqrt(2)'
.param UH = ' VDD/sqrt(2)'
.param cload=0.1pf
.param l=45n
.param wp=90n
.param wa= 90n
.param wn= 225n
.param w=90n
.param nvt=0.22v
.param pvt=-0.22v
.param nvt1=0.18v
.param pvt1=-0.22v
.param vdd=0.5v
```

```
.GLOBAL vdd
VDD vdd 0 0.5
VWL wl 0 0.5
********when reading, use VDD********
.IC V(BL) = 0.5
.IC V(BLB) = 0.5
********6T SRAM cell********
M1 vdd qb qd vdd        pch1 l='l' w='wp'
M2 vdd q qbd vdd        pch1 l='l' w='wp'
M3 qd qb 0 0              nch1 l='l' w='wn'
M4 qbd q 0 0              nch1 l='l' w='wn'
M5 bl wl qd 0             nch1 l='l' w='wa'
M6 blb wl qbd 0           nch1 l='l' w='wa'
Cblb    blb    0    cload
Cbl     bl     0    cload
* use voltage controlled voltage sources (VCVS)
* changing the co-ordinates in 45 degree angle
EQ Q 0 VOL=' 1/sqrt(2)*U + 1/sqrt(2)*V(V1)'
EQB QB 0 VOL='-1/sqrt(2)*U + 1/sqrt(2)*V(V2)'
* inverter characteristics
EV1 V1 0 VOL=' U + sqrt(2)*V(QBD)'
EV2 V2 0 VOL='-U + sqrt(2)*V(QD)'
* take the absolute value for determination of SNM
EVD VD 0 VOL='ABS(V(V1) - V(V2))'
.DC U UL UH 0.01
.PRINT DC V(QD) V(QBD) V(V1) V(V2)
.MEASURE DC MAXVD MAX V(VD)
* measure SNM
.MEASURE DC SNM param='1/sqrt(2)*MAXVD'
*******library*********
…
```

(Considering the pages, the library model for nch,pch and nch1 are elided here)

```
…
.end
```

4. Hspice Code for Calculating 8T Read SNM

```
* SRAM 8T READ SNM ANALYSIS
.option nopage nomod post
.param U = 0
.param UL = '-VDD/sqrt(2)'
.param UH = ' VDD/sqrt(2)'
.param cload=0.1pf
.param l=45n
```

```
.param w=90n
.param nvt=0.52261v
.param pvt=-0.587v
.param nvt1=0.4v
.param vdd=0.8v
.GLOBAL vdd
VDD1 vdd1 0 0.8
VRWL Rwl 0 0.8
VWWL wwl 0 0
*********when reading, use VDD*********
.IC V(BL) = 0.8
.IC V(BLB) = 0.8
.IC V(RBL) = 0.8
*********8T SRAM cell*********
M1 vdd1 qb qd vdd1        pch l='l' w='w'
M2 vdd1 q qbd vdd1      pch l='l' w='w'
M3 qd qb 0 0                nch l='l' w='w*2'
M4 qbd q 0 0                nch l='l' w='w*2'
M5 bl wwl qd 0               nch l='l' w='w'
M6 blb wwl qbd 0           nch l='l' w='w'
*********Read bit*********
M18 rbl rwl out 0          nch l='l' w='w'
M19 out qbd 0 0               nch1 l='l' w='w'
Cblb    blb    0    cload
Cbl      bl      0    cload
********* use voltage controlled voltage sources (VCVS)
*********changing the co-ordinates in 45 degree angle
EQ Q 0 VOL=' 1/sqrt(2)*U + 1/sqrt(2)*V(V1)'
EQB QB 0 VOL='-1/sqrt(2)*U + 1/sqrt(2)*V(V2)'
*********inverter characteristics*********
EV1 V1 0 VOL=' U + sqrt(2)*V(QBD)'
EV2 V2 0 VOL='-U + sqrt(2)*V(QD)'
*********take the absolute value for determination of SNM*********
EVD VD 0 VOL='ABS(V(V1) - V(V2))'
.DC U UL UH 0.01
.PRINT DC V(QD) V(QBD) V(V1) V(V2)
.MEASURE DC MAXVD MAX V(VD)
*********measure SNM*********
.MEASURE DC SNM param='1/sqrt(2)*MAXVD'
********library*********
…
```

(Considering the pages, the library model for nch,pch and nch1 are elided here)

```
…
.end
```

5. Hspice Code Used to Collect 6T Read SNM Data for MATLAB

```
* SRAM 6T READ SNM ANALYSIS
.option nopage nomod post

.param cload=0.1pf
.param l=45n
.param wp=90n
.param wa=90n
.param wn= 225n
.param w=90n
.param nvt=0.22v
.param pvt=-0.22v
.param nvt1=0.18v
.param pvt1=-0.22v
.param vdd=0.5v
.GLOBAL vdd
VDD vdd 0 0.5
VWL wl 0 0.5
********when reading, use VDD*********
VBL bl 0    0.5
VBLB blb 0    0.5
VQB QB 0 0.5
*********6T SRAM cell*********
M1 vdd qb q vdd       pch1 l='l' w='wp'
M2 vdd q qb vdd       pch1 l='l' w='wp'
M3 q qb 0 0             nch1 l='l' w='wn'
M4 qb q 0 0             nch1 l='l' w='wn'
M5 bl wl q 0            nch1 l='l' w='wa'
M6 blb wl qb 0          nch1 l='l' w='wa'
Cblb    blb    0    cload
Cbl     bl     0    cload

  .DC VQB 0 0.5 0.01
  *.prob IQB=par('0-I(VQB)')
  .print dc v(Q)
********library*********
…
(Considering the pages, the library model for nch,pch and nch1 are elided here)
…
.end
```

6. Hspice Code Used to Collect 8T Read SNM Data for MATLAB

```
* SRAM 8T READ SNM ANALYSIS
.option nopage nomod post

.param cload=0.1pf
.param l=45n
.param w=90n
.param wn=225n
.param nvt=0.62261v
.param pvt=-0.587v
.param nvt1=0.4v
.GLOBAL vdd
VDD vdd 0 0.4
VRWL Rwl 0 0.8
VWWL wwl 0 0
******* when reading, use VDD
.IC V(BL) = 0.8
.IC V(BLB) = 0.8
.IC V(RBL) = 0.8
VQB QB 0 0.4
*******8T SRAM cell*******
M1 vdd qb q vdd       pch l='l' w='w'
M2 vdd q qb vdd       pch l='l' w='w'
M3 q qb 0 0             nch l='l' w='wn'
M4 qb q 0 0             nch l='l' w='wn'
M5 bl wwl q 0           nch l='l' w='w'
M6 blb wwl qb 0         nch l='l' w='w'
*******Read bit*******
M18 rbl rwl out 0       nch l='l' w='w'
M19 out qb 0 0           nch1 l='l' w='w'
Cblb   blb   0   cload
Cbl    bl    0   cload

 .DC VQB 0 0.4 10m
 .print dc v(Q)
*******library*********
…
```

(Considering the pages, the library model for nch,pch and nch1 are elided here)

```
…
.end
```

7. MATLAB Code for Plotting SNM Butterfly Picture

```
clear all;
clc;
x=loadsig('sram_read_snm.sw0');
lssig(x);
Q2=evalsig(x,'q');
QB2=evalsig(x,'qb');
plot(Q2,QB2,'y',QB2, Q2,'y')
```