Abstract

The project studies and investigates the characteristic evaluation of CNTFETs. It has two main sections:one is library comparison; another is ACCNT structure analysis.

Firstly,because CNTFET is a most promising device in nanometer realm integrate circuit,library design and analysis are important for future related work in industrial areas. In this project, the whole CNTFET library has been set up. And Stanford CNTFETs model library compare with BSIM4 MOSFET model and PTM MOSFET model library in propagation delay,power consumption and leakage current aspects. BSIM4 model is current existing model,while PTM model is a predictive model. Using these two different kinds of models, the characteristic of CNTFET library has been evaluated with current and future model roundly. Extensive simulations have been studied,which show that CNTFETs library can perform better characteristics than the current MOSFETs and future MOSFETs models. For example,in temperature influence,leakage current,propagation delay,static properties and VTC aspects, CNTFET is superior to MOSFET. Moreover,tubes also influence CNTFET characteristic. More tubes will lead to have less propagation delay. The related simulation study and analysis has been given in this thesis.

Secondly,previous researchers propose a novel approach to increase metallic tube tolerance without removing metallic tubes in CNTFET. This is named ACCNT. The project also focuses on ACCNT structure evaluation and analysis, such as effect on three important parameters(delay,leakage,power) in different ACCNT structure. Moreover,with the popularity of this new design methodology,the analysis on metallic tubes in ACCNT structure looks extremely important. The metallic tubes influence has been studied and researched in this thesis as well.

Accomplished task:

- Analysis of Ion/Ioff ratio in different ACCNT structure,static properties in different input patterns,VTC in CNTFET,temperature influence.
- Building the Stanford CNTFET library(19 logic gates) and comparing with BSIM4,PTM MOSFET library in delay,power and leakage.
- Analysis of tube numbers influence on delay,leakage and power consumption.
- Analysis metallic tube influence on ACCNT structure.
- Design full adder by using ACCNT structure.

Keywords: *CNTFET library, ACCNT, metallic tube tolerance, propagation delay, power consumption, leakage current, tube numbers.*

Declaration

A dissertation submitted to the University of Bristol in accordance with the requirements of the degree of Master of Science in the Faculty of Engineering. It has not been submitted for any other degree or diploma of any examining body. Except where specifically acknowledged, it is all the work of the Author.

Junchen Lu, September 2011

Contents

Library Characterization and Analysis of Carbon Nanotube-Based Logic

September 29, 2011

1 Introduction

With the innovation of products in microelectronic fields,researchers realize the importance of integrated circuit(IC) in different application areas. From our daily life to professional industrial fields,IC design becomes ubiquitous. The IC design involves in many electronic devices which are familiar by people, such as resistors,capacitances and transistors.

In the past,researchers focused on scaling the feature sizes of integrate circuits. This approach was known as a significant method to improve running speed,power dissipation and integration density. In 1965,Gordon Moore's prediction said that the transistor number will have exponentially grown—the number of transistor will double every year[1]. Until a few years ago,this law was still keep. But the situation has been varied recently. Figure1-1 shows the trends of the number of transistor from 1970-2010.

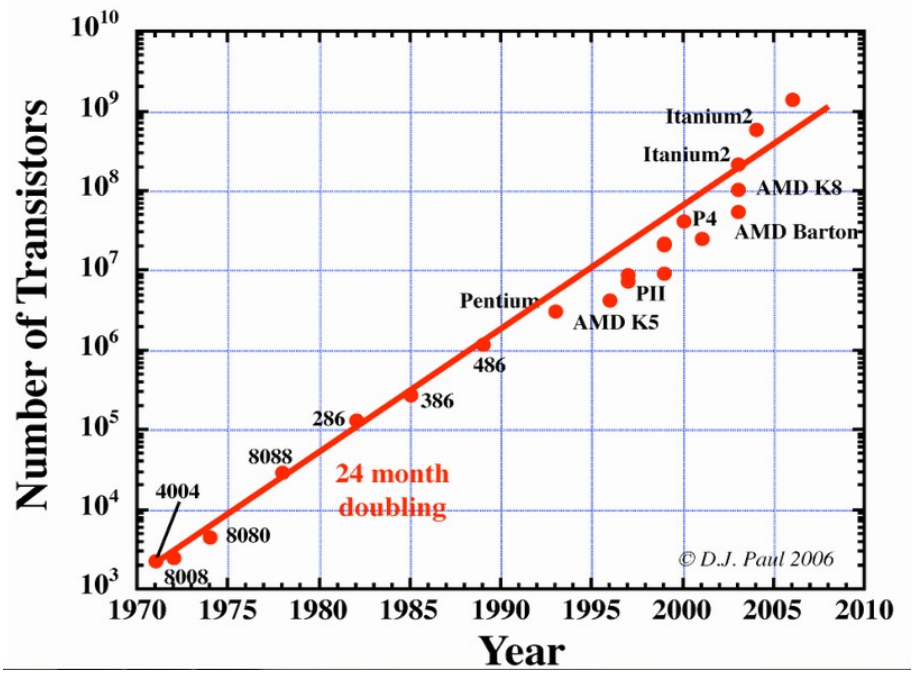


Figure 1-1 Transistor Counts from 1970-2010[2]

Transistor plays a quite important role in the integrate circuit. Nowadays,it is commonly used in chips. Because of the high requirement in circuit function and performance,more and more transistors need to be integrated in same area chips. Current technology already made the small size transistor(nanometer region). After the invention of nano-tube,MOSFET has gone into a submicrion/nano region(below than 65nm). Recently,the smallest size is 16nm in channel length,this nanometer region transistor has been predicted as a potential device.[3].

However,the shrink of channel length in transistor will bring problems. When the physical length of gate is below than 65nm(goes into nanometer region),the approaches of parameter calculation are different from traditional transistors[1]. The reason is that the transfer time of carriers to cross the gate channel is proportional to gate length(Sumit Kumar,2008)[4]. Therefore small gate length would have small gate delay and small interconnection dimension. Although the transistor scaling would cause the reducing delay and low cost,some performance problems still exist which will be described in this project. The smaller the gate length, the harder to obey the MOORE'S LAW which was a rule for transistor development. The figure1-2 shows the change of transistor size in 1990s. Currently,the technology already reach sub-30nm realm.

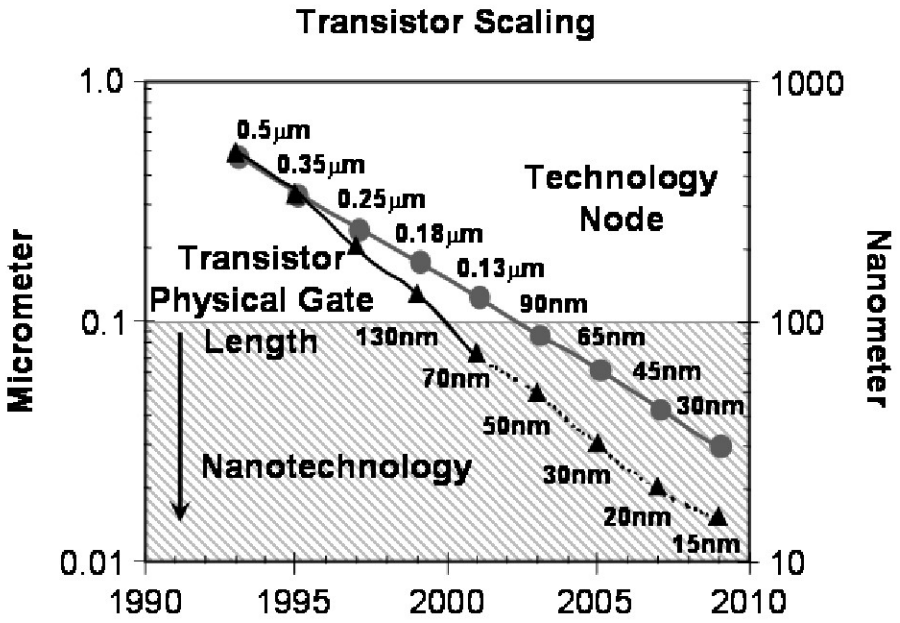


Figure 1-2 Scaling of transistor size in 1990s[5]

Because of the difficulties caused by manufacturing of small size transistor, researchers pay their attention on a new type of field-effect transistor which is named carbon nano-tube field-effect transistor(CNTFET).CNTFETs characterization is similar to MOSFETs and in some behaviors (propagation delay,leakage,power consumption) it is better than MOSFETs.Thus in some areas it can replace traditional MOSFETs. At the same time,lots of improvement are used to receive better features in MOSFET. For example, 16nm and 22nm PTM low-power and high-performance model have been used in 2008. So we can see that nowadays transistors are already go into a nanometer realm.

Due to the high requirement of CNTFETs in the near future,CNTFET technology is one focus in nowadays technology development. Research founds that the chirality of carbon nano-tubes would cause two different tubes:metallic tubes and semiconducting tubes. Semiconducting tubes have better features in gate control,but metallic tubes will cause the out-of control of transistor. So researches on analysis of the tube influence and metallic tube tolerance are important in future development.

This project will focus on the CNTFETs library characterization analysis,the influence of metallic tubes and improved circuit structure.

1.1 Aims and objectives

The main objectives of this project is analysis the characterization of CNTFETs, comparing with conventional MOSFETs (two different models–BSIM4 and PTM), benefits and drawbacks of the new transistor evaluation. The steps are listed at below:

- Basic simulation on single CNTFET,such as ION/IOFF ratio evaluation,static properties,voltage transfer characteristic.
- Using Stanford 32nm CNTFET model to assemble the whole library which contains 19 logic gates,such as inverter,and,aoi21,mux0n,min,flip-flop and so on.
- In same environment parameters, Compare the CNTFETs library with the MOSFETs library(BSIM4 and PTM) in propagation delay, leakage current, temperature and power consumption aspect.
- Evaluating the influence of tube numbers in different CNTFETs logic gates.
- Analysis the structure of ACCNT design,such as the influence of metallic tubes in ACCNT structure and metallic tube tolerance.
- Using ACCNT design methodology to design full-adder.

In each step,extensive simulations need to be done and the simulation results has been analysed.The implementation of project is based on Matlab and Hspice.Hspice can be used to calculate the current or power in certain transistor at the whole circuit and get intuitional figures.

1.2 Structure of thesis

This thesis has seven chapters:

- Introduction presents the challenge in microelectronics and the trend of nowadays transistor.
- Chapter2 introduces the fundamental knowledge of MOSFET and CNTFET. In MOSFET part,the main study will concentrate on MOSFET scaling down,such as the benefits and drawbacks caused by small size MOSFETs.In CNTFETs part, some introduction about the structure of carbon nano-tube and CNTFET will be given. Moreover, the negative of CNTFETs has been shown, and the

approaches to solve this problem in other papers are described in this chapter. At last,writer evaluate the benefits and drawbacks of these two methods(tube configuration and ACCNT design).

- Chapter3 refers to the methodology used in this project. The models used in CNTFET and MOSFET library have been explained.

- Chapter4 is the basic simulation which based on CNTFETs, such as analysis the VTC, temperature influence,Ion/Ioff ratio. Moreover, this chapter includes building the CNTFETs library and comparing with the BSIM4 MOSFETs library and the PTM MOSFETs library, and analysis the influence of tube numbers.

- Chapter5 is related to ACCNT design. Firstly, analysis the metallic tube tolerance of this structure has been evaluated. Metallic tube influence has also been referred in this chapter. But this analysis has been done in an equivalent way. Because the Stanford model used in this project is an ideal model. Finally,Using this structure to design full adder.

- Chapter6, conclusion to CNTFETs library characteristic and ACCNT characteristic.

- Chapter7, future work related to solve the current problems and the aspects which need to be improved.

2 Background

2.1 Background of MOS Field-Effect-Transistors and scaling down of transistor

In this part, a brief introduction of MOS Field-Effect-Transistors(MOSFET) has been given. MOSFET is an important part on wafer. Usually,the MOSFET can be used to make amplifying and switching signals which are common devices in the microelectronics field,such as using in differential amplifier, current mirror. In MOSFET, if a gate voltage existed, a conducting channel between the source and drain terminal can be formed. The difference between NMOSFET and PMOSFET is the different channel type. NMOS has a N-channel between drain and source,while PMOS has a P-channel. The high input voltage will lead to N-MOSFET turn on,while the low input voltage will cause P-MOSFET turn on. MOSFET is the most popular transistor in integrate circuits, and it can replace the place of BJT[1].

With the precise requirements of low leakage,power consumption and propagation delay, some of traditional MOSFETs can not match the desired requirements. New materials have been used to improve the corresponding performances. "the high k dielectric material is used to replace S_iO_2 in gate insulator to receive low power consumption"(quoted from Wikipedia). Moreover, some companies combine the high k dielectric and the metal in gate for 45nm transistors.(cited from Wikipedia)

Because of the high integration requirements and the multi-function implementation,a number of researches have been done on scaling down of transistors. But with the scaling down of transistor size, new problems may appear, such as increased leakage current and large parametric variation[1]. Therefore,a new material which is named Carbon Nano-tube attracts more people's eyes.

2.1.1 Advantages and challenges of transistor scaling down

With the development of technology, the size of transistor is scaling down. The small size transistor has a short channel length. Thus,the equivalent resistance of channel is reduced. The low resistance allows more current through the channel compared with the previous transistor. Although the width of channel influence the equivalent resistance of channel,this problem can be solved easily by reducing the value of unit resistance. Moreover,the scaling down of transistor means reducing the area of gate terminal which can reduce the gate terminal capacitance effectively. It is expected that the fabrication costs per transistor would be reduced. Because the number of transistor per wafer was increased.

But side effects still exist with scaling down of transistor. Producing MOSFETs with channel length less than 1u is a challenge. Because problems such as large gate-oxide leakage,increased influence on interconnect capacitance and process variation would appear.

As the thickness of transistor goes into nanometer level(about 1.2nm),the tunneling effect occurs which would cause large leakage current and power consumption. In order to solve this problem,larger dielectric constant insulators are used in gate-oxide(such as Hafnium and Zirconium). High dielectric constant allows a thicker gate layer while keep high capacitance. Thick gate oxide layer can reduce quantum

tunneling current,so the leakage current would be reduced.(cited from Wikipedia)

The switching speed of logic gate is related to the gate capacitance.The gate capacitance will be reduced with the scaling of the transistor size.Because of the minimizing of transistor, more transistors can be fabricated in same size wafer. So the interconnect capacitance becomes a most important reason in switching speed control.

As the transistors are smaller than before,the probability of process variations would increase. So it would influence the transistor characteristic. This variations make that the designer's work becomes more difficult than before. From the drawbacks of scaling down transistor,we know that traditional transistor can not satisfy current technology demands. So an advanced transistor which is named CNTFET has an exciting future.

2.1.2 Supply voltage and threshold voltage trends on scaling down of Transistor

As the channel length(Lch) scaling down, the supply voltage,threshold voltage,gate-oxide thickness were reduced[6]. The trends are shown in figure at below.In order to keep the active power in a reasonable region, the supply voltage should be decreased in order to limited the short channel effect and hot carrier effect[7].The reasons are explained in Equation2-1.

$$P_{ac} = (C_{sw}{V_{dd}}^2/2)f \tag{2-1}$$

$$P_{dissipation} = I_g V_{dd} \tag{2-2}$$

C_{sw} is total switching capacitance,f is clock frequency,$P_{dissipation}$ is power dissipation, I_g is total gate leakage[6].

In advanced technology, the C_{sw} would be increased. This is because of Moore's Law which allows more transistors can be fabricated in same wafer. Moreover, the clock frequency is higher than before. So the direct way to decrease active power is using relatively low supply voltage. Moreover,the reducing of power supply will reduce the power dissipation at the same time. Equation2-2 shows this reason.

Compare with the supply voltage,the threshold voltage decrease slightly. The reason for this phenomenon is inverse subthreshold slope which is a definition that tells how well it shut off.

$$S = ln(10)\frac{nK_BT}{q} \tag{2-3}$$

So threshold voltage isn't relate with the channel length of transistor. But it would be influenced by the thermally activated diffusion. So the Vth just has a slight reduction. Importantly,the threshold voltage can not less than 0.3-0.4V,because of the extremely high leakage current and large delay caused by the small threshold voltage. Now some methods are used to solve small threshold voltage problem,such as multiple-threshold voltage device, dynamic-threshold devices[8]. The multiple-threshold voltage method let circuit use low threshold voltage to increase speed in critical path,but using high threshold voltage in any other places.

Moreover,the oxide thickness also has been minimized. Because of the relevant direct tunneling, the minimum value is 3nm for silicon oxidation[7]. The changes of Vdd,Vth,gate-oxide thickness are shown in Figure2-1.

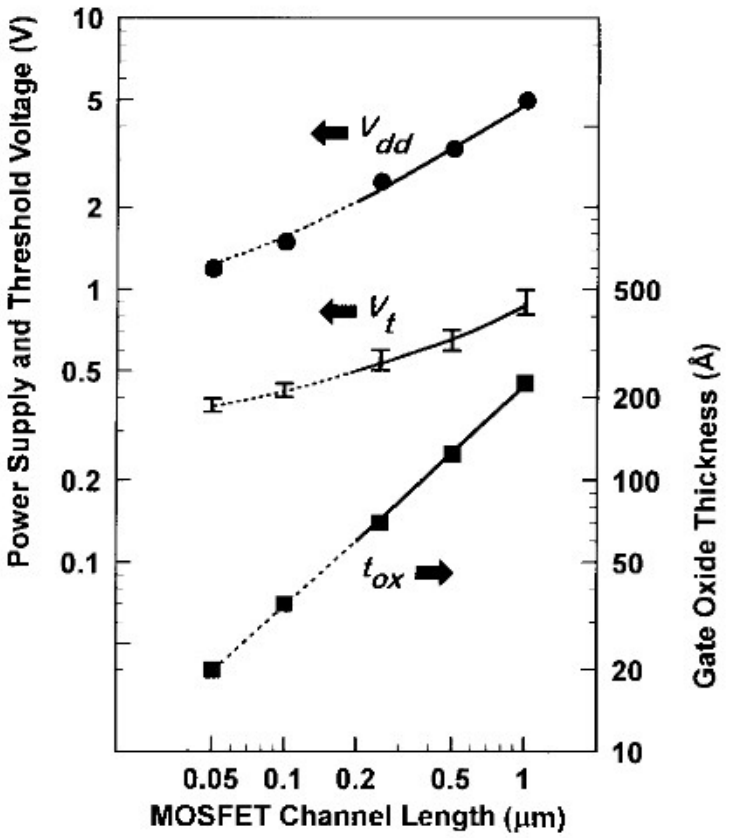


Figure 2-1 Vdd,Vth,gate-oxide thickness(tox) trends in channel length[6]

But when the channel length of transistors are below than 100nm, the ways of reducing supply voltage,oxide thickness and raising doping degree in channel would not bring much improve. Because high doping concentration cause bad transistor performance and carrier confinement,then would cause higher Vth than theoretical value.[7][9][10]

So researching on the new transistor(CNTFET) still looks very important. In next part, writer will compare the Voltage Transfer Characteristic of CNTFET with different channel length MOSFET.

2.2 Background of Carbon Nano-Tube

"MOORE'S LAW states that the number of transistors per integrated circuit doubles every year"(quoted from[5]). After the nanometer size transistor has been achieved, making transistor which smaller than nanometer region will be more difficult than before. Moreover,the MOORE'S LAW becomes hard to obey. The reasons can be divided into two sections. One challenge is to overcome the feature of current MOSFET, such as low delay, low leakage current, low power consumption. extend information processing is another challenge. It can be optimized by using advanced architectural method. Nowadays,new technologies are created to improve the transistor characteristics. Such as, metal-gate/high- stacks[11], strained-Si channels[12], nonplanar fully depleted Tri-gate CMOS transistor architecture[13].

Nowadays,carbon nano-tube field-effect transistors (CNTFETs) utmost attracts researchers to notice. In this paper, a logic circuit CNTFET library will be designed. Moreover, writer will compare the characterization between carbon nano-tube field-effect transistors and conventional transistors in time delay, power consumption, leakage current aspects, then analysis ACCNT design(metallic CNT tolerant design).

"Carbon nano-tubes are carbon's allotropes which are constructed in a cylindrical nano-structure"(quoted from Wikipedia). It has the characteristics of electro conductivity, tensile strength, thermal conductivity, kinetics and nano machines[14]. Due to its unique characteristic,different types of carbon nanotube structure can be formed and all of them would have the unique characterization.

2.2.1 Types of Carbon Nano-Tube

Currently,single-walled nanotubes (SWNT), Multi-walled nanotubes (MWNT), nanotorus are most popular types in CNT field.

The structure of a SWNT looks like its name. It is a cylinder structure which was formed by a single layer of grapheme. The SWNT's diameter is close to 1nm. Compare with the diameter,this structure has a long length which is 1,000,000 times longer than diameter[14]. Because of its unique structure,SWNT has a excellent electric properties. The band gap of SWNT(from 0 to 2eV) is larger than MWNT[14]. The metallic characteristics can be used in transistor. Nowadays,because of the developing manufacturing technology,the price of SWNT is much lower than before. In this project,CNTFET model we used is a single-walled nano-tube structure.

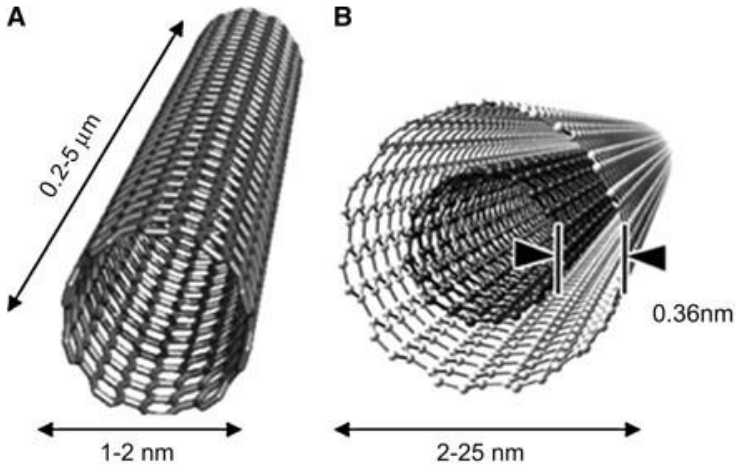


Figure 2-2 SWNT structure(a), MWNT structure(b)(figure from google)

Another structure is Multi-walled nanotubes.This structure has multiple layers of graphite. The behaviors of MWNT are similar to SWNT,but MWNT just show metallic behavior.

Nanotorus is a carbon nanotube which connected into a ring structure. Because of this structure,it has its unique behaviors which are different from other structures,such as magnetic movement and thermal stability[14]. These properties can be used in magnet field.

In different fields, we need to make use of their different characteristics. Based on the behaviors and characteristics,it can be used in different industrial area.

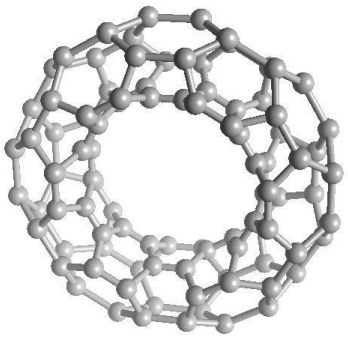


Figure 2-3 Structure of Nanotorus(figure from google)

Figure2-2,2-3 show the structure of these three kinds of carbon nano-tube.

2.2.2 Approaches of production in Carbon Nano-Tube(CNT)

Currently, there are three main approaches to produce the nanotube in large numbers. One is arc discharge, another one is laser ablation, the last one is chemical vapor deposition (CVD)[14].

Arc discharge: In this approach, carbon was put in a heat environment,then the carbon will be evaporated. After these steps,the carbon nanotube was formed. This oldest approach still plays an important role in SWNT and MWNT fabrication. But it has some drawbacks, such as low yield(only 30% tubes can be formed at one time).[15]

Laser ablation: Carbon nanotube was evaporated by a laser in a high temperature room which is filled with reactive gas. Then nano-tubes would be grown on the cooler surfaces of the reactor [15]. Laser ablation is the main approach to generate SWNT. This method can produce about 70 percent nanotubes which have a controllable diameter. The diameter is determined by the temperature. However,this approach is more expensive than others.[15]

Chemical vapor deposition (CVD): A nickel, cobalt or iron substrate put and heated in the reactor,then ammonia gas and carbon gas are injected into the reactor. Finally, carbon nanotubes would grow on the substrate. CVD is the most popular way to generate CNT in commercial field. The benefits of this method is high price/unit ratio and controllable CNT growing place.[15]

2.2.3 Applications of Carbon Nano-Tube

Because of the chirality,strength and flexibility of carbon nanotube, nano-tube can be used in many fields in nowadays.

Transistor The most familiar productions which are made of CNT is the CNTFETs. This transistor has the ability of digital switching using single electrons[16]. Ballistic CNTFET with high-k dielectric gate and ohmic metal contacts has higher Ion than traditional MOSFET(about 20 times higher). But the problem is hard to produce in a great quantity

Electrical cables Because of its metal characteristic, this material can be used in electrical wires. This kind of wires have high conductivity which is much better than cooper.

Solar cells This battery is made of CNT and buckyballs. Buckyballs can not transfer the electrons,but it can attract electrons. Then the sun can stimulate high polymer and help buckyballs attract electrons. At last,nanotube act as a wire to transfer the electrons.

Medical fields It can be used to cure disease. CNT can be inserted in cells which have cancer disease. After being expose to waves,the CNT would be heated and it can kill the surrounding cells.

Others Currently,CNT has been used in lots of field, such as cloth material,space field and so on.

2.3 Carbon Nano-tube Field-Effect Transistors (CNTFETs)

Carbon Nano-tube Field-Effect Transistors(CNTFET) is a new kind of transistor which use array of carbon nano-tube to replace the silicon which used in conventional transistor (MOSFET). CNTFETs(created in 1988) have been proved that it would have a good future in next few years[17].

Currently,four kinds of CNTFET are very popular which are top-gate CNTFETs, back-gate CNTFETs,wrap-around gate CNTFETs and suspended CNTFETs. From the name of different CNTFETs, people can easily understand the structure of them. Top-gate CNTFET is the transistor which has a thin gate on the top of tubes. The benefit of this structure is that it would have high electric field even use a low gate voltage. This is because of the thin gate it has. Back-gate CNTFET which has the gate at bottom(under nanotubes) is the earliest CNTFET. In 2008,wrap-around gate CNTFET has been found[18]. In this structure the gate material wrapped the nanotube. This structure can reduce the leakage current effectively and even increase Ion/Ioff. The last one is suspended CNTFETs. In this device, tubes are suspended over the substrate. It has the benefits of reducing contact between tubes and substrate. But problems still exist, such as lack of material to make this transistor and only used in small size transistor. Because long tubes will curve in the middle,this would be easy to touch the metal contact.

Compare with MOSFET,the I-V characteristics are similar,which also need positive Vg to turn on the N-CNTFET and negative Vg to turn on P-CNTFET. Moreover,

Ids also influence by Vgs and Vds which can be calculated in the equation at below

$$I_{ds} = \frac{2qkT}{\pi * h}[F_0(\frac{U_{SF}}{kT}) - F_0(\frac{U_{DF}}{kT})] \tag{2-4}$$

$$U_{SF} = E_F - q(V_{SC}) \tag{2-5}$$

$$U_{DF} = E_F - q(V_{SC}) - q(V_{DS}) \tag{2-6}$$

Where F_0 is fermi-dirac integral of order 0,k is Boltzmann constant,T is temperature,h is planck constant,V_{DS} is self-consistent voltage[19].

In this project,CNTFET of Stanford model is used.It is a top-gate CNTFETs. The structure of Stanford model are shown at below. CNT chirality in 32nm Stanford model is semiconducting characteristic. So this model is treated as an ideal one.

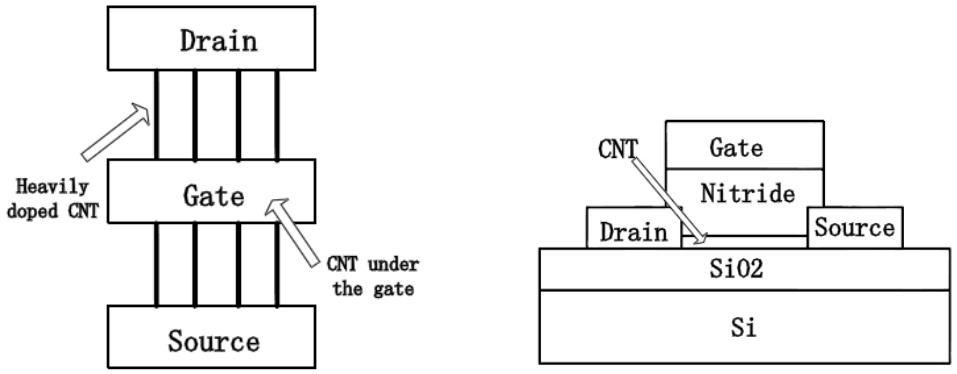


Figure 2-4 CNTFET layout and side view

Compare with the traditional MOSFET,CNTFET act as an ideal substitute in the same field. As the technology scaling down,traditional MOEFET suffered from large parametric variations and increasing leakage current. While CNTFET already deal with the issue,and it has a similar operation principle and device structure. Moreover, it has excellent current capabilities.

In reality,due to different chirality of tubes, metallic tubes would exist in CNTFETs inevitably. Although the metallic characteristic has its benefits when we use it in wires, it would cause the gate of transistor out of control. So the way which is popular at before is removing metallic tubes. New technologies used to generate small percent of metallic tubes are Plasma CVD method and General CVD method. Plasma CVD method would has about 11% metallic and 89±2.3% semiconducting tubes. General CVD method would has about 30% metallic and 70% semiconducting tubes[20]. "A newest Preferential Synthesis can fabricate CNT with just 4% metallic tubes and 96% semiconducting tubes"(Qu, Nano Letters 2008).

Because of the two different kinds of tubes in CNTFET,CNTFET displays different behavior. Metallic CNTs' behavior looks like metallic wires. So it will cause ohmic-short between source and drain. In this situation, the current only depends on the drain-source voltage which would not influenced by the gate voltage. Semiconducting CNTs exhibits a current which controlled by gate-voltage and it would offer high ON-OFF ration(about 10e6)[21].In order to achieve large current drive and small propagation delay, more tubes are needed. So the possibility of metallic tubes

would increase which was not good for the function of CNTFET. The experimental data[21] shows CNTFET with a mix of semiconducting tube and metallic tube has an extremely low on-off ratio. Because the current would not control by gate voltage if metallic tube exist. Then it would cause high OFF current.

In order to solve the problem of metallic tubes,electrical burning and chemical etching methods are used. But other problems would appear by using these methods. Current-induced electrical burning technique is not good for area efficiency, because it needs space of contact between each nano-tube[15]. The theory of chemical etching technique is removing tubes which have a certain tube diameter[15]. Because of the different diameter in metallic tubes,chemical etching method will remove all metallic tubes, also would remove some semiconducting tubes which need to remain.The semiconducting tubes in transistor can reduce the switching time of logic gate,so in CNTFET fabrication we need to protect the semiconducting tubes.

Moreover, another kind of idea has been mentioned,that is changing the transistor structure or circuit structure. Using different tube configuration belongs to the approach of changing transistor structure. Another method is ACCNT design which is a methodology to changing circuit design.

2.3.1 Tube configuration method

Through simulations we know, CNTFET needs more than one tube in single transistor. Because only one tubes would have larger propagation delay,low driving current(related simulation are shown at below).In order to improve the performance of CNTFET, array of CNTs are needed in CNTFET.Large number of array in CNTFET can make variety structure variety. Changing tube configuration is considered as a important resolution.The different configuration of CNT can result different characteristic.

Nowadays, there are four configurations. Shared-tube configuration and parallel-tube configuration already exist in manufacturing field. Transistor-stacking(TrS) and tube-stacking (TuS) configurations are new structures which have been proposed recently.

Shared-tube(ST) configuration use one tube to form a multi-channel structure (four channel are formed in Figure2-5(a)). The configuration has switching source and drain contacts,so the contact numbers are decreased dramatically. Parallel-tube transistors are enable to deliver macroscopic currents which is an important development for future circuit application[22]. Because all transistors share the same tube,transistors would related with each other. So if one part of the tube has metallic characteristic,the whole structure can not be used.

The parallel-tube(PT) configuration use parallel tubes to connect the source and drain terminal in transistor. Fig2-5(b) shows a four parallel tubes structure.

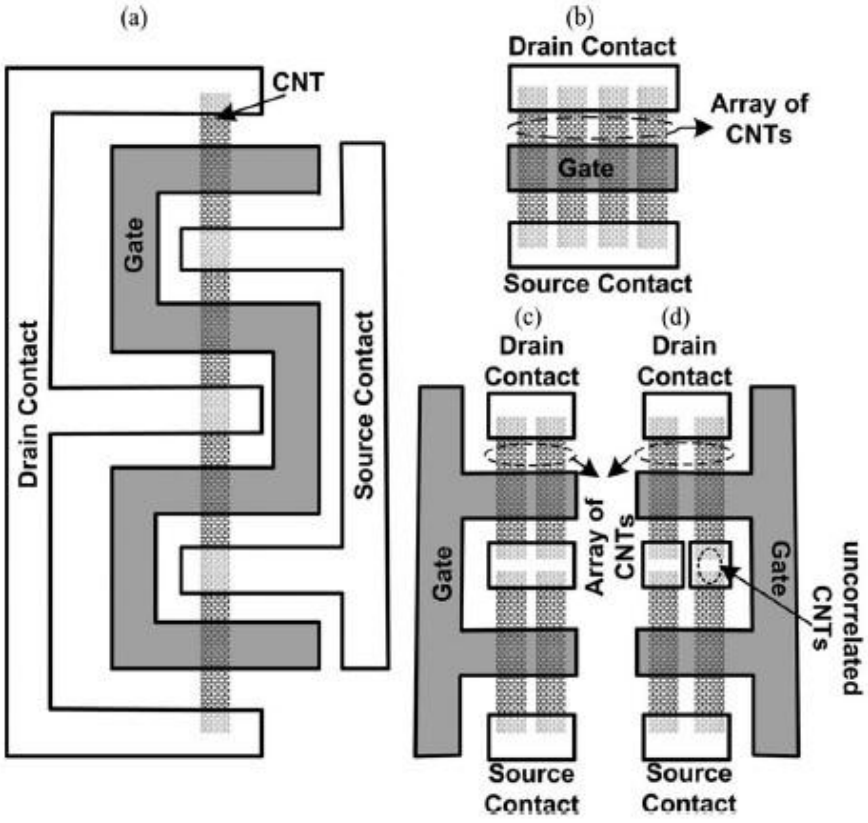


Figure 2-5 Tube configurations (a) ST, (b) PT, (c) TrS, and (d) TuS.(figure from[23])

These two configurations would have low metallic tube tolerance.Because if only one metallic tube grow in the transistor,the channel from source to drain terminal would have a ohmic short. In order to improve this tolerance, new configurations have been proposed. One is Transistor-stacking(TrS) configuration, another one is tube-stacking(TuS) configuration. Both of these method can be used to increase metallic tube tolerance.

Transistor-stacking configuration(TrS) is shown in fig2-5(c). This method use two tubes to connect the source and drain terminal,instead of using only one tube to connect them at before. Then all tubes are stacked on a same internode. Another method is tube-stacking configuration(TuS),which is shown in fig2-5(d).This structure is similar to TrS,the only difference is that all tubes are stacked on different nodes.

However, it has some performance penalties. For example,the channel number would be reduced in TuS and TrS. In PT configuration,one channel need only one tube,but in these new configurations,it would need more than one tube. Moreover,the drive current would be reduced[23]. Misaligned tubes in TrS or TuS is another challenge. Because it would influence the yield of logic gates[23]. Compare these two kinds of configuration, metallic tube tolerance of TuS is higher than TrS, this means the metallic influence on TuS would be small. So it is good to transistor performance. In TuS,short circuit only happened when tubes on same stack are metallic tube. If at least one semiconducting tube exist in each stack,the transistor still can works ap-

propriately. But this structure would need more precise control. Moreover,compare with TrS, TuS will have small leakage current. Because no node share with others nodes[23].

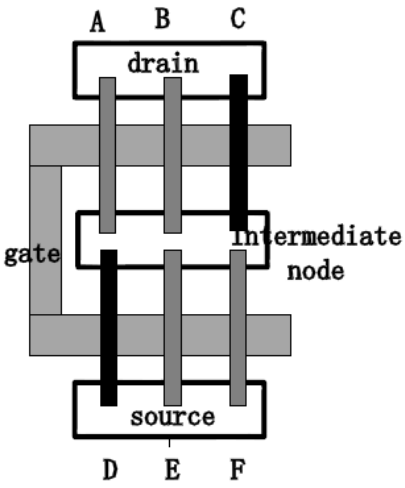


Figure 2-6 TrS configurations,C and D are metallic tubes[23]

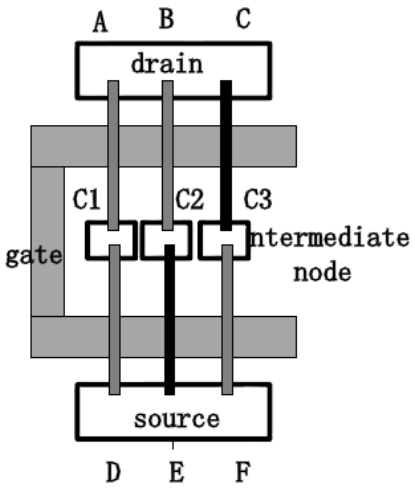


Figure 2-7 TuS configuration,C and E are metallic tubes[23]

From Figure2-6 we know, in TrS if C and D are metallic tubes, the transistor can not work correctly. Because the ohmic short between the source and drain. In TuS, C and D are metallic tubes, this structure still has correct logic function. Because there is no ohmic short between the two terminals(Figure2-7).

Through the explanation at above, we can find TuS has high metallic tube tolerance than TrS.

Area estimation in CNTFET

CNTFET would have more area efficiency than MOSFET in integrate circuit. First, PMOS/NMOS are generated on a piece of n-well/p-well and the distance from source to well should be larger than 6λ(so the distance from PMOS to NMOS is larger than 12λ). Second,in order to receive the same resistance value in NMOS and PMOS, PMOS's width is 2 times wider than NMOS. Because the mobility of holes is lower than mobility of electrons. But size of PCNTFET and NCNTFET are same. Moreover,there is no limitation for the tube distance. So CNTFET can reduce the size of logic circuit.

While compare with the different tube configuration area, we can find that parallel tube configuration would have higher area efficiency than TrS configuration. It is shown in Fig2-6 and Fig2-7. Because of distance between the nodes is 3λ, So TrS take more space than PT[24]. Some details are show in figures at below.

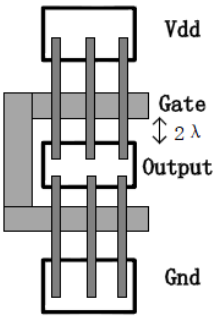


Figure 2-8 Layout of inverters implemented with Parallel Tube

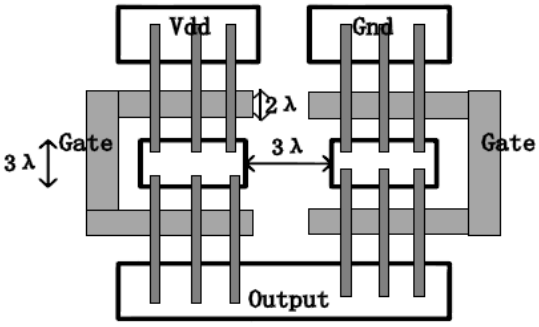


Figure 2-9 Layout of inverters implemented with Transistor Stacking(TrS)

2.3.2 ACCNT design method

As mentioned before, researchers focus on eliminating metallic CNTs, such as electrical burning and etching. But all of these methods can not eliminate all metallic tubes, even some of them would destroy the structure of semiconducting tubes. While ACCNT a new solution is being made[21]. ACCNT is a design method that uses asymmetrically correlated CNT to create CNTFET logic circuit. This can make sure the logic gate function correct by changing the structure of logic gate. Moreover, this design would increase the metallic CNT tolerance without the need of removing metallic tubes.

Asymmetrically correlated carbon nano-tube design(ACCNT) is a solution which don't need to remove and break the metallic tubes from transistor like conventional method. This design methodology can improve the probability of metallic tubes and receive high Ion-Ioff ratio.

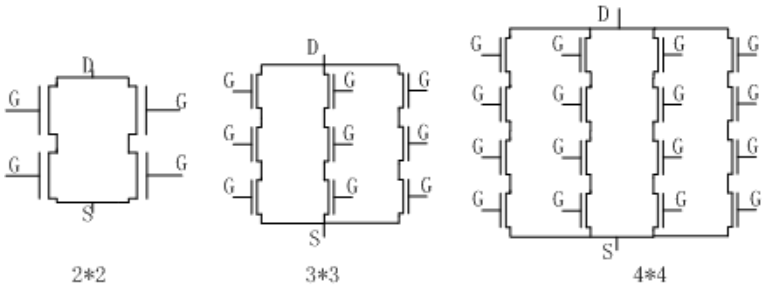


Figure 2-10 ACCNT design structure

In this project, writer use 2*2,3*3 or more CNTFETs ACCNT design to replace one P-CNTFET or N-CNTFET. This design method would not change the logic function of circuit,and it would reduce the influence cause by metallic tubes. In conventional design,if only one metallic tube exist in transistor,this transistor can not work correctly. So the whole function of circuit will be influence. In ACCNT structure,assume the transistor in the first column and first row have metallic tubes,this transistor can be treat as a resistor. But other transistors in the same column still work normally. So the whole function is not changed by only one transistor. Only

when all transistors in the same column have metallic tubes,the logic function would be influenced. But the ratio is much smaller than before.

In fabrication,CNTFETs in horizontal are identical.Because their share same tubes. Thus, if CNTFET1 has 6 tubes and 3 of them are metallic tubes,CNTFET2 and CNTFET3 contain the same number of metallic tubes and semiconducting tubes (structure are shown in Figure2-11). So they are highly correlated. But actually,this is an ideal situation,because the length of tubes are not same in manufacture. This part writer assume no variation exist in the length of CNT, so we can treat the CNTFET in same row are identical.

Then,the transistors in vertical are uncorrelated and different.This can make sure the metallic tubes would not exist in all transistors in same column at the same time. So we can draw the conclusion that CNTFETs in horizontal are same, CNTFETs in vertical are different. The placement of tubes are shown in figure at below(the red one means metallic tube,the blue one means semiconducting tube).

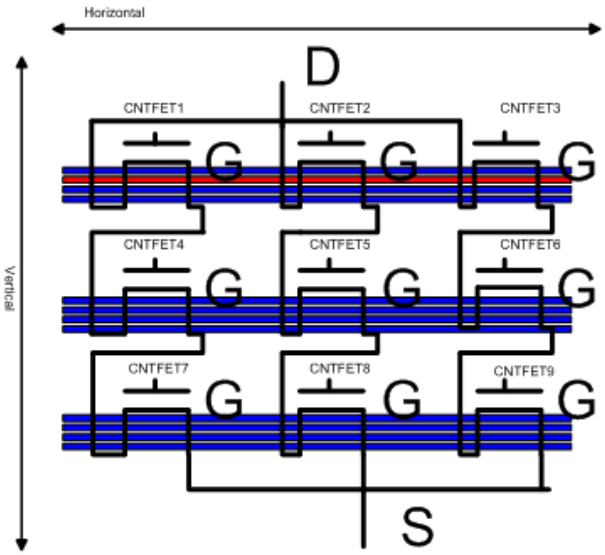


Figure 2-11 ACCNT structure in tubes

Using P_{semi} to represent the probability of a tube is semiconducting.The probability of one CNTFET with N_{cnt} tubes is

$$P_{pertransistor} = (P_{semi})^{N_{CNT}} [21] \tag{2-7}$$

So the probability of having correct logic function/metallic tubes tolerance in one vertical line can be calculated as below:[21]

$$P_{overall} = 1 - (1 - (P_{semi})^{N_{CNT}})^{m_{rows}} \tag{2-8}$$

Where $P_{overall}$ is the probability of metallic tolerance,N_{CNT} is number of tubes in one transistor, m_{rows} is the number of transistor in one column.

From the equation we can see,increase the number of transistor in each column would cause high metallic tolerance.Even it can approach 100% when we use more transistors.

On the other hand,put more transistors in serious would lead to reduced Ion. Because series transistor bring large total resistance which would increase by a factor of transistor number in one column. The reduced drive current may not satisfy the minimum current which can make the circuit works appropriately. In simulation did at before,we found the increased tube numbers(N_{CNT}) would bring large drive current. But from Equation2-8 we can see,it also would degrade metallic CNT tolerance.

In ACCNT design methodology,n columns of series transistors are used to increase the drive current(increased by a factor of column numbers). Moreover,because the transistor in same row share tubes,the total metallic tube tolerance is same with the first column metallic tube tolerance. To sum up,ACCNT design not only increase $P_overall$,but also keep drive current unchanged.

Actually,ACCNT design can be achieved in other structures,such as Parallel structures, Series structures,Weave structure[21]. Parallel structure is shown in figure at below. Further works in this project are base on Parallel rows structure. While in Series structure,transistors in same row put in parallel,then connect each row in series. The Weave structure combine the two above methods together. This approach can share the contacts in adjacent row or column,so the number of contacts reduced. Moreover the capacitance between contacts and space would reduced in this way.The three structures have different benefits. Parallel Structure would have less probability of ohmic short(only when metallic tubes exist in same column). Series Structure would have less probability of open circuit. At last,Weave Structure have the minimum size compare with other. Which one is best would depends on the circuit we need.

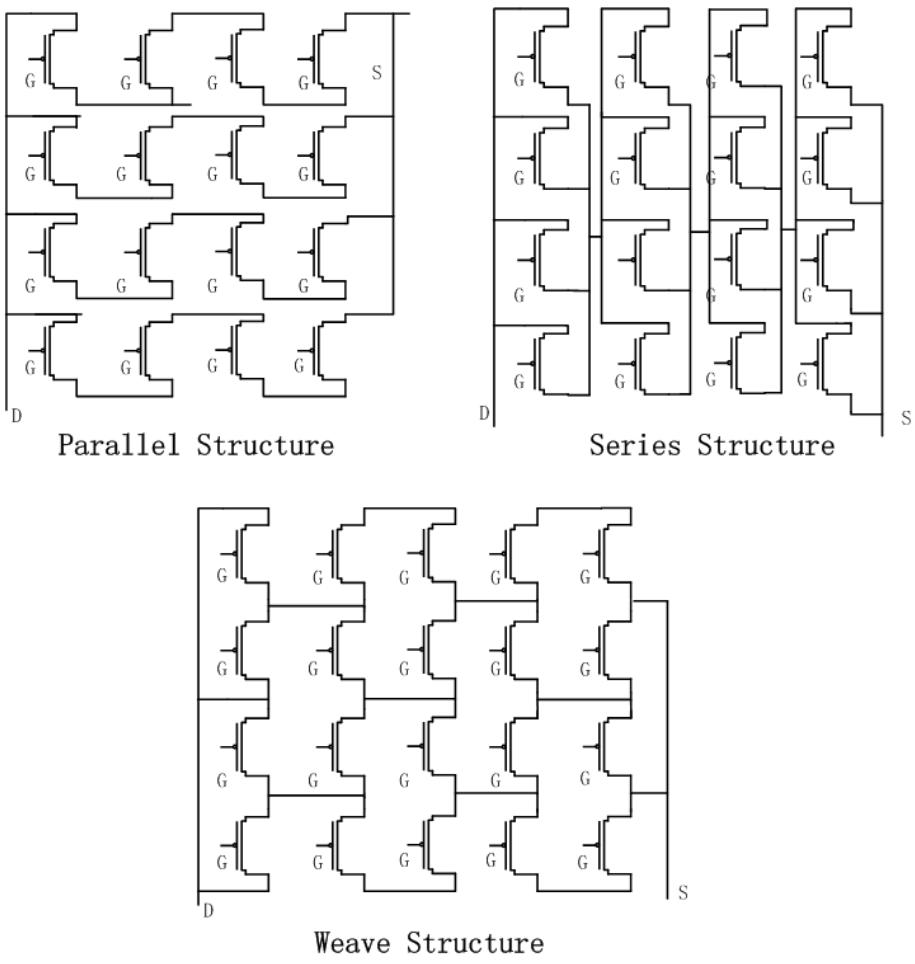


Figure 2-12 ACCNT structure

Ideally,from the structure we know that CNTFETs in the same row have identical characteristic(such as threshold voltage,leakage current), CNTFETs in same column have different characteristic. Because of the identical characteristic in different columns, the number of columns would not influence the total metallic tubes.

But in reality, the above situation is an ideal one. With the increase of series CNTFETs number,the length variation would bring influence to ACCNT structure. Because CNTFETs in same row share the same tubes, more transistors would need long CNT. But sometimes CNT would ended midway,so the number of tubes in same row would be different. This would cause the characteristic difference in same row.

However,it can be improved with the scaling down of transistor. When the channel length is scaling,the tube situation in same row would be same. Because the probability of tube ended midway would decrease. All in all,this is still a potential design method is the near future. The circuit design does not need extra processes,so it is easy to implement. And it do not need to remove the metallic tubes in CNTFET. This ACCNT structure can be used to have high output resistance in analog circuit,and can be used in current mirror as a matched device(Albert Lin,2009).

Incorrect connection of ACCNT structure

As we said at before,the correct connection way is that CNTFETs in same row

are same and CNTFETs in same column are different. One error connection would be connect the transistor which share same tubes in series(connect the row in series at here). In this situation,the semiconducting probability would not be improved. Because transistors in series are same,so the total probability would equal to one transistor probability.[21]

$$P_{overall} = P(atleastonesemitube) = P(allsemitube) = (P_{semi})^{N_{CNT}} \tag{2-9}$$

From equation2-9 we know,it is same with conventional single transistor. In order to have improved metallic tube tolerance,transistor in same column should be different.

Another error connection is that transistor in same row are not share the same tubes. So transistor would be different and would have different number of semiconducting and metallic tubes. The total probability of semiconducting would not only depends on just one column. All columns in the structure would have influence on it,because each row have different probability. The equation can be shown as below:

$$P_{overall} = (1 - (1 - (P_{semi})^{N_{CNT}})^{m_{rows}})^{n_{column}} \tag{2-10}$$

We know the probability would be much smaller than before. Because each column should have one semiconducting tube at least. In this error connection way, getting 99 percent $P_{overall}$ with equal row and column number,at least 59*59 structure is needed. While in a the correct ways,only 41*41 structure is enough(Albert Lin,2009)[21]. So the correct connection method is more area efficiency.

When error connection happens in rows and columns at same time,this would be the worst situation(even worse than the single transistor). The semiconducting probability is:

$$P_{overall} = ((P_{semi})^{N_{CNT}})^{n_{column}} \tag{2-11}$$

3 Methodology

3.1 Models been used in project

3.1.1 CNTFET model

In this project, CNTFETs choose to use 32nm Stanford Model.The Stanford university CNTFET model is a compact, CMOS-like, enhancement-model. Moreover,this model consider some non-ideal situation. For example, extension region effect in source and drain,inter-CNT charge screening effect(from Stanford university nanoelectronics group).

Some limitations exist in Stanford model:the minimum tube number is one.The channel length can not be less than 10nm. If the sub-10nm region is defined in this model, errors would happen. But there is no limitation in the maximum channel length. If the length is larger than 100nm,it would be treat as long-channel transistor. channel length less than 100nm would treat as short-channel device automatically. Moreover,the minimum channel width is 4nm. At last, some kind of parasitics capacitance and resistance are considered,such as source-drain capacitance and gate resistance. Schottky barrier also can be observed in this model. But things need to be taken carefully is that the doping concentration in source/drain extension region should above the first conduction band. Otherwise, error result may be received(from Quick user Guide,2009).

There are two types of model: Stanford CNTFET Model; Uniform-tubes CNTFET Model. The Stanford CNTFET Model consider charge screening effect. Because the tubes place at the margin in different from the tubes place in the middle. In this model,The CNTs at the margin have small charge screening effect. Thus,Comparing with Uniform-tubes CNTFET Model,Stanford CNTFET model is more accurate.

The Uniform-tubes CNTFET Model don't consider charge screening effect. Because it uniform the tubes in transistor.This model have faster speed than the former one.But it would be less accurate than Standard Model.

In order to improve the times of running,the code at below should be included at the beginning of Hspice CNTFET model code.

```
**************************************************
.options POST
.options AUTOSTOP
.options INGOLD=2 DCON=1
.options GSHUNT=1e-12 RMIN=1e-15
.options ABSTOL=1e-5 ABSVDC=1e-4
.options RELTOL=1e-2 RELVDC=1e-2
.options NUMDGT=4 PIVOT=13
.param TEMP=27
**************************************************
```

Then calling relevant model files in code is important. 'CNFET.lib' file contains the CNTFET model which need to be used in this project. '.lib' command(".lib 'CNFET.lib' CNFET") means calling the model file. So all models in 'CNTFET.lib' can be imported. The syntax of CNTFET model is similar to CMOS model. CNTFET model also has four terminals: source drain,gate,substrate. Moreover the port of source and drain can not be changed. The sub terminal can be used as a back gate in

some circuit.But the original gate terminal still need to be used as gate(like gate in MOSFET), because some parameter use an estimated value in substrate terminal.

In Stanford model,if not definition for parameter values, it means using the default value,and all default value in this model can be found in [25].

3.1.2 MOSFET model

In order to compare CNTFET with MOSFET roundly,the 45nm BSIM4(Berkeley Short-Channel IGFET Model) MOSFET model and 45nm PTM(Predictive Technology Model) model have been used.

BSIM4 has been develop based on BSIM3. Because of current technology requirement,transistors need to be smaller than before. But reducing transistor size would bring challenges to transistor,such as non-uniform substrate doping concentration and probabilities to RF application[26]. While this model already solve the problems when transistor scaling into 100nm realm. Moreover,BSIM4 has more advantages than BSIM3[26]:

- In high-frequency and high-speed analog/digital circuit,it has accurate intrinsic input resistance.
- A accurate channel thermal noise model.
- A accurate gate direct tunneling effect.
- It is a gate-induced leakage(drain-source) model(first time in BSIM model).

PTM(Predictive Technology Model) is a precise, predictive and customizable model in future microelectronic technology. This model can be used to predict the characteristic of transistor which would appear in next few years. PTM also has its benefits when channel length go into sub-10nm region. The benefits are list at below(from Predictive Technology Model Website)[**?**]:

- Using a novel way to predict the characteristic which is more physical and scalable.
- Reliability problem and emerging variability already been solved in this model.
- It is a predication of different kinds of transistor.For example,FinFET,Bulk.

3.2 Method on comparing MOSFET and CNTFET on different parts

As we know,the Stanford CNTFET is similar to conventional MOSFET. So methods to design the logic circuit are similar. Writer set the supply voltage to 0.7V which can make sure all models(Stanford CNTFET,BSIM4 MOSFET and PTM MOSFET) work appropriately. And other environment variations(temperature,load capacitance) should set to the same value. This will let they work in same(equivalent) situation. While in MOSFET Wp/Wn=2 use to make same resistance value in pull-up and pull-down network.In CNTFET, PCNTFET/NCNTFET=1, because P/N CNTFET have

same driving current ability. The equivalent parameter in CNTFET is tube numbers. The width of CNTFET increase means the number of tubes increase. In CNTFET library writer set tube=3 as a default value.

The following items demonstrate the method in each part:

- VTC analysis: writer sweep the supply voltage from 0.1V to 0.8V in different channel length MOSFET models. In all of this circuits, 10f capacitance is loaded at the end.Because in practical circuit,loading capacitance would exist, this can let the simulation circuit more close to practical circuit.Finally, compare the transition region of different model,such as the threshold voltage and switching speed from the output waveform.

- Temperature influence analysis: simulations work on different temperature. Then using '.meas' to calculate the average power,delay,Ids in different situation.The calculate result are saved in '.mt' file when it is a transient analysis. When the circuit has a dc analysis,The result will be saved in'.sw' file. Using matlab to generate line chart from the data in Hspice,so we can see the trend easily.

- Static properties analysis: changing the input patterns for NAND gate,then do transient,dc analysis separately.At last,the waveform can show the difference caused by input pattern clearly.

- Ion,Ioff analysis: simulations are based on ACCNT structure transistor, ACCNT structure and tube numbers impact on Ion/Ioff ratio. In this part,we use ACCNT structure from 1*1 to 4*4 and tube numbers from 1 to 4 as an example. As we know,Stanford MOSFET model don't have key word to calculate the Ids in certain transistor.So writer use the current through supply voltage(I(vdd)) to replace it. Ion and Ioff are calculated from Vdd.These two values depend on the in put value. For example,in P-CNTFET ACCNT structure,Ion can be calculated in VDD when all inputs are 0; Ioff can be calculated in VDD when all inputs are 1. In N-CNTFET ACCNT structure,the input values are reverse. At last,make a table to show the trend of Ion/Ioff when the structure and tube number changes.

- Library comparison: the delay calculated in library is not the longest delay in every logic gate. In MOSFET,we can use capacitance and input pattern to find the longest delay.While in CNTFET,due to the different structure,the capacitance influence will be different.So the way to find the longest delay in MOSFET is not useful in CNTFET. In order to compare the same logic gate in different model fairly,delay in same logic gate is the same path delay. The power consumption in here is the mean value in the whole transient analysis. The leakage current is only the subthreshold leakage current which is the main part of total leakage current. In MOSFET, leakage is measured by key word 'lx4(transistor name)' which is the Ids of certain transistor. But in CNTFET,the only method to calculated is using I(vdd). From this we can see the value in MOSFET is more precise than the counterpart of CNTFET. Because some logic gate(such as flip-flop,mux0n,mux1n,min and so on) is build by some subcircuits, and more than one path will be connected with Vdd node. In some

logic gate,there is not input pattern can let all pull-up networks turn off at same time. So it may contains a small part of Ion current in some sub-circuit's pull-up path. All in all the practical value in CNTFETs should be smaller than the calculated value from Hspice simulation in CNTFET model.

3.3 Method on ACCNT analysis

In ACCNT analysis,writer create 1*1,2*2,3*3,4*4,5*5 as sub-circuit separately, each logic will call these sub-circuit.All CNTFETs in this part have 3 semiconducting tubes in each transistor.

The way to analysis the metallic tubes in ACCNT structure is an equivalent method to replace the existence of metallic tubes. High input voltage for N-CNTFET or low input voltage for P-CNTFET are given to the transistor which has metallic tubes. Using this way is that Stanford model do not consider the situation of metallic tubes. And from the characteristic of metallic tubes(ohmic short when metal tube exist in transistor),writer found using input gate voltage to turn on the transistor instead of ohmic short caused by metal is an equivalent way. In ACCNT structure,transistor in same row are same,so if CNTFET in first row and first column has metallic tubes,all transistor in first row will have metallic tubes. It looks like the CNTFETs in first row are turn on. So change the input to let this row of transistor turn on is a convenient method to replace the metallic percentage in ACCNT structure. Different percentage of metallic tubes are controlled by the number of tubes which are turn on.

Full adder in different ACCNT structure is easy to be realized by using ACCNT structure models. ACCNT full adder needs to use ACCNT model to replace the single CNTFET used in conventional design.No other parameters need to be changed in this design.

More details of methodology for building the whole library and ACCNT design/analysis will be explained in each section separately.

4 Result

4.1 Simulation results and assessment on Carbon Nano-tube Field-Effect Transistors (CNTFETs)

The operation principle of CNTFET is similar to traditional CMOS. The output characteristic for P-CNTFET and N-CNTFET are shown in Figure4-1 and Figure4-2.

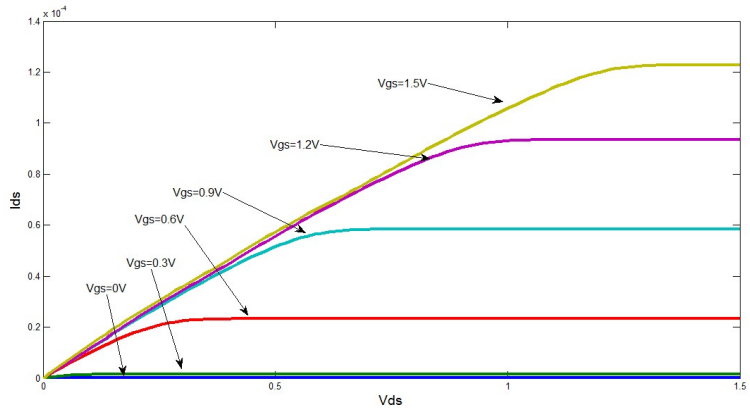


Figure 4-1 Output characteristic of N-type CNTFET as a function of Vgs

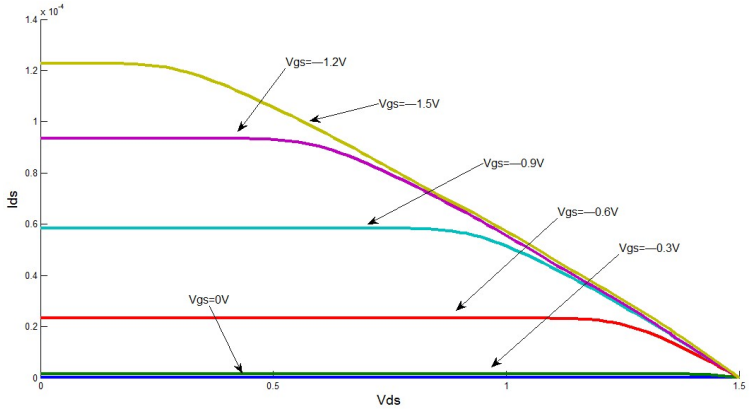


Figure 4-2 Output characteristic of P-type CNTFET as a function of Vgs

In MOSFET,if it is N-MOSFET,the substrate of transistor is P-type,the source and drain terminal is N-type. When the gate voltage increased, holes would driven away from the gates. Then the inversion layer was forming. The n-channel exists between source and drain. When the voltage Vds is large than zero,the current is conducted. The larger the Vgs,the higher the density of electron in inversion layer. So the current between source and drain would increase. If the Vgs is below than threshold voltage,only a small leakage current would exist in the channel.

If it is P-MOSFET, the substrate of transistor is N-type,the source and drain terminal is P-type. When Vgs is negative,the p-channel was forming. If Vgs is much smaller than zero,it will leads to much higher electron density than before. So the current in saturation region is higher than small Vgs. If Vgs is less negative than threshold voltage,the p-channel would disappear.

From the output characteristic of CNTFETs we know, its characterization is similar to MOSFETs. Moreover, in some performance it is superior to CMOS, such as excellent current capabilities, low power delay product, lower average leakage power which would be verified at below. Compare CNTFET with MOSFET, the width ratio of PMOS/NMOS is 2-3 in MOSFET (in this project, PMOS/NMOS=2 has been used), because holes move more slowly than electrons,the PMOS has to be wider to deliver the same current as NMOS. In CNTFET, PCNFET/NCNFET ratio is 1, because NCNFET and PCNFET have same current driving capabilities. Moreover, CNTFET devices are 6x faster than NMOS and 13x faster than PMOS[27]. CNTFET displays a big improvement in time delay which because of the high gain in CNTFET. And its improved performance still preserved in low supply voltage.

4.1.1 Voltage transfer characteristic for CNTFET and MOSFET

In MOSFET,when the channel length is less than 65nm,many side effects appear. In this section,different channel length MOSFETs models(Low-power model) are compared with 32nm Stanford CNTFET model.

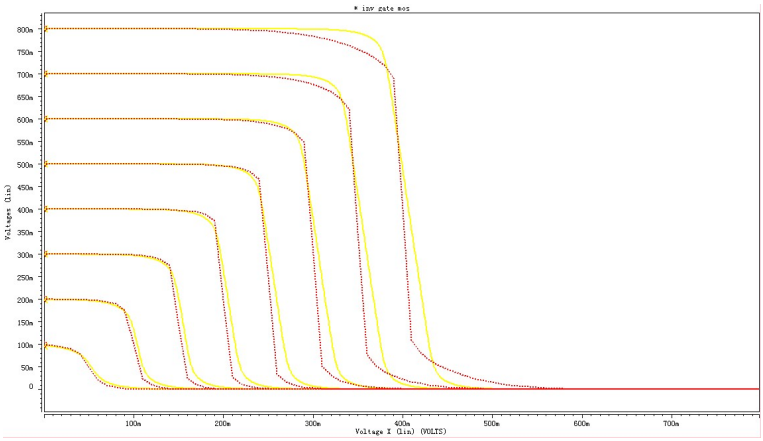


Figure 4-3 Voltage transfer characteristic for 32nm CNTFET and 45nm MOSFET

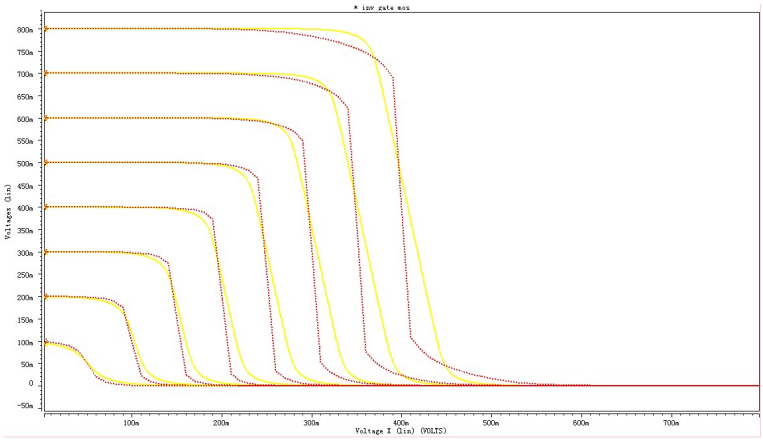


Figure 4-4 Voltage transfer characteristic for 32nm CNTFET and 32nm MOSFET

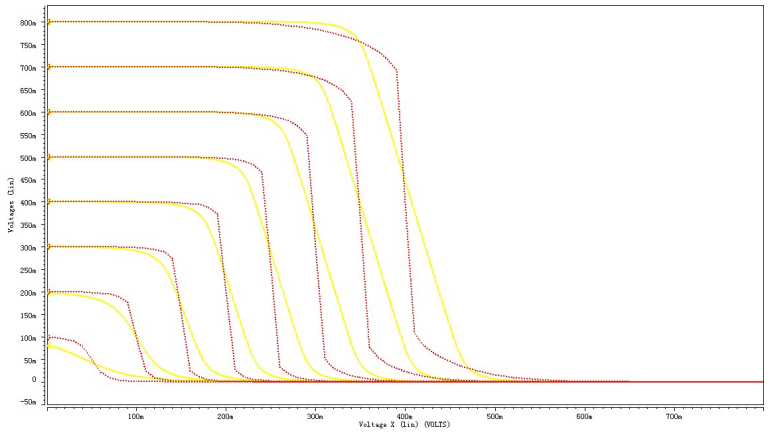


Figure 4-5 Voltage transfer characteristic for 32nm CNTFET and 22nm MOSFET

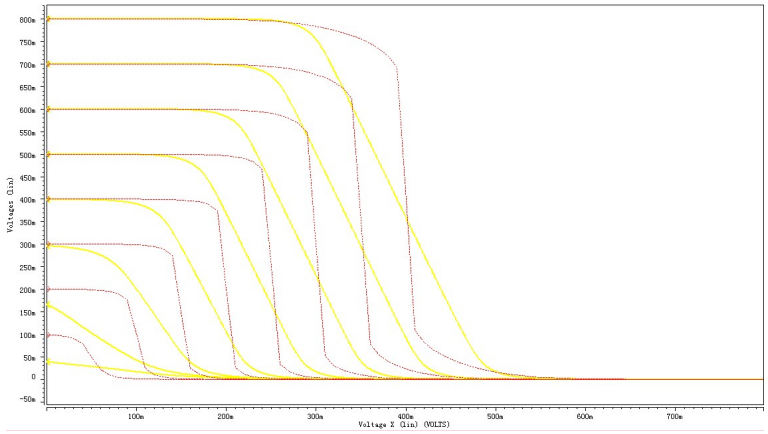


Figure 4-6 Voltage transfer characteristic for 32nm CNTFET and 16nm MOSFET

The X-axis is Vin,Y-axis is Vout.The curves in four figures are the voltage transfer characteristic at different supply voltage(from 0.1V -0.8V). From simulations we know that CNTFET performs a better characteristic than MOSFET in different channel length model. Even when the channel length of MOSFET is 45nm, CNTFETs still have better performance in different supply voltage. The curves in four figures are symmetric. And the inverter logic gates would switch on when Vin=Vdd/2. Moreover, CNTFETs still have a steep curve when the supply voltage is quite small. Compare with the MOSFET of different channel length, the long channel length would has better voltage transfer characteristic. And small size transistor will influenced by short channel effect.

4.1.2 Temperature influence

The environment temperature would affect the transistor in two different aspects: (1)threshold voltage reduced with the rising of temperature.So in same Vgs,the received Ids will larger than before.(2)As the increase of temperature,the majority carrier mobility in channel is degraded. Then the transfer characteristic slope minimized,this will cause low transconductance.

In this part,the circuit simulation temperature sweeps from 0 to 125 degree,then compare 32nm MOSFET with 32nm CNTFET at the delay, power consumption and leakage current.All the simulations are based on inverter logic gate.

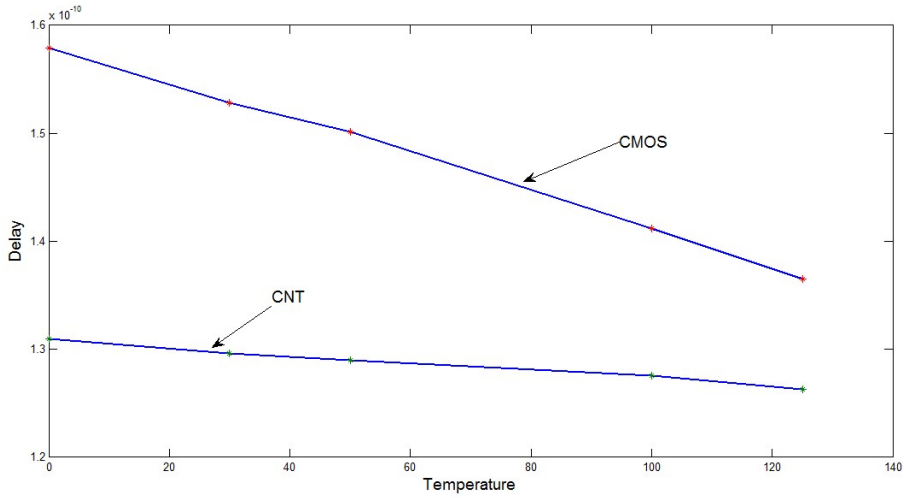


Figure 4-7 Delay characteristic at different temperature

From figur4-7 we can see that the propagation delay of MOSFET and CNTFET inverters are decreased with the rising of temperature. In MOSFET,the delay is 1.579e-10s at zero degree,and it reduce to 1.365e-10s at 125 degree which is still larger than CNTFET in any circuit simulation temperature. In CNTFET, the delay of inverter almost keep constant(about 1.365e-10s). So CNTFET has a better stability in propagation delay.

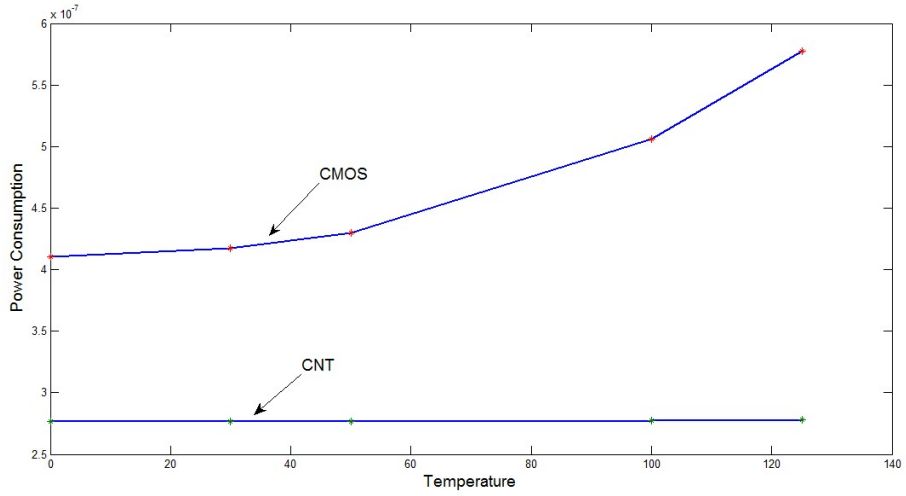


Figure 4-8 Power characteristic at different temperature

With the increase of temperature, the average power consumption for MOSFET increase from 4.106e-07W to 5.775e-07W, because of the increase of leakage current. While CNTFET's leakage keep stable about 2.77e-07W which is good to characterization of CNTFET. So in Figure4-8 we can see that the leakage current in CNTFET is less related with environment temperature.

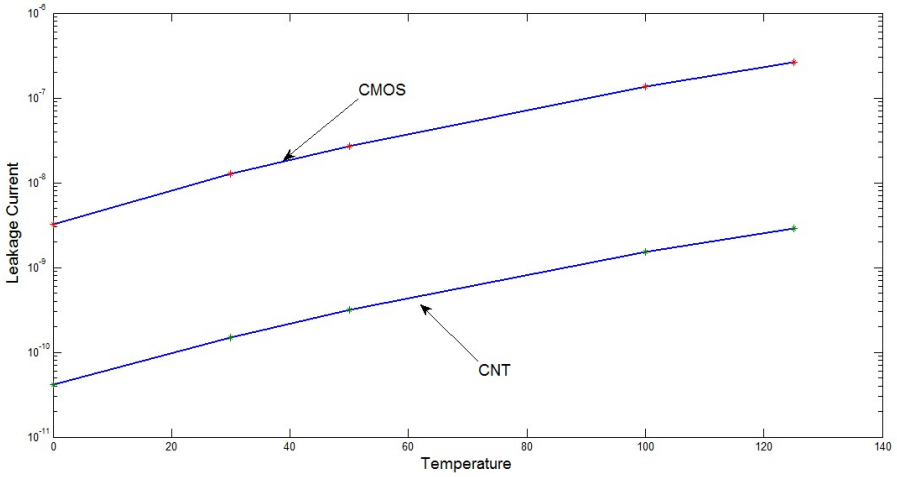


Figure 4-9 Power characteristic at different temperature

In leakage current,CNTFET still performs better characterization than MOSFET,although both of them would increased by high temperature which can be shown in Figure4-9. The leakage current is consist of three parts:subthreshold leakage current, gate-oxide leakage current, band-to-band tunneling leakage current. The subthreshold leakage is the significant part which takes a large percentage. So in Hspice, we test this part of leakage to replace the total leakage. Subthreshold leakage means the current from drain to source when the transistor turn off or the gate voltage less than threshold voltage. In Berkeley Short-Channel IGFET model(BSIM),it is mainly determined by the structure of transistor and working temperature.

$$I_{sub} = I_0 e^{(V_{gs}-V_t)/(nV_T)} \tag{4-1}$$

$$I_0 = u_0 C_{ox}(W/L)V_T^2 e^{1.8} \tag{4-2}$$

C_{ox}-gate-oxide thickness,W-channel width,L-channel length,V_T-thermal voltage,V_t-threshold voltage,n-Threshold amplitude coefficient

4.1.3 Static properties of complementary CMOS and CNT gate

In this part,different input patterns are given to observe delay and voltage transfer characteristic. From Figure4-10 we can see that the switching speed is different in different input patterns. And the table at below shows the delay time in details.

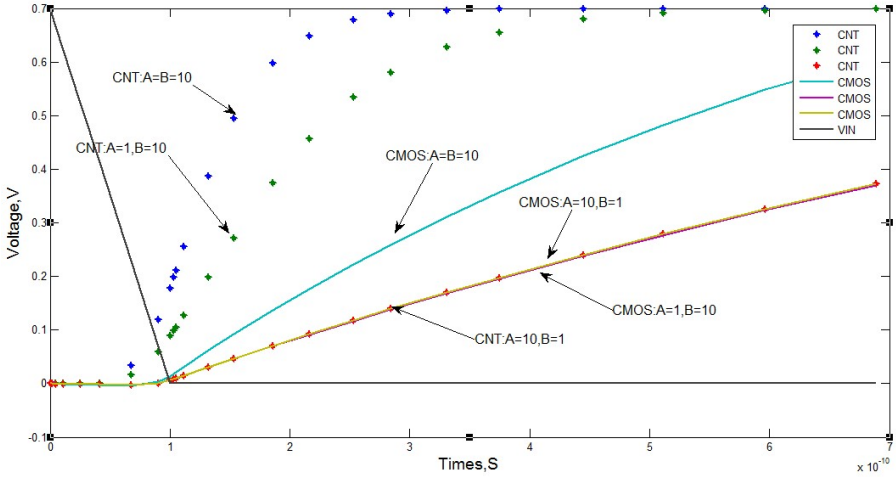
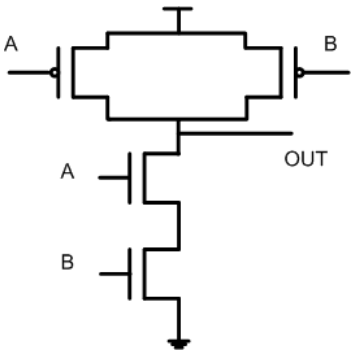


Figure 4-10 Transient analysis of different input patterns



Input Data Pattern	CMOS Delay	CNT Delay
A=B=0->1	1.946e-09	2.613e-10s
A=1,B=0->1	1.934e-09	2.476e-10s
A=0->1,B=1	1.916e-09	2.580e-10s
A=B=1->0	3.178e-10	7.620e-11s
A=1,B=1->0	5.991e-10	1.283e-10s
A=1->0,B=1	5.948e-10	5.948e-10s

Figure 4-11 NAND GATE

Because of charging and discharging capacitance in transistor, the delay depends on input patterns. This part focus on characterization of different input patterns. 32nm PTM-model(Predictive Technology Model) and 32nm Stanford CNTFET model have been used to compare the delay. In MOSFET,width of PMOS/width of NMOS=2. In CNTFET,the number of semiconducting tubes is 3. In order to compare the two kinds of transistor in same surrounding,the supply voltage,load capacitance,temperature,and other environment variable are same.

Figure4-10 shows low-to-high delay for different input patterns,CNTFET is much faster than MOSFET in different input patterns. Only when input is B=1,A=1->0,the delay for CNTFET and MOSFET are same. In other input patterns,the delay in CNTFET improved about 60%-90% than MOSFET. As expected,when two inputs go low at same time,it result in a smallest delay. The worst case in MOSFET depends on which input goes low first. Because different potential in internal node cause the charging and discharging in capacitance. For example, when B=1 and A switch from 1 to 0,the PUN(pull-up network) only need to charge the output node capacitance,because transistor A(NMOS) is turn off. But when A=1 and B switch form 1 to 0,it would need extra time to charge the internal node capacitance and output node capacitance, because transistor A(NMOS) is turn on. So this situation in MOSFET would have larger delay than former one. The simulation result can be show in

table.In MOSFET,when A=1 and B=1->0,it has 5.991e-10s delay which is slightly larger than 5.948e-10(A=1->0,B=1).

In CNTFET,the delay in different input patterns are smaller than counterpart of MOSFET as we expect. The precise values are shown in table at above. So we can get the result that CNTFET performs better delay characterization than MOSFET in same environment variable.

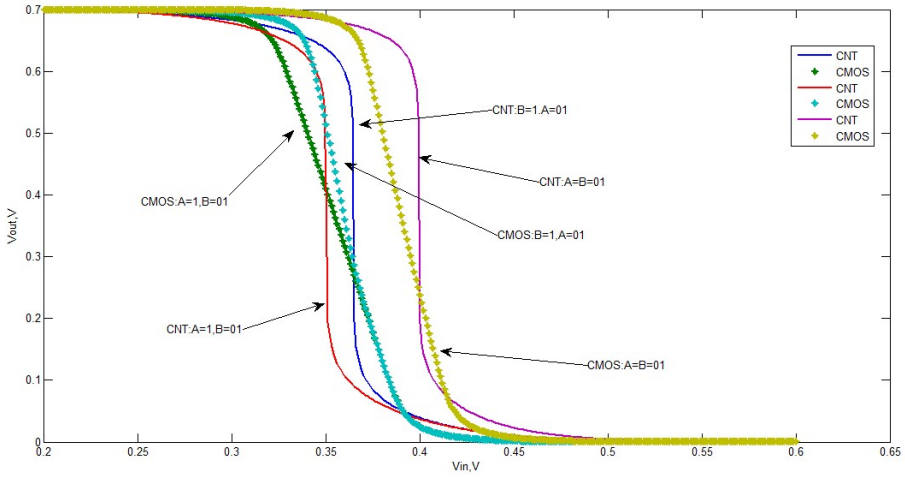


Figure 4-12 VTC of CMOS and CNT nand gate with different input patterns

Figure4-12 shows the voltage transfer characteristic in CNTFET and MOSFET. In this part,writer analysis the pull-down network as an example.As we know,there are three situations which can cause the output goes low.(1)A and B change from 0 to 1 at the same time,(2)A keep constant at 1,B changes from 0 to 1,(3)B keep constant at 1,A changes from 0 to 1. From simulation we know VTC performs a slightly difference when input patterns are different.

In MOSFET,case(1) inputs switch at same time. In the initial value,both P-MOSFETs are turn on,so it would have a strong pull up network which would cause the curve shift right than others. In case(2) and case(3) the pull up networks are weaker than case(1),the curves move left than the former one(show it in figure4-12).As we know the threshold voltage would influence on the internal node voltage(Vnode)

$$V_{thn_A} = V_{th0} + r((\sqrt{|2\Phi_f| + V_{node}}) - \sqrt{|2\Phi_f|})[28] \tag{4-3}$$

$$V_{thn_B} = V_{th0} \tag{4-4}$$

From the two equations we know, in case(2),the A-NMOS is turn on,so the pull down network depends on B-NMOS.The threshold voltage of B is equal to V_{th0} which is less than Vth of A. So the distance of moving left is more than case(3).In case(3),the B-NMOS is turn on,so V_{node} is bigger than zero.From equation4-3 we know that this situation needs high threshold voltage to let the output pull down(the curve in the middle).

In VTC simulation, CNTFET has similar trend but it performs better than MOSFET. The VTC curves of CNTFET are steeper than MOSFET and switch in the middle of the supply voltage(around 0.35V).

4.1.4 Ion Ioff of CNTFET

Because of the unique structure of CNTFET, the features would be influenced by the unique parameter such as the number of tubes in transistor and the probability of metallic tubes. This part writer will focus on the Ion-Ioff ratio in different tube numbers and ACCNT structure(explained in next chapter).

In Hspice, we assume all tubes in transistor are semiconducting tubes. The Ion current of semiconducting tubes is I_{ONs}. The Ioff current of semiconducting tubes is I_{OFFs}. The equations are shown at below(describe in[29])

$$I_{ONs} = \frac{g_{CNT}(V_{DD} - V_{th})}{1 + g_{CNT} L_s \rho_s} \tag{4-5}$$

$$I_{OFFs} = \frac{I_{ONu}\mu}{r}(10^{-V_{th}/S}) \tag{4-6}$$

g_{CNT} - transconductance of CNTFET;ρ_s - resistance per source region length;L_s - CNT length;I_{ONu} is the mean value of I_{ONs};r - the maximum value of Ion/Ioff.

From Equation(4-5),(4-6), the number of tubes increase would cause the decrease of ρ_s which because of the arrange of tubes. So the ON-current would increase,followed by the increase of Ioff. In Hspice simulation,through sweep the number of tubes,we can find the larger tube numbers cause large Ion and Ioff current. The simulation result obeys the result get from the equations.

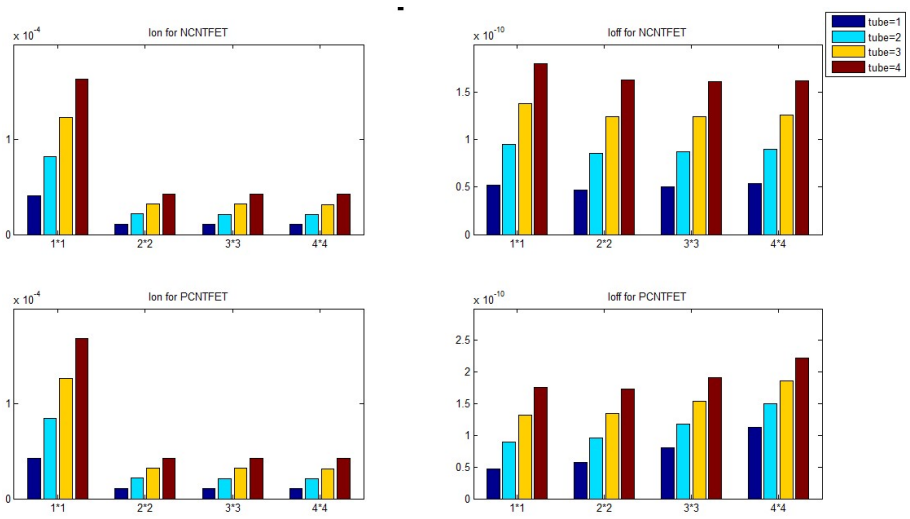


Figure 4-13 Ion Ioff for CNTFET at different accnt structure

In ACCNT structure(described in next chapter),the complicated ACCNT structure cause Ion decrease slightly in P-CNTFET and N-CNTFET. But it is worthwhile to note that the Ioff(leakage) almost keep stable in these two kinds(P-CNTFET and N-CNTFET) of transistor when the structure becomes complicated.The stable leakage current is good for the performance of transistor.

The parameter to evaluate a better characterization of transistor is Ion/Ioff ratio. Table3 is the Ion-Ioff ratio of P/N-CNTFET. As the number of tubes increase,the ratio would increase,which means the Ion is much bigger than Ioff(even can be neglect). Even large number would cause a slightly increase on Ioff, the speed of

Ion increase is higher than the speed of Ioff increase.So Ion/Ioff would larger than before(conventional CNTFET structure). But the drawback is that the ratio would decrease when the more transistors are used(such as 4*4 structure). Although the disadvantage exists in this structure,this structure still has a potential future in next microelectronic development. Because this structure has the advantage of reducing the probability of metallic tubes(high metallic tube tolerance).

N-CNTFET	TUBE=1	TUBE=2	TUBE=3	TUBE=4
1*1	0.785e+6	0.866e+6	0.893e+6	0.907e+6
2*2	0.227e+6	0.251e+6	0.258e+6	0.262e+6
3*3	0.212e+6	0.245e+6	0.257e+6	0.263e+6
4*4	0.196e+6	0.236e+6	0.251e+6	0.255e+6
N-CNTFET	TUBE=1	TUBE=2	TUBE=3	TUBE=4
1*1	0.892e+6	0.941e+6	0.955e+6	0.962e+6
2*2	0.186e+6	0.224e+6	0.238e+6	0.246e+6
3*3	0.132e+6	0.182e+6	0.206e+6	0.221e+6
4*4	0.094e+6	0.075e+6	0.170e+6	0.190e+6

Table4-2 Ion/Ioff ratio for N-CNTFET and P-CNTFET

4.2 Delay,power,leakage of MOSFET and CNTFET

Because of the demand for complicated and fast computation,more and more high density circuits were used. Using traditional MOSFET to reduce the delay, power, leakage was much harder than before.So CNTFET act as a perfect substitute in microelectronic field.In this project the main objective is building the whole library in CNTFET and comparing the CNTFET characteristic with MOSFET.

4.2.1 Calculation of delay,power consumption,leakage current

propagation delay of MOSFET is determined by the parasitic delay and effort delay which was shown in equation at below:

$$D = f + p \tag{4-7}$$

Where f is effort delay or stage effort which depends on the complexity and fan-out of the gate; p is parasitic delay inherent to the gate when no load is attached.From these we know, when load capacitance increased, propagation delay would increase.

While in CNTFET, because of the different structure, the factor which would influence the delay would be slightly different. For example,limited control over the growth of CNT would generate misaligned CNTs, which can lead to incorrect logic function in circuit[30]. Moreover, there are two types of tubes in CNTFET, one is metallic tube; another one is semiconducting tube. Because of the existence of metallic tubes, the ohmic short between source and drain would result in large current in the OFF network. Moreover, reduced static noise margin will be generated, and delay will be influenced.

In complementary circuit, the pull-up network has pull-up delay,the pull-down network has pull-down delay.

$$D_{PU} = K\frac{1}{I_{ON\_PU} - I_{OFF\_PD}} \tag{4-8}$$

where I_{ON_PU} is the total on current of pull-up network,I_{OFF_PD} is the total off current of pull-down network.D_{PU} is the delay of pull up network.

$$D_{PD} = K\frac{1}{I_{ON\_PD} - I_{OFF\_PU}} \tag{4-9}$$

where I_{ON_PD} is the total on current of pull-down network,I_{OFF_PU} is the total off current of pull-up network.D_{PD} is the delay of pull down network. The delay of complementary circuit is the biggest one(equation cited from[31]).

$$D_g = max(D_{PU}, D_{PD}) \tag{4-10}$$

So from the above description,the delay of logic gate would influenced by Ion and Ioff of the PDN and PUN.

Power consumption was a secondary consideration behind speed and area in microelectronic technology. It is another important part to measure the transistor performance. As the transistor number and frequency increased,power consumption would increase dramatically.

In CMOS,the total power consumption can be divided into four parts:P_D,P_{SC},P_S and P_G[32].

$$P_T = P_D + P_{SC} + P_S + P_G \tag{4-11}$$

P_D - dynamic power;P_{SC} - short-circuit power;P_S - static power;P_G - gate leakage power. P_D is caused by subthreshold conduction through OFF transistor,tunneling current, contention current in rationed circuit.While P_S was mainly due to charging and discharging of load capacitance[33].

$$P_D = \alpha(C * f * {V_{DD}}^2) \tag{4-12}$$

$$P_{SC} \approx (0.15 * P_D) \tag{4-13}$$

$$P_S = I_{off} * V_{DD} \tag{4-14}$$

$$P_G = I_g * V_{DD} \tag{4-15}$$

where C is the load capacitance;α is activity factor;f is clock frequency;I_g is the gate leakage.The ways of power calculation still can be used in CNTFET logic circuit.In this project, average power consumption was calculated in both models.

Leakage Current The leakage current of CNTFET would depends on the tube diameter and supply voltage.Beacuse these two parameter would influence the band gap of carbon nano-tubes and band-to-band tunneling.

4.2.2 Load capacitance influence on BSIM4 MOSFET model and Stanford CNTFET model

In MOSFET,the load capacitance would bring a significant influence in propagation delay,power consumption and leakage current.While in CNTFET,no full-scale research did on the influence of load capacitance and building the whole library systematically.So one of main objectives is building the CNTFET library and analysis the characterization of it.

In this part,writer use BSIM4 MOSFET model to compare with Stanford CNTFET model.

Delay of BSIM4 MOSFET model and Stanford CNTFET model library with different load

In MOSFET,the load capacitance would influence the propagation delay which writer already mentioned at before.The two figures are show the propagation delay when the load capacitance is 10f and when no load capacitance.The measured delay in this part is not the longest delay in each logic gate. But the delay in same logic function,same path delay have been measured.

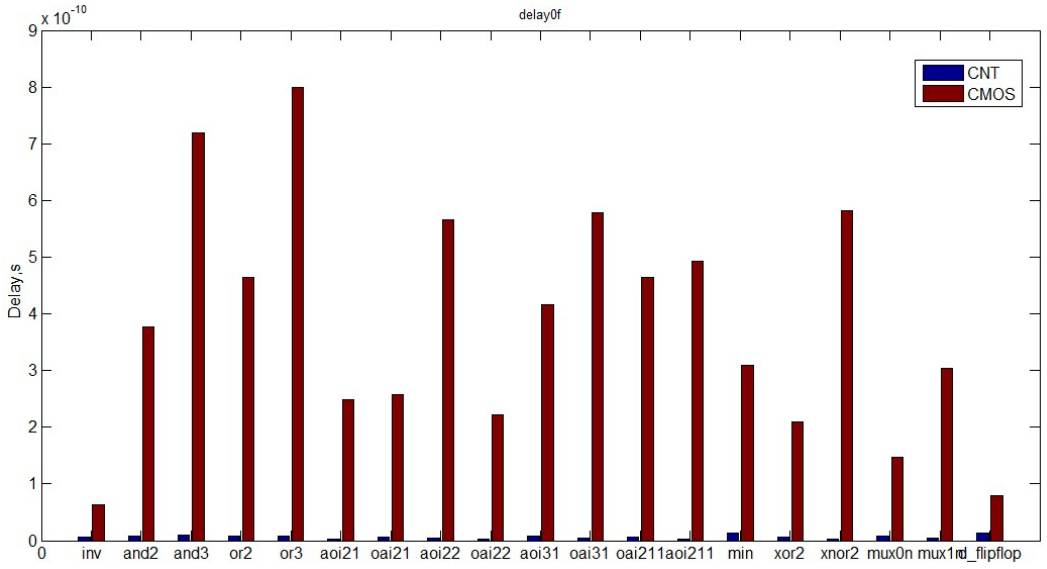


Figure 4-14 Delay for BSIM4 MOSFET and CNTFET-0f

Without load capacitance,the delay of the whole library logic gates are relatively small. MOSFET almost keep around 10^9, while CNTFET only about 10^12 10^11(data result from Hspice simulation)which is about 100-1000 times smaller than MOSFET.

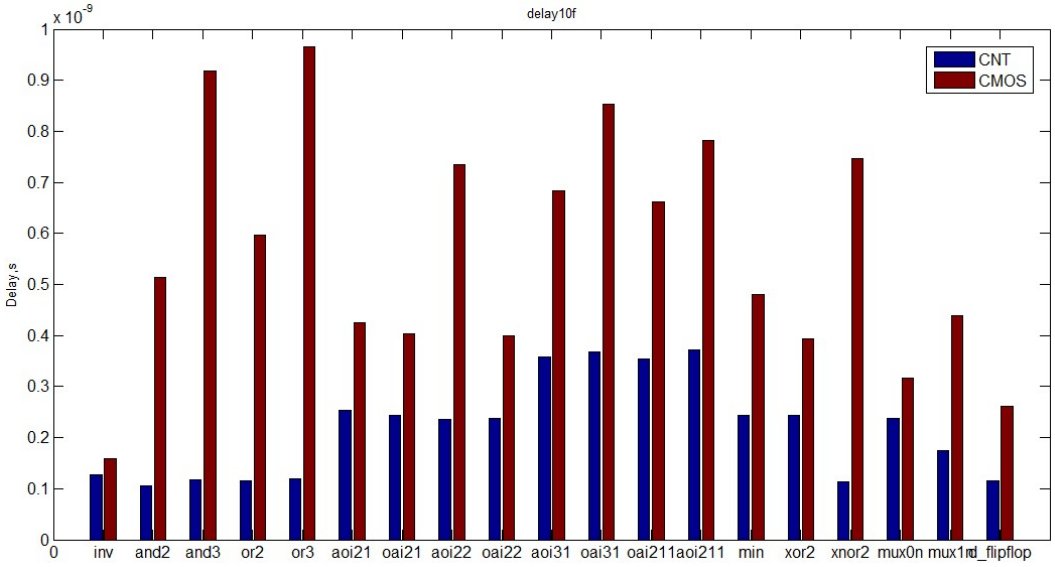


Figure 4-15 Delay for BSIM4 MOSFET and CNTFET-10f

When the load capacitance increased,the delay for both models are increase.But CNTFETs are still much faster than MOSFET which can be show in Figure4-15. In 'and gate','or gate', the improvement are significant.

Power of BSIM4 MOSFET model and Stanford CNTFET model library with different load

In this part,writer calculate the average power consumption in the two models.In order to compare it in same situation,using the same supply voltage, input pulse, temperature and other environment parameters to make sure it can be compared fairly. As we know,the input patterns would influence the power consumption,because the different Ion and leakage current would cause different power conusmption. So in same logic gate,the input pulses are same.

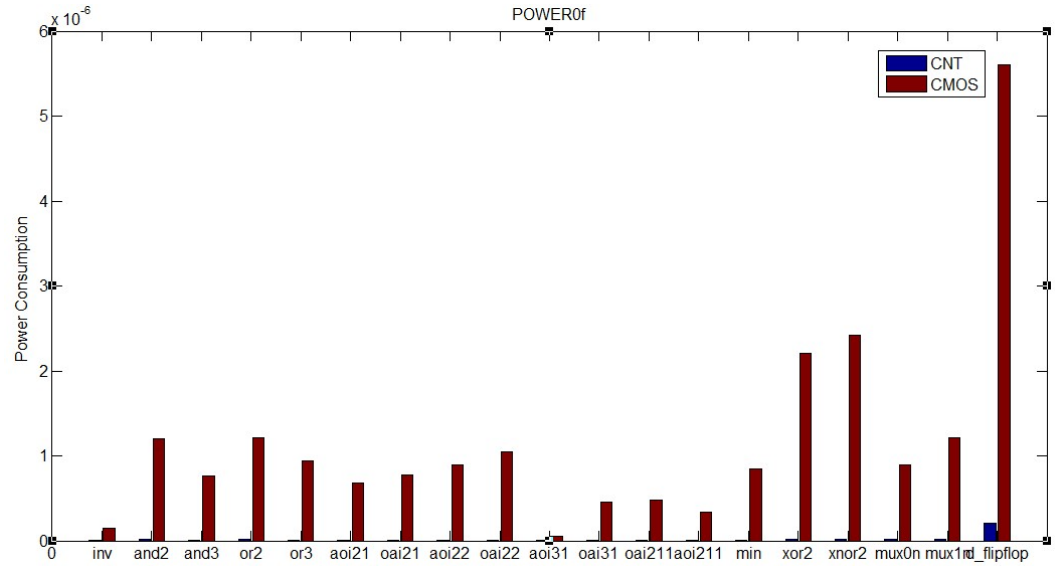


Figure 4-16 Power for BSIM4 MOSFET and CNTFET-0f

Through analysis we can see that the average CNTFET power consumption almost 100 times smaller than MOSFET in the whole library. Even when the circuit load 10f capacitance at the end, both of their power consumption would increase, but the improvement in CNTFET library still exist(show it in Figure4-17).

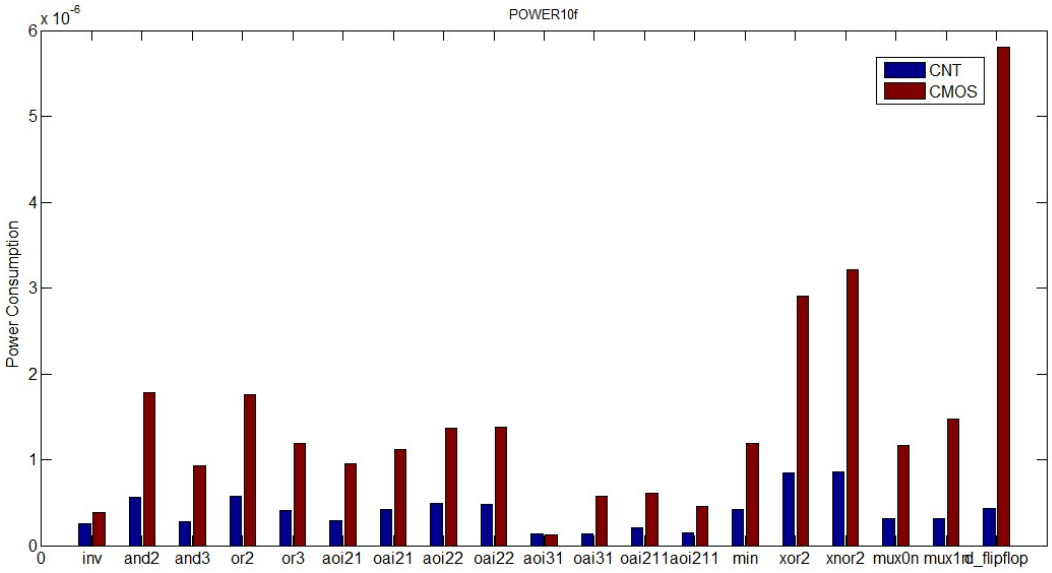


Figure 4-17 Power for BSIM4 MOSFET and CNTFET-10f

Further simulations also show the low power characterization,such as loading 100f capacitance.The significant benefit it has can be used in lots of microelectronic fields which need low power dissipation.

Leakage of MOSFET model and CNTFET model library

This project we only consider the main leakage current–subthreshold leakage.In BSIM4, using the key word 'lx4(transistor name)' to get the value of Ids.So we can calculate all the transistor which is off to get the total leakage current. But in Stanford CNTFET,no key words have been given to calculate the Ids. So using I_{vdd}(current through supply voltage) to replace Ids. The experiment data of leakage current it CNTFET would be larger than practical value.Because other currents are calculate in it.For example,in flip-flop,this kind of logic circuit is consisted of sub-circuits.In this circuit,no input pattern existed to let all transistors in pull-up network turn off.

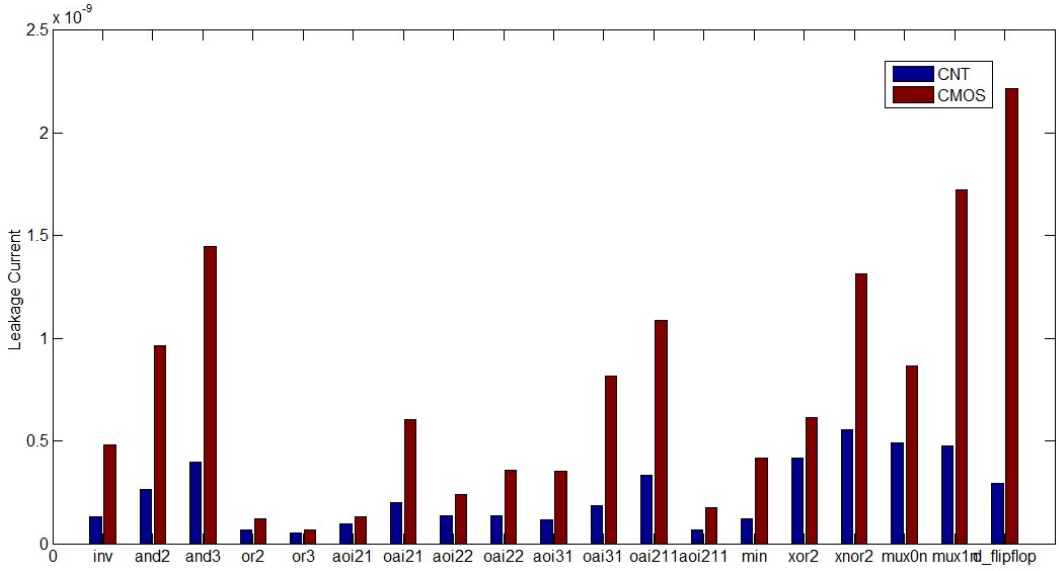


Figure 4-18 Leakage for MOSFET and CNTFET

The result shows CNTFETs have a small leakage current.Actually,the leakage characterization for CNTFET would be better than the figure shows.

After simulation in Stanford CNTFET library and BSIM4 library,we found that Stanford CNTFET has better characteristic in delay,power consumption,leakage current.When the load capacitance exist,these advantages still exist.

4.2.3 Load capacitance influence on PTM MOSFET model and Stanford CNTFET model

PTM MOSFET model is a predictive model. In this part we use 45nm channel length PTM model. This model is an improved one which has less delay,power consumption,leakage current than 45nm BSIM4 model we used at before.

Delay of VTL MOSFET model and Stanford CNTFET model library with different load

From figure4-19 we know,CNTFET library which without load capacitance still has less delay than PTM model,although PTM is an improved model in these parameters.

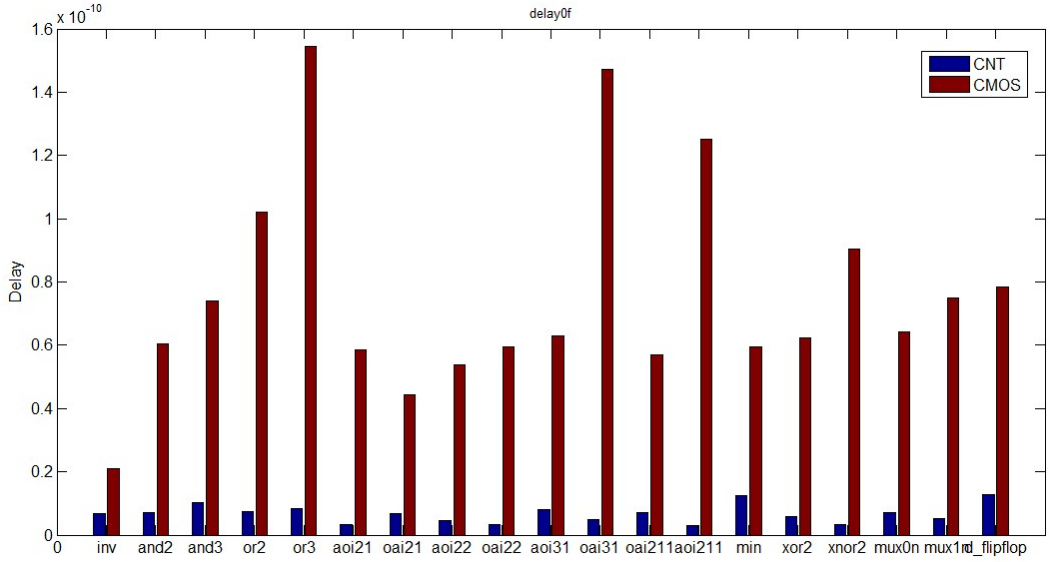


Figure 4-19 Delay for PTM MOSFET and Stanford CNTFET-0f

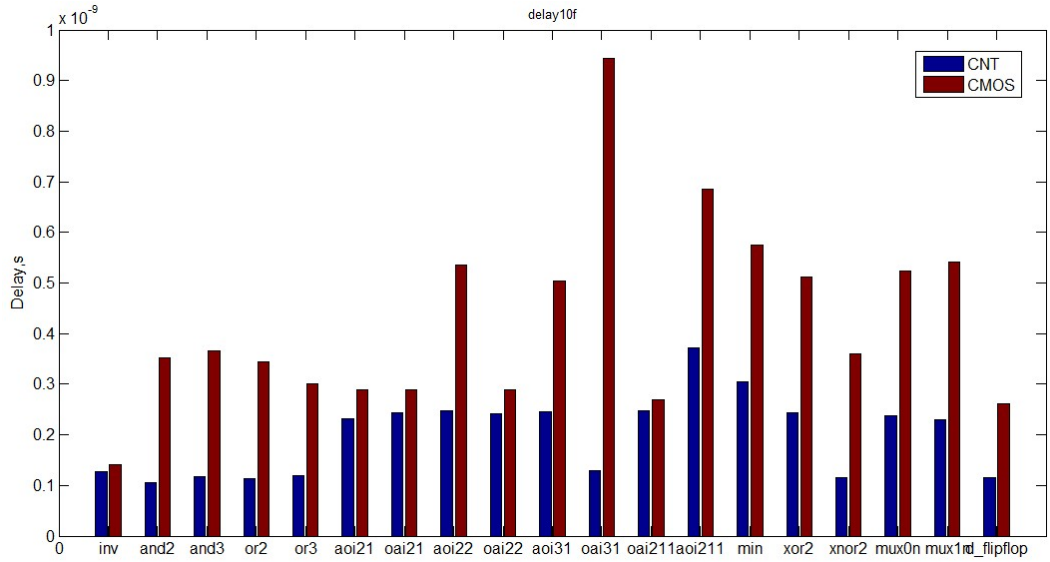


Figure 4-20 Delay for PTM MOSFET and Stanford CNTFET-10f

As the load capacitance increase to 10f in each logic gate. The delay for both two models are increased. But CNTFET model always perform slightly better characteristic in propagation delay than PTM MOSFET model. Compare Figure4-20 with Figure4-15,the delay for PTM low power model improves a lot than BSIM4 model.Although it is a improved model, its delay characteristic still inferior to CNTFET model.

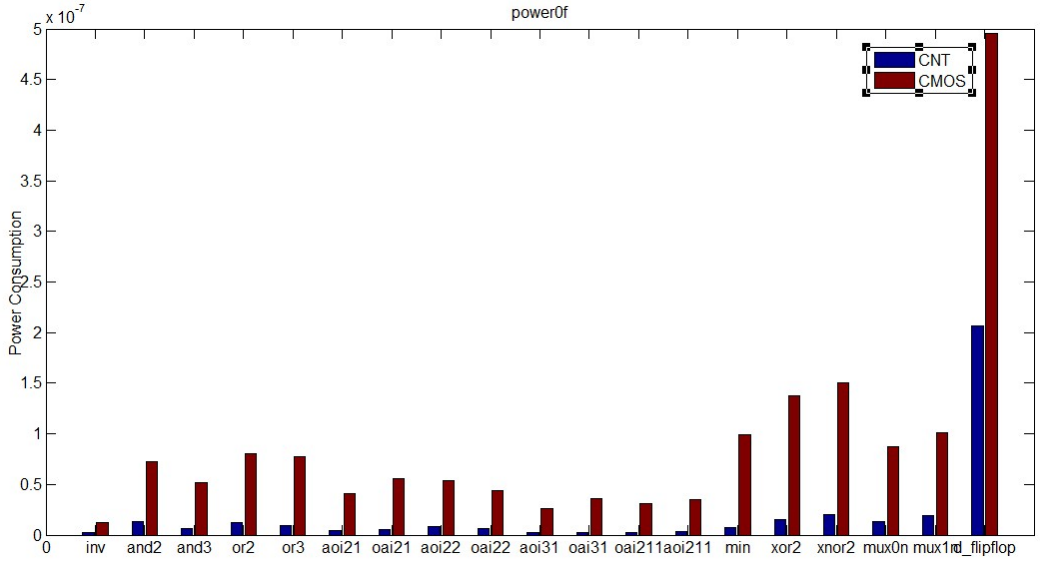


Figure 4-21 Power for PTM MOSFET and Stanford CNTFET-0f

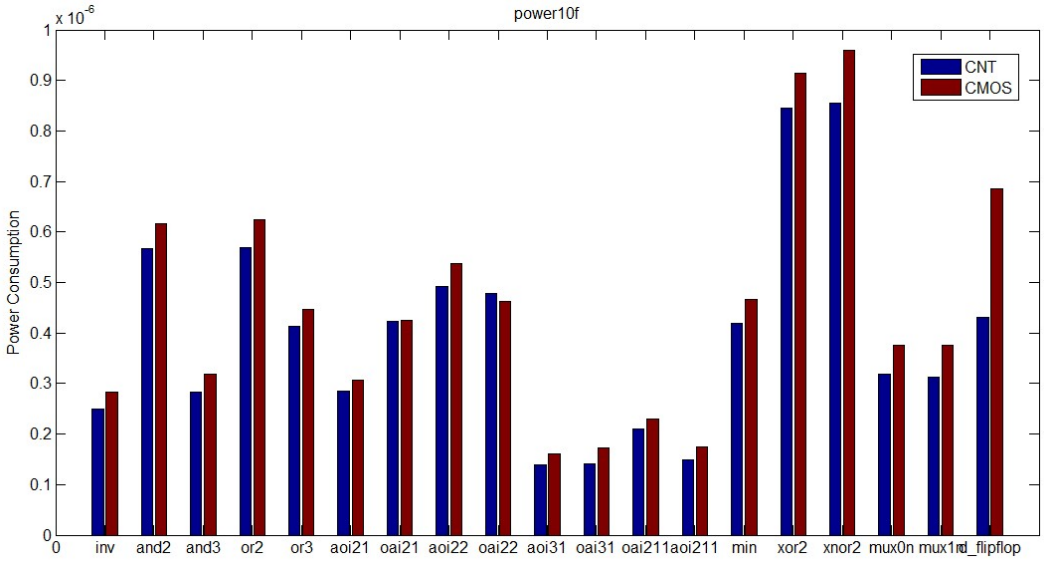


Figure 4-22 Power for PTM MOSFET and Stanford CNTFET-10f

power of VTL MOSFET model and Stanford CNTFET model library with different load

In power consumption part,load capacitance also influence the power consumption in CNTFETs and MOSFETs. Logic gates without capacitance would has relatively low power. All CNTFETs logic gates in this situation would have almost 10 times power consumption improvement than PTM MOSFET models. In 10f capacitance,both models' power increased.But CNTFET's power consumption is slightly less than 45nm PTM MOSFET. Only in OAI22 logic gate,CNTFET's power consumption is larger than MOSFET. But the difference in this logic gate is not obvious. This small degradation can be neglected when we compare it with the benefits it has.

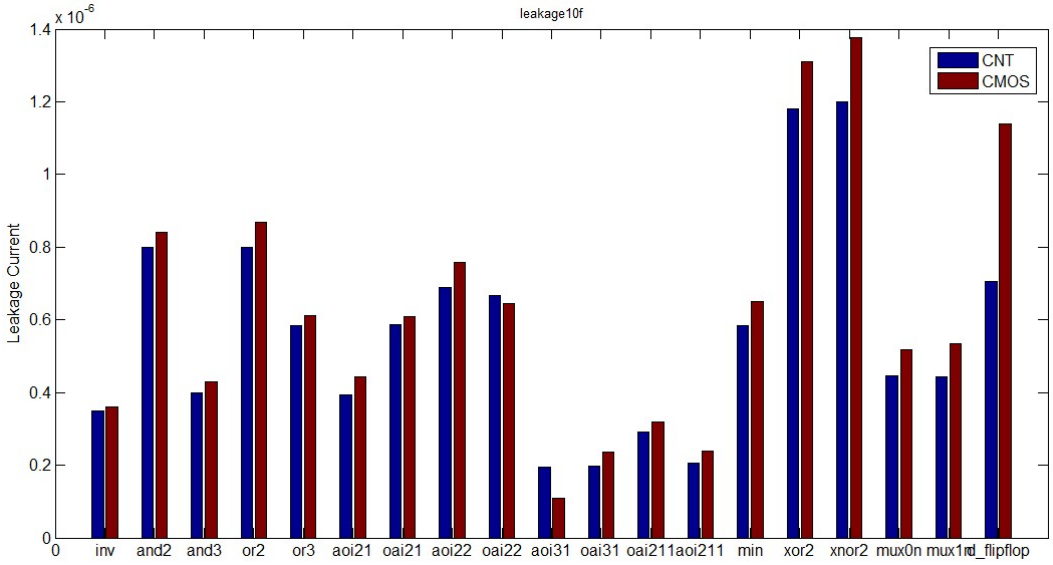


Figure 4-23 Leakage for PTM MOSFET and Stanford CNTFET

leakage of VTL MOSFET model and Stanford CNTFET model library with different load

Compare CNTFET model with predictive MOSFET model in leakage current aspect, the simulation result shows that CNTFET still performs better than this new improved MOSFET.CNTFET logic gates in library have slightly smaller leakage current than the counterpart in MOSFET. Only in OAI22 and AOI31 logic gate CNTFET have a slightly more leakage current.

So,after comparing the two models,writer get the conclusion that CNTFETs performance is still better than the improved PTM MOSFET models.To sum up,Stanford CNTFET model has a excellent advantages in delay,power and leakage.It is a potential model,because it is even better than the predictive model(PTM).

4.2.4 CNTFET library with different number of tubes

The tubes in CNTFET can be divided into two parts, semiconducting tubes and metallic tubes. If metallic tubes exist in CNTFET,the gate terminal has no control and has a serious impact on static current,delay,power. Because the ohmic short between source and drain, new technologies are use to reduce the number of metallic tubes in manufacturing industry,such as Plasma CVD method,General CVD method[34].In this part,we assumed all metallic tubes have been removed. The number of tubes means semiconducting tube numbers.

In general,if the number of tubes is increased, the delay of logic gates are decreased. In figure4-24,when the tubes increase from 1 to 4,the delay for all logic gates would decrease steadily. So large tube numbers would bring a great improvement in delay which is good to switching speed.

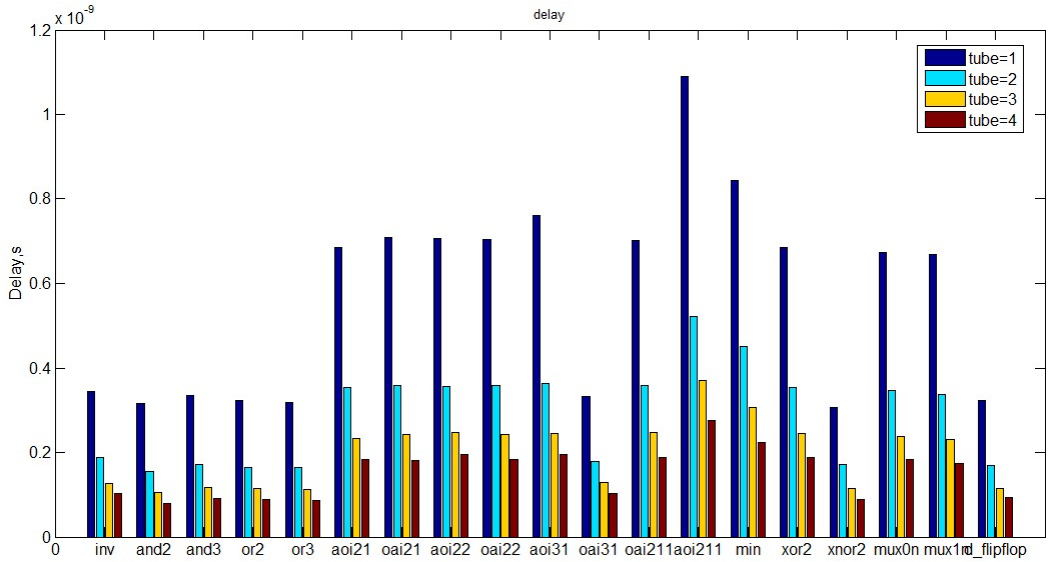


Figure 4-24 Delay for CNTFET,at different number of tubes

While with the growth of tube numbers,power consumption would increased at the same time. So the influence on power dissipation is another important thing we should consider. Like what writer did in last section,give the same input pulse to same logic gate which has different tube number,then calculate the mean value of power consumption.

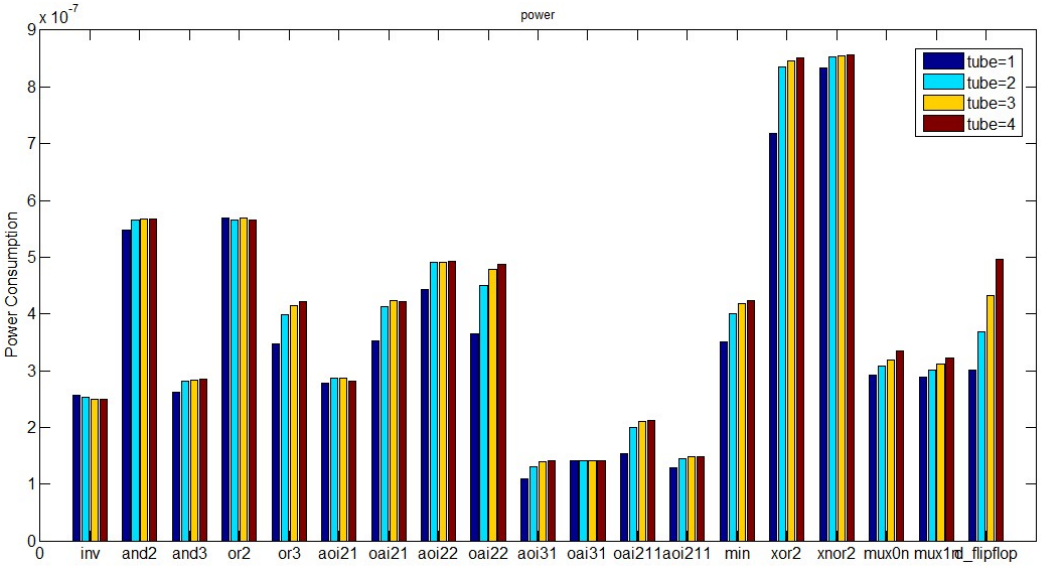


Figure 4-25 Power for CNTFET,at different number of tubes

Figure4-25 shows the increase of tube numbers would not have dramatic influence on power consumption. In some logic gate, it almost keep constant in different tube numbers. Delay and power consumption are two opposite factors. In CNTFET, more tubes will cause less delay but slightly more power consumption. But in the two figures at above,we can find that the increased tube numbers would bring more benefits than its drawbacks.

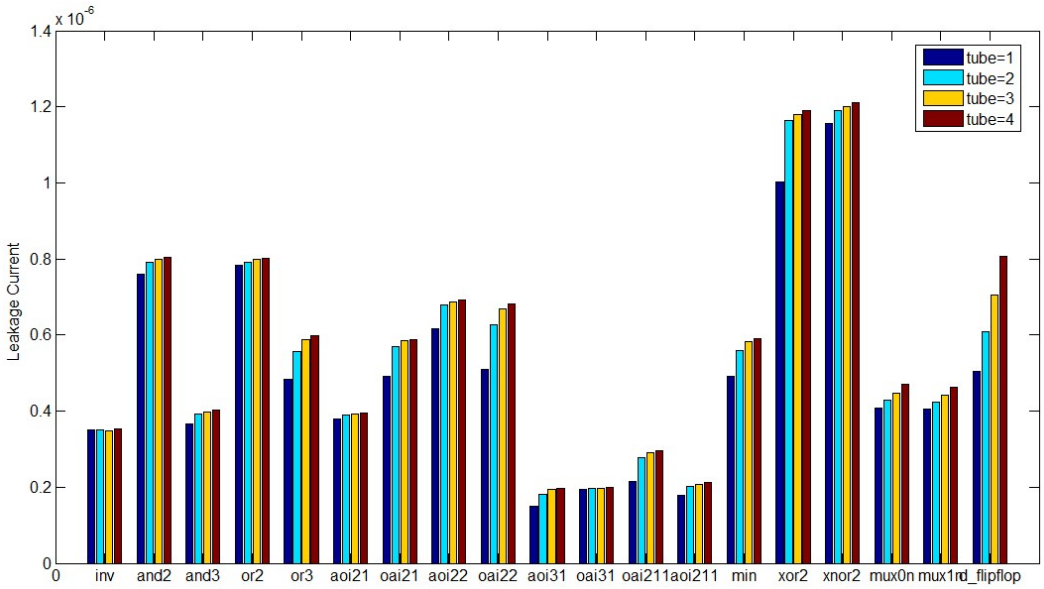


Figure 4-26 Leakage current for CNTFET,at different number of tubes

Another thing need to consider is the leakage current after changing the tube numbers. The leakage current is proportional to the tube numbers.Because more tubes would transfer more Ioff. High leakage current would cause characteristic degradation. The results are shown in Figure4-26.

So choosing the tube numbers in CNTFET we should consider and balance many factors,like delay,power consumption and leakage current we mentioned at before. Another important thing we need to consider is that the area and probability of metallic tubes in large number tubes CNTFET. Now,some problems can be solved through new ways of design which i will mention later.

4.2.5 Conclusion of CNTFET library characterization

This part sum up the delay and power consumption value of CNTFET library at different situation and show the percentage of changes in CNTFET compare with the counterpart of BSIM4 MOSFET.

Logic Gate	32nm CMOS	32nmCNT							
	2w/w	Tube=1		Tube=4		Tube=6		Tube=8	
INV	I.581E-10	3.437E-10	+117.4%	1.029E-10	-34.9%	7.585E-11	-52.0%	6.3693-11	-59.7%
AND2	5.147E-10	3.171E-10	-38.4%	7.922E-11	-84.6%	6.136E-11	-88.1%	4.838E-11	-90.6%
AND3	9.175E-10	3.346E-10	-63.5%	9.141E-11	-90.0%	6.488E-11	-92.9%	5.306E-11	-94.2%
OR2	5.967E-10	3.233E-10	-45.8%	8.775E-11	-85.3%	6.143E-11	-89.7%	4.847E-11	-91.9%
OR3	9.653E-10	3.192E-10	-66.9%	8.664E-11	-91.0%	6.074E-11	-93.7%	4.785E-11	-95.0%
AOI21	4.253E-10	6.863E-10	+61.4%	1.825E-10	-54.9%	1.280E-10	-71.6%	9.627E-11	-77.4%
OAI21	4.030E-10	7.079E-10	+75.7%	1.814E-10	-54.9%	1.288E-10	-68.0%	9.836E-11	-75.6%
AOI22	7.355E-10	7.066E-10	-3.9%	1.947E-10	-73.6%	1.306E-10	-82.2%	1.040E-10	-85.9%
OAI22	3.992E-10	7.050E-10	+76.6%	1.826E-10	-54.2%	1.285E-10	-67.8%	9.889E-11	-75.2%
AOI31	6.827E-10	7.601E-10	+11.3%	1.960E-10	-71.3%	1.321E-10	-80.7%	1.066E-10	-84.4%
OAI31	8.532E-10	3.318E-10	-61.1%	1.025E-10	-87.9%	7.722E-11	-90.9%	6.301E-11	-92.6%
OAI211	6.610E-10	7.029E-10	+16.3%	1.888E-10	-71.5%	1.302E-10	-80.3%	1.037E-10	-84.3%
AOI211	7.823E-10	1.089E-09	+39.2%	2.758E-10	-64.7%	1.783E-10	-77.2%	1.470E-10	-82.0%
MIN	4.812E-10	8.439E-10	+75.4%	2.242E-10	-53.4%	1.610E-10	-66.5%	1.231E-10	-74.4%
XOR	3.926E-10	6.863E-10	+74.8%	1.882E-10	-52.1%	1.284E-10	-67.3%	1.050E-10	-73.3%
XNOR	7.475E-10	3.064E-10	-59.0%	8.851E-11	-88.2%	6.167E-11	-91.7%	3.961E-11	-94.7%
MUX0N	3.167E-10	6.743E-10	+112%	1.836E-10	-42.0%	1.292E-10	-59.3%	1.022E-10	-67.7%
MUX1N	4.388E-10	6.687E-10	+52.4%	1.739E-10	-60.4%	1.189E-10	-72.9%	9.133E-11	-79.2%
D_FF	3.738E-10	3.239E-10	-13.3%	9.243E-11	-75.3%	5.684E-11	-84.8%	3.236E-11	-91.3%

Table4-3 Delay of CMOS and CNT library

Logic Gate	32nmCMOS	32nm CNT							
	2w/w	Tube=1		Tube=4		Tube=6		Tube=8	
INV	3.855e-7	2.557e-7	-33.7%	2.487e-7	-35.5%	2.484e-7	-35.6%	2.448e-7	-36.5%
AND2	1.780e-6	5.473e-7	-69.3%	5.669e-7	-68.2%	5.774e-7	-67.6%	5.733e-7	-67.8%
AND3	9.256e-7	2.618e-7	-71.8%	2.854e-7	-69.2%	2.873e-7	-68.9%	2.897e-7	-68.7%
OR2	1.758e-6	5.693e-7	-67.6%	5.646e-7	-67.9%	5.771e-7	-67.2%	5.783e-7	-67.1%
OR3	1.191e-6	3.465e-7	-70.9%	4.217e-7	-64.6%	4.276e-7	-64.1%	4.360e-7	-63.4%
AOI21	9.481e-7	2.783e-7	-70.6%	2.805e-7	-70.4%	2.901e-7	-70.4%	2.793e-7	-70.5%
OAI21	1.177e-6	3.523e-7	-70.0%	4.212e-7	-64.2%	4.199e-7	-64.3%	4.174e-7	-64.5%
AOI22	1.154e-6	4.427e-7	-61.6%	4.934e-7	-57.2%	4.925e-7	-57.3%	4.928e-7	-57.3%
OAI22	1.064e-6	3.651e-7	-65.7%	4.872e-7	-54.2%	4.890e-7	-54.0%	4.909e-7	-53.9%
AOI31	3.945e-7	1.093e-7	-72.9%	1.417e-7	-64.1%	1.421e-7	-63.9%	1.429e-7	-63.7%
OAI31	5.762e-7	1.408e-7	-75.6%	1.413e-7	-75.5%	1.413e-7	-75.5%	1.417e-7	-75.4%
OAI211	4.713e-7	1.536e-7	-67.4%	2.120e-7	-55.0%	2.115e-7	-55.1%	2.090e-7	-55.7%
AOI211	4.726e-7	1.283e-7	-61.3%	1.491e-7	-68.5%	1.514e-7	-68.0%	1.567e-7	-66.8%
MIN	1.185e-6	3.499e-7	-70.5%	4.232e-7	-64.3%	4.225e-7	-64.3%	4.247e-7	-64.1%
XOR	2.901e-6	7.181e-7	-75.2%	8.520e-7	-70.6%	8.507e-7	-70.7%	8.567e-7	-70.5%
XNOR	3.216e-6	8.339e-7	-74.1%	8.559e-7	-73.4%	8.637e-7	-73.1%	8.701e-7	-72.9%
MUX0N	1.171e-6	2.926e-7	-75.0%	3.339e-7	-71.5%	3.577e-7	-69.2%	3.830e-7	-67/3%
MUX1N	1.477e-6	2.892e-7	-80.4%	3.277e-7	-77.8%	3.492e-7	-76.4%	3.729e-7	-74.8%
D_FF	5.810e-6	3.001e-7	-94.8%	2.120e-7	-91.5%	6.214e-7	-89.3%	7.002e-7	-87.9%

Table4-4 Power of CMOS and CNT library

To summarize,tube numbers bring a large improvement on propagation delay. In table.4-3 we can see that CNTFET delay in some logic gate (such as inverter, AOI21, OAI21, MUX0N) is still larger than MOSFET's counterpart when tube=1. But this can be solved easily when we just add one more tube on transistor. As we can see,propagation delay has significant improvement when tube=2 and all CNTFET logic gates are faster than MOSFET logic circuit. At the same time,the power consumption in this situation(tube=2) is almost same with tube=1 situation. And in table4-4 we can see that only a tiny increase in power consumption when the tube number increase. So tube numbers would not bring too much affects on power consumption,while it would bring a dramatic influence on propagation delay.

After data analysis, CNTFET based logic circuit should have at least two (semiconducting)tubes,this can make sure it has superior features than MOSFET.

5 Simulation based on asymmetrically correlated CNT (ACCNT)

5.1 ACCNT design analysis

In this section,researches are based on Parallel structure of ACCNT. Due to the new design structure would bring more transistor in logic gate and more capacitance between the contacts, the propagation delay,power consumption and leakage current will be changed. The propagation delay is determined by the electrons storing speed on gate capacitance of transistor. So small delay would need high energy/power consumption to store the energy in small time. The performance in CNTFETs characterization have been shown in different structure.

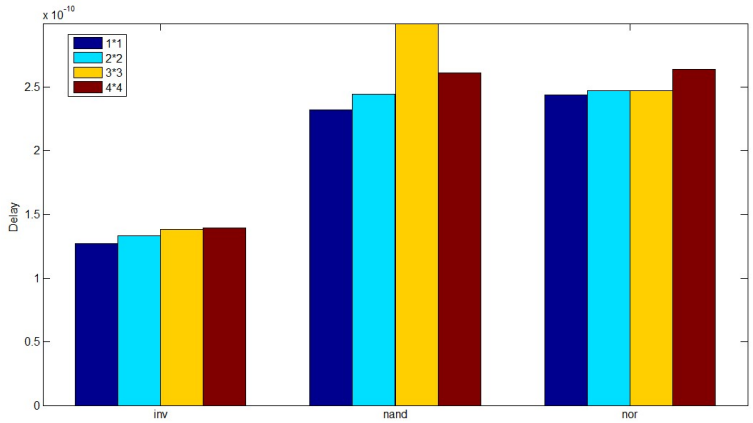


Figure 5-1 delay for accnt design,at different structure

The delay features at different ACCNT structure are shown in Figure5-1. Using the basic logic gates(inverter,NAND,NOR) as an example to see the trend of delay. As the structure becomes complicated, the delay would not increase too much by the structure. So this phenomenon is good to the transistor which need high speed and high metallic tube tolerance. In the introduction,we explain that the delay of CNTFET logic gate is depend on the difference of Ion and Ioff. While the Ion and Ioff also depends on the series and parallel MOSFET and capacitance in logic gate. So the structure would bring little influence on propagation delay definitely.

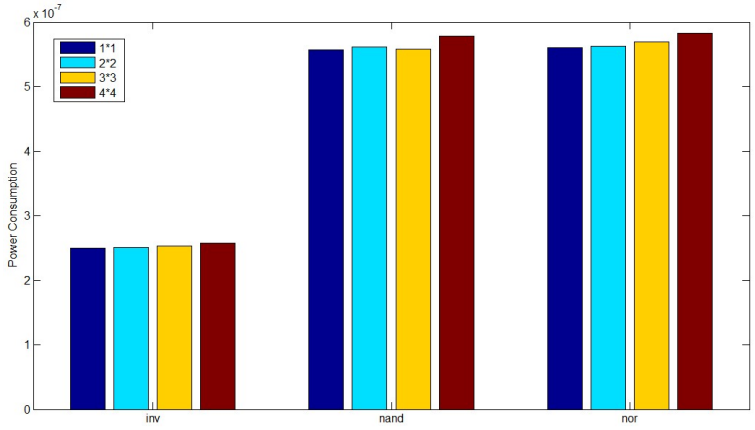


Figure 5-2 Power for accnt design,at different structure

While power consumption depends on the supply voltage,input pulse,load capacitance and off current of the logic gate. Because the power supply,input pulse and load capacitance are same. The factor which influence the power consumption is Ioff in different structure. Through analysis we know that the power consumption almost makes no change in same logic gate.

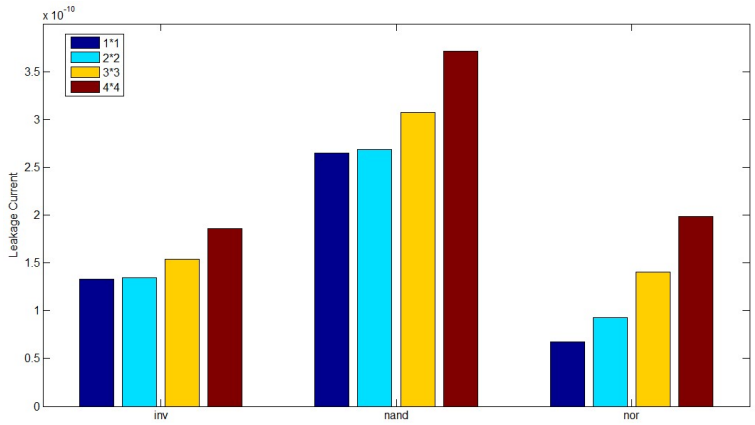


Figure 5-3 Leakage for accnt design,at different structure

But Figure5-3 demonstrate that high leakage would caused by large ACCNT structure. Because more columns would cause high leakage when the transistor turn off. It can be fixed by reducing the number of columns(like using three transistors in series and two columns of transistor). But things need to be considered is that we need to make sure the current drive is larger than the minimum current which can let the transistor works normally.

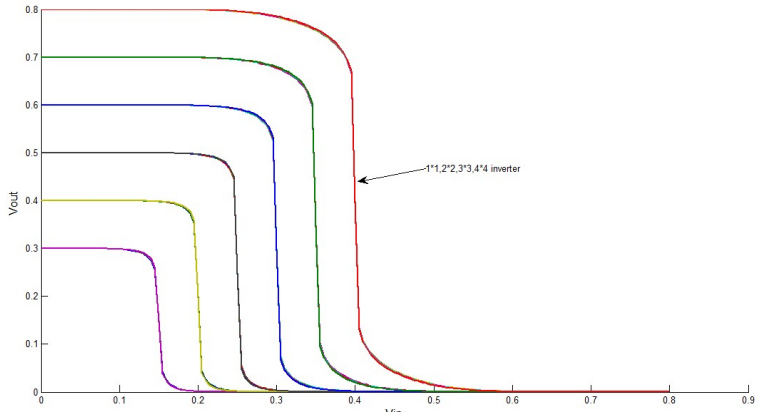


Figure 5-4 VTC at different structure

Figure5-4 shows voltage transfer characteristic in different ACCNT structure. In complicated structure,ACCNT still has steep curve in transition region which almost same with the conventional logic gate design(the curves in same supply voltage almost overlap). The curves still symmetric and the logic gate would switch when input reach Vdd/2. So the ACCNT would not influence voltage transfer characteristic in CNTFETs.

5.2 Metallic tubes influence on leakage in ACCNT structure

This part use 5*5 inverter to analyse the influence of metallic tubes. As we mentioned before,ACCNT structure has a benefit of increased metallic tube tolerance. This part focuses on analysis the influence of metallic tubes on ACCNT structure.

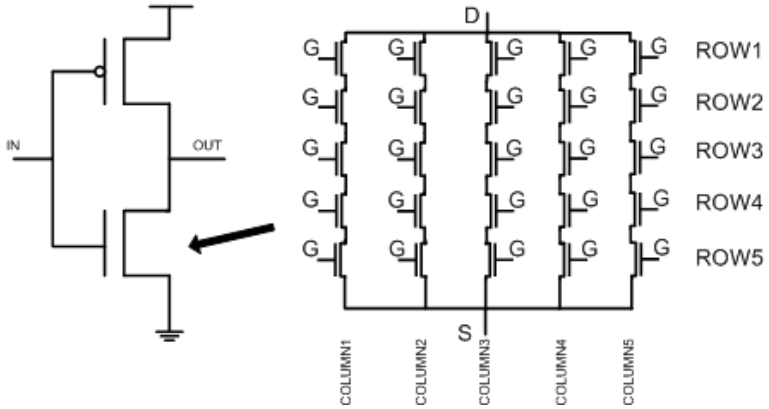


Figure 5-5 5*5 Inverter

As we know, transistors in same row share same tubes. So if CNTFET in first row and first column have one metallic tube,the other 4 CNTFETs in first row have one metallic tube. 32nm Stanford model are used in this project.In this model,all tubes are treat as semiconducting tubes and the parameters which can decide the chirality of tubes are neglected. The approach writer used to measure the influence of metallic tubes in Hspice is that giving the P-CNTFET low input voltage and N-CNTFET high voltage when metallic tube exist. Because of metallic tubes characterization, metallic

tubes will cause the ohmic short of transistor, the current from drain to source would are not controlled by Vgs. So it can be treat as a resistor.

Five cases have been done in 5*5 ACCNT inverter structure.(1)without metallic tubes; (2)10% metallic tubes;(3)20% metallic tubes;(4)30% metallic tubes;(5)40% metallic tubes. In case(1), giving high input voltage to let the pull up network close(all P-CNTFET turn off),then calculating the current through Vdd(which almost equal to subthreshold leakage) in Hspice. In case(2),giving one row of P-CNTFET low input(0V),and giving high input voltage to let the rest of P-CNTFETs turn off, then measuring the leakage current. In case(3),giving two rows of P-CNTFET low input(0V), and following the steps in case(2). Case(4) and case(5) are similar to case(3), only the P-CNTFET row numbers which have low input voltage are different. Things need to mention is that,if all transistors in series have metallic tubes(50 percent metallic at here), the logic gate can not works appropriately. So this situation we need to avoid in practical manufacture.

Simulation on leakage current for different metallic tube percentages are shown at below.

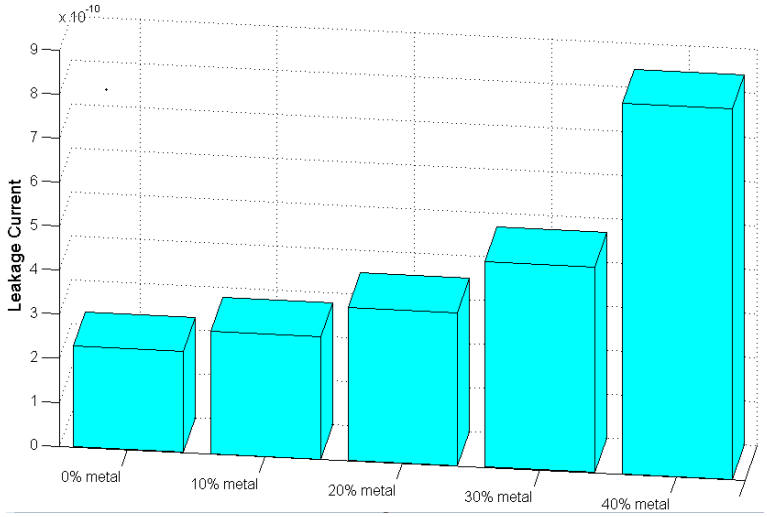


Figure 5-6 Leakage at different metallic tube percent

Through simulation we know,the metallic tubes would increase the leakage current significantly. Because if metallic tubes exist,this transistor can be treat as ohmic short. So the number of series transistors are smaller than before. This situation will cause high leakage. Moreover, the parallel numbers are not change. So we can get the conclusion that the total leakage current would increased. And the experimental result shows in Figure5-6 also obey this rule.

All in all,the exist of metallic tubes not only influence the logic function of circuit, but also cause degradation of leakage,power consumption and propagation delay. So in future,efforts put on reducing the influence of metallic tubes are important.

5.3 Design full-adder based on ACCNT structure

Because of the benefit of asymmetrically correlated carbon nano-tube design (ACCNT), this design methodology can be used in lots of logic circuit for improving the

metallic tolerance.

This part writer use ACCNT to design full adder in 2*2,3*3,4*4 structure as an example.

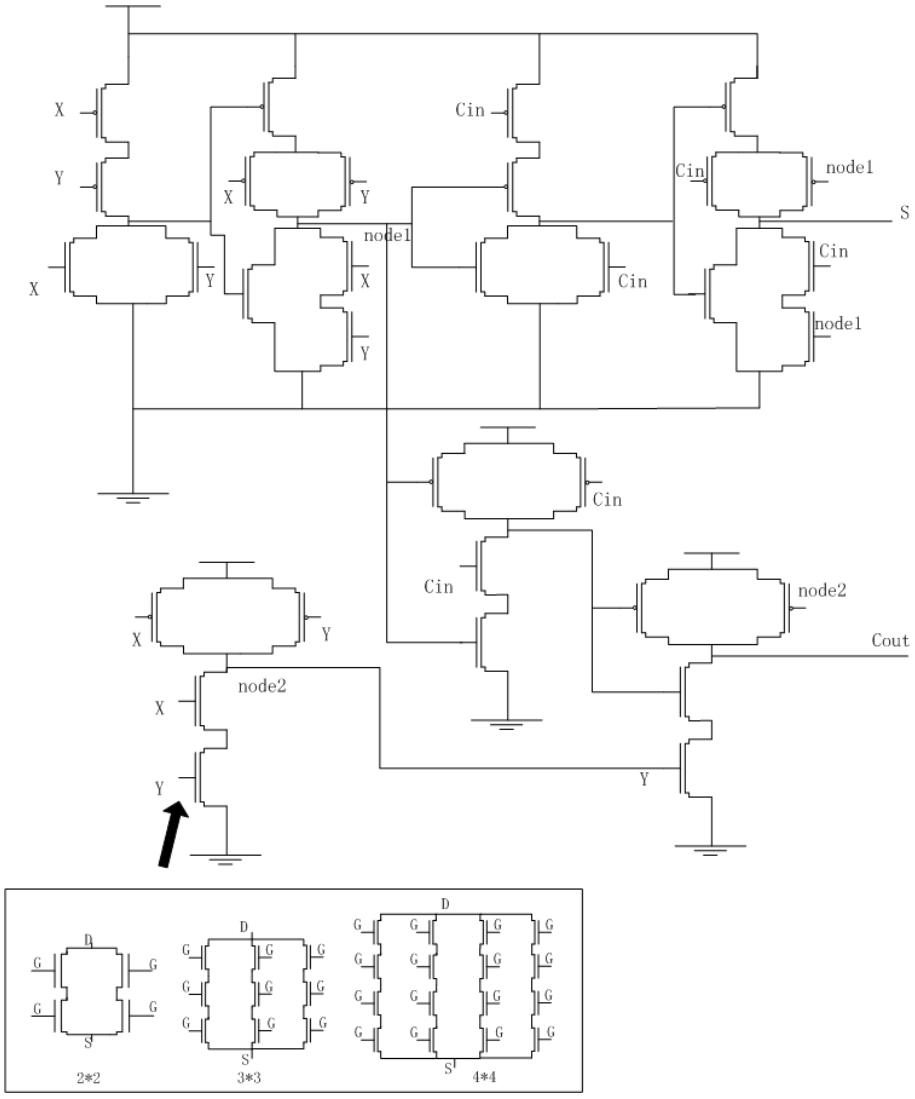


Figure 5-7 Fulladder in ACCNT structure

The structure at above is the full adder which is made of singe CNTFET. ACCNT full-adder design need to use 2*2,3*3,4*4 sub-circuits to replace every transistor in the above circuit. In order to design the circuit easily,writer create sub-circuits for the three different structure separately.Then call this sub-circuit to replace the single transistor. This is similar to what we did in Figure5-5. Through waveform verification, the logic function of all these full-adder circuits have correct function.

The delay and power consumption for different ACCNT structure are concluded in Table5-1. Definitely,the complicated ACCNT structure would lead to increased propagation delay and power consumption which are shown in the table.In this design,the delay has been measured when one of input X=1,Y=Cin=0,and output S change from 0 to 1. And the power is the average power in the simulation time.

Fulladder Structure	Delay	Power
1*1	2.387e-10	8.808e-07
2*2	2.685e-10	9.572e-07
3*3	3.119e-10	1.081e-06
4*4	3.696e-10	1.093e-06

Table5-1 Leakage at different metallic tube percent

So in actual ACCNT design,factors we need to consider are not only the metallic tube tolerance of structure,but also the delay,power and leakage.It should not larger than the maximum value that the logic gate can stand. So further research still need to do, such as design new structure to make sure no degradation in CNTFET characteristics,but it still has high metallic tube tolerance.

6 Conclusion

6.1 CNTFET library

Through extensive simulation and background reading,we can draw the conclusion that 32nm CNTFET has its unique benefits in propagation delay,power consumption and leakage current. The result can be shown in Chapter4. Compare these characteristic in CNTFET with corresponding MOSFETs in different model(BSIM4 and PTM), CNTFET not only has the similar operating principle and transmission performance, but also has relatively high switching speed,lower power consumption and lower leakage current. Even comparing the delay and VTC in different input patterns, CNTFET is always better than conventional transistor. All this characteristic in CNTFETs still superior to the counterpart in BSIM4 and PTM MOSFETs in different load capacitance.

Moreover,32nm CNTFETs have better voltage transfer characteristic than 45nm, 32nm, 22nm,16nm BSIM4 MOSFETs(simulation shows in section4.1.1). CNTFETs has steep curve in transition region, which is because of the high gain it has. Moreover, this performance still exist in low supply voltage(0.3V).

Using an inverter logic gate as an example,writer analyse the influence of temperature. Simulations are done from 0degree to 125degree. Simulation results are shown it section4.1.2. We can found that CNTFETs still perform well in extreme temperature(0degree and 125degree). But in MOSFET, the three important parameters(delay, power, leakage) change a lot,so it is less stable than CNTFET.

Because of the slightly different structure in CNTFET, the factors which would influence the characteristic would be different with traditional MOSFET. In this project writer evaluate the influence of semiconducting tube numbers(assume no metallic tube existed in this situation). Extensive simulation found that large tube numbers will has a significant improvement in delay. Because it equals to increase the width of MOSFET transistor, more electrons or holes can transfer in a unit time. Moreover,the power consumption almost keep stable in different tube numbers. These features are good to CNTFETs characteristic. But another aspect we need to consider is the leakage current. The data analysis shows that the leakage current would increase steadily with the increase of tube numbers. So in actual design,we should consider and balance the drawbacks and benefits which bring from the large number tubes. Then decide which factor is more important in certain design.

6.2 ACCNT analysis

In ACCNT analysis,calculation shows more CNTFETs in series would have high metallic tube tolerance, more CNTFETs in parallel would have high driving current and would not influence the probability of semiconducting tubes in the whole circuit. These benefits can let circuit works appropriately without removing the metallic tubes. So it will be easy to realize. But problems still exist, such as the large area waste when structure turns to be complicated.

Chapter5 shows when the ACCNT structure turn to be complicated,the delay, power, leakage increase slightly. But compare with the unique benefit(high metallic tube tolerance) is has, the slightly degraded characteristic can be neglected.

If at least one transistor is made of semiconducting tube,this logic circuit still has correct function. But more metallic tubes would cause degradation in some characteristic. For example,it would cause relatively large delay,power consumption and leakage current when more metallic tubes grow in it. As expected, the simulation result matches this rule perfectly.

Another benefit is that it is easy to fabricate in industrial field. Because we don't need to change the inside structure of transistor,we only need to change the outside structure of circuit. In this project,a full adder has been design using this structure.

Although it has some drawbacks,the high metallic tube tolerance and ease of implementation are more important than others. So in practical design, this novel design method is popular in microelectronic.

7 Future work

The challenge for manufacturing field is the massive production. It is a long way to go to increase the production efficiency and reduce the cost per transistor. Now many researches focus on method of growth the nano-tubes and printing technology.

Another important issue in near future is minimizing the influence of metallic tubes. Currently,the ways are used now can be divided into two parts:etching metallic tubes by using chemical material;changing the structure of circuit or transistor. But both of these approaches have its problems. For example,semiconducting tubes may be destoried,metallic tubes can not be removed completely,the space of circuit would be increased. So future researches will be interested on minimizing these kind of technical issue.

Moreover,in ACCNT design analysis,although this structure improve the metallic tube tolerance efficiently,drawbacks would appear at same time,such as the slightly increased delay, leakage current and power consumption. So efforts on reducing these disadvantages are very important.

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Appendix

Code for ACCNT 4*4 full adder circuit:

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**********************************************************
***********************************************
.options POST
.options AUTOSTOP
.options INGOLD=2 DCON=1
.options GSHUNT=1e-12 RMIN=1e-15
.options ABSTOL=1e-5 ABSVDC=1e-4
.options RELTOL=1e-2 RELVDC=1e-2
.options NUMDGT=4 PIVOT=13
.param TEMP=27
************************************************
**********************************************************
.TITLE 'IDS vs VGS for CNFET'
Include relevant model files
.lib 'CNFET.lib' CNFET
*******Beginning of circuit and device definitions**********
***************Supplies and voltage parameter:****************
.param vdd=0.7
**********Some CNFET parameters:***************
.param Ccsd=0 CoupleRatio=0
.param m_cnt=1 Efo=0.6
.param Wg=0 Cb=40e-12
.param Lg=32e-9 Lgef=100e-9
.param Vfn=0 Vfp=0
.param m=19 n=0
.param Hox=4e-9 Kox=16
.param delay =0.1ns
.data devinf cload
100f
10f
0
.enddata
**************Define power supply***************************
Vdd Vdd 0 vdd
VA1 a 0 pulse (0 vdd 0 delay delay 4n 9.2n)
VB1 b 0 pulse (0 vdd 1n delay delay 9n 19.2n)
VC1 ci 0 pulse (0 vdd 1n delay delay 18n 36.2n)
*************End define power supply************************

******************** *4model_pfet ************************
.subckt pfetmodel vin up down Vdd
*PCNTFET
XCNT_1 node1 vin up Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_2 node2 vin node1 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_3 node3 vin node2 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_4 down vin node3 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_5 node4 vin up Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_6 node5 vin node4 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_7 node6 vin node5 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_8 down vin node6 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3
```

XCNT_9 node7 vin up Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_10 node8 vin node7 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_11 node9 vin node8 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_12 down vin node9 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_13 node11 vin up Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_14 node12 vin node11 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_15 node13 vin node12 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNT_16 down vin node13 Vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3
.ends

********************4*4model_nfet*************************
** NCHTFET*
.subckt nfetmodel vin up down 0

XCNTn_1 up vin node1 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_2 node1 vin node2 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_3 node2 vin node3 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_4 node3 vin down 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_5 up vin node4 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_6 node4 vin node5 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_7 node5 vin node6 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_8 node6 vin down 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_9 up vin node7 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_10 node7 vin node8 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_11 node8 vin node9 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_12 node9 vin down 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_13 up vin node10 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_14 node10 vin node11 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

```
XCNTn_15 node11 vin node12 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

XCNTn_16 node12 vin down 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9 n1=m n2=n tubes=3

.ends

********************NAND2 MODEL *************************
.subckt nand_2 x y out Vdd 0
Xmodel1 x Vdd out Vdd pfetmodel
Xmodel2 y Vdd out Vdd pfetmodel
Xmodel3 x out node1 0 nfetmodel
Xmodel4 y node1 0 0 nfetmodel
.ends

***************NOR2 MODEL ********************************
.subckt nor_2 va vb Vdd out
Xmodel1 vb Vdd node Vdd pfetmodel
Xmodel2 va node out Vdd pfetmodel
Xmodel3 va out 0 0 nfetmodel
Xmodel4 vb out 0 0 nfetmodel
.ends

********** Y='(C+A*B) SUBCIRCUIT**************************
.subckt _XOR va vb vc out Vdd
Xmodel1 vc Vdd node1 Vdd pfetmodel
Xmodel2 vb node1 out Vdd pfetmodel
Xmodel3 va node1 out Vdd pfetmodel
Xmodel4 vc out 0 0 nfetmodel
Xmodel5 va out node2 0 nfetmodel
Xmodel6 vb node2 0 0 nfetmodel
.ends

********XOR MODEL*********************************
.subkt xor x y out Vdd
Xnor2 x y Vdd out1 nor_2
X_x x y out1 out Vdd _XOR
.ends

********FULL ADDER MODEL*********************************
.subckt xfd x y ci out cout Vdd
Xxor_1 x y node1 Vdd xor
Xxor_2 node1 ci out Vdd xor
Xnand_1 ci node1 node2 Vdd 0 nand_2
Xnand_2 x y node3 Vdd 0 nand_2
Xnand_3 node3 node2 cout Vdd 0 nand_2
.ends

********CALL FULL ADDER MODEL*****************************
X_fulladder a b ci out cout Vdd xfd
c1 out 0 10f

********MEASRURE DELAY,POWER*****************************
.meas tran pow AVG power
.meas tran tdelay trig v(a) val='vdd/2' rise=1
+targ v(out) val='vdd/2' rise=1
.tran 0.5n 9n
.ends
.end
```