Assignment 2

Valid-Invalid Protocol

Group 14
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Results using 1 processor

Tracefile : Debug

```
Available CPUs: 1

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       40      19      21      60      26      34      45.000000


1-Bus Reads     21
2-Bus Writes    60
3-Bus Wait Cycles       0
Total Useful Accesses (without waits)   81
Average waiting time per access:        0
Simulation ends at      11726 ns
```

Tracefile : Random

```
Available CPUs: 1

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       33031   18659   14372   32505   18306   14199   56.404114


1-Bus Reads     14372
2-Bus Writes    32505
3-Bus Wait Cycles       0
Total Useful Accesses (without waits)   46877
Average waiting time per access:        0
Simulation ends at      6256978 ns
```

Tracefile : FFT 16

```
Available CPUs: 1

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       86298   7652    78646   43195   10882   32313   14.312743


1-Bus Reads     78646
2-Bus Writes    43195
3-Bus Wait Cycles       0
Total Useful Accesses (without waits)   121841
Average waiting time per access:        0
Simulation ends at      15685268 ns


Comments are by default at level 3
Put COMMENTS equal to desired level at line 31
Put COMMENTS equal 1 for cpus
Put COMMENTS equal 1 for bus
Put COMMENTS equal 3 for caches
abhishek@Abhishek-PC:/mnt/g/lab$
```

Results using 2 processors

Tracefile : Debug

```
abhishek@Abhishek-PC:/mnt/g/lab$ ./usama.bin tracefiles/dbg_p2.trf

        SystemC 2.3.2-Accellera --- May  4 2020 18:13:49
        Copyright (c) 1996-2017 by all Contributors,
        ALL RIGHTS RESERVED
Available CPUs: 2

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       30      0       30      25      1       24      1.818182
1       32      0       32      34      1       33      1.515152


1-Bus Reads     62
2-Bus Writes    60
3-Bus Wait Cycles       8730
Total Useful Accesses (without waits)   122
Average waiting time per access:        71
Simulation ends at      14291 ns
```

Tracefile : Random

```
Available CPUs: 2

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       16496   385     16111   16402   393     16009   2.364885
1       24556   865     23691   24803   877     23926   3.529245


1-Bus Reads     39802
2-Bus Writes    41206
3-Bus Wait Cycles       5490498
Total Useful Accesses (without waits)   81008
Average waiting time per access:        67
Simulation ends at      10060998 ns
```

Tracefile : FFT 16

```
abhishek@Abhishek-PC:/mnt/g/lab$ ./usama.bin tracefiles/fft_16_p2.trf

        SystemC 2.3.2-Accellera --- May  4 2020 18:13:49
        Copyright (c) 1996-2017 by all Contributors,
        ALL RIGHTS RESERVED
Available CPUs: 2

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       29312   3402    25910   15417   2013    13404   12.106240
1       29262   3151    26111   14801   1898    12903   11.458593


1-Bus Reads     52021
2-Bus Writes    30218
3-Bus Wait Cycles       4143023
Total Useful Accesses (without waits)   82239
Average waiting time per access:        50
Simulation ends at      7628563 ns
```

Results using 4 processors

Tracefile : Debug

```
Available CPUs: 4

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Warning: (W545) sc_stop has already been called
In file: ../../../src/sysc/kernel/sc_simcontext.cpp:1004
In process: cpu_1.execute @ 25895 ns

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       8       0       8       8       1       7       6.250000
1       27      0       27      32      0       32      0.000000
2       43      1       42      38      2       36      3.703704
3       45      0       45      41      0       41      0.000000


1-Bus Reads     122
2-Bus Writes    120
3-Bus Wait Cycles       44571
Total Useful Accesses (without waits)   242
Average waiting time per access:        184
Simulation ends at      25895 ns
```

Tracefile : Random

```
Available CPUs: 4

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Warning: (W206) vector contains 4-value logic
In file: /mnt/g/lab/systemc/include/sysc/datatypes/bit/sc_proxy.h:1514
In process: cache_1.bus_controller @ 2 ns

Warning: (W545) sc_stop has already been called
In file: ../../../src/sysc/kernel/sc_simcontext.cpp:1004
In process: cpu_1.execute @ 18434230 ns

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       8039    85      7954    8251    89      8162    1.068140
1       20450   0       20450   20221   0       20221   0.000000
2       26553   982     25571   26498   1056    25442   3.841586
3       29600   0       29600   29695   3       29692   0.005059


1-Bus Reads     83575
2-Bus Writes    84665
3-Bus Wait Cycles       33544216
Total Useful Accesses (without waits)   168240
Average waiting time per access:        199
Simulation ends at      18434230 ns
```

Tracefile : FFT 16

```
Available CPUs: 4

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Warning: (W545) sc_stop has already been called
In file: ../../../src/sysc/kernel/sc_simcontext.cpp:1004
In process: cpu_2.execute @ 5052367 ns

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       11274   1743    9531    6552    936     5616    15.028610
1       9417    1461    7956    6083    760     5323    14.329032
2       9834    1526    8308    5523    613     4910    13.928502
3       9881    1498    8383    5972    706     5266    13.902731


1-Bus Reads     34178
2-Bus Writes    24130
3-Bus Wait Cycles       10523057
Total Useful Accesses (without waits)   58308
Average waiting time per access:        180
Simulation ends at      5052367 ns
```

Results using 8 processors

Tracefile : Debug

```
Available CPUs: 8

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Warning: (W545) sc_stop has already been called
In file: ../../../src/sysc/kernel/sc_simcontext.cpp:1004
In process: cpu_7.execute @ 64998 ns

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       6       0       6       4       0       4       0.000000
1       34      0       34      22      0       22      0.000000
2       35      0       35      43      0       43      0.000000
3       39      2       37      46      2       44      4.705882
4       36      0       36      55      0       55      0.000000
5       52      0       52      46      0       46      0.000000
6       48      3       45      51      2       49      5.050505
7       42      1       41      55      5       50      6.185567


1-Bus Reads     286
2-Bus Writes    322
3-Bus Wait Cycles       335554
Total Useful Accesses (without waits)   608
Average waiting time per access:        551
Simulation ends at      64998 ns
```

Tracefile : Random

```
Available CPUs: 8

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Warning: (W545) sc_stop has already been called
In file: ../../../src/sysc/kernel/sc_simcontext.cpp:1004
In process: cpu_7.execute @ 41207484 ns

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       4113    22      4091    4030    35      3995    0.699988
1       18318   0       18318   18440   0       18440   0.000000
2       25834   21      25813   25470   30      25440   0.099407
3       29549   1275    28274   28801   1180    27621   4.207369
4       31366   2       31364   30548   1       30547   0.004845
5       32015   12      32003   31781   26      31755   0.059565
6       32327   1626    30701   32285   1653    30632   5.074909
7       32536   1687    30849   32584   1771    30813   5.310197


1-Bus Reads     201413
2-Bus Writes    203939
3-Bus Wait Cycles       209784639
Total Useful Accesses (without waits)   405352
Average waiting time per access:        517
Simulation ends at      41207484 ns
```

Tracefile : FFT 16

```
Available CPUs: 8

Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment02.vcd)

Warning: (W545) sc_stop has already been called
In file: ../../../src/sysc/kernel/sc_simcontext.cpp:1004
In process: cpu_2.execute @ 4165313 ns

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       4956    1114    3842    3153    747     2406    22.949809
1       3983    819     3164    2890    542     2348    19.802124
2       3997    872     3125    2703    507     2196    20.582090
3       4043    867     3176    2695    497     2198    20.243396
4       4055    854     3201    2662    475     2187    19.785619
5       4055    852     3203    2733    512     2221    20.094284
6       4074    821     3253    2710    490     2220    19.324882
7       4124    833     3291    2705    471     2234    19.095036


1-Bus Reads     26255
2-Bus Writes    22251
3-Bus Wait Cycles       24386388
Total Useful Accesses (without waits)   48506
Average waiting time per access:        502
Simulation ends at      4165313 ns
```

Implementations and Observations:

- To avoid data inconsistency, we must implement bus locking and unlocking mechanism. This ensures the data remains coherent throughout the implementation/simulation.