Assignment 3

MOESI Protocol

Group 14
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Results using 1 processor

Tracefile : Debug

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       40      19      21      60      26      34      45.000000


1-Bus Reads     21
2-Bus Writes    26
3-Bus Rd-exclusive      34
3-Bus Wait Cycles       0
Total Useful Accesses (without waits)   81
Average waiting time per access:        0
Total-local cache transfers (Coherence) 0
Simulation ends at      8326 ns
```

Tracefile : Random

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       33031   18659   14372   32505   18306   14199   56.404114


1-Bus Reads     14372
2-Bus Writes    18306
3-Bus Rd-exclusive      14199
3-Bus Wait Cycles       0
Total Useful Accesses (without waits)   46877
Average waiting time per access:        0
Total-local cache transfers (Coherence) 0
Simulation ends at      6205478 ns
```

Tracefile : FFT 16

```
Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment03.vcd)

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       86298   7652    78646   43195   10882   32313   14.312743


1-Bus Reads     78646
2-Bus Writes    10882
3-Bus Rd-exclusive      32313
3-Bus Wait Cycles       0
Total Useful Accesses (without waits)   121841
Average waiting time per access:        0
Total-local cache transfers (Coherence) 0
Simulation ends at      15652368 ns
```

Results using 2 processors

Tracefile : Debug

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       30      0       30      25      1       24      1.818182
1       32      0       32      35      1       34      1.492537


1-Bus Reads     62
2-Bus Writes    2
3-Bus Rd-exclusive      58
3-Bus Wait Cycles       0
Total Useful Accesses (without waits)   122
Average waiting time per access:        0
Total-local cache transfers (Coherence) 0
Simulation ends at      6767 ns
```

Tracefile : Random

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       16496   385     16111   16402   393     16009   2.364885
1       24556   865     23691   24803   877     23926   3.529245


1-Bus Reads     39802
2-Bus Writes    1270
3-Bus Rd-exclusive      39936
3-Bus Wait Cycles       1070665
Total Useful Accesses (without waits)   81008
Average waiting time per access:        13.2168
Total-local cache transfers (Coherence) 0
Simulation ends at      7749084 ns
```

Tracefile : FFT 16

```
Info: (I702) default timescale unit used for tracing: 1 ps (group14_assignment03.vcd)

Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       29312   3402    25910   15417   2013    13404   12.106240
1       29262   3151    26111   14801   1898    12903   11.458593


1-Bus Reads     52021
2-Bus Writes    3911
3-Bus Rd-exclusive      26307
3-Bus Wait Cycles       1140776
Total Useful Accesses (without waits)   82239
Average waiting time per access:        13.8715
Total-local cache transfers (Coherence) 0
Simulation ends at      6104318 ns
```

Results using 4 processors

Tracefile : Debug

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       8       0       8       8       1       7       6.250000
1       27      0       27      32      0       32      0.000000
2       43      1       42      38      2       36      3.703704
3       45      0       45      42      0       42      0.000000


1-Bus Reads     122
2-Bus Writes    3
3-Bus Rd-exclusive      117
3-Bus Wait Cycles       2
Total Useful Accesses (without waits)   242
Average waiting time per access:        0.00826446
Total-local cache transfers (Coherence) 0
Simulation ends at      8788 ns
```

Tracefile : Random

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       8039    85      7954    8251    89      8162    1.068140
1       20450   0       20450   20221   0       20221   0.000000
2       26553   982     25571   26498   1056    25442   3.841586
3       29600   0       29600   29695   3       29692   0.005059


1-Bus Reads     83575
2-Bus Writes    1148
3-Bus Rd-exclusive      83517
3-Bus Wait Cycles       9195726
Total Useful Accesses (without waits)   168240
Average waiting time per access:        54.6584
Total-local cache transfers (Coherence) 0
Simulation ends at      11175178 ns
```

Tracefile : FFT 16

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       11274   1743    9531    6552    936     5616    15.028610
1       9417    1461    7956    6083    760     5323    14.329032
2       9834    1526    8308    5523    613     4910    13.928502
3       9881    1498    8383    5972    706     5266    13.902731


1-Bus Reads     34178
2-Bus Writes    3015
3-Bus Rd-exclusive      21115
3-Bus Wait Cycles       2689847
Total Useful Accesses (without waits)   58308
Average waiting time per access:        46.1317
Total-local cache transfers (Coherence) 0
Simulation ends at      2957542 ns
```

Results using 8 processors

Tracefile : Debug

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       6       0       6       4       0       4       0.000000
1       34      0       34      22      0       22      0.000000
2       35      0       35      43      0       43      0.000000
3       39      2       37      46      2       44      4.705882
4       36      0       36      55      0       55      0.000000
5       52      0       52      46      0       46      0.000000
6       48      3       45      51      2       49      5.050505
7       42      1       41      55      5       50      6.185567


1-Bus Reads     286
2-Bus Writes    9
3-Bus Rd-exclusive      313
3-Bus Wait Cycles       45
Total Useful Accesses (without waits)   608
Average waiting time per access:        0.0740132
Total-local cache transfers (Coherence) 0
Simulation ends at      10003 ns
```

Tracefile : Random

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       4113    22      4091    4030    35      3995    0.699988
1       18318   0       18318   18440   0       18440   0.000000
2       25834   21      25813   25470   30      25440   0.099407
3       29549   1275    28274   28801   1180    27621   4.207369
4       31365   2       31363   30548   1       30547   0.004846
5       32015   12      32003   31782   26      31756   0.059564
6       32327   1626    30701   32285   1653    30632   5.074909
7       32536   1687    30849   32584   1771    30813   5.310197


1-Bus Reads     201412
2-Bus Writes    4696
3-Bus Rd-exclusive      199244
3-Bus Wait Cycles       74177735
Total Useful Accesses (without waits)   405352
Average waiting time per access:        182.996
Total-local cache transfers (Coherence) 0
Simulation ends at      21031659 ns
```

Tracefile : FFT 16

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU     Reads   RHit    RMiss   Writes  WHit    WMiss   Hitrate
0       4956    1114    3842    3153    747     2406    22.949809
1       3983    819     3164    2890    542     2348    19.802124
2       3997    872     3125    2703    507     2196    20.582090
3       4043    867     3176    2695    497     2198    20.243396
4       4055    854     3201    2662    475     2187    19.785619
5       4055    852     3203    2733    512     2221    20.094284
6       4074    821     3253    2710    490     2220    19.324882
7       4124    833     3291    2705    471     2234    19.095036


1-Bus Reads     26255
2-Bus Writes    4241
3-Bus Rd-exclusive      18010
3-Bus Wait Cycles       6051971
Total Useful Accesses (without waits)   48506
Average waiting time per access:        124.767
Total-local cache transfers (Coherence) 0
Simulation ends at      1742206 ns
```

Performance Analysis and Conclusion:

1. **Hit rate**

   Valid-Invalid protocol and MOESI protocol have same hit rates. This is because there no pre-fetching process in MOESI protocol.

2. **Bus Requests**

   No of bus requests in MOESI protocol are less in every case than that in Valid-Invalid protocol. In MOESI protocol there is no bus requests occurring for the states MODIFIED and EXCLUSIVE, hence the bus requests are less here. Let us look at the following table:

3. **Average waiting time per access**

   Since the no. of bus request are less, the waiting time for the bus acquisition in MOESI protocol is also less than Valid-Invalid protocol. Let us look at the following table:

Average waiting time	Valid-Invalid Protocol	MOESI Protocol
DBG p8	551	0.0740
RND p8	517	182.996
FFT16 p8	502	124.767

4. **Total execution time**

Total execution time	Valid-Invalid Protocol	MOESI Protocol
DBG p8	64998 ns	10003 ns
RND p8	41207484 ns	21031659 ns
FFT16 p8	4165313 ns	1742206 ns

As seen from above table the total execution time of MOESI protocol is very less than the Valid-Invalid protocol in almost all the cases.