

LLCWhisp: Feasibility of Occupancy Attacks on Fully Associative LLCs with Random Eviction

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- ▶ Such shared caches are vulnerable to **timing and conflict-based side-channel attacks**.
- ▶ Fully Associative LLCs with **Random Eviction Policy (RFA-LLC)** is a proposed mitigation for conflict-based side-channel attacks.
- ▶ But **RFA-LLC** is vulnerable to **occupancy-based attacks**.



- ▶ These attacks use:
 - **Cache fills**
 - **Difference in hit and miss latency**
 - **Disturbance measurements due to different Eviction patterns**



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- ▶ **Real-world systems** include:
 - **OS scheduling noise**
 - **Interrupts and background tasks**
- ▶ These introduce significant **noise and uncertainty** in attack performance.



- ▶ Evaluate the feasibility of **occupancy-based attacks** on RFA-LLCs in real system setting
 - In the presence of realistic OS and system-level interference
 - Using **gem5 full-system simulation** with Linux OS

Occupancy-Based Attack Model



Attacker Core

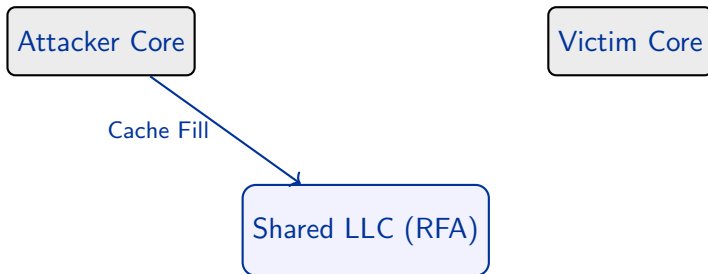
Occupancy-Based Attack Model



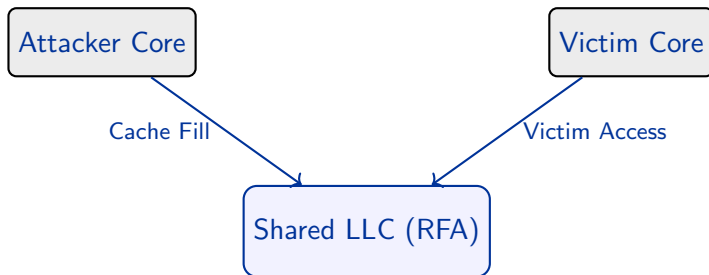
Attacker Core

Victim Core

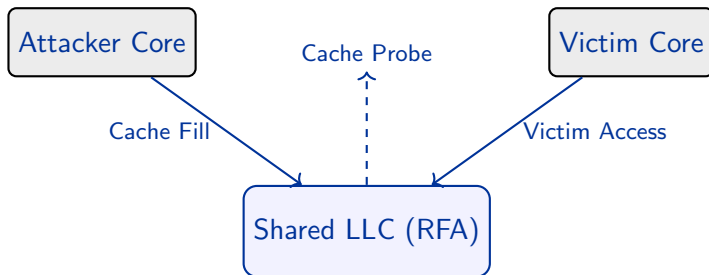
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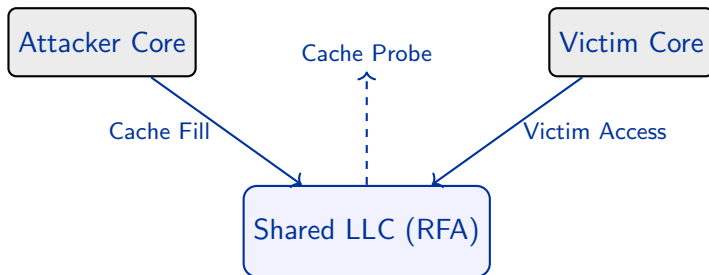
Occupancy-Based Attack Model



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Occupancy-Based Attack Model



Attack Steps:

1. Attacker fills the LLC
2. Victim evicts some cache lines
3. Attacker probes occupancy
4. Inference via disturbance



- ▶ Implementation and experimentation of FA cache with random replacement policy in gem5
- ▶ Validation of cache fill and probe measures for occupancy-based attacks in realistic setting
- ▶ Analyzing the effect of OS noise on occupancy-based attack performance



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- ▶ **Simulator:** Experiments are conducted on the **gem5 full-system simulator** using the **Linux operating system**.
- ▶ **System Noise:** All experiments are conducted in presence of **realistic OS scheduling and background activity**, to evaluate feasibility of occupancy attacks in realistic settings.



► Fully-Associative LLC:

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► **Efficient Random Eviction:** In gem5 we maintain an **Invalid Blocks List** data structure that:

- Tracks all cache lines invalidated
- Allows constant-time insertion/removal as blocks become invalid/valid

ISA	x86
Frequency	3GHz
Cores	2
L1-I, L1-D	32KB, 8-way, 64B line, 1 cycles, LRU, no prefetch
L2	256KB, 16-way, 64B line, 3 cycles, no prefetch, LRU
L3 (LLC)	2MB, 32768-way, 64B line, 15 cycles, no prefetch, RandomRP
DRAM	SingleChannelDDR3_1600 3GB

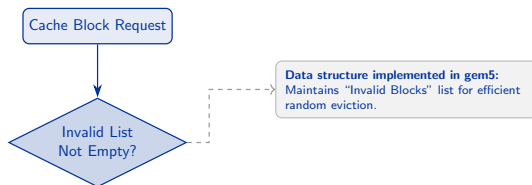
Table: Gem5 System Configurations

Cache Block Request Handling in gem5

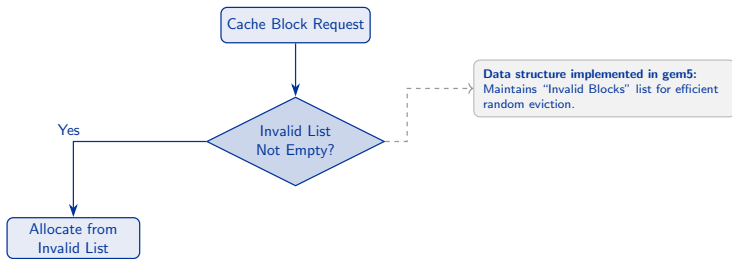


Cache Block Request

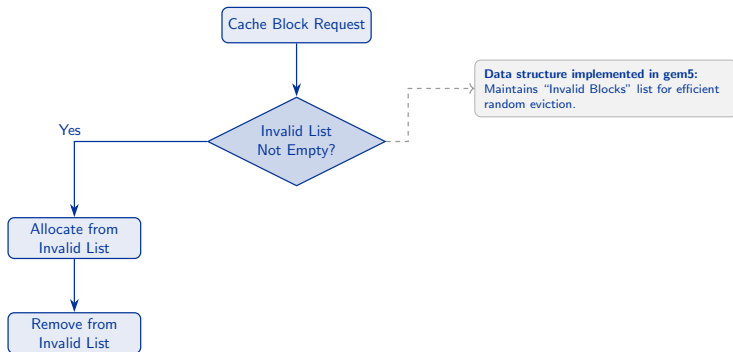
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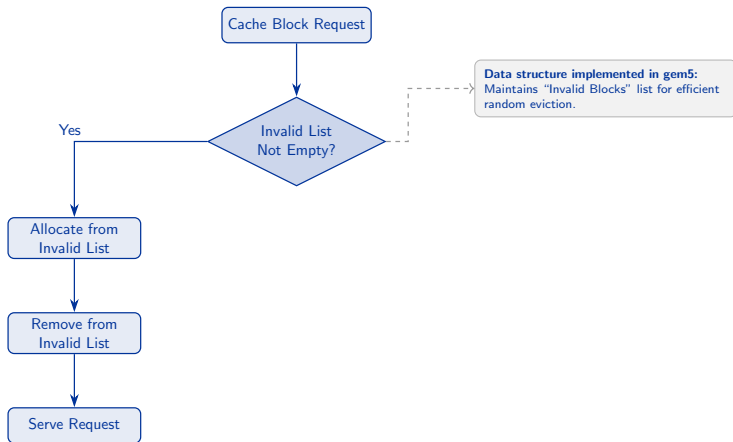
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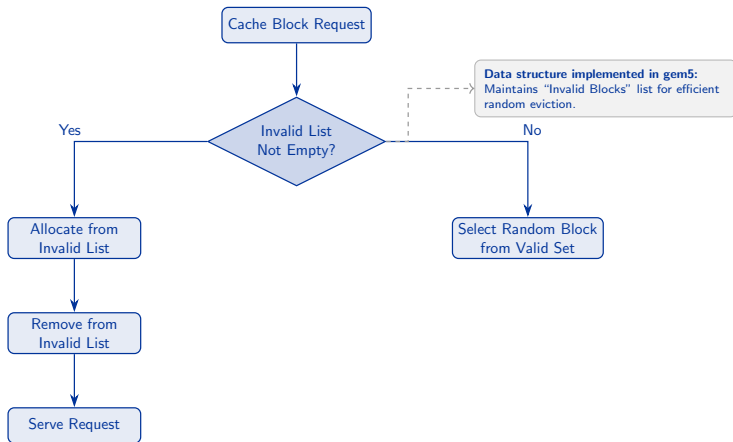
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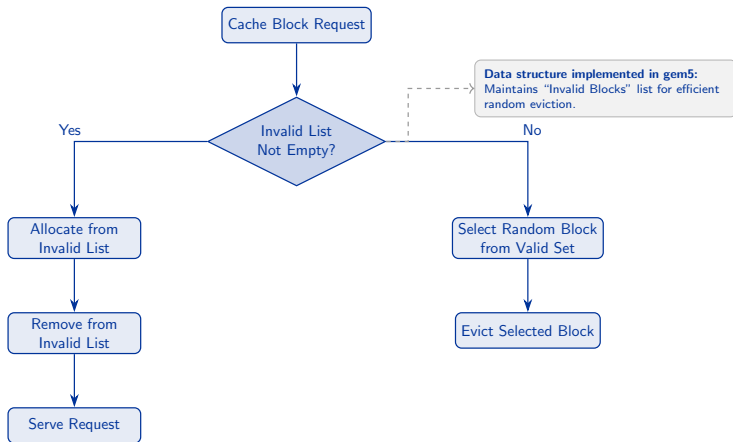
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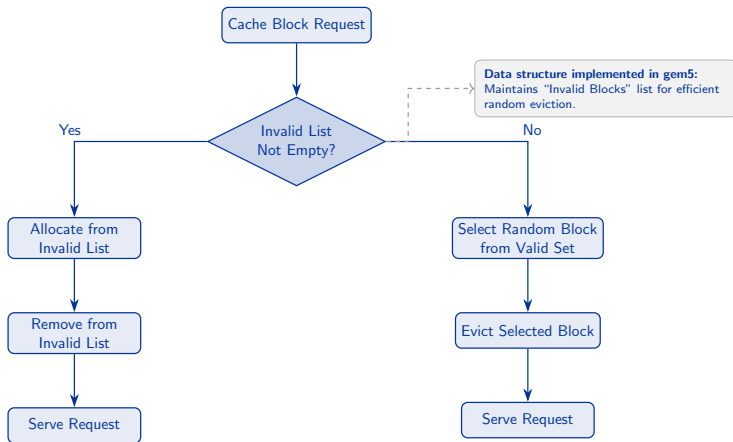
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- ▶ **CRProbe:** Accessing data and using access latency to detect hit or miss which helps calculating occupancy.

CRFill and CRProbe Visualization



FA Cache

CRFill and CRProbe Visualization



FA Cache

↓ CRFill

CRFill and CRProbe Visualization



FA Cache

↓ CRFill

Filled with Attacker Data



CRFill and CRProbe Visualization



FA Cache

↓ CRFill

Filled with Attacker Data



↓ CRProbe

CRFill and CRProbe Visualization



FA Cache

↓ CRFill

Filled with Attacker Data



↓ CRProbe

Holes created for cache hits



CRFill and CRProbe Visualization



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↓ CRFill

Filled with Attacker Data



↓ CRProbe

Holes created for cache hits





CRProbe Algorithm

```
int i = arr_size - 1
while i  $\geq$  0 do
    t1 = rdtsc
    load(arr[i])
    delay = rdtsc - t1
    clflush(arr[i])
    if delay < hit_miss_threshold OR i == arr_size-1
then
    occ++
    i = i - 1
done
```



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Note: Misses are handled carefully to avoid evicting filled lines—crucial in random eviction LLCs.



- ▶ Goal: To study the effectiveness of cache filling under realistic OS scheduling and background activity.
- ▶ Setup: Multiple access patterns tested with data sizes and access counts denoted as x^a — where data size is x times of LLC size and a is the number of iterations over the data..



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Occupancy values reflect the ability of attacker to maintain control over cache blocks despite system noise.

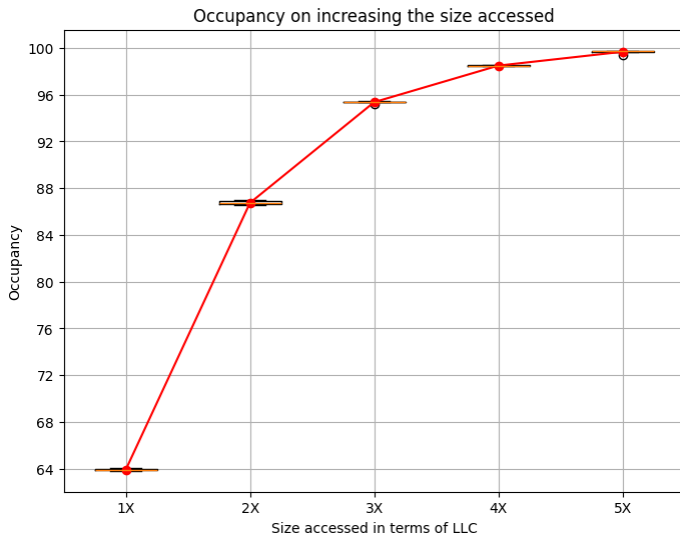


Figure: CRFill step

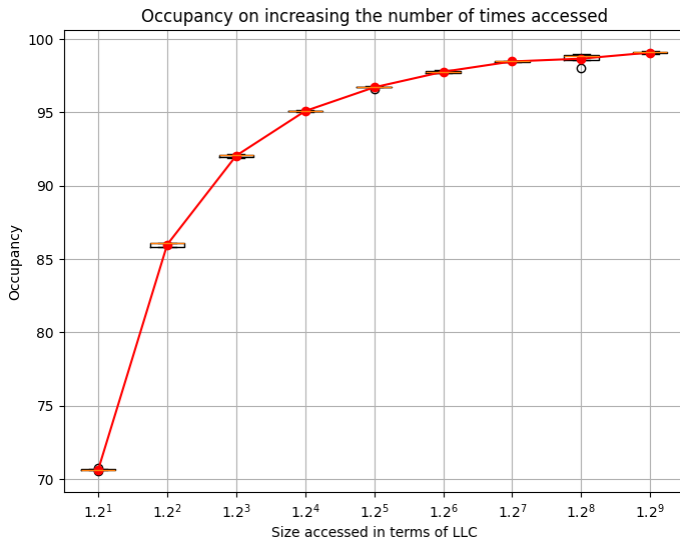


Figure: CRFill step

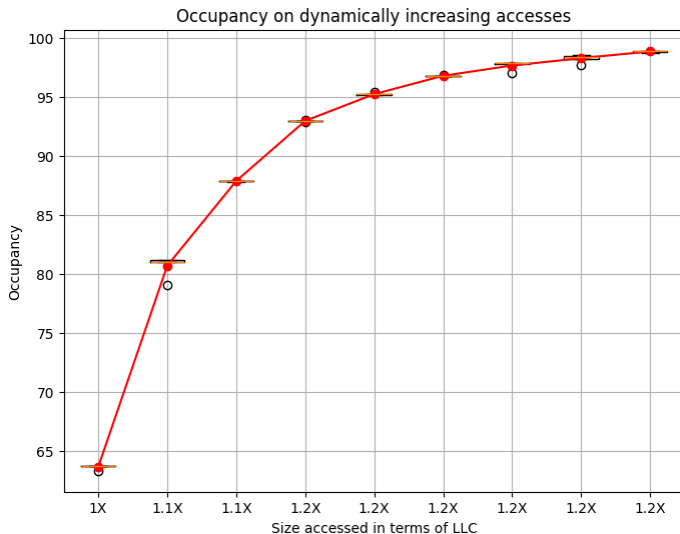


Figure: CRFill step



Inference

Occupancy-based attacks are practically feasible even in noisy, full-system environments. Minimal OS-induced disturbance observed, with attackers consistently achieving high occupancy across patterns.



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Fingerprinting using Cache Footprint



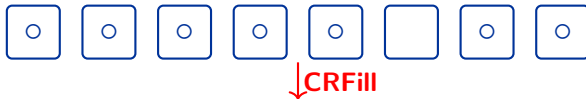
Holes after CRProbe (Hit->flush->hole)



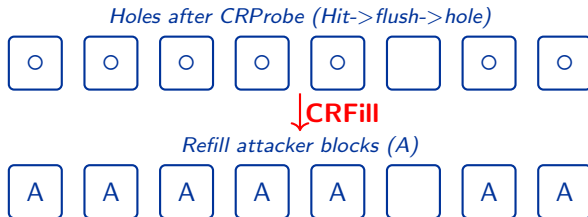
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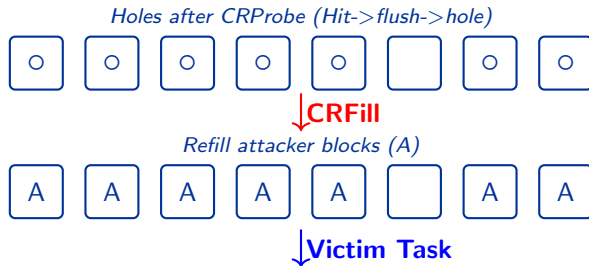
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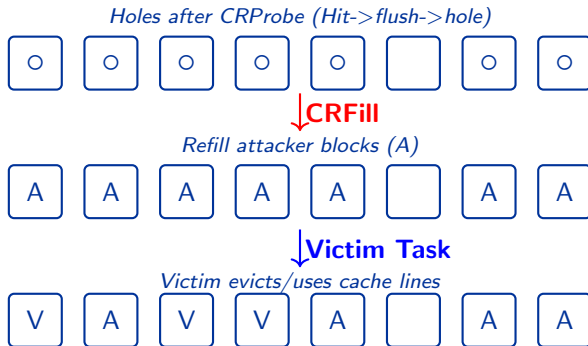
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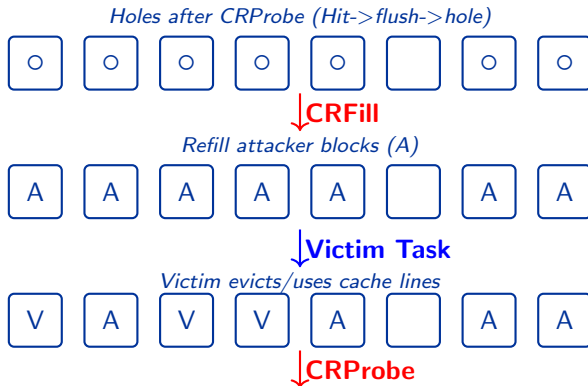
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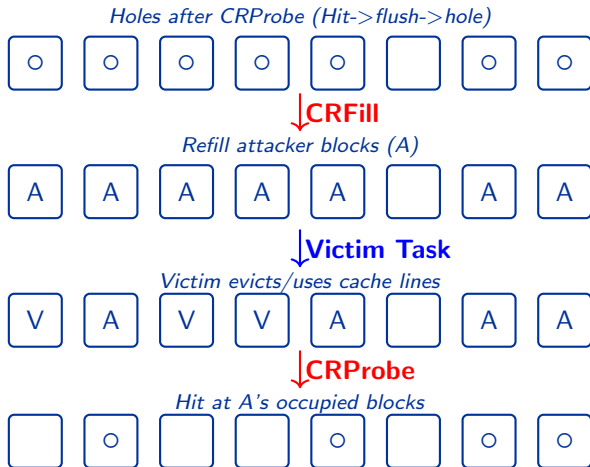
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Key Challenge in Realistic Setups

Realistic setups introduce **non-deterministic noise** due to OS and background processes.

Experimental Procedure: OS Noise Analysis



- ▶ Attacker executes **CRFill** and **CRProbe** to occupy a significant portion of the LLC.
- ▶ Then, the process goes inactive for a controlled interval (x ms), allowing only OS/background activities.

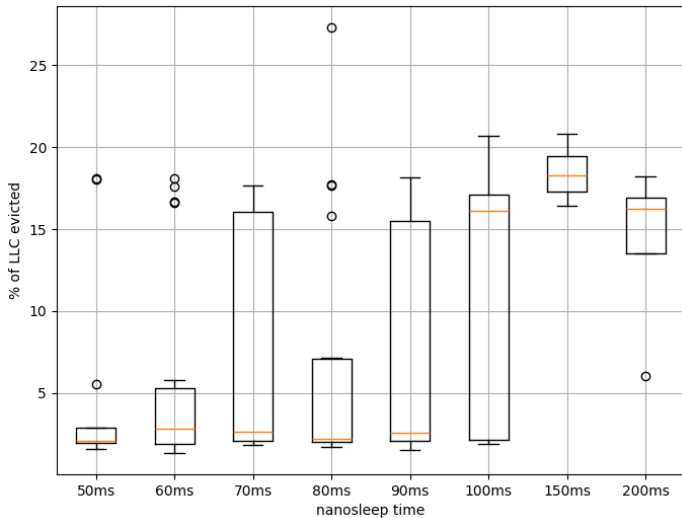


- ▶ Attacker executes **CRFill** and **CRProbe** to occupy a significant portion of the LLC.
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- ▶ We conduct this using **two methods of inactivity**:
 - `nanosleep()` system call
 - `rdtsc`-based busy wait using a `while` loop

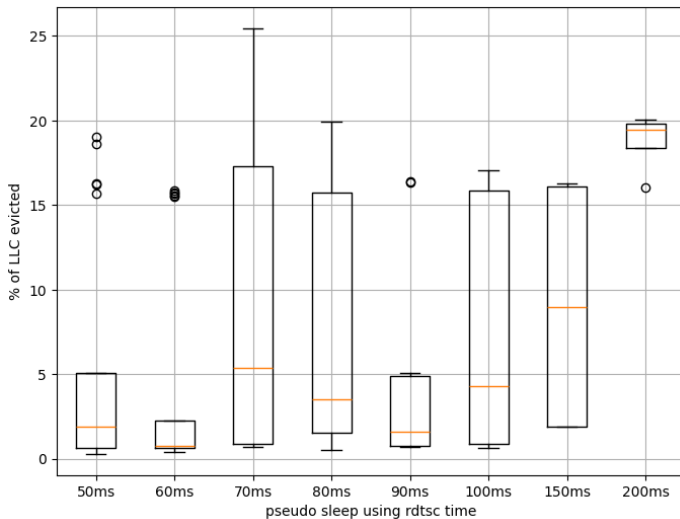


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- ▶ We conduct this using **two methods of inactivity**:
 - `nanosleep()` system call
 - `rdtsc`-based busy wait using a `while` loop
- ▶ After x ms, attacker **probes** the cache again to estimate how many of its blocks were disturbed.
- ▶ This helps infer the **extent of OS-induced eviction** over time.

Footprint due to sleep



Footprint due to pseudo sleep





Observation

A longer idle interval \rightarrow more blocks disturbed \rightarrow higher system activity footprint.

However, **the presence of OS noise introduces considerable variability** in the observed cache behavior, impacting the consistency of attack performance.



Key Takeaway

Operating system noise significantly increases variability in cache occupancy, leading to observable degradation in attack performance.

- ▶ The attacker can still achieve **substantial occupancy** across diverse access patterns even in noisy settings.
- ▶ However, **system-level interference** introduces **non-determinism** in cache behavior, impacting repeatability and effectiveness of occupancy-based attacks.



Next Steps

- ▶ Investigate techniques to **mitigate the impact of OS-induced noise** on cache behavior to carry out cache occupancy based attacks.
- ▶ Explore **adaptive or noise-resilient attack strategies** that can maintain effectiveness even under significant system-level interference.



Thank you for Attending!

Questions and Answers!