Step-Up Switching-Mode Converter With High Voltage Gain Using a Switched-Capacitor Circuit

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***Abstract*—A new circuit is proposed for a steep step-up of the line voltage. It integrates a switched-capacitor (SC) circuit within a boost converter. An SC circuit can achieve any voltage ratio, allowing for a boost of the input voltage to high values. It is unregulated to allow for a very high efficiency. The boost stage has a regulation purpose. It can operate at a relatively low duty cycle, thus avoiding diode-reverse recovery problems. The new circuit is not a cascade interconnection of the two power stages; their operation is integrated. The simplicity and robustness of the solution, the possibility of getting higher voltage ratios than cascading boost converters, without using transformers with all their problems, and the good overall efficiency are the benefits of the proposed converter.**

***Index Terms*—Pulsewidth-modulated (PWM) dc–dc converter, step-up switching converter, switch capacitor.**

I. Motivation

THE RECENT emerging technology requires dc-to-dc converters with a steep voltage ratio. For example, high-intensity discharge lamps (HID) for automobile headlamps require stepping up the typical 12-V battery voltage to about 100-V output voltage, at 35-W power [1]. The telecommunication industry needs to interact with the computer industry in its desire to use the telecom infrastructure to provide Internet services. The telecom equipment uses a -48-V bus distributed power system, backed by a 48-V dc battery plant. The information industry uses uninterruptible power supplies, but the backuptime provided by them is not enough; a better choice for providing longer reverse time is to use the -48-V telecom power supply and to boost it to the necessary 380-V intermediate dc bus. This application requires no isolation in the dc-to-dc step-up front-end, since the isolation is provided by the following stages, which transform the 380-V bus to the voltages required by the servers for data processing [2].

Usual boost converters cannot provide such a high dc voltage ratio. One can not work at a high duty-cycle value, due to the latch-up condition; in a typical example given in [3], where the parasitic resistances in the power stage have been accounted as 1% from the load value, the maximum voltage ratio was 4.7 for operating at a nominal duty cycle $D = 0.88$. Practically, such a value is unrealizable, due to regulation requirements; for compensating changes in load or line, the duty cycle may have to be increased, and a latch-up operation appears. An extreme duty cycle is also not desirable due to diode-reverse recovery problems: the output rectifier would conduct for a very short time period, and the high diode forward current and output voltage would degrade the efficiency.

The dc-to-dc converters comprising high-frequency transformers can provide a high voltage gain, but their efficiency is drastically degraded by losses associated with the leakage inductors, which induce high voltage stress, large switching losses and serious electromagntic interference (EMI) problems. A solution for recycling the leakage energy is proposed in [4] and [5]: a flyback converter is modified as the center-tapped inductor buck–boost converter and a passive clamp circuit is used for recycling the leakage energy. However, the proposed circuit is by no means simple. It presents resonating currents, peaks in the magnetizing inductance current, and currents through and voltage across switches, overpassing their nominal values in their counterparts in classical buck-boost pulsewidth modulated (PWM) converters.

A cascade of two dc-to-dc boost converters was proposed in [6], where an intermediate dc voltage is established between the two stages. Schottky diodes have been used instead of fast-recovery diodes, as they have a lower forward-voltage drop and no reverse recovery. However, the cascade of two boost converters implies a low total efficiency, which is equal to the product of the efficiencies of each converter. This mitigates against the simplicity of the circuit; similarly, if one uses a quadratic boost converter.

A novel method is proposed in this paper. An integration of a switched-capacitor (SC) circuit within a boost converter. It is known that an SC converter can provide any voltage ratio, depending on the number of capacitors used in its structure. However, its efficiency is dramatically reduced when it is required to provide a constant output voltage. If there is no such constraint, as in the case when the SC-circuit output voltage is the input of a boost-regulated converter, the SC converter can operate with a high efficiency.

The new circuit is described in Section II. Its steady-state topologies are exactly analyzed by using state–space equations. Using an energy-balance method, the input-to-output voltage ratio is found. A discussion on the choice of the parameters and simulation diagrams is given in Section III. Experimental results and conclusions are presented in Section IV.

II. New Step-Up Circuit and its Analysis

It is known [7], [8] that a step-up SC circuit can provide any line-to- load voltage ratio. If n is the number of capacitors used in the SC structure, then

$$V_{0_{\text{ideal}}} = (n+1)V_g \tag{1}$$

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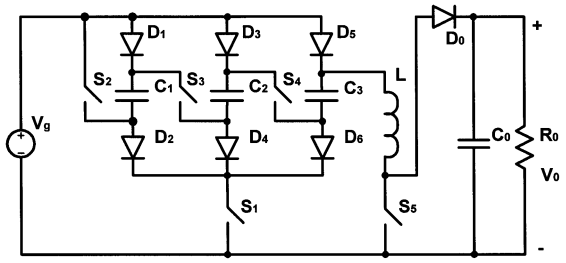

Fig. 1. Step-up switching converter with a high voltage ratio.

where V_g is the line voltage, and V_0 the output voltage. The losses (diode's forward and drop voltages on the parasitic resistances of the capacitors and transistors in conduction) are neglected. The output capacitor C_0 (connected in parallel to the load) is not accounted in n, because its role is to reduce the output ripple. Therefore, by choosing n, any voltage ratio can be attained. The SC converter would be the ideal choice for an application where no isolation is needed, if it were not for the efficiency(η) requirement. As

$$\eta = \frac{V_0}{(n+1)Vg} \tag{2}$$

when an output voltage at a certain constant level is required, the efficiency may drop considerably. Therefore, an SC circuit is proposed in this paper only as an intermediate stage in the boost converter, the requirement for a given fixed output voltage of the SC stage being dropped.

In order to compare the proposed circuit with a quadratic boost converter and to realize a step-up voltage ratio of about ten, as required by today's technological applications, it was chosen as $n = 3$. However, if a higher voltage ratio is required, it can simply be obtained by increasing n.

In Fig. 1, the new converter is presented. It is composed of an SC circuit with three capacitors C_1, C_2, and C_3, four active switches $S_1 \sim S_4$, and six diodes $D_1 \sim D_6$. The switch S_5, inductor L, diode D_0, and capacitor C_0 form an usual boost converter, i.e., the SC circuit is inserted between the line and the boost stage. The switches diagram is given in Fig. 2(a), and the three switching topologies are presented in Fig. 2(b)–(d). The durations of the three topologies are xDT_s, $(1-x)DT_s$, and $(1-D)T_s$, i.e., the classical on-topology of a boost converter is split into two stages. The first stage overlaps the on-topology of the SC circuit. The second stage is combined with the off-topology of the SC circuit. The second part of the off-topology of the SC circuit overlaps the off-topology of the boost converter. As a result, *the SC circuit and the boost converter do not operate as a cascade of converters*, but their operation is integrated. The choice of the value of x will be explained in the design section.

An exact analysis algorithm was used. The following state equations have been written for each of the three switching topologies, by taking into account all parasitic elements r_L for the dc resistance of the inductor, and r_C for the dc capacitor resistance, (r_{C_0} was neglected, as being much smaller than the load value), r_{S_1} for the on-resistance of any of the switches S_1-S_4, r_{S_5} for the on-resistance of switch S_5 (note that S_5 has to withstand the output voltage V_0, i.e., is submitted to a higher voltage stress than $S_1 \sim S_4$). V_D is the forward voltage of any of the diodes.

For the first switching topology

$$\begin{aligned}
\frac{dv_{C_k}}{dt} &= -\frac{1}{C\,(r_C + r_{S_1})} v_{C_k} + \frac{V_g - 2V_D}{C(r_C + r_{S_1})}, \qquad k = 1,2,3 \\
\frac{di_L}{dt} &= -\frac{r_L + r_{S_5}}{L} i_L + \frac{V_g - V_D}{L} \\
\frac{dv_{C_o}}{dt} &= -\frac{1}{RC_o} v_{C_O}.
\end{aligned} \tag{3}$$

For the second switching topology

$$\begin{aligned}
\frac{dv_{C_1}}{dt} &= \frac{dv_{C_2}}{dt} = \frac{dv_{C_3}}{dt} = -\frac{1}{C} i_L \\
\frac{di_L}{dt} &= \frac{1}{L} v_{C_1} + \frac{1}{L} v_{C_2} + \frac{1}{L} v_{C_3} \\
&\quad - \frac{3r_{S_1} + r_{S_5} + r_L + 3r_C}{L} i_L + \frac{V_g}{L} \\
\frac{dv_{C_0}}{dt} &= -\frac{1}{RC_o} v_{C_o}.
\end{aligned} \tag{4}$$

For the third switching topology

$$\begin{aligned}
\frac{dv_{C_1}}{di} &= \frac{dv_{C_2}}{dt} = \frac{dv_{C_3}}{dt} = -\frac{1}{C} i_L \\
\frac{di_L}{dt} &= \frac{1}{L} v_{C_1} + \frac{1}{L} v_{C_2} + \frac{1}{L} v_{C_3} \\
&\quad - \frac{3r_{S_1} + 3r_C + r_L}{L} i_L + \frac{V_g - V_D}{L} - \frac{1}{L} v_{C_0} \\
\frac{dv_{C_o}}{dt} &= \frac{1}{C_o} i_L - \frac{1}{RC_o} v_{C_O}
\end{aligned} \tag{5}$$

where C is the value of any of the equal capacitors C_1, C_2, C_3.

An approximate input-to-output voltage ratio, M, is found by using the classical energy balance approach in which the losses are neglected. As shown in Fig. 3, in the first topology $V_L \approx V_g$, in the second one $V_L \approx 4V_g$ (as usual in this method, the transient times are considered short enough, thus allowing to see the capacitor as a constant voltage source of value V_g), and in the third topology $V_L = 4V_g - V_0$. As in a steady-state cycle $\int_o^{Ts} V_L dt = 0$, it results in

$$V_g x D T_s + 4V_g(1-x)DT_s + (4V_g - V_o)(1-D)T_s = 0 \tag{6}$$

or

$$M = \frac{V_o}{V_g} = \frac{4 - 3xD}{1 - D}.$$

The relationship shows again the integrated operation between the two converters, the SC converter with three capacitors which boosts the line four times, the boost converter that boosts the line $1/(1-D)$ times, and the integrated term $-3xD$.

III. Design Aspects of Proposed Converter

A. Parameters Design

Four parameters have to be chosen L, C, x, and f_s ($f_s = 1/T_s$, f_s is the switching frequency). The first design formula for L is the classical one

$$L = V_g \frac{DT_s}{\Delta I_L} \tag{7}$$

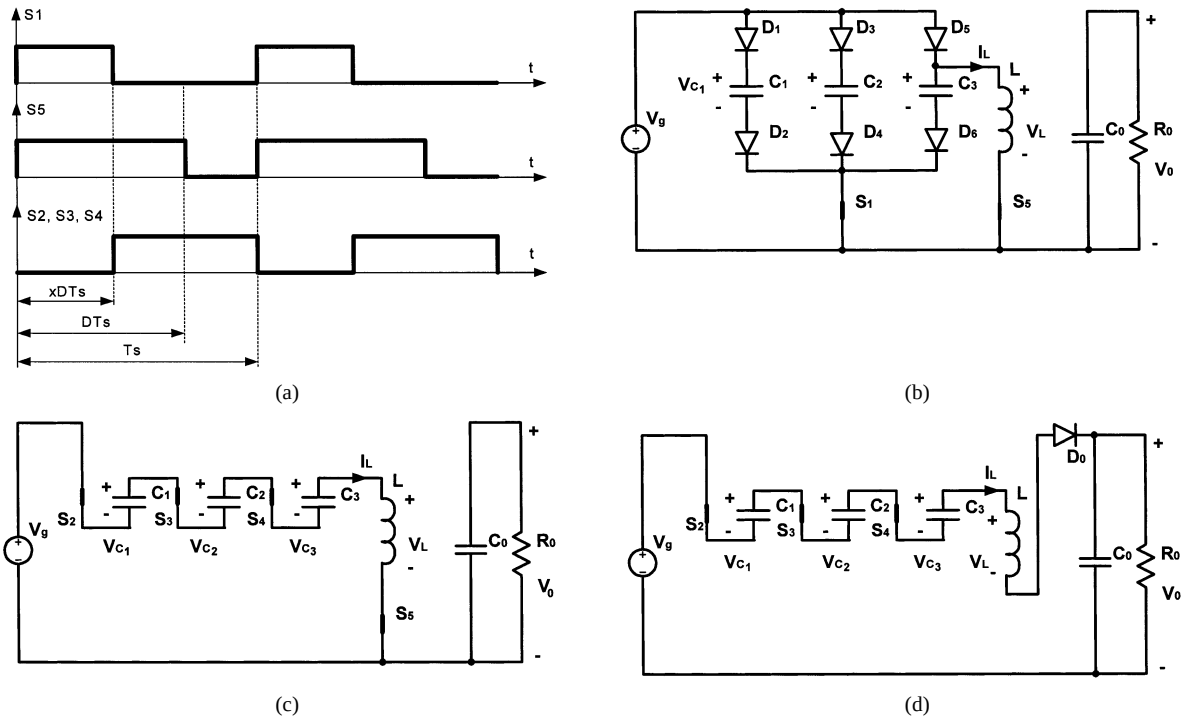

Fig. 2. (a) Timing diagram; (b) first switching topology; (c) second switching topology; and (d) third switching topology of the proposed converter.

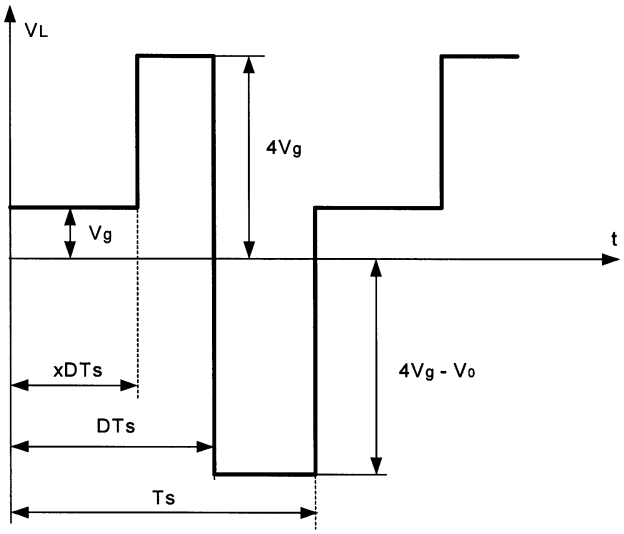

Fig. 3. Approximative inductor voltage balance for a steady-state (nominal) cycle.

based on imposing a small ripple ΔI_L on i_L.

The first design formula for C and f_s is the classical one, requiring for a small ripple in the voltage ΔV_C (as explained in [9], this requirement comes not only from the desire of having a clean dc load voltage, but mainly from the need of increasing the efficiency of the SC circuit and decreasing the peak of the charging capacitor current in the first switching topology, i.e., decreasing the EMI)

$$Cf_s = \frac{V_o}{2R_o(\Delta V_C)} \tag{8}$$

which gives one degree of design freedom.

However, in the proposed circuit, L, C, f_s, and x have to meet one more complicated constraint, the duration of the first topology xDT_s has to be calculated in such a way as to: 1) allow for charging of C_1, C_2, and C_3 at their nominal required value (typically for an SC circuit, see [7], the nominal operating point has to be on the linear part of the capacitor charging characteristic), and 2) avoid sensible discharging of the capacitors in the second topology. These requirements give an implicit constraint. By using the time-domain equations of each topology, the constraints have been applied to the steady-state cycle, and numerical implicit equations have been found and solved by the computer. By choosing $f_s = 100$ kHz, and designing $L = 0.1$ mH, and $C = 100$ μF, it was numerically found that a ten times step up of the voltage is obtained for $x = 0.39$ (Note that for other choices of L and C, it would be possible to find another x which would give the voltage ratio of ten. This is due to the fact that there are three design constraints for four parameters). Equation (6) was derived for an ideal converter; therefore, the dependency of x on L, C, and f_s was not visible in (6).

B. Control Circuit

The ratio between the duration of the first topology, xDT_S, and that of the second topology, $(1-x)DT_S$ is constant. For compensating line or load disturbances, the PWM adjusts D, i.e., the duration of each one of the switching topologies, but not the ratio x (the driving signal of S_1 is related to that of S_5).

C. Simulation Results

By using cyclically (3)–(5), with the boundary conditions: 1) the state at the end of a topology is the initial state for the following topology, and 2) the state at the end of each cycle is the initial state for the next cycle, the simulated main waveforms of the converter have been found. The values of the parasitic

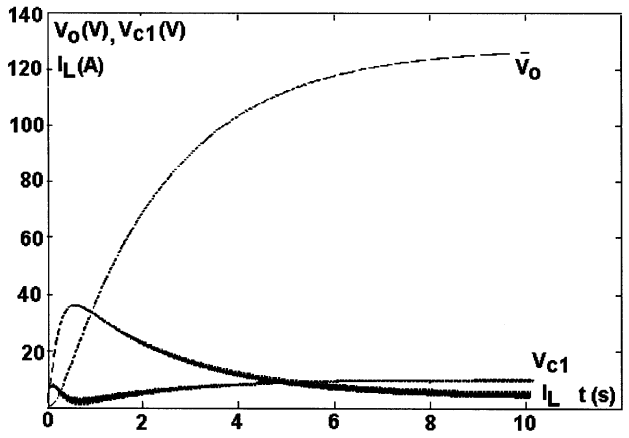

Fig. 4. Transient waveforms: inductor current $i_L(t)$; capacitor voltage $v_{C_1}(t) = v_{C_2}(t) = v_{C_3}(t)$; load voltage (simulation results).

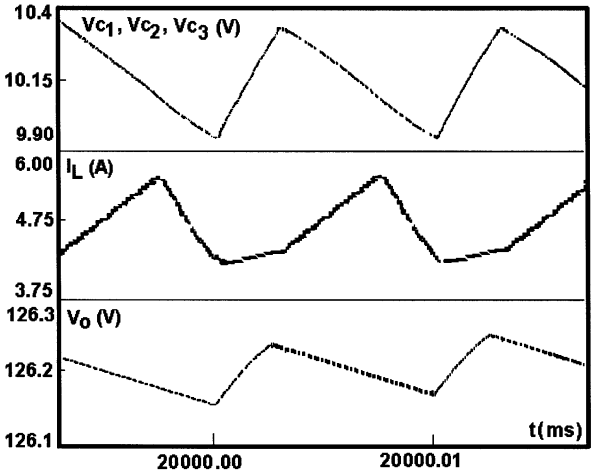

Fig. 5. Steady-state cycle: capacitor voltages $V_{C_1} = V_{C_2} = V_{C_3}$, inductor current I_L, load voltage V_0 (simulation results).

elements are those of the experimental circuit ($r_C = 0.02\ \Omega$, $V_D = 0.3$ V).

The transient waveforms of the inductor current, capacitor voltages and load voltage are shown in Fig. 4. A picture of a steady-state (nominal) switching cycle for V_{C_1}, V_{C_2}, V_{C_3}, I_L and V_0 is given in Fig. 5. The presence of an inductor belonging to the boost stage in the charging and discharging SC topologies limits the transient peak of the charging current, compared to that noticed in classical SC converters [7].

One can still see high current peaks in the charging process of the capacitors. Recently, a new control method was proposed, in which switch S_1 acts as a current source, assuring a constant current charging of the switched capacitor [10].

D. Efficiency Discussion

An interpretation of (2) was given in [9]. Apparently, for a certain set V_g, V_o, n can be chosen such that to get even 100% efficiency. The problem is that, by using a given number n of capacitors, there is a maximum *achievable* value for V_0 [9]

$$V_0 \text{ achievable} = \frac{(n+1)(V_g - V_D)}{1 + \frac{nr}{R_o}\left(1 + \frac{1}{2D}\right)},\ r = r_s + r_c. \quad (9)$$

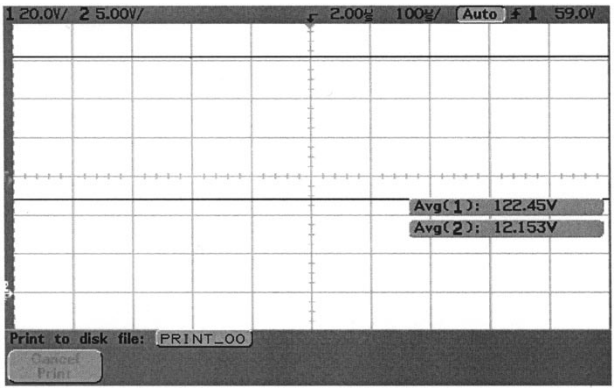

Fig. 6. Experimental results: steady-state load voltage.

In typical SC step-up converters, the load voltage has to be regulated at a certain value $\overline{V}_0$ (which, of course, can be only lower than V_0 *achievable*), and this is the value that appears in (2). For example, in [7], a 5–12-V step-up converter was designed, requiring $n = 2$ and giving, according to (2), $\eta = 80\%$. However, with $n = 2$, one could get an output voltage of about 14.3 V, i.e., the same converter could be working with an efficiency of 95%, if not for the customeŕs need of a load voltage of 12 V. It was proved in [9] that the efficiency of an SC converter is independent of the value of the parasitic resistances; the efficiency depends only on the value of $\bar{V}_o$.

In the circuit proposed in this research, there is no request on the output voltage of the SC converter, as all the regulation is imposed on the boost stage. This is why the boost stage is needed. Therefore, the SC block can operate with its maximum intrinsic efficiency, which allows for a high efficiency of the designed converter.

IV. Experimental Results and Conclusion

The converter was built in the laboratory for $P = 35$ W, $V_g = 12$ V, getting $V_0 = 120$ V when working at a nominal $D = 0.7$, i.e., the line voltage was boosted ten times. Operating at such a value of D allows for alleviating the diode recovering problems and avoids a latch-up condition. In the design, $f_s = 100$ kHz, $L = 0.1$ mH, $C = 100\ \mu$F, $C_0 = 100\ \mu$F (multilayer ceramic capacitors with $r_C = 0.02\ \Omega$ have been used). Schottky diodes are used (chosen for their low forward voltage and less recovery problems). Note that $S_1 \sim S_4$ are submitted to low voltages $3V_g$ for S_1, V_g for S_2–S_4, and only S_5 is submitted to the load voltage. This allows for a choice of transistors with a very low on-resistance for S_1–S_4, thus improving the efficiency. The value of x used in the practical circuit was closed to the calculated value for getting the desired dc gain.

The experimental results are given in Fig. 6. It is possible to note that a clean dc load voltage, ten times the line, was achieved. The experimental load voltage waveform confirms that the output voltage ripple is negligible. This result validates the simulation waveforms shown in Fig. 5 (a ripple of 0.1 V in the output voltage of 120 V). The measured efficiency is, as expected, lower than the calculated one (91%), due to practical conditions in which the prototype was built in the laboratory. Except for this, the efficiency can still be improved by intro-

ducing soft switching for S_5, that will allow for decreasing the switching losses of S_5 and D_0.

In the proposed circuit, n was chosen as 3, in order to get a step up of the line of about ten times. This value answers present requests of the industry and permits a comparison of the new converter with a cascade of hard-switching boost converters/quadratic boost converter, that would achieve the same voltage ratio, but with a lower efficiency. One advantage of the proposed circuit is its flexibility. By simply increasing the number of capacitors n, any higher voltage ratio could be achieved. A generalization of (6) gives $M = ((n+1) - nxD)/(1-D)$. It can be noted that the increase in M is obtained with almost no decrease in the efficiency (as, each additional capacitor requires only an additional small transistor and two diodes), making the proposed converter for applications where no isolation is required a much better solution than cascading a few boost converters.

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