Analog CMOS IC Design

ECP 405 Lab File

INDIAN INSTITUE OF INFORMATION TECHNOLOGY, KOTA

SUBMITTED TO: DR. BHARAT CHOUDHARY

SUBMITTED BY: ABHISHEK KUMAR

ID: 2021KUEC2053

BATCH : B2

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Experiment 1

AIM: To study drain and transfer characteristics of NMOS and PMOS.

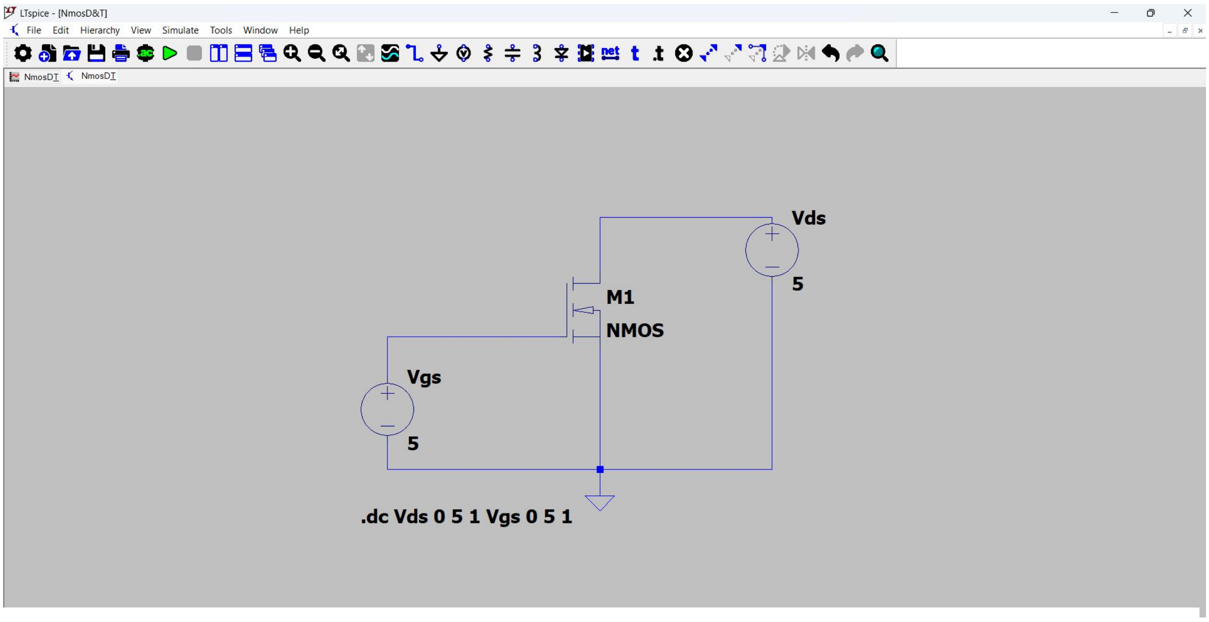
Theory:

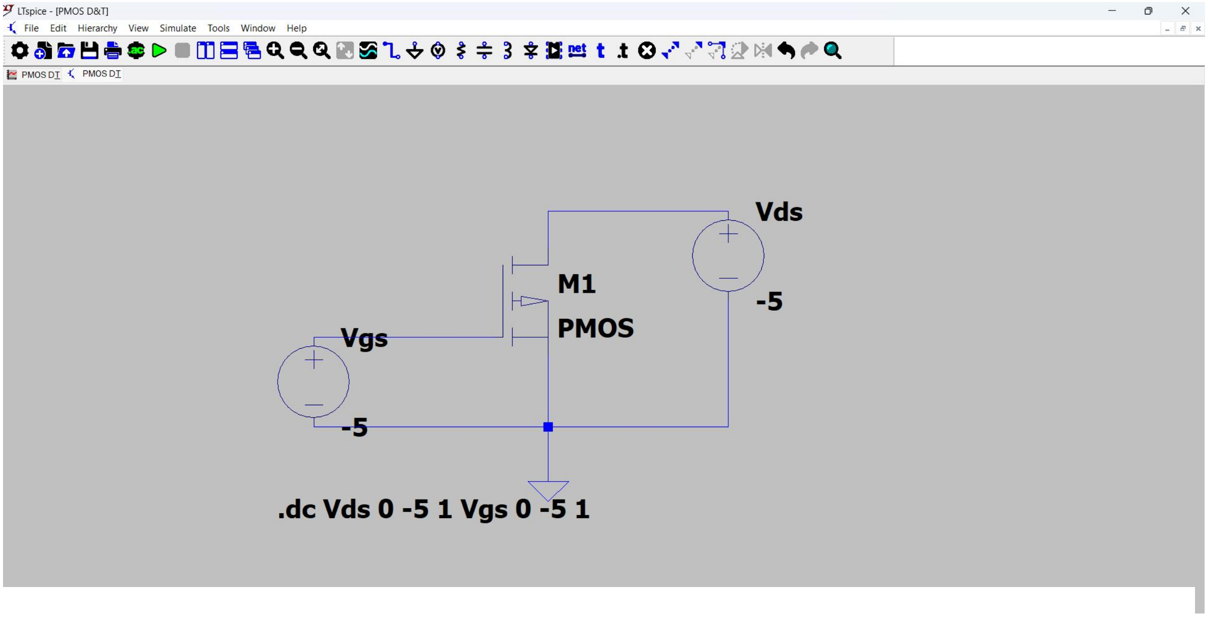
The drain and transfer characteristics of NMOS and PMOS transistors are fundamental for analyzing their behavior. The drain characteristic shows the relationship between the drain current (IDI_DID) and the drain-source voltage (VDSV_{DS}VDS) for different gate-source voltages (VGSV_{GS}VGS). The transfer characteristic relates IDI_DID to VGSV_{GS}VGS while keeping VDSV_{DS}VDS constant, highlighting the transistor's operation in cutoff, triode, and saturation regions. NMOS operates with positive voltages, while PMOS uses negative voltages. These characteristics help in designing circuits such as amplifiers and switches, providing insights into voltage and current control.

Formula:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \text{ (Saturation region for NMOS)}$$

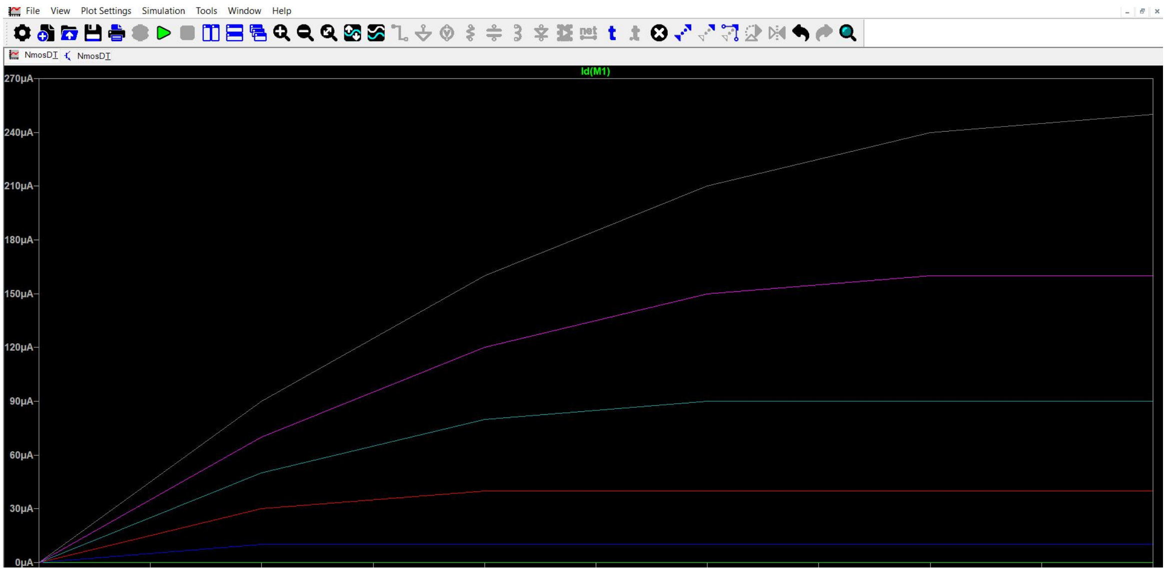
Circuit Diagram (NMOS, PMOS):



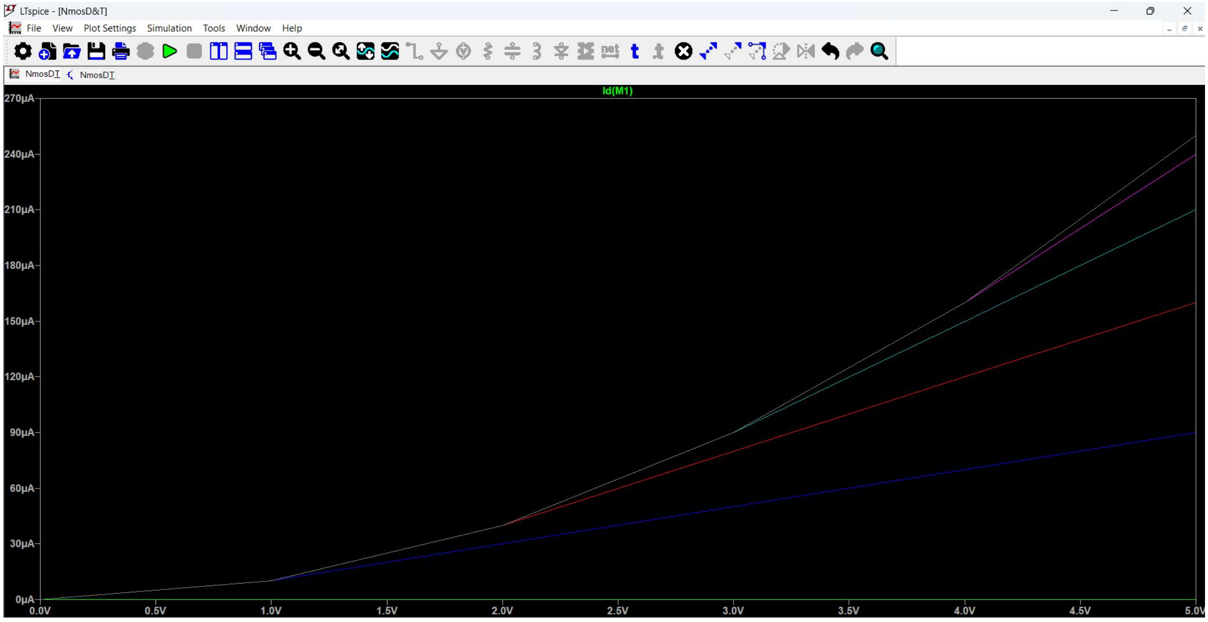


Result (Nmos, pmos):

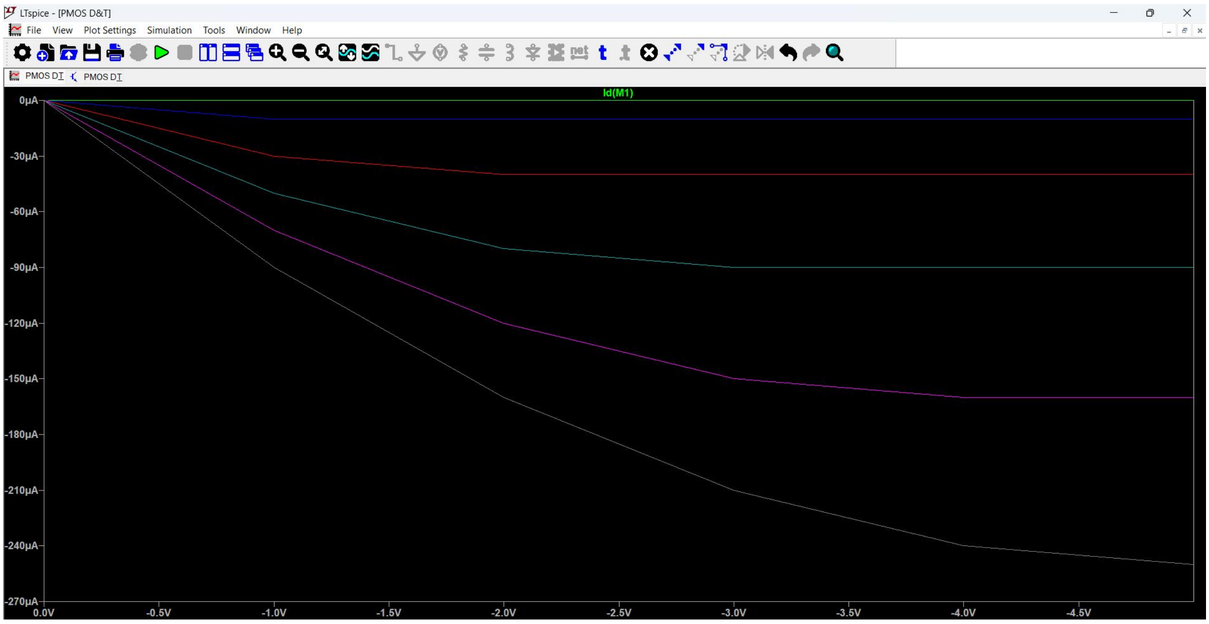
NMOS, Dran vds vs ids



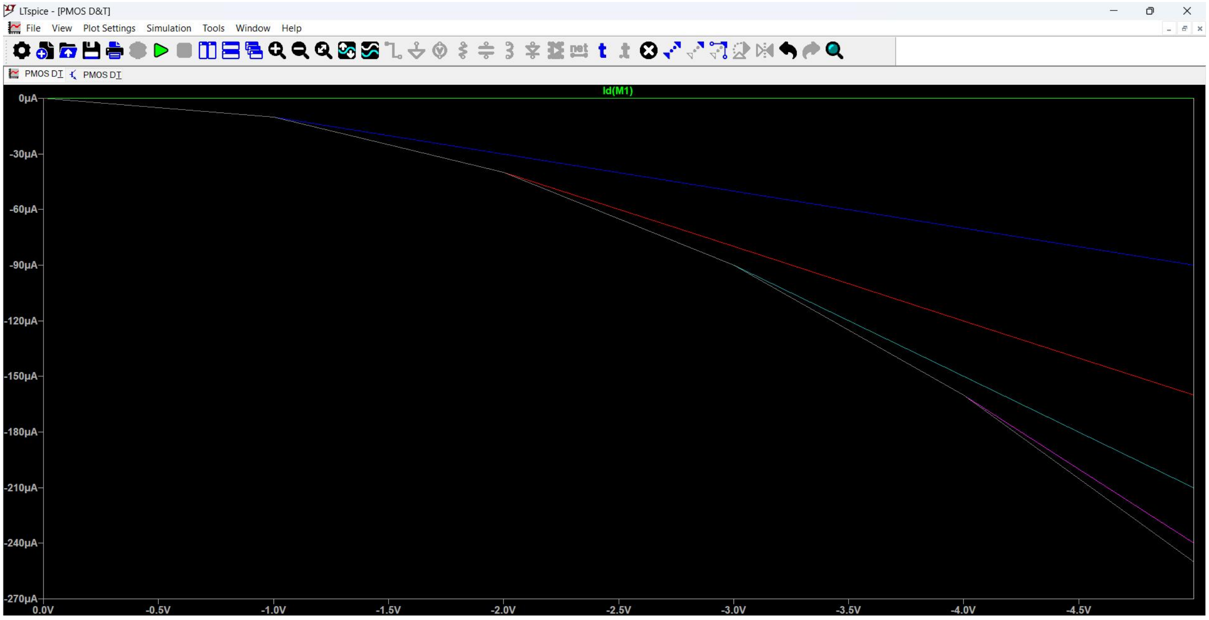
NMOS, Transfer vgs vs ids



PMOS, Dran vds vs ids



PMOS, Transfer vds vs ids



Conclusion: By observing the drain and transfer characteristic graphs, the operational behavior of NMOS and PMOS transistors is verified.

Experiment 2

AIM: NMOS Common Source Amplifier with Resistive Load.

Theory:

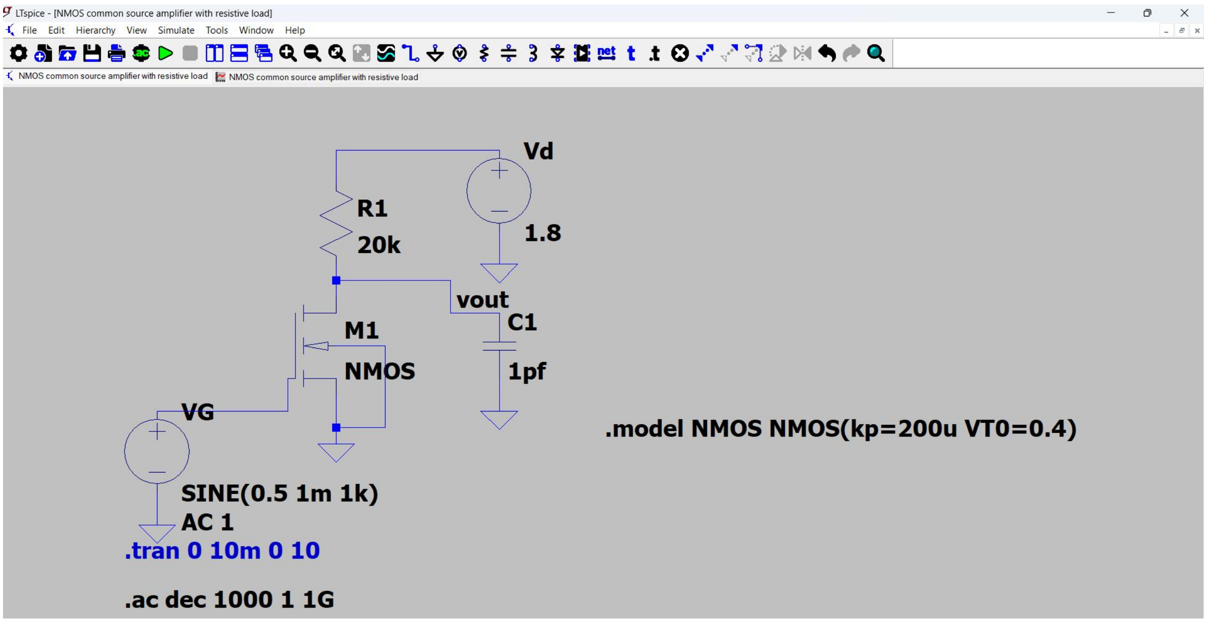
The NMOS common source amplifier is widely used for voltage amplification in analog circuits. It uses a resistive load to convert changes in the drain current (IDI_DID) to voltage variations across the load. The input signal modulates VGSV_{GS}VGS , controlling IDI_DID . A significant voltage gain is achieved by optimizing the transistor's transconductance (gmg_mgm) and the load resistance (RDR_DRD). This amplifier provides high gain but has moderate input resistance and low output resistance. Proper biasing ensures the transistor operates in the saturation region for linear amplification.

Formula:

Voltage gain: $A_v = -g_m R_D$

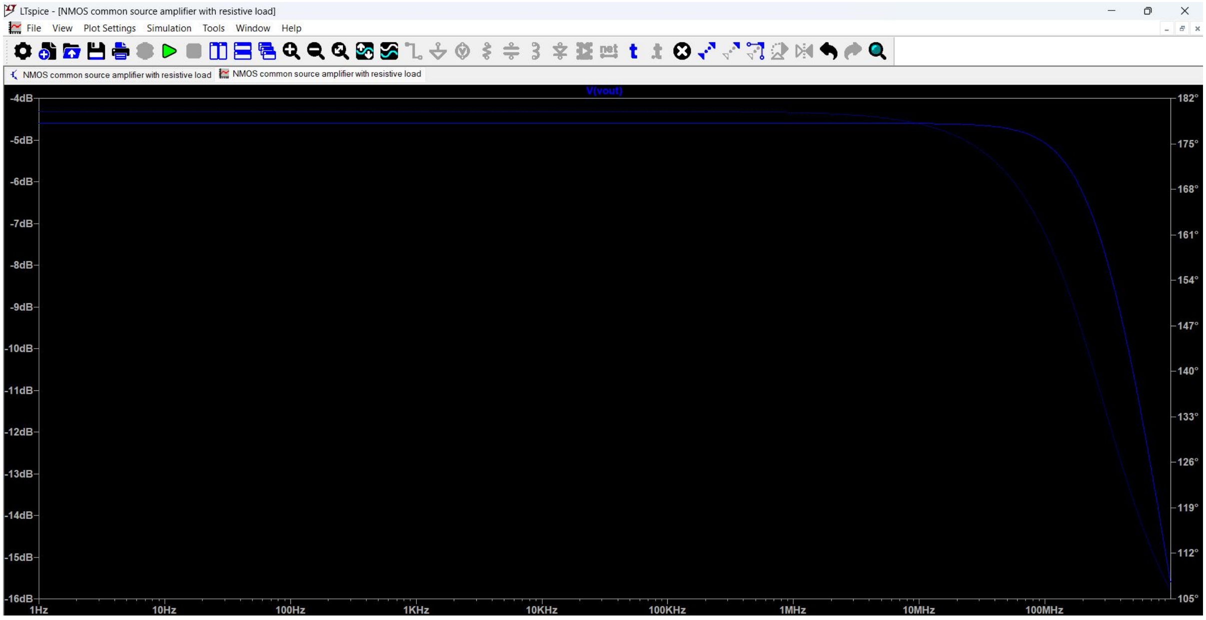
$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_D}{V_{GS}-V_{th}}$$

Circuit Diagram:

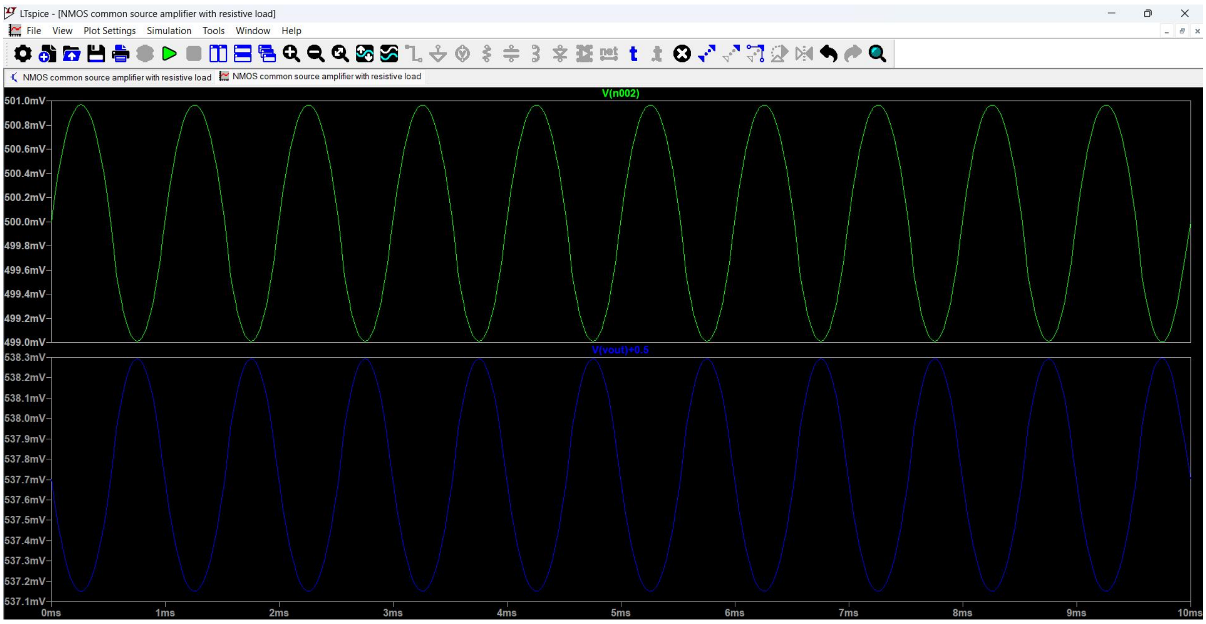


Result:

Ac Analysis



Transient Analysis



Conclusion: The input-output graphs confirm the voltage gain and functionality of the NMOS common source amplifier with resistive load.

Experiment 3

AIM: PMOS Common Source Amplifier with Resistive Load

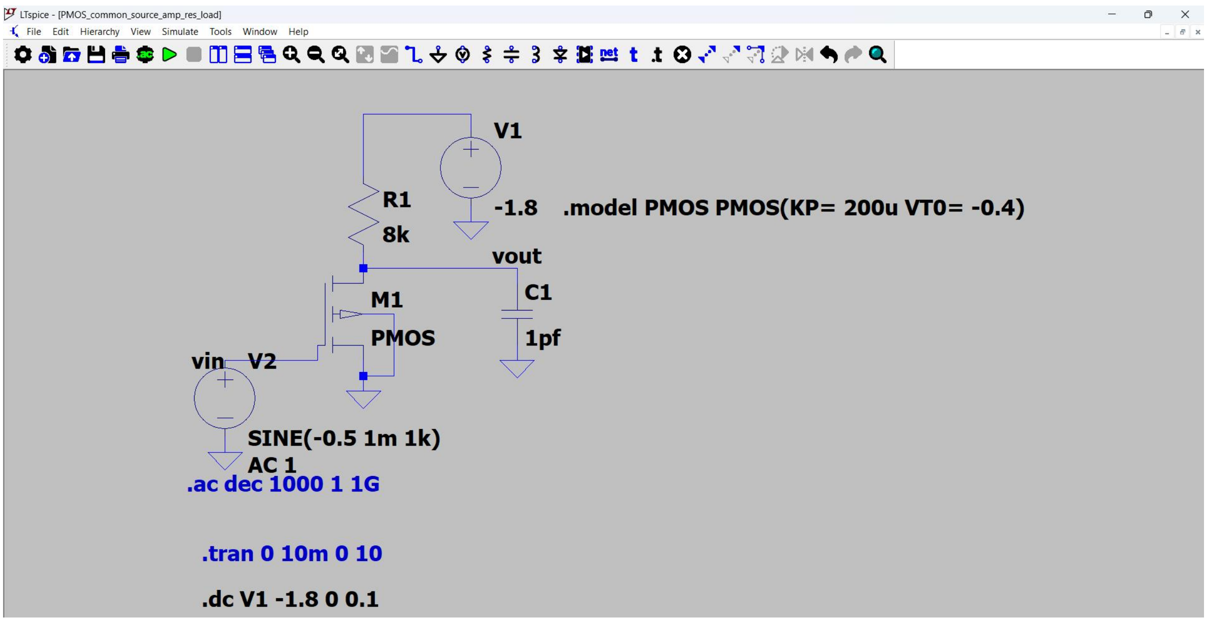
THEORY: The PMOS common source amplifier operates like the NMOS version but with reversed polarity for voltages and currents. It uses a resistive load to convert variations in the source current (ISI_SIS) to output voltage changes. The input signal modulates VSGV_{SG}VSG , driving the transistor into saturation for amplification. This configuration is particularly suited for high-side amplification. While it has lower electron mobility compared to NMOS, it is still effective in achieving significant voltage gain by careful design of the load resistance and device parameters.

Formula:

Voltage gain: $A_v = -g_m R_D$

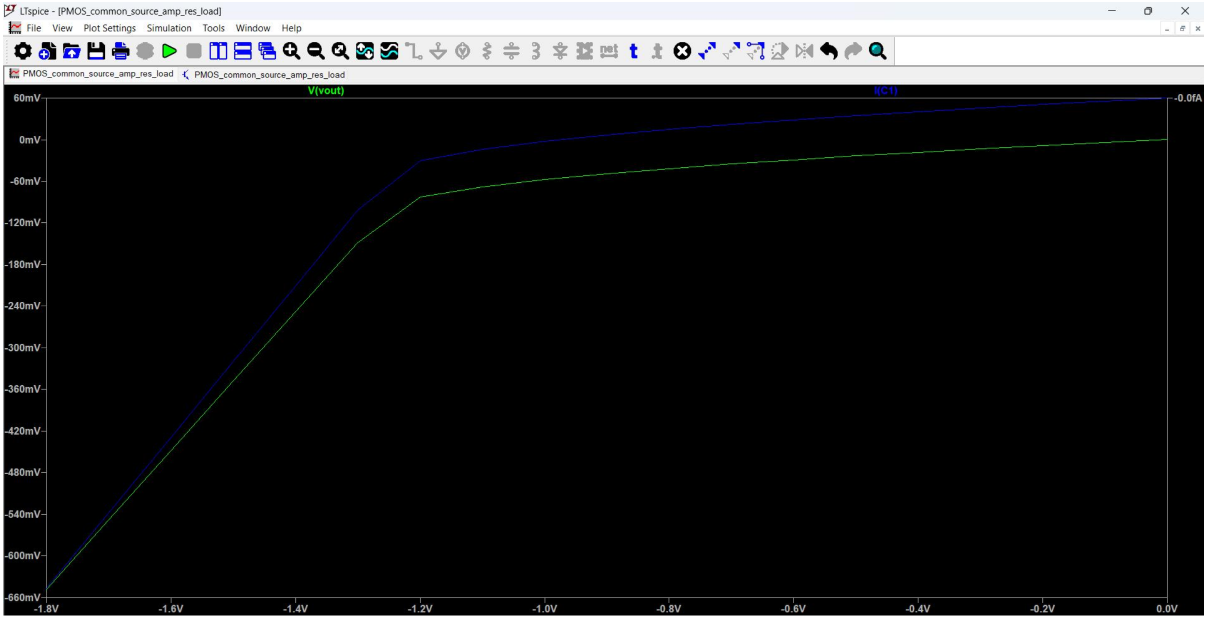
$$g_m = \frac{2I_S}{V_{SG} - |V_{th}|}$$

Circuit Diagram:

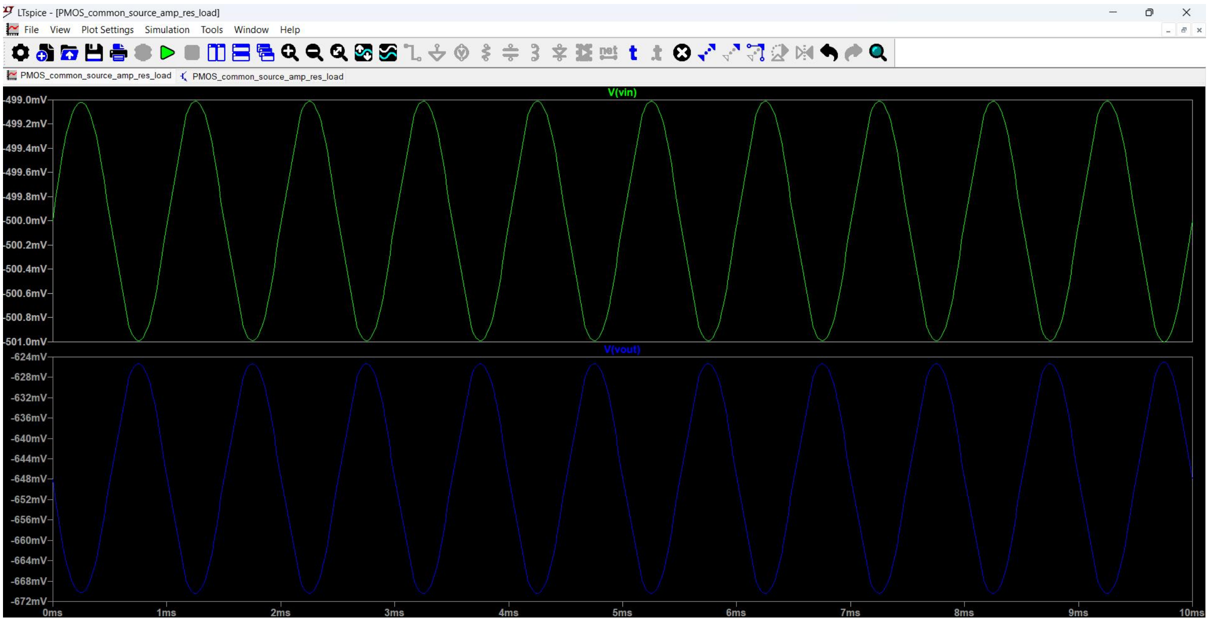


Result:

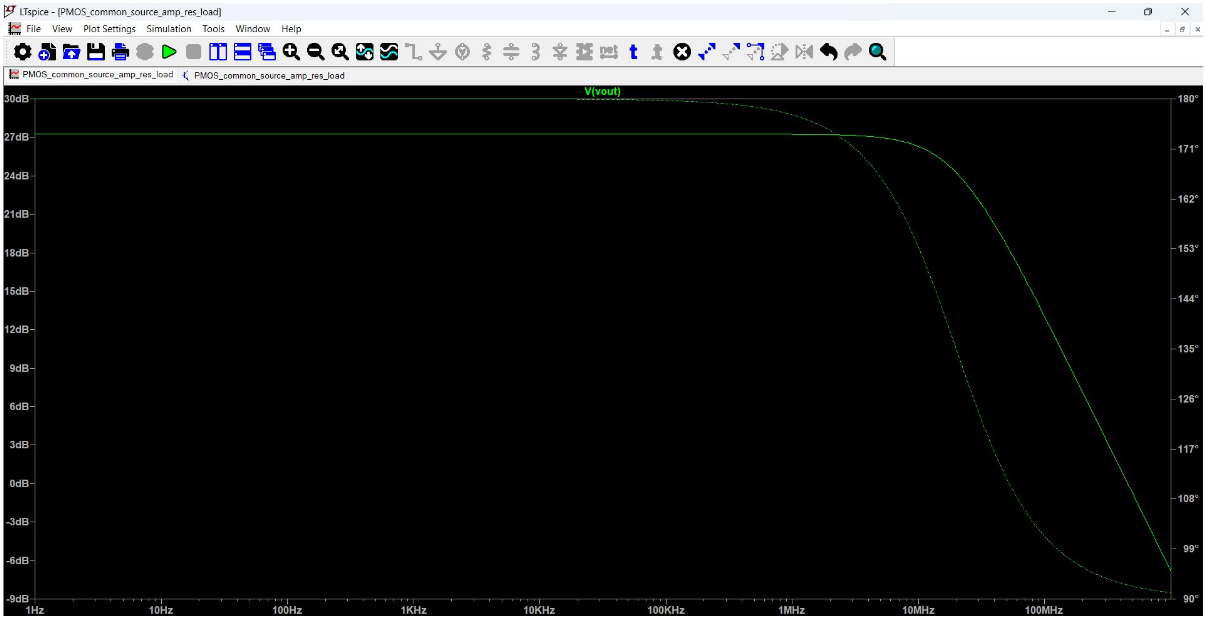
DC Sweep Analysis



Transient Analysis



Ac Aanlysis



Conclusion: Graphical analysis verifies the performance and voltage amplification of the PMOS common source amplifier using a resistive load.

Experiment 4

Aim: Common Source Amplifier with Degenerative Resistance

THEORY:

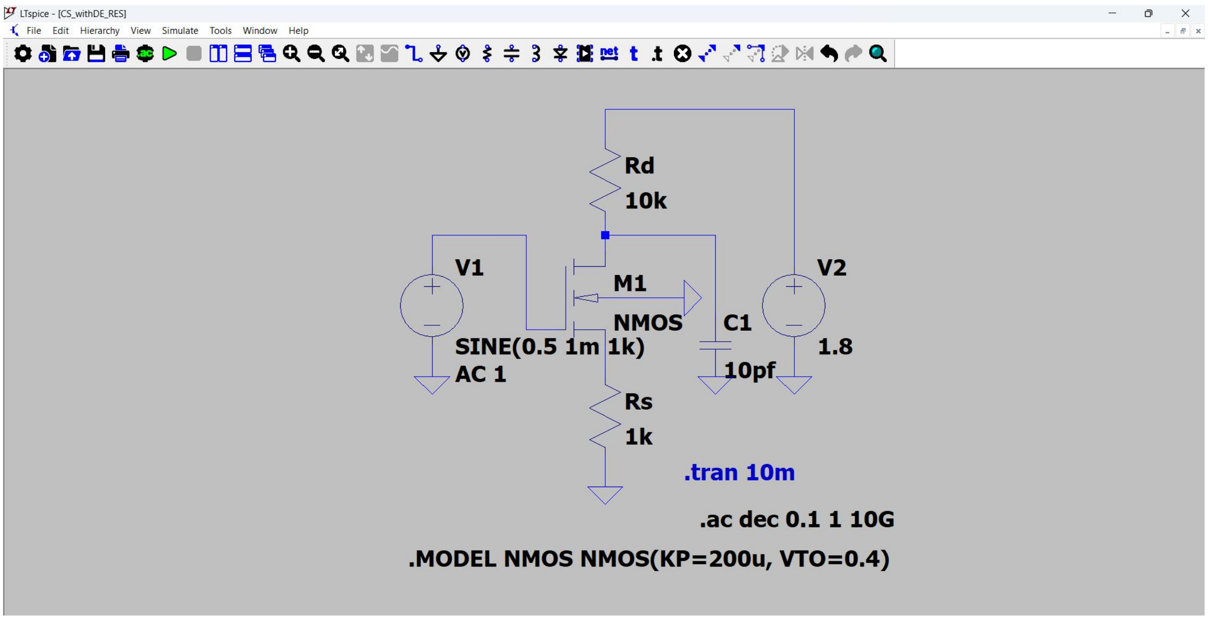
Degenerative resistance introduces negative feedback in a common source amplifier by adding a source resistor (RSR_SRS). This feedback stabilizes the amplifier's operating point, reduces distortion, and improves linearity. Negative feedback decreases the effective transconductance (gm,effg_{m,eff}gm,eff), leading to a lower but more stable voltage gain. The trade-off between gain and stability is controlled by RSR_SRS . This configuration is often used in applications requiring precision and reliability in signal amplification.

Formula:

Effective transconductance: $g_{m,eff} = \frac{g_m}{1+g_m R_S}$

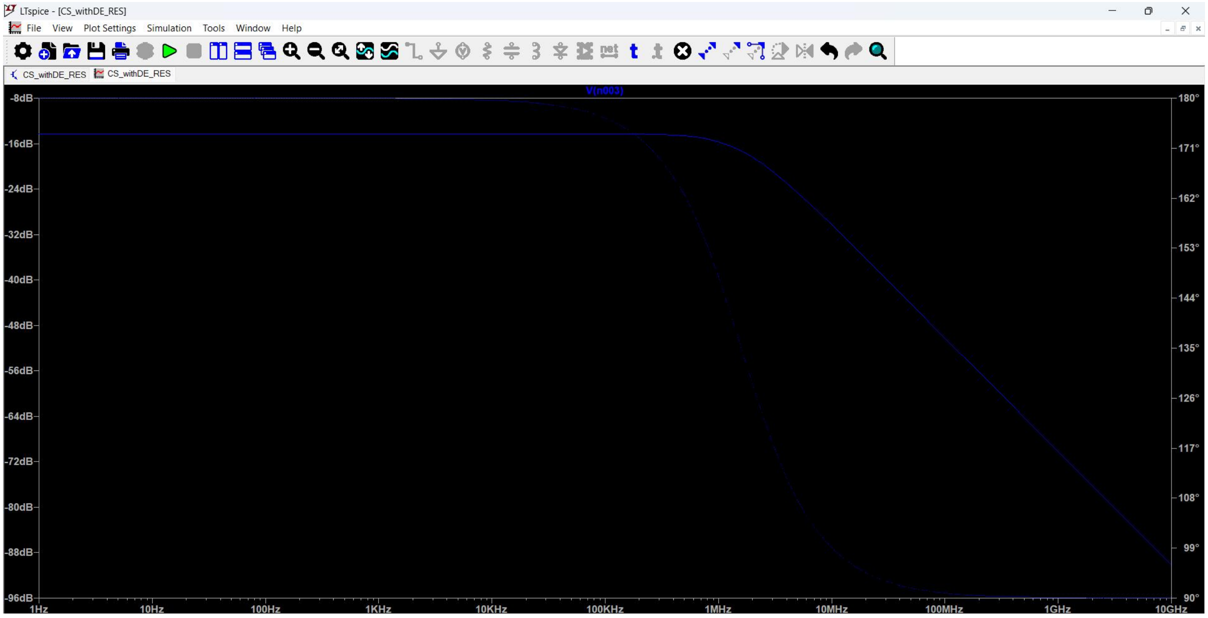
Voltage gain: $A_v = -\frac{g_m R_D}{1+g_m R_S}$

Circuit Diagram:

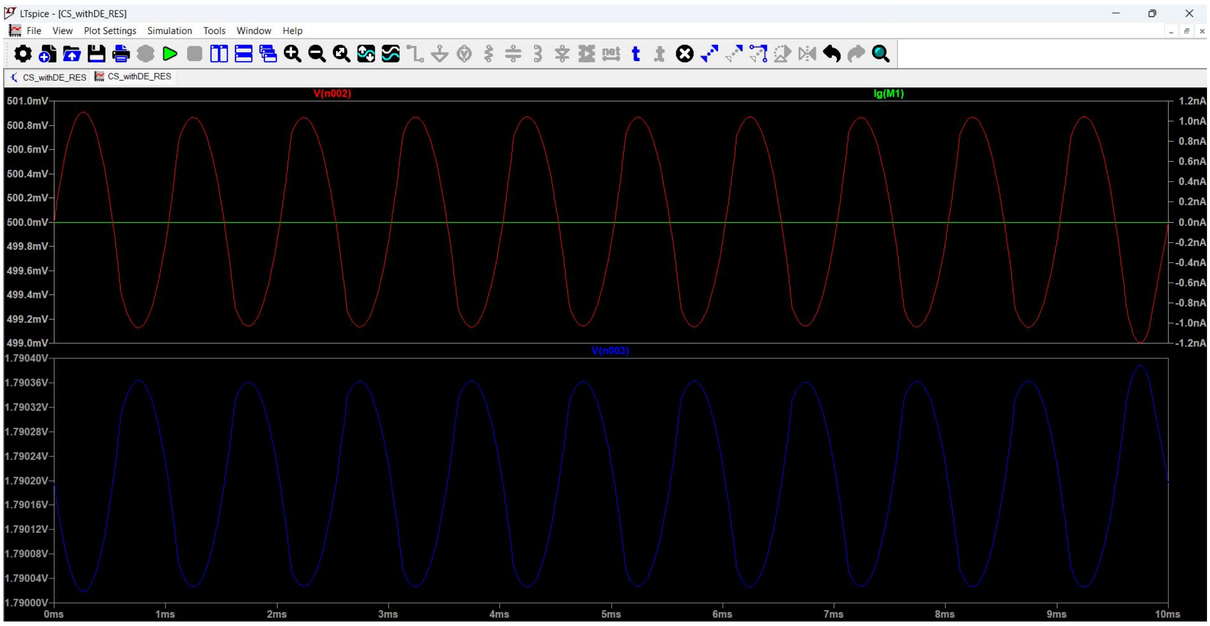


Result:

Ac Analysis



Transient Analysis



Conclusion: The observed graphs demonstrate the impact of degenerative resistance on stability, linearity, and reduced distortion in the amplifier.

Experiment 5

Aim: Common Source Amplifier with Diode-Connected NMOS Load

THEORY:

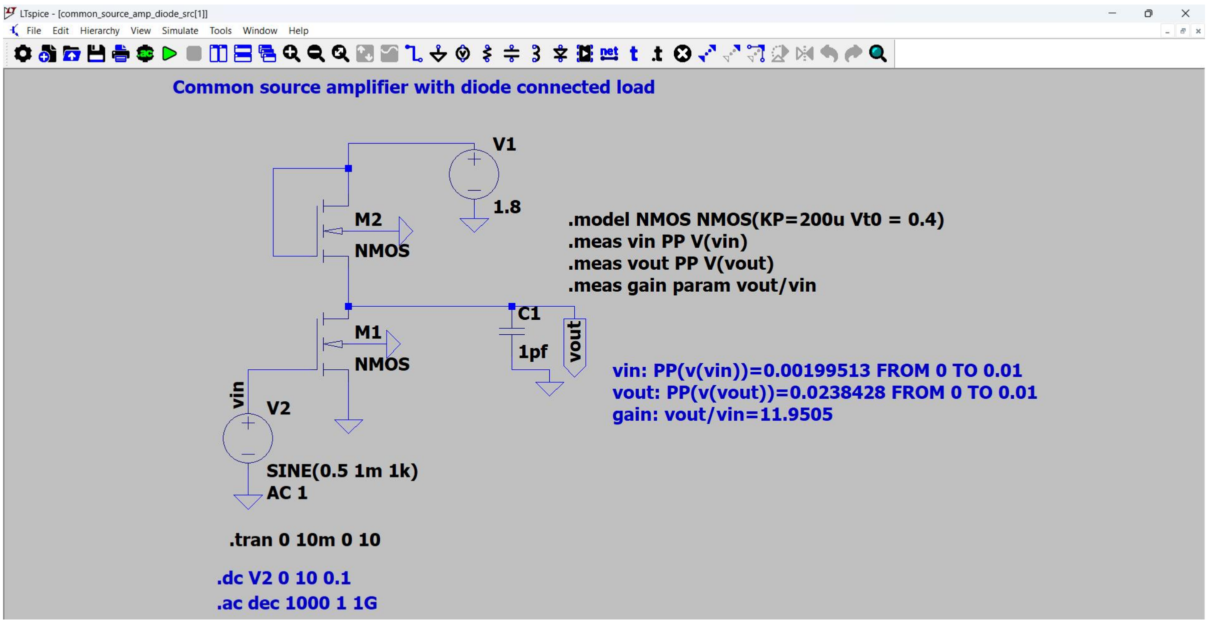
A diode-connected NMOS load uses an NMOS transistor with its gate and drain shorted, ensuring it operates in saturation. This configuration provides high output impedance, which enhances voltage gain. The diode-connected load is often used in analog circuits to achieve linear amplification while maintaining a simple design. The output voltage varies with the input signal, as the load provides a constant current pathway, ensuring stable operation.

Formula:

Load impedance: $R_{load} = \frac{1}{g_{m,load}}$

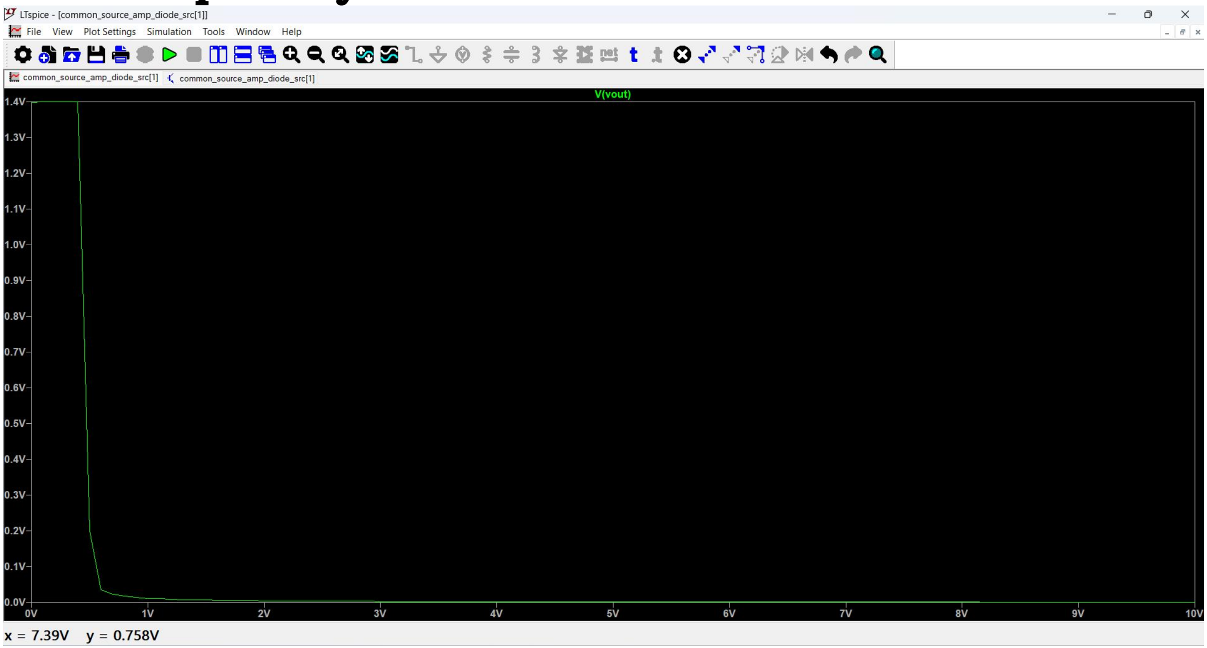
Voltage gain: $A_v = -\frac{g_m}{g_{m,load}}$

Circuit Diagram:

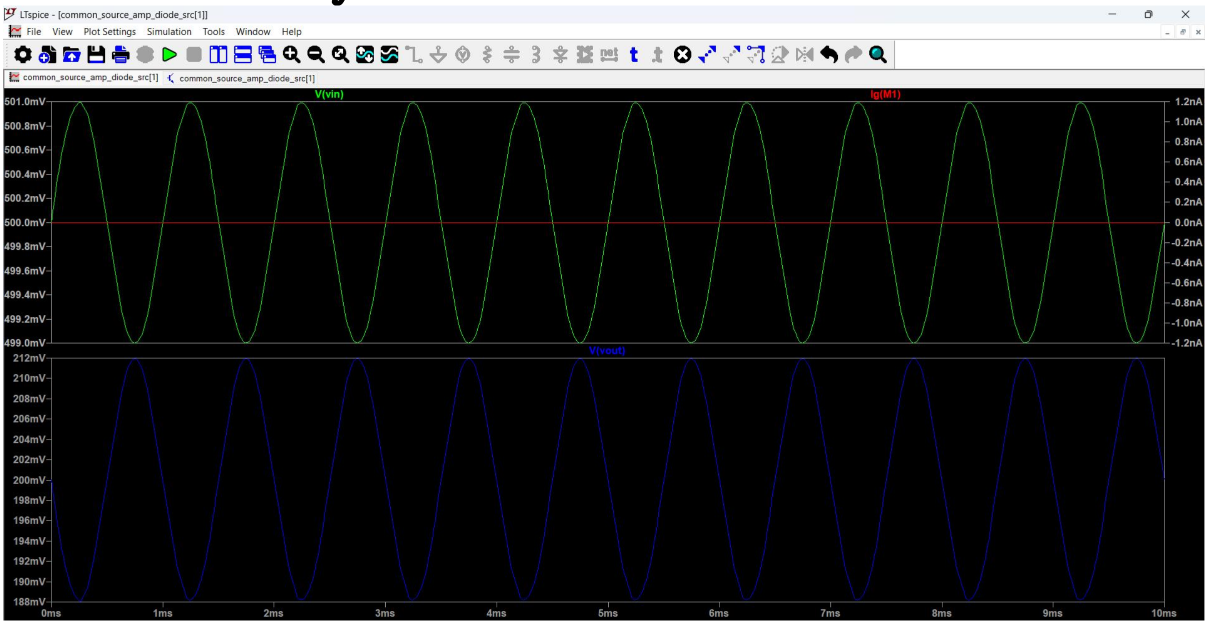


Result:

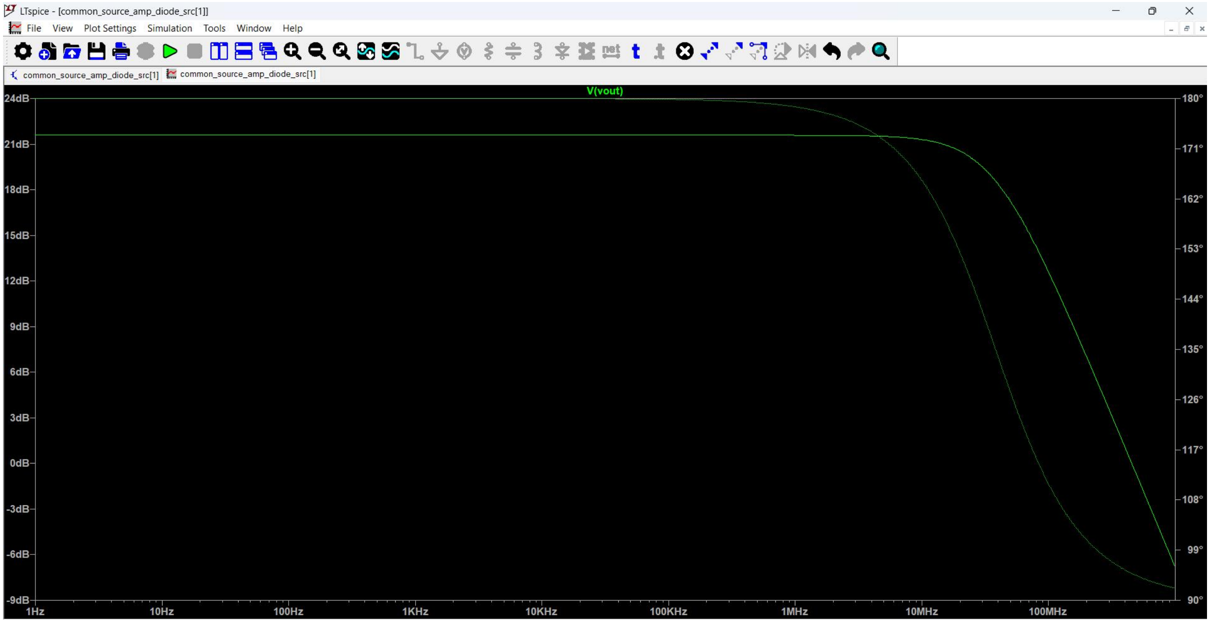
DC Sweep Analysis



Transient Analysis



AC Analysis



Conclusion: Graphical results validate the improved gain and linearity provided by the diode-connected NMOS load in the amplifier circuit.

Experiment 6

AIM: Common Source Amplifier with Diode-Connected PMOS Load

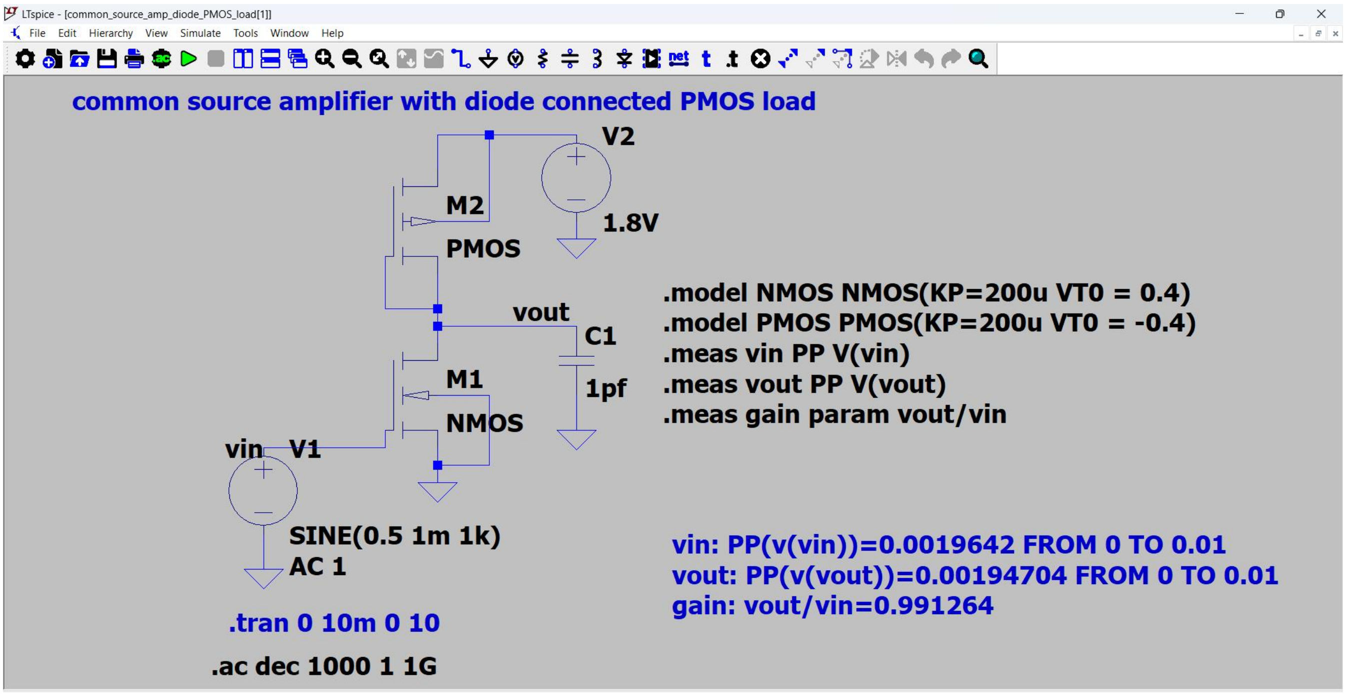
THEORY: The diode-connected PMOS load functions similarly to the NMOS version, providing high impedance at the output. It is used in circuits requiring a pull-up load. The PMOS transistor's source-drain current flows through the load, allowing voltage gain proportional to the transconductance ratio. This configuration ensures stable amplification and is often seen in complementary metal-oxide-semiconductor (CMOS) analog circuits.

Formula:

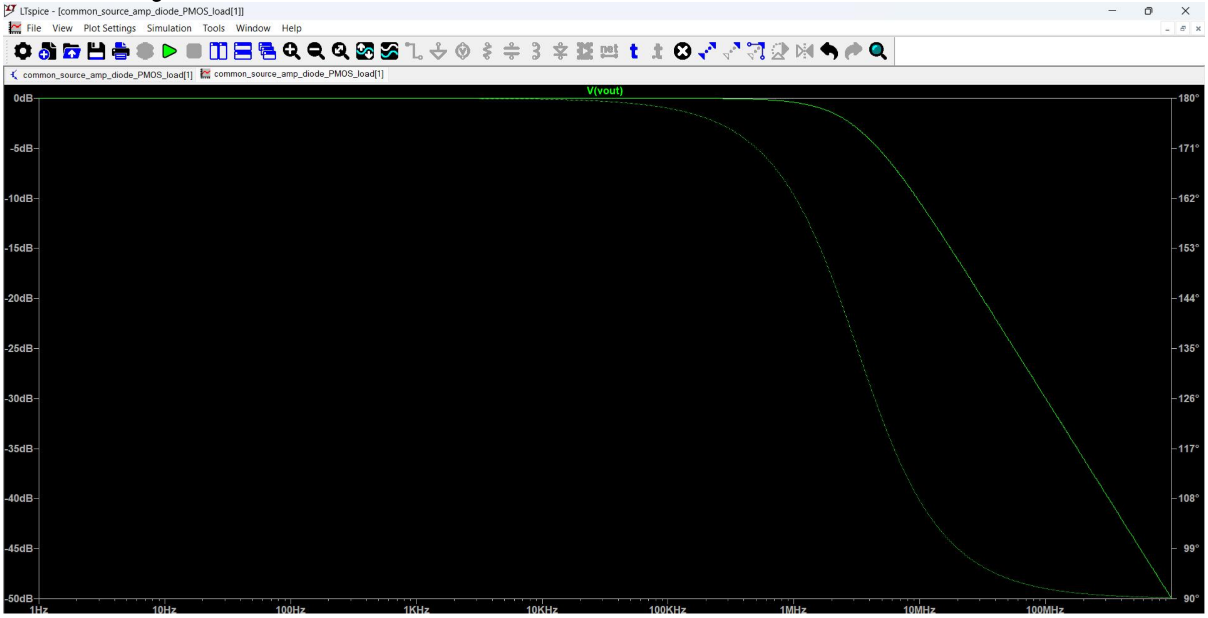
Load impedance: $R_{load} = \frac{1}{g_{m,load}}$

Voltage gain: $A_v = -\frac{g_m}{g_{m,load}}$

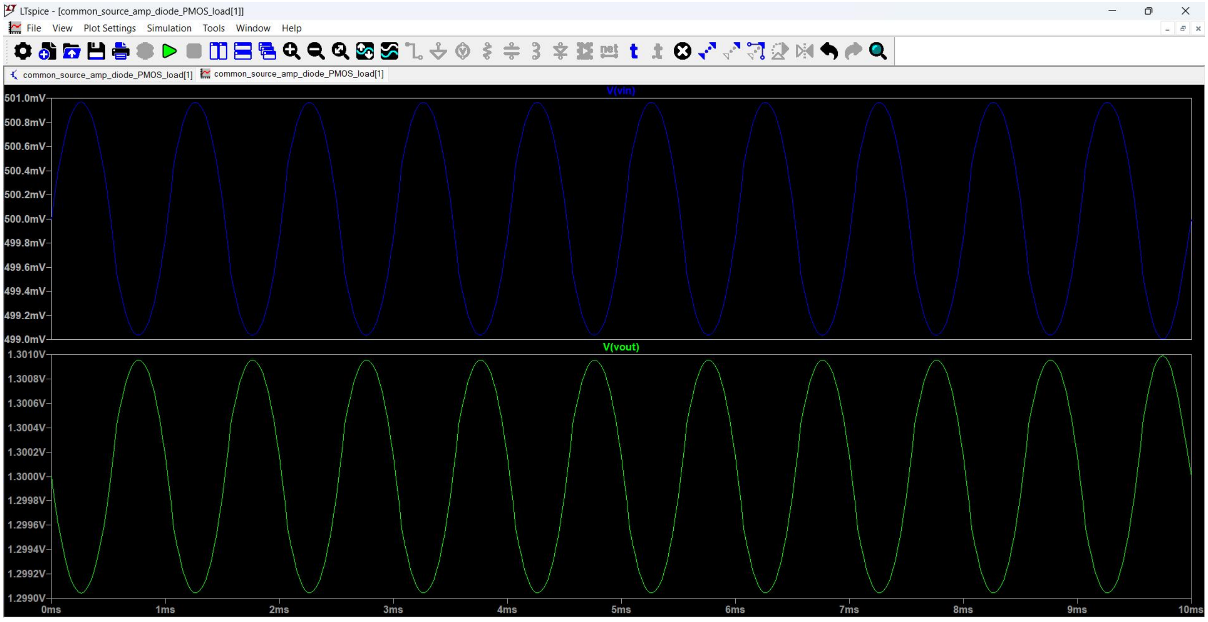
Circuit Diagram:



Result
Ac Analysis



Transient Analysis



Conclusion: The output graphs confirm the high impedance and stable gain achieved with the diode-connected PMOS load configuration.

Experiment 7

Aim: Common Source Amplifier with Current Source Load

THEORY:

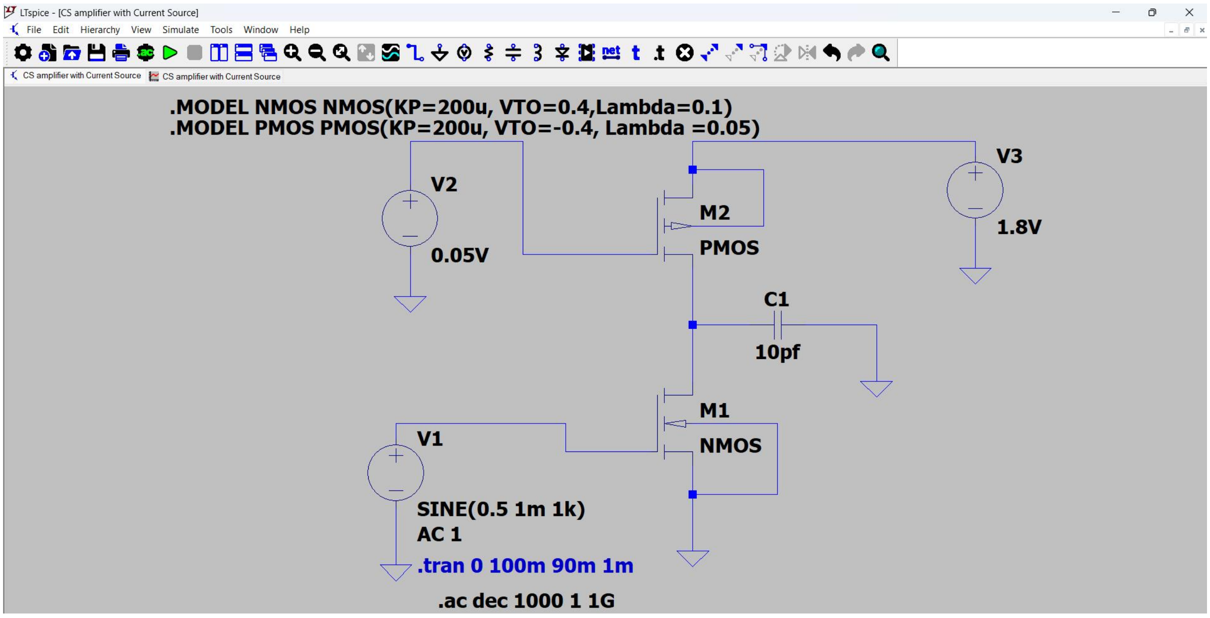
A current source load in a common source amplifier provides an almost infinite load resistance, maximizing voltage gain. The constant current source ensures minimal distortion, enabling the amplifier to operate efficiently. This configuration is common in high-performance analog circuits. The voltage gain is determined by the product of transconductance (gmg_mgm) and the effective output resistance.

Formula:

$$\text{Voltage gain: } A_v = -g_m R_{out}$$

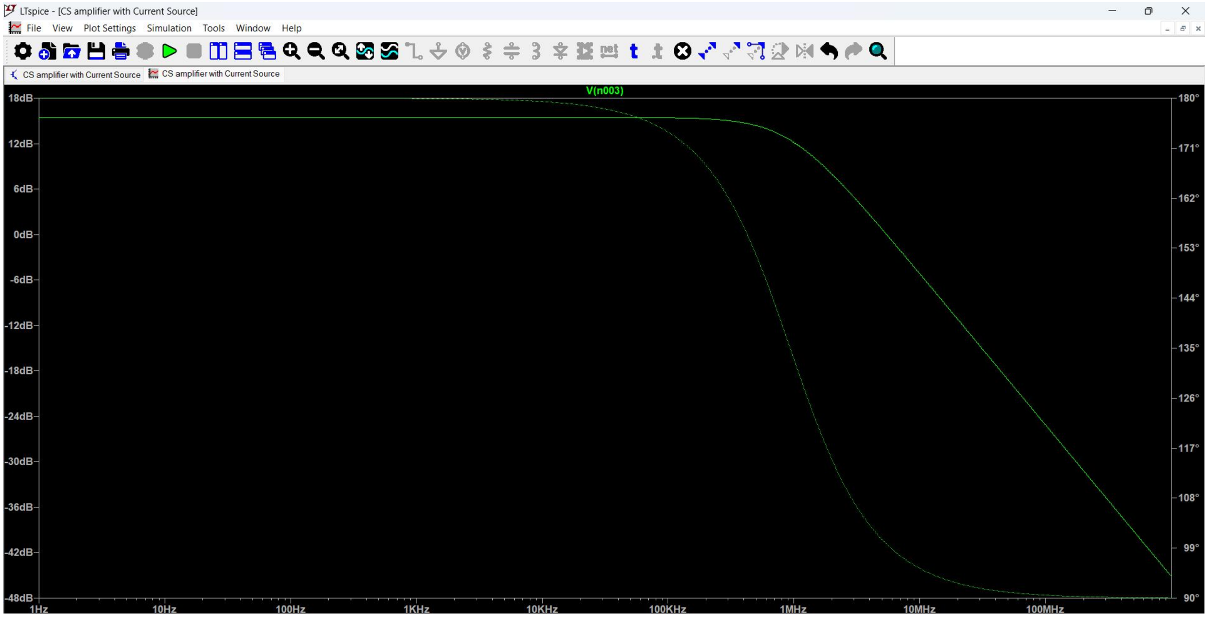
$$\text{Output resistance: } R_{out} = R_{load} \parallel R_{source}$$

Circuit Diagram:

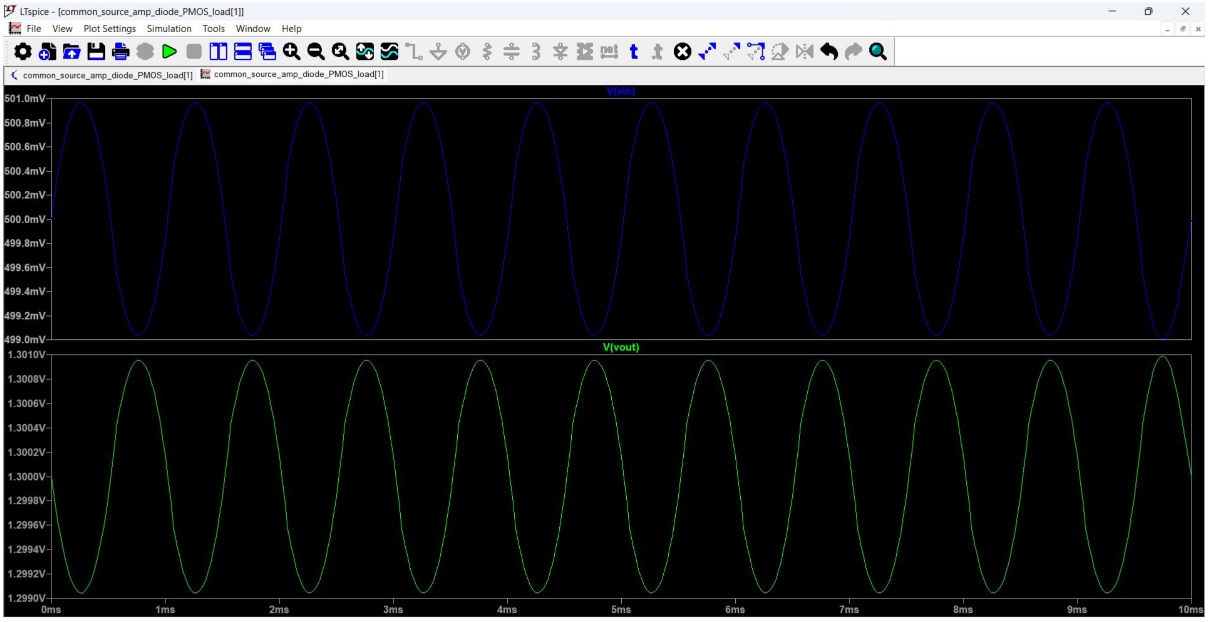


Result:

Ac Analysis



Transient Analysis



Conclusion: Graph analysis shows the increased gain and minimized distortion due to the current source load in the amplifier.

Experiment 8

AIM: Source Follower Circuit Using Resistive Load

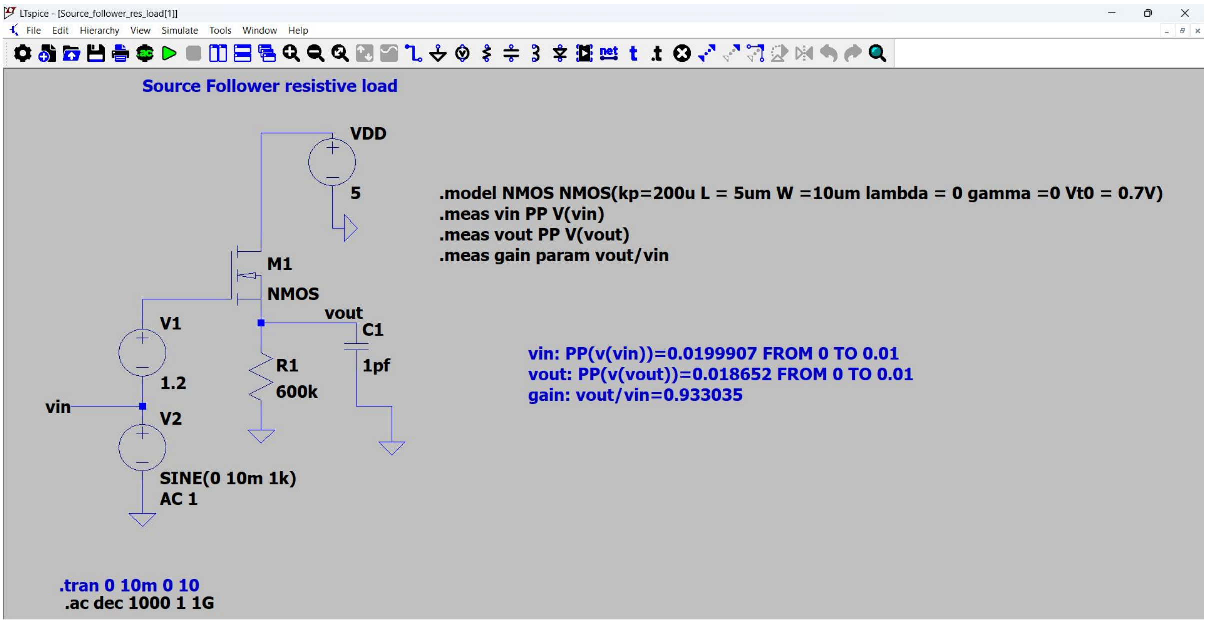
THEORY: The source follower, or common drain amplifier, provides voltage buffering with unity gain. Its high input impedance and low output impedance make it ideal for impedance matching. The input signal modulates VGSV_{GS}VGS , producing a source voltage close to the input voltage, minus a small drop. While it does not amplify the input voltage, it is efficient in maintaining signal integrity for interfacing stages.

Formula:

Voltage gain: $A_v \approx \frac{1}{1+\frac{1}{g_m R_S}}$

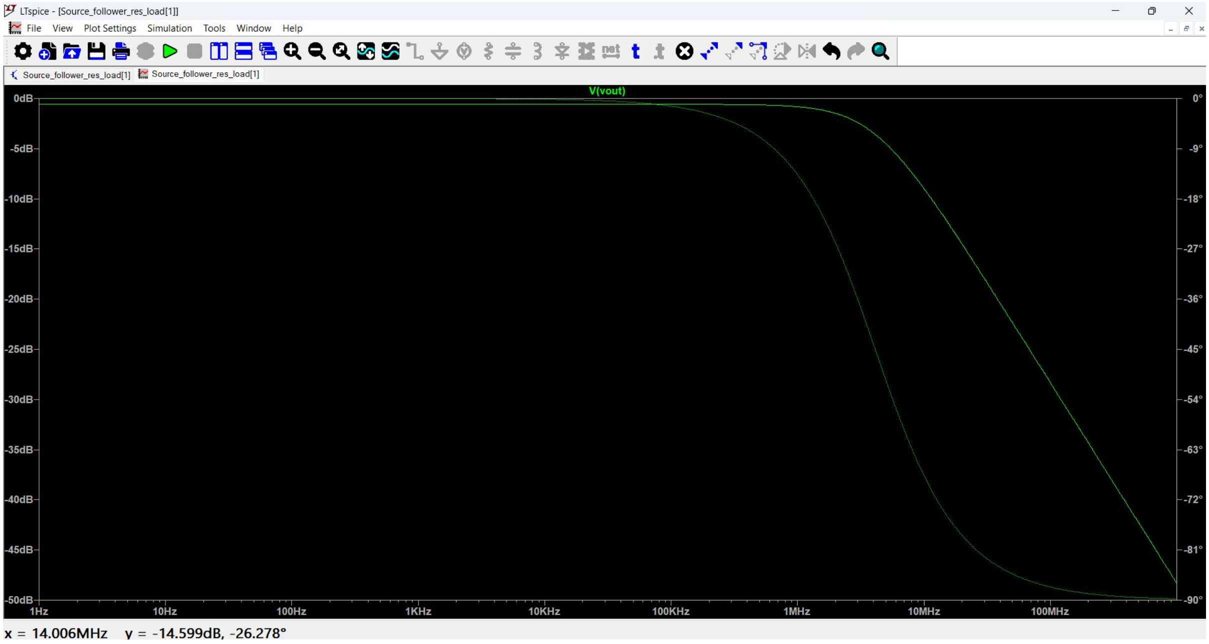
Output impedance: $Z_{out} = \frac{1}{g_m + g_m^2 R_S}$

Circuit Diagram:

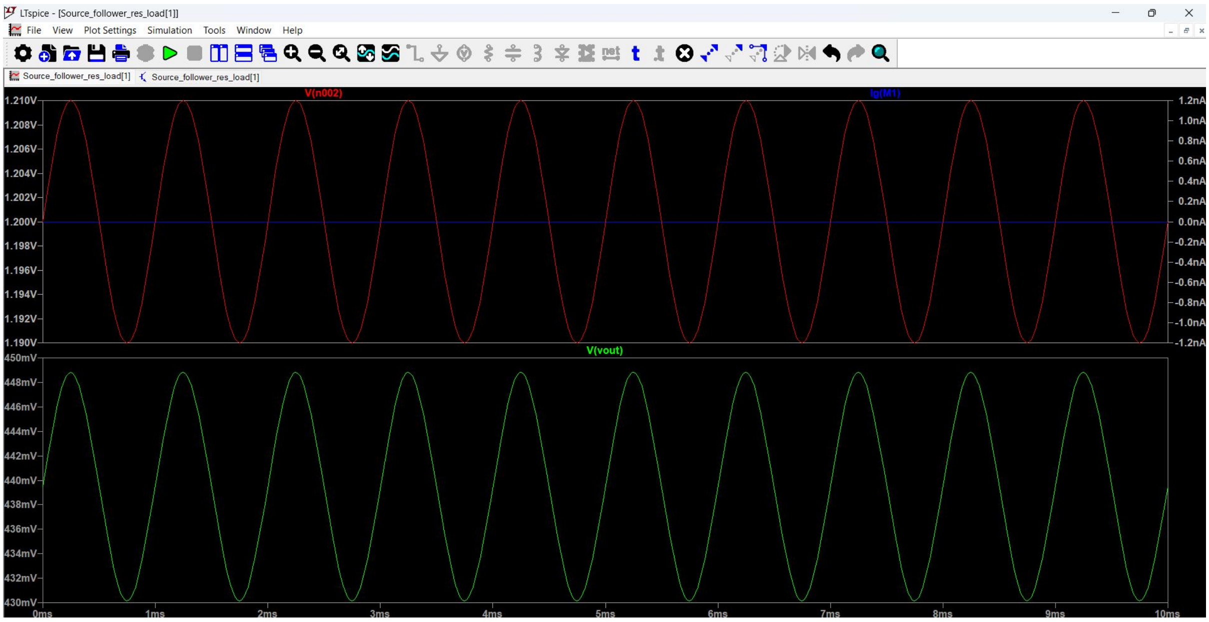


Result:

Ac Analysis



Transient Analysis



Conclusion: By examining the graphs, the source follower's impedance matching and unity gain characteristics are verified effectively.

Experiment 9

AIM: Common Gate Amplifier

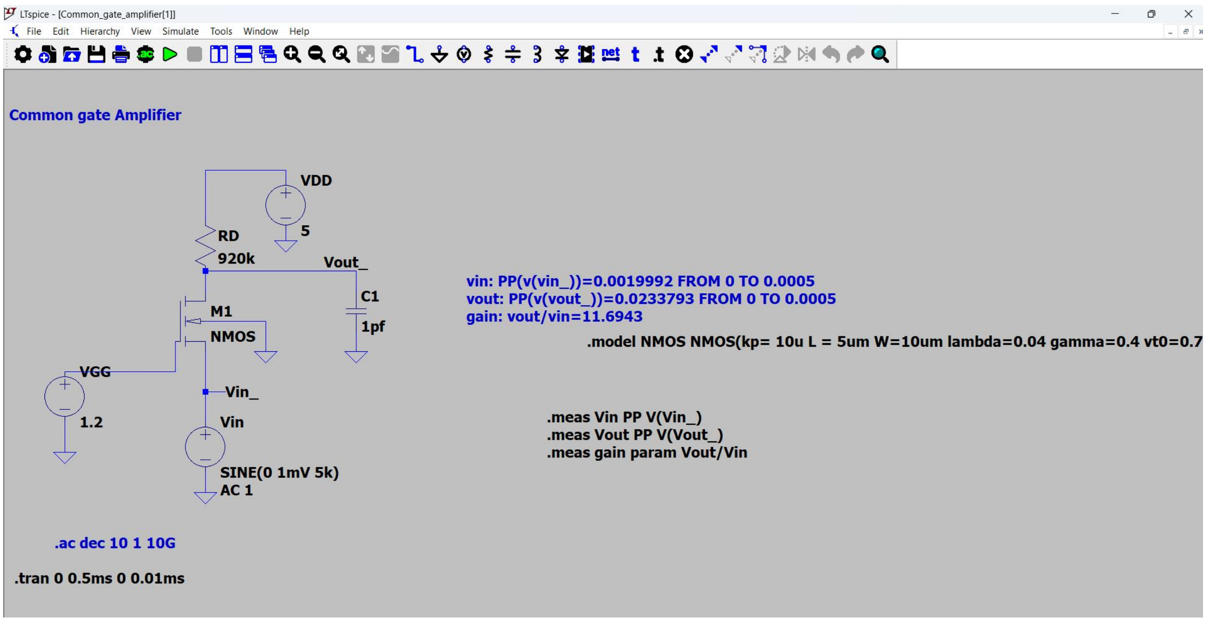
THEORY: The common gate amplifier is known for its low input impedance and high-frequency response. The input signal is applied at the source, while the gate is held at a fixed voltage. This configuration is suitable for amplifying high-frequency signals and impedance matching in RF circuits. It offers a moderate voltage gain with no phase inversion, making it versatile in analog signal processing.

Formula:

Voltage gain: $A_v = g_m R_D$

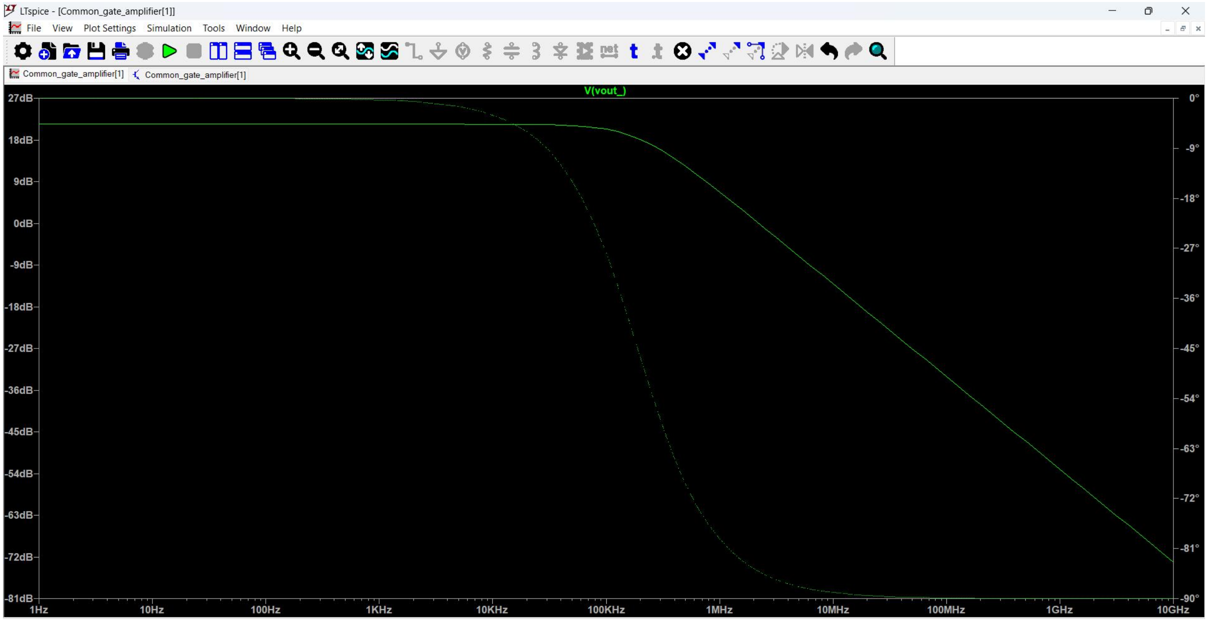
Input impedance: $Z_{in} \approx \frac{1}{g_m}$

Circuit Diagram:

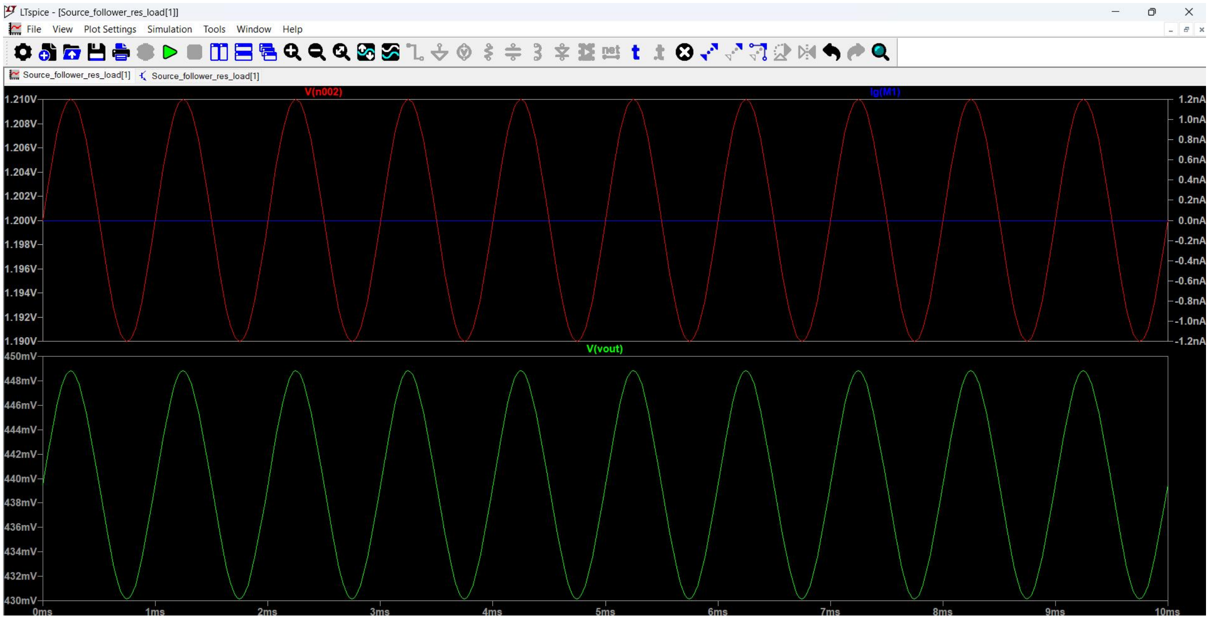


Result:

AC Analysis



Transient Analysis



Conclusion: The observed graphs confirm the common gate amplifier's low input impedance and moderate voltage gain without phase inversion.