Department of Computer Science & Engineering
Winter 2019-2020

Tentative Schedule for CS2093D Hardware Lab

Sl No.	Date of the Lab session	Submission	Topic	Maximum Marks
1	Jan 2	Theory class		0 marks
2	Jan 6, 7, 9	Theory class		0 marks
3	Jan 16	Practice session		0 marks
4	Jan 23	Assignment-1 (Evaluation)	Integer Handling	5 marks
5	Jan 30	Assignment-2 (Evaluation)	Array Handling	5 marks
6	Feb 6	**Test1**		**20 marks**
7	Feb 13	Assignment -3 (Evaluation)	String Handling	5 marks
8	Feb 27	Assignment -4 (Evaluation)	floating point operations	5 marks
9	Mar 5	**Test2**		**20 marks**
10	Mar 12	Theory class (Design of processor using Verilog)		0 marks
11	Mar 19	Practice session		5 marks
12	Mar 26	Practice session		
13	Apr 2	**Test-3**		**25 marks**
14	April 9	**Viva exam**		**20 marks**

N.B:

- The 5 marks for each assignment consist of 2 marks for submission and 3 marks for modification.
- The total marks scored for the assignment evaluations will be downscaled to 10 Marks at the end!!!