University of Engineering & Management

UEM KOLKATA

श्रद्धावान लभते ज्ञानम्

Good Education, Good Jobs

CS391 – Analog & Digital Electronics Lab

Experiment List (Week wise)

WEEK-1	1) Familiarity with basic gates ICs (AND,OR, NOT and XOR) and Realization of NOT,AND,OR and XOR operations by using universal gates (both NAND and NOR). 2) Design a circuit to indicate 4 bit odd and even numbers. 3) Realization of a circuit to display prime and non prime numbers (4 bit). 4) Implementation of Half Adder. Implementation of Full Adder. Carryout expression is implemented by basic gates.
WEEK-2	5) Implementation of Full Adder by using 2 half Adders and an OR gate. 6) Implementation of Half Subtractor. 7) Implementation of Full Subtractor. Borrowout expression is implemented by basic gates. 8)Implementation of Full Subtractor using 2 Half Subtractors and an OR gate.
WEEK-3	9) Realization of a circuit to convert BCD to Excess -3 codes. 10) Realization of a circuit to convert Excess -3 codes to BCD. 11) Design a circuit to convert 4 bit Binary to 4 bit Gray code. 12) Design a circuit to convert 4 bit Gray code to 4 bit Binary.
WEEK-4	13) Realization of an Even Parity Generator and Checker circuit. 14) Implementation of 2 bit comparator circuit. 15) Realization of the internal architecture of 4:1 Multiplexer and 1:4 De-multiplexer.
WEEK-5	16) Implementation of Full Adder using MUX 74153. 17) Implementation of Full Subtractor using 74153. 18) Realization of 4:2 Priority Encoder along with output indicator (basic gates).
WEEK-6	19) Realization of the internal architecture of 3:8 Decoder using basic gates. 20) Realization of octal to binary encoder using basic gates. 21) Implement Full Adder using 74138. 22) Implement Full Subtractor using 74138.
WEEK-7	23) Truth table verification of SR flip-flop (using NAND gates only). 24) Truth table verification of D flip-flop (using NAND gates only). 25) Truth table verification of JK flip-flop (using NAND gates only). 26) Truth table verification of T flip-flop (using NAND gates only). 27) Design a Master slave flip-flop.

WEEK-8	28) Design 4-bit synchronous up counter. 29) Design 4-bit synchronous down counter. 30) Design 4-bit asynchronous up counter. 31) Design 4-bit asynchronous down counter.
WEEK-9	32) Design a 3-bit synchronous up/down' counter using JK flip-flop with external mode signal M. If M=1,counter counts up and with M=0, counter counts down. 33) Design and implement MOD-4 Ring counter.
WEEK-10	35) Realization of Serial-in-Serial-Out shift register. 36) Realization of Serial-In-Parallel Out Shift register. 37) Realization of Parallel-In-Parallel Out Shift register. 38) Realization of Parallel-In-Serial Out Shift register.
WEEK-11	39) Realization of Bidirectional shift register (All using D flip-flops). 40) Analog Electronics Experiments: a) Design of a Schmitt Trigger using 555 timer. b) Design of a Class A amplifier.