

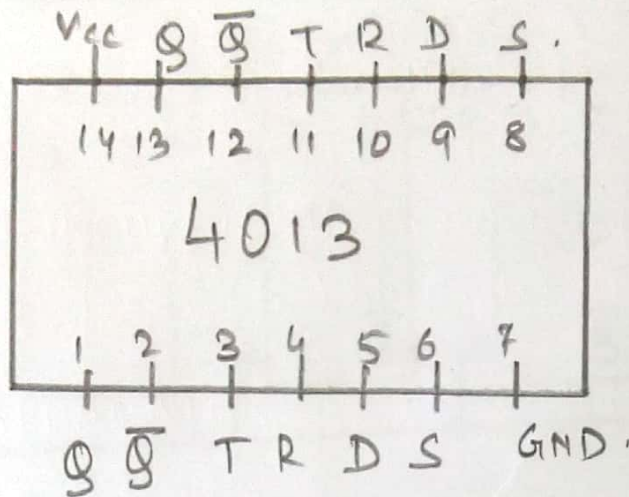
EXPERIMENT NUMBER - 35 :-TITLE :- Realization of Shift-Register Circuit.OBJECTIVE :- Realization of Shift-Register Circuit,  
(a) SISO, (b) SIPO, (c) PIPO, (d) PISO.APPARATUS REQUIRED :-

S/No	Component's Name	Specification	QTY
1	D Flip-Flop	4013	2
2	Breadboard Kit	-	1
3	Wires	-	1 bunch

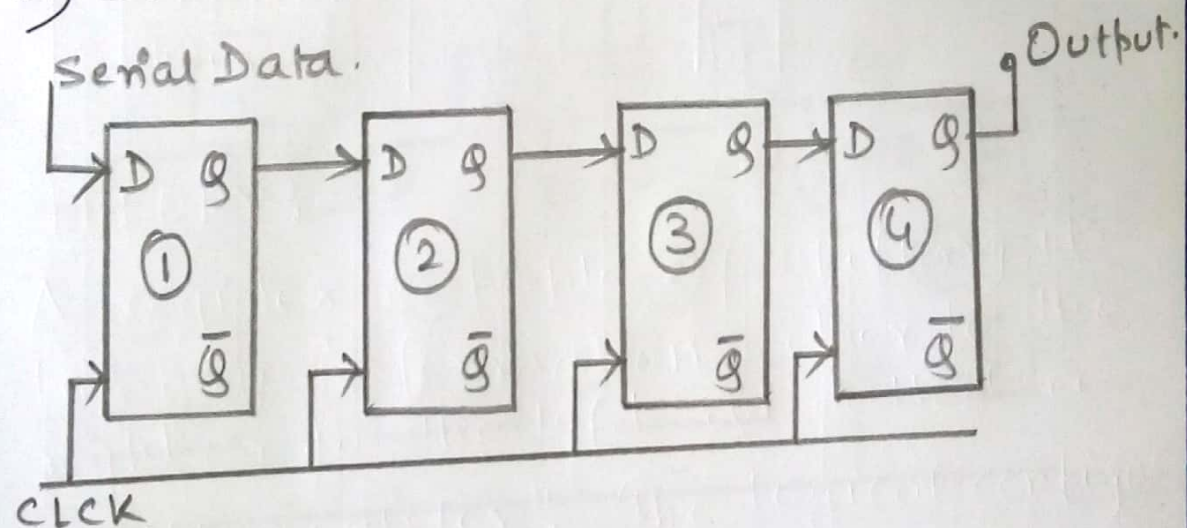
THEORY :-

A register capable of shifting its binary information either to the right or to the left is called a "shift register". The logical configuration of a shift-register consists of a chain of flip-flops connected in cascade, with the output of one flip-flop connected to the input of the next flip-flop. All flip-flops receive a clock pulse which causes the shift.

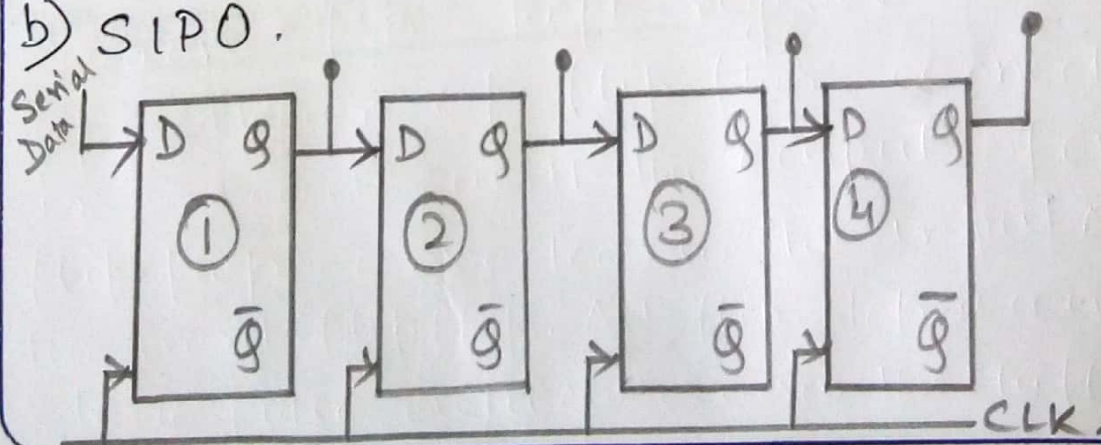
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PIN CONFIGURATION:-CIRCUIT DIAGRAM:-

a) SISO



b) SIPO.



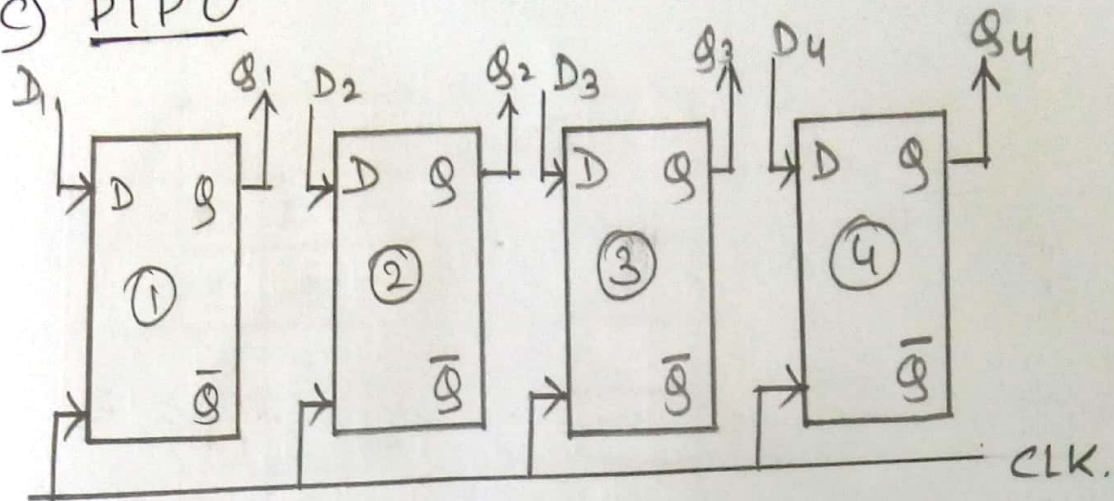
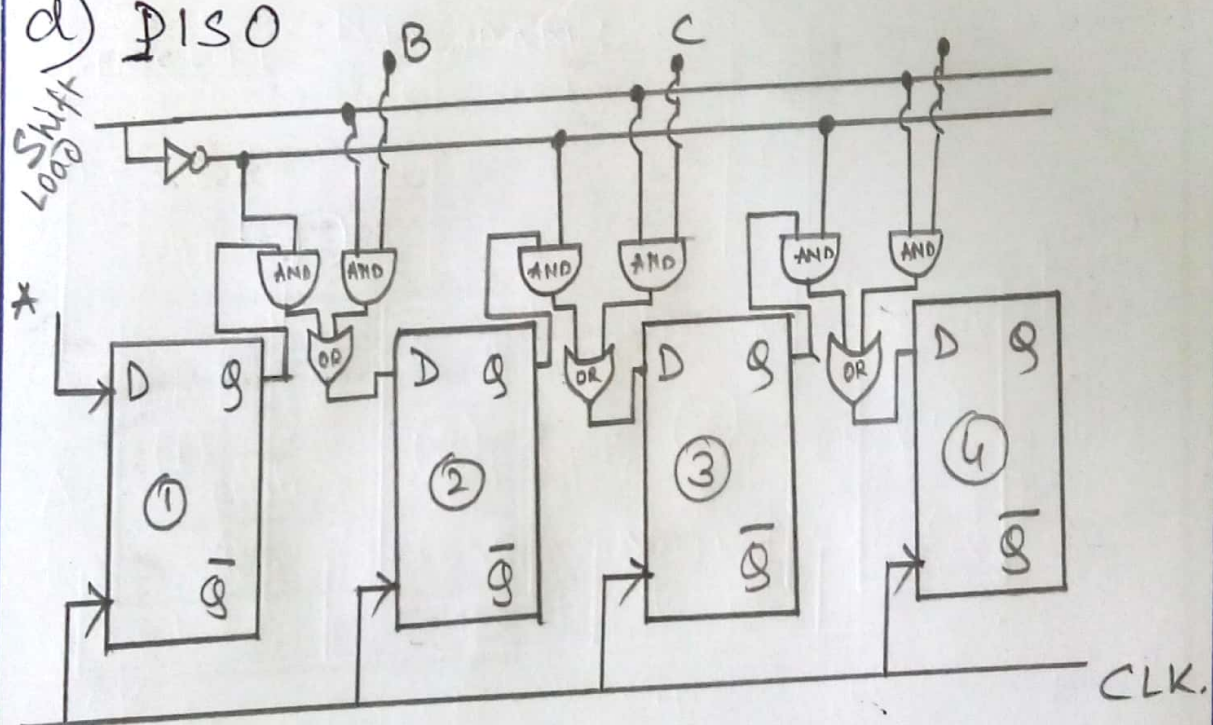
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c) PIPOd) DISOOBSERVATION TABLE:-a) SISO.

D.T.O.

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a) SISO.

CLK	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Output
Initial Value	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	0	1	1	0	0
4	1	0	1	1	1

b) SIPO.

CLK	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

c) PIPO.

CLK	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>output</sub>
Initial state	0	0	0	0	
1	1	1	0	0	0
2	1	1	1	0	0
3	1	1	1	1	0
4	1	1	1	1	1

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d) DISO.

clk	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Output
1	1	1	1	1	1
2	0	1	1	1	1
3	0	0	1	1	1
4	0	0	0	1	1
5	0	0	0	0	1
6	0	0	0	0	0

CONCLUSION:-

With the help of this experiment, we came to know about different shift register, and how they are made using 4013 IC and its difference within them.

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