Experiment - 15

Title :-

Realization of a circuit for parity generator and parity checker.

Objective :-

To design a circuit for odd and even parity generator and also odd and even parity checker.

Apparatus Table :-

Sl. No.	Component Name	Specification	Quantity
1	XOR gate	IC 4070	1
2	NOT gate	IC 4069	1
3	Trainer Kit	-	1
4	Connecting Wires	-	1 bunch

Theory :-

Parity Bit :-

The parity generating technique is one of the most widely used error detection techniques for the data transmission. In digital system, when binary data is transmitted and processed, data may be subjected to noise so that such noise can alter 0s (of data bits) to 1s and 1s to 0s

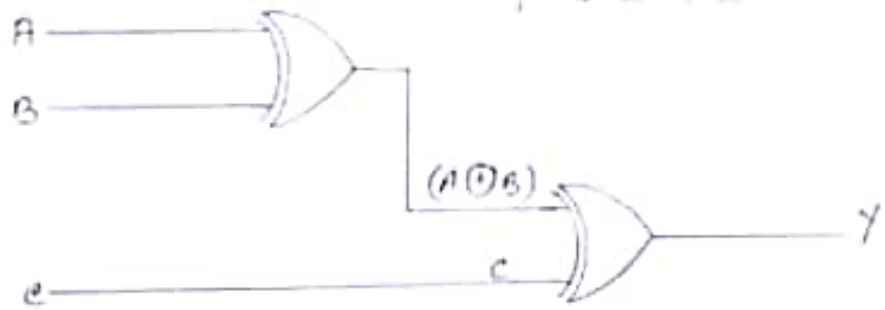
Parity generator and checker :-

A parity generator is combinational logic that generates the parity bit in the transmitter. On the other hand, a circuit that checks the parity in the receiver is called parity checker. A combined circuit or devices of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data word.

The sum of the data bits and parity bits can be even or odd. In even parity, the added parity bit will make the total number of 1s odd amount.

The basic principle involved in the implementation of parity circuit is that sum of odd number of 1s is always 1 and sum of even number of 1s is always zero. Such error detecting and correcting can be implemented by using XOR gates.

$Y = (A \oplus B) \oplus C$



Three bits

Parity Generator:-

It is combinational circuit that accepts an n-1 bit stream data and generates the additional bit that is to be transmitted with the bit stream. This additional or extra bit is termed as a parity bit.

In even parity bit scheme, the parity bit is '0' if there are even number of 1s in the data stream and the parity bit is '1' if there are odd number of 1s in the data stream.

In odd parity bit scheme, the parity bits is '1' if there are even number of 1s in the data stream and the parity bit is '0' if there are odd number of 1's in the data stream.

Parity Checker :—

It is a logic circuit that checks for possible errors in the transmission. This circuit can be an even parity checker or odd parity checker depending on the type of parity generated at the transmission end when this circuit is used an even parity checker the number of input bits must always be even.

When a parity error occurs, the 'sum even' output goes low and 'sum odd' output goes high. If this logic circuit is used as an odd parity checker, the number of input bits should be odd, but if an error occurs the 'sum odd' output goes low and 'sum even' output goes high.

Even Parity Generator :—

Theory :—

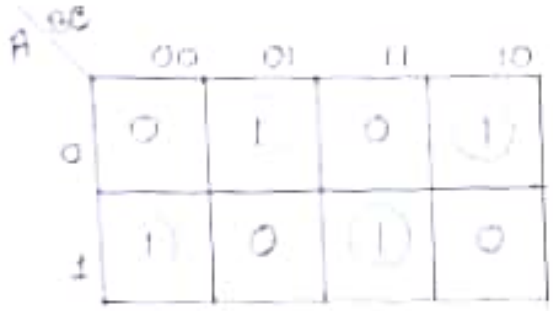
Let us assume that a 3-bit message is to be transmitted with an even parity bit. At the three inputs A, B, C are applied to the circuits and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P.

The truth table of even parity generator in which 1 is placed as parity bit in order to make all 1s as even when the number of 1s in the truth table is odd.

Truth Table :—

3-bit message			Even parity bit generator (P)
A	B	C	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

K-map :-



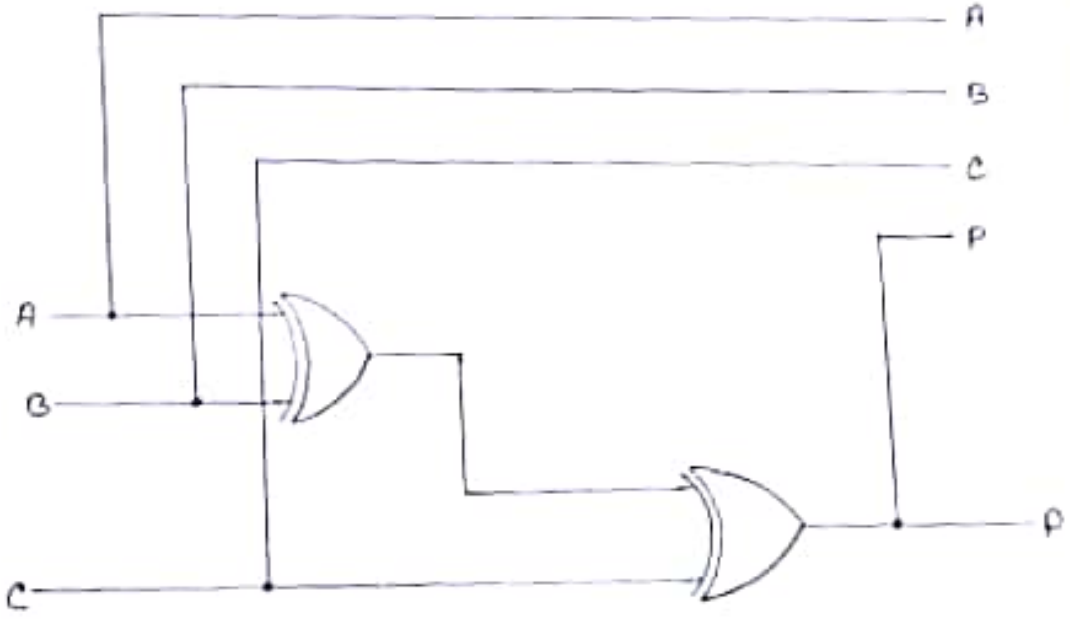
$$P = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$

$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$

$$= A \oplus B \oplus C$$

Circuit Diagram :-



$$P = A \oplus B \oplus C$$

Observation Table :-

3-bit message			Even parity bit generator (P)
A	B	C	P
0	0	0	0
0	0	1	1
1	1	0	0
1	1	1	1

Odd Parity Generator :-

Theory :-

Let us consider that the 3-bit data is to be transmitted with an odd parity bit. The three inputs are A, B and C and P is the output parity bit. The total number of bits must be odd in order to generate the odd parity bit.

In the truth table, 1 is placed in the parity bit in order to make the total number of bits of odd when the total number of 1s in the truth table is even.

Truth Table :-

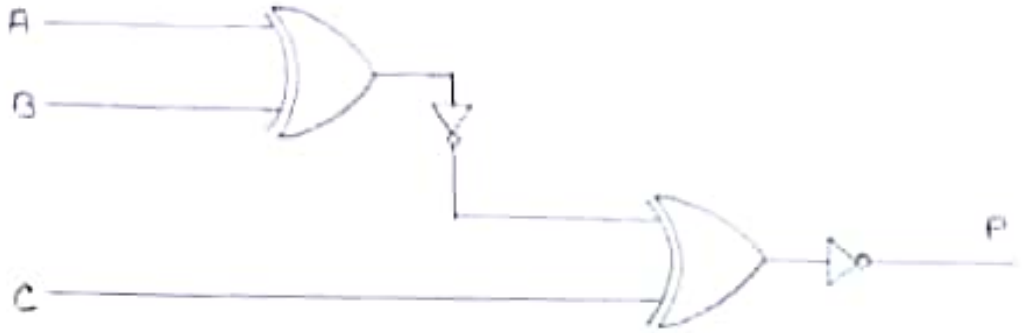
3-bit message			Odd parity bit generator (P)
A	B	C	P
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

K-map :-

A \ BC	00	01	11	10
0	(1)	0	(1)	0
1	0	(1)	0	(1)

$$P = \overline{((\overline{A \oplus B}) \oplus C)}$$

Circuit Diagram :-



$$P = \overline{(\overline{(A \oplus B)} \oplus C)}$$

Observation Table :-

3-bit message			Odd parity bit generator (P)
A	B	C	P
0	0	0	1
0	1	0	0
0	0	1	0
1	0	0	0
1	1	1	0

Even Parity Checker :-

Consider that three input message along with even parity bit is generated at the transmi-
-tting end. These four bits are applied as input to the parity checker circuit which checks the possibili-
-ty of error on the data. Since the data is transmitted with even parity, four bits received at circuit must have an even number of 1s.

If any error occurs, the received message consists of odd number of 1s. The output of the parity checker is denoted by PEC (parity error check).

The below truth table for the even parity checker in which PEC = 1 if the error occurs, i.e., the four bits received have odd number of 1s and PEC = 0 if no error occurs, i.e., if the 4-bit message has even number of 1s.

Truth Table :-

4bit received message				Parity error checker (C_p)
A	B	C	P	C_p
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

K-map :-

AB \ CP	00	01	11	10
00	0	(1)	0	(1)
01	(1)	0	(1)	0
11	0	(1)	0	(1)
10	(1)	0	(1)	0

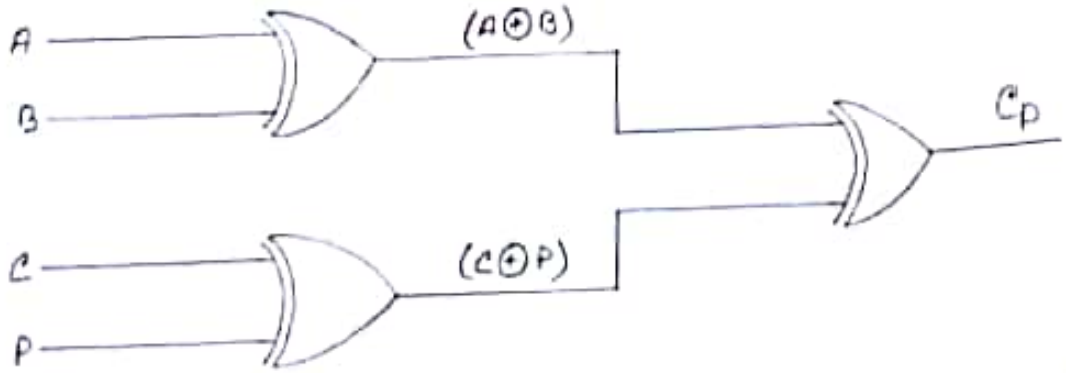
$$PEC = \bar{A}\bar{B}(\bar{C}P + C\bar{P}) + \bar{A}B(\bar{C}\bar{P} + CP) + A\bar{B}(\bar{C}P + C\bar{P}) + AB(\bar{C}\bar{P} + CP)$$

$$= \bar{A}\bar{B}(C \oplus P) + \bar{A}B(\overline{C \oplus P}) + A\bar{B}(C \oplus P) + AB(\overline{C \oplus P})$$

$$= (\bar{A}\bar{B} + AB)(C \oplus P) + (\bar{A}B + A\bar{B})(\overline{C \oplus P})$$

$$= (A \oplus B) \oplus (C \oplus P)$$

Logic Diagram :-



$C_p = (A \oplus B) \oplus (C \oplus P)$

Observation Table :-

4bit received message				Parity error checker
A	B	C	P	C_p
0	0	0	0	0
0	0	0	1	1
0	0	1	1	0
0	1	1	1	1
1	0	0	0	1
1	1	0	0	0
1	1	1	0	1
1	1	1	1	0

P.T.O.

Odd Parity Checker :-

Conside that a three bit message along with odd parity bit is transmitted at the transmitting end. Odd parity checker circuit receives these 4bits and checks whether any error are present in the data.

If the total number of 1s in the data is odd, then it indicates no error, where as if total number of 1s is even then it indicates the error since the data is transmitted with odd parity at transmitting end.

In the truth table for odd parity checker where PEC = 1 if the 4 bit message received consists of even number of 1s (hence the error occurred) and PEC = 0 if the message contains odd number of 1s (that means no error)

Truth Table :-

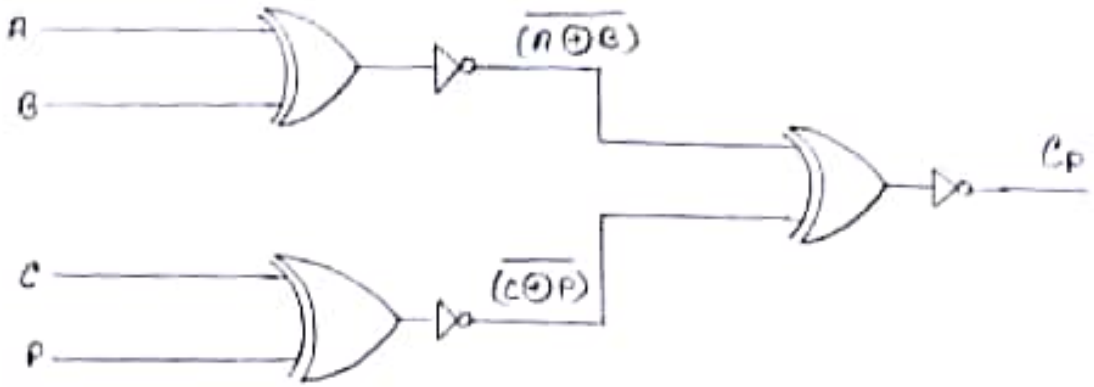
4bit received message				Parity error checker (C_P)
A	B	C	P	C_P
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

K-map :-

AB \ CP	00	01	11	10
00	1	0	1	0
01	0	1	0	1
11	1	0	1	0
10	0	1	0	1

PEC : $\overline{((\overline{A \oplus B}) \oplus (\overline{C \oplus P}))}$

Circuit Diagram :-



C_P : $\overline{((\overline{A \oplus B}) \oplus (\overline{C \oplus P}))}$

Observation Table:-

4 bit received message				Parity error checker (C_P)
A	B	C	P	C_P
0	0	0	0	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	1	1	1	1

Conclusion:-

Parity bit is the most common error detecting code. It is used to detect single bit error in the transmited binary information. 3-bit (odd/even) Parity generator and 4-bit (odd/even) Parity checker circuit has been designed using XOR gate and NOT gate and its truth table verified.