(1) SOLUTION SET
CS&IT UTI 2017

Q:11

Step 1: Start.

Step 2: Introduce an unified Cache in the between CPU & Memory. which can Store both data/address/opcode.

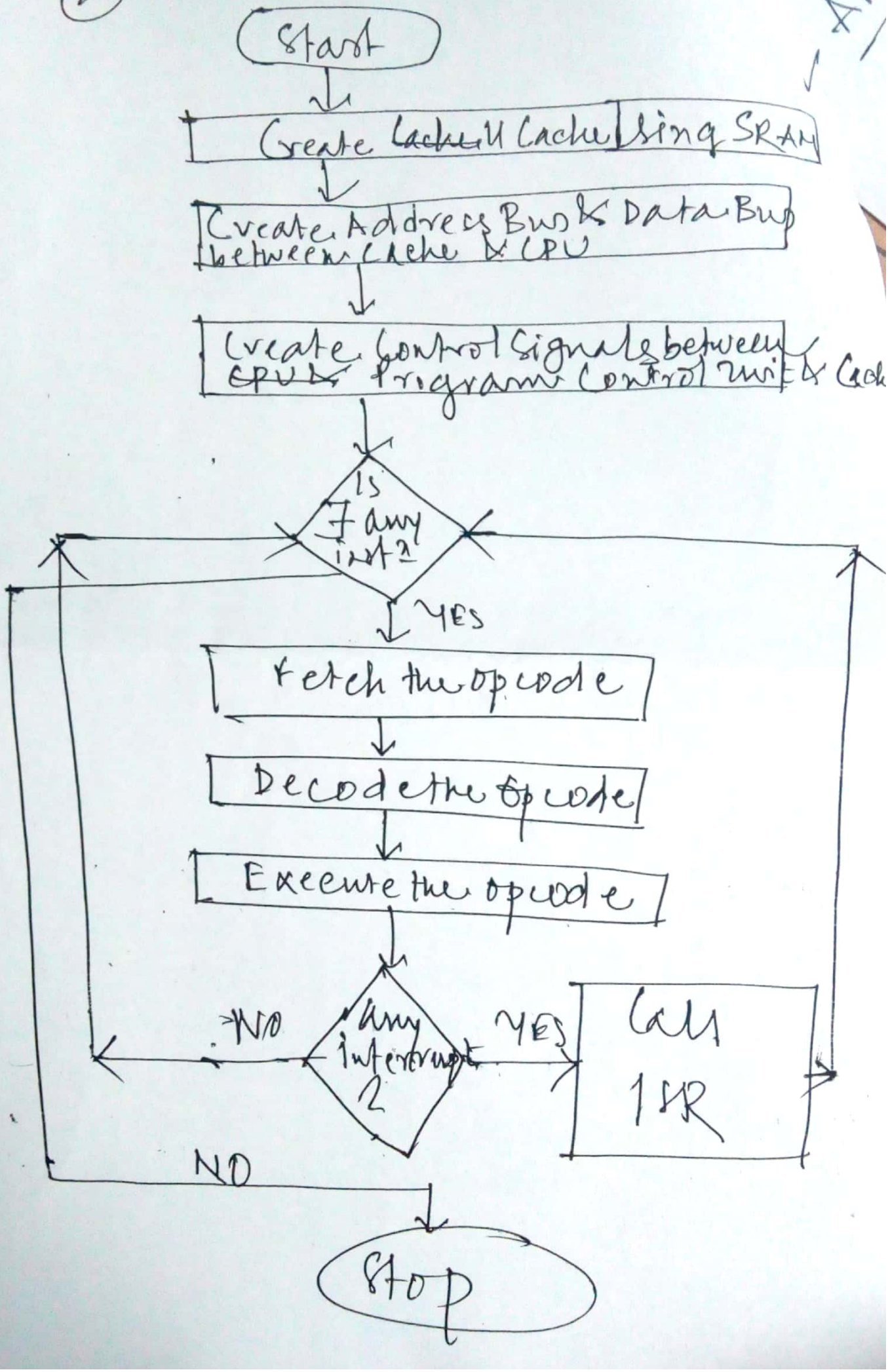
Step 3: Connect this memory with Datapath & Program Control Unit of the CPU i.e. with DR using Address bus (↑) & Data Bus (↕).

Step 4: Connect the Control Signals of Program control unit with Cache.

Step 5: Stop.

Conclusion: As the Speed of Cache is almost equivalent to CPU register hence, the kind of Speed at which CPU register is receiving the data/address from Cache & the kind of Speed at which CPU register is sending the data/address to the Cache ∃ no Speed mismatch.

(2)



Answer: Follow P. No. 1.11 from Tk Ghos
2e. Figure 1.8.

Q: 13. a) Data insufficient Give Full marks.

b) 2048 × 2048 bits

c) 3 GHz = $10^9 \times 3$ Hz 1 Hz = 1 cycle/se
= 3×10^9 cycles per second.

∴ 1 Sec. no. of counted ~~Switch~~ Switch/ cycles occurred 25

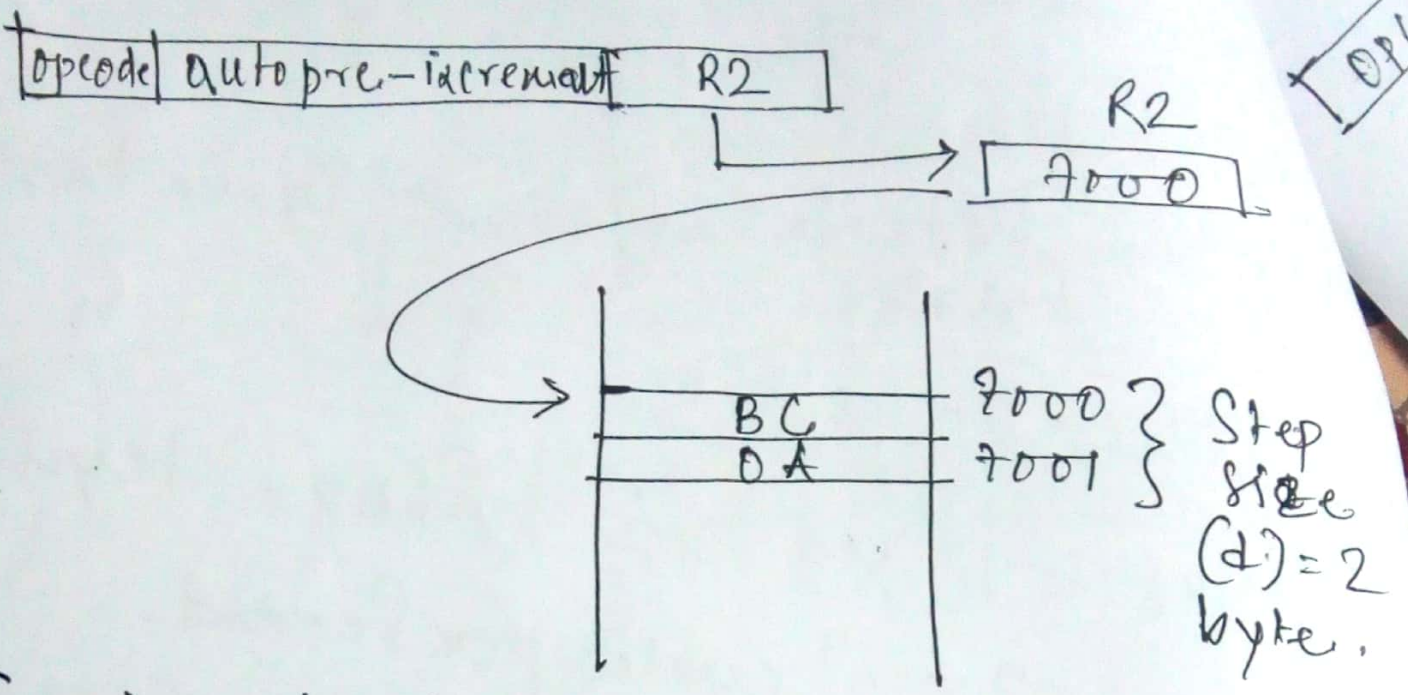
So, 25 cycles in 1 sec.
3×10^9 " " $\frac{3 \times 10^9}{25}$.

d) Speed up = $\frac{\text{Exe-time}_{\text{before}}}{\text{Exe-time after}}$

8 = $\frac{\text{~~Exe-time bef.~~} 120 \text{ ns}}{\text{Exe-time after}}$

$\text{Exe-time}_{\text{after}} = \frac{120}{8} = 15 \text{ ns}$

Q:14 (a) Given, [R2] = 7000 (4)



So, in the 1st iteration:

EA = old [R2] + d (step size)

= [7000] · 7000 + 2

= 7002 = new [R2]

2nd: EA = old [R2] + d

= 7002 + 2 = 7004 = new [R2]

3rd: EA = old [R2] + d

= 7004 + 2 = 7006 = new [R2]

Q:14 (b) Given, instⁿ ⇒ JUMP 2000

OPCODE	ADDRESSING MODE	ADDRESS
OFH	PC-Relative	2000 (B)

JUMP 2000 takes 3 bytes:
Because to Store 'JUMP Address' opcode we need 1B.
to store 2000 offset we need 2B.

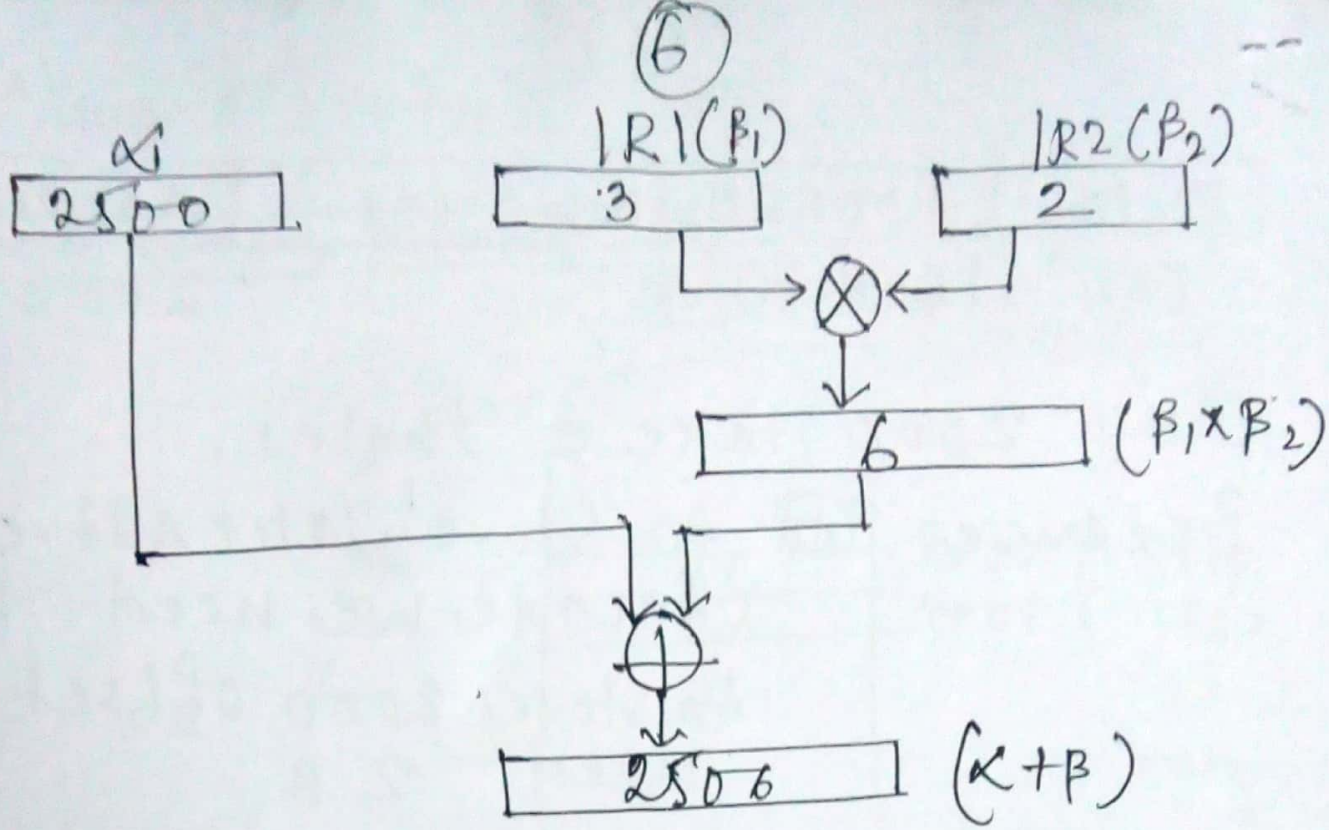
So, total no. of Bytes is 3B.
Which is Step Size ord.

Now, $\alpha = [PC] + d$.
$= 7050 + 3$ As $[PC] = 7050$
$= 7053$

∴ The address from which next inst^{n} Jump is
$= 7053 + 2000$
$= 9053 = EA$

Q:14 (c) Inst^{n} Format: LDA 2500

OPCODE	ADDRESSING MODE	2500
32	INDEX REGISTER	α



(α+β) ≡ the address of A[3]

@Orunayan @ (1) C, VP).