EXPERIMENT NUMBER-32:-

TITLE:- Implementation of 3-bit synchronous down counter using D-Flip Flop.

OBJECTIVE:- Implimenting a 3-bit synchronous down counter using D-Flip Flop.

APPARATUS REQUIRED:-

Sl. No.	Component's Name	Specification	QTY.
1	D-flipflop	4013	2
2	Trainer Kit	–	1
3	Wires	–	1

THEORY:-

In a synchronous down counter, the flip-flop in the lowest order position is complemented with every pulse. A flip-flop in any other position is complemented with a pulse position provided all the lower-order bits equal to 0.

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TRUTH TABLE:-

Present state			Next step			Output		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	D_3	D_2	D_1
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	0
0	1	1	0	0	1	0	0	1
0	1	1	0	1	0	0	1	0
1	0	0	0	1	1	0	1	1
1	0	1	1	0	0	1	0	0
1	1	0	1	0	1	1	0	1
1	1	1	1	1	0	1	1	0

K-Map:-

a) For D_1,

Q_3 \ Q_2Q_1	00	01	11	10
0	1	0	0	1
1	1	0	0	1

So, $D_1 = \overline{Q_1}$

b) For D_2,

Q_3 \ Q_2Q_1	00	01	11	10
0	1	0	1	0
1	1	0	1	0

So, $D_2 = \overline{Q_2}\,\overline{Q_1} + Q_2 Q_1 = (Q_2 \oplus Q_1)'$

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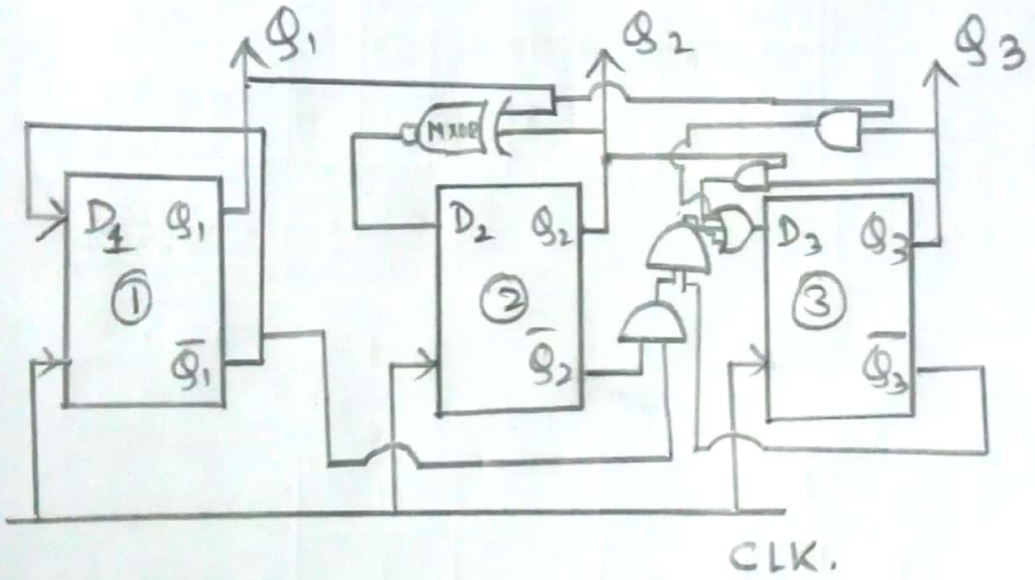
For D_3 ;

Q_3 \ Q_2Q_1	00	01	11	10
0	1	0	0	0
1	0	1	1	1

So, $D_3 = \bar{Q}_3\bar{Q}_2\bar{Q}_1 + Q_1Q_3 + Q_2Q_3$

CIRCUIT DIAGRAM :-



OBSERVATION TABLE :-

Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	D_3	D_2	D_1
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	0
1	1	0	1	0	1	1	0	1
1	1	1	1	1	0	1	1	0

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CONCLUSION:-

With the help of this experiment, we came to know about, the synchronous down do-counter and its works. We verified with the truth table of it after making the circuit with D-Flip-Flop.

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