2nd mid sem

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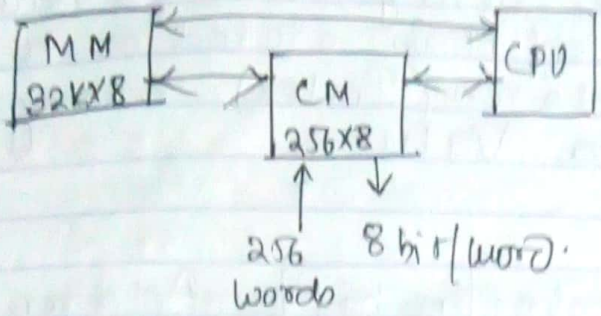
VP

Page
Date 9/10/19.

## Cache Memory :- (Cache Mapping).

1k = 1024.




Main Memory sends duplicate copy in cache.

Cache Mapping →

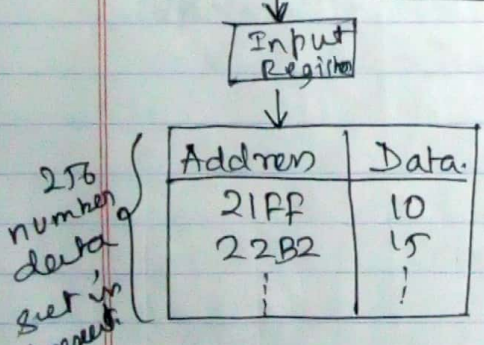
Procedure of Mapping.

→ Associative mapping
→ Direct " } Search is on cache.
→ Set-Associative "

### Associative Mapping

Fastest and flexible type of mapping

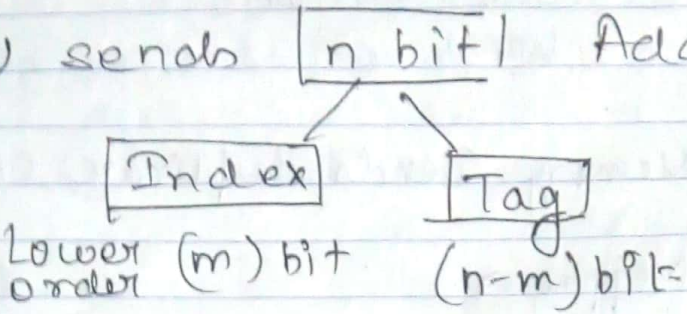
CPU Sends → n bit Address




→ If found, i.e., address it will send the data otherwise it will go to main memory.

## Direct Mapping

- Instead of storing total CPU Address one part of it is stored as the cache address (Index) along with the Data Value.




CPU uses m-bit (Index) to Search Cache Memory – Storage capacity of cache $2^m$ and total capacity of main memory is $2^n$, where $n > m$ (always).

Suppose, in n → 00FF.

Then, Index → FF } → part is stored with
Tag → 00 } → works like flag

Under 1 Index ~~number~~ numerous tag values. E.g.

| Tag | Index |
|---|---|
| 00 | 00 |
| 00 | 01 |
| ⋮ | |
| 00 | FF |

↳ Index.

| Index | Tag. | Data. |
|---|---|---|
| Index \| Tag (n-bit.) | | |

Index Match + Tag Match → Cache hit.

Since, Index is > Then Tag, so cache bit decreased. So, Block number is increased.

Block no:

| Tag | Block | word. |
|---|---|---|

Suppose, 256 spaced = $2^8$, = 8 bit.

then, 8 block number will be produced.

K-Way (set Associative Mapping).
(Tag-Data pair).
→ Improved version of direct Mapping

Under If K-Way mapping, then
K Tag-Data pair will be present.

Suppose 2-Way., the 2 Tag-Data pair

| Index | Tag Data | Tag Data. |
|---|---|---|
| 00 | 01 52 | 02 17 |
| 01 | 21 | 22 |

Index → then Tag Data is matched, then its a cache hit.

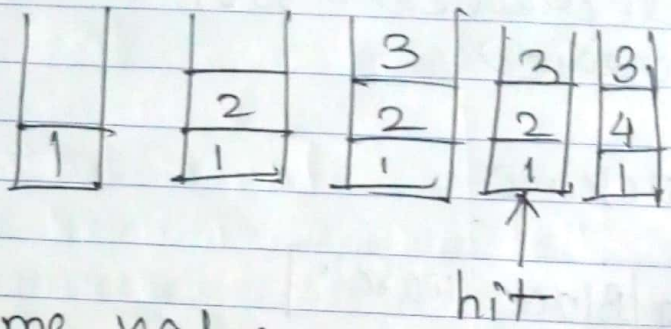
## ⑧ Replacement Policy (Cache Replacem

→ FIFO. (First In First Out).
→ LRU (Least Recently Used)

Reference String or Data Reference Stream
↳ Mention in question, then cache replace

1 2 3 1 4 5 2 1

FIFO →




If same value comes hit, is counted
% hit ratio = No. of hits. / Total no. of reference

LRU → Counts hit, where the least used number is replaced.

@Srinayan@

Page: Date: 16/10/17

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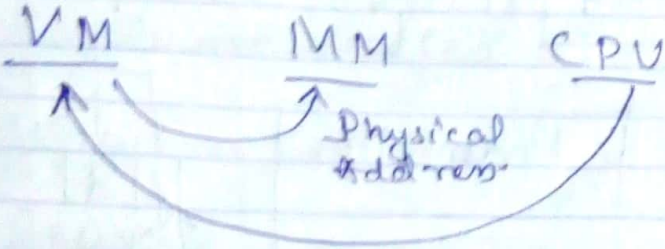
Virtual Memory (Eg. Size is Secondary Memory).

↳ Virtual Slot which can give same amount of memory, & it becomes cost effective.




Virtual / Logical Address. → Address generated by processor, ∴ to bring concept of VM.

→ Logical Address Space (Address produced without interruption).
→ Physical Address Space. (To store the data).

Logical to Physical Address Mapping :—

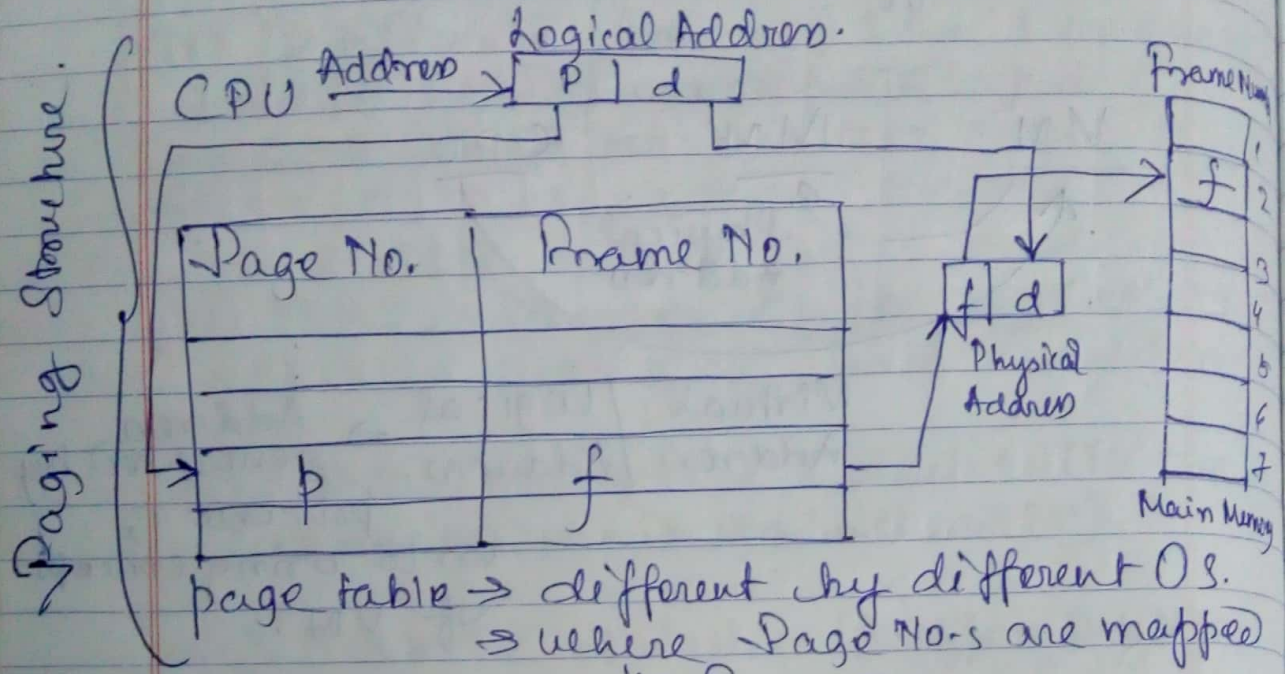
page – Paging (A Non-contiguous process, finding empty, & stored).
↳ A program getting divided in pages, stored in VM.
Frame → to bring page at physical memory is for the.

Size of 1 page = Size of 1 frame.

No of page (≠ (Not always but maximum)) No. of frame.

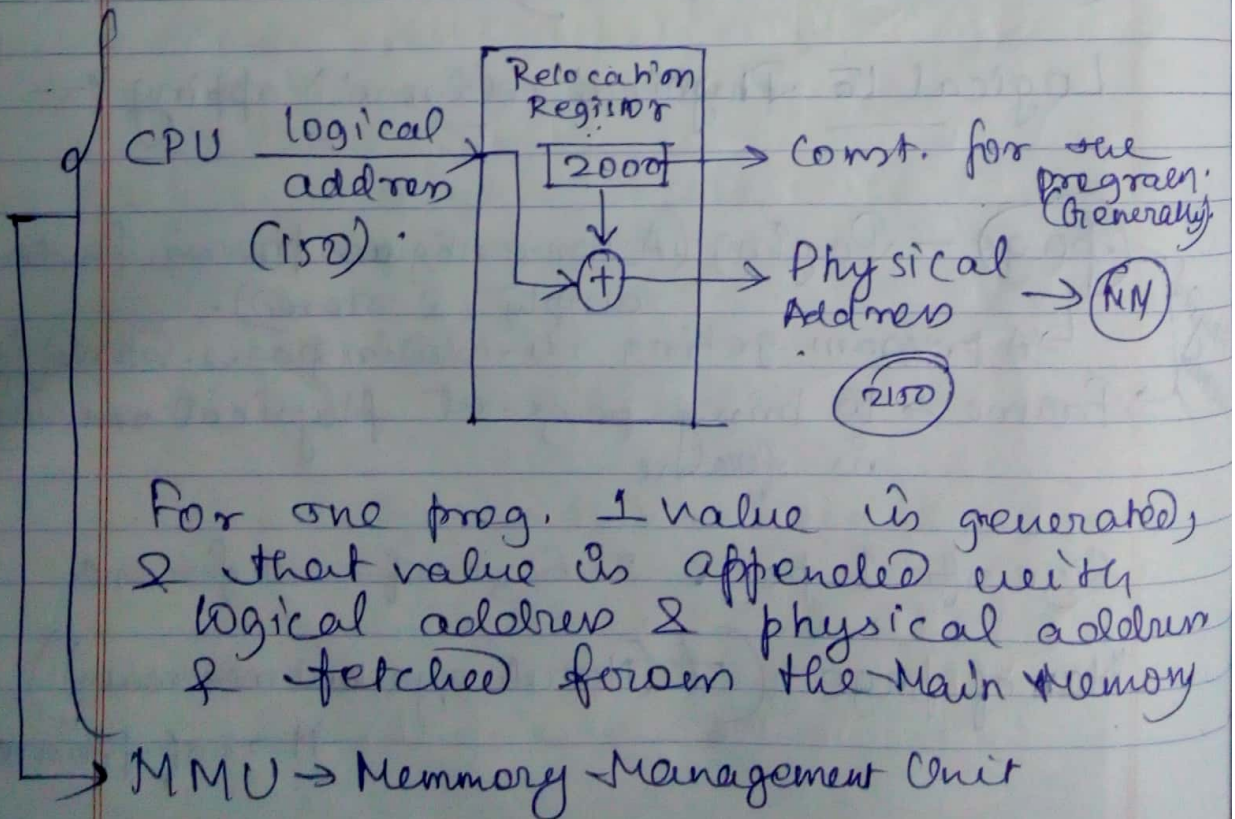
Page Number + data (offset) = Logical address / Location.

Frame Number + data (offset) = Physical address.




page table → different by different OS.
⇒ where Page No.s are mapped with Frame Nos.

## Relocation Register / Base Register




For one prog. 1 value is generated, & that value is appended with logical address & physical address & fetched from the Main Memory

Advantages:- (Paging)

1. It supports time sharing system.
2. As it is a non-contiguous process hence memory is utilized efficiently.

Disadvantage → (Paging)

1. Page Break —

Ulantage of size is called page breake.

16 KB page size = 4 KB.

Req. ~~page size = 4 KB.~~ 4.

But, if 18 KB & page size 4 KB

Req. page = 5, 5 × 4 = 20 KB

so, 2 KB unused.

(Page Break).

1 program → Only one page table.

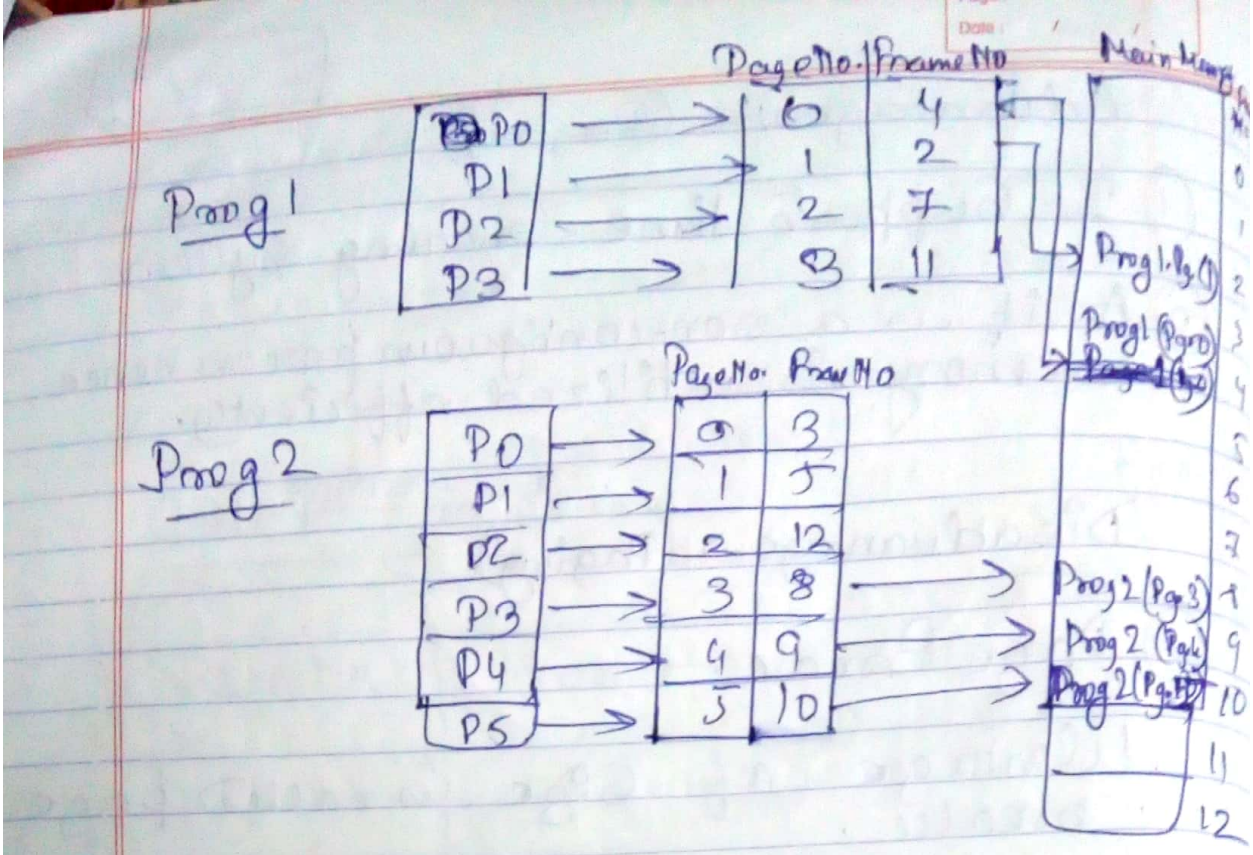
E.g. →

Prog 1 → 16 KB. } Pagesize = 4 KB.

Prog 2 → 24 KB }

→ No. of pages = $\frac{16}{4}$ = 4 page → Page 0 - Page 3

→ No. of pages = $\frac{24}{4}$ = 6 page → Page 0 - Page 5




Frame Number is Random.

## Page Fault :-

When a page is req. to execute & if execution

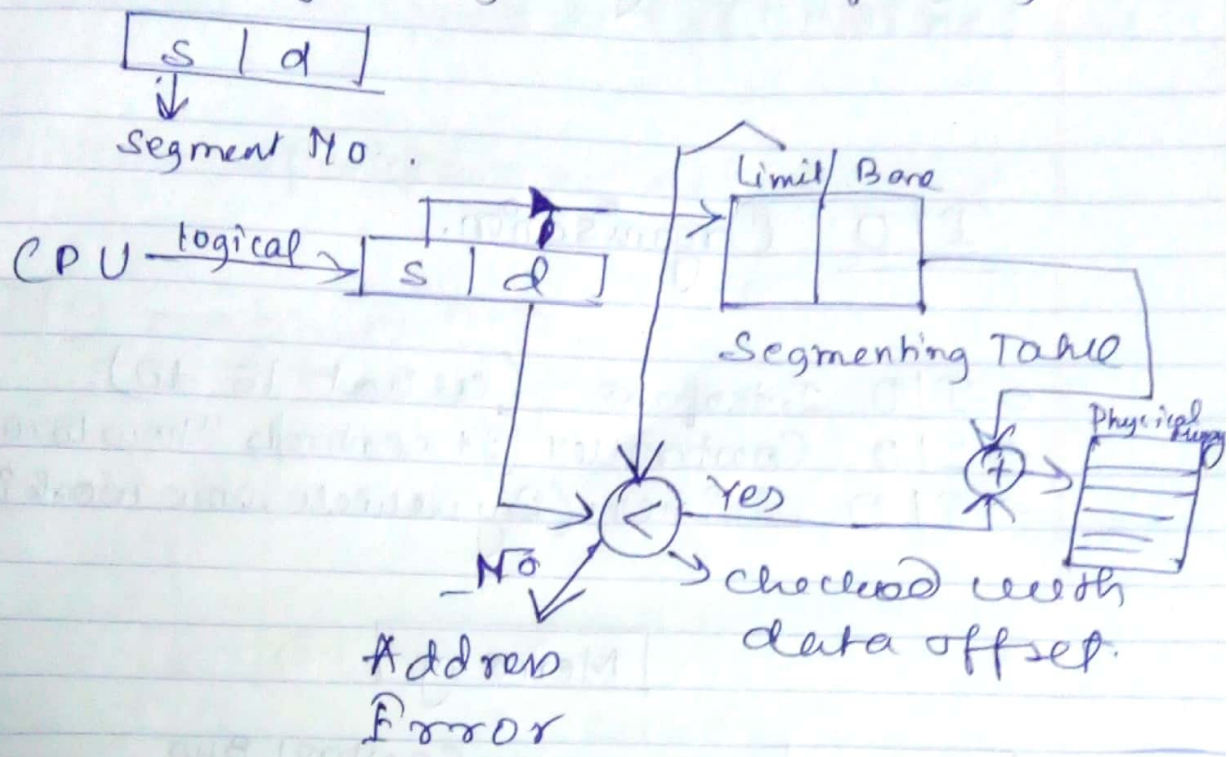
Page not found in Page execution or in main memory
↳ Page Fault.

Two types

→ FIFO
→ LRU
→ OPR (Optimal Page Replacement).
(Opp. of OPR LRU).
↳ which data will not be used in near recent future.

## Segmentation :—

Dividing prog. in no. of segments.




## Advantage

(1) Efficient utilization of physical memory as a range of storage space, assigned for each program segment other than one single page as it was in paging.

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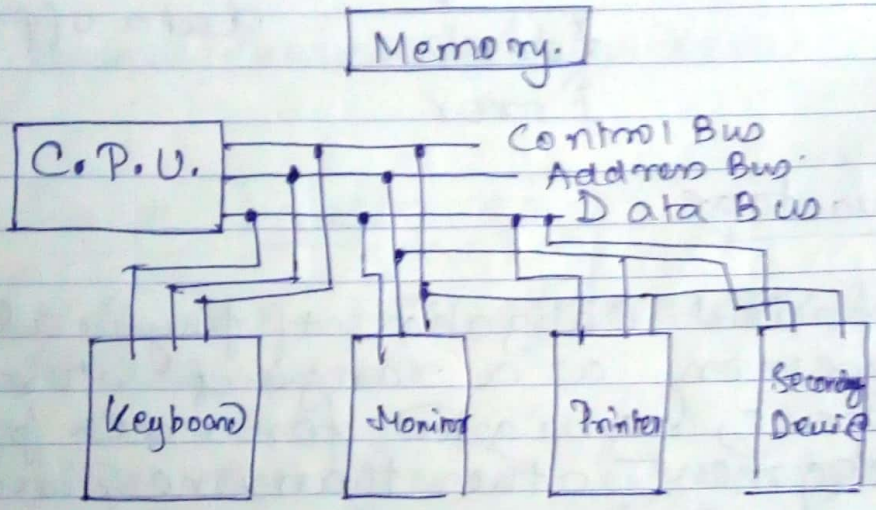
## Segmentation

Segment = segment no. + data offset.

## I/O Organisation.

→ I/O Interface (what to do).
→ I/O Controller (It controls "how to work" part)
→ I/O driver. (By which how work is done)




I/O Structure of Computer System.

4) I/O Commands

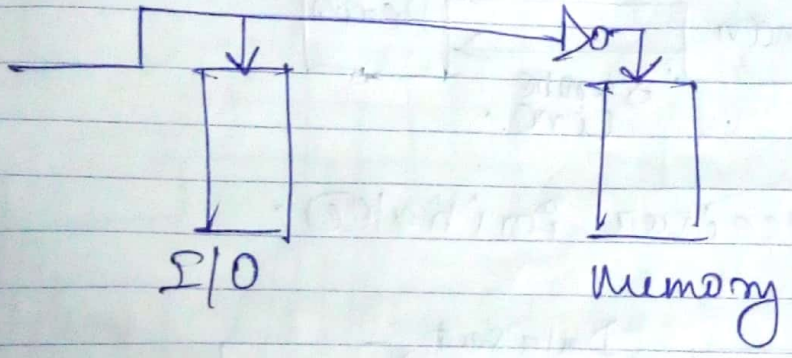
- Control (Choosing purpose)
- Test (Working condition or not)
- Read (Fetching the data)
- Write. (Overwriting).

# I/O Access

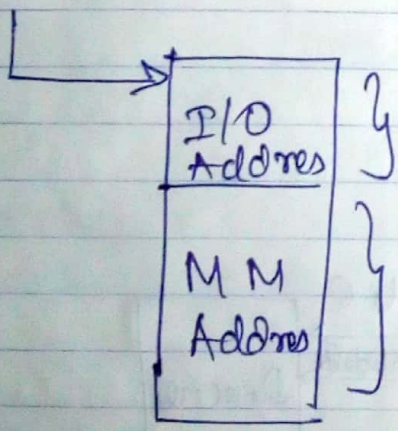
① I/O mapped I/O. (2 separate address space)
② Memory mapped I/O. (1 address space).

CPU → Specifies one Address.

## ① I/O mapped I/O




## ② Memory mapped I/O.




① I/O data transfer. wrong.

(Barier) – Synchronous → if data gets transfer, then understand (data transfer time = Time received)
– Asynchronous.

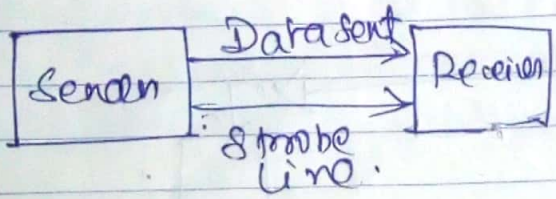
↳ Master ⇔ Slave → Relation.

Asynchronous
- → Sender initiated
- → Receiver initiated (Receiver asking for data)

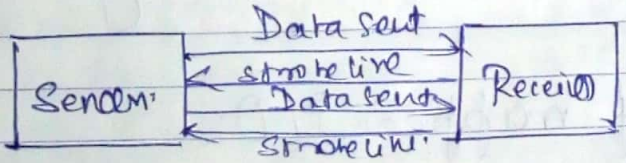
↳ strobe
↳ Handshaking.

Strobe (Activate means Receiver is busy)

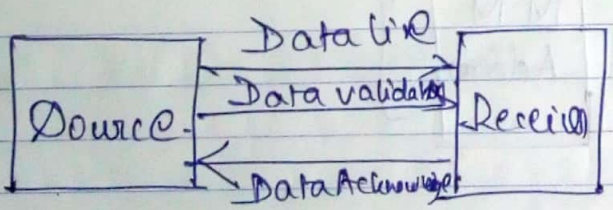
→ Sender initiated.




→ Receiver initiated.



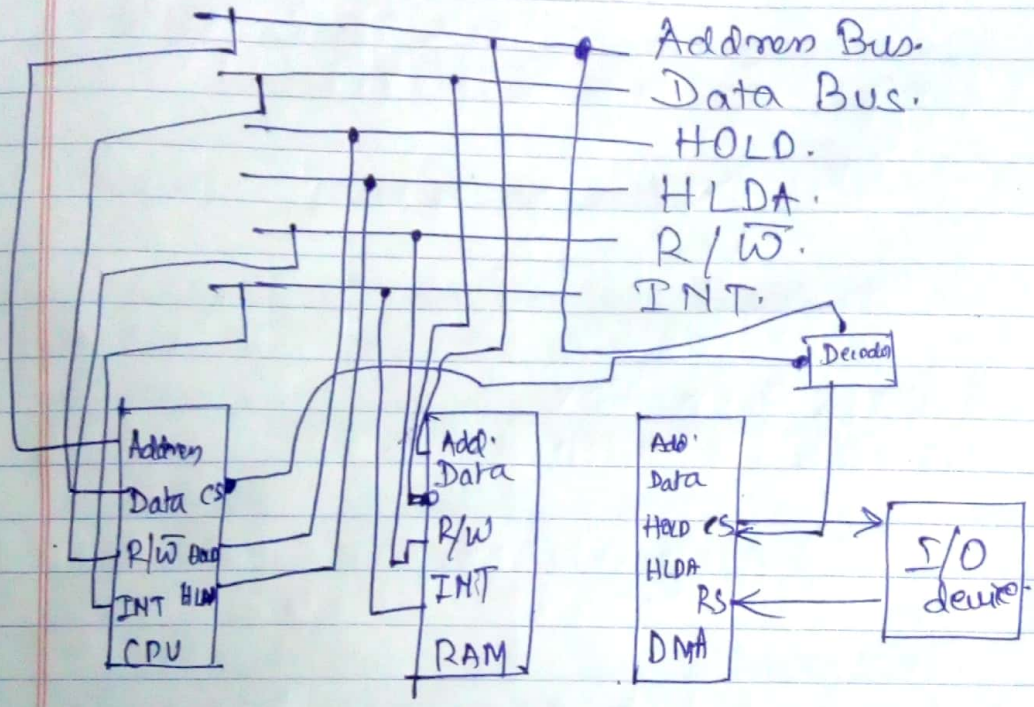

Handshaking




(*) Advantage & Disadvantage.

## Modes of data transfer

— Programmed I/O. (One work at a time).
— Interrupt – Initiated I/O.
— DMA. (Direct Memory Address.).
Ad. → Sets processor free for other works.




CS → Chip select
RS → Register select

## Two types of data transfer in DMA:

→ Cycle Stealing
As DMA is present, CPU transfers work to the DMA.

→ Block Burst transfer.
→ To use all the block in one accon.

→ Bus Arbitration

→ ~~I cont~~ How to select next bus that I want to use.

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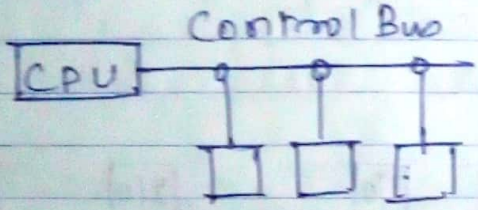
## DMA Transfer :—

→ By bypassing CPU

- Cycle Stealing → Processor is bypassed for some cycle.
- Block Burst
  → When file transfer is done by DMA, it gets uninterrupted.

One I/O → One will be worked.
One by One the work is done.

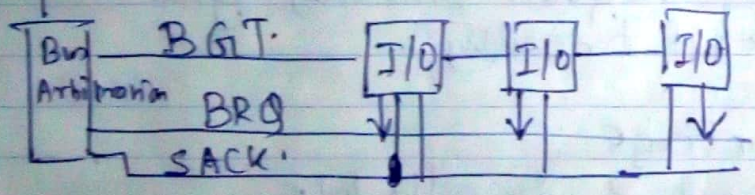
## BUS ARBITRATION :— (Only concentration Control Bus)




The process by which the I/O transfer is given to which Bus, is selected.

Types—
- CENTRALIZED
- DISTRIBUTED.

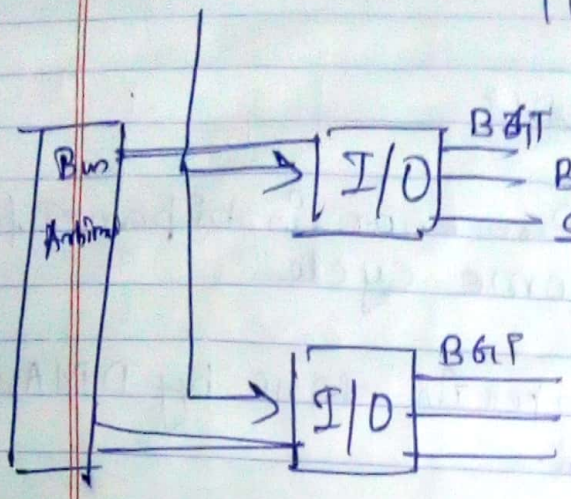
Centralized




- BGT → Bus Grant Transmission. Line.
- BRQ → Bus Request Line
- SACK → Site Acknowledgement.

→ Depends on Choosing the I/O.

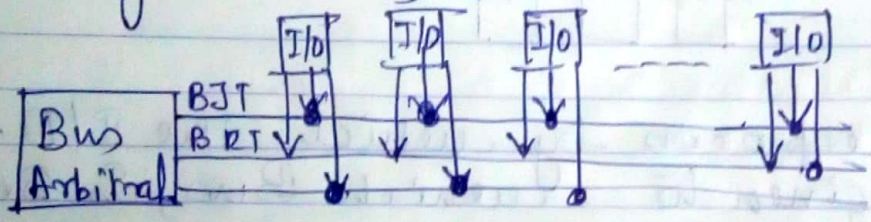
- Distributed → For each I/O, three lines are connected.




Application

1. → Daisy Chaining (Centralised)
2. → Polling (Centralised) → Rotating Priority
3. → Independent Priority Bus Control Method (Distributive) / Fixed Priority.

① Daisy Chaining.



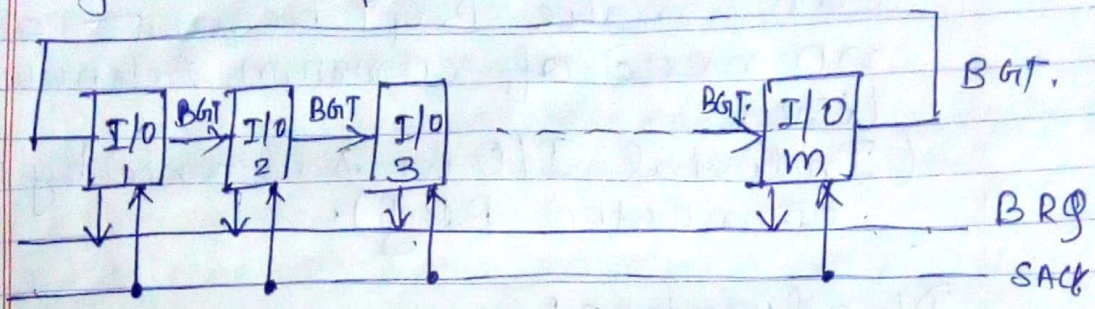

Based on the distance of I/O from Bus Arbitral the priority is taken or made.

Disadvantage
→ Only higher priority gets the chance.
→ Fixed priority.

Advantage
→ Easy & Scalable.

② Polling (NO Bus Arbitral).

Algorithm is fee in the Bus lines.




Advantage:-

① Rotating the priority.
② All the I/O devices gets equal priority for requesting & getting the grant.

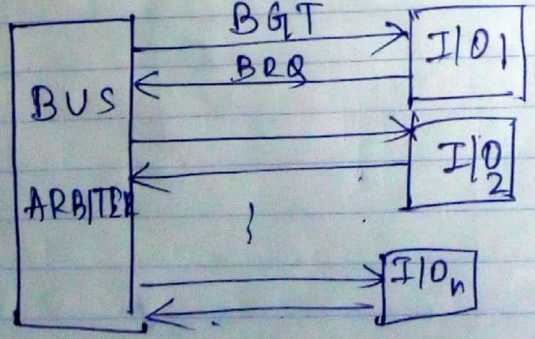
E.g.→ If BGT is at I/O → 2,
I/O 3 has priority 1 and
I/O 1 has priority m (or last priority).

Then if I/O 3 & I/O 1 makes the request for next BGT I/O 3 will be granted but not I/O 1.

Disadvantage:-

① Priority depends on BGT line hence circuit becomes Complicated

③ Independent Priority




1. If Two request are there simultaneously only the priority one will be selected.

Advantage:-

→ As centralised, all I/O device can make BGT request and no need of common Acknowledge line.
(Indivial I/O is Addressed by the connected BRQ).

Disadvantage:-

→ If the centralised Bus Arbitrar break down then the I/O devices cannot communicate for the Bus Request.

→ As individual BGT and BRQ line is connected more hardware is required.

→ NOTES AFTER MID SEM-1

→ IF U DON'T HAVE NOTES BEFR MID-SEM1, JUST PING ME.