16-bit Signed Pipelined Radix-4 Booth Multiplier with Sleep Mode

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***Abstract*—This report presents the design and implementation of a 16-bit signed pipelined radix-4 Booth multiplier with sleep mode, optimized for energy efficiency, high-speed operation, and low area usage. The multiplier employs a Wallace tree structure for partial product reduction and a configurable design supporting both signed and unsigned operations. Static power consumption is reduced through an integrated sleep mode during idle states. The design meets strict specifications for input/output capacitance and timing while utilizing pipelining to achieve high throughput. Detailed simulations and performance analyses demonstrate compliance with design constraints and optimized metrics, including power, area, and frequency.**

***Index Terms*—Radix-4 Booth multiplier, Wallace tree, pipelining, low power, configurable design.**

I. INTRODUCTION

Efficient multipliers are vital for computational systems, particularly in DSP and embedded applications. This project implements a 16-bit signed pipelined radix-4 Booth multiplier that integrates sleep mode to minimize power consumption during idle states. The design features a Wallace tree for rapid partial product reduction and supports configurable input modes for signed and unsigned operations.

II. BASIC BUILDING BLOCKS

This section describes the key components and their corresponding layouts in the 16-bit signed pipelined radix-4 Booth multiplier design. The components are organized into two levels based on their hierarchical integration into the multiplier.

A. Level 1 Layout

Level 1 includes the fundamental building blocks used in the design. These components are critical for implementing the radix-4 Booth encoding, partial product generation, and addition stages. Each component is optimized for area, power, and performance.

- **Inverter:** Basic digital inverter for signal inversion with minimal area and low delay.
- **Buffer:** Buffers designed for driving signals over long interconnects.
- **MUX 2:1:** 2:1 multiplexer for selecting inputs during Booth encoding and control signal generation.
- **Booth Encoder:** Encodes input bits into radix-4 representations to reduce the number of partial products.
- **Booth Selector:** Selects partial products based on the Booth encoded values.
- **Carry Save Adder:** Performs addition of multiple operands in the Wallace tree.
- **Propagation Generation Block:** Generates propagate and generate signals for carry computations in the addition stage.
- **Full Adder:** Core arithmetic unit for single-bit addition.

B. Level 2 Layout

Level 2 integrates multiple Level 1 components into higher-order modules for efficient operation.

- **17-bit Decoder:** Decodes control signals for managing radix-4 Booth operations.
- **Full Encoder:** Generates partial product bits for input operands.
- **4-Bit Carry Skip:** Implements a 4-bit carry skip adder for fast addition.
- **32-Bit Carry Skip:** Extends the carry skip mechanism to 32 bits for higher precision additions.
- **FA Set (1 to 7):** Sets of full adders designed for different levels of the Wallace tree.

C. Design Considerations

- **Area Optimization:** All components are manually laid out to ensure minimal area while meeting performance requirements.
- **Metal Usage:** Up to Metal-5 is utilized for interconnect routing, ensuring proper signal integrity and power distribution.
- **Performance Trade-offs:** The components are designed to achieve an optimal balance of speed, power, and area.

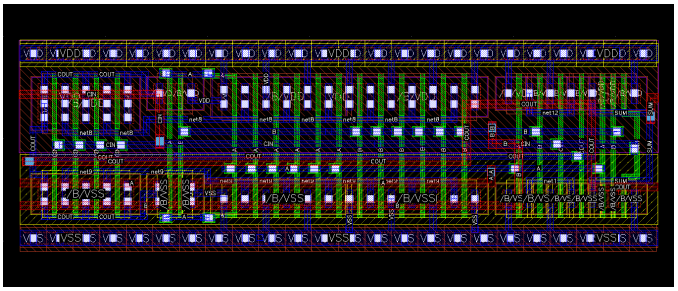

Fig. 1. Layout of Full Adder

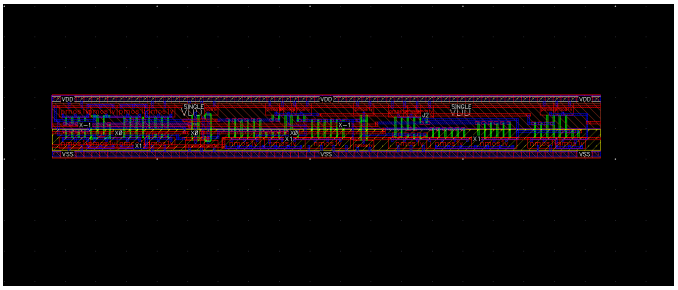

Fig. 2. Layout of Booth Encoder

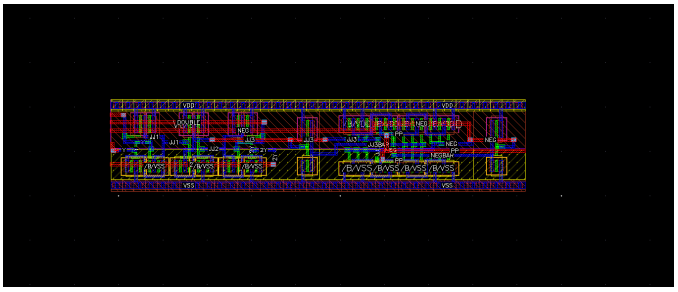

Fig. 3. Layout of Booth Selector

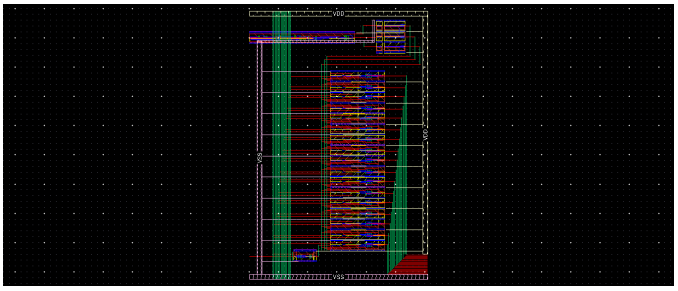

Fig. 4. Layout of 17 bit Decoder

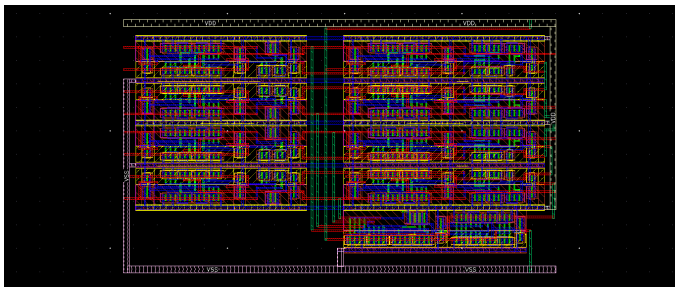

Fig. 5. Layout of 4 bit Carry Skip Adder

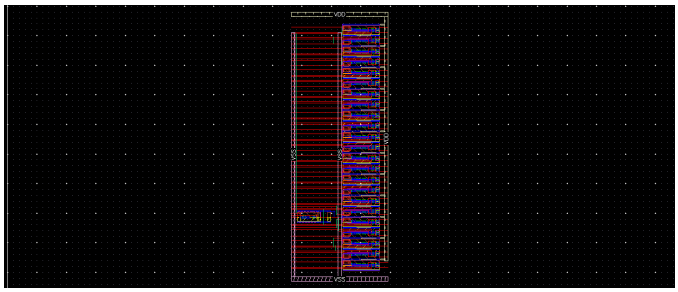

Fig. 6. Layout of Full Adder Set

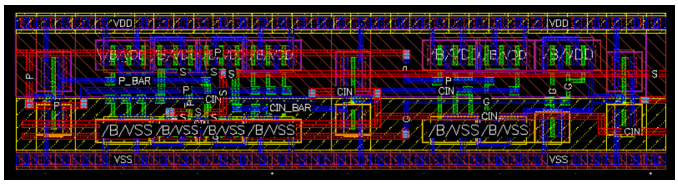

Fig. 7. Layout of Carry Sum Block

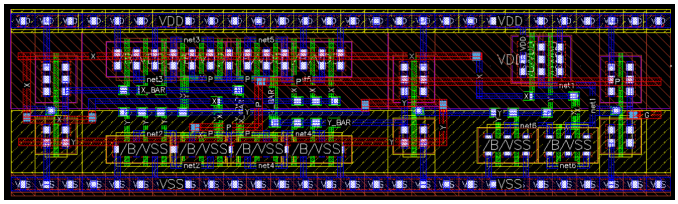

Fig. 8. Layout of Propagate Generate Block

III. ARCHITECTURE

The radix-4 Booth multiplier reduces the number of partial products by encoding input operands in groups of three bits. A Wallace tree structure further compresses partial products efficiently. The multiplier incorporates pipelining to improve throughput by enabling parallel processing across stages.

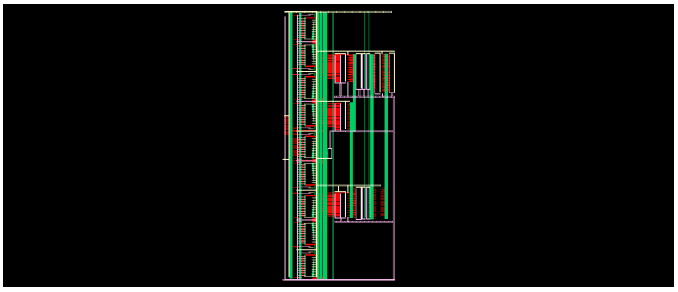

Fig. 9. Layout of Multiplier

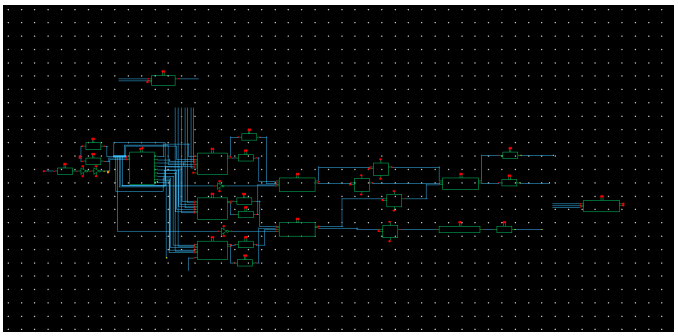

Fig. 10. Schematic of Multiplier

A. Sleep Mode

The sleep mode minimizes static power by gating unused portions of the circuit during inactivity. A sleep signal disables logic blocks, reducing leakage power.

B. Wallace Tree

The Wallace tree is employed to reduce the latency of partial product addition. It balances speed and resource usage.

C. Pipelining

Pipelining increases the throughput of the multiplier by enabling parallel processing across different stages. Each stage processes a portion of the multiplication operation, allowing new input data to be introduced while previous data is still being processed. This significantly improves the overall performance, especially for high-speed applications.

D. Signed and Unsigned Multiplication

The design supports both signed and unsigned multiplication, making it versatile for various applications. A control signal determines whether the inputs are treated as signed or unsigned, with appropriate handling of the sign bit during Booth encoding and partial product addition.

E. Signal Quality Enhancement with Buffers

Buffers are strategically placed throughout the design to improve signal quality and drive strength. This ensures that signals propagate correctly across long interconnects, minimizing delays and ensuring reliable operation, even at high frequencies.

F. Input Capacitance Matching

To ensure compatibility with the driving circuits, the input capacitance of critical inputs (A, B, CLK, SLEEP, and SIGNED) is matched to a reference inverter with dimensions $W_{NMOS} = 260\,\text{nm}$ and $W_{PMOS} = 390\,\text{nm}$. This design choice minimizes signal distortion for further stages.

IV. TESTING AND CHARACTERIZATION

The multiplier was tested for functional correctness, timing compliance, and power efficiency. Detailed analysis was conducted to evaluate power consumption, energy efficiency, performance, and area.

A. Power (Sleep Mode and Active Mode)

Power analysis was conducted for both active and sleep modes to evaluate the efficiency of the sleep mode feature:

- **Active Mode:** During active operation, the dynamic power consumption was measured across different input activity levels. The measured power was 1.018mW at the target frequency.
- **Sleep Mode:** In sleep mode, leakage power was minimized by gating unused portions of the circuit. The power was reduced to 1.716nW.

The power results demonstrate significant power savings in sleep mode, validating the efficacy of the design.

B. Energy per Multiplication

The energy consumed per multiplication was calculated using the formula:

$$E_{\text{operation}} = \frac{\text{Power}}{\text{Frequency}}$$

- **Active Mode:** At a frequency of 500 MHz, the energy per multiplication was computed to be:

$$E_{\text{active}} = 2.036\text{pJ}$$

- **Sleep Mode:** During idle states, the energy consumption was significantly lower due to the reduced power of 1.716nW.

C. Power (Sleep Mode and Active Mode)

Power consumption was analyzed at fast (FF), typical, and slow (SS) corners for both sleep and active modes. The results are summarized in Table I.

These results highlight the variation in power consumption across process, voltage, and temperature corners, demonstrating the robustness of the design.

TABLE I
POWER CONSUMPTION ACROSS DIFFERENT CORNERS

Corner	Voltage (V)	Temperature (°C)	Power (mW)
FF	1.1	-40	1.123
Typical	1.0	27	1.018
SS	0.9	127	0.653

TABLE II
OPERATING FREQUENCY ANALYSIS

Condition	Frequency
Without Clock Sizing (Input A, B Sized)	1.6 GHz
With Clock Sizing	0.5 MHz

D. Performance (Frequency)

The operating frequency of the multiplier was evaluated under two conditions: without clock sizing and with clock sizing. The results are summarized in Table II.

E. Area

The synthesized design's area was measured using the Nangate 45nm Open Cell Library. The total cell area of the multiplier was determined to be 90607.5 μm^2. The following factors contributed to the area: The area results indicate an efficient layout while meeting the specified constraints.

TABLE III
AREA BREAKDOWN OF KEY COMPONENTS

Component	Dimensions (μm)	Area (μm^2)
Booth Encoder	17.945 x 2.065	37.0564
Booth Selector	9.375 x 2.06	19.3125
Full Adder	6.26 x 2.065	12.9229
D Flip Flop	4.12 x 1.995	8.2194
17-bit Decoder	30.42 x 45.88	1395.6696
Multiplier (16-bit)	221.75 x 408.6	90607.0500

This efficient layout meets the specified area constraints while optimizing the performance and power trade-offs.

V. CONCLUSION

The project achieved the goals of optimizing energy efficiency, performance, and area. Key features like the Wallace tree for partial product reduction, pipelining for throughput, and configurable signed/unsigned operation enhanced the design. Sleep mode reduced static power, making it ideal for energy-constrained applications.

Testing across process corners validated its robustness, while the layout minimized area and ensured timing closure. Insights gained include:

1) **Signal degradation over wires** is a major issue and requires effective buffering.
2) **Block placement** significantly impacts area and performance.
3) **Wiring** often dominates area, energy, and delay over logic.

Future work could explore higher radix designs and better interconnect optimizations for further improvements.

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