Overview of Design

The clock is of 100MHz having a time period of 10ns.
The reset will initialize the state as A0.
The start button will tell to start the filtering.
The switch will tell which type of filter is to be done. When 0 the smoothening filter and when 1 sharpening filter.

There are 3 states A0, A1 and A2:

A0: The initial state which is used for initialization of parameters. When start will become 1 and button_pressed=0 then it the state will change to A1 when switch=0 and A2 when switch=1.

A1: The state in which smoothening filter will process. When the filtering will be done then done will become 1 and state change to A0.

A2: The state in which sharpening filter will process. When the filtering will be done then done will become 1 and state change to A0.

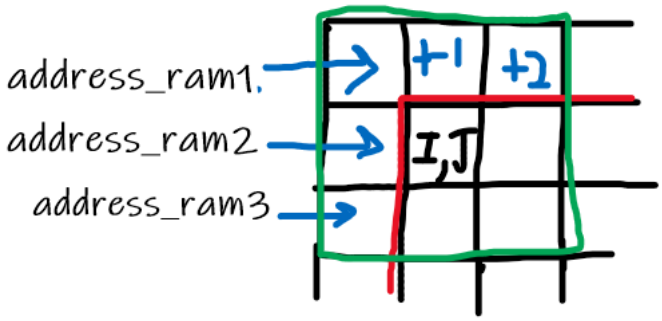
Almost same process will be in A1 and A2, only the address for rom read(address_rom) will be different.

The sub_count will vary from 0 to 10 as it will track of all the work for one value of (I,J) of final image. 0 to 8 for read, 1 to 9 for MAC and 10th for write as read for ram and rom will give data after clock edge.

The count will vary from 0 to 18643((118*158)-1) as it will keep track that for how much (I,J) the work is done, total no of (I,J) is 118*158 as we can't do for the corner row and column of original image.

The address for read in rom(address_rom) will be initialized with 0 if switch=0 and 16 if switch=1. It will increment by one on each increment of sub_count and become 0 or 16 again when sub_count=10.

The address_write will be initialized with 32768 and increment by 1 on each increment of count. When count become 18643 it will again become 32768.



The address_rom1,address_rom2,address_rom3 are three parameter to perform the operation as it will be easier then to do all the work. It will be initialized with 0,160,320 respectively.

For the I,J given in image will be computed by using the 9 blocks of original image which is inside green box. So depending on count we can choose address for ram read or write. Which is there in vhdl and after these 9 read and one write the address_ram1,2,3 will be incremented by 1 so the next 9 will be accessed by the same way. There is one more thing is that when the I,J will change row then there should be increment of 3 in address_ram1,2,3 which is checked by count_col as it will happen when count_col become 157.