SPICE Project

Done by:-

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QUESTION 1 : Simulation of symmetrical and skewed CMOS inverter, and pass transistor

Minimum sized NMOS parameters:-

Channel length(Ln) = 180𝜇𝑚

Channel Width(Wn) = 400𝜇𝑚

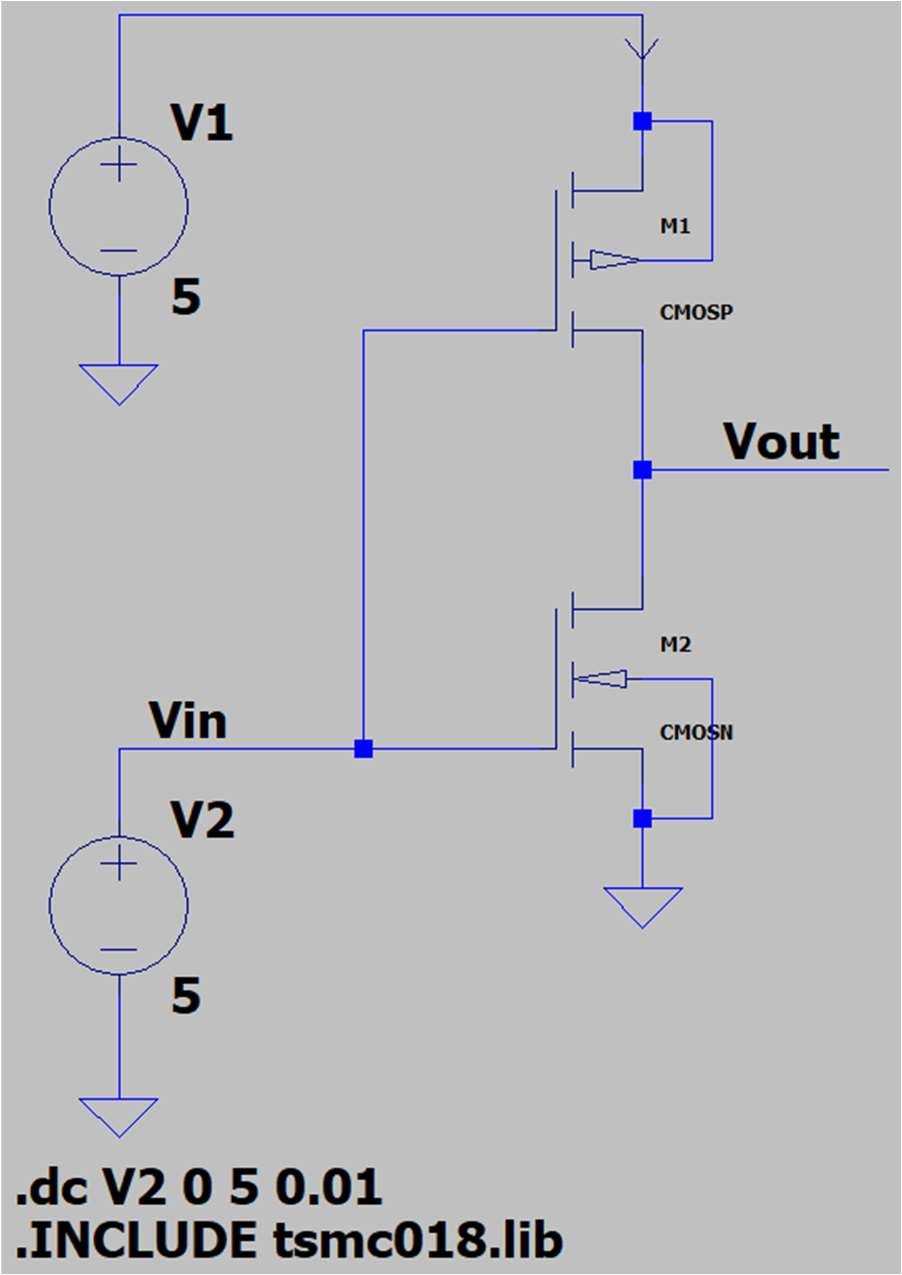
Minimum sized PMOS parameters:-

Channel length(Lp) = 180𝜇𝑚

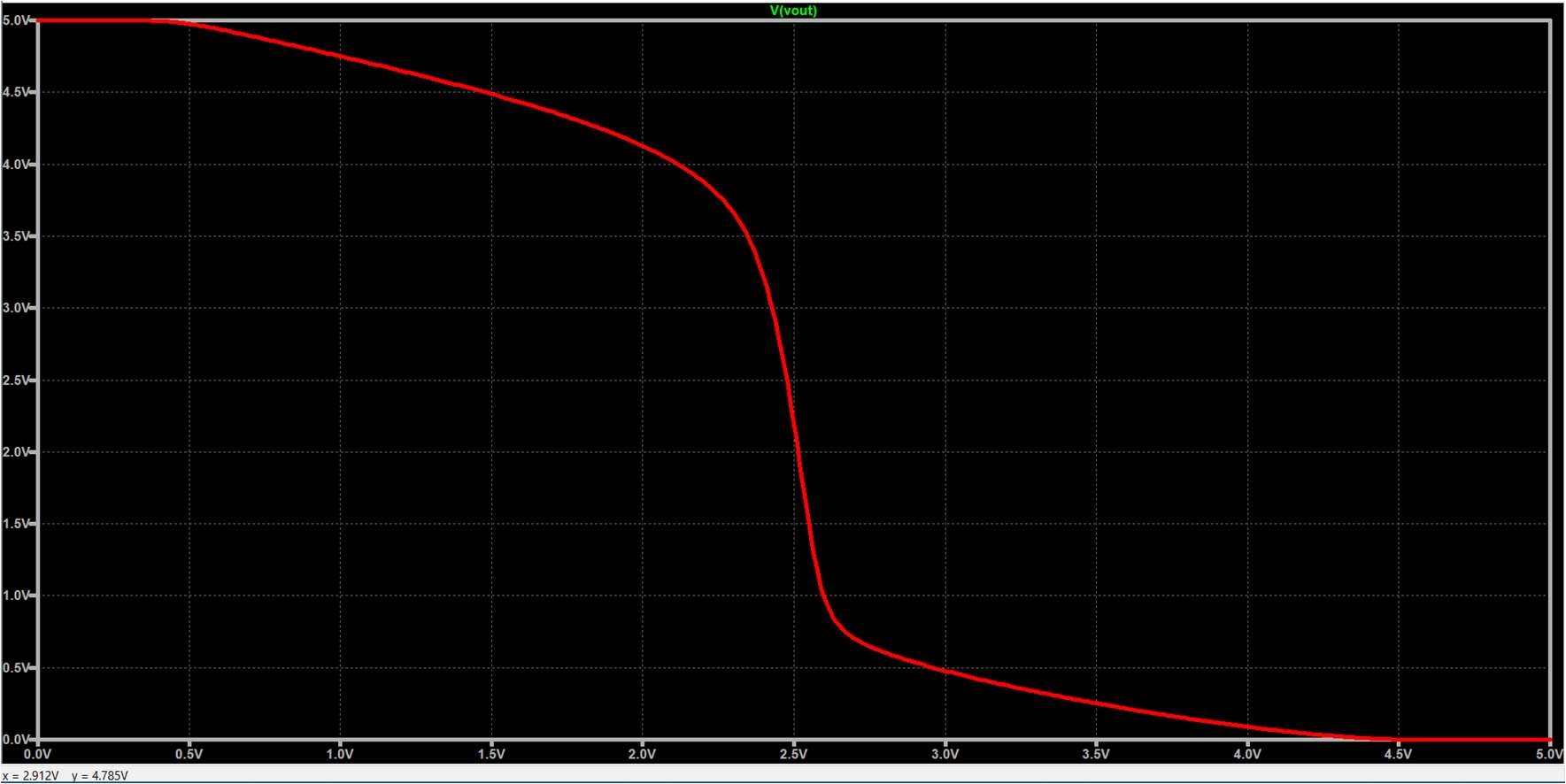
Channel width(Wp)= 800𝜇𝑚

PART A:

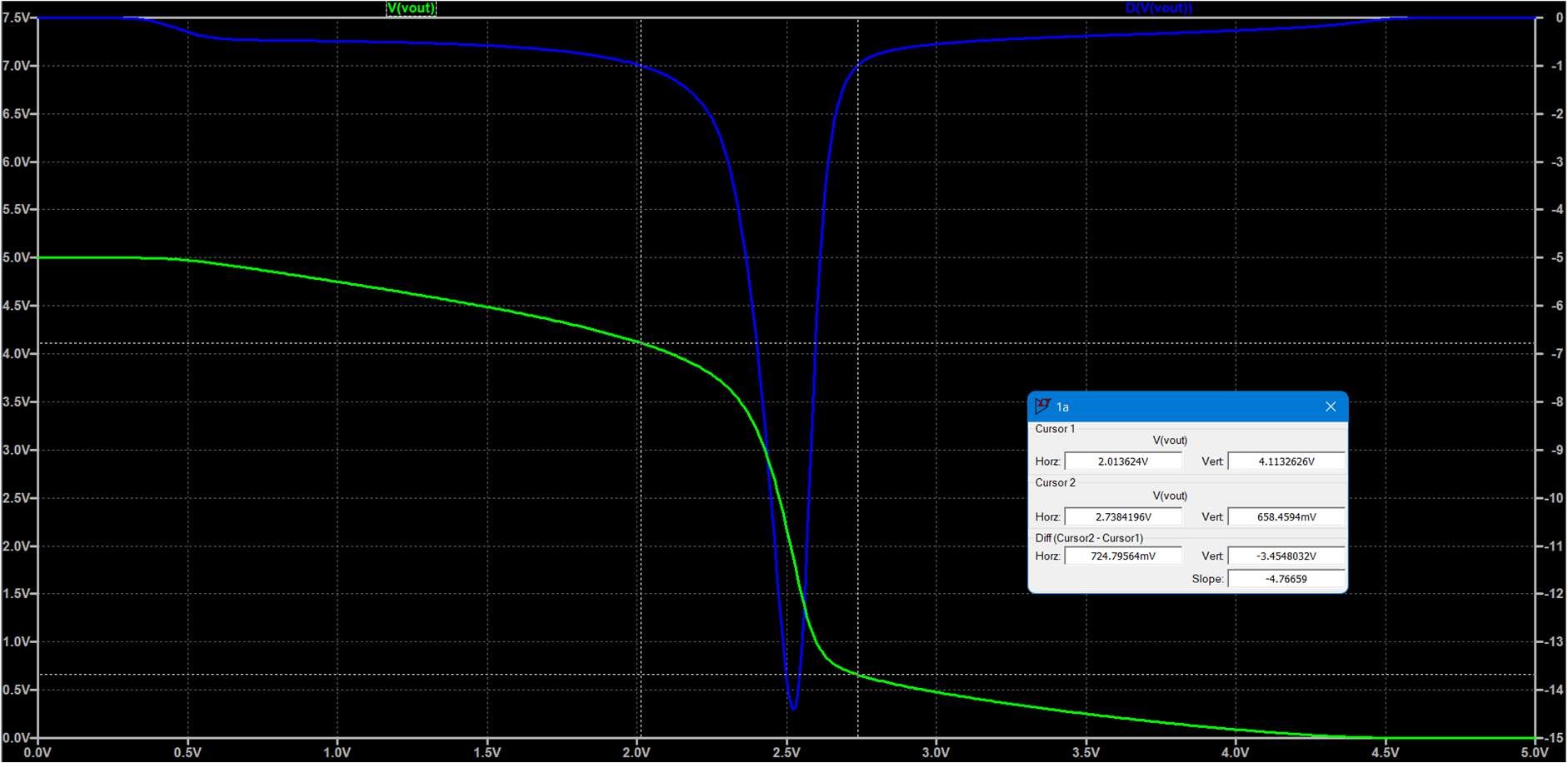
Since 2𝜇 =𝜇 , we take W/L ratio of pmos twice as that of nmos

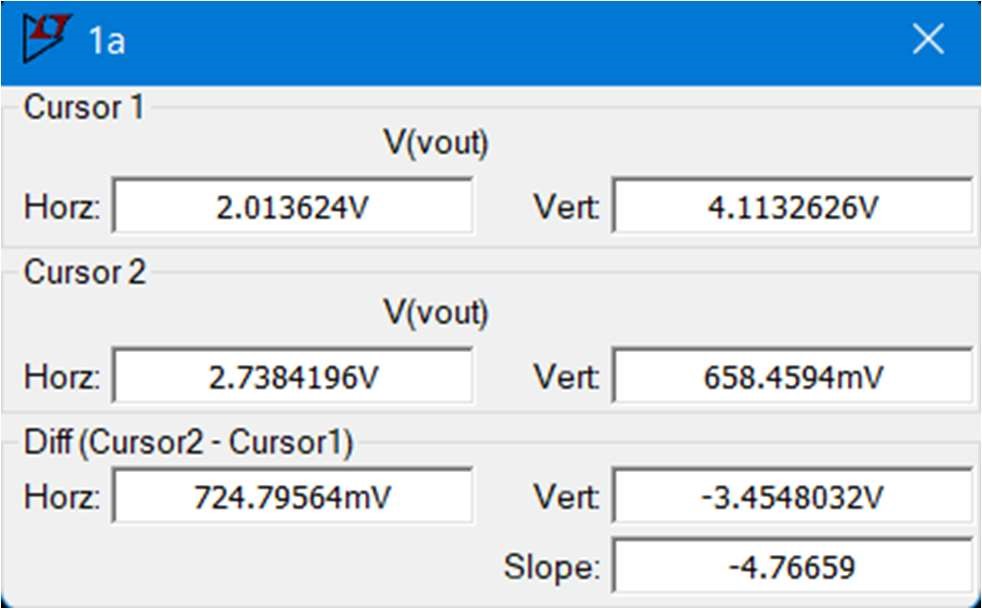


VTC of minimum sized inverter:



Calculation of VOL, VIL, VOL, VOH





VOL = 658.459 mV

VIL = 2.013 mV

VIH = 2.73 mV

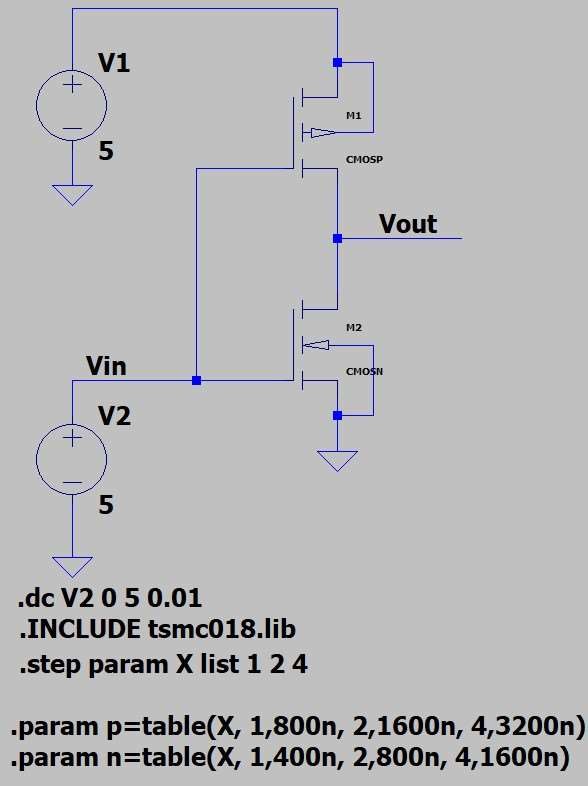
VOH = 4.11 mV

High noise margin = VOH – VIH = 1.38 mV

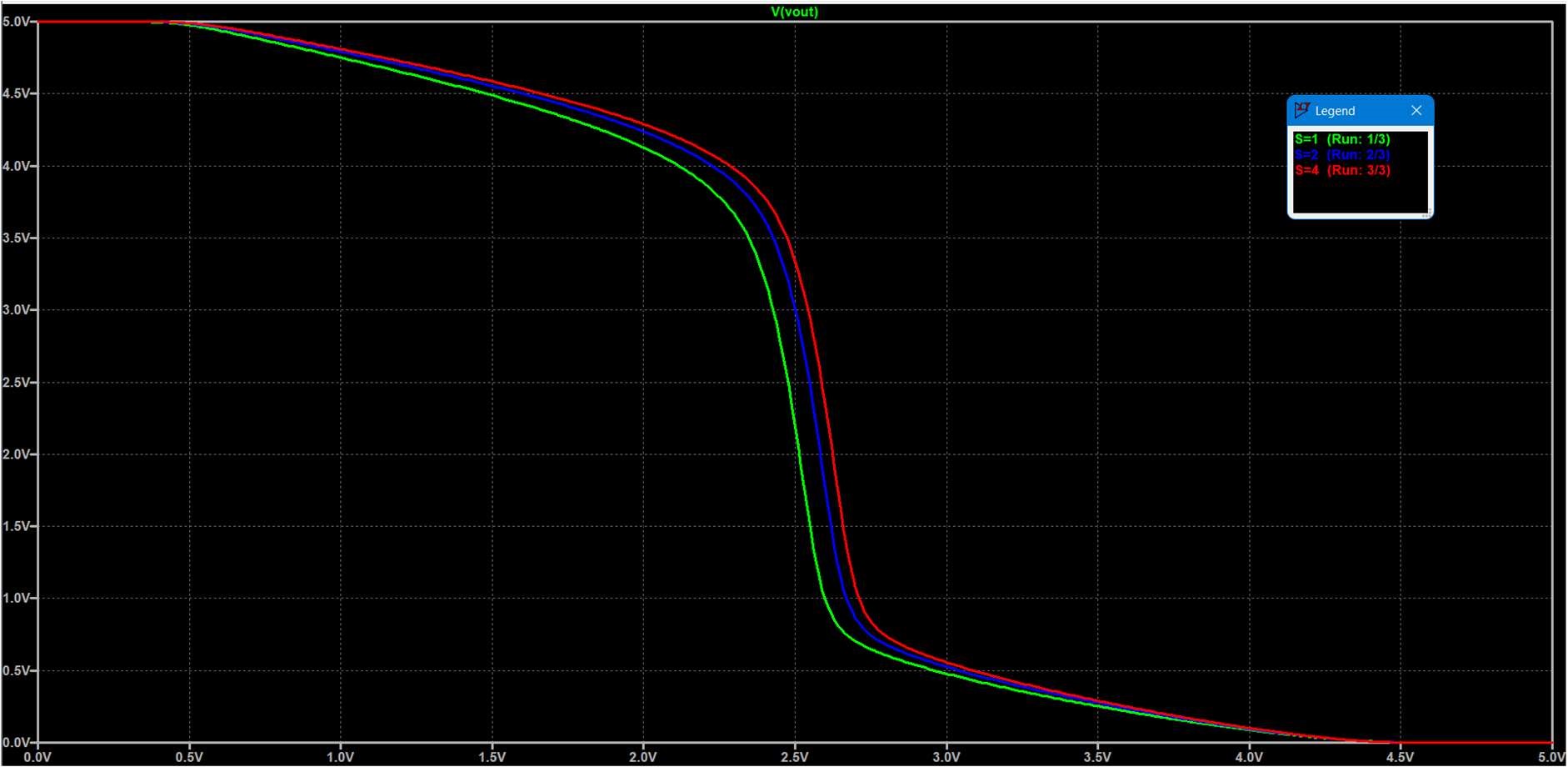
Low noise margin = VIL - VOL = 1.4428 mV

Noise immunity of inverter

VTC of inverter when S=1,2,4 :- Schematic:



As S increases, VTC shifts towards right

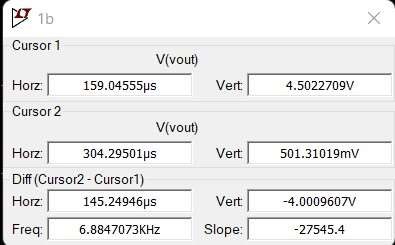


PART B:

1. When no external capacitance is attached.

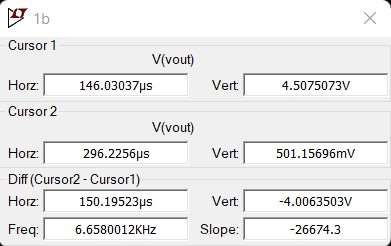
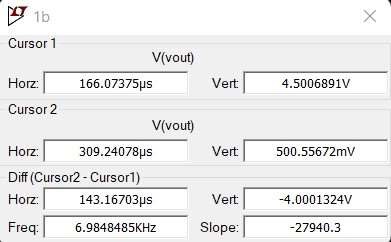
Fall Time :



Fall time delay when S is 1 = 150.19 𝜇𝑠

Fall time delay when S is 2 = 145.24 𝜇𝑠

Fall time delay when S is 4 = 143.167 𝜇𝑠



Rise Time:

Rise time delay when S is 1 = 149.53

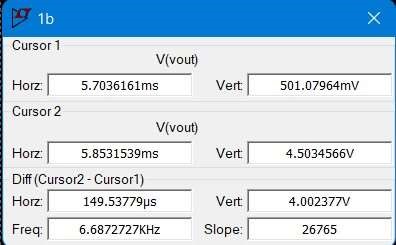
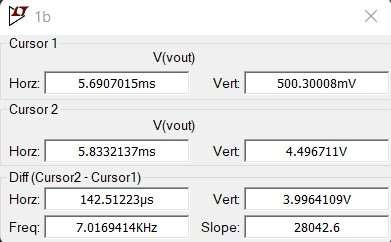
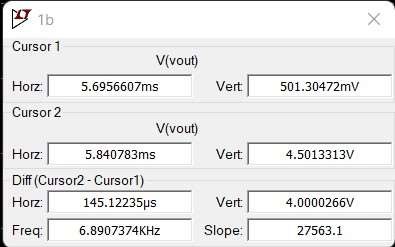
𝜇𝑠

Rise time delay when S is 2 = 145.122

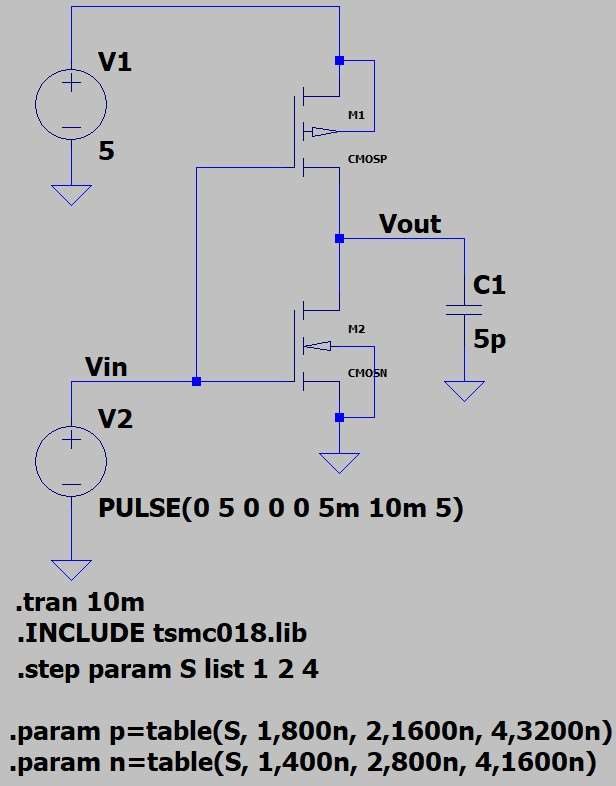
𝜇𝑠

Rse time delay when S is 4 = 142.51

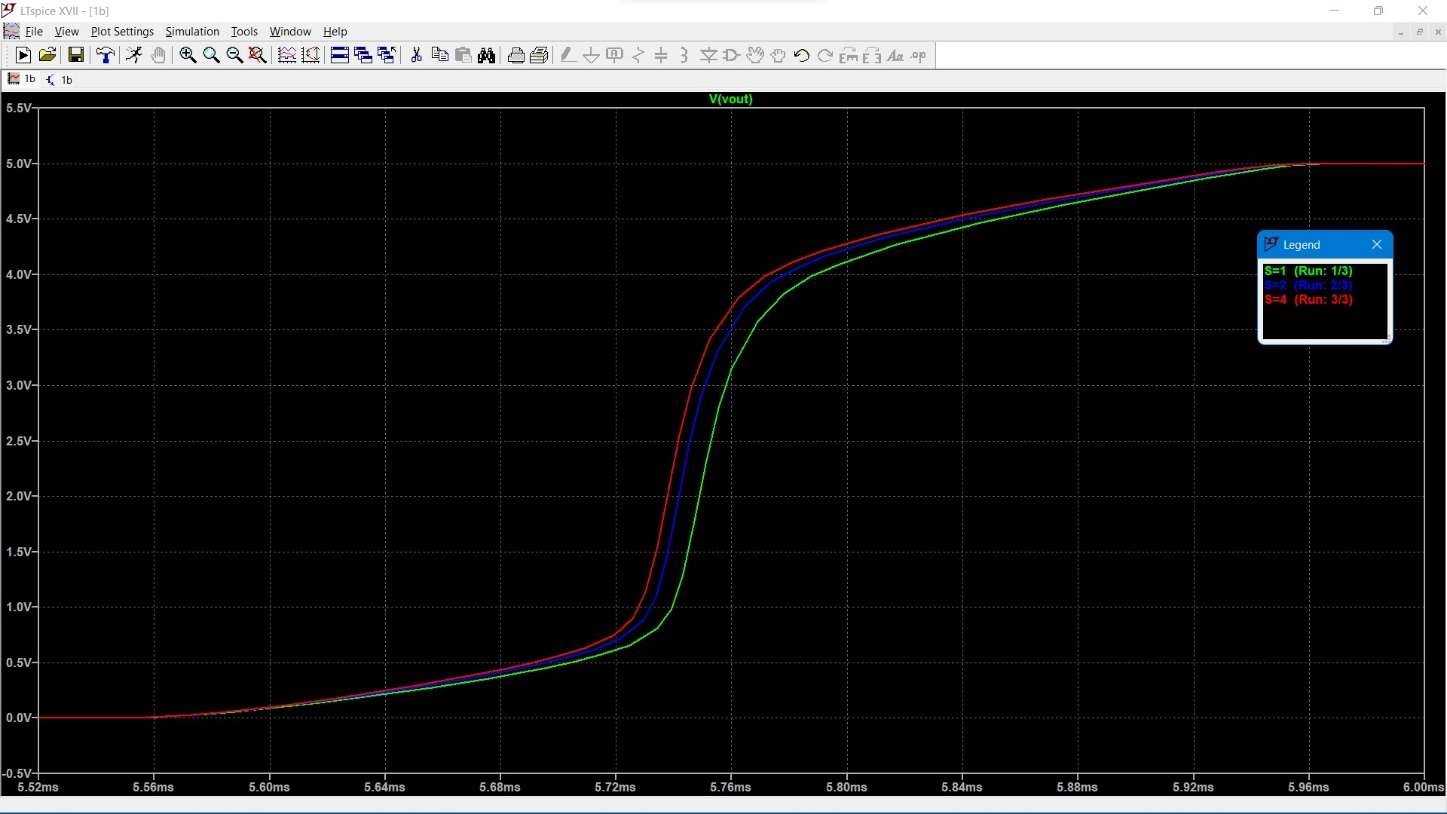
𝜇𝑠



1. When external capacitance(5pF) is attached:



Rise time:

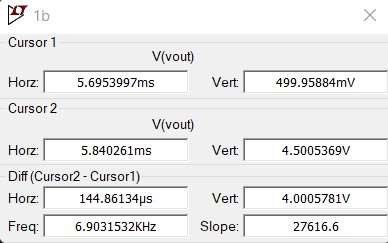
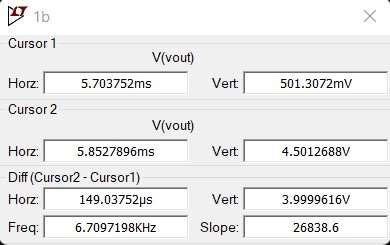


Rise time delay when S is 1 = 149.53 𝜇𝑠

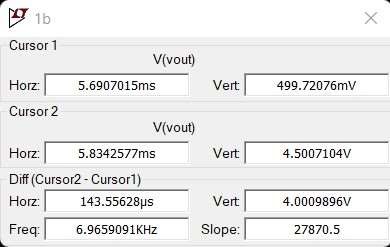
Rise time delay when S is 2 = 145.122 𝜇𝑠

Rse time delay when S is 4 = 142.51 𝜇𝑠

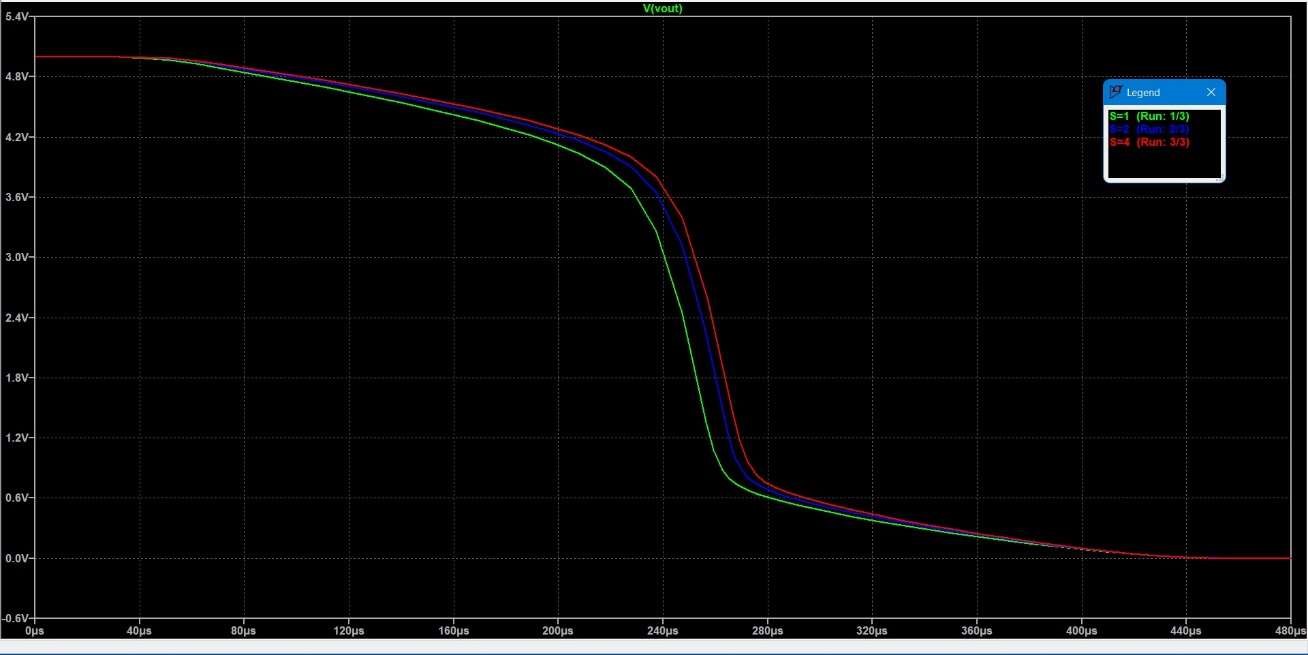
S=1 S=2



S=3



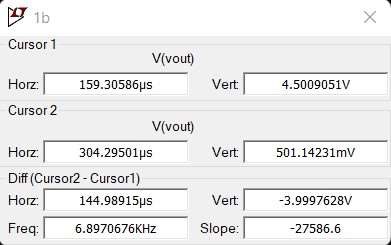
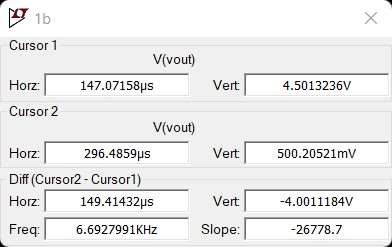
Fall Time:

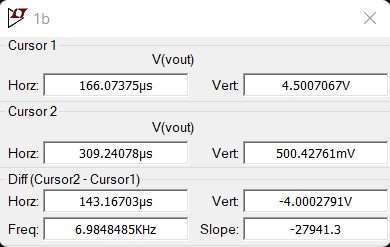


Fall time delay when S is 1 = 149.41 𝜇𝑠

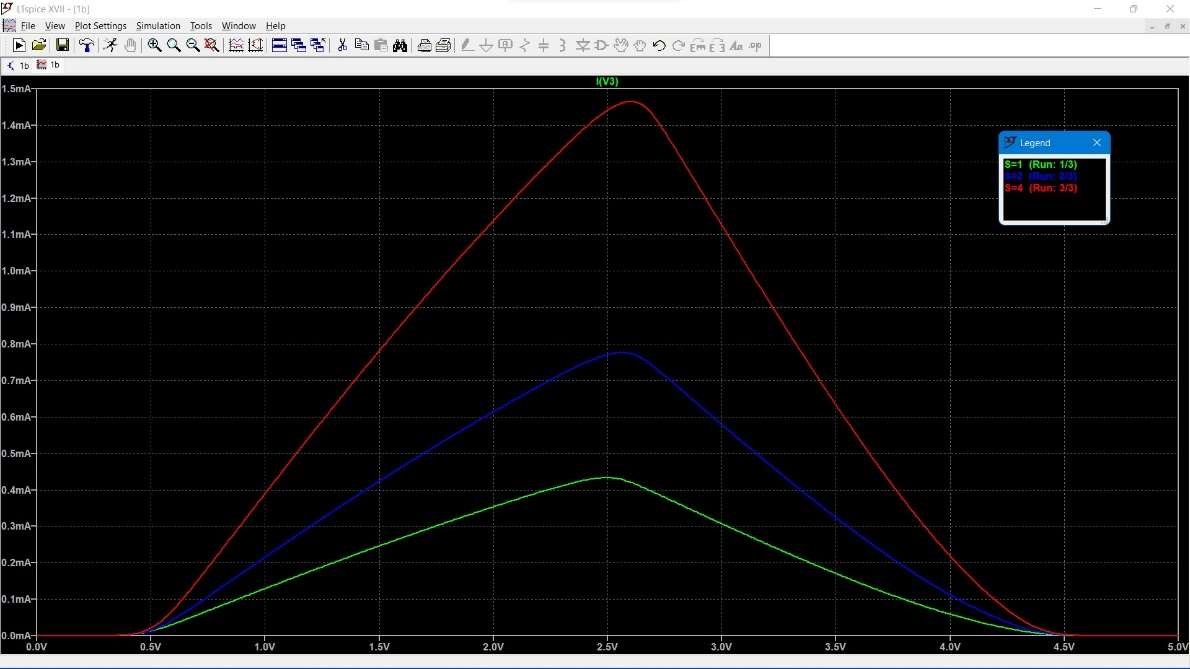
Fall time delay when S is 2 = 144.989 𝜇𝑠

Fall time delay when S is 1 = 143.16 𝜇𝑠

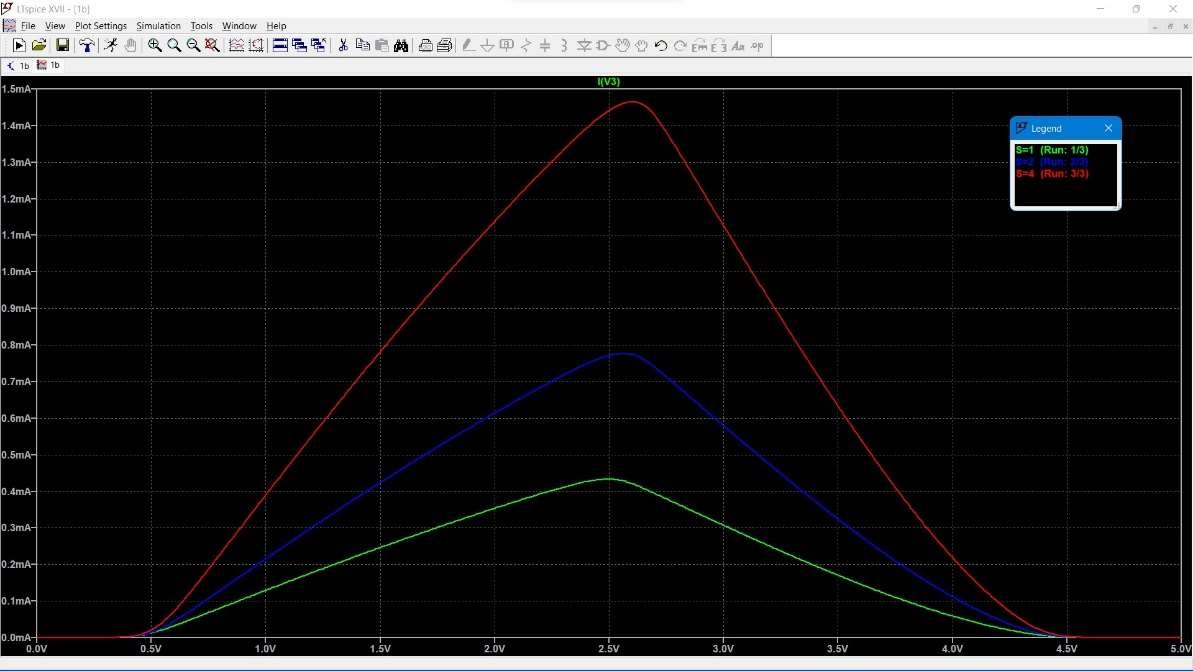




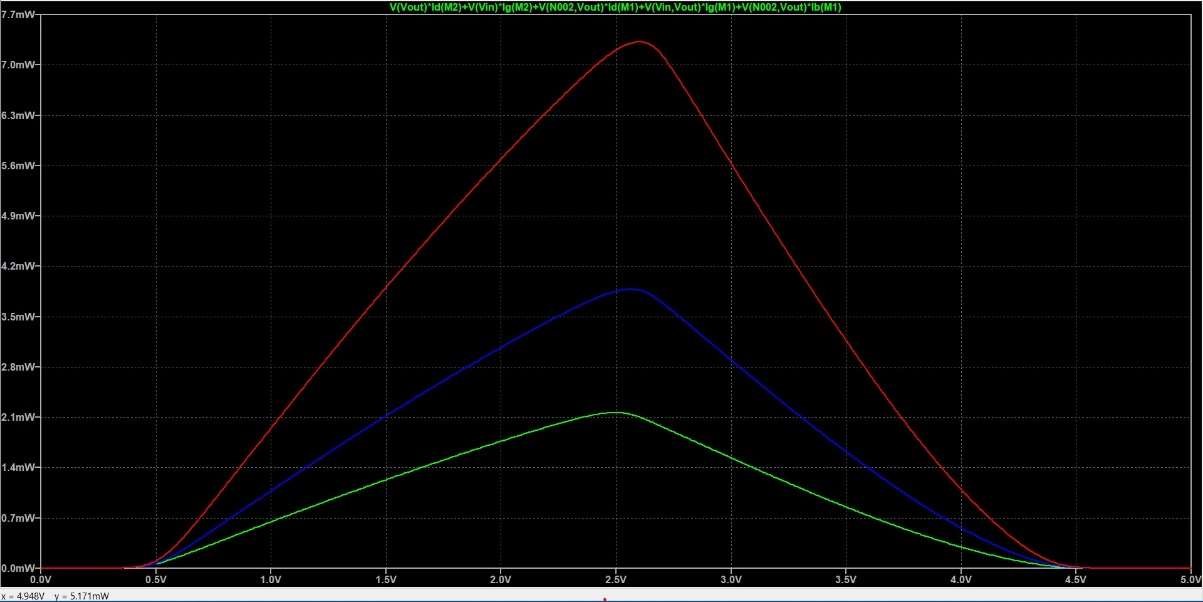
Current drawn when capacitor is not connected :



Current drawn when capacitance is connected:

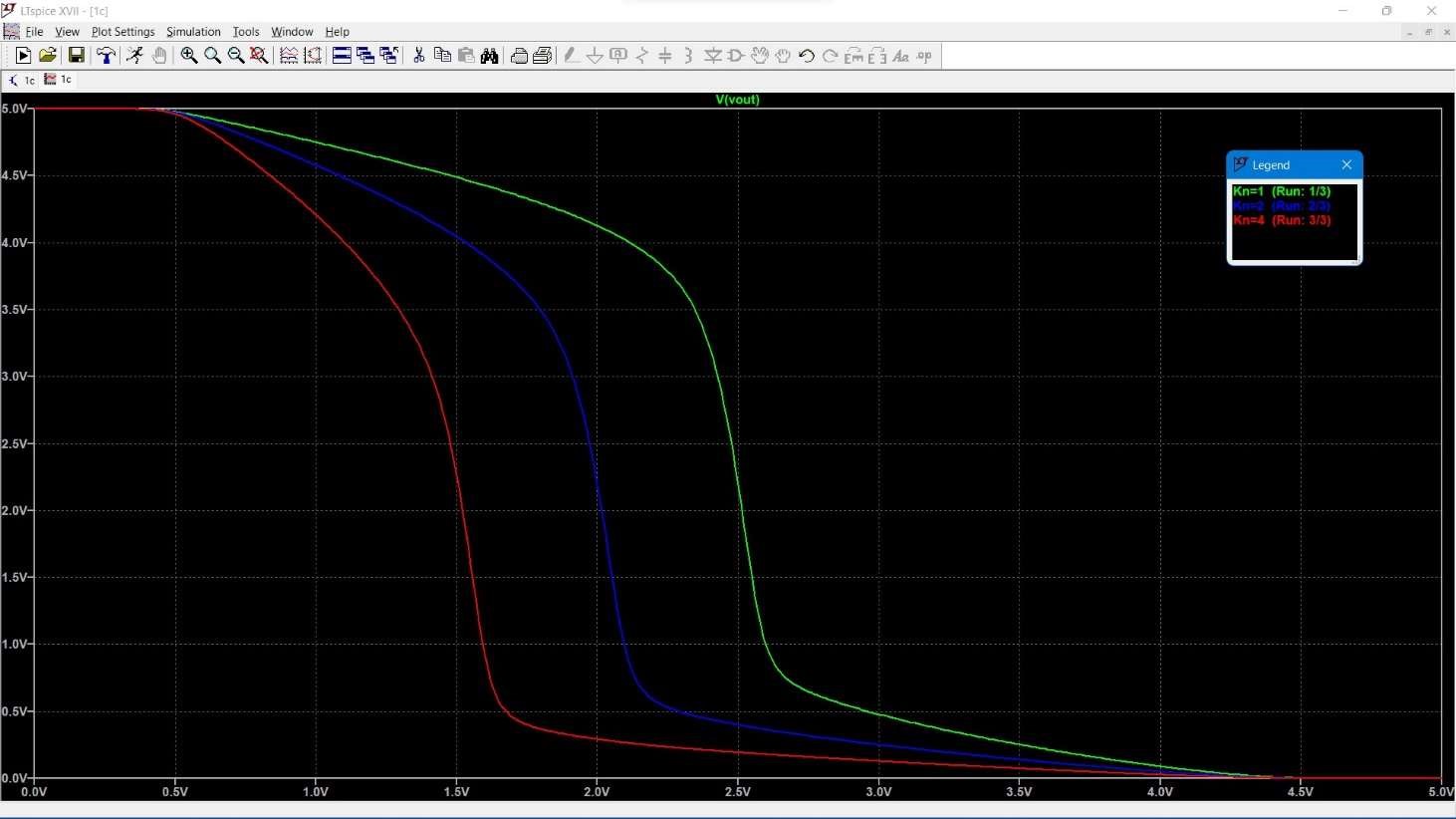
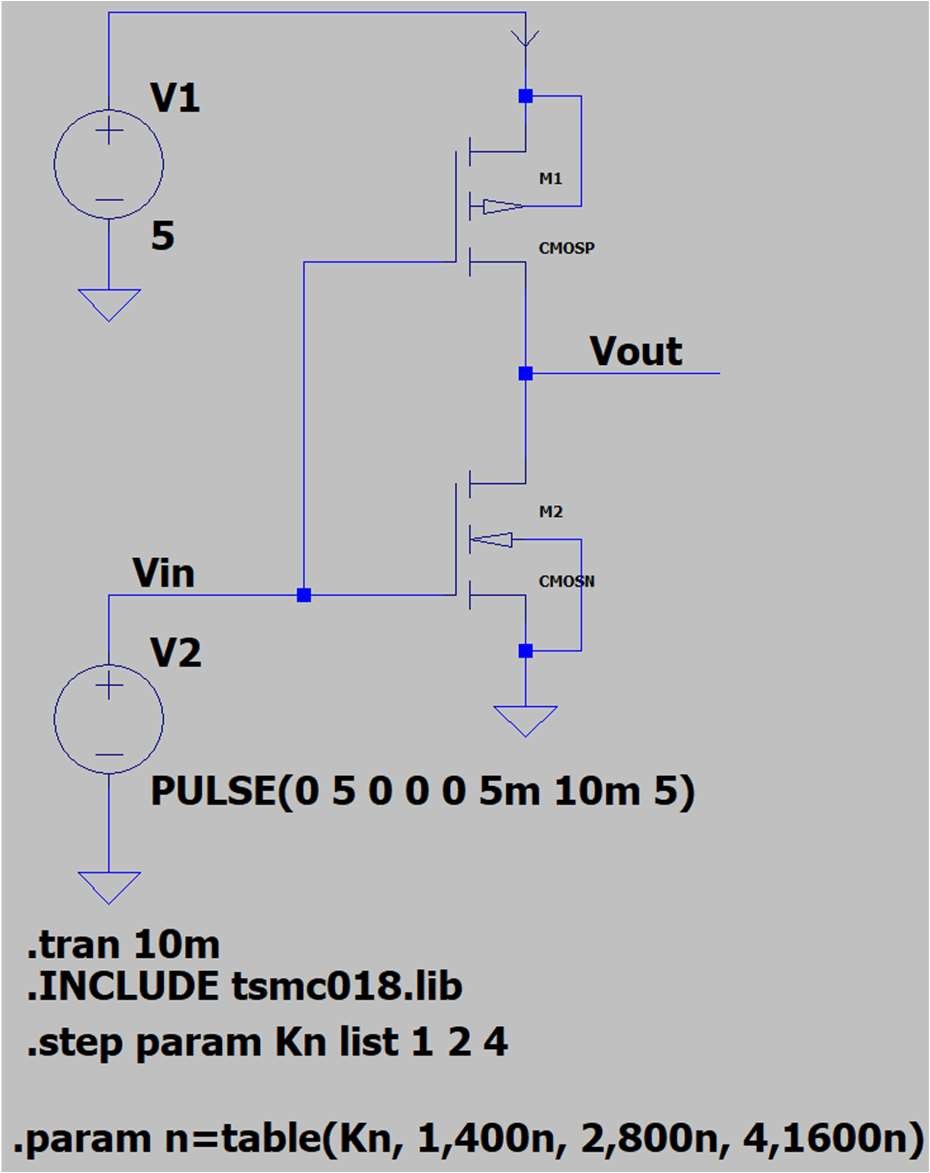


Power dissipation:



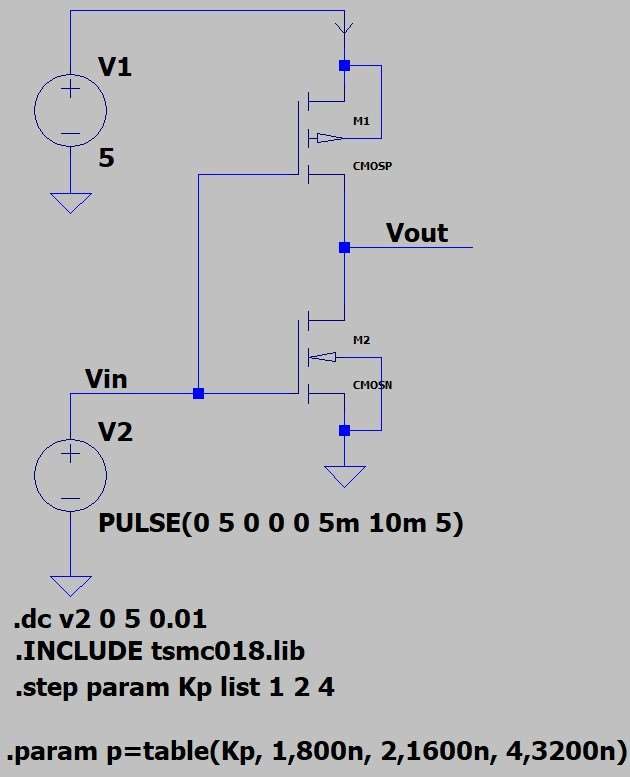
PART C:

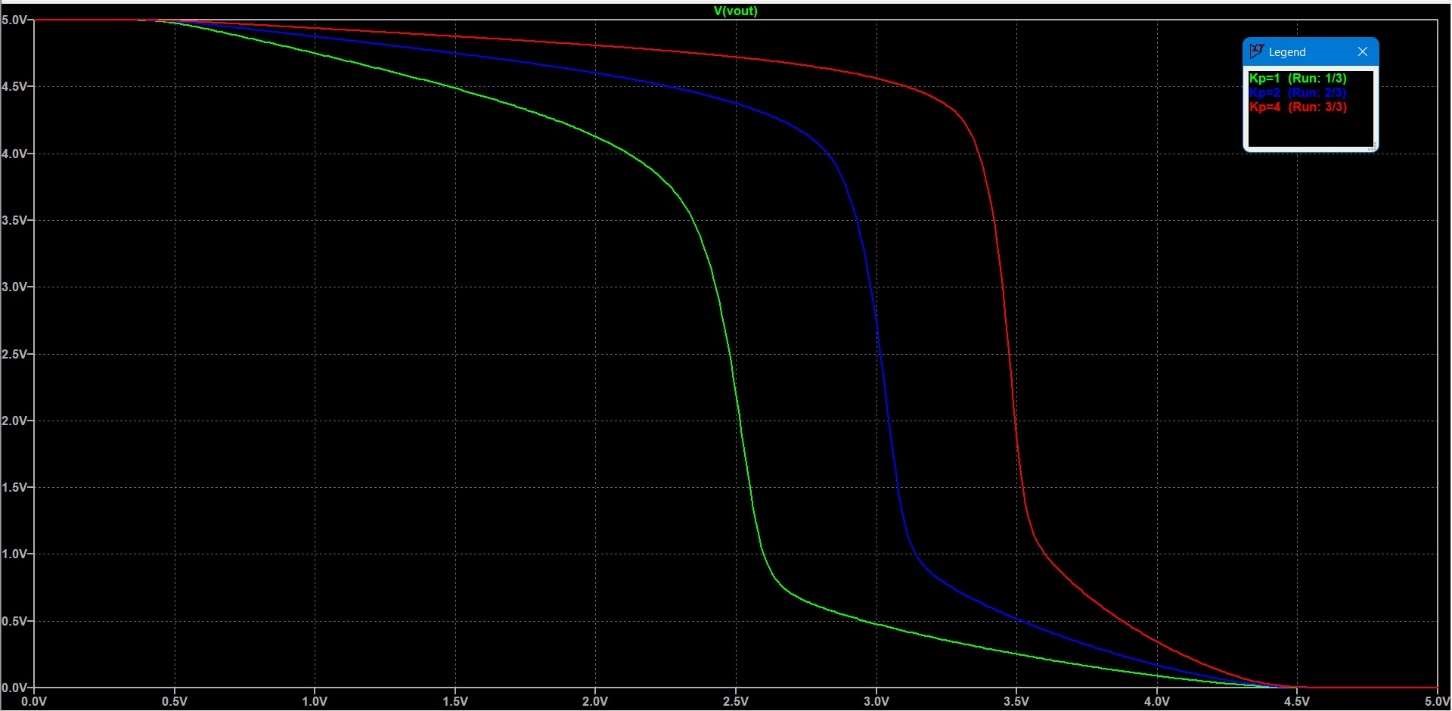
1. VTC when Kn = 1,2,4 :



As Kn increases, VTC shifts towards left

1. VTC when Kp = 1,2,4





As Kp increases, VTC shifts towards right

PART D:

When Kp is varied(Kp=1,2,4) and Kn is fixed.

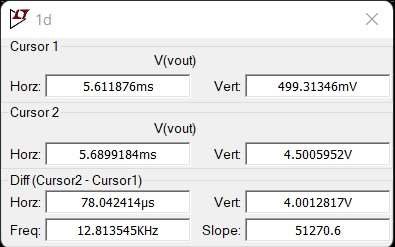
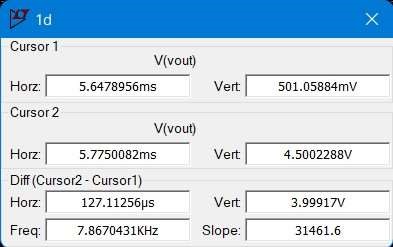
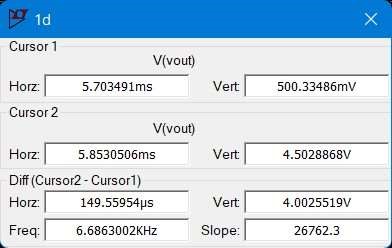
(i) Rise time delays when external capacitor is not attached :



Rise time delay when Kp is 1 = 149.55 𝜇𝑠

Rise time delay when Kp is 2 = 127.11 𝜇𝑠

Rise time delay when Kp is 4 = 78.04 𝜇𝑠

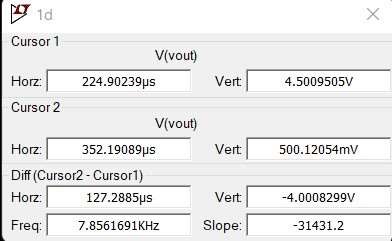
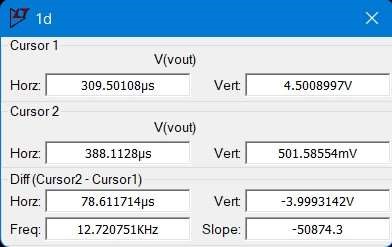


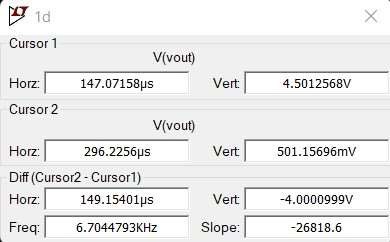
Fall time delays when external capacitor is not attached :



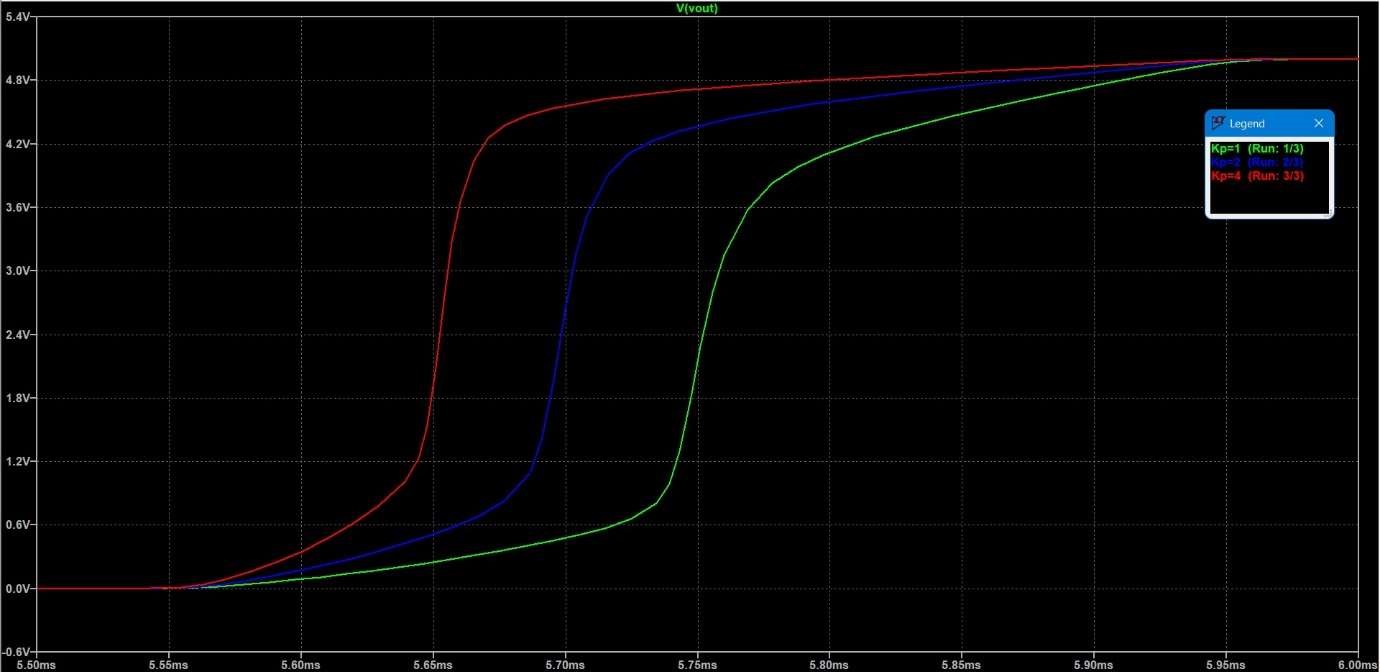
Fall time delay when Kp is 1 = 78.611 𝜇𝑠

Fall time delay when Kp is 2 = 127.2885 𝜇𝑠 Fall time delay when Kp is 4 = 149.154 𝜇𝑠





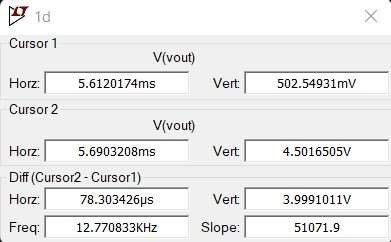
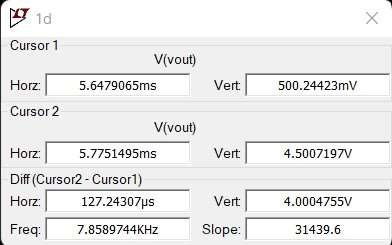
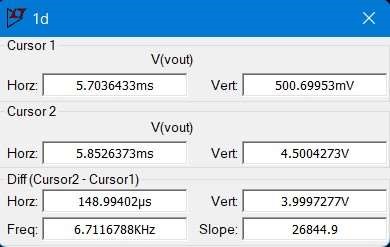
Rise time delays when external capacitor is attached :



Rise time delay when Kp is 1 = 148.99 𝜇𝑠

Rise time delay when Kp is 2 = 127.243 𝜇𝑠

Rise time delay when Kp is 4 = 78.303 𝜇𝑠

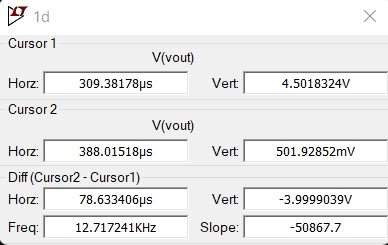
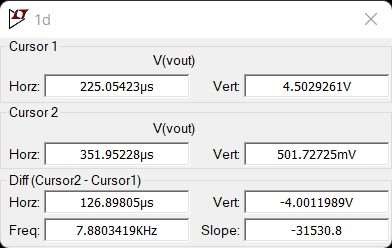


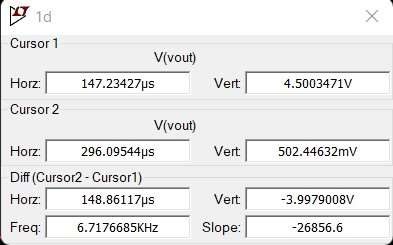
Fall time delay when capacitor is attached:



Fall time delay when Kp is 1 = 78.633 𝜇𝑠

Fall time delay when Kp is 2 = 126.89 𝜇𝑠 Fall time delay when Kp is 4 = 149.86 𝜇𝑠





When Kn is varied(Kn=1,2,4) and Kp is fixed.

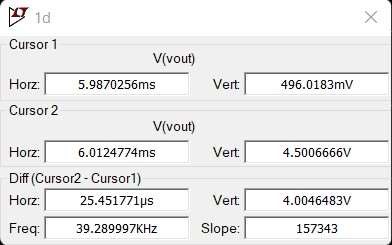
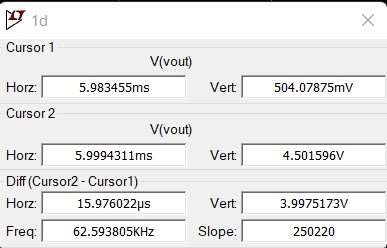
(i) Rise time delay when no external capacitance is connected



Rise time delay when Kn is 1 = 13.824 𝜇𝑠

Rise time delay when Kn is 2 = 16 𝜇𝑠

Rise time delay when Kn is 4 = 25.451 𝜇𝑠



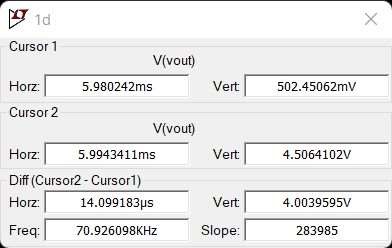
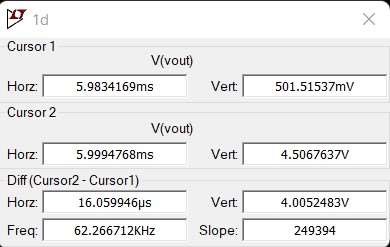
Rise time delay when external capacitance(5pF) is connected:

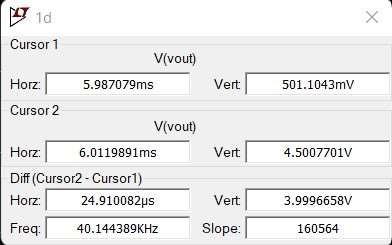


Rise time delay when Kn is 1 = 16.05 𝜇𝑠

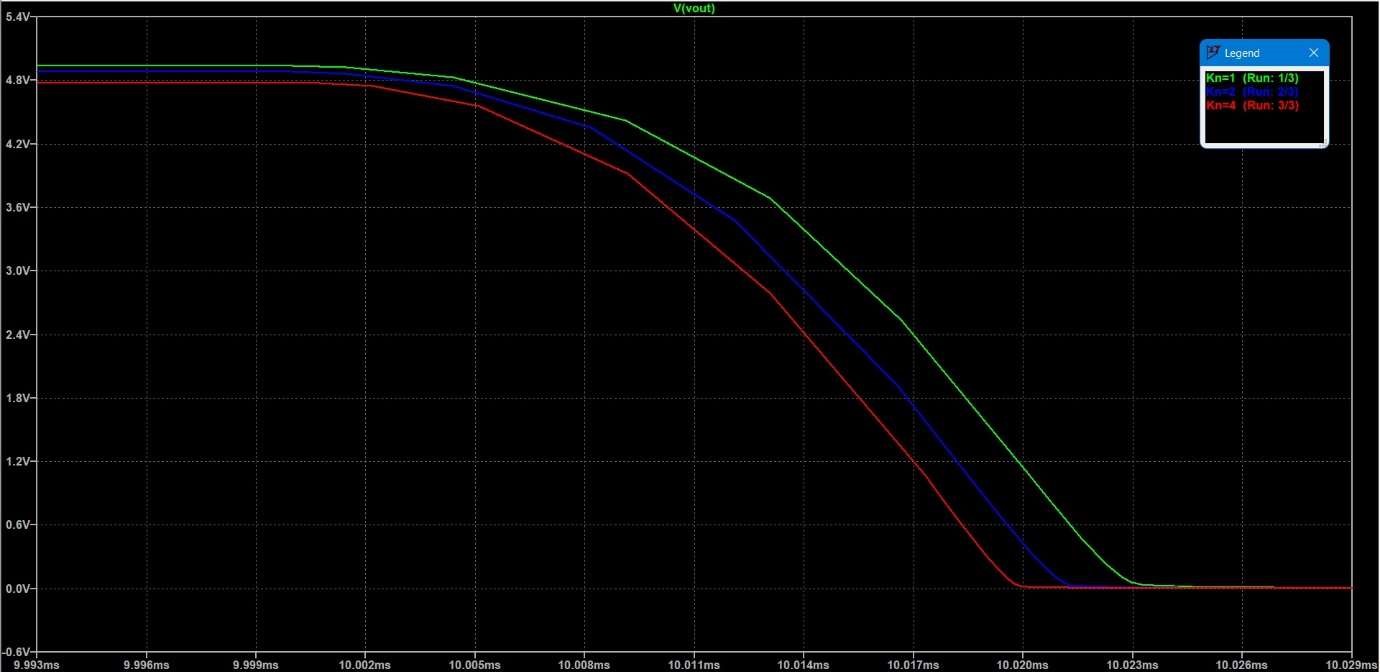
Rise time delay when Kn is 2 = 14.1 𝜇𝑠

Rise time delay when Kn is 4 = 24.91 𝜇𝑠





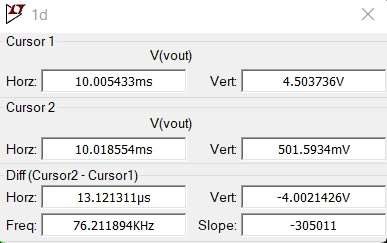
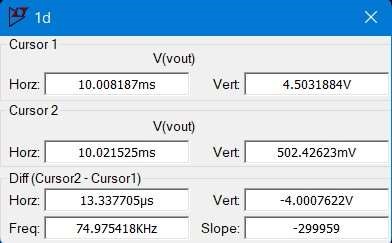
Fall time delay when external capacitor is not connected:

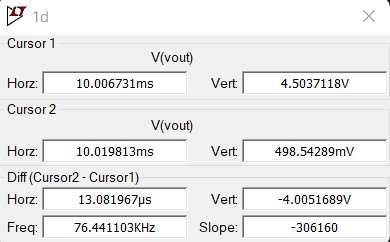


Fall time delay when Kn is 1 = 13.33 𝜇𝑠

Fall time delay when Kn is 2 = 13.12 𝜇𝑠

Fall time delay when Kn is 4 = 13.081 𝜇𝑠





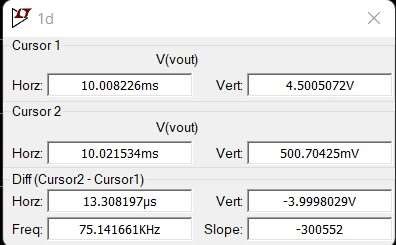
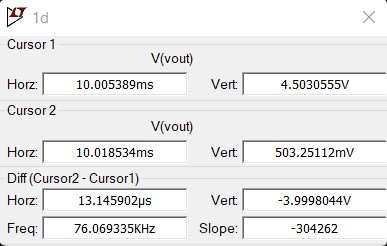
Fall time delay when external capacitor(5pF) is connected:

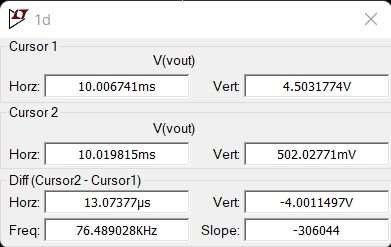


Fall time delay when Kn is 1 = 13.14 𝜇𝑠

Fall time delay when Kn is 1 = 13.3 𝜇𝑠

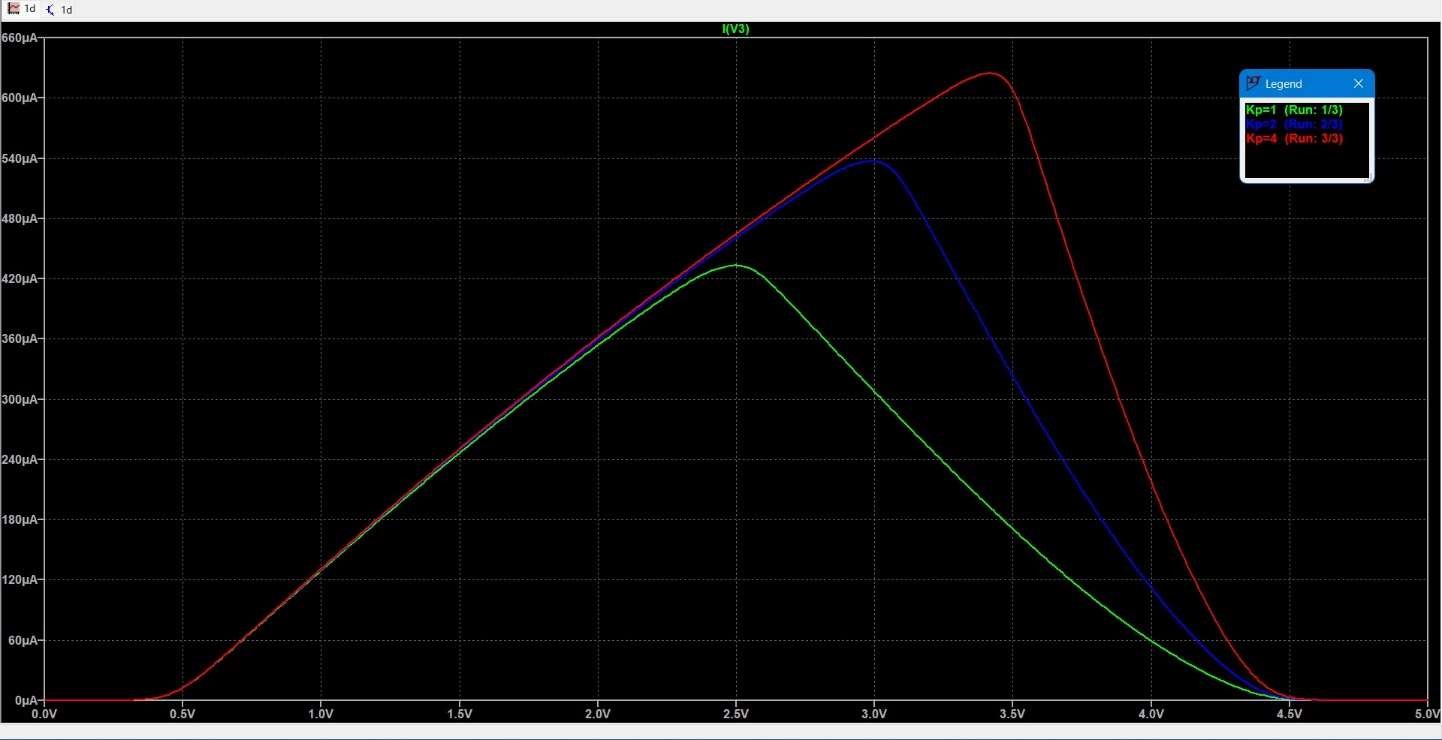
Fall time delay when Kn is 1 = 13.07 𝜇𝑠



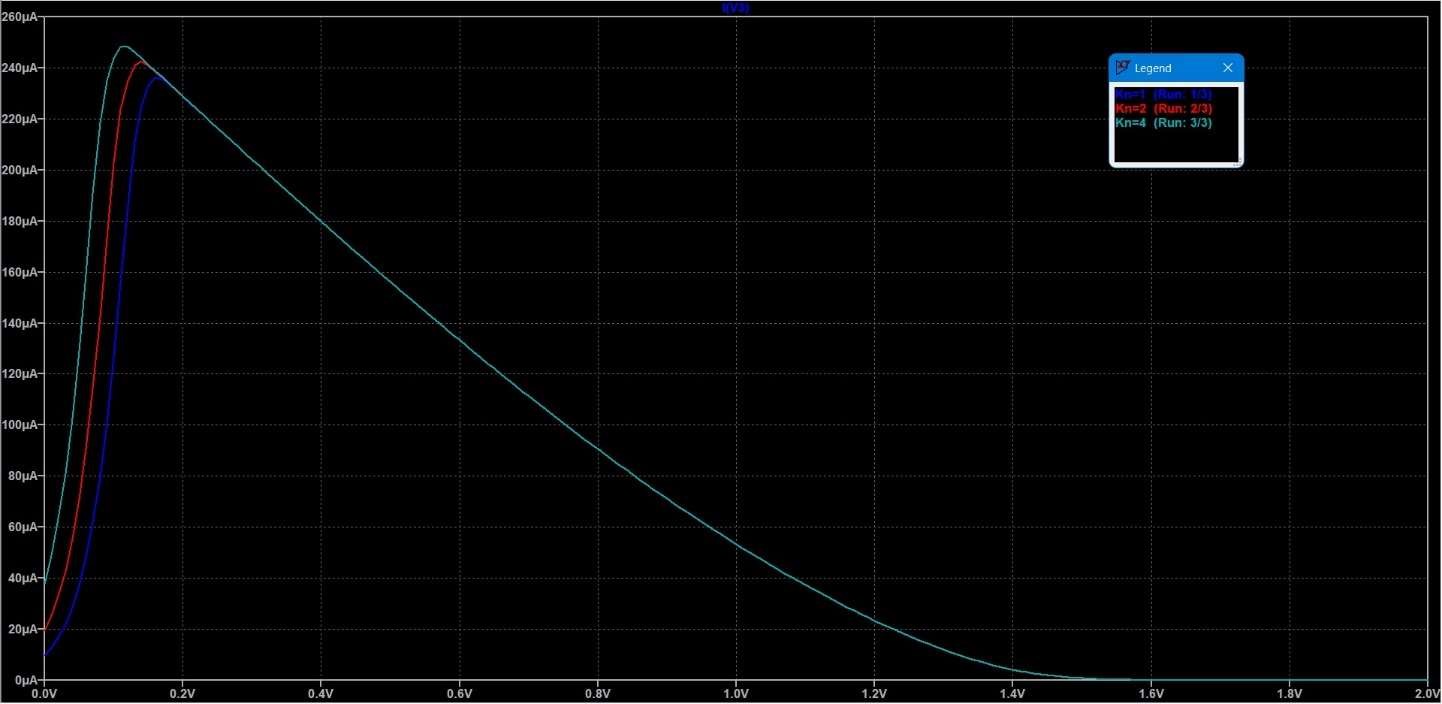


Current drawn from the power supply when capacitor is not connected at the output:

1. When Kp is varied(Kp=1,2,4) and Kn is fixed

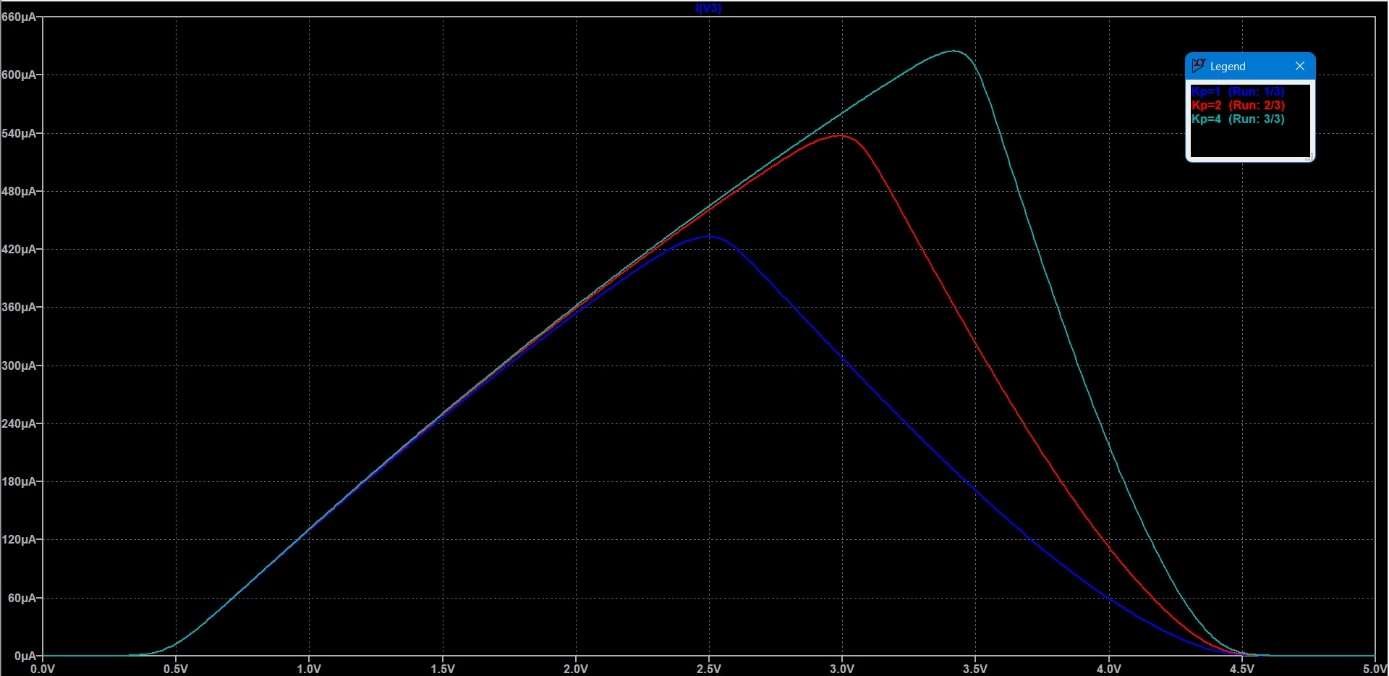


1. When Kn is varied(Kn=1,2,4) and Kp is fixed



Current drawn from the power supply when capacitor is connected at the output:

1. When Kp is varied(Kp=1,2,4) and Kn is fixed



1. When Kn is varied(Kn=1,2,4) and Kp is fixed

