T GOVARDHAN

M.Tech | Department of Electrical Engineering, IIT Kanpur
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ACADEMIC QUALIFICATIONS

DEGREE	INSTITUTE	YEAR	CPI/%
M.Tech(EE)	Indian Institute of Technology, Kanpur	2022 - Present	8.13/10
B.Tech(EE)	Chaitanya Bharathi Institute of Technology, Hyderabad	2014 - 2018	7.12/10
Class XII (Intermediate)	Sri Chaitanya Boys Junior College, Vijayawada	2012 - 2014	94.7%
Class X (SSC)	AP Residential BC Boys School, Chityala	2012	9.8/10

SCHOLASTIC ACHIEVEMENTS

- Secured **All India Rank 451** in GATE (EE) 2023.
- Secured **"A" grade in Industrial Automation and Control (EE617A)** in 2022-23, I Semester, IIT Kanpur.
- Secured **"A" grade in Non-linear Control (EE798R)** in 2022-23, Summer term Course, IIT Kanpur.

WORK EXPERIENCE

• Chegg India Private Limited
*Position: **Subject Matter Expert** in Electrical Engineering.*

- Worked as a freelance independent contractor by providing solutions to student's questions.

ACADEMIC PROJECTS

• Design and implementing a control technique for a ball-plate balancing system. (*Ongoing*)
M.Tech Thesis | Supervisor: Dr. Soumya Ranjan Sahoo, DisCon Lab, IIT Kanpur.

- Initially Implementing a ball-beam balance to control the position of a ball on a beam
- The objective of this project is to control a ball on a plate when disturbance is applied to the ball.

• Efficient DC Fast Charging System for Electric Vehicles by using 12-Pulse Rectifier with DC-Side Buck Converters.
B.E Project (Major) (July'17 – May'18)

- Charge the Battery for EV Charging and along with maintain the good power factor.
- The main application of this project was EV Charging.

COURSE PROJECTS

• Design of single-stage differential amplifier (Analog VLSI Circuits) (*Nov'22*)
Course Project : EE610A | Instructor: Dr. Imon Mondal, IIT Kanpur.

The design was based on non-inverting configuration with an open loop gain of 40dB, 3dB bandwidth of 25MHz, CMMR of 80dB, power supply of 1.8V in LTSPICE.

• Simulation of symmetrical and skewed CMOS inverter (Self Project) (*June'23*)
Simulation of symmetrical CMOS inverter and observed static VTC, noise margin, and effect of CMOS inverter sizing on VTC in LTspice.

• FSM design of Electronic lock (Self Project) (*May'23*)
Verilog code implemented with a finite state machine that represents the behavior of a digital lock with a specific sequence of button presses required to open the lock (01011) and verified with the testbench.

• Simulation of multiplexer at the structural level and simulation of JK flip-flop Using Verilog (Self Project) (June'23)
Simulated 2:1 MUX at structural and behavioral level using Verilog and verified the results using a test bench. Simulated JK flip-flop at structural level and implemented up-counter using JK flip-flop and verified results using a test bench.

• High Frequency Two Stage Miller Compensated Opamp with Single Ended Output (self-project). (*May'23*)
Designed a two-stage miller compensated opamp achieving <1% settling error and Developed Closed-loop bandwidth of >25MHz (180 nm).

• Reachability of Unicycle using Lie Algebra (EE651A) (*May'23*)
Course Project : EE651A | Instructor: Dr.Abhilash Patel, IIT Kanpur.

The reachability of unicycle is analyzed by the application of lie algebra.

• Lyapunov-Based Tracking Control for Unicycle Mobile Robot (EE798R) (*July'23*)
Course Project : EE798R | Instructor: Dr.Abhilash Patel, IIT Kanpur.

Implemented control strategy based on Lyapunov approach for nonholonomic Unicycle mobile robot

RELEVANT COURSE WORK

Analog VLSI Circuits	Basics of Modern Control Systems
Digital Control	Digital Electronics
Linear Control Systems	Signals and Systems
Power Semiconductor Drives	Advanced Protective Relaying
Industrial Automation and Control	Nonlinear systems
Electrical Machines	Nonlinear Control
Power Systems	Digital Signal Processing
Power Electronics	Power System Operation and Control
Switch Gear and Protection	Analog Electronics
HVDC and FACTS	Measurements and Instruments
Microprocessor and Microcontrollers	Utilization of Electrical Energy
Fuzzy Set, Logic & Systems & Applications	Renewable Energy

AREA OF INTEREST

Analog VLSI Circuits, Analog IC Design, Digital VLSI Design, Digital Electronics, Power Electronics, Power Systems, Electrical Machines, Electric Drives, FPGA and ASIC Design, Analog Electronics.

TECHNICAL SKILLS

- **Programming languages:** MATLAB, C, Verilog.
- **Softwares and Tools :** Simulink, Free CAD, LaTeX, LTSpice, MS Office

POSITIONS OF RESPONSIBILITY

- **Teaching Assistant** for Control System Lab (EE380A) in **IIT-Kanpur**
- **Teaching Assistant** for Robust Control (EE654A)in **IIT-Kanpur**

ADDITIONAL INFORMATION

- Hobbies: Playing Cricket, Playing Chess, Listening to Music, Cycling.
- Languages Known: English, Telugu, Hindi.