Bold means that any value is accepted.

Required OPCodes in 68K assembly

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **MOVE** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 0 | (size) | | (destination\_register\_mode) | | | | | | (Source\_mode\_register) | | | | | | | | |
| Page#: 220 | | | | | | | | | | | | | | | | | | | |
| **MOVEA** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 0 | (size) | | dest\_Register | | | 0 | 0 | 1 | (Source\_mode\_register) | | | | | | | | |
| Page#: 223 | | | | | | | | | | | | | | | | | | | |
| **ADDI** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | (size) | | (EffectiveAddress\_mode\_register) | | | | | | | | |
|  | **16BitWordData(Always Included)** | | | | | | | | **8-BitByteData(Always Included)** | | | | | | | | | | |
|  | **32-BitLongData(Included if ADDI.L is used)** | | | | | | | | | | | | | | | | | | |
| Page#: 113 | | | | | | | | | | | | | | | | | | | |
| **BTST** | | | | | | | | | | | | | | | | | | | |
| Dyn | 0 | 0 | 0 | 0 | **(Register)** | | | 1 | 0 | 0 | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Stat | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | (EffectiveAddress\_mode\_register) | | | | | | | | |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **BitNumber** | | | | | | | | | | |
| Page#: 166 | | | | | | | | | | | | | | | | | | | |
| **NOP** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | | 0 | | 0 | | 0 | 1 |
| Page#: 251 | | | | | | | | | | | | | | | | | | | |
| **RTS** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | | 0 | | 1 | | 0 | 1 |
| Page#: 273 | | | | | | | | | | | | | | | | | | | |
| **LEA** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 1 | 0 | 0 | **(Register)** | | | 1 | 1 | 1 | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 214 | | | | | | | | | | | | | | | | | | | |
| **CLR** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | (size) | | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 177 | | | | | | | | | | | | | | | | | | | |
| **JSR** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | (size) | | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 213 | | | | | | | | | | | | | | | | | | | |
| **MOVEM** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 1 | 0 | 0 | 1 | **(dr)** | 0 | 0 | 1 | **(size)** | (EffectiveAddress\_mode\_register) | | | | | | | | |
| **RegisterListMask** | | | | | | | | | | | | | | | | | | | |
| Page#: 232 | | | | | | | | | | | | | | | | | | | |
| **ADDQ** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 1 | 0 | 1 | **(data)** | | | 0 | (size) | | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 115 | | | | | | | | | | | | | | | | | | | |
| **MOVEQ** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 1 | 1 | 1 | **(Register)** | | | 0 | (data) | | | | | | | | | | |
| Page#: 238 | | | | | | | | | | | | | | | | | | | |
| **Bcc** | | | | | | | | | | | | | | | | | | | |
|  | 0 | 1 | 1 | 0 | **(Condition)** | | | | **(8-bit displacement)** | | | | | | | | | | |
| **16-BIT DISPLACEMENT IF 8-BIT DISPLACEMENT = $00** | | | | | | | | | | | | | | | | | | | |
| **32-BIT DISPLACEMENT IF 8-BIT DISPLACEMENT = $FF** | | | | | | | | | | | | | | | | | | | |
| Page#: 130 | | | | | | | | | | | | | | | | | | | |
| **DIVU** | | | | | | | | | | | | | | | | | | | |
| W | 1 | 0 | 0 | 0 | **(Register)** | | | 0 | 1 | 1 | (EffectiveAddress\_mode\_register) | | | | | | | | |
| L | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | (EffectiveAddress\_mode\_register) | | | | | | | | |
|  | 0 | **RegisterDq** | | | 0 | **size** | 0 | 0 | 0 | 0 | 0 | | 0 | | 0 | | **RegisterDr** | | |
| Page#: 201 | | | | | | | | | | | | | | | | | | | |
| **OR** | | | | | | | | | | | | | | | | | | | |
|  | 1 | 0 | 0 | 0 | **(Register)** | | | (OPMode) | | | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 254 | | | | | | | | | | | | | | | | | | | |
| **SUB** | | | | | | | | | | | | | | | | | | | |
|  | 1 | 0 | 0 | 1 | **(Register)** | | | (OP-Mode) | | | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 278 | | | | | | | | | | | | | | | | | | | |
| **CMP** | | | | | | | | | | | | | | | | | | | |
|  | 1 | 0 | 1 | 1 | **(Register)** | | | (Op-Mode) | | | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 179 | | | | | | | | | | | | | | | | | | | |
| **ADD** | | | | | | | | | | | | | | | | | | | |
|  | 1 | 1 | 0 | 1 | **(Register)** | | | (Op-Mode) | | | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 108 | | | | | | | | | | | | | | | | | | | |
| **ADDA** | | | | | | | | | | | | | | | | | | | |
|  | 1 | 1 | 0 | 1 | **(Register)** | | | (Op-Mode) | | | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 111 | | | | | | | | | | | | | | | | | | | |
| **MULS** | | | | | | | | | | | | | | | | | | | |
| W | 1 | 1 | 0 | 0 | **(Register)** | | | 1 | 1 | 1 | (EffectiveAddress\_mode\_register) | | | | | | | | |
| L | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | (EffectiveAddress\_mode\_register) | | | | | | | | |
|  | 0 | **RegisterDI** | | | 1 | **size** | 0 | 0 | 0 | 0 | 0 | | 0 | | 0 | | RegisterDh | | |
| Page#: 240 | | | | | | | | | | | | | | | | | | | |
| **AND** | | | | | | | | | | | | | | | | | | | |
|  | 1 | 1 | 0 | 0 | **(Register)** | | | Op-Mode | | | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 119 | | | | | | | | | | | | | | | | | | | |
| **LSL, LSR** | | | | | | | | | | | | | | | | | | | |
| Reg | 1 | 1 | 1 | 0 | **(Reg\_Count)** | | | **(dr)** | (Size) | | **(i/r)** | 0 | | 1 | | **(Register)** | | | |
| Mem | 1 | 1 | 1 | 0 | 0 | 0 | 1 | **(dr)** | 1 | 1 | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 218 | | | | | | | | | | | | | | | | | | | |
| **ASL, ASR** | | | | | | | | | | | | | | | | | | | |
| Reg | 1 | 1 | 1 | 0 | **(Reg\_Count)** | | | **(dr)** | (Size) | | **(i/r)** | 0 | | 0 | | **(Register)** | | | |
| Mem | 1 | 1 | 1 | 0 | 0 | 0 | 0 | **(dr)** | 1 | 1 | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 126 | | | | | | | | | | | | | | | | | | | |
| **ROL, ROR** | | | | | | | | | | | | | | | | | | | |
| Reg | 1 | 1 | 1 | 0 | **(Reg\_Count)** | | | **(dr)** | (Size) | | **(i/r)** | 1 | | 1 | | **(Register)** | | | |
| Mem | 1 | 1 | 1 | 0 | 0 | 1 | 1 | **(dr)** | 1 | 1 | (EffectiveAddress\_mode\_register) | | | | | | | | |
| Page#: 265 | | | | | | | | | | | | | | | | | | | |