



# SACRAMENTO STATE

EEE 234

## **PROJECT 2**

**DESIGN, SIMULATION AND LAYOUT OF AN ALU**

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**SEMESTER: FALL 2018**

PROJECT PARTNERS:

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- 2) DHWANIT JUNEJA

DATE OF SUBMISSION: DECEMBER 07, 2018

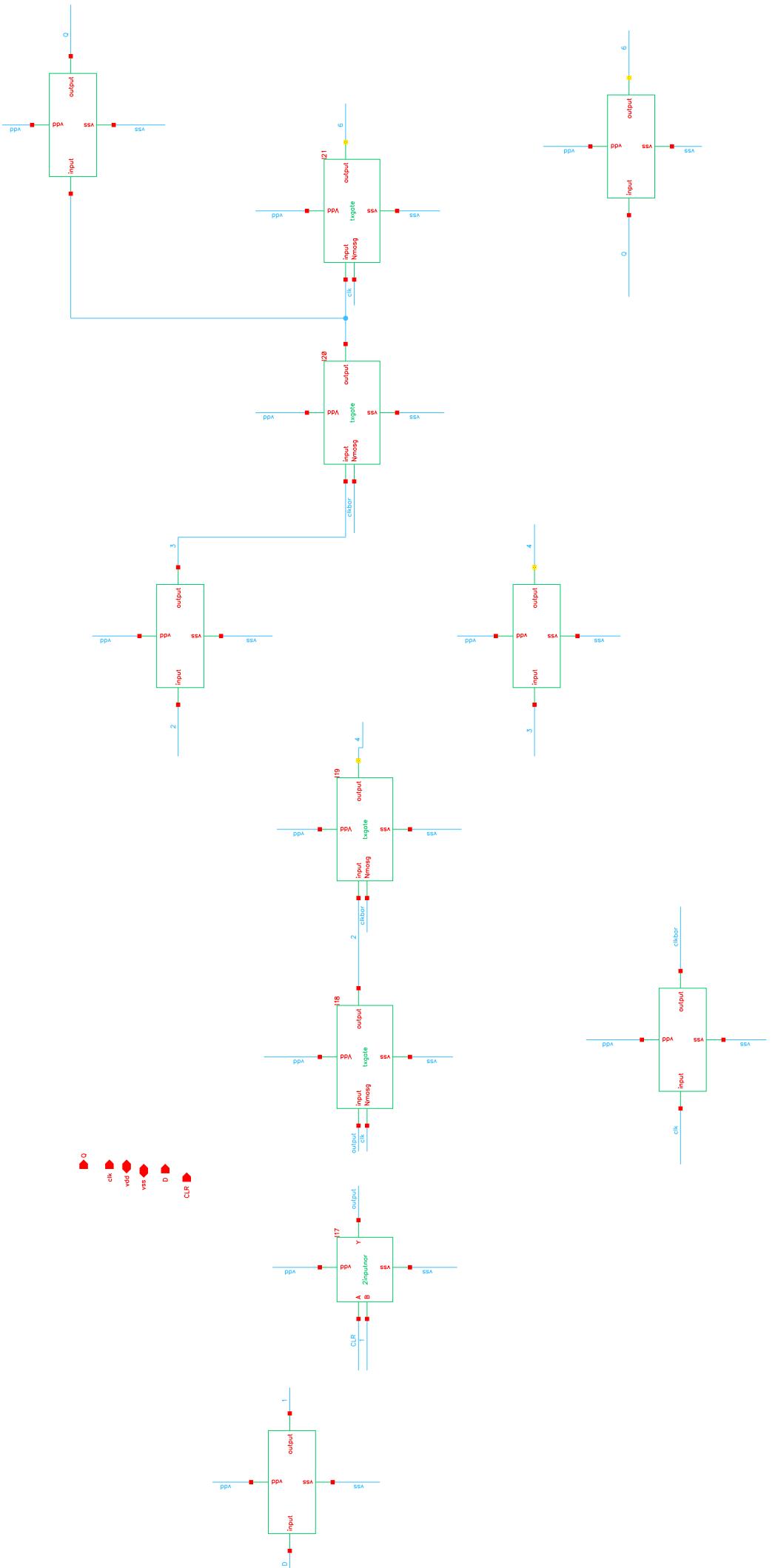
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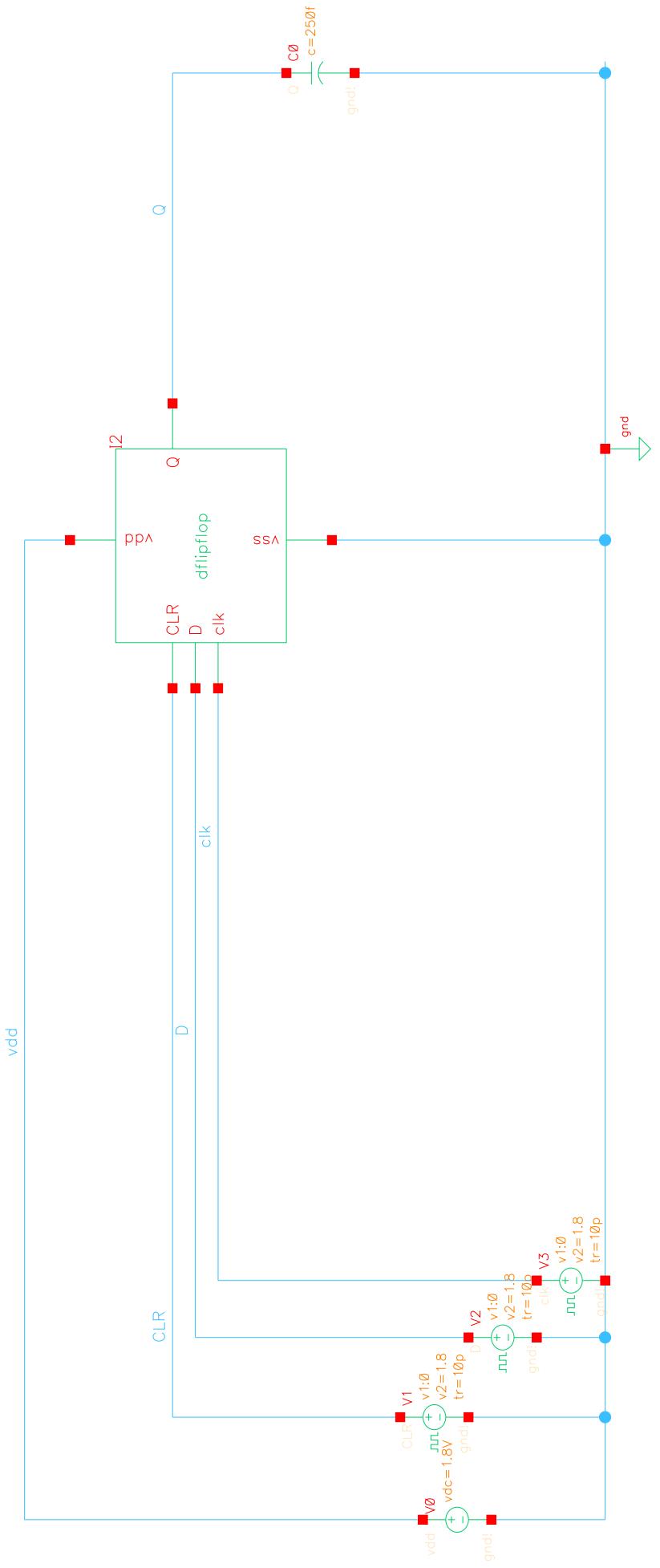
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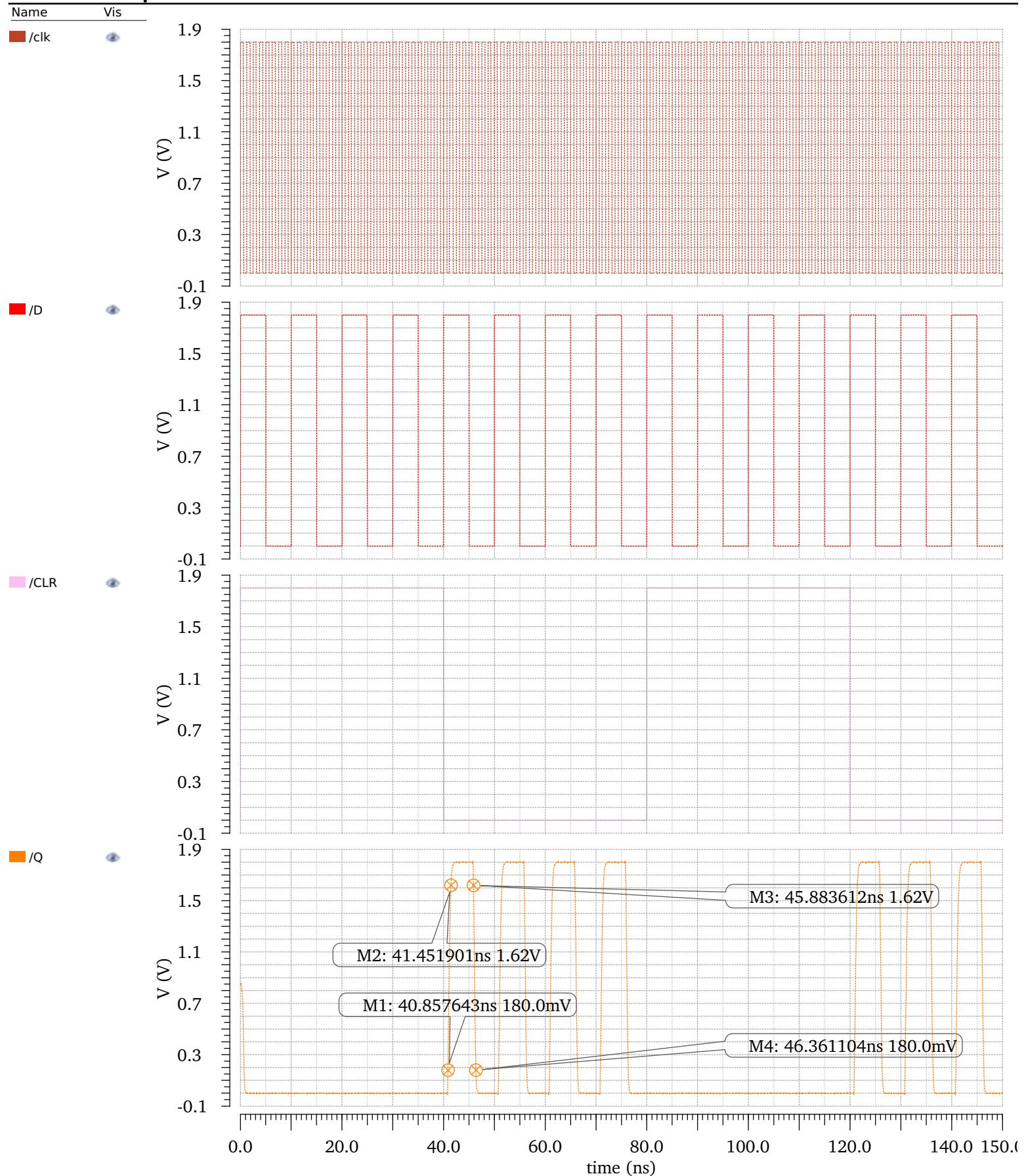
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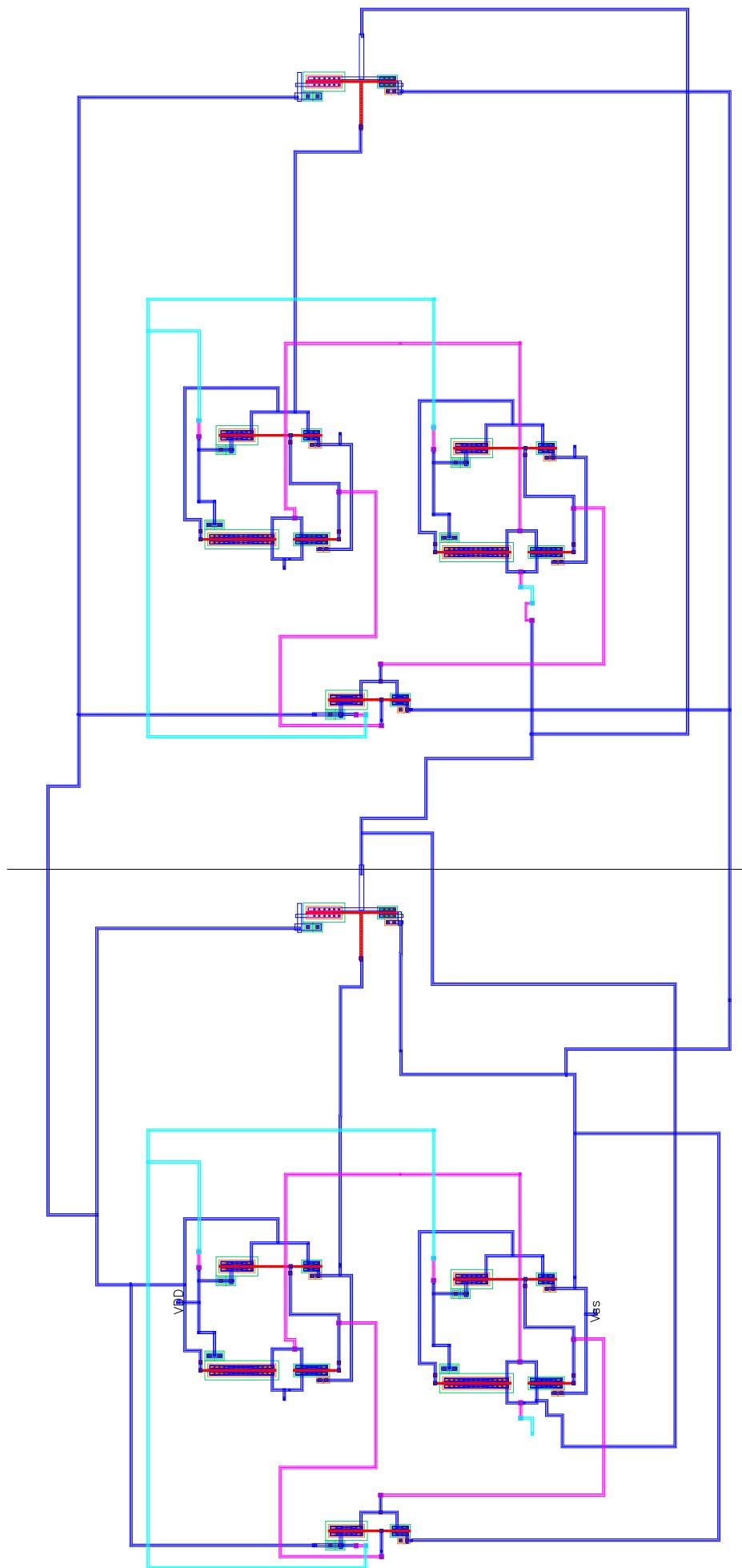
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## **D FLIP FLOP**





**Transient Response****Tue Dec 4 14:51:48 2018**



File Tools Options Help

```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "Dff_layout layout" *****
Total errors found: 0
```

```
mouse L: showClickInfo()
M: setDRCForm()
R: _JxHiMousePopUp()
```

1 | >

```
@(#)$CDS: LVS version 6.1.7-64b 12/07/2018 19:41 (sjfhw305) $
```

```
Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/junejad/EEE234/project3/LVS -l -s -t  
/gaia/class/student/junejad/EEE234/project3/LVS/layout  
/gaia/class/student/junejad/EEE234/project3/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.
```

```
Net-list summary for /gaia/class/student/junejad/EEE234/project3/LVS/layout/netlist  
count  
24 nets  
0 terminals  
13 pmos  
13 nmos
```

```
Net-list summary for /gaia/class/student/junejad/EEE234/project3/LVS/schematic/netlist  
count  
16 nets  
6 terminals  
13 pmos  
13 nmos
```

```
Devices in the netlist but not in the rules:  
pmos nmos
```

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	26	26
total	26	26

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	24	16
total	24	16

	terminals	
un-matched	0	0
matched but different type	0	0
total	0	6

Probe files from /gaia/class/student/junejad/EEE234/project3/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

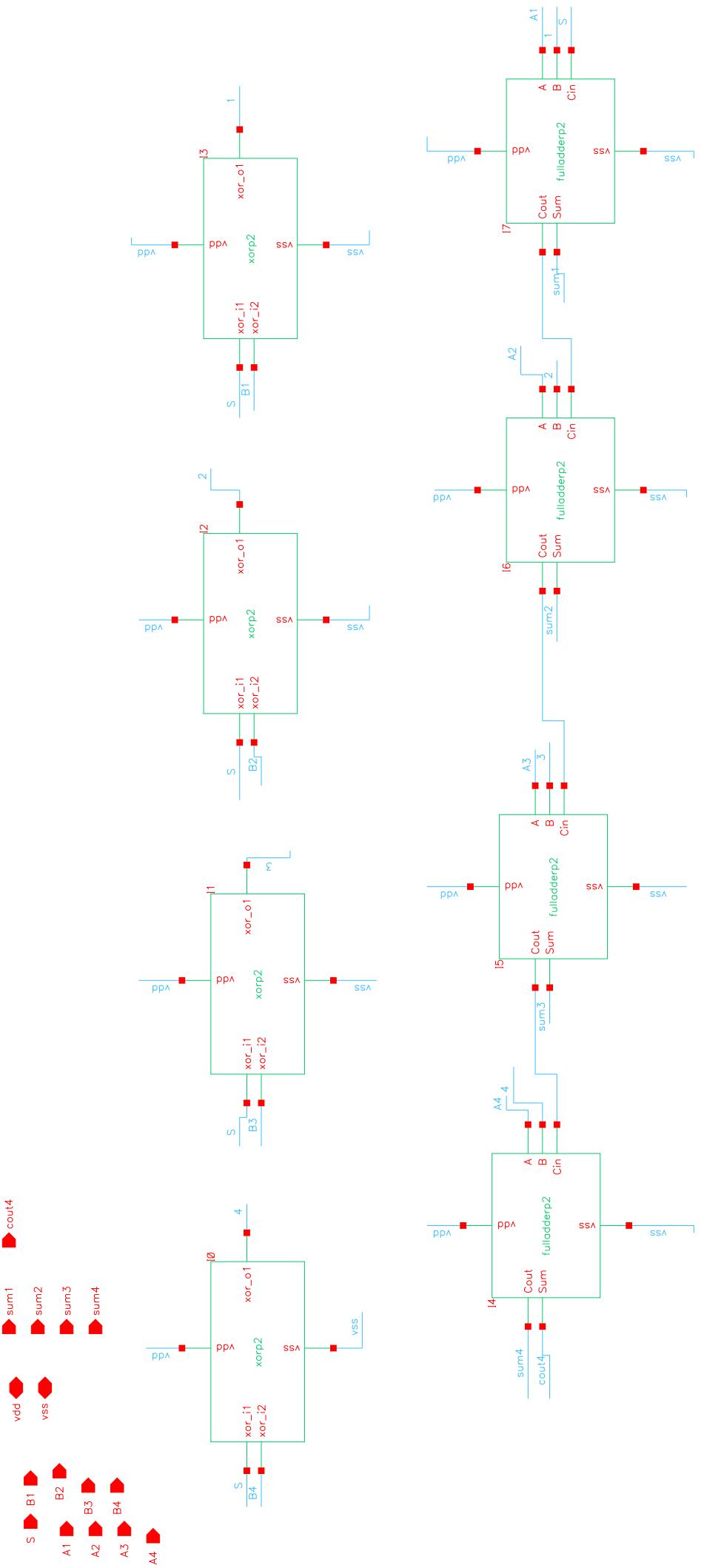
termbad.out:  
Page8

prunenet.out:  
prunedev.out:  
audit.out:  
Probe files from /gaia/class/student/junejad/EEE234/project3/LVS/layout  
devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:

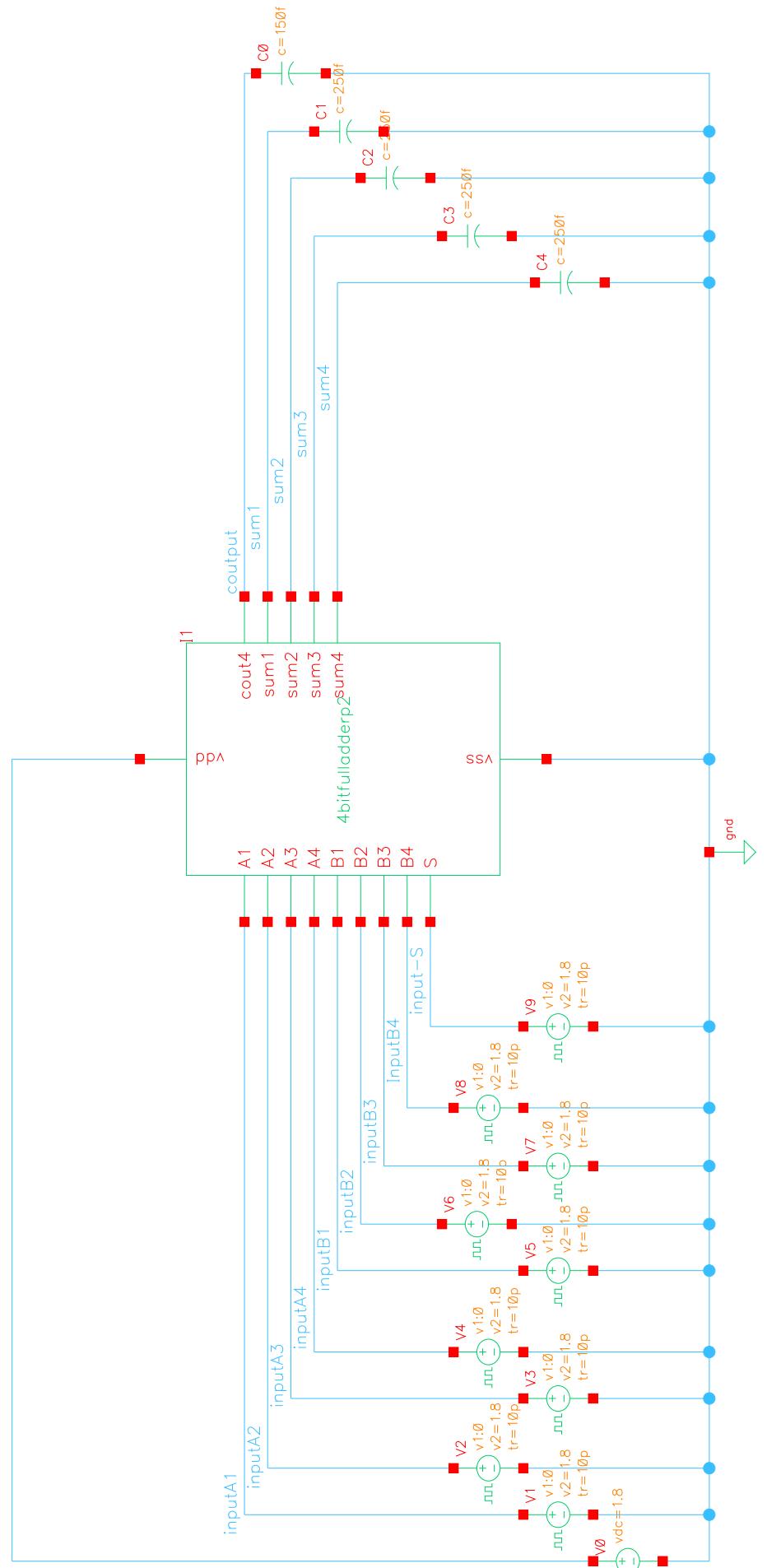
# **4 BIT FULL**

# **ADDER**

# SCHEMATIC



## TEST BENCH SCHEMATIC



## SYMBOL

[@instanceName]

cout4

sum1

sum2

sum3

sum4

[@partName]

A1

A2

A3

A4

B1

B2

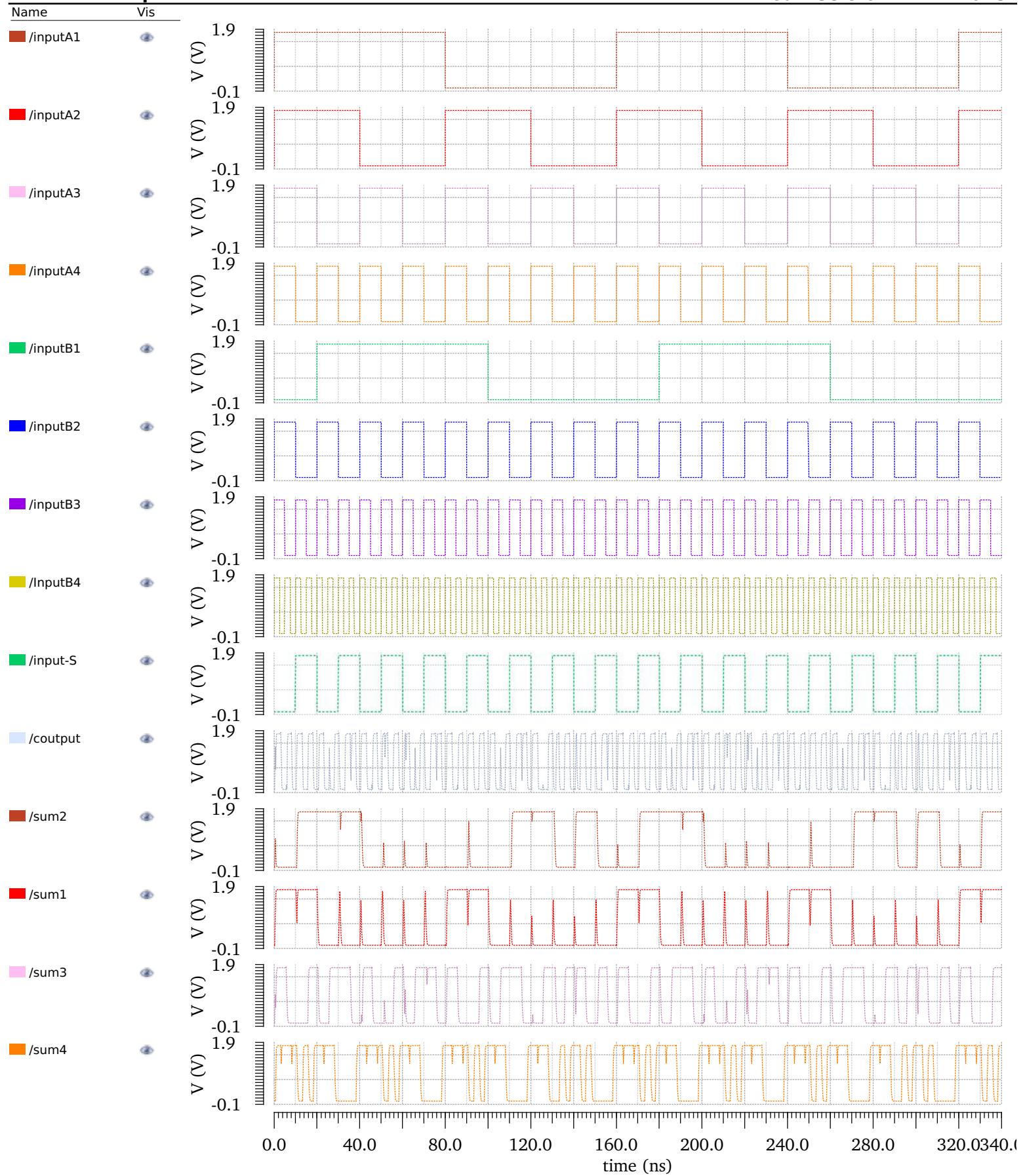
B3

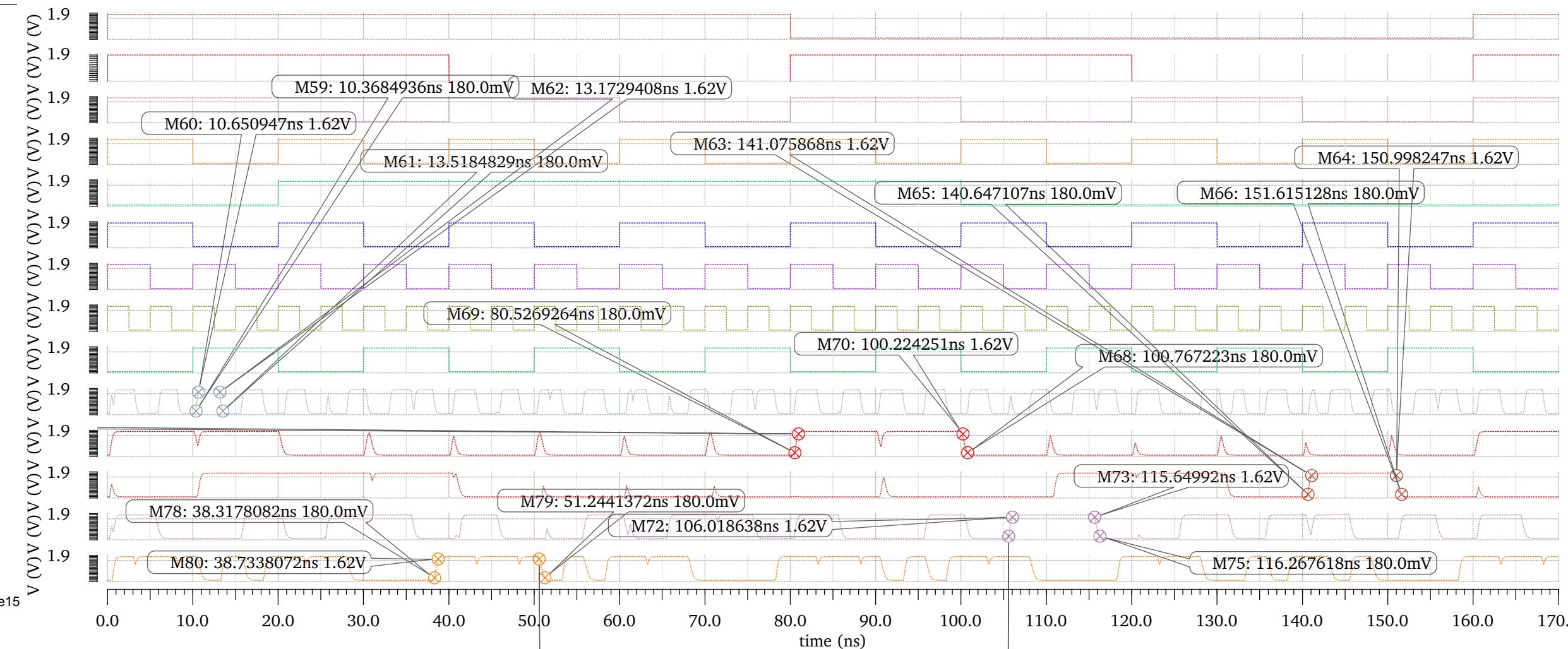
B4

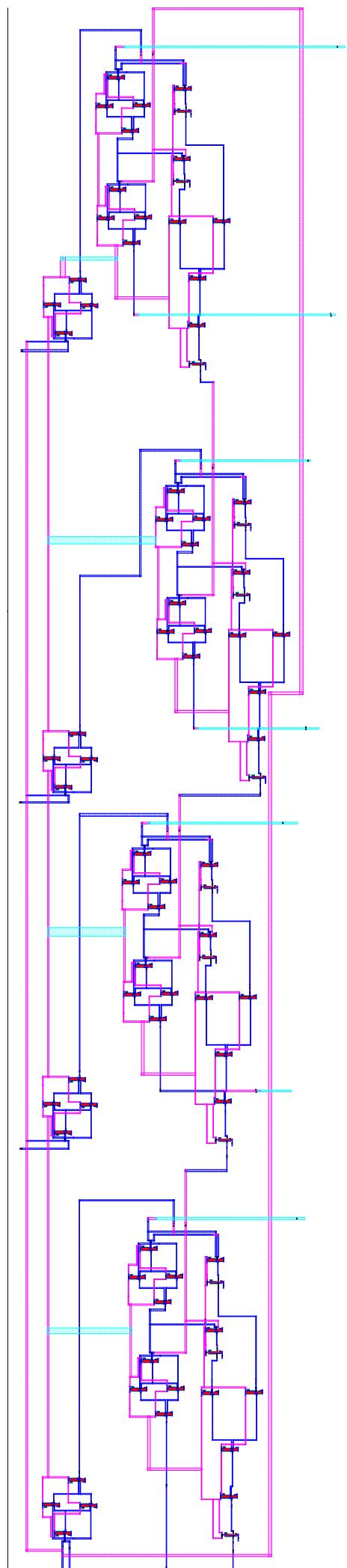
S

ppv

vss

**Transient Response****Wed Dec 5 04:24:27 2018**





File Tools Options Help

```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "4bitfulladder_layout layout" *****
Total errors found: 0
```

mouse L: showClickInfo()

M: setDRCForm()

R: \_JxHiMousePopUp()

1 | >

```
@(#)$CDS: LVS version 6.1.7-64b 12/07/2018 19:41 (sjfhw305) $
```

Command line:

```
/software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -  
dir /gaia/class/student/junejad/demo/LVS -l -s -t  
/gaia/class/student/junejad/demo/LVS/layout  
/gaia/class/student/junejad/demo/LVS/schematic
```

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

```
Net-list summary for  
/gaia/class/student/junejad/demo/LVS/layout/netlist  
count  
167 nets  
0 terminals  
156 pmos  
156 nmos
```

```
Net-list summary for  
/gaia/class/student/junejad/demo/LVS/schematic/  
netlistcount  
167 nets  
16 terminals  
156 pmos  
156 nmos
```

Devices in the rules but not in the netlist:

```
cap nfet pfet nmos4 pmos4
```

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	312	312
total	312	312

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	167	167
total	167	167

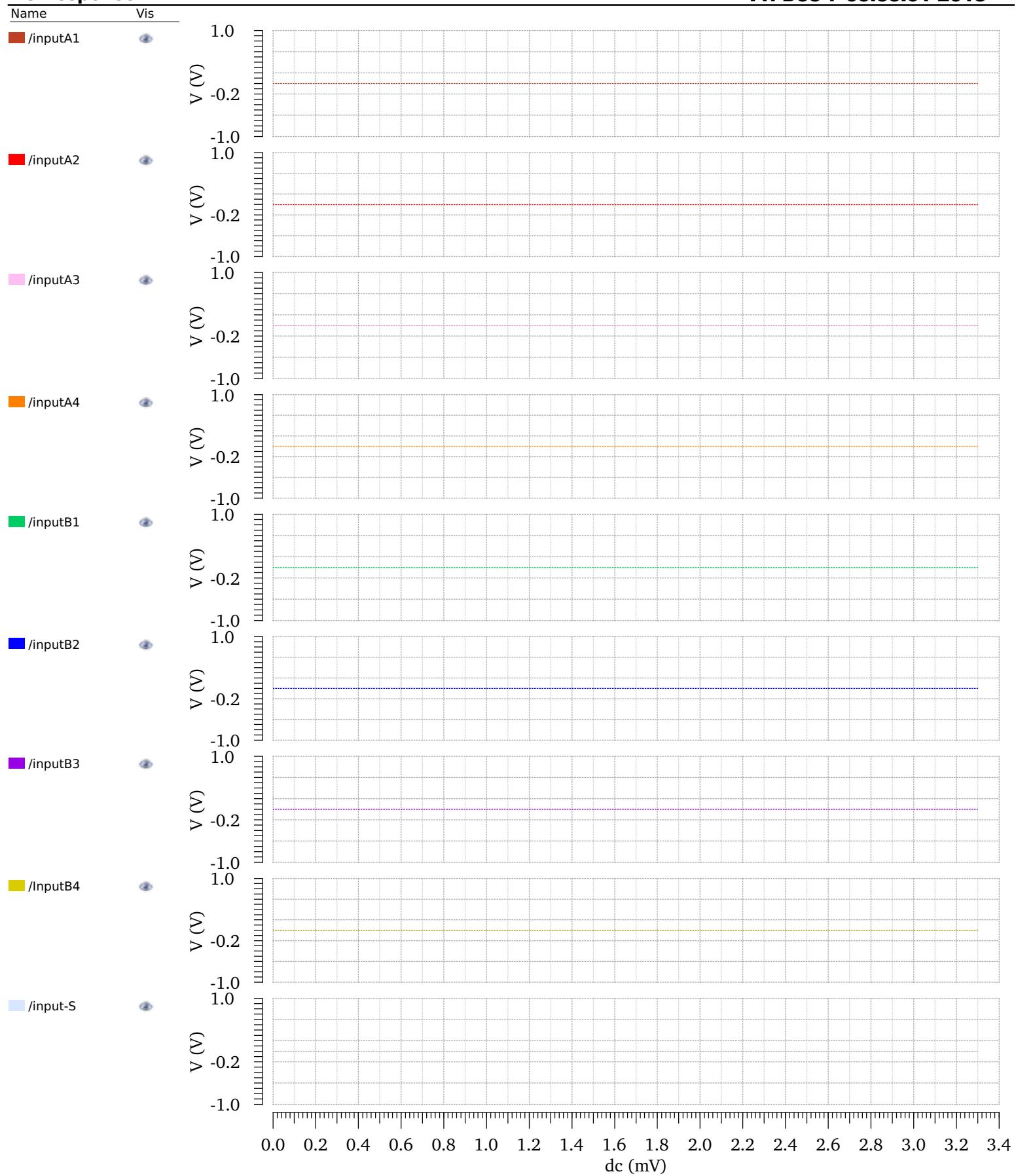
  

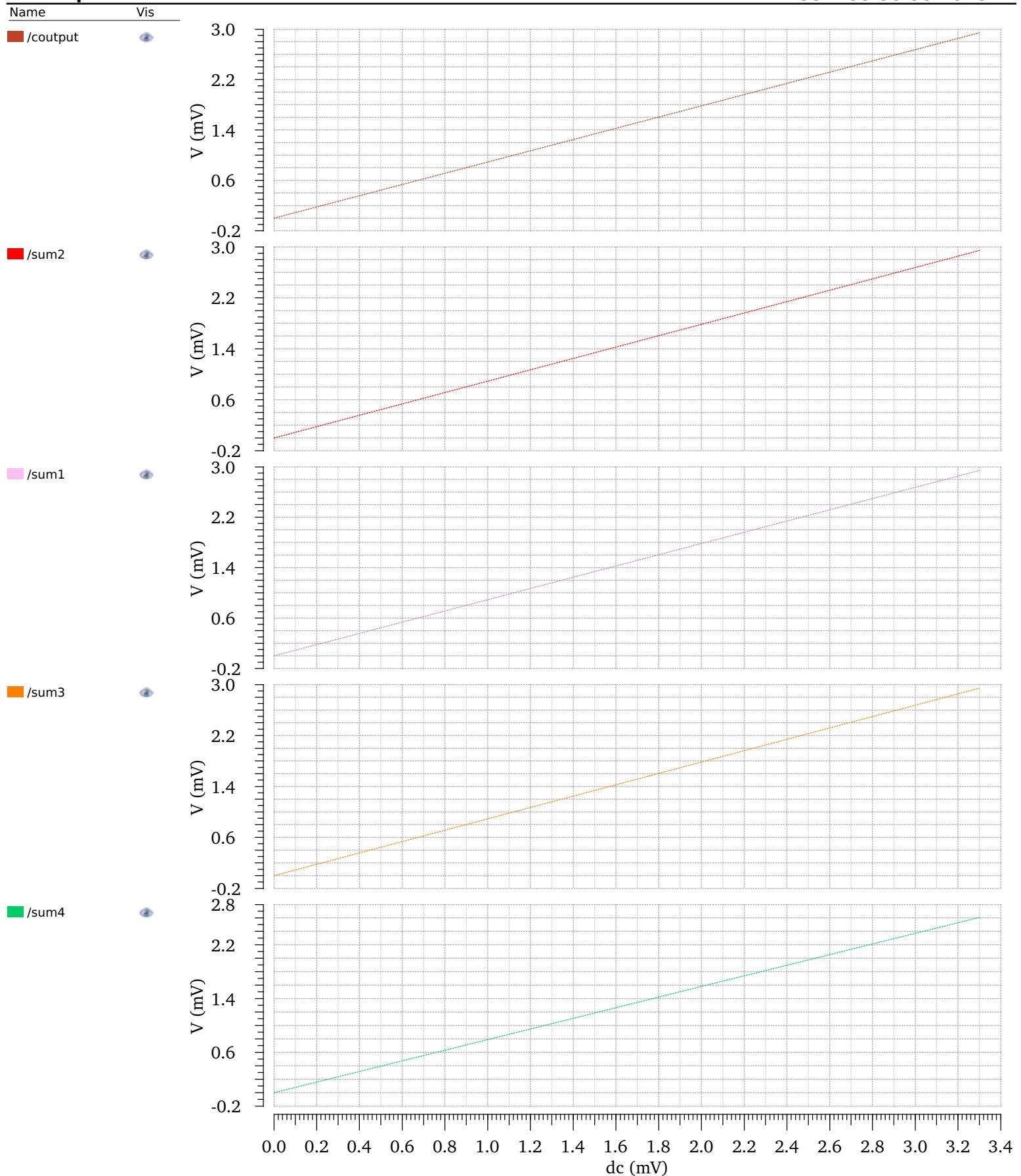
	terminals	
un-matched	0	0
matched but different type	0	0
total	0	16

Probe files from /gaia/class/student/junejad/demo/LVS/

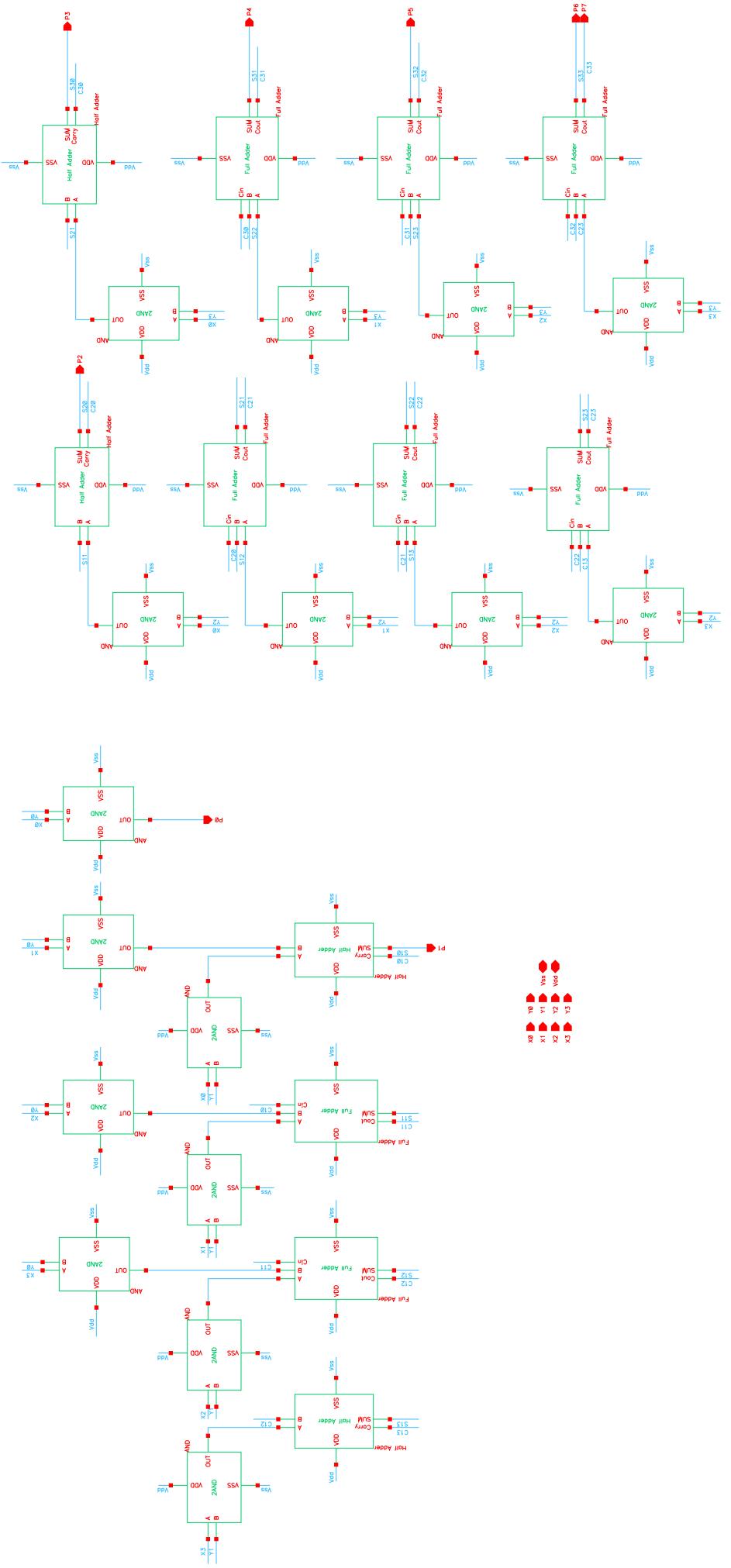
schematic devbad.out:

```
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:  
  
Probe files from /gaia/class/student/junejad/demo/LVS/  
layout devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:
```

**DC Response****Fri Dec 7 05:33:01 2018**

**DC Response****Fri Dec 7 05:36:06 2018**

( '6+H )  
A I @H=D@-9F



# SYMBOL

[@instanceName]

P $\emptyset$  P $1$  P $2$  P $3$  P $4$  P $5$  P $6$  P $7$

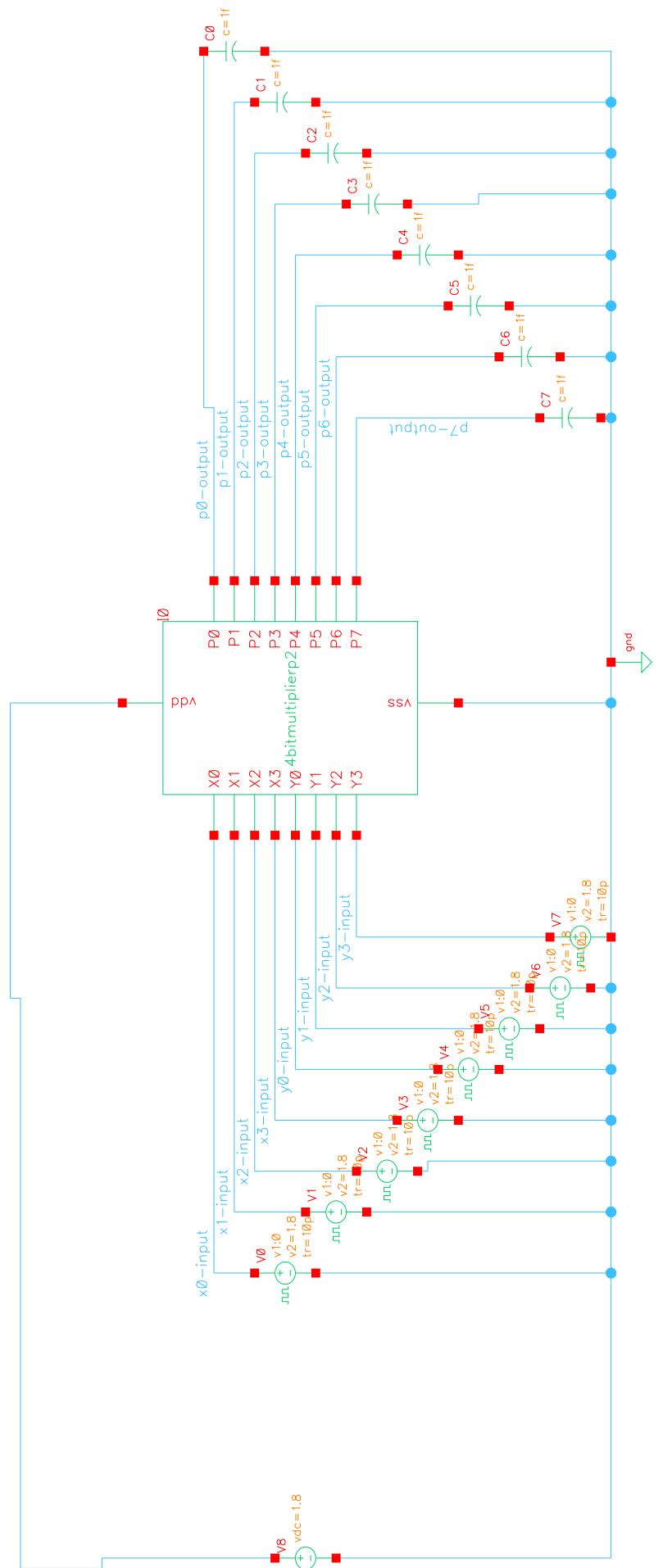
ppl

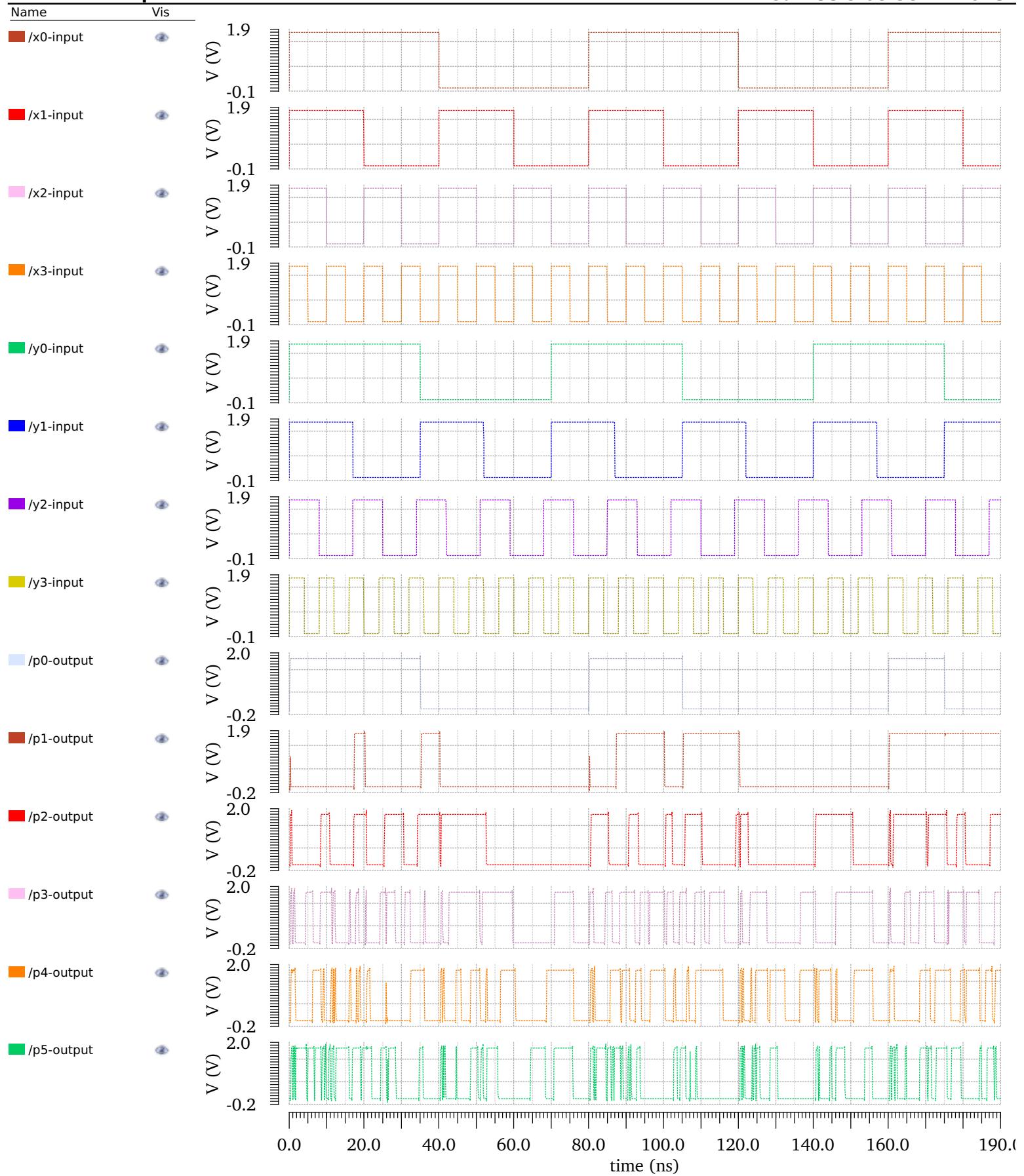
SSA

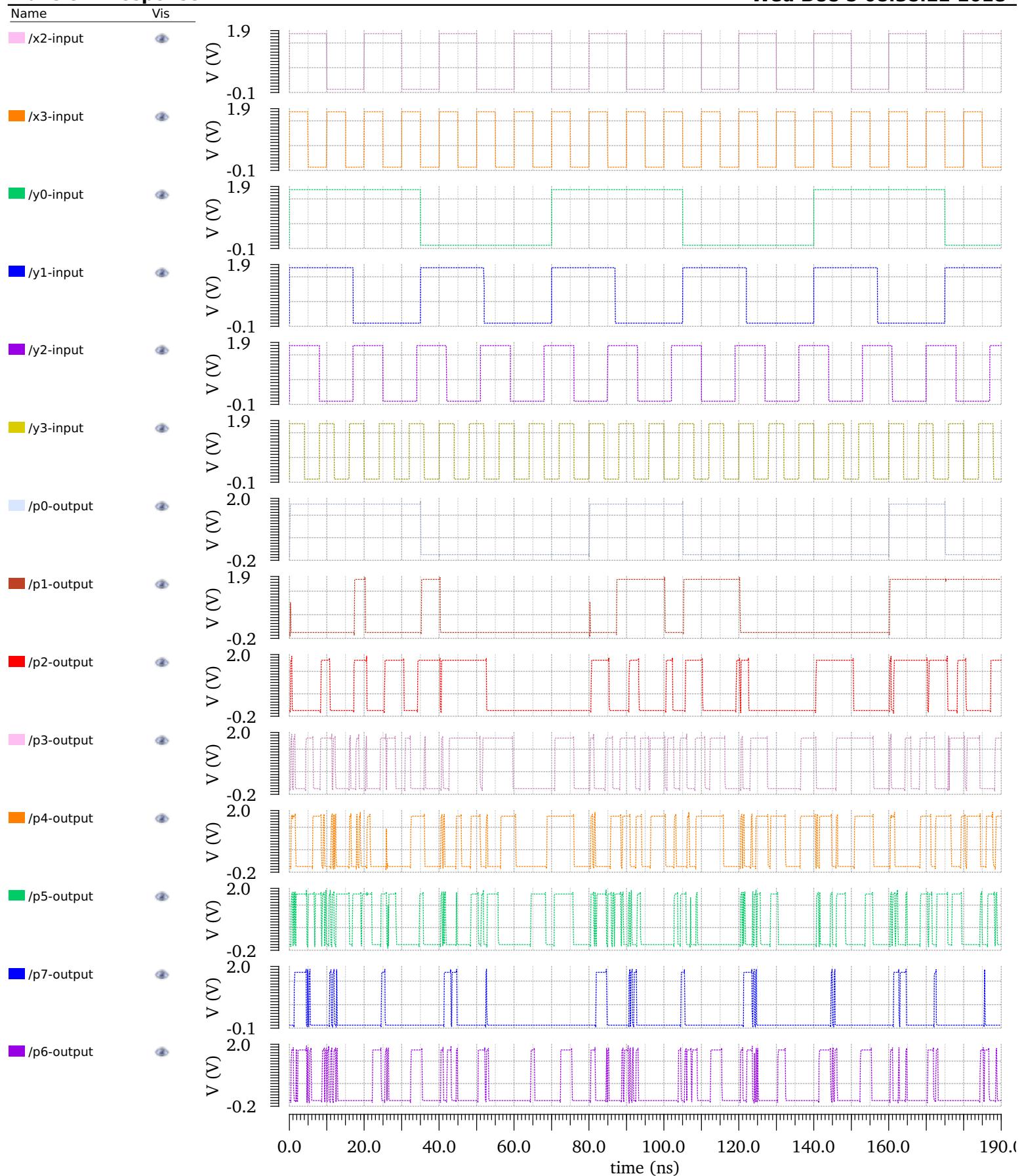
[@partName]

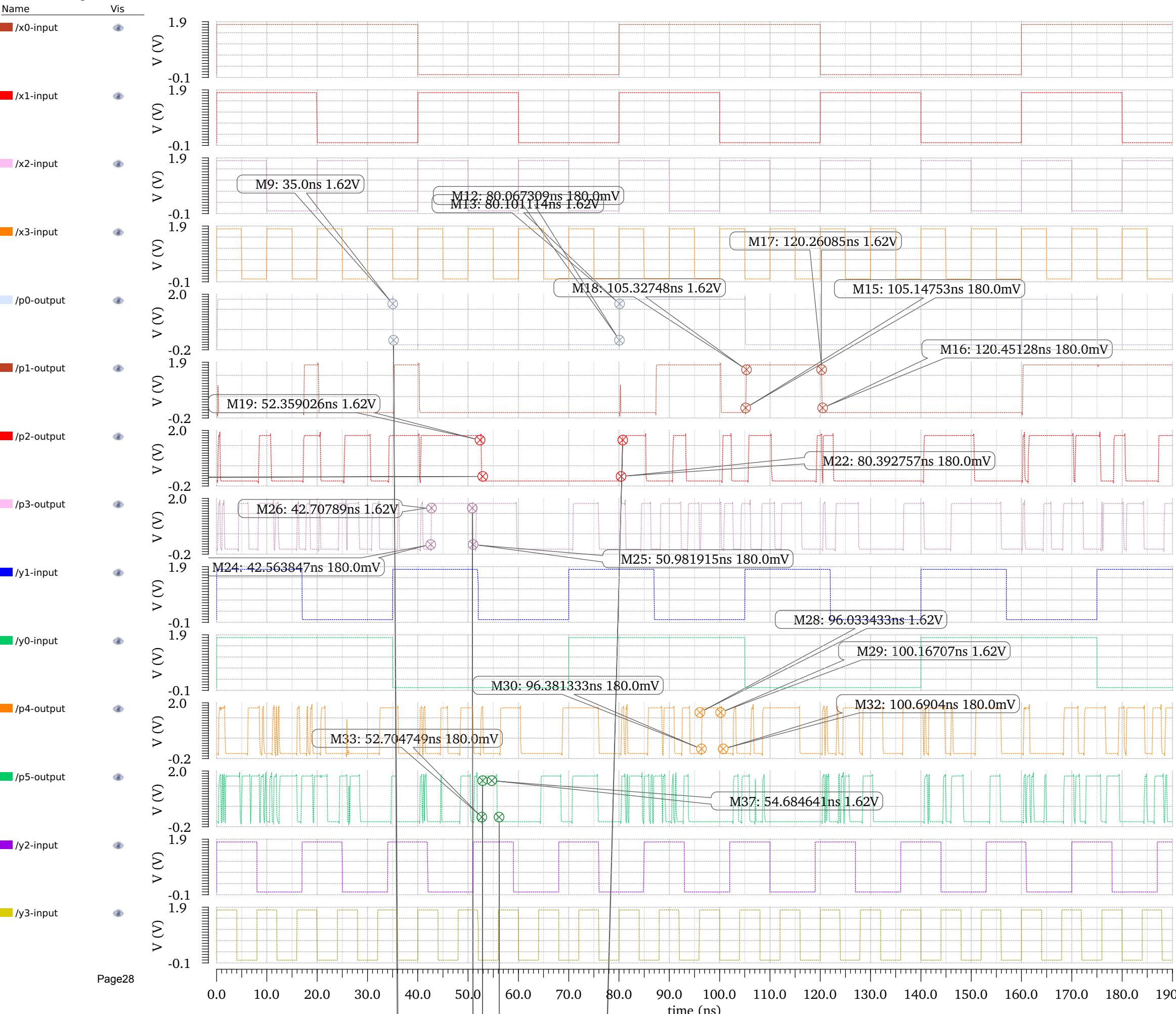
X $\emptyset$  X $1$  X $2$  X $3$  Y $\emptyset$  Y $1$  Y $2$  Y $3$

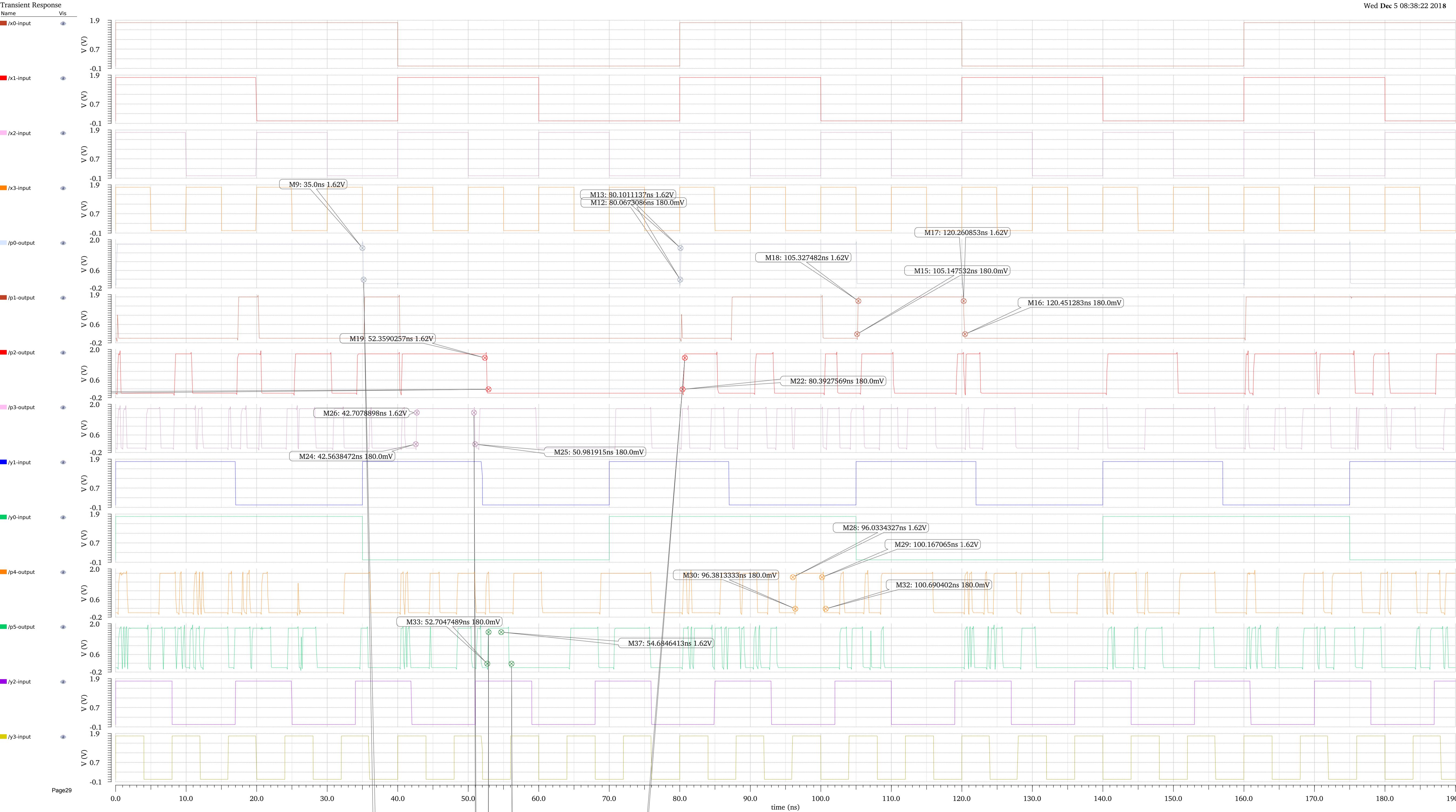
# TEST BENCH SCHEMATIC

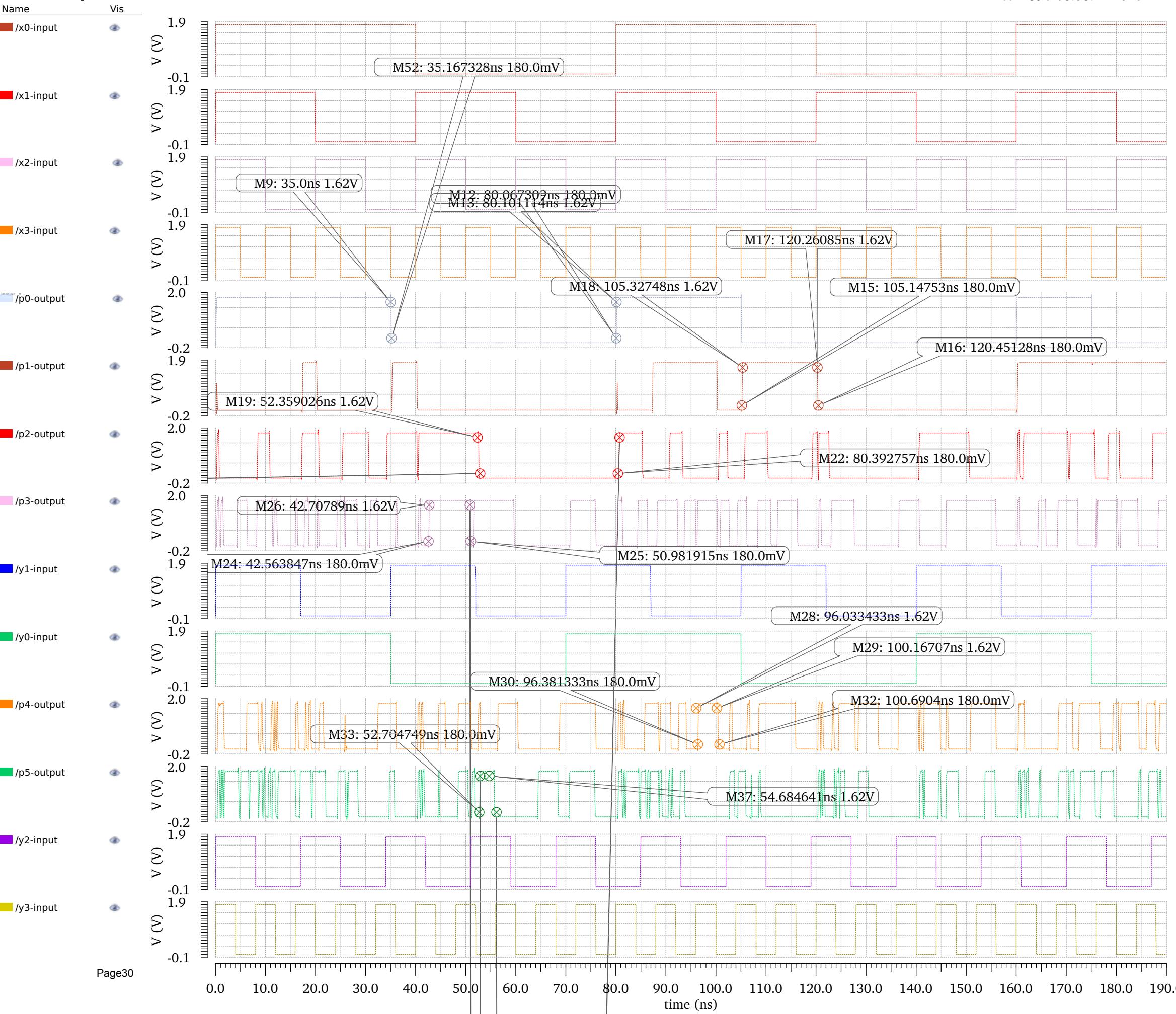


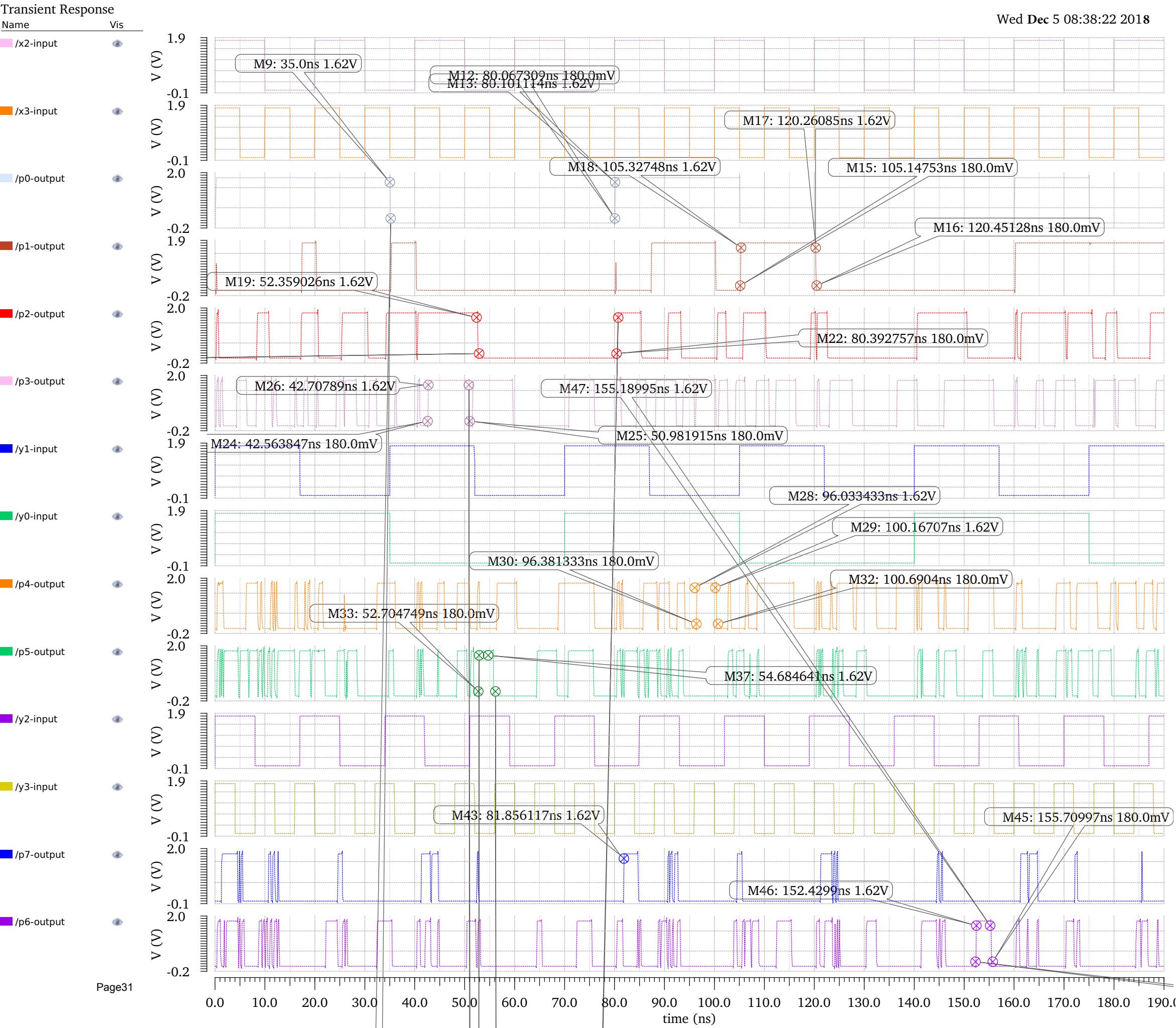
**Transient Response****Wed Dec 5 08:38:22 2018**

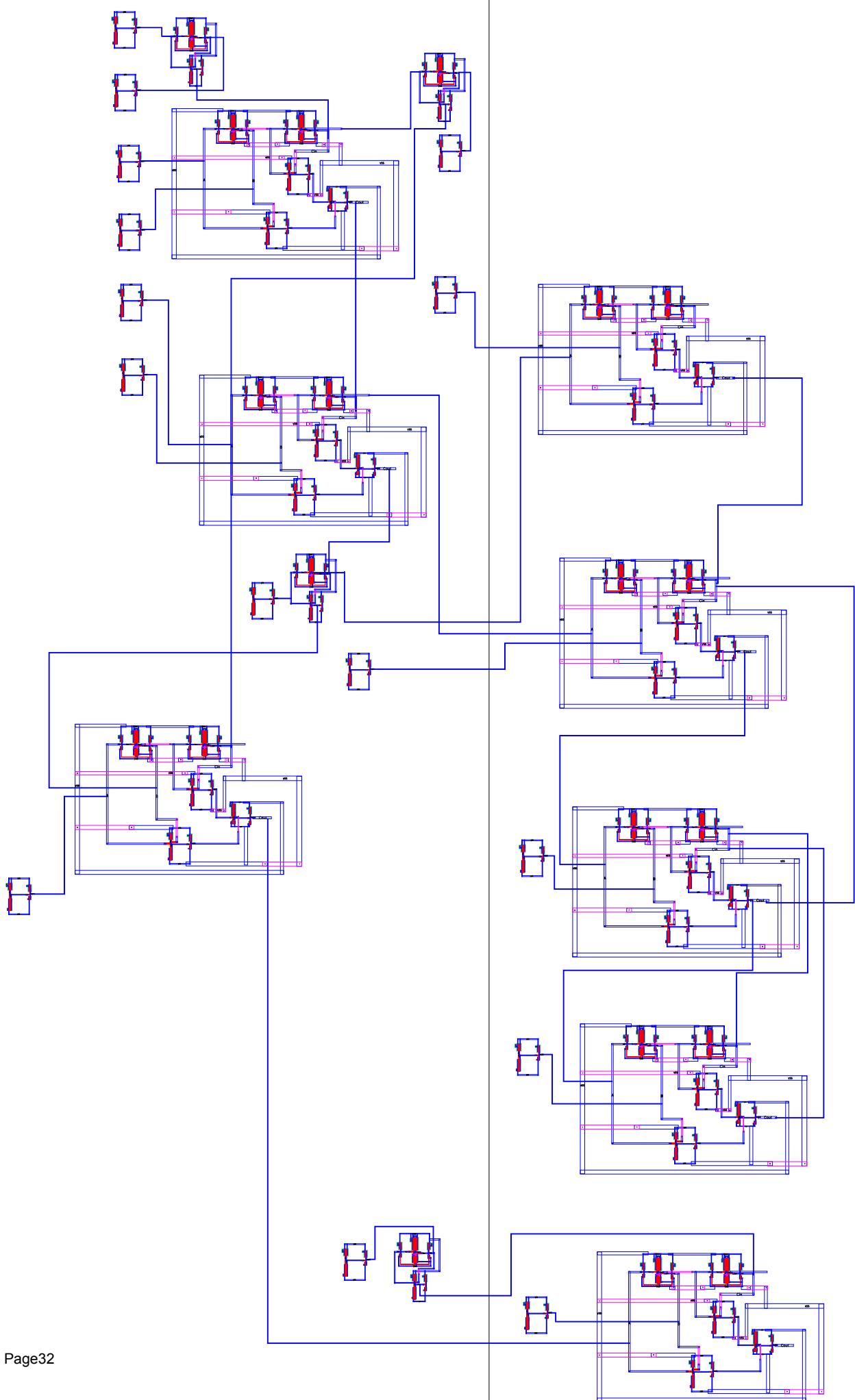
**Transient Response****Wed Dec 5 08:38:22 2018**











File Tools Options Help

```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "4bitMultiplier_L layout" *****
Total errors found: 0
```

mouse L: showClickInfo()

M: setDRCForm()

R: \_IxHiMousePopUp()

1 | >

Command line:  
 /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -  
 dir /gaia/class/student/junejad/demo/LVS -l -s -t  
 /gaia/class/student/junejad/demo/LVS/layout  
 /gaia/class/student/junejad/demo/LVS/schematic  
 Like matching is enabled.  
 Net swapping is enabled.  
 Using terminal names as correspondence points.  
 Compiling Diva LVS rules...

Net-list summary for  
 /gaia/class/student/junejad/demo/LVS/layout/netlist

count	
350	nets
0	terminals
340	pmos
340	nmos

Net-list summary for  
 /gaia/class/student/junejad/demo/LVS/schematic/  
 netlistcount

350	nets
18	terminals
340	pmos
340	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

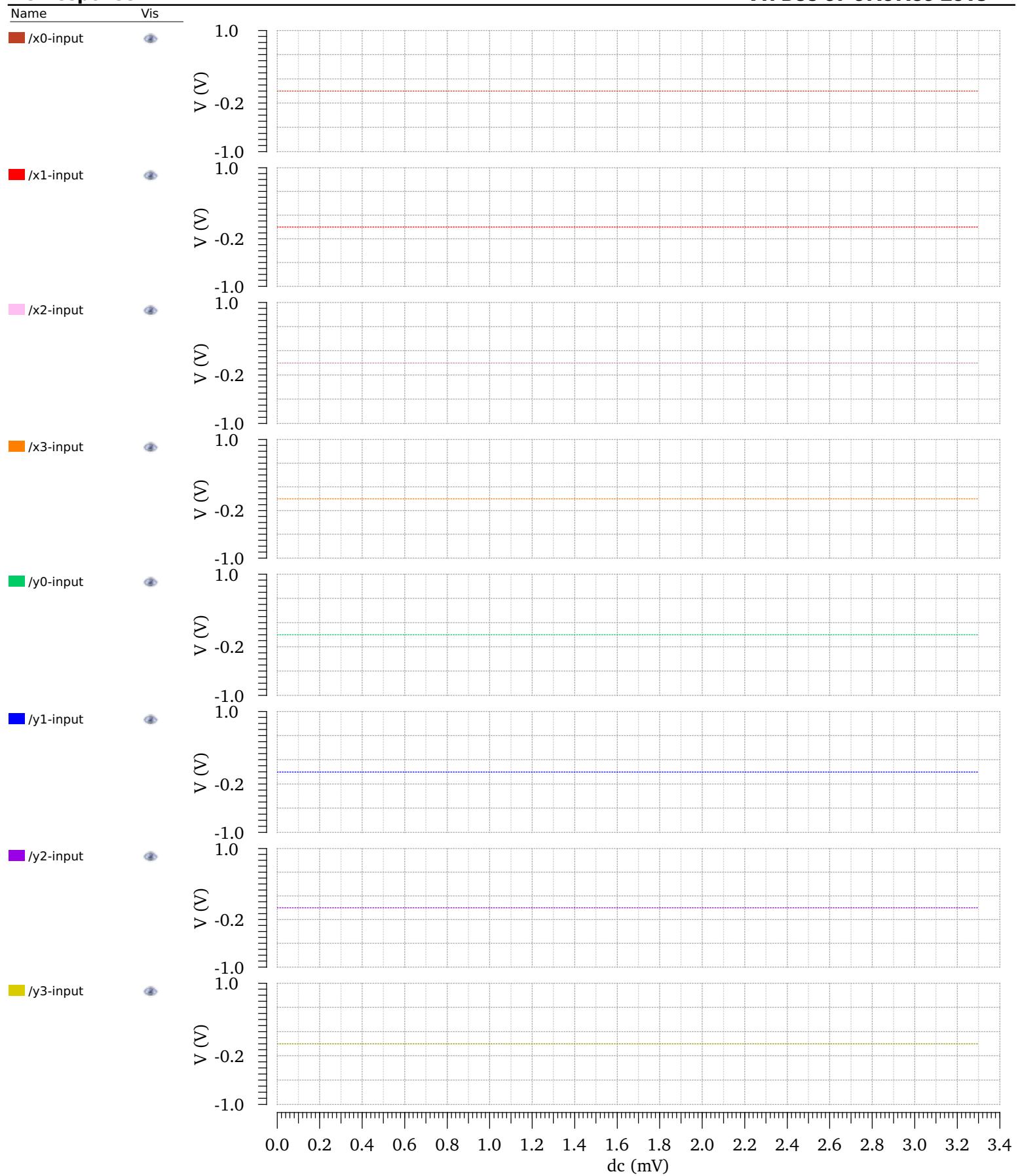
	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	680	680
total	680	680
nets		
un-matched	0	0
merged	0	0
pruned	0	0
active	350	350
total	350	350
terminals		
un-matched	0	0
matched but different type	0	0
total	0	18

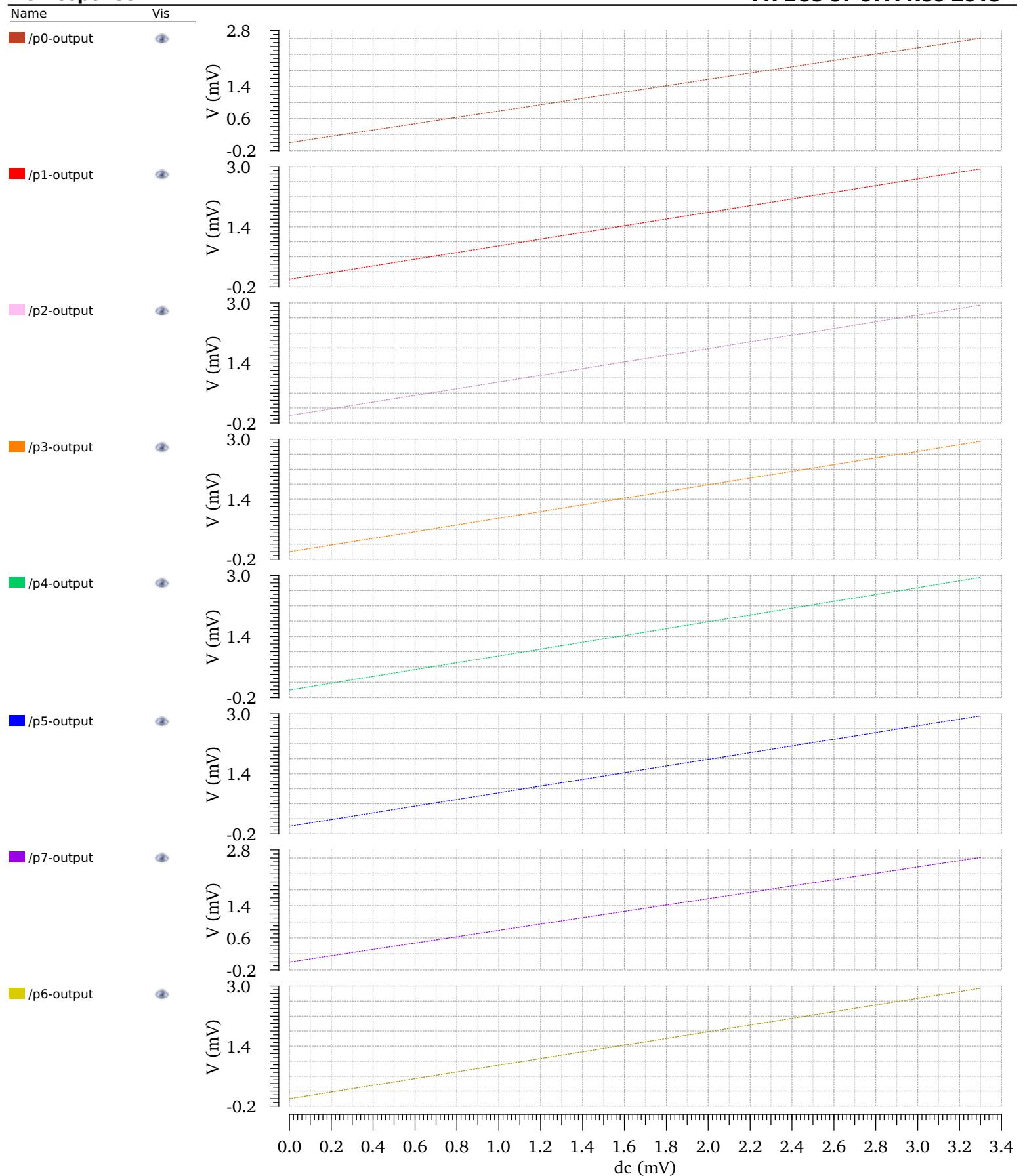
Probe files from /gaia/class/student/junejad/demo/LVS/

schematic devbad.out:

netbad.out:

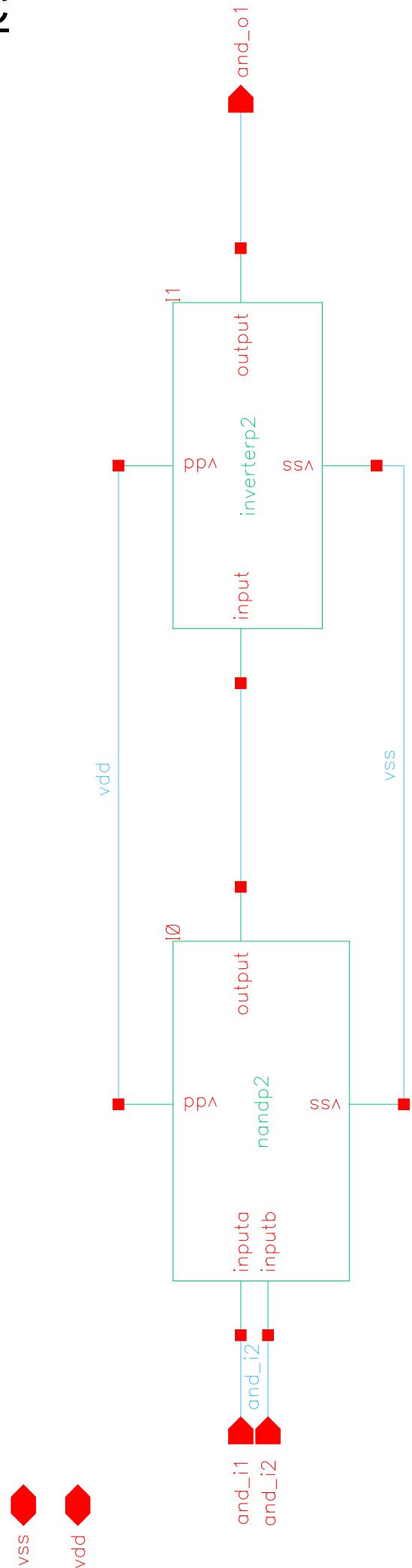
```
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:  
  
Probe files from /gaia/class/student/junejad/demo/LVS/  
layout devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:
```

**DC Response****Fri Dec 07 07:07:59 2018**

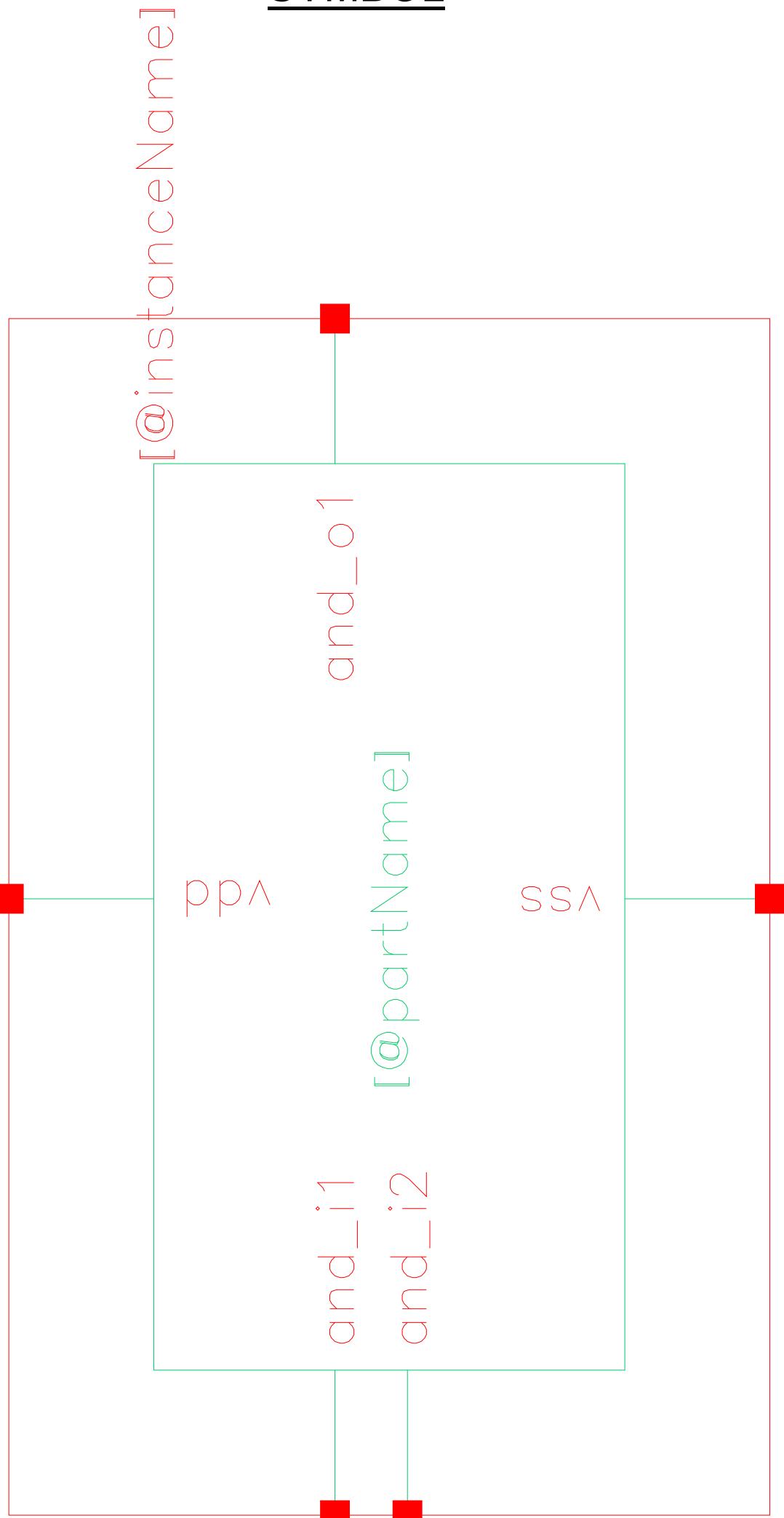
**DC Response****Fri Dec 07 07:11:59 2018**

**AND**

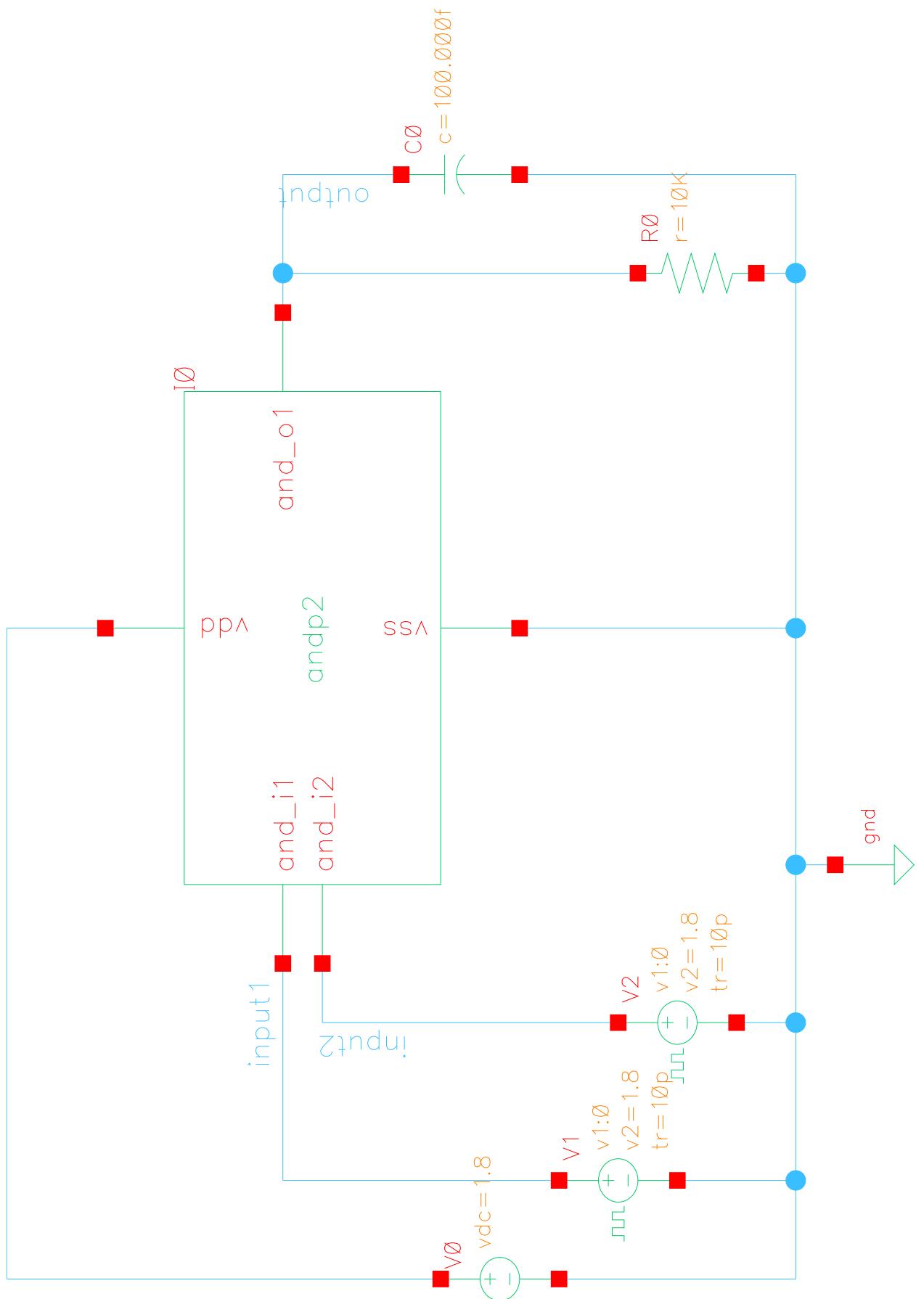
# SCHEMATIC

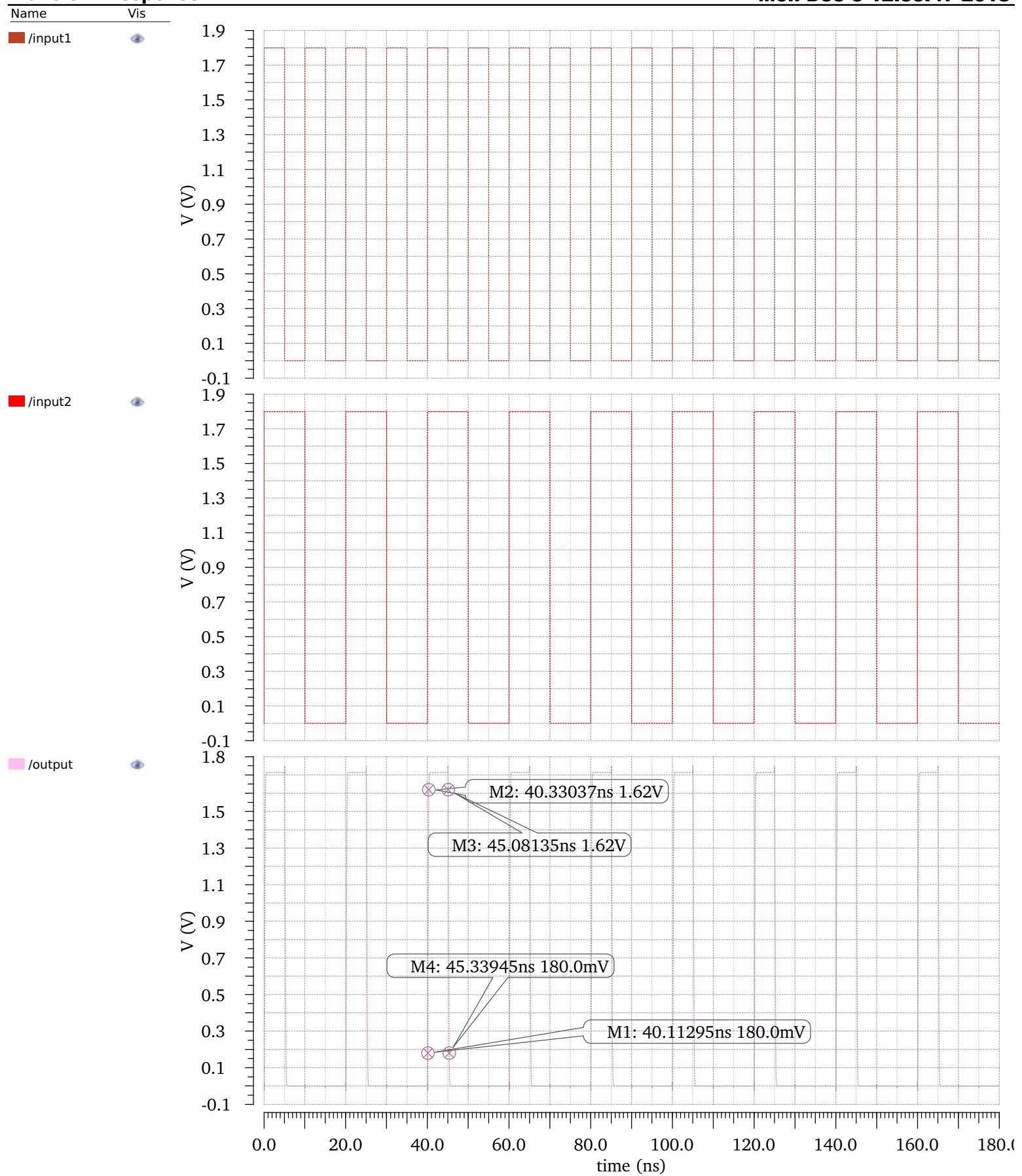


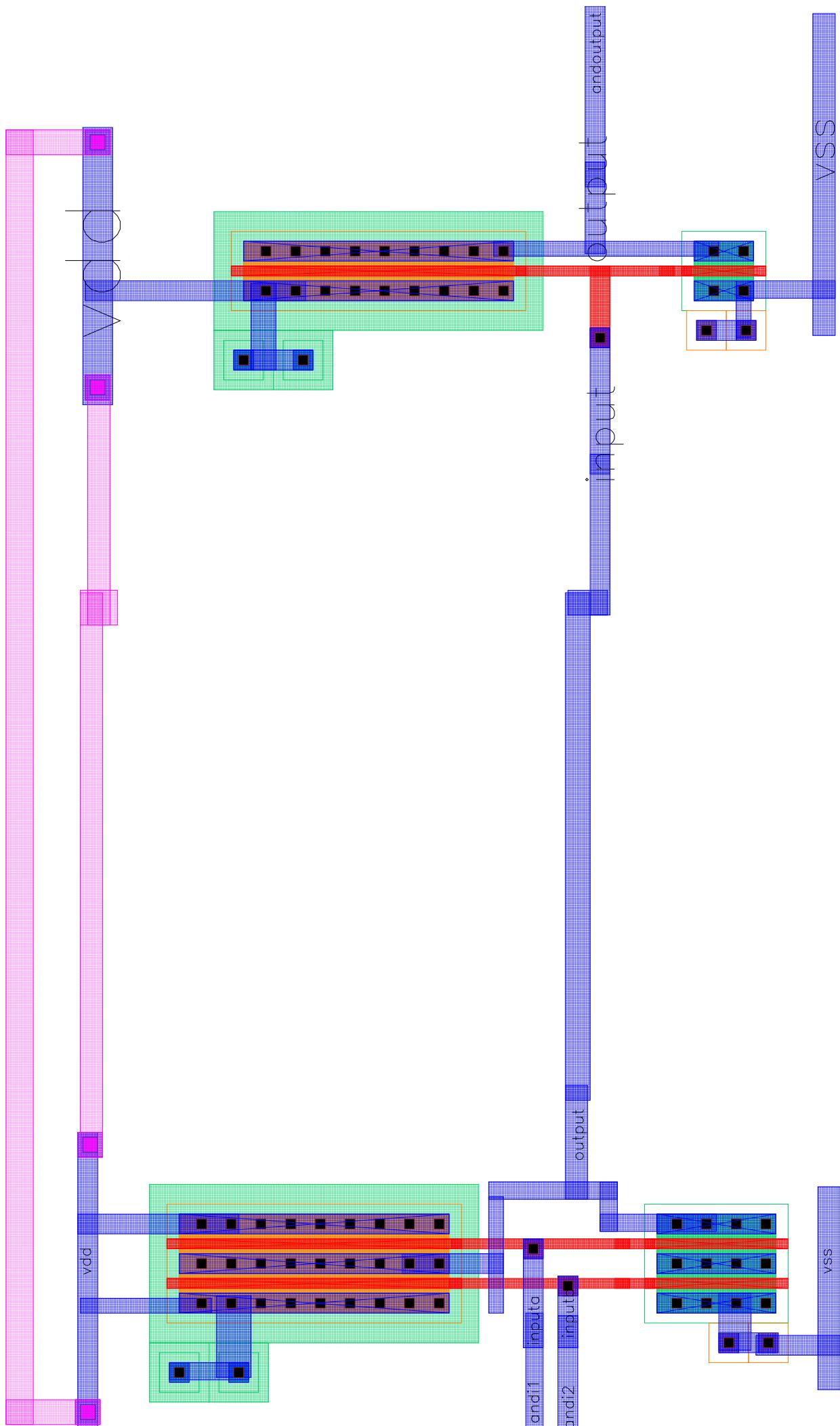
# SYMBOL



# TEST BENCH SCHEMATIC



**Transient Response****Mon Dec 3 12:35:47 2018**



Virtuoso® 6.1.7-64b - Log: /gaia/class/student/junejad/CDS.log@thea.ecs.csus.edu

File Tools Options Help

cadence

```
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "2inAND_layout layout" *****
Total errors found: 0
```

mouse L: showClickInfo() M: setDRCForm() R: \_JxHiMousePopUp()

1 >

```

                                and lvs.txt
@(#) $CDS: LVS version 6.1.7-64b 12/07/2018 19:41 (sjfhw305) $

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -
dir /gaia/class/student/junejad/demo/LVS -l -s -t
/gaia/class/student/junejad/demo/LVS/layout
/gaia/class/student/junejad/demo/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

```

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/layout/netlist
count
    7          nets
    0          terminals
    3          pmos
    3          nmos

```

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/schematic/netlist
count
    7          nets
    5          terminals
    3          pmos
    3          nmos

```

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	6	6
total	6	6
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	7	7
total	7	7

	and lvs.txt	
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	0	5

Probe files from /gaia/class/student/junejad/demo/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/junejad/demo/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

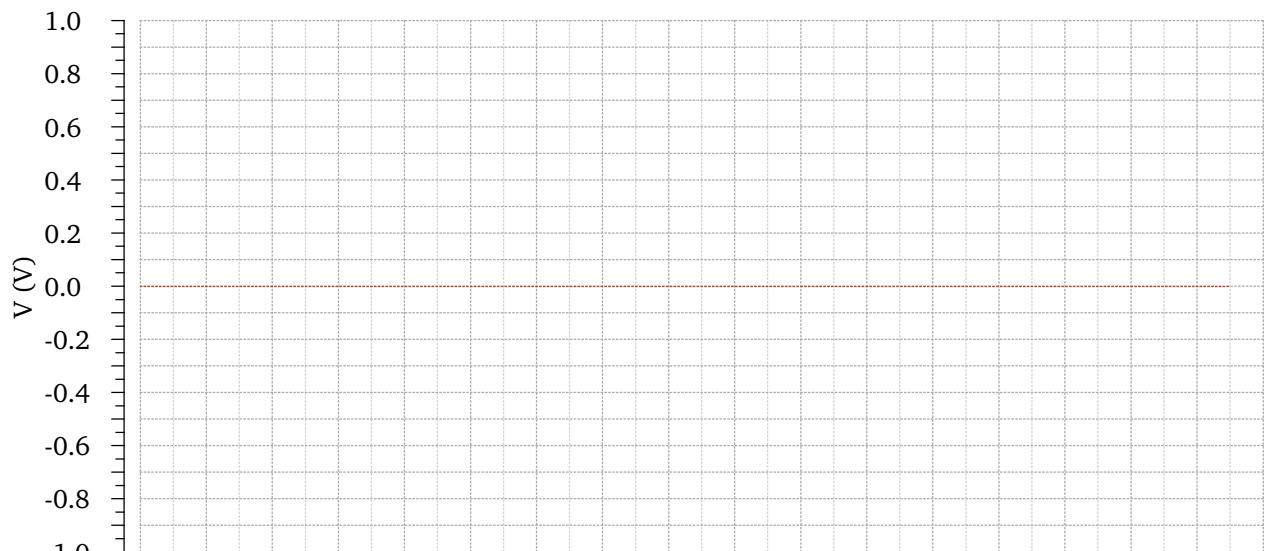
prunedev.out:

audit.out:

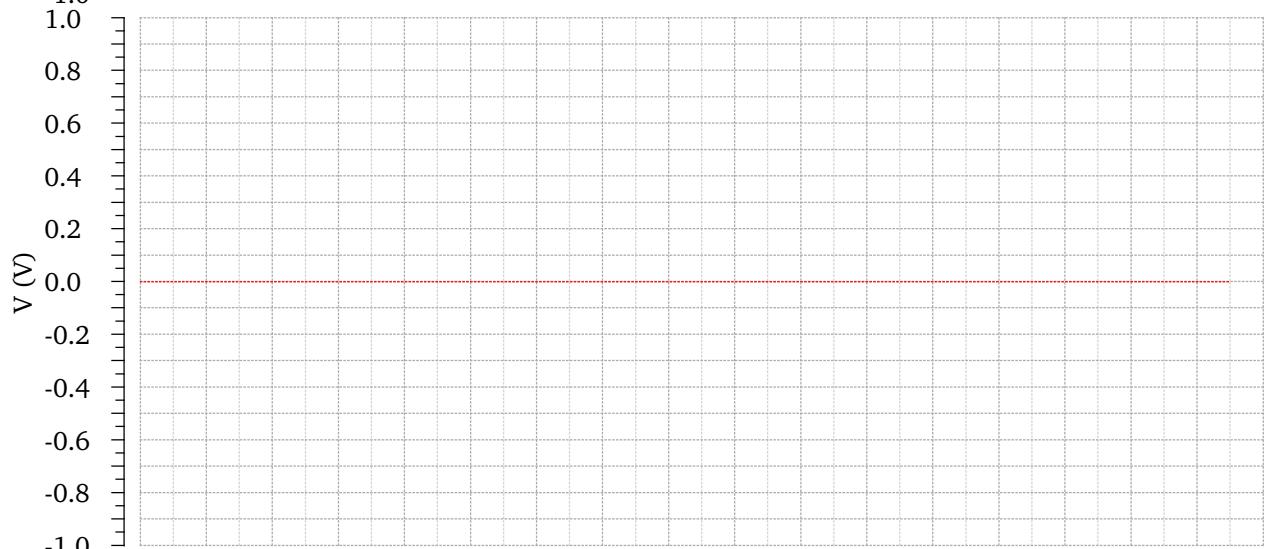
**DC Response****Fri Dec 07 05:19:35 2018**

Name Vis

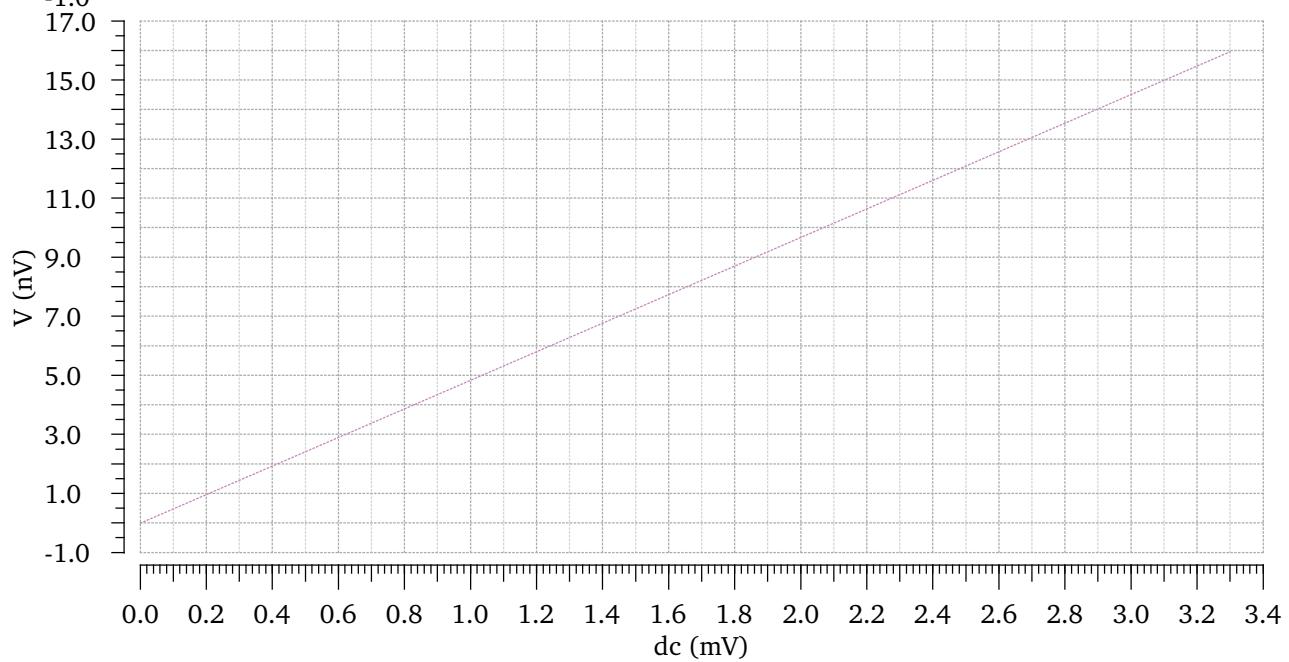
■ /input1



■ /input2



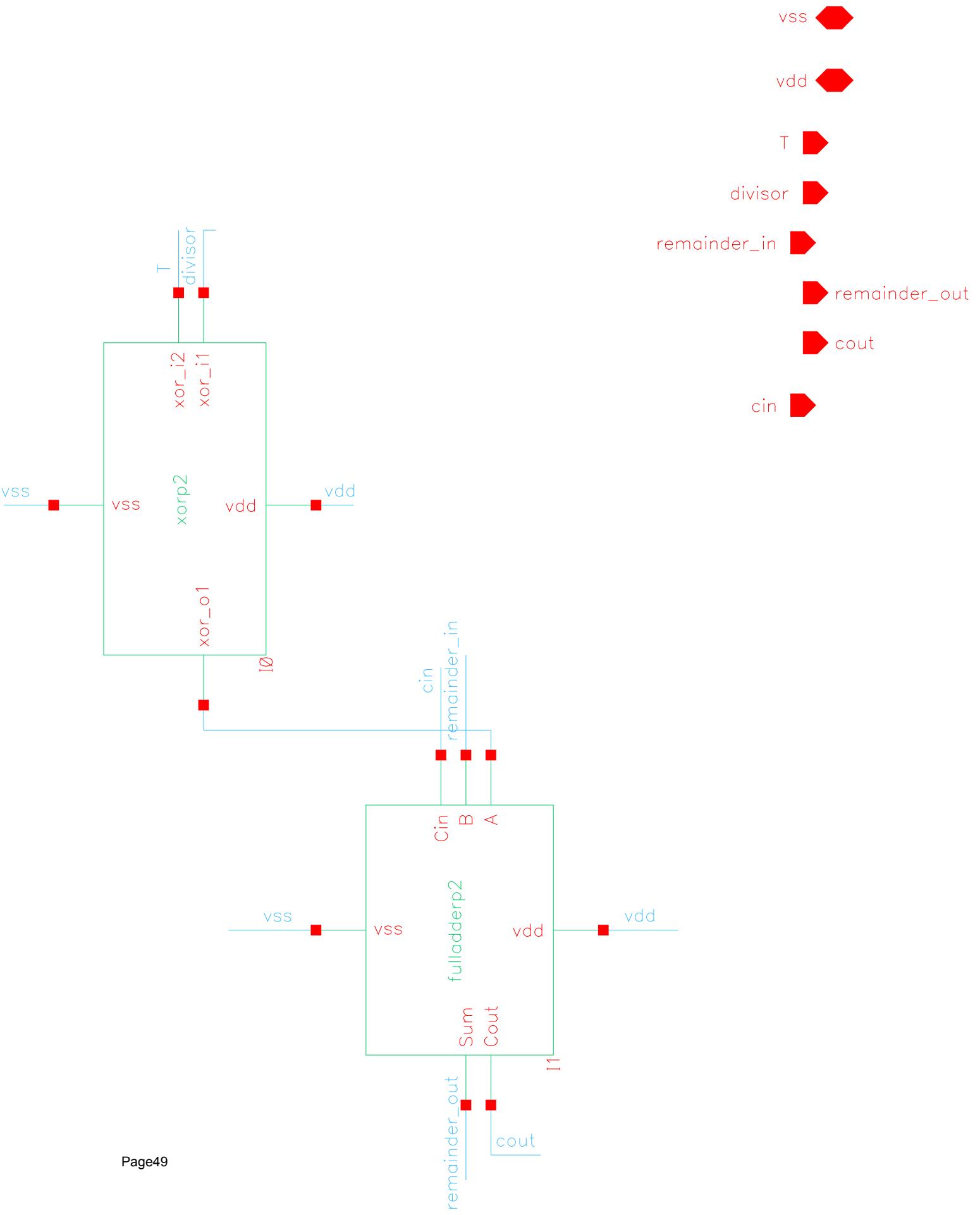
■ /output



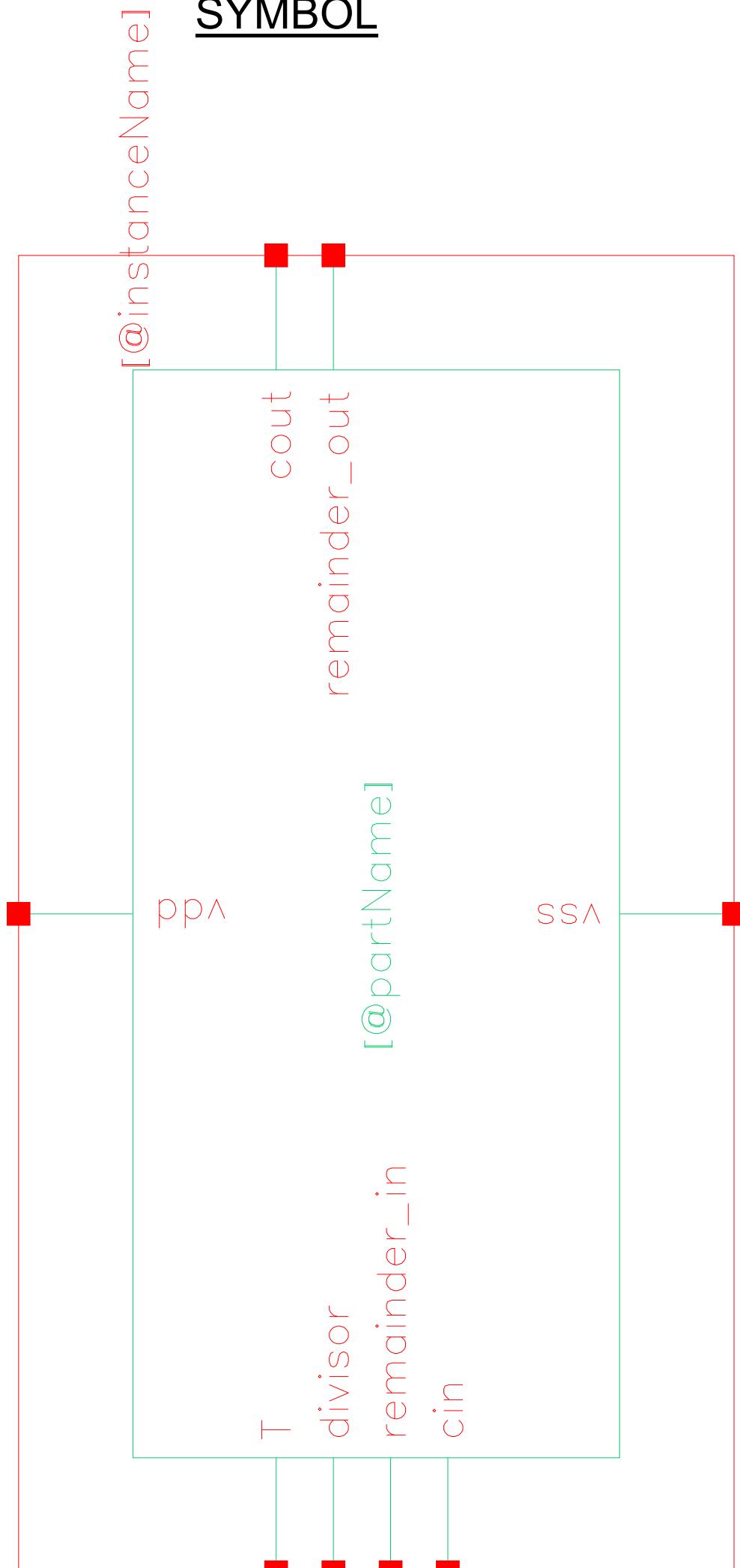
# **ADDER and**

# **SUBTRACT**

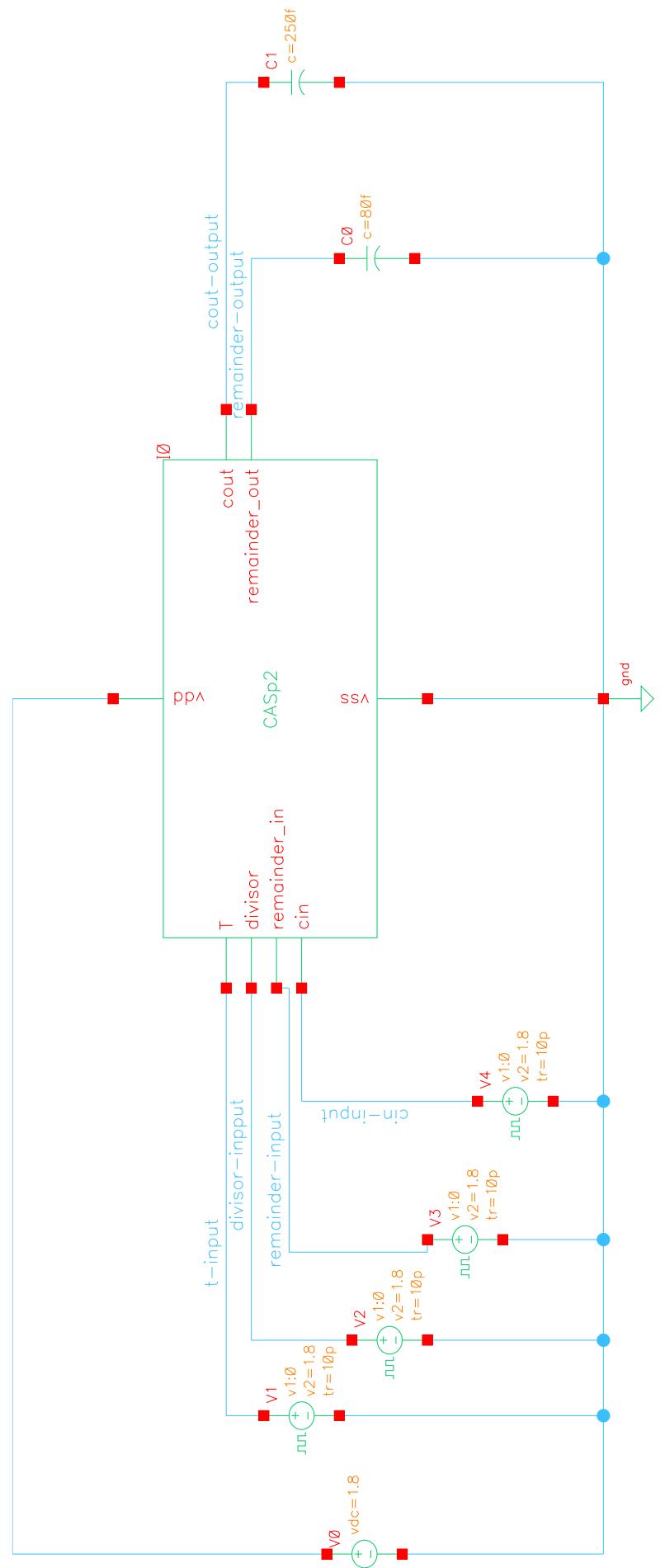
# SCHEMATIC

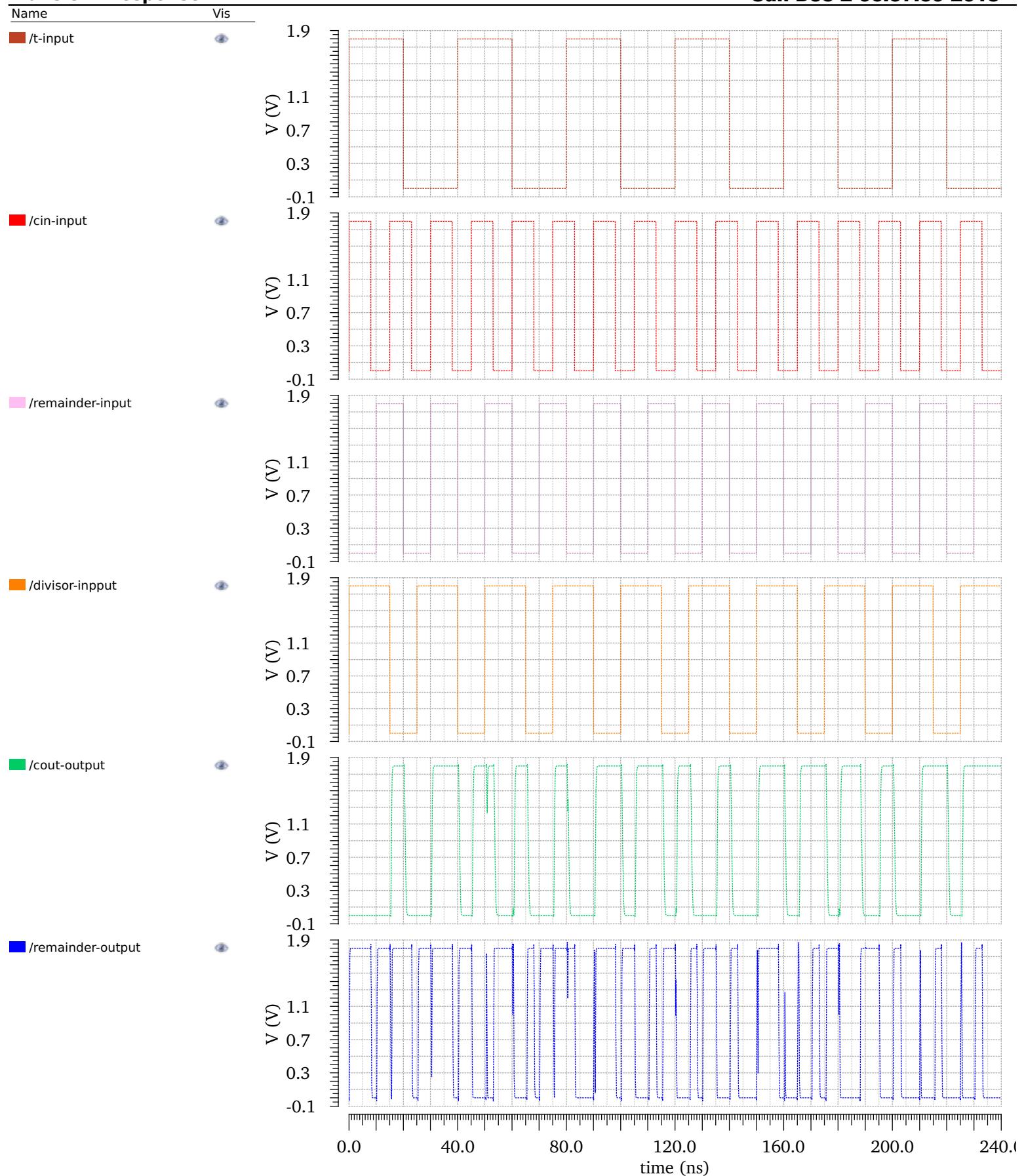


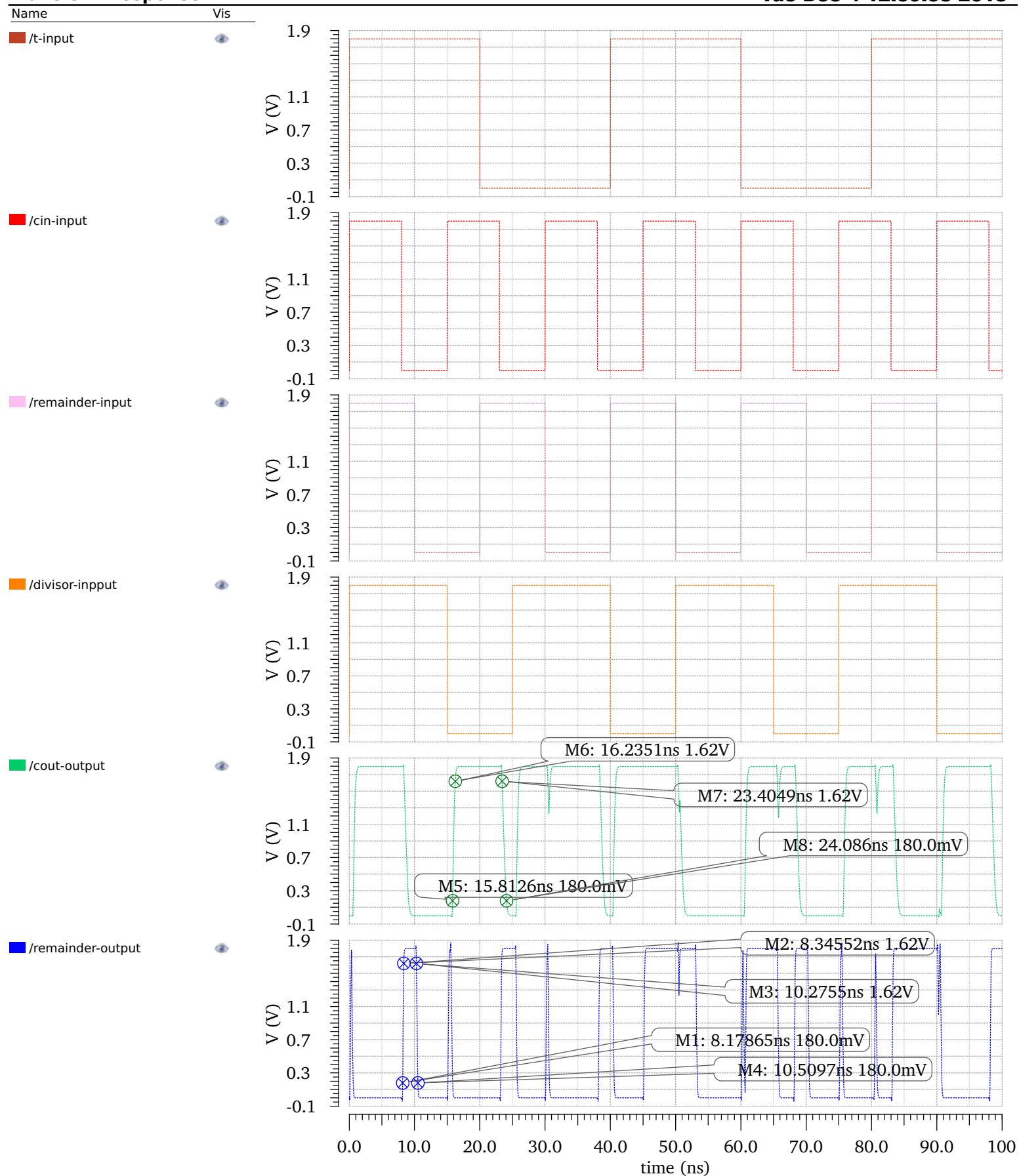
# SYMBOL

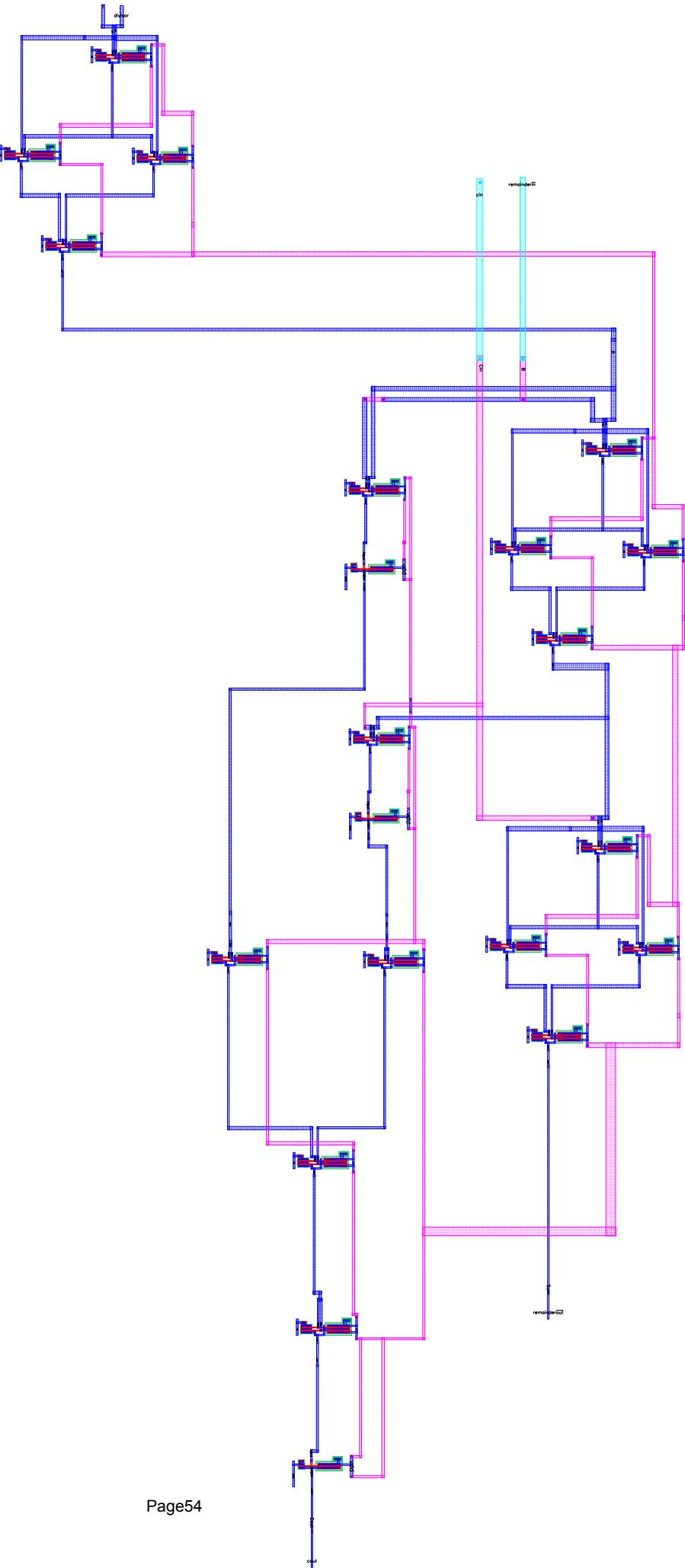


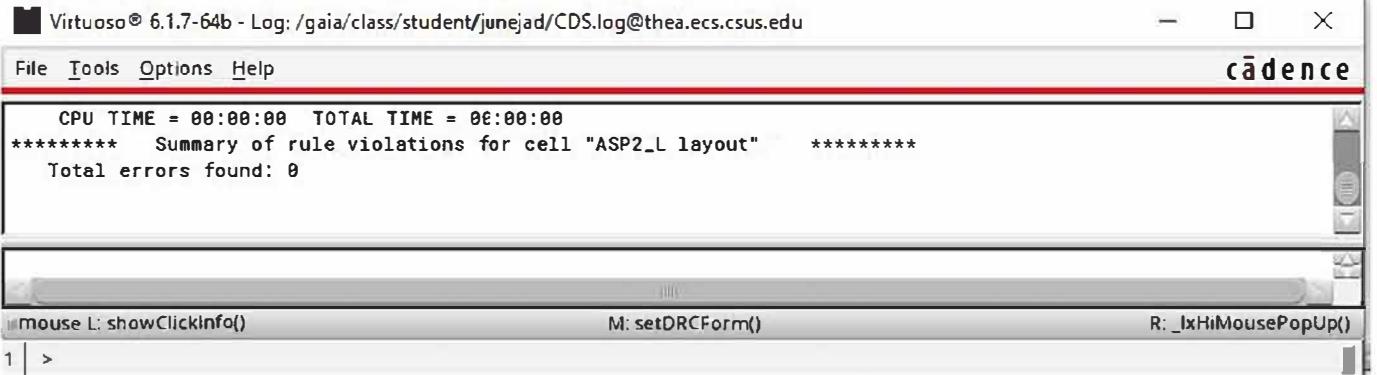
# TEST BENCH SCHEMATIC



**Transient Response****Sun Dec 2 06:57:59 2018**

**Transient Response****Tue Dec 4 12:39:58 2018**





```

casp2 lvs .txt
@(#) $CDS: LVS version 6.1.7-64b 12/07/2018 19:41 (sjfhw305) $

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -
dir /gaia/class/student/junejad/demo/LVS -l -s -t
/gaia/class/student/junejad/demo/LVS/layout
/gaia/class/student/junejad/demo/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

```

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/layout/netlist
count
 45      nets
  0      terminals
 39      pmos
 39      nmos

```

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/schematic/netlist
count
 45      nets
  8      terminals
 39      pmos
 39      nmos

```

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	78	78
total	78	78
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	45	45
total	45	45

```
          casp2 lvs .txt  
          terminals  
un-matched           0      0  
matched but  
different type       0      0  
total                0      8
```

Probe files from /gaia/class/student/junejad/demo/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/junejad/demo/LVS/layout

devbad.out:

netbad.out:

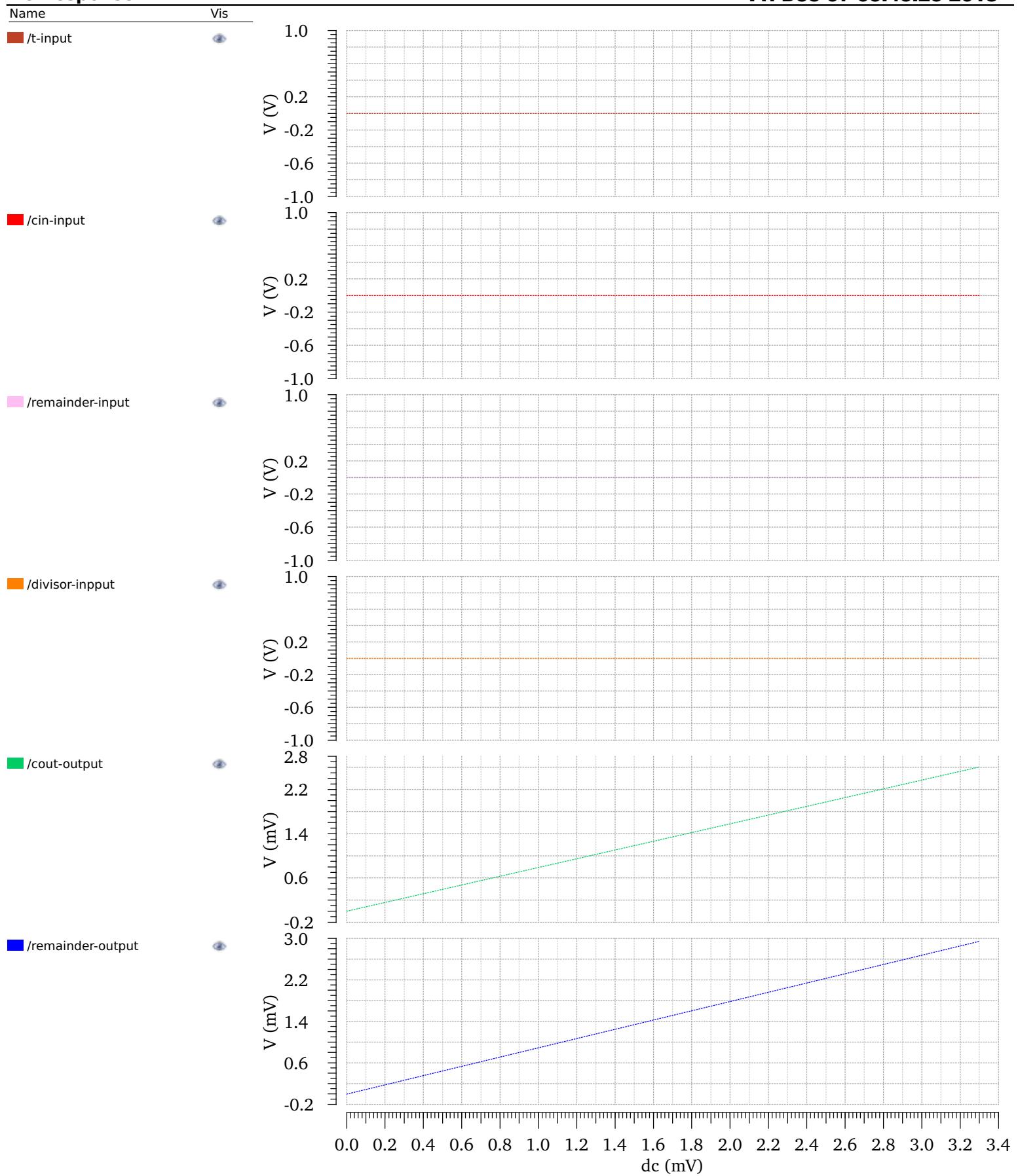
mergenet.out:

termbad.out:

prunenet.out:

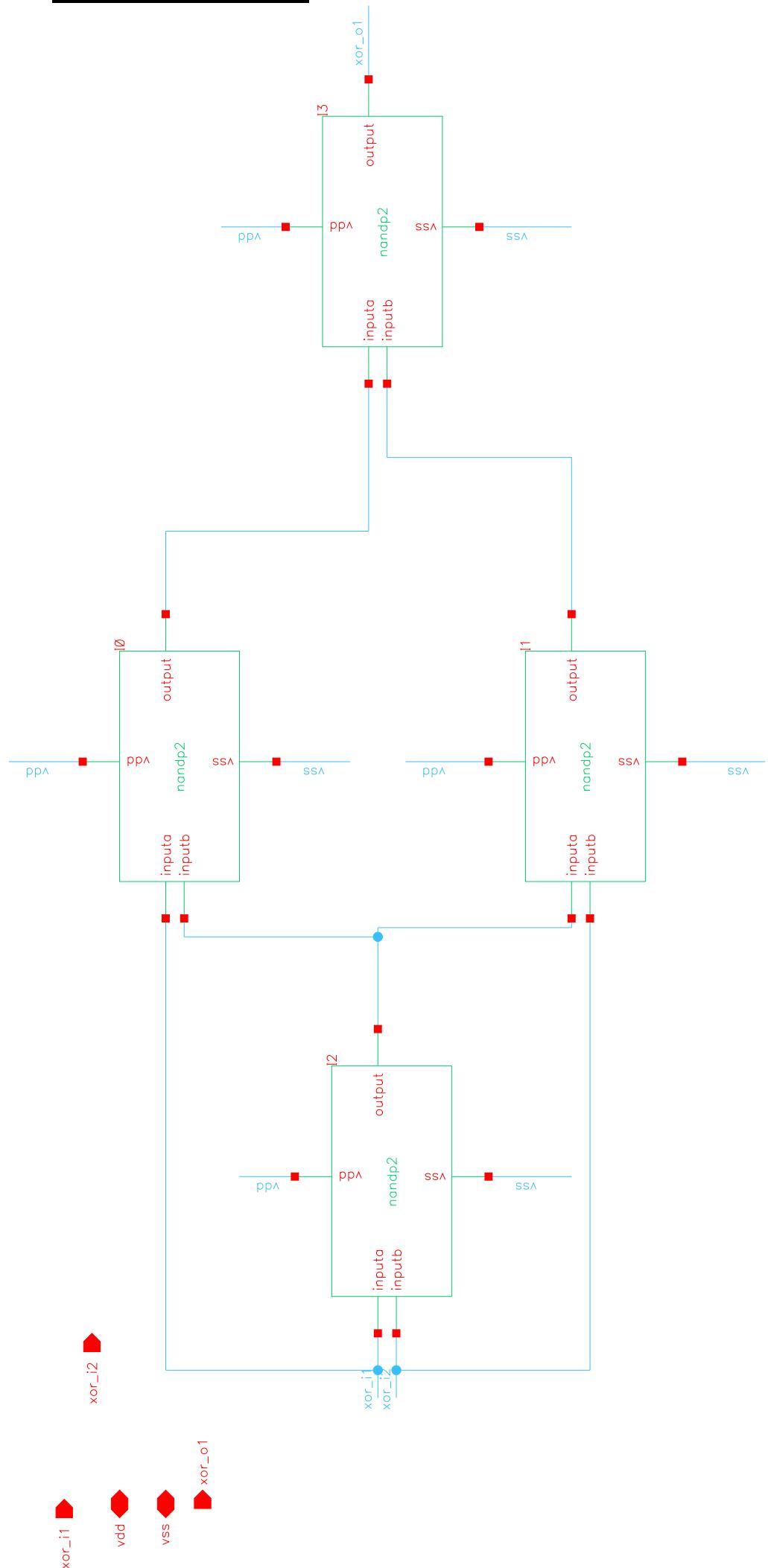
prunedev.out:

audit.out:

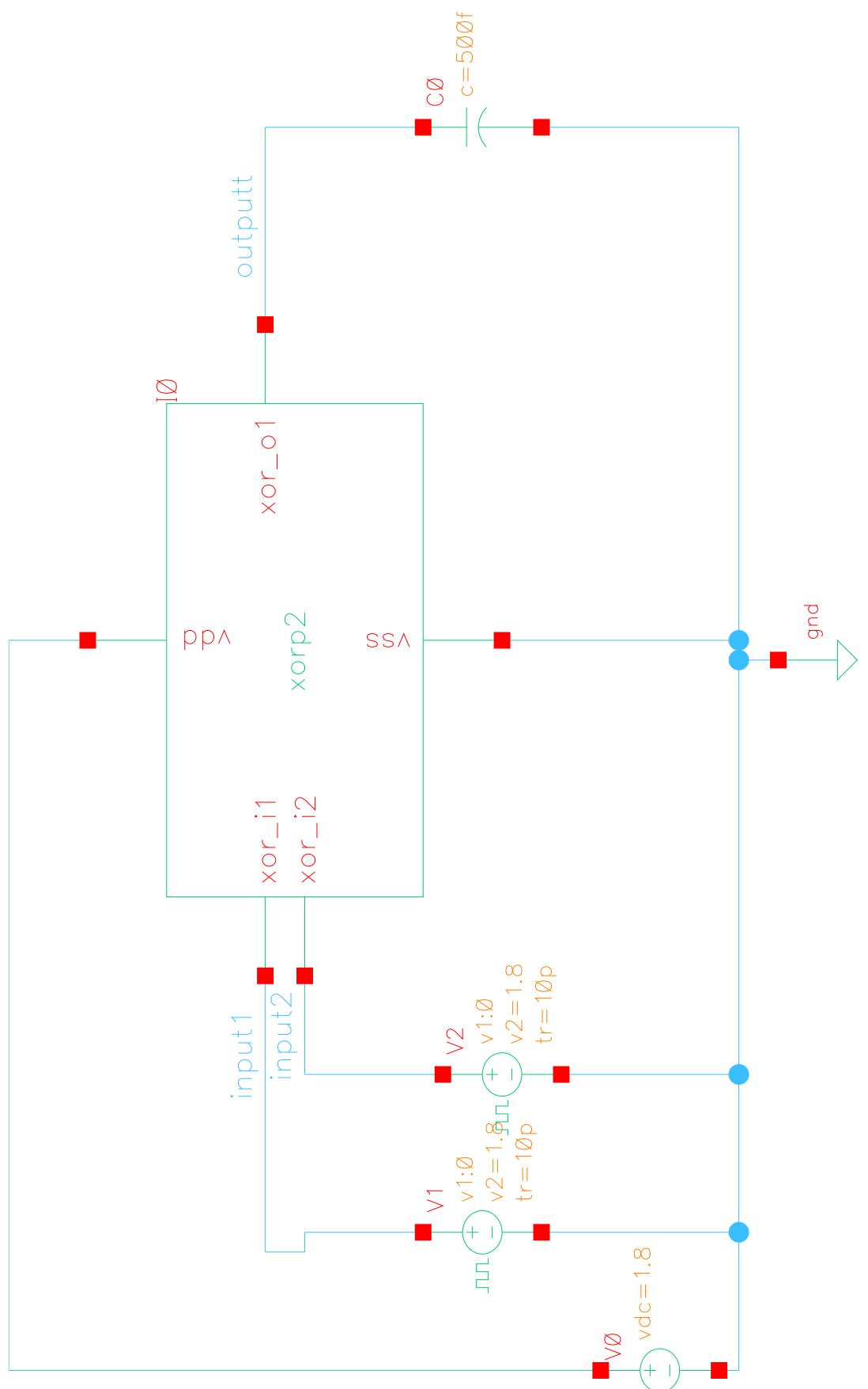
**DC Response****Fri Dec 07 05:45:25 2018**

**XOR**

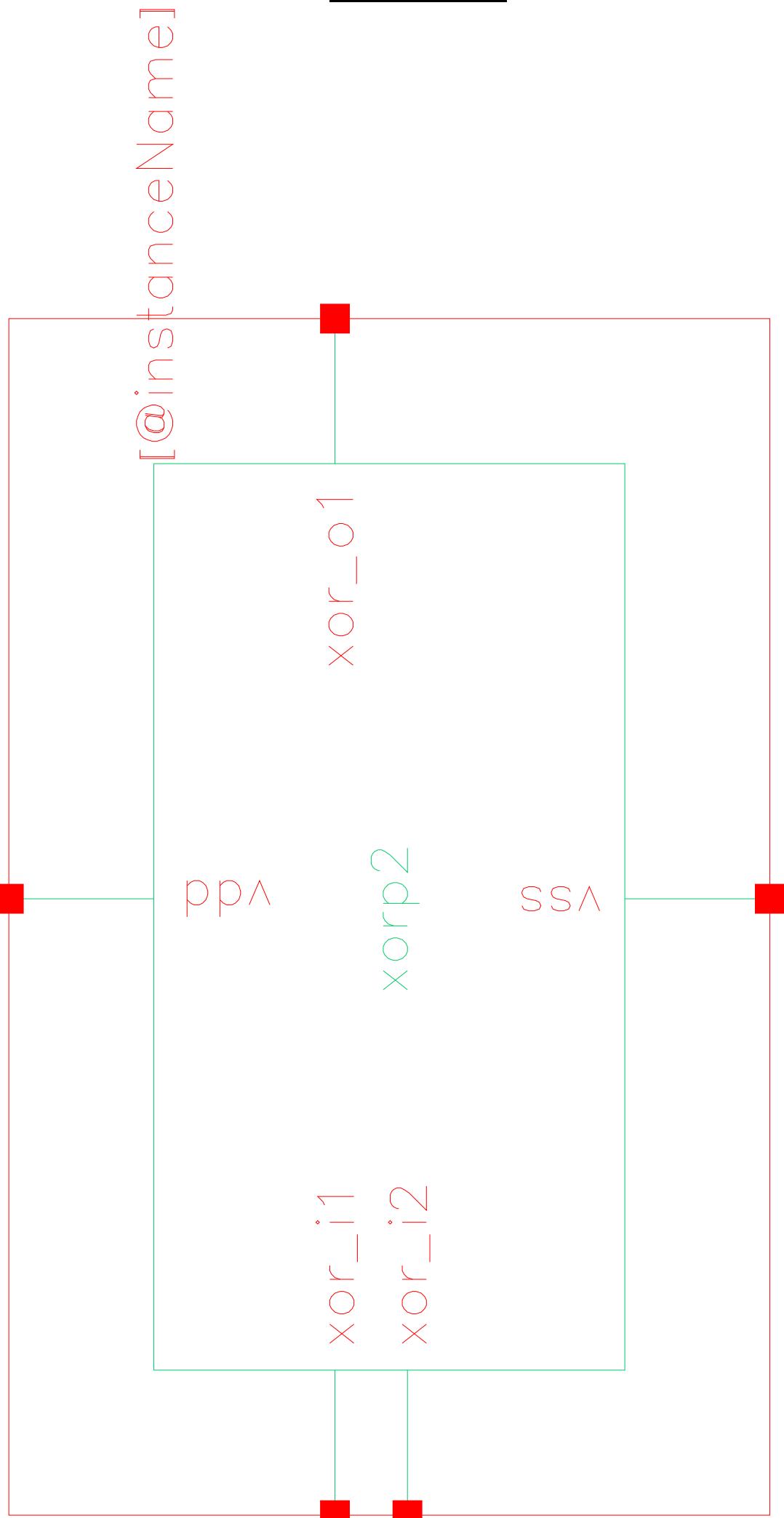
# SCHEMATIC



# TEST BENCH SCHEMATIC



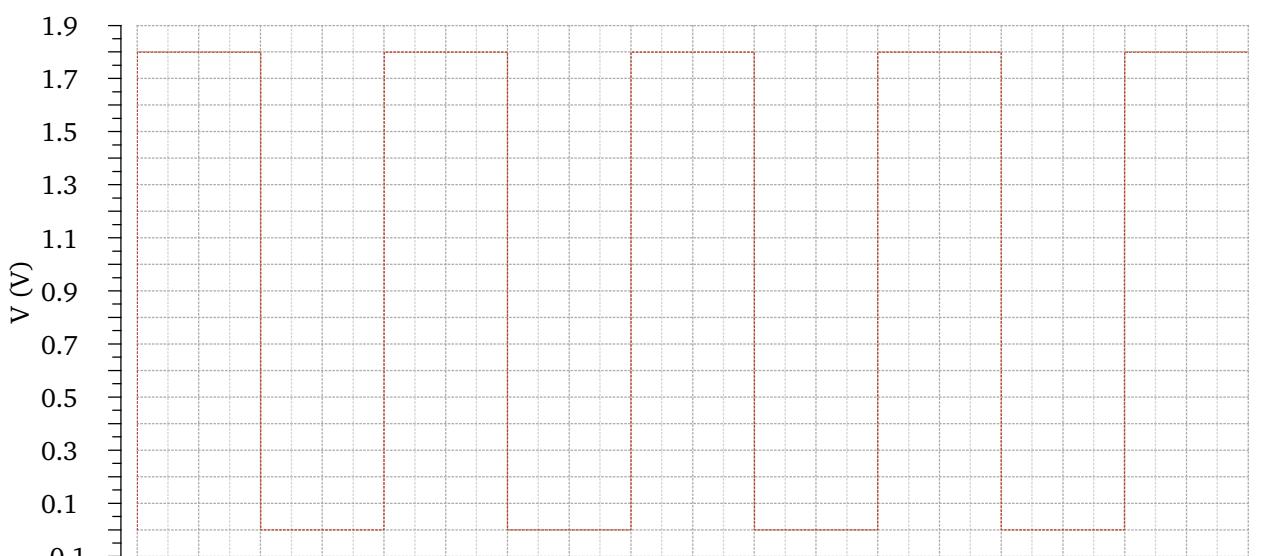
# SYMBOL



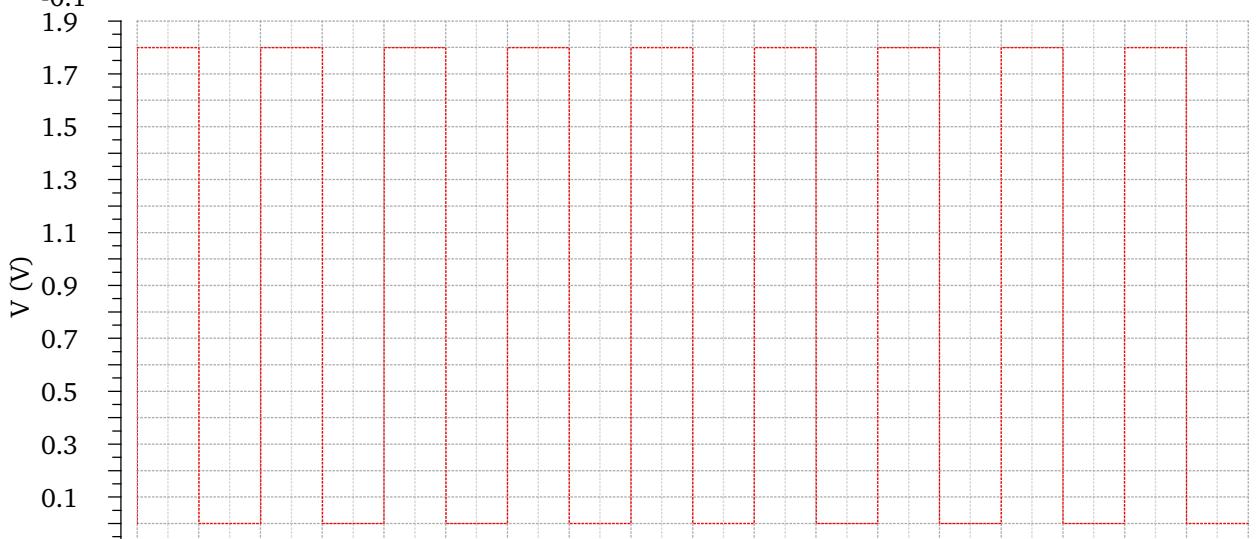
**Transient Response****Mon Dec 3 15:04:50 2018**

Name Vis

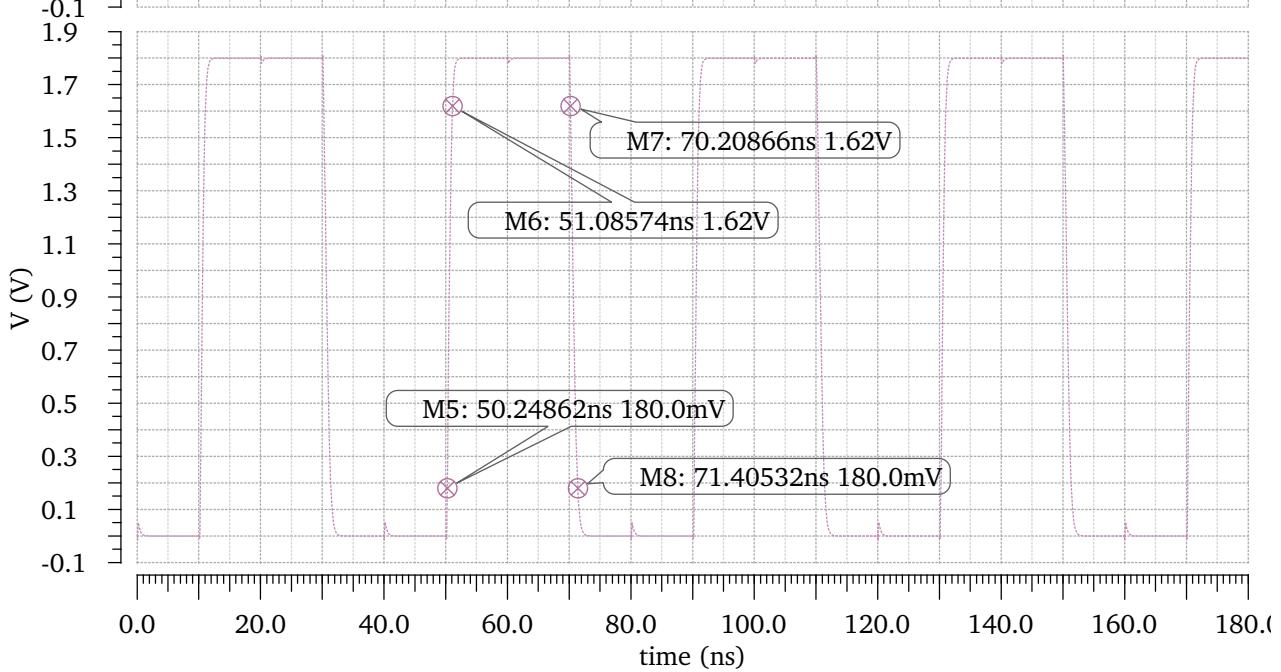
■ /input1

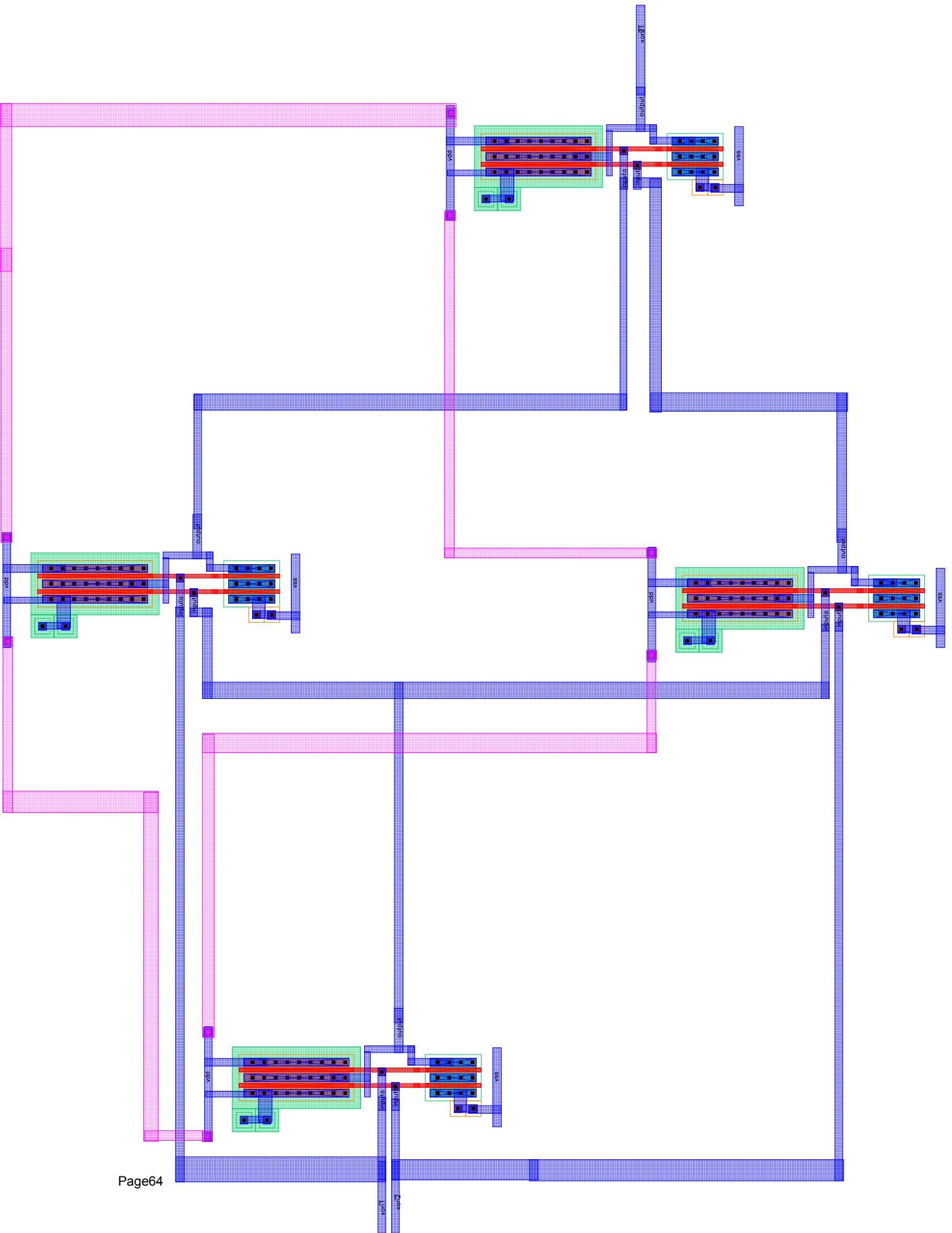


■ /input2



■ /outputt





Virtuoso® 6.1.7-64b - Log: /gaia/class/student/junejad/CDS.log@thea.ecs.csus.edu

File Tools Options Help

cadence

```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "XOR_layout layout" *****
Total errors found: 0
```

mouse L: showClickInfo()  
M: setDRCForm()  
R: \_JxHiMousePopUp()

1 >

```

xor lvs.txt
@(#) $CDS: LVS version 6.1.7-64b 12/07/2018 19:41 (sjfhw305) $

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -
dir /gaia/class/student/junejad/demo/LVS -l -s -t
/gaia/class/student/junejad/demo/LVS/layout
/gaia/class/student/junejad/demo/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

```

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/layout/netlist
count
 12      nets
  0      terminals
  8      pmos
  8      nmos

```

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/schematic/netlist
count
 12      nets
  5      terminals
  8      pmos
  8      nmos

```

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	16	16
total	16	16
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	12	12
total	12	12

	xor	lvs.txt
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	0	5

Probe files from /gaia/class/student/junejad/demo/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/junejad/demo/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

**DC Response****Fri Dec 07 02:30:38 2018**

Name Vis

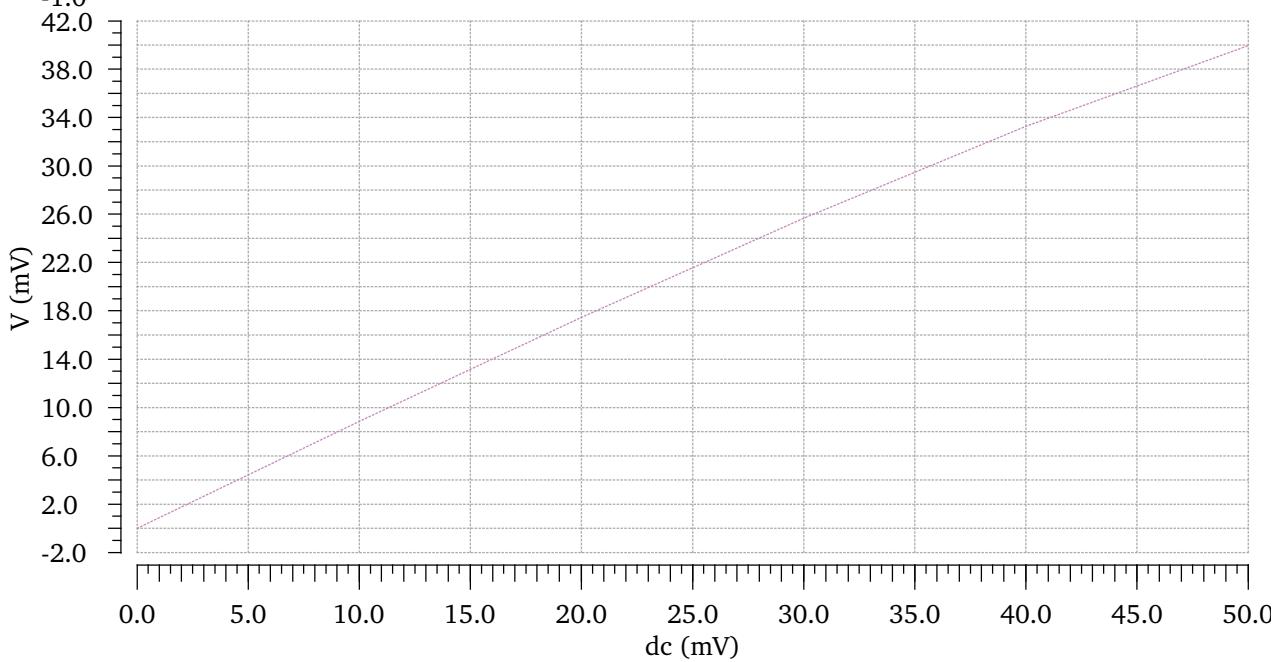
■ /input1



■ /input2

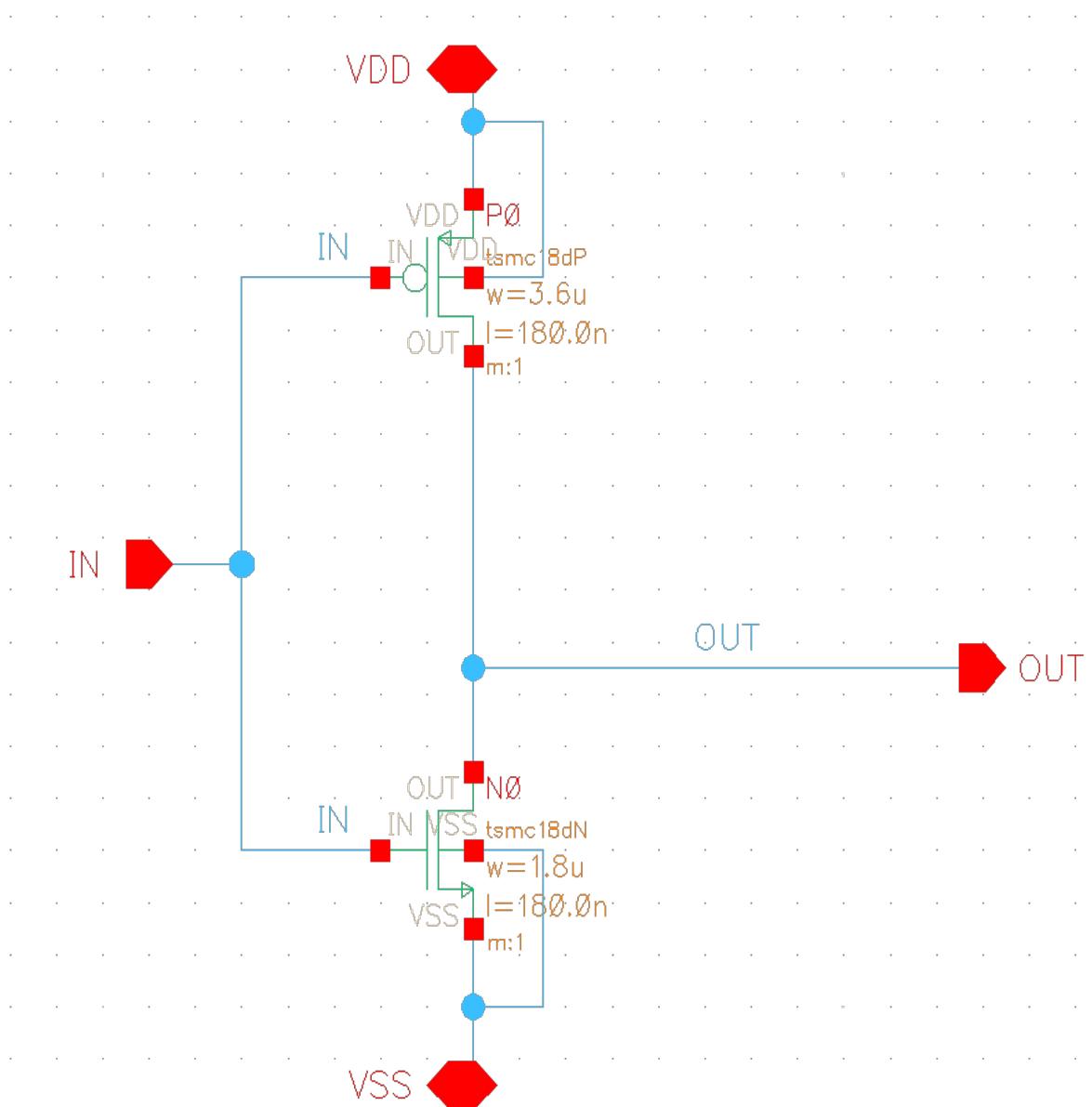


■ /outputt

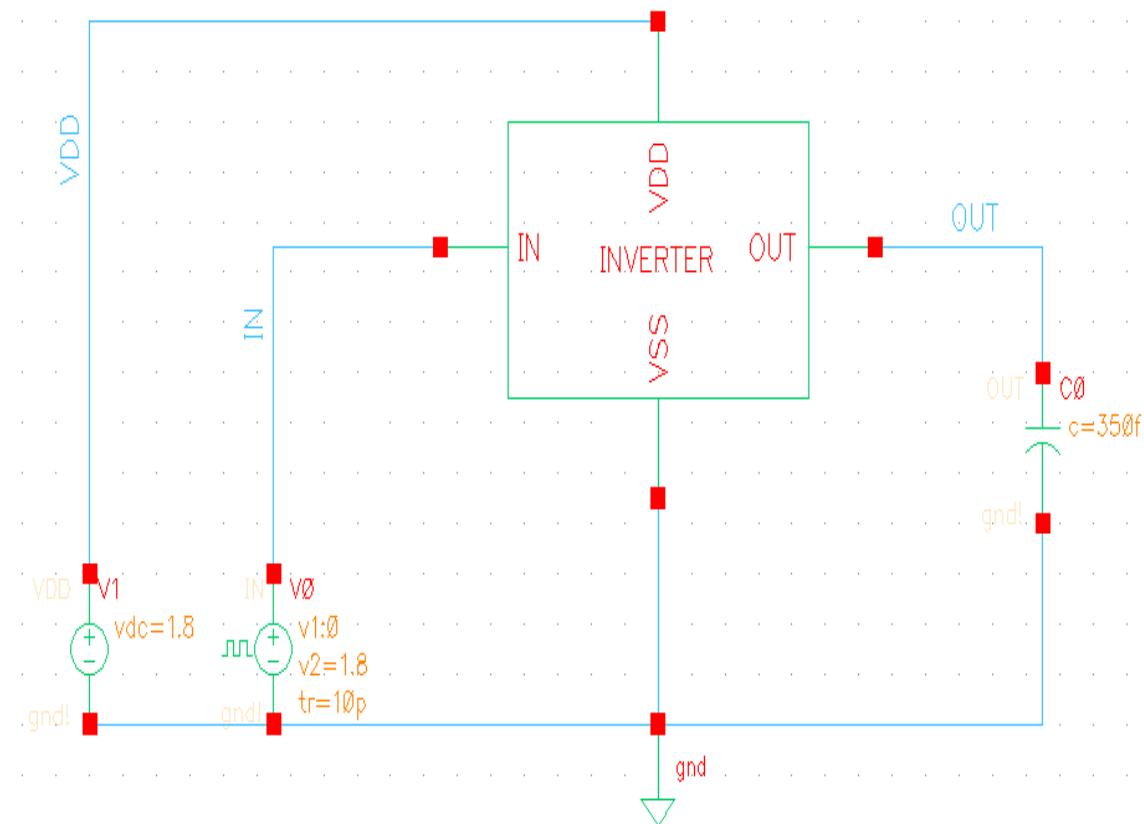


# **CMOS INVERTER**

## SCHEMATIC OF INVERTER



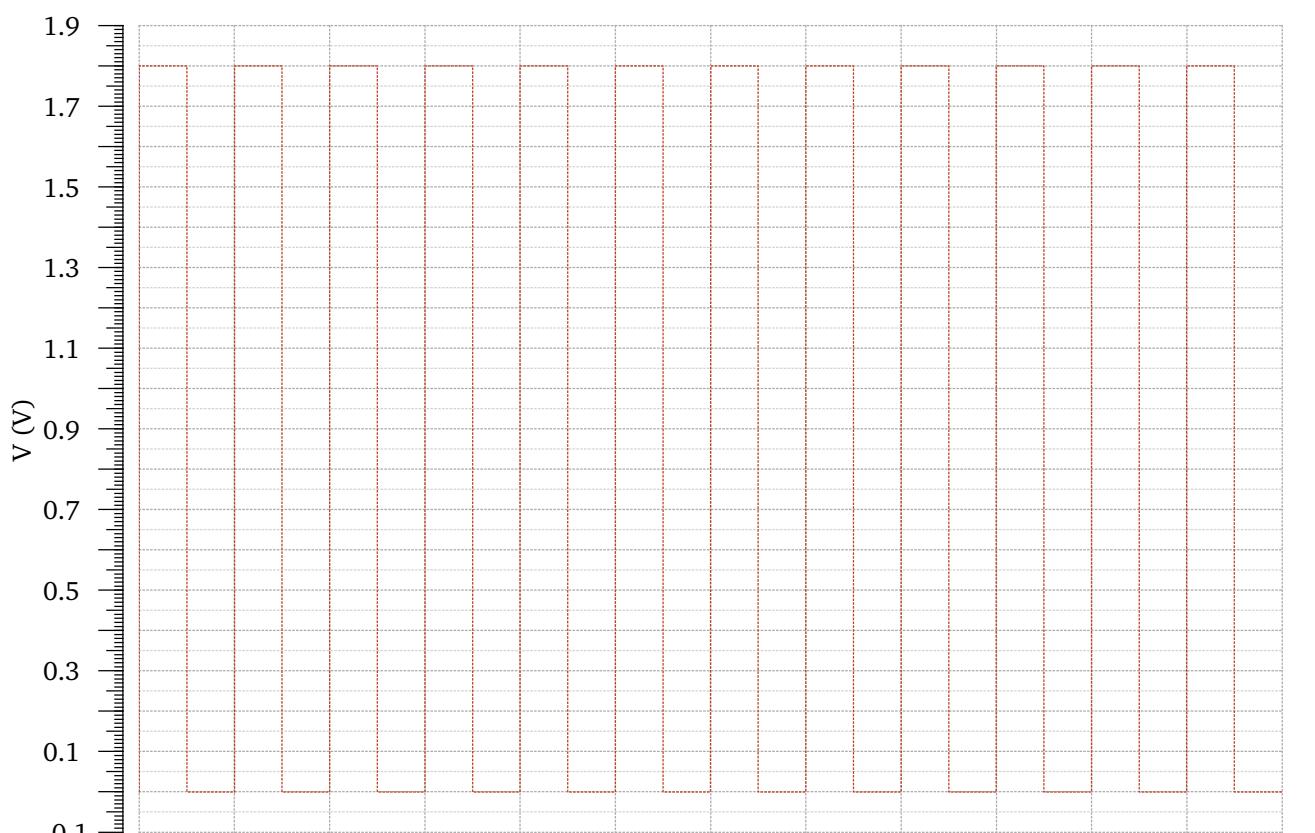
## TESTBENCH SCHEMATIC OF INVERTER



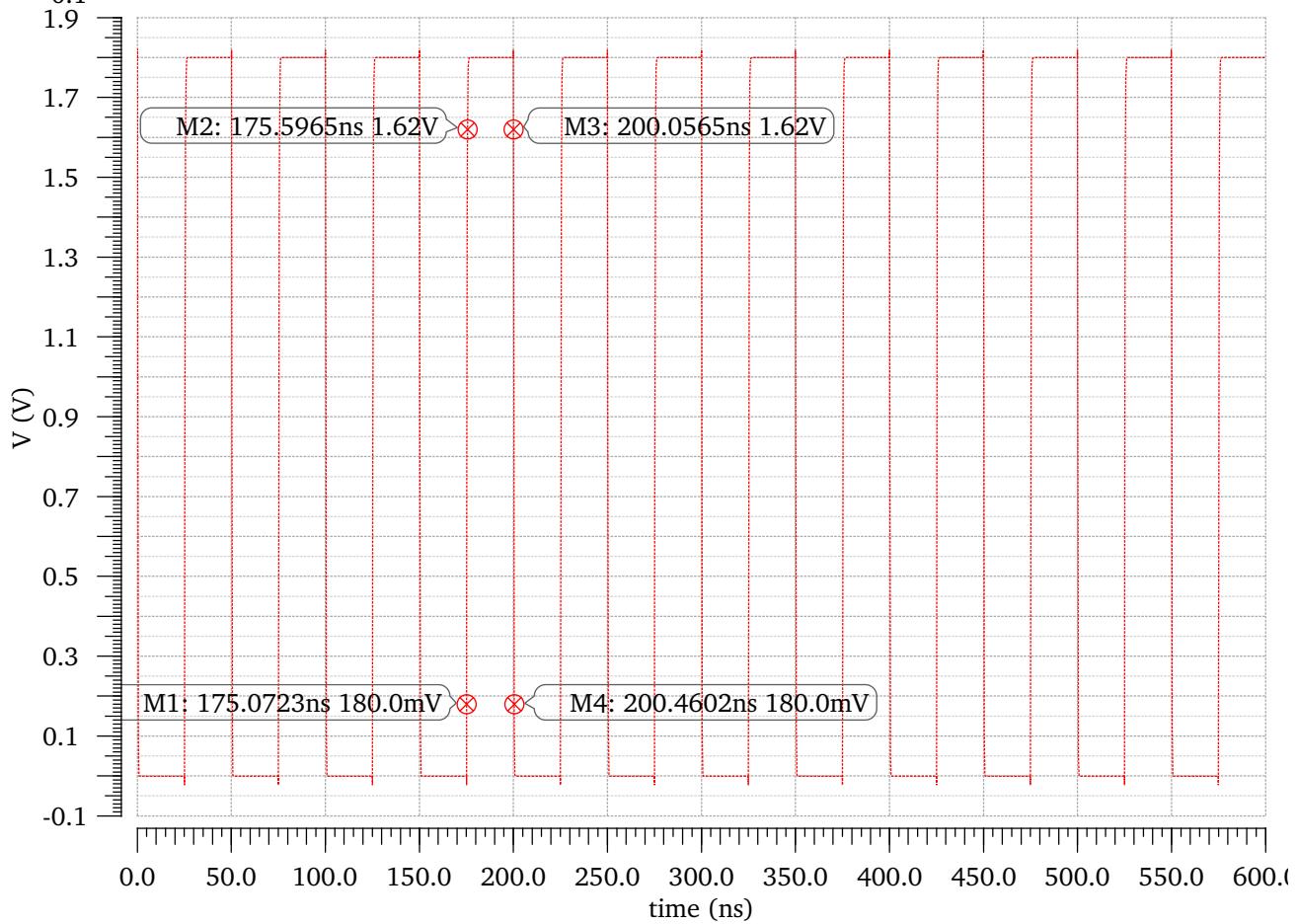
**Transient Response****Fri Oct 5 14:15:21 2018**

Name Vis

/IN



/OUT



# DRC FILE

Virtuoso® 6.1.7-64b - Log: /gaia/class/student/junejad/CDS.log@thea.ecs.csus.edu

File Tools Options Help

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

\*\*\*\*\* Summary of rule violations for cell "Inverter\_L layout" \*\*\*\*\*

Total errors found: 0

mouse L: showClickInfo() M: setDRCForm() R: \_IxHiMousePopUp()

1 >

The screenshot shows a software window titled 'Virtuoso® 6.1.7-64b - Log: /gaia/class/student/junejad/CDS.log@thea.ecs.csus.edu'. The menu bar includes 'File', 'Tools', 'Options', and 'Help'. The main pane displays a log message indicating a clean DRC check: 'CPU TIME = 00:00:00 TOTAL TIME = 00:00:00', '\*\*\*\*\* Summary of rule violations for cell "Inverter\_L layout" \*\*\*\*\*', and 'Total errors found: 0'. At the bottom, there are three status indicators: 'mouse L: showClickInfo()', 'M: setDRCForm()', and 'R: \_IxHiMousePopUp()'. A scroll bar is visible on the right side of the main pane.

# LVS FILE

## Untitled

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS  
-dir /gaia/class/student/junejad/CMOS\_Inverter/LVS -l -s -t  
/gaia/class/student/junejad/CMOS\_Inverter/LVS/layout  
/gaia/class/student/junejad/CMOS\_Inverter/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.

Net-list summary for  
/gaia/class/student/junejad/CMOS\_Inverter/LVS/layout/netlist

count	
4	nets
0	terminals
1	pmos
1	nmos

Net-list summary for  
/gaia/class/student/junejad/CMOS\_Inverter/LVS/schematic/netlist

count	
4	nets
4	terminals
1	pmos
1	nmos

Devices in the netlist but not in the rules:

pcapacitor pmos nmos

The net-lists match.

	layout	schematic
	instances	

un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2

## nets

un-matched	0	0
merged	0	0
pruned	0	0
active	4	4
total	4	4

## terminals

un-matched	0	0
matched but		

	Untitled	
different type	0	0
total	0	4

Probe files from /gaia/class/student/junejad/CMOS\_Inverter/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/junejad/CMOS\_Inverter/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

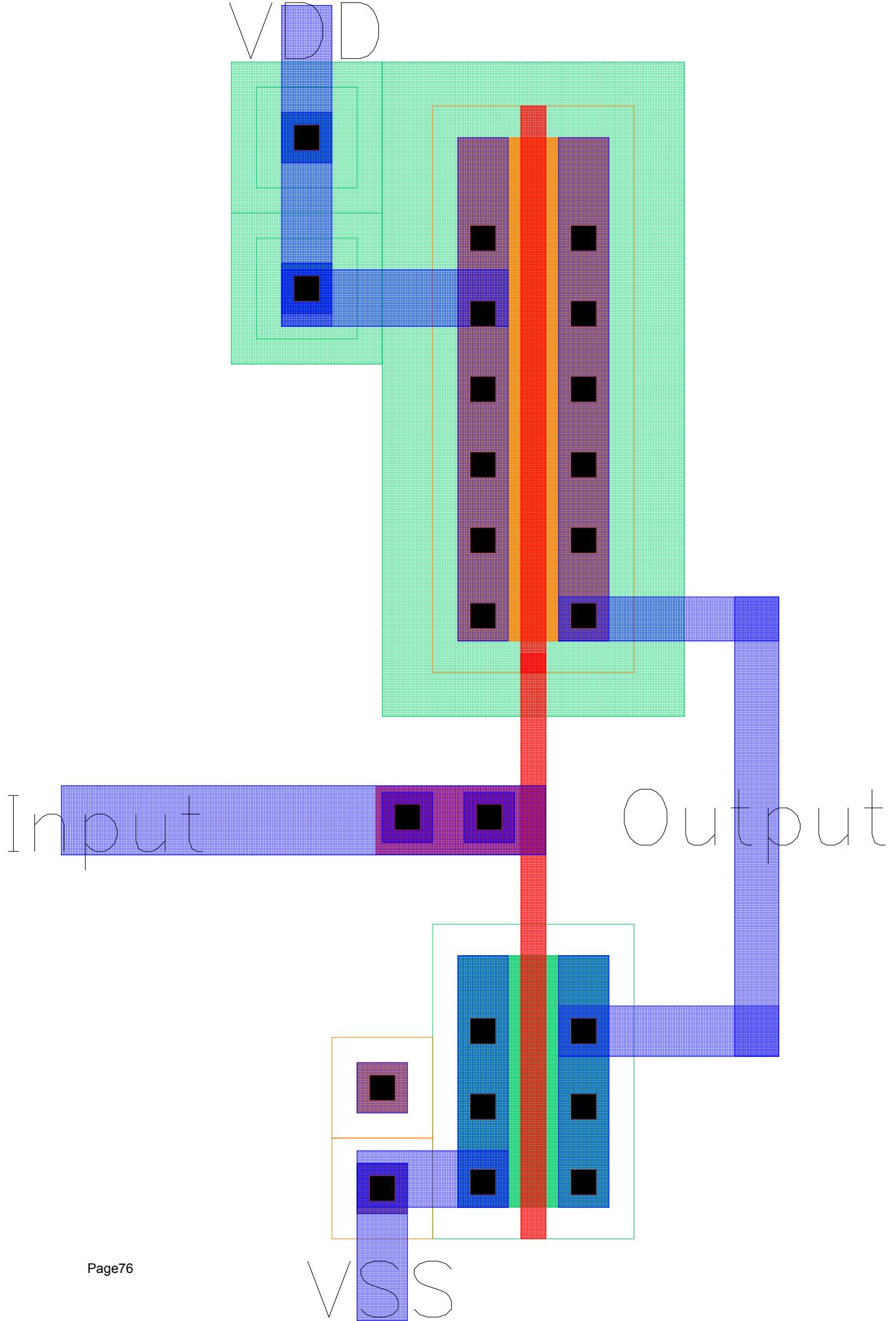
termbad.out:

prunenet.out:

prunedev.out:

audit.out:

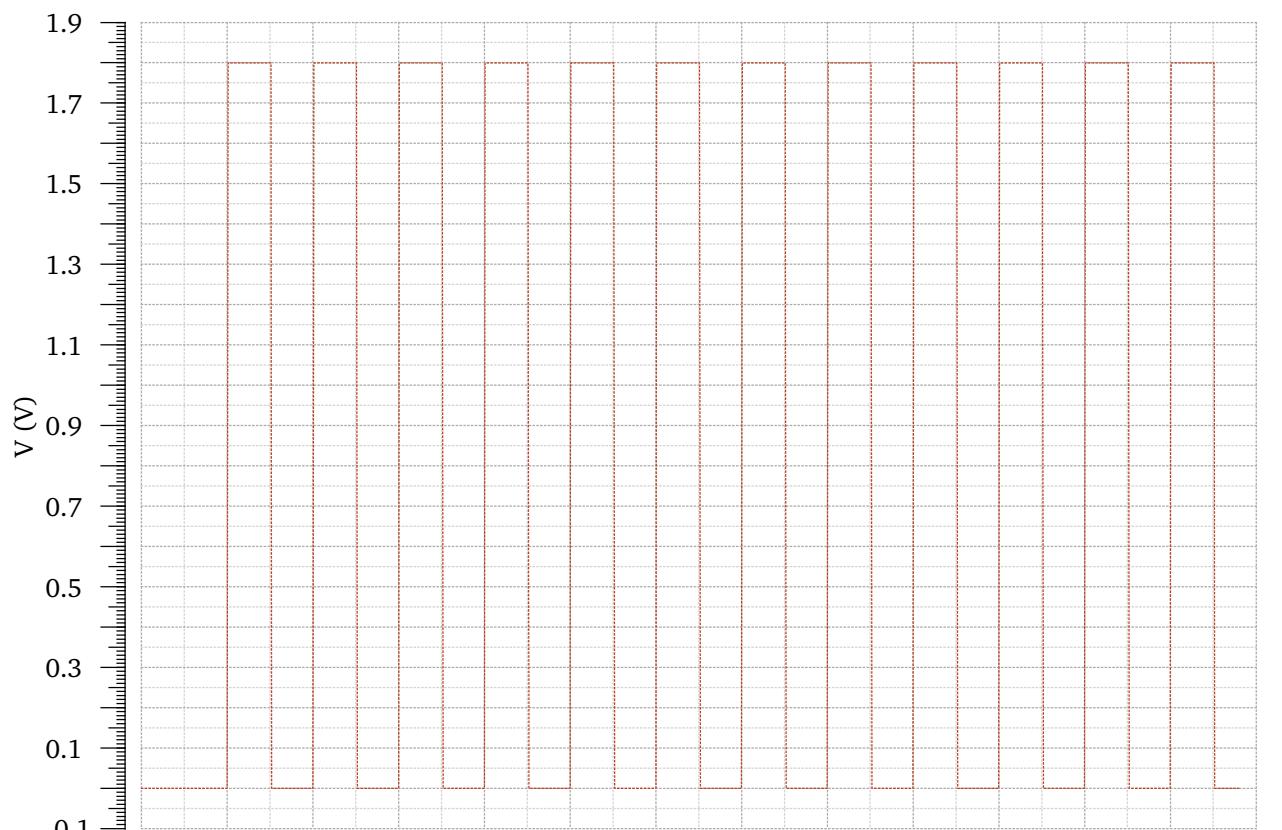
## LAYOUT



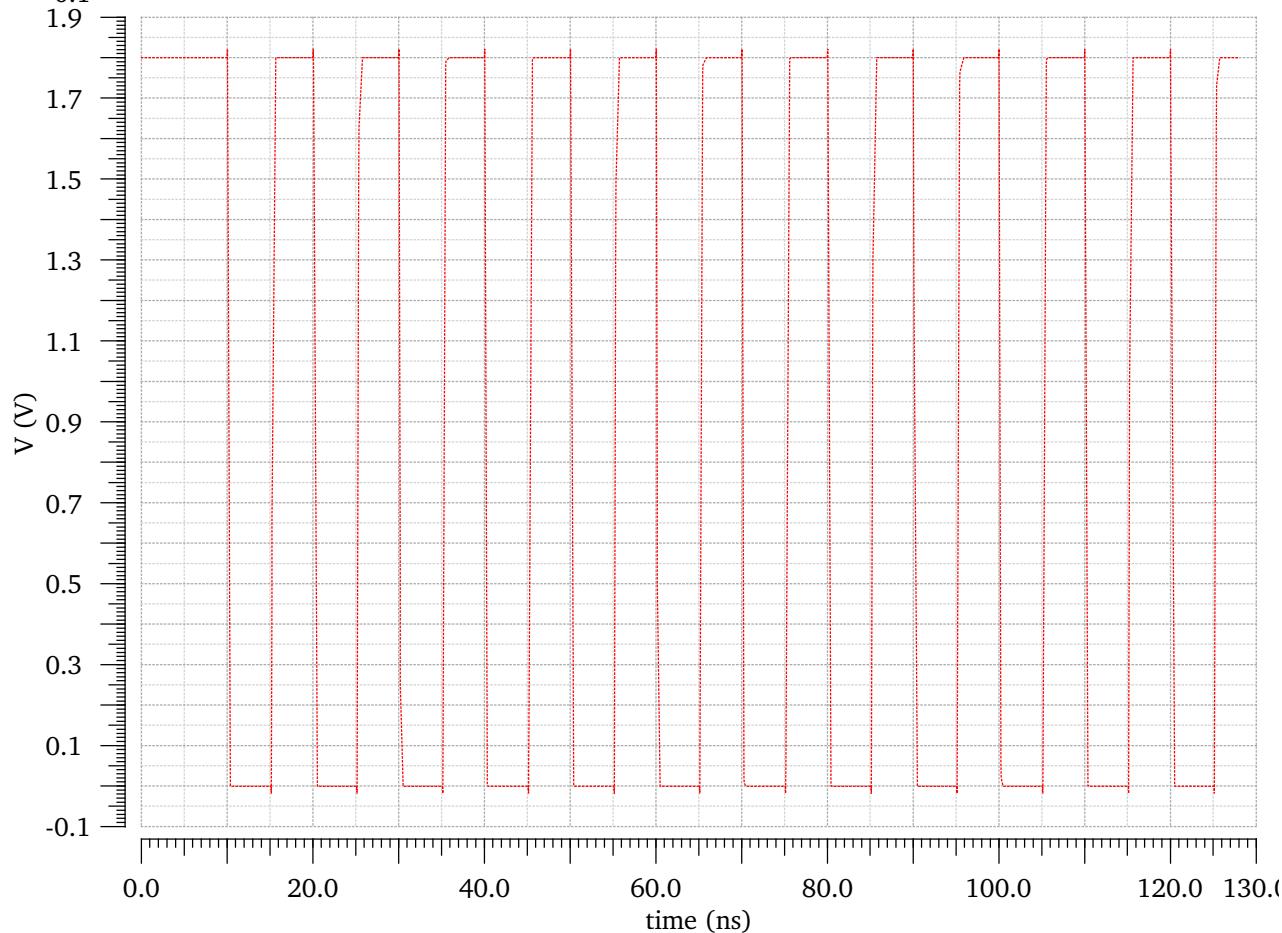
**Transient Response****Sat Oct 6 10:15:59 2018**

Name Vis

■ /Input



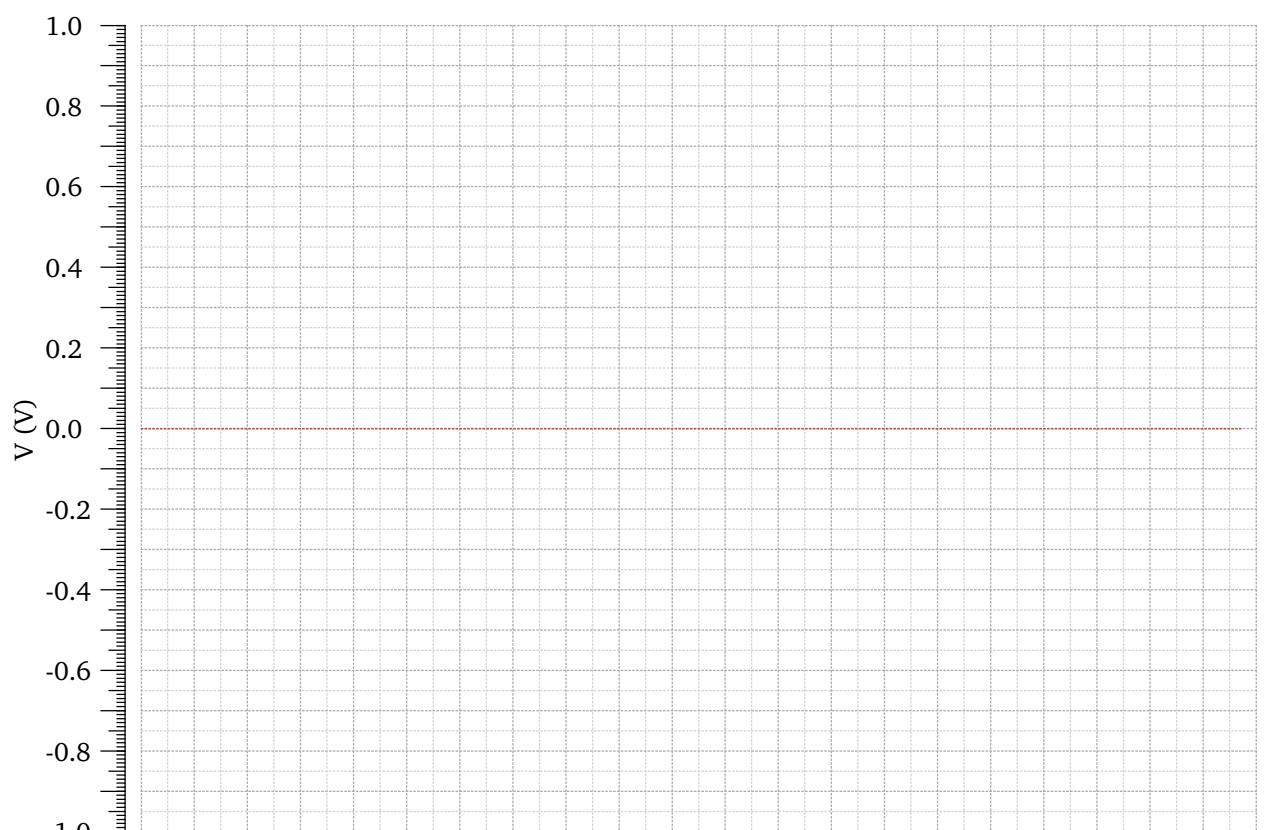
■ /Output



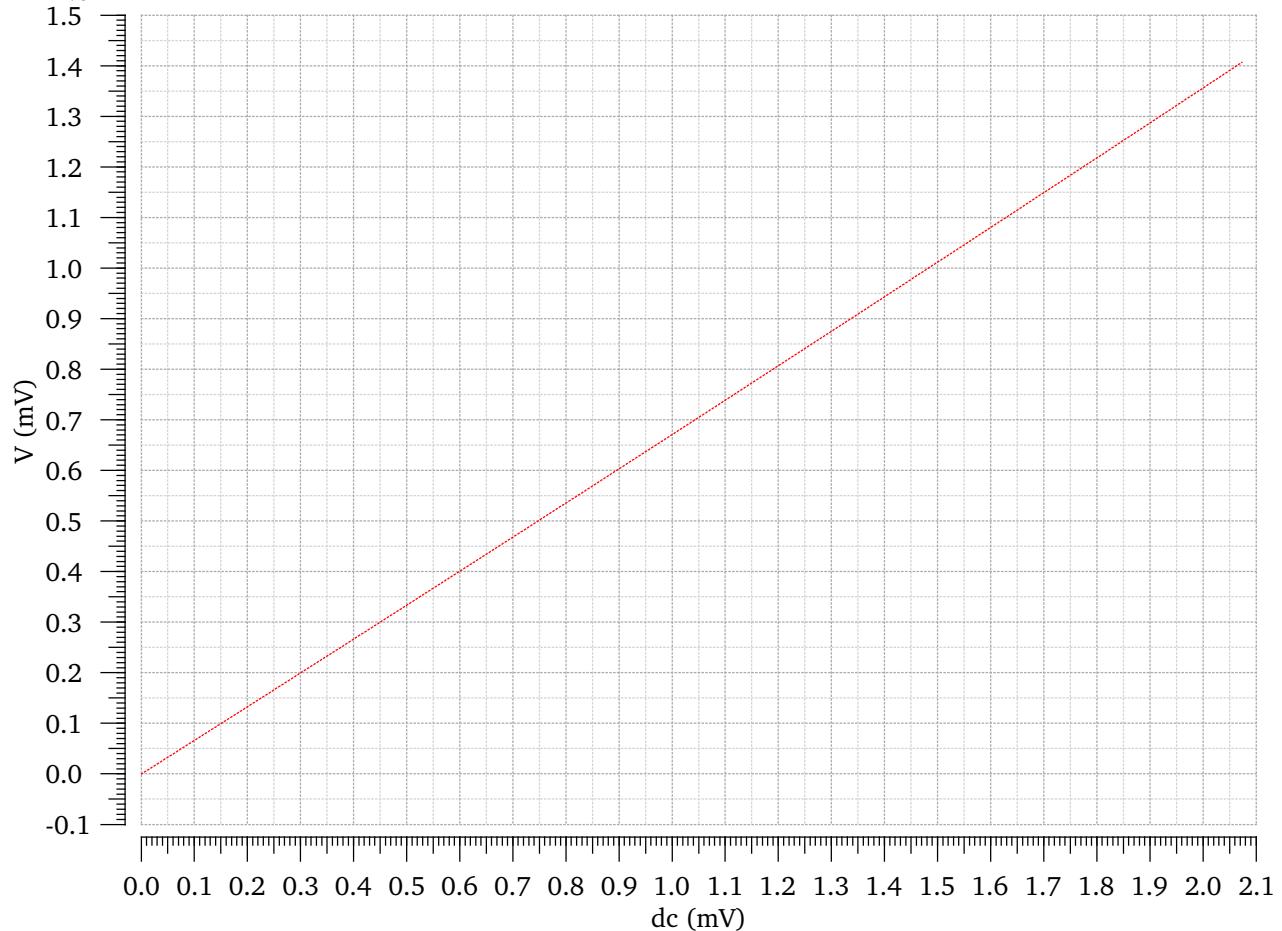
**DC Response****Sat Oct 6 10:15:59 2018**

Name Vis

■ /Input

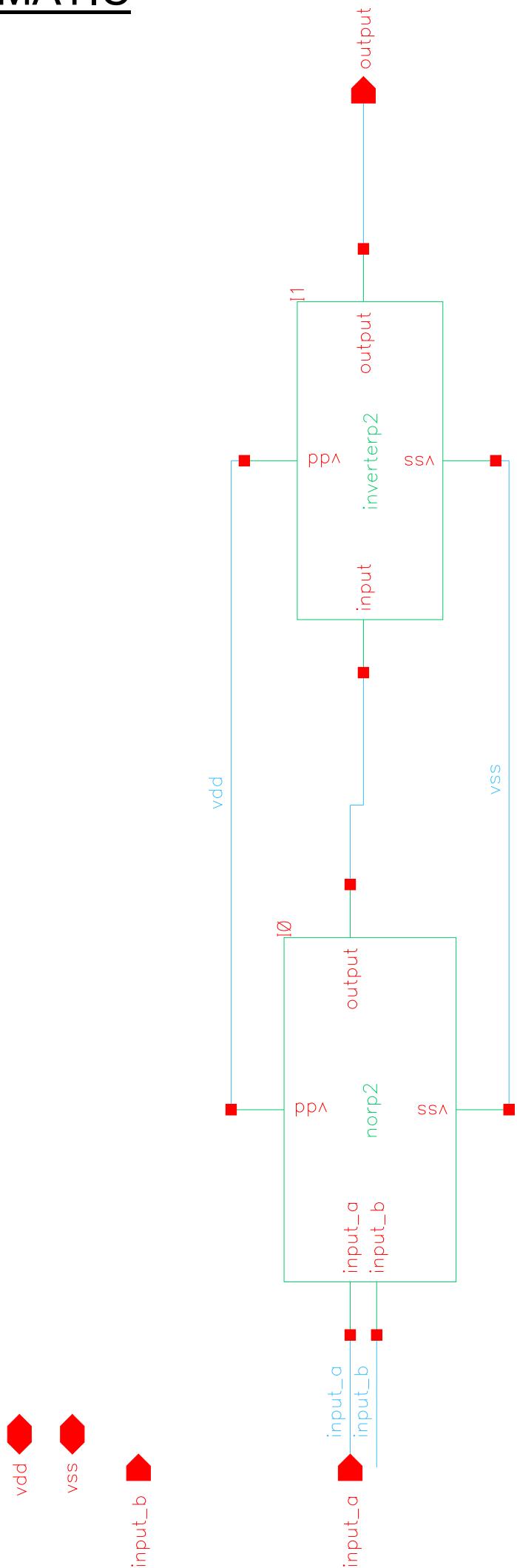


■ /Output

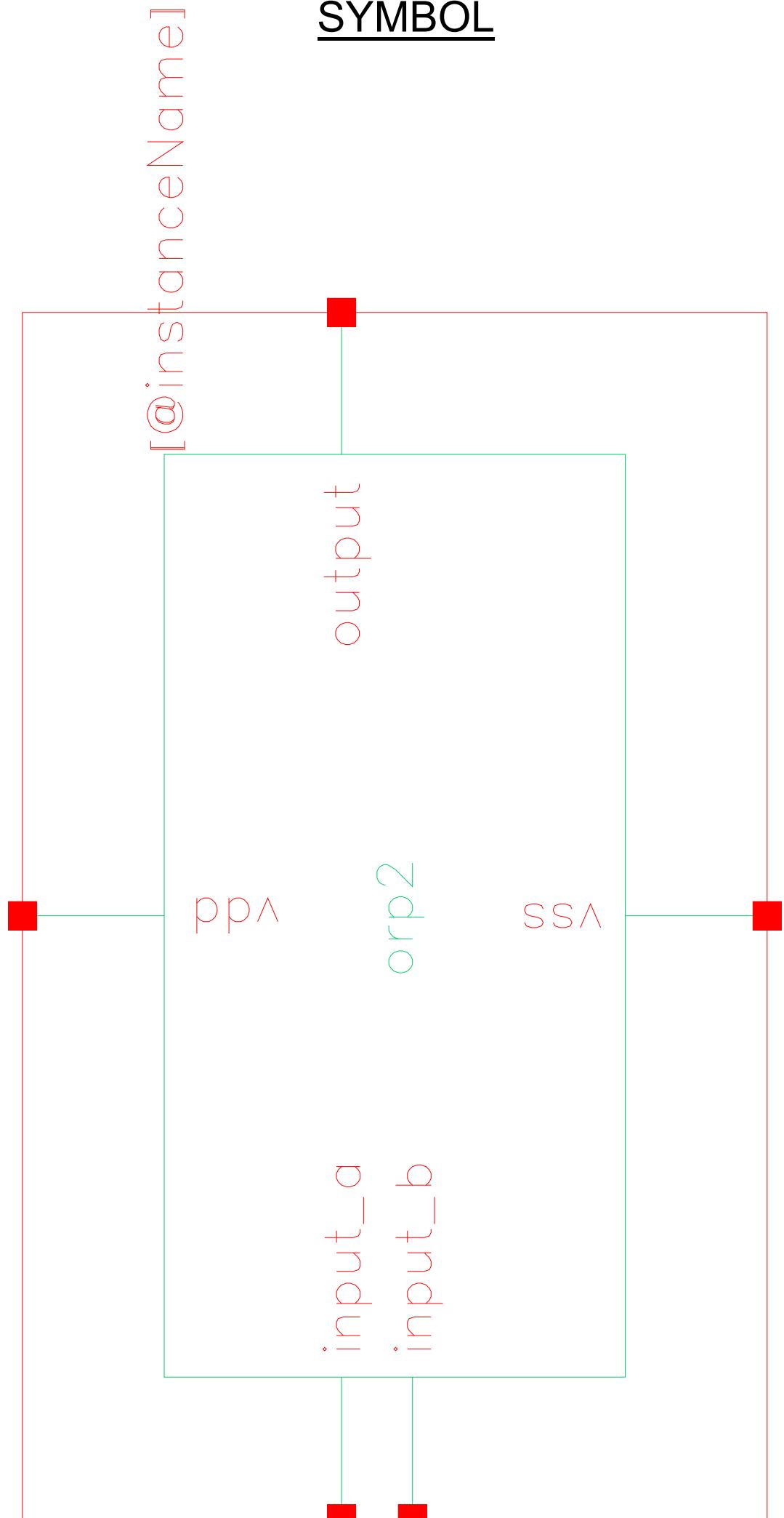


**OR**

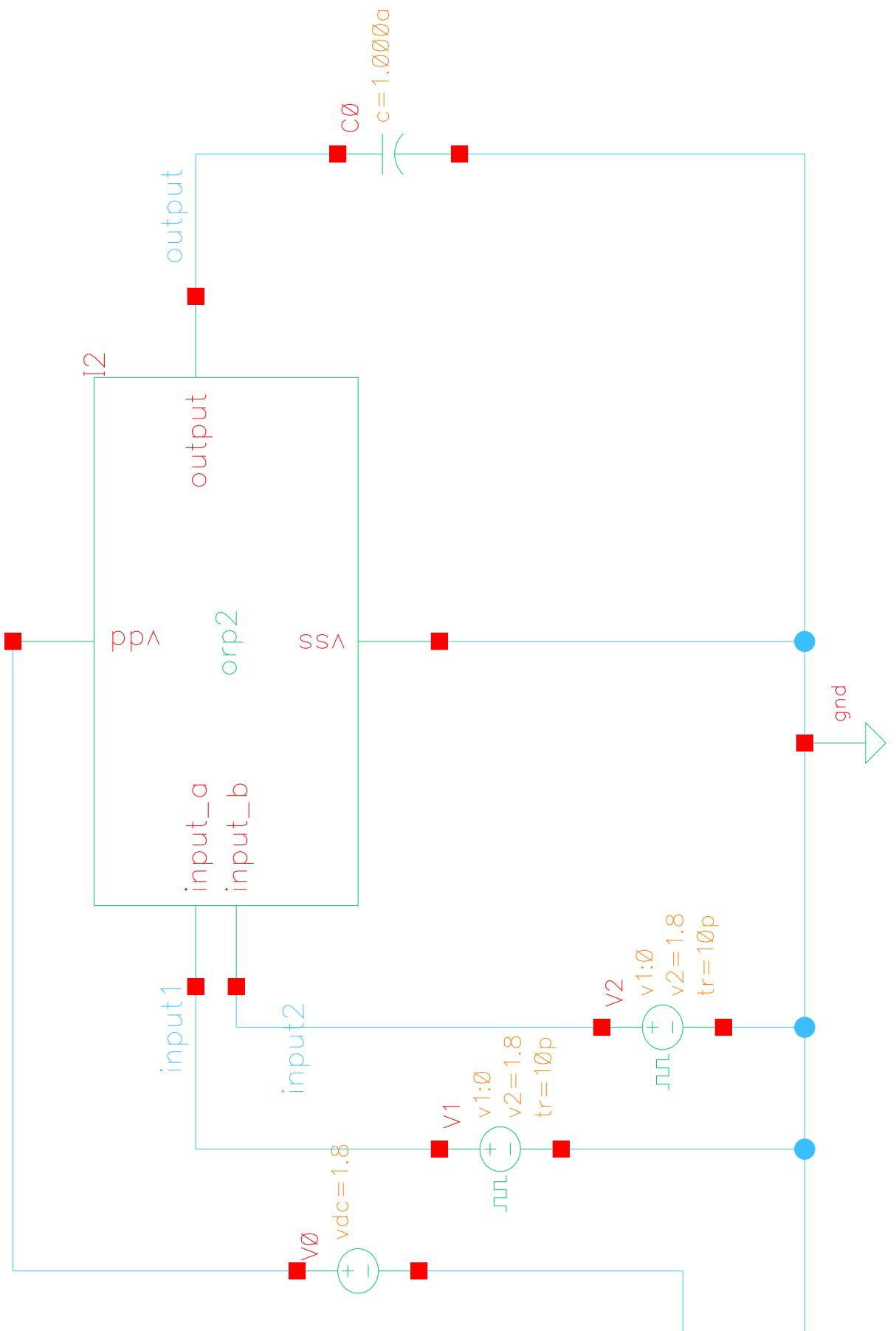
# SCHEMATIC



## SYMBOL

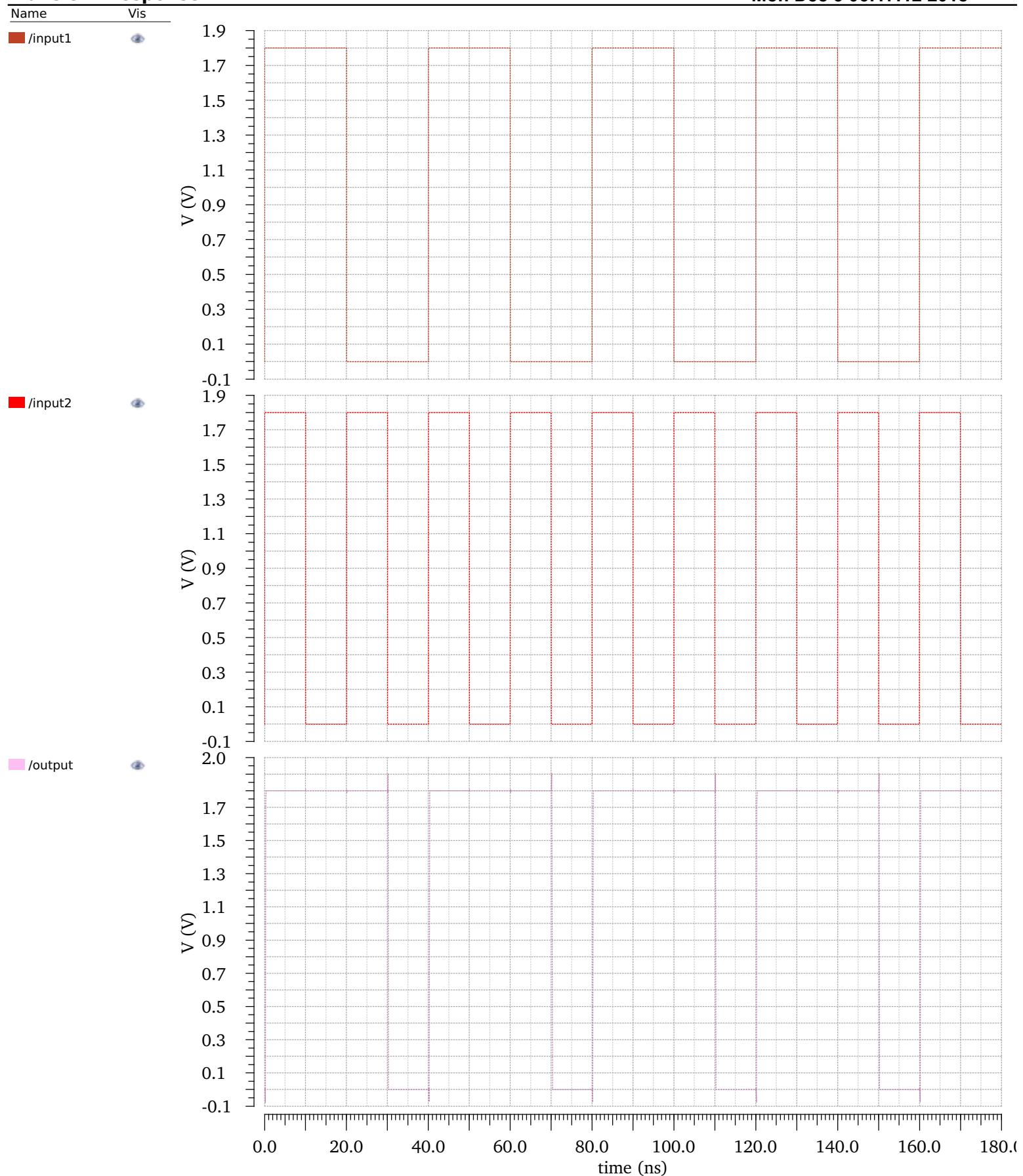


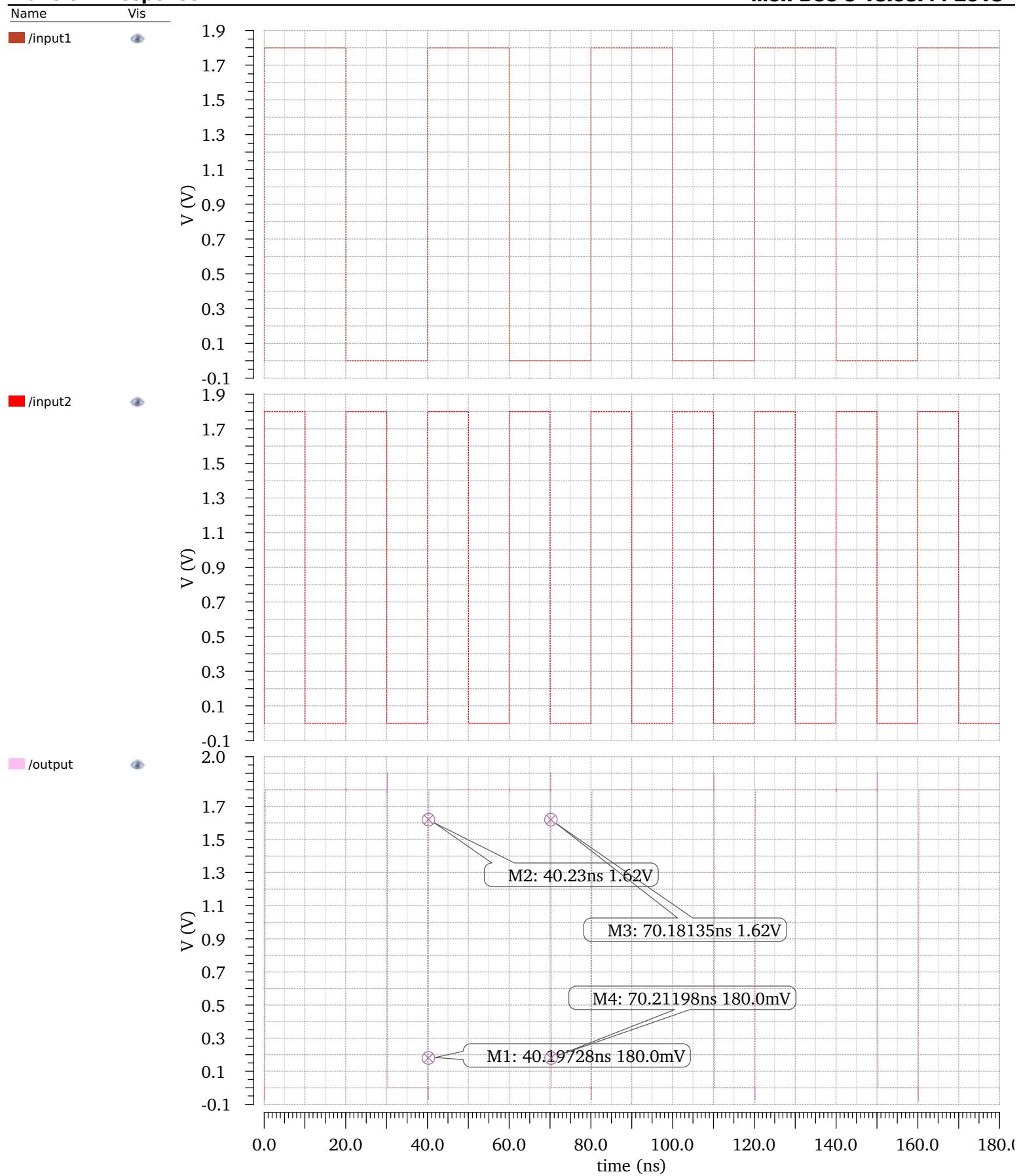
# TEST BENCH SCHEMATIC

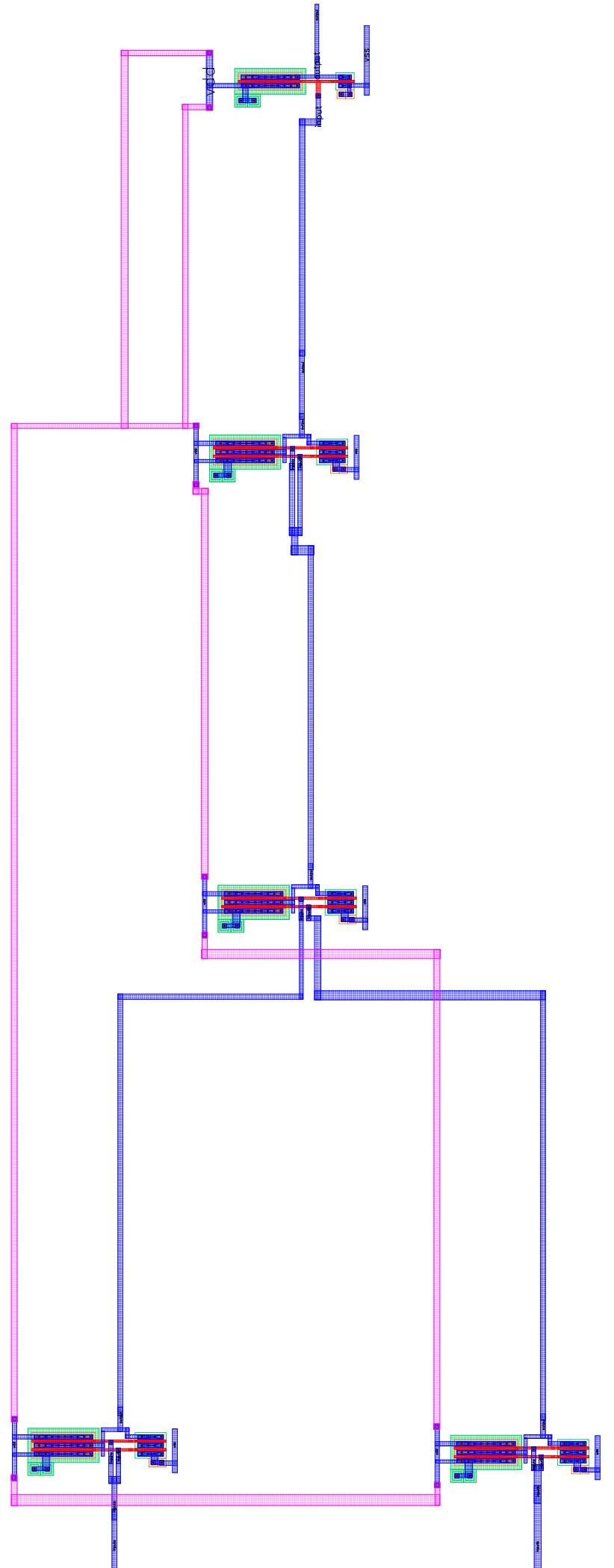


**Transient Response**

Mon Dec 3 06:17:12 2018



**Transient Response****Mon Dec 3 18:08:44 2018**



Virtuoso® 6.1.7-64b - Log: /gaia/class/student/junejad/CDS.log@thea.ecs.csus.edu

File Tools Options Help

cadence

```
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "0R4imp_layout layout" *****
Total errors found: 0
```

mouse L: showClickInfo()  
M: setDRCForm()  
R: \_JxHiMousePopUp()

```

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS
-dir /gaia/class/student/junejad/demo/LVS -l -s -t
/gaia/class/student/junejad/demo/LVS/layout
/gaia/class/student/junejad/demo/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/layout/netlist

count	
13	nets
0	terminals
9	pmos
9	nmos

Net-list summary for /gaia/class/student/junejad/demo/LVS/schematic/netlist

count	
-------	--

13	nets
5	terminals
9	pmos
9	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	18	18
total	18	18
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	13	13
total	13	13

	or lvs.txt	
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	0	5

Probe files from /gaia/class/student/junejad/demo/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/junejad/demo/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

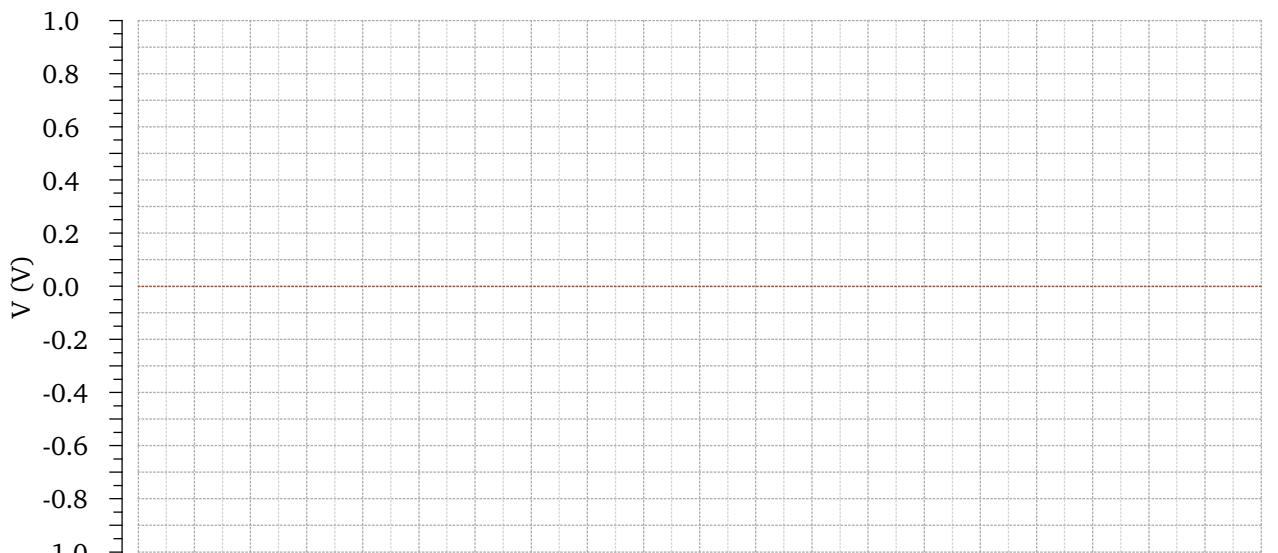
prunedev.out:

audit.out:

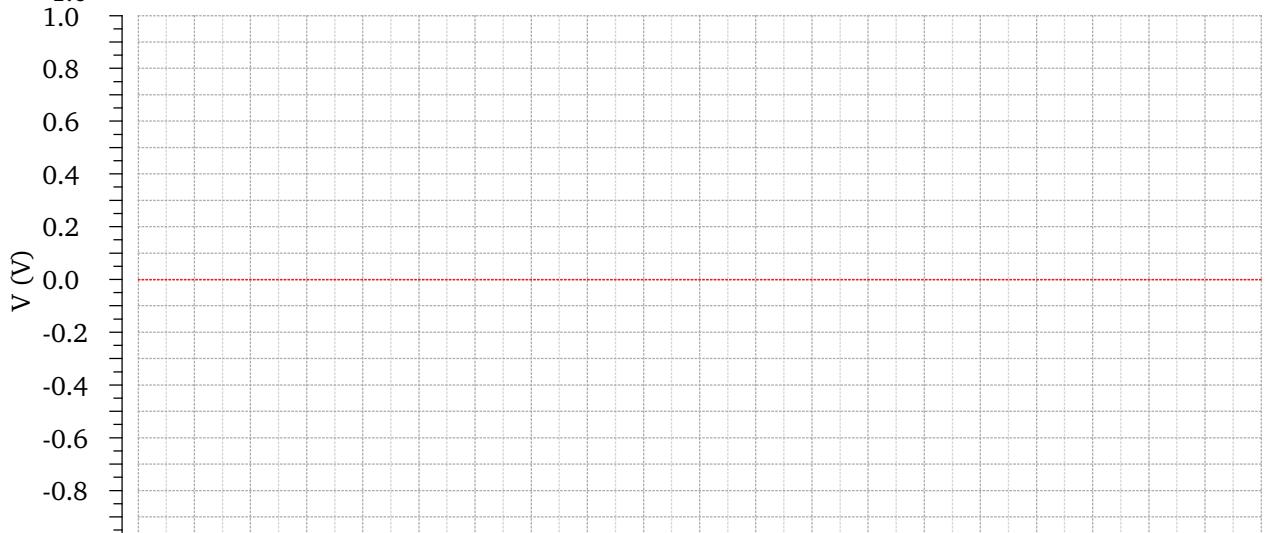
**DC Response****Fri Dec 07 02:52:04 2018**

Name Vis

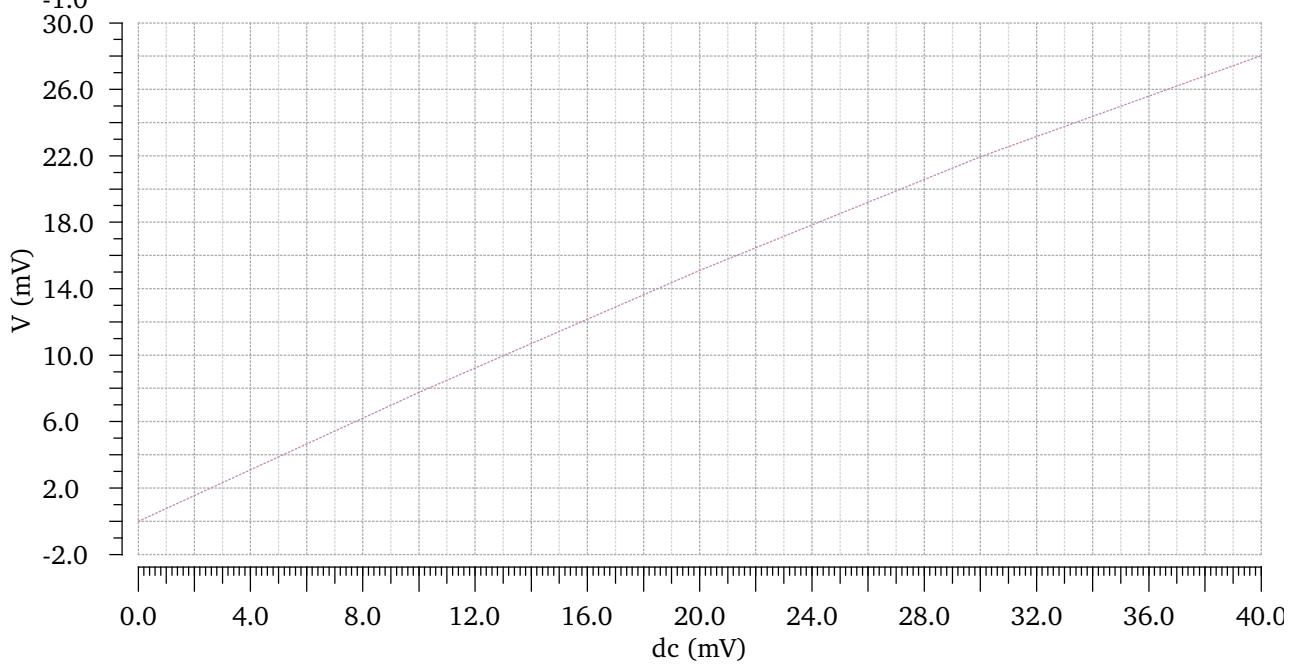
■ /input1



■ /input2

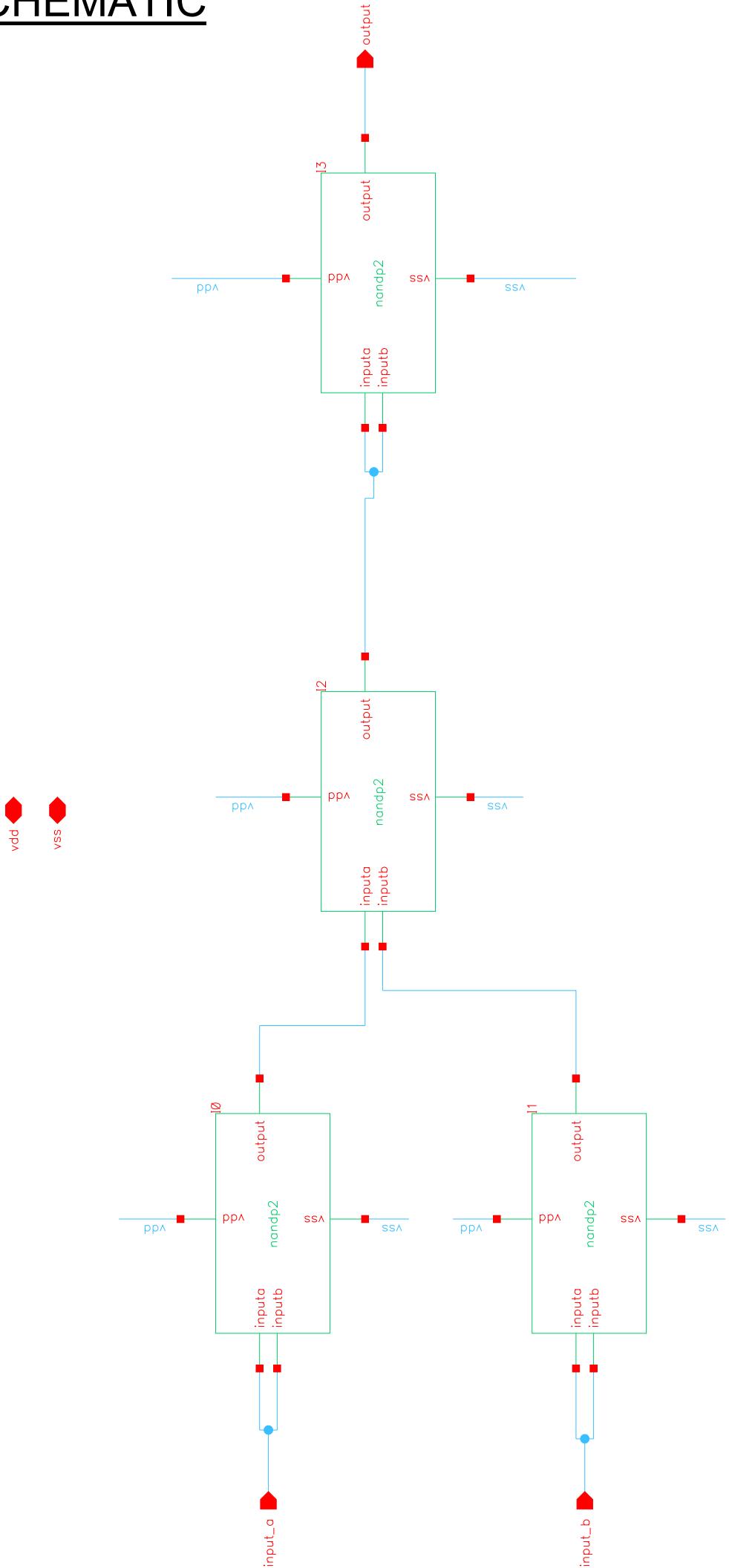


■ /output

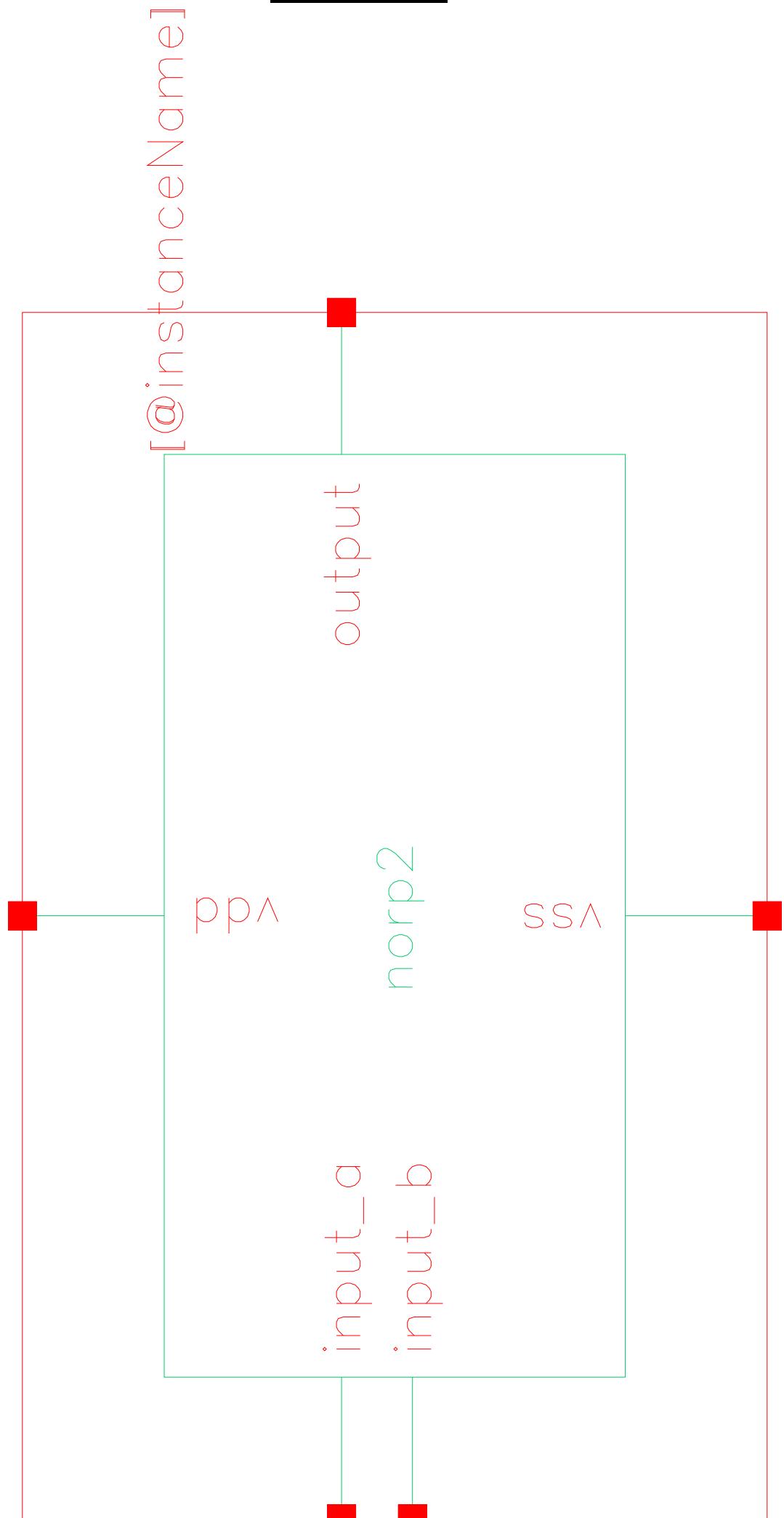


**NOR**

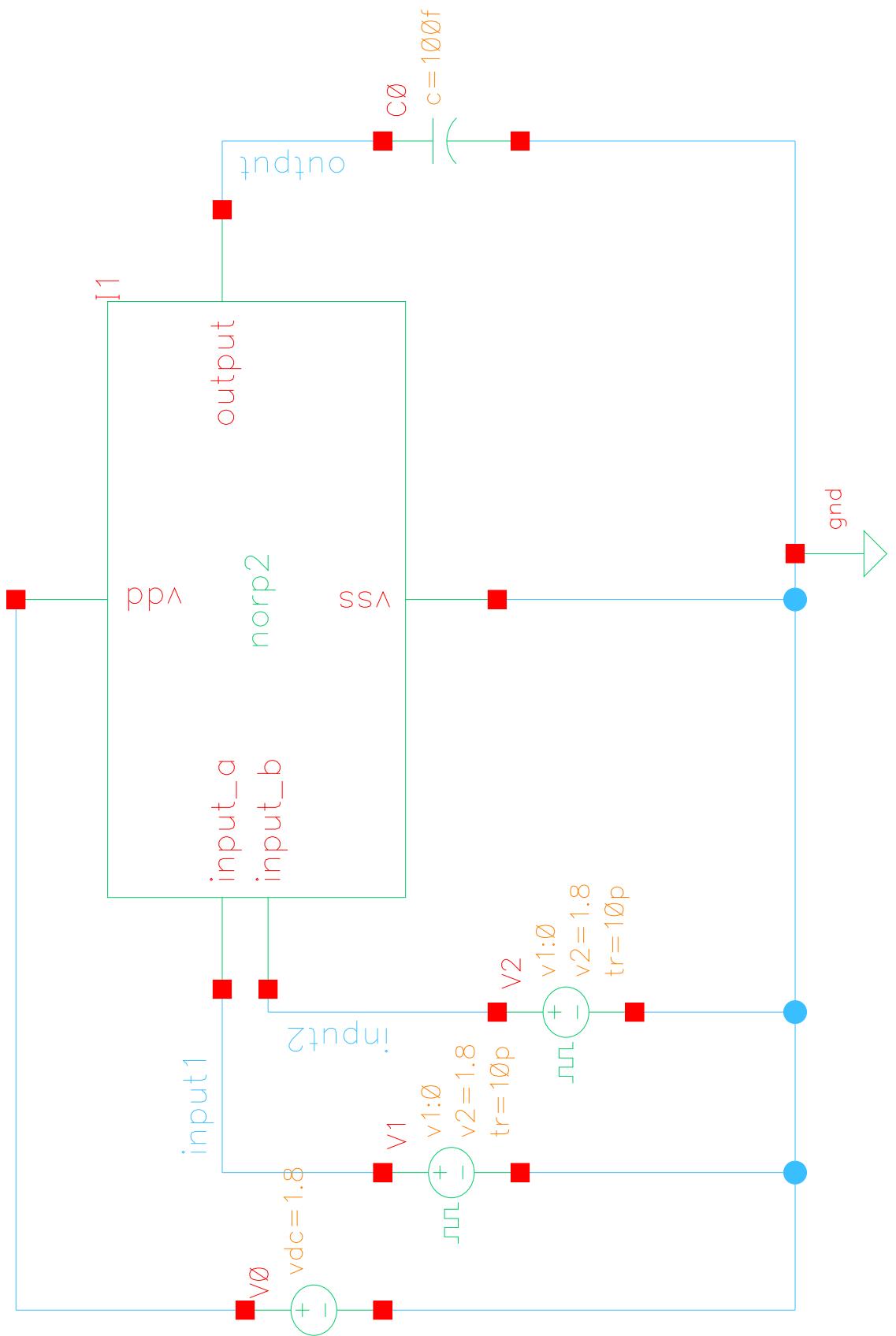
# SCHEMATIC

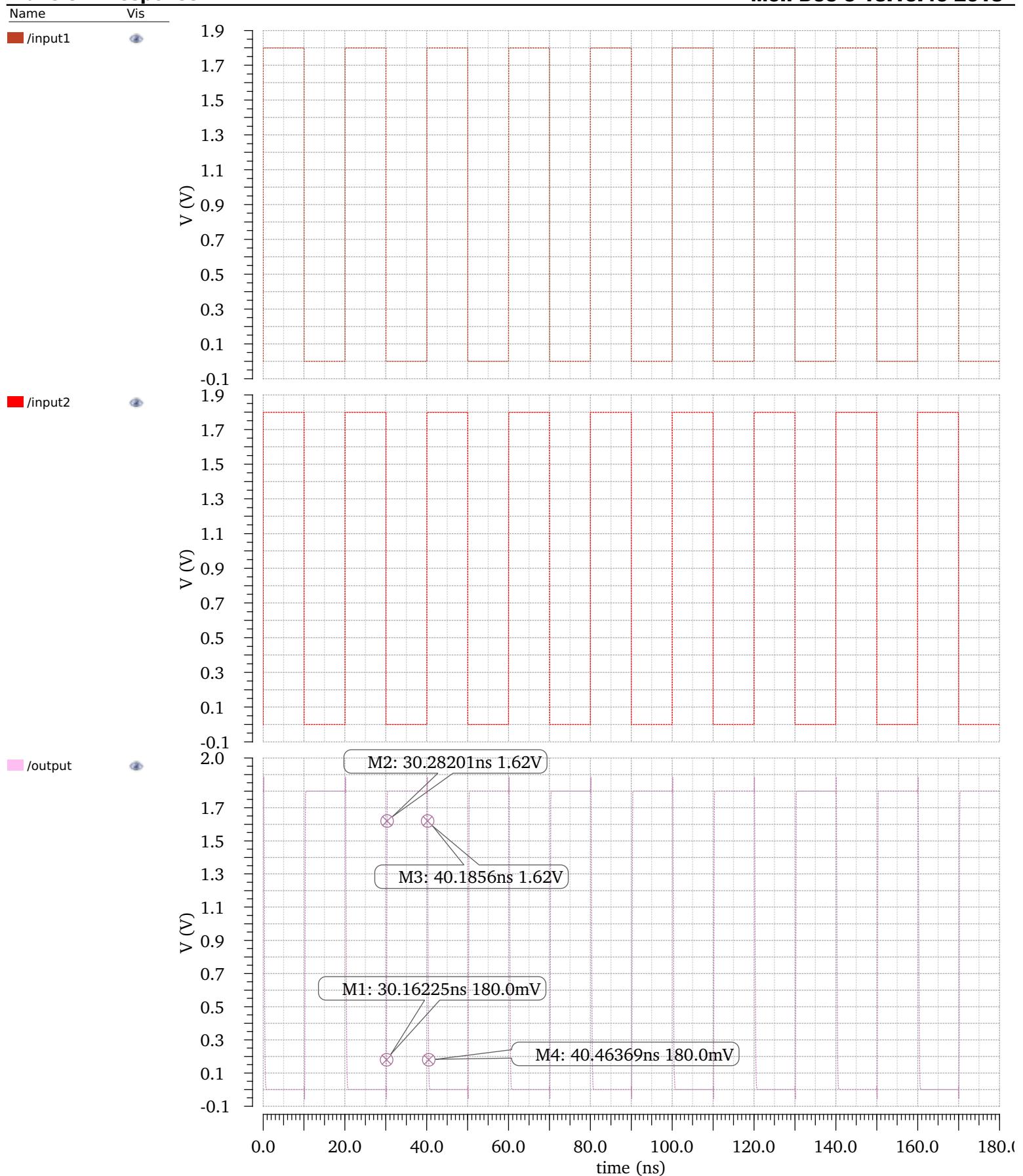


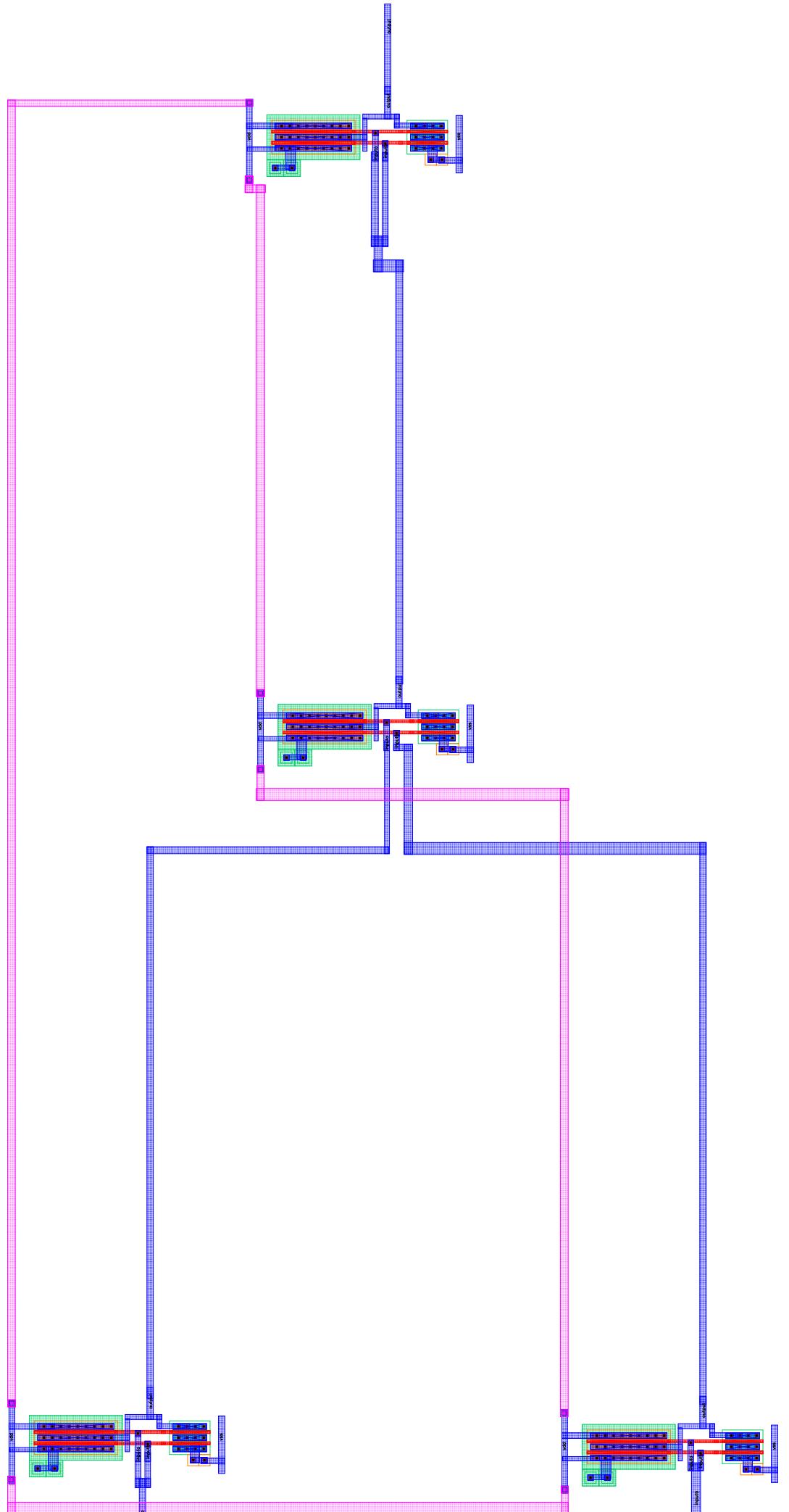
# SYMBOL



# TEST BENCH SCHEMATIC



**Transient Response****Mon Dec 3 18:13:46 2018**



Virtuoso® 6.1.7-64b - Log: /gaia/class/student/junejad/CDS.log.1@thea.ecs.csus.edu

File Tools Options Help

cadence

```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "NORG_L layout" *****
Total errors found: 0
```

mouse L: showClickInfo()  
M: setDRCForm()  
R: \_bxHiMousePopUp()

```

nor lvs.txt
@(#) $CDS: LVS version 6.1.7-64b 12/07/2018 19:41 (sjfhw305) $

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -
dir /gaia/class/student/junejad/demo/LVS -l -s -t
/gaia/class/student/junejad/demo/LVS/layout
/gaia/class/student/junejad/demo/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

```

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/layout/netlist
count
 12      nets
  0      terminals
  8      pmos
  8      nmos

```

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/schematic/netlist
count
 12      nets
  5      terminals
  8      pmos
  8      nmos

```

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	16	16
total	16	16
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	12	12
total	12	12

	nor lvs.txt	terminals
un-matched	0	0
matched but different type	0	0
total	0	5

Probe files from /gaia/class/student/junejad/demo/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/junejad/demo/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

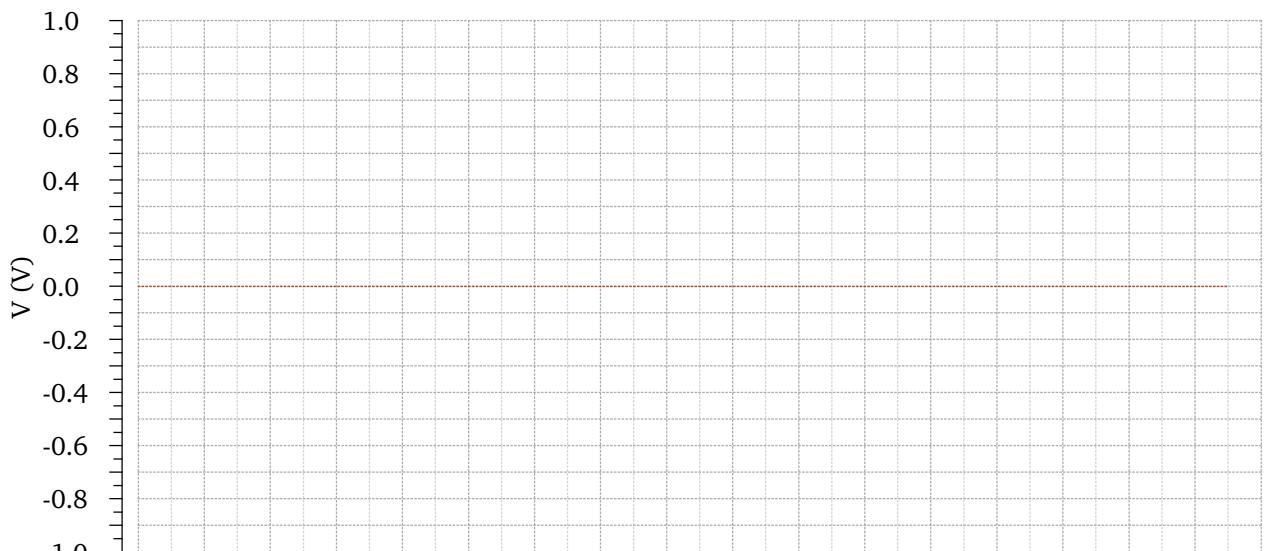
prunedev.out:

audit.out:

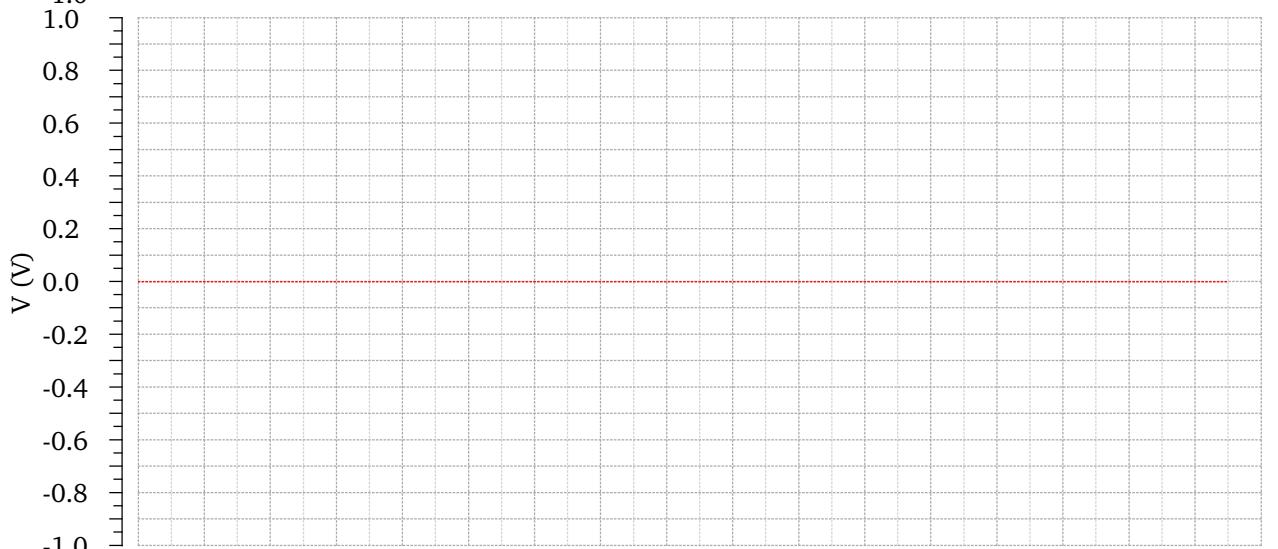
**DC Response****Fri Dec 07 03:19:00 2018**

Name Vis

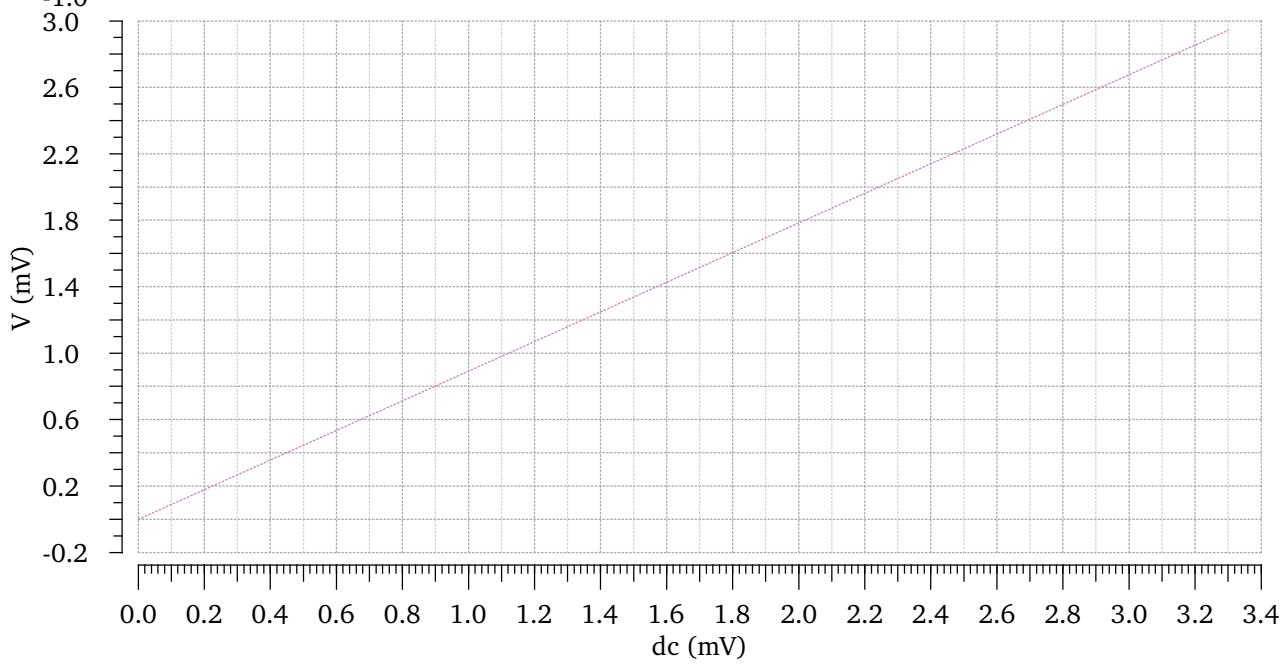
■ /input1



■ /input2

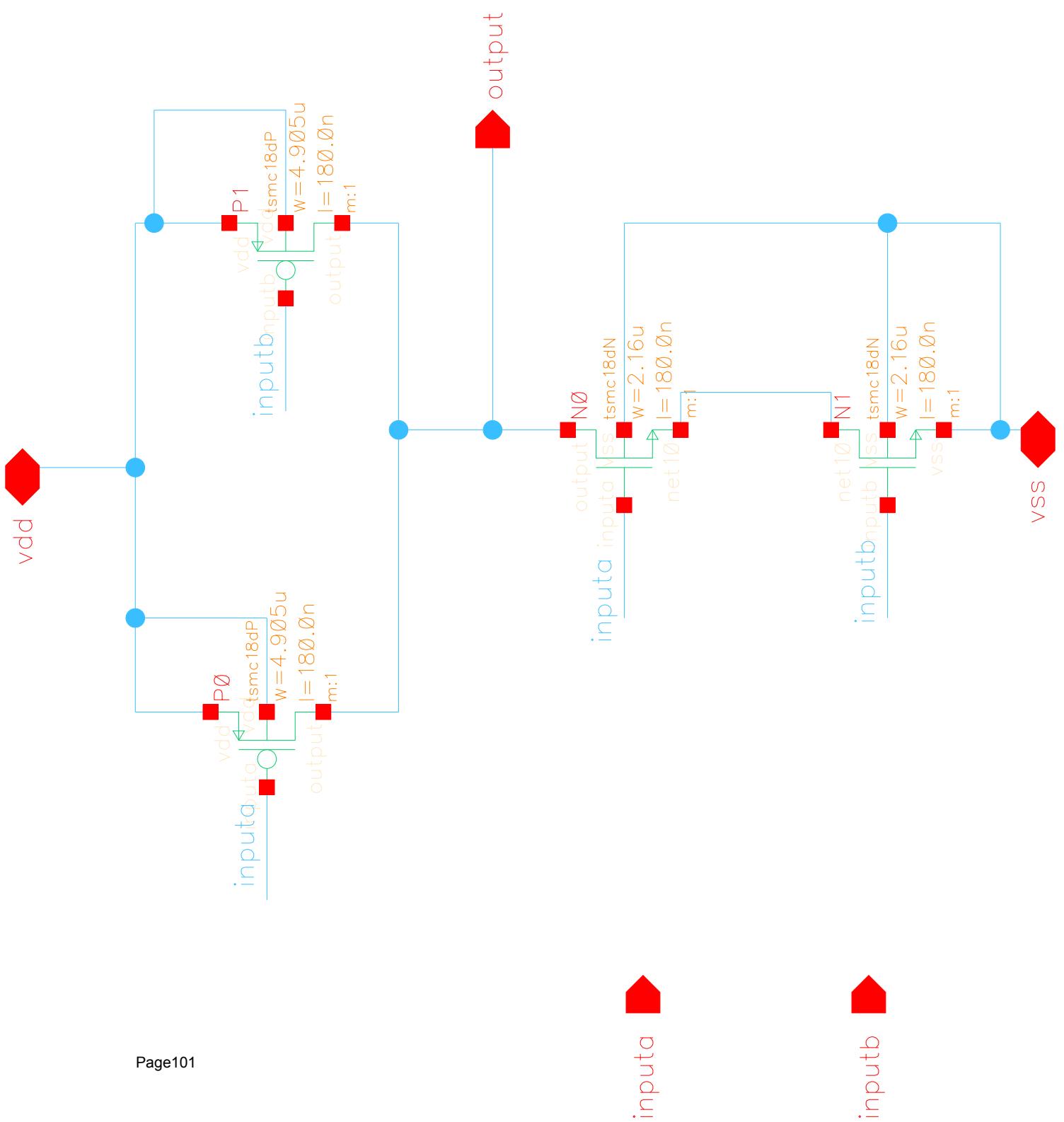


■ /output

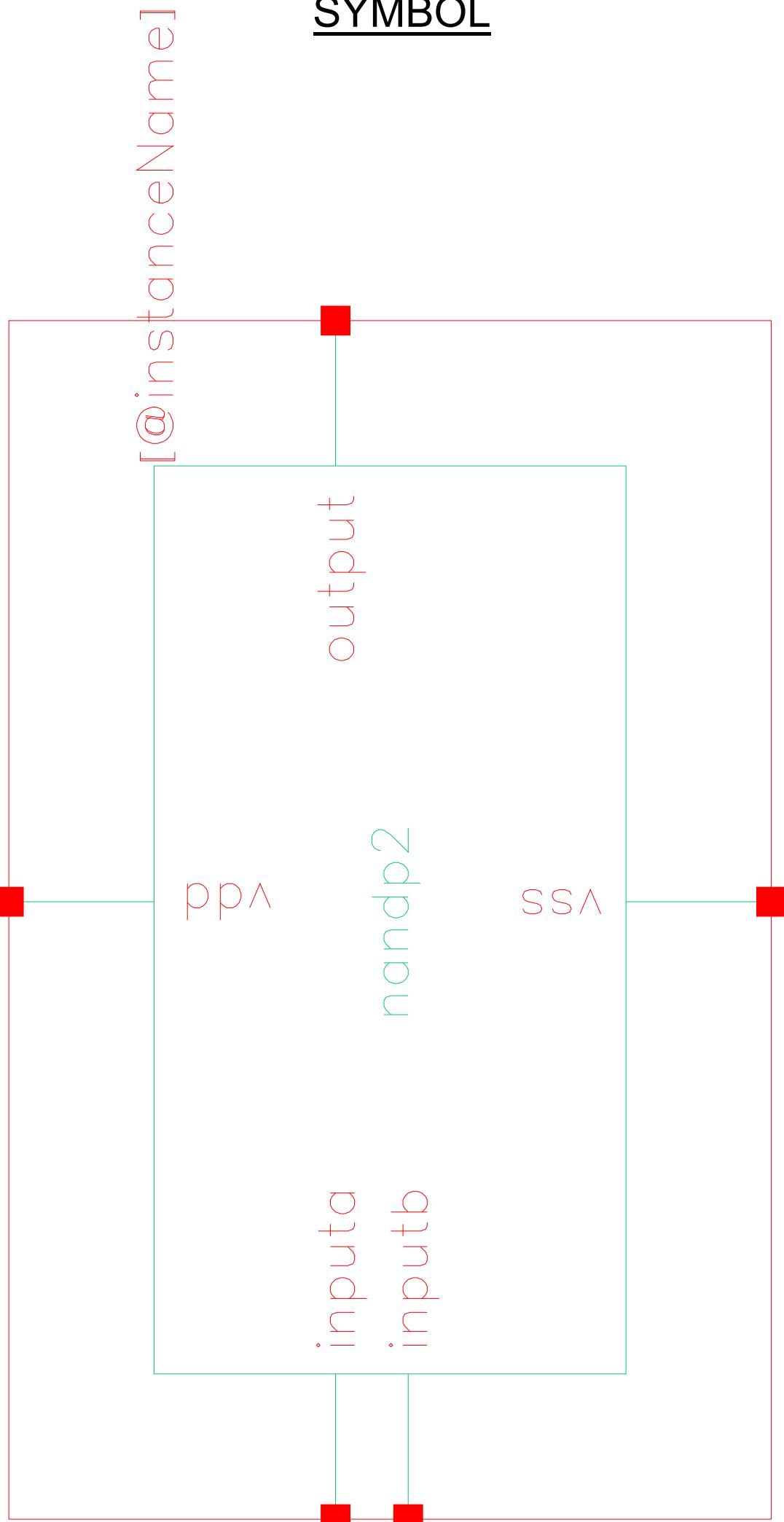


**NAND**

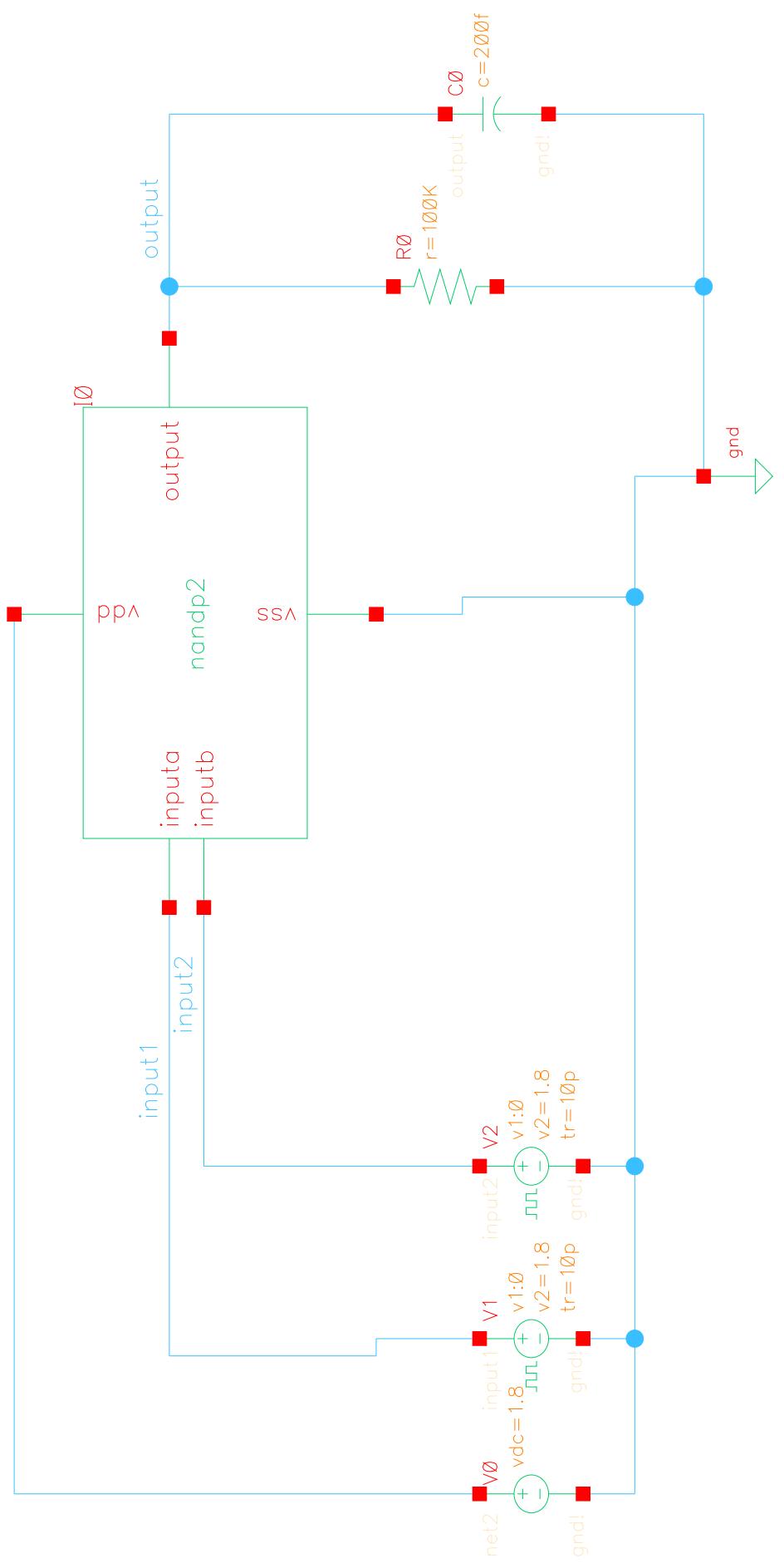
# SCHEMATIC

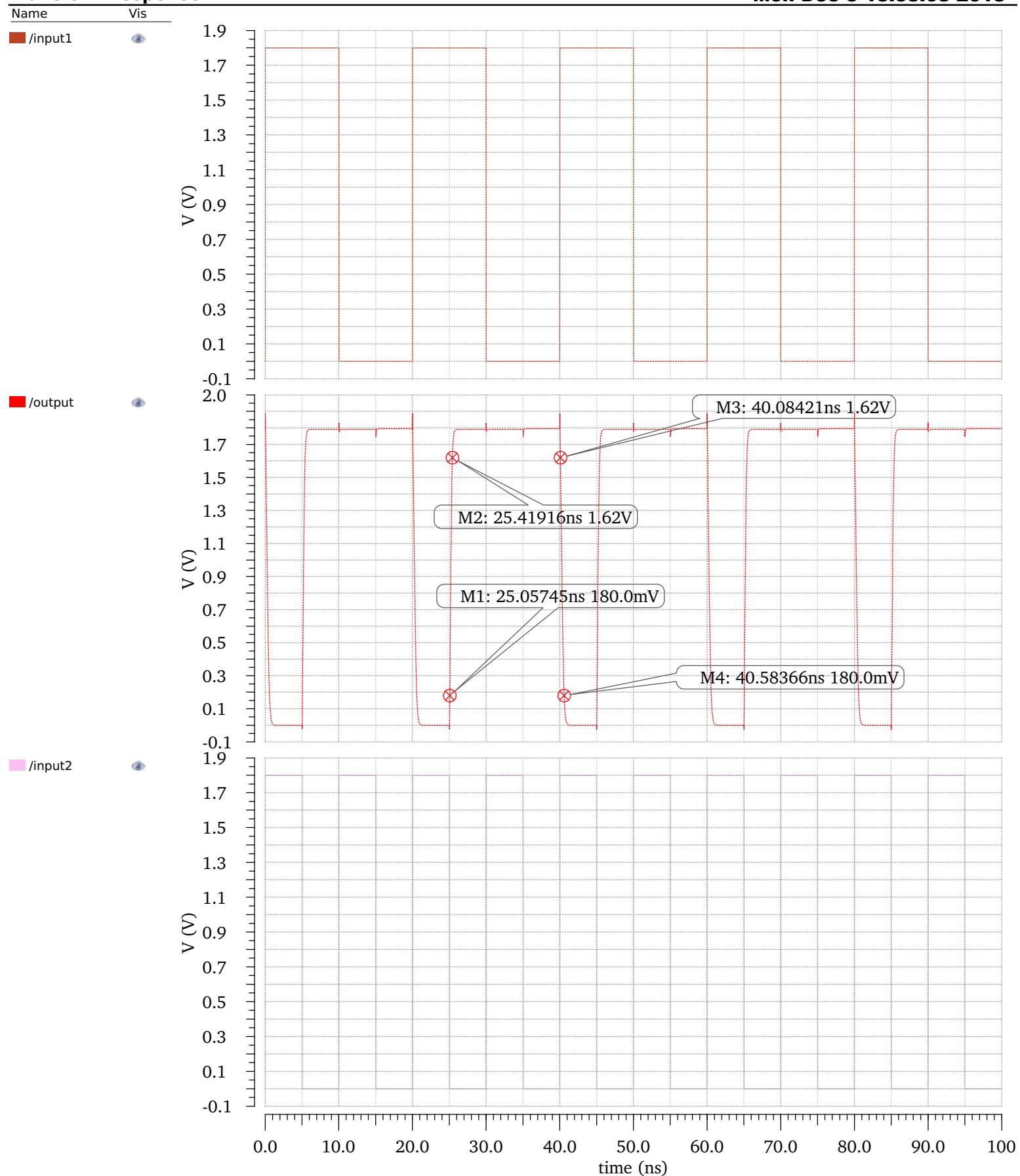


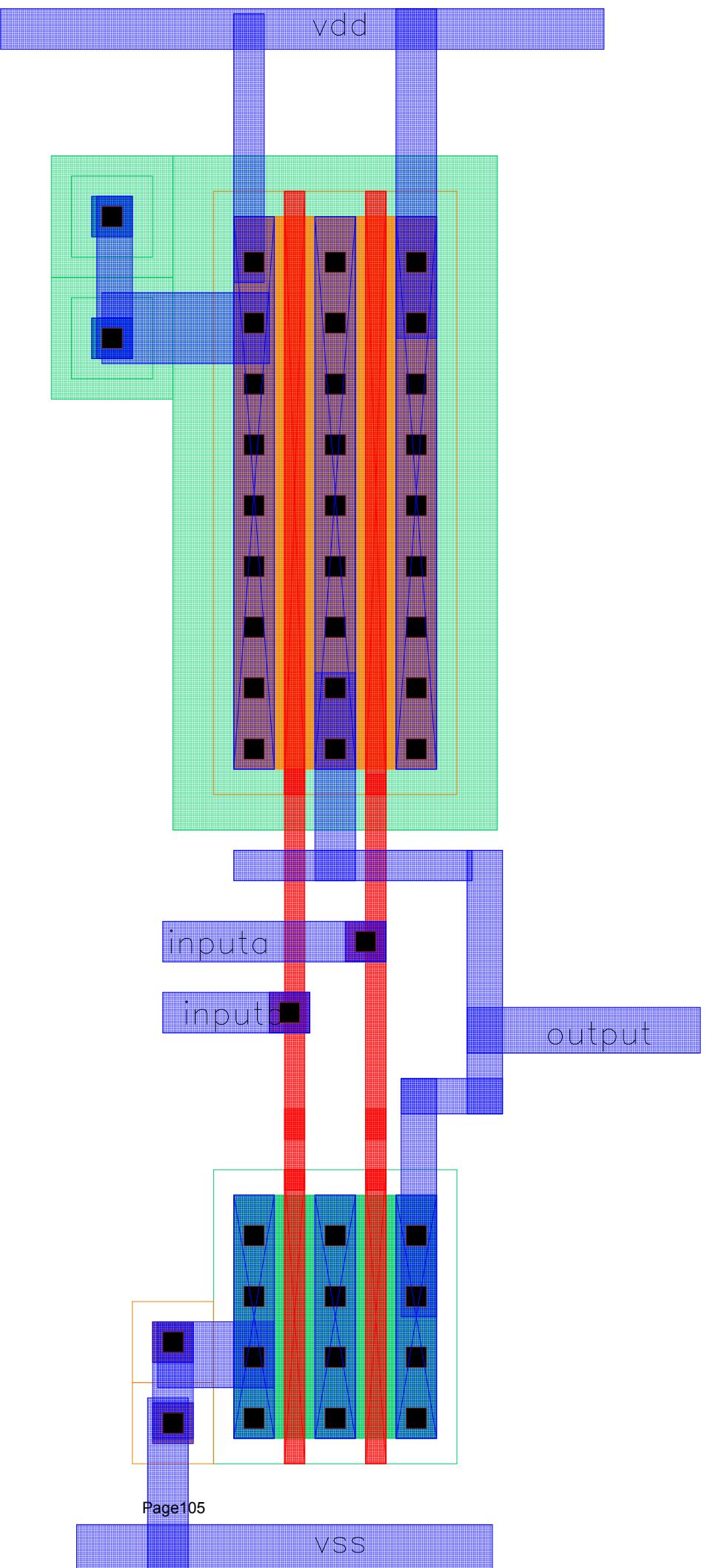
# SYMBOL



# TEST BENCH SCHEMATIC



**Transient Response****Mon Dec 3 18:38:08 2018**



File Tools Options Help

```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "2inNAND_layout layout" *****
Total errors found: 0
```

mouse L: showClickInfo()

M: setDRCForm()

R: \_lxHiMousePopUp()

1 | >

```

nand lvs.txt
@(#) $CDS: LVS version 6.1.7-64b 12/07/2018 19:41 (sjfhw305) $

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -
dir /gaia/class/student/junejad/demo/LVS -l -s -t
/gaia/class/student/junejad/demo/LVS/layout
/gaia/class/student/junejad/demo/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

```

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/layout/netlist
count
 6      nets
 0      terminals
 2      pmos
 2      nmos

```

```

Net-list summary for /gaia/class/student/junejad/demo/LVS/schematic/netlist
count
 6      nets
 5      terminals
 2      pmos
 2      nmos

```

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	4	4
total	4	4
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	6	6
total	6	6

	nand	lvs.txt
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	0	5

Probe files from /gaia/class/student/junejad/demo/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/junejad/demo/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

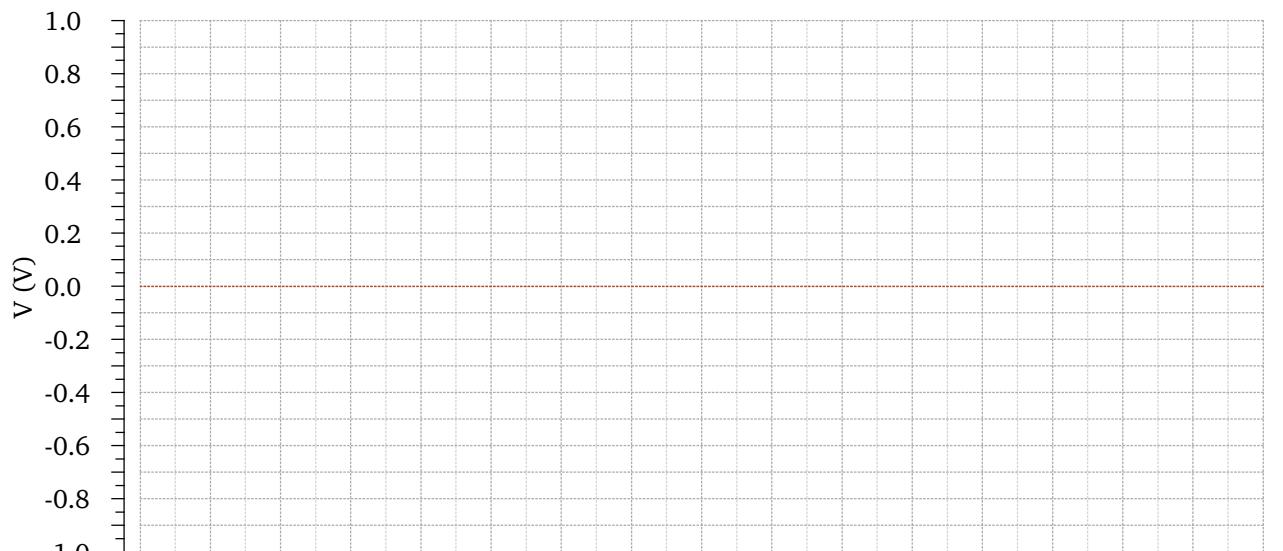
prunedev.out:

audit.out:

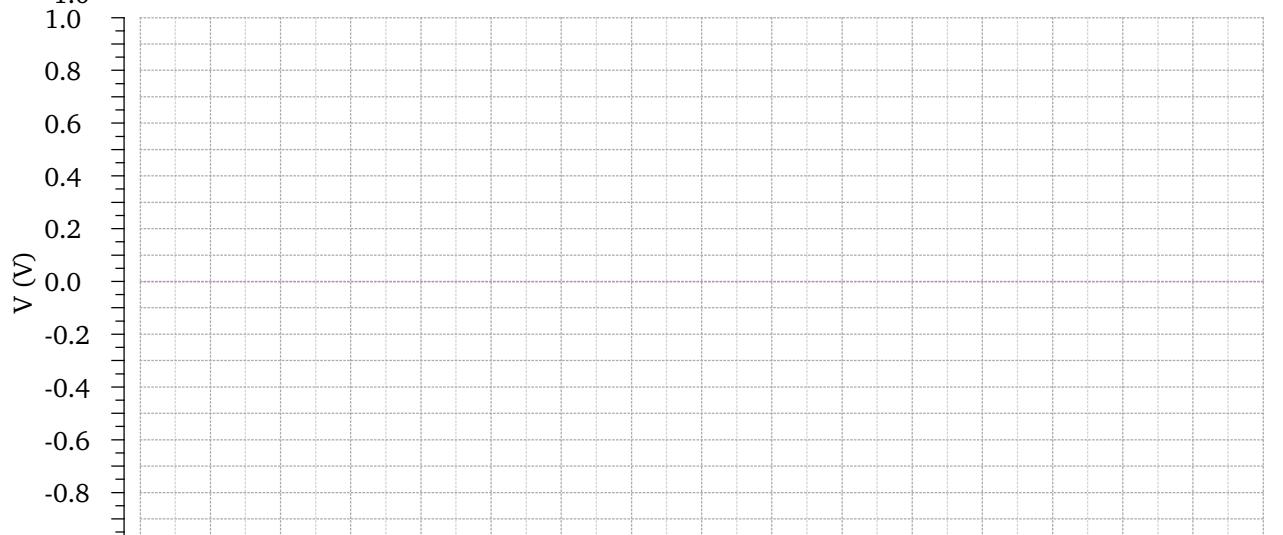
**DC Response****Fri Dec 07 03:28:13 2018**

Name Vis

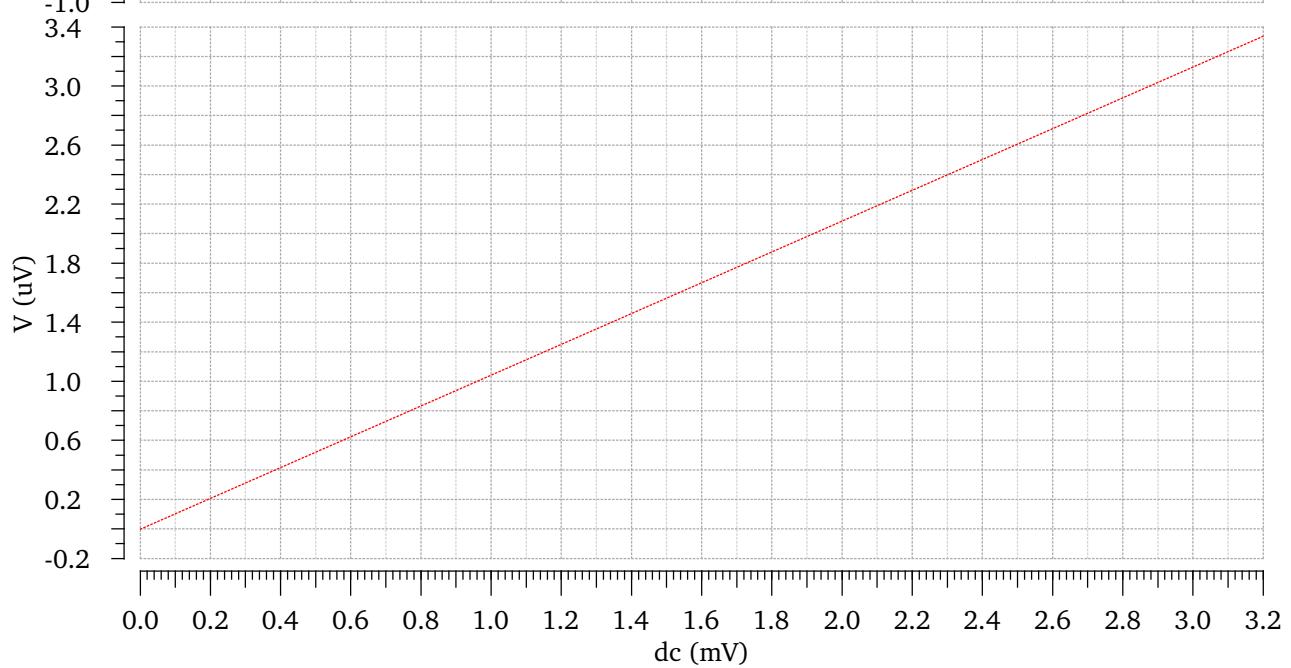
■ /input1



■ /input2



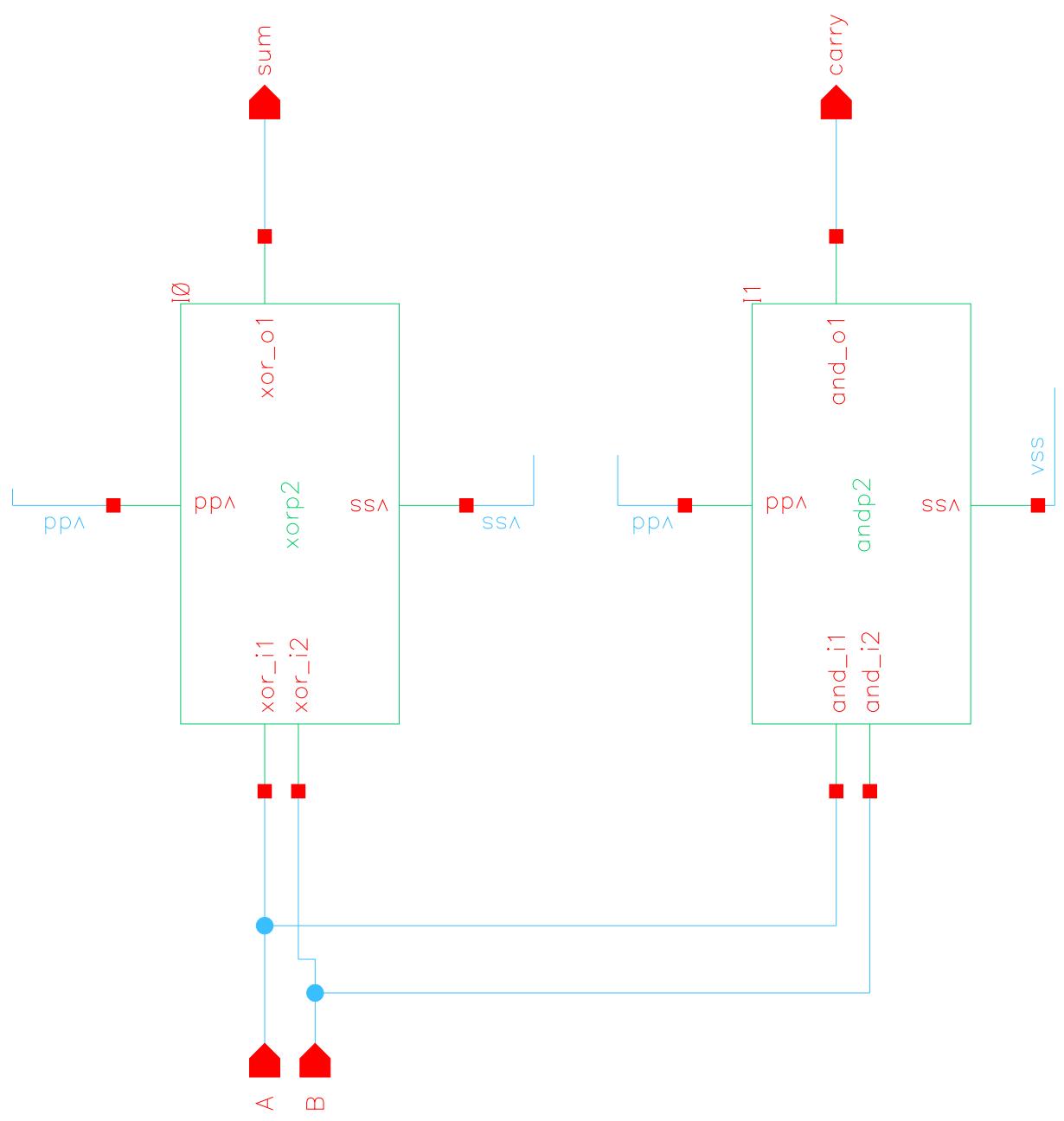
■ /output



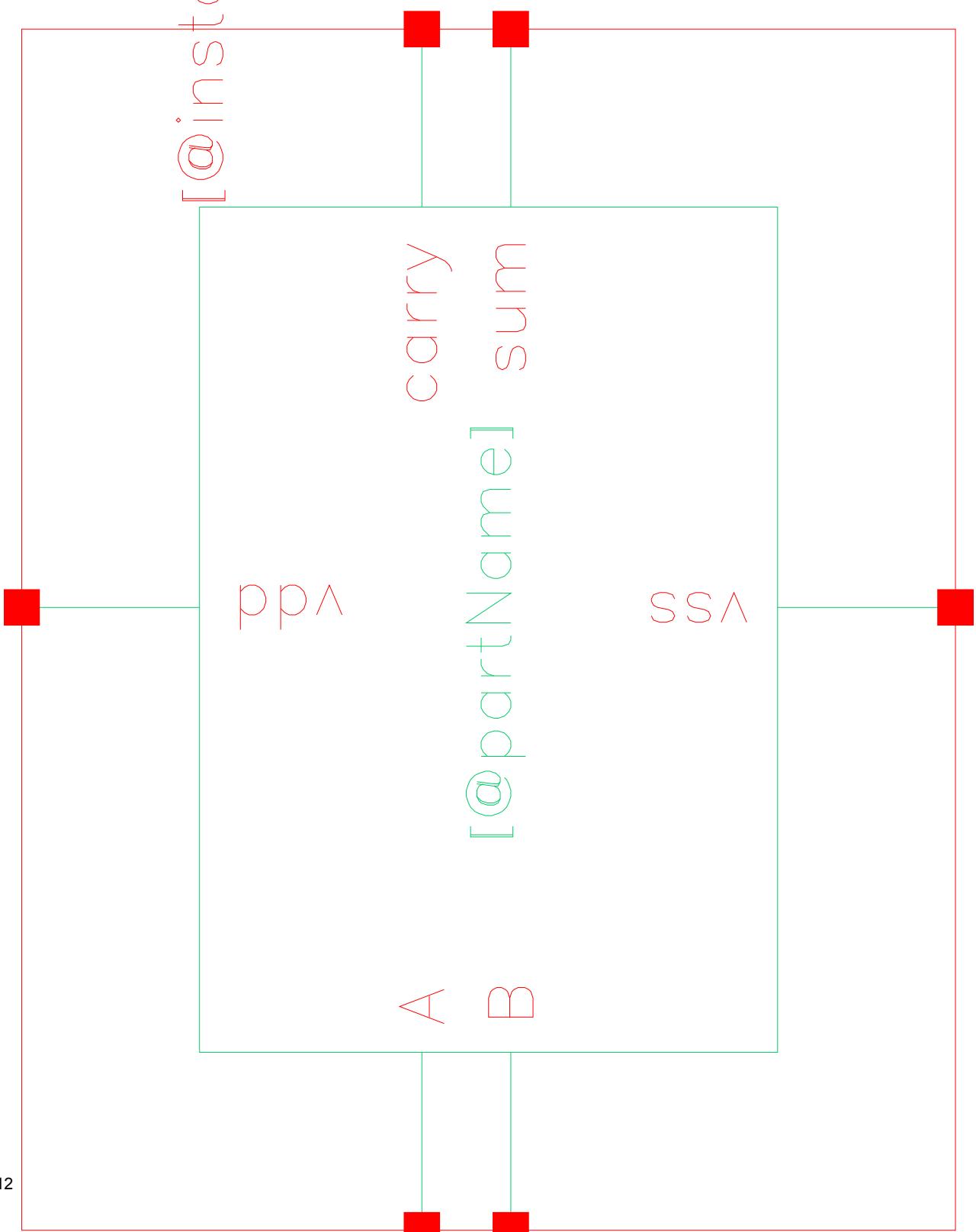
# **HALF ADDER**

# SCHEMATIC

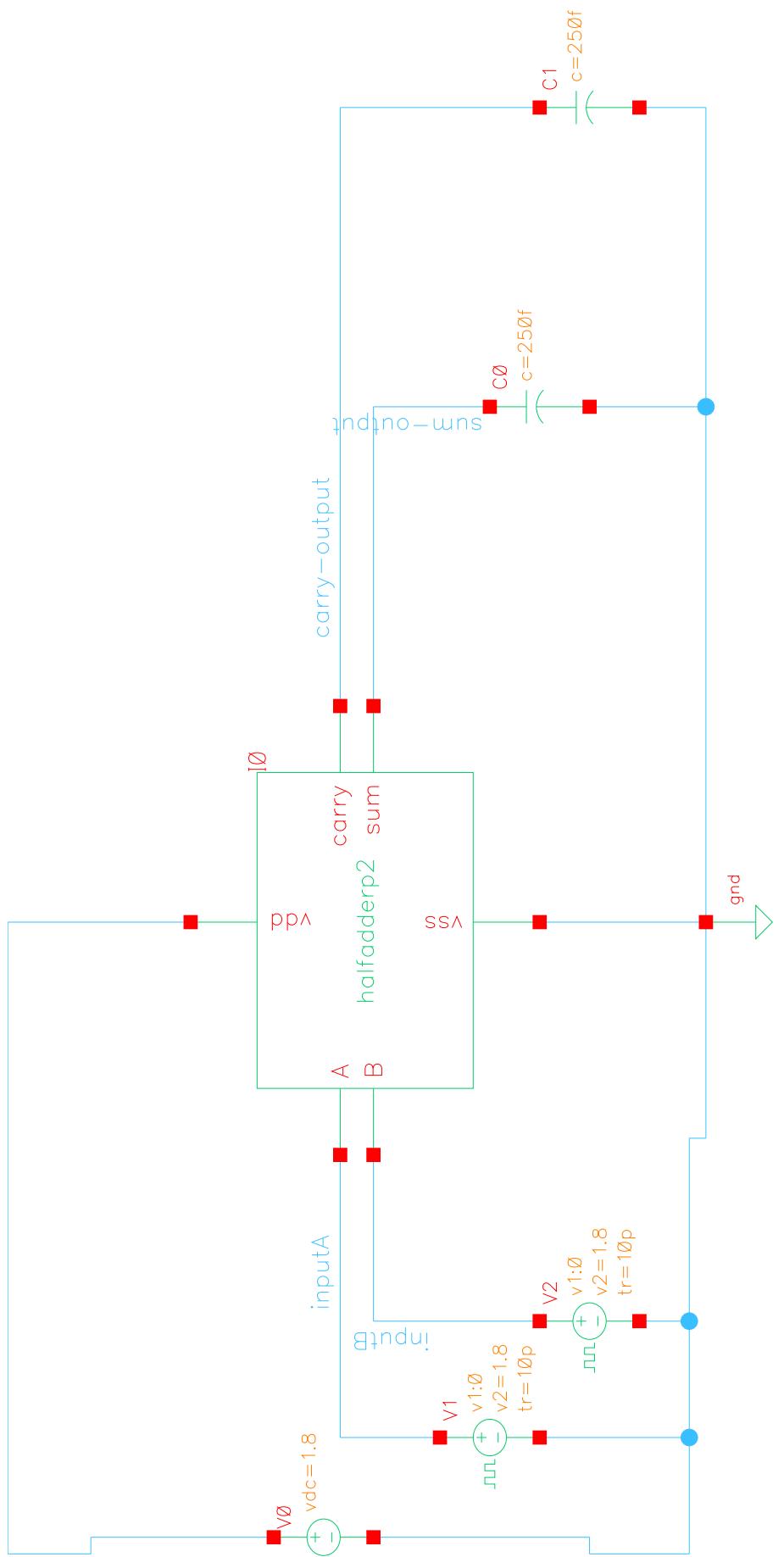
vdd  
vss

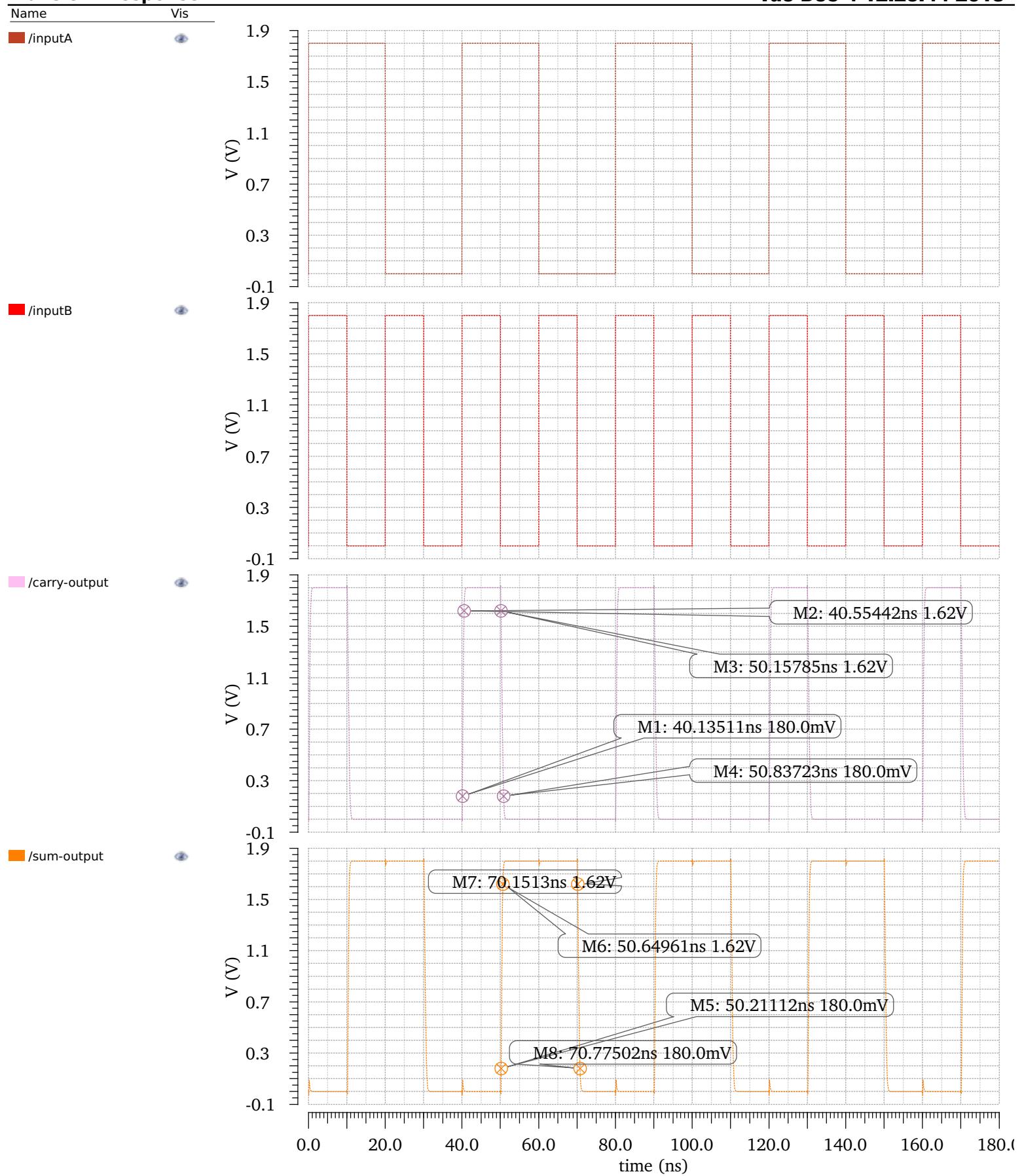


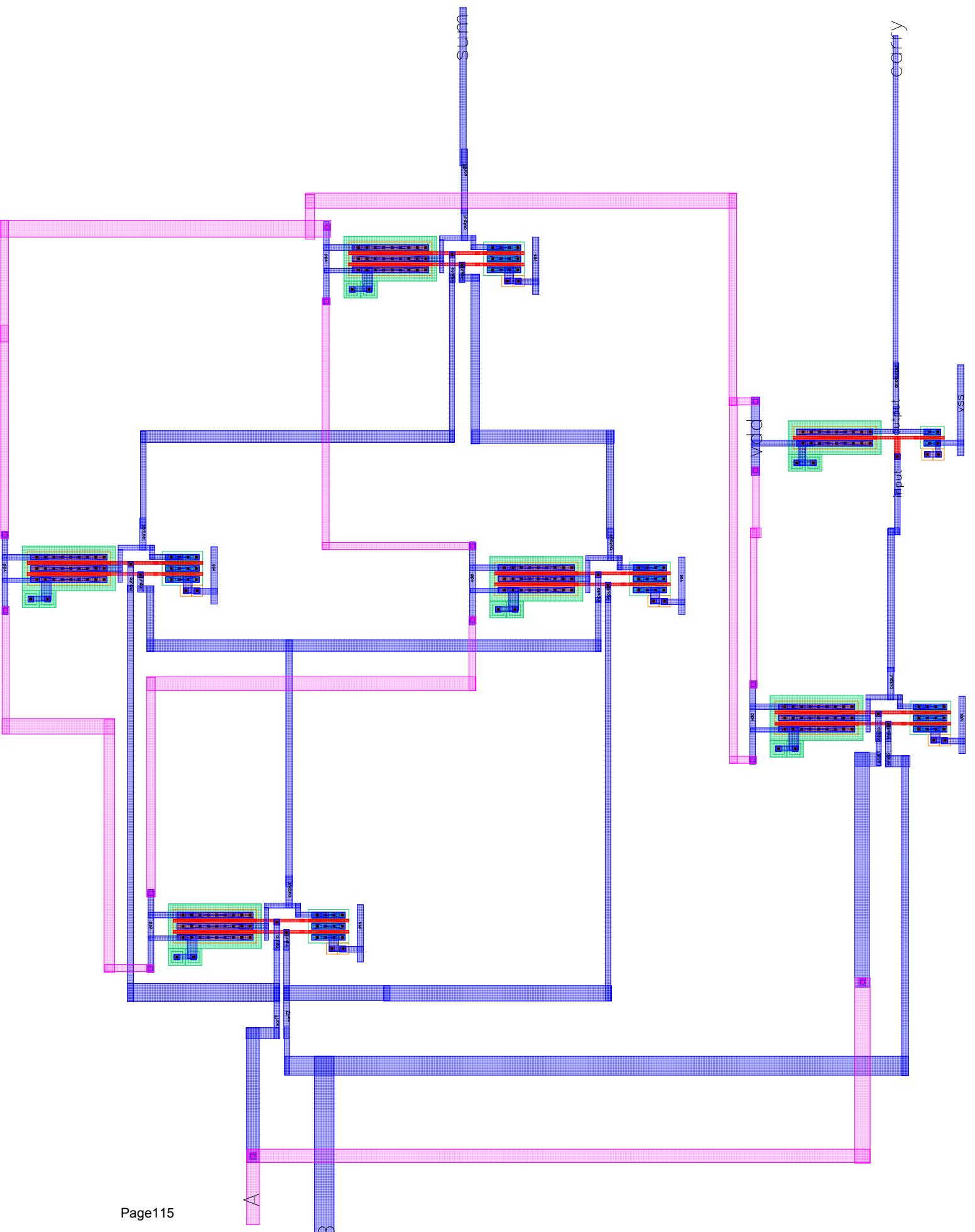
# SYMBOL



# TEST BENCH SCHEMATIC



**Transient Response****Tue Dec 4 12:23:44 2018**



Virtuoso® 6.1.7-64b - Log: /gaia/class/student/junejad/CDS.log@thea.ecs.csus.edu

File Tools Options Help

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00  
\*\*\*\*\* Summary of rule violations for cell "HalfAdder\_layout layout" \*\*\*\*\*  
Total errors found: 0

mouse L: showClickInfo() M: setDRCForm() R: \_JxHiMousePopUp()  
1 >

```
@(#)$CDS: LVS version 6.1.7-64b 12/07/2018 19:41 (sjfhw305) $
```

```
Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS  
-dir /gaia/class/student/junejad/demo/LVS -l -s -t  
/gaia/class/student/junejad/demo/LVS/layout  
/gaia/class/student/junejad/demo/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.
```

```
Net-list summary for /gaia/class/student/junejad/demo/LVS/layout/netlist
```

```
count  
15      nets  
0       terminals  
11      pmos  
11      nmos
```

```
Net-list summary for /gaia/class/student/junejad/demo/LVS/schematic/netlist  
count  
15      nets  
6       terminals  
11      pmos  
11      nmos
```

```
Devices in the netlist but not in the rules:  
pmos nmos
```

```
The net-lists match.
```

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	22	22
total	22	22

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	15	15
total	15	15

	terminals	
un-matched	0	0
matched but		

	halfadder lvs.txt	
different type	0	0
total	0	6

Probe files from /gaia/class/student/junejad/demo/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/junejad/demo/LVS/layout

devbad.out:

netbad.out:

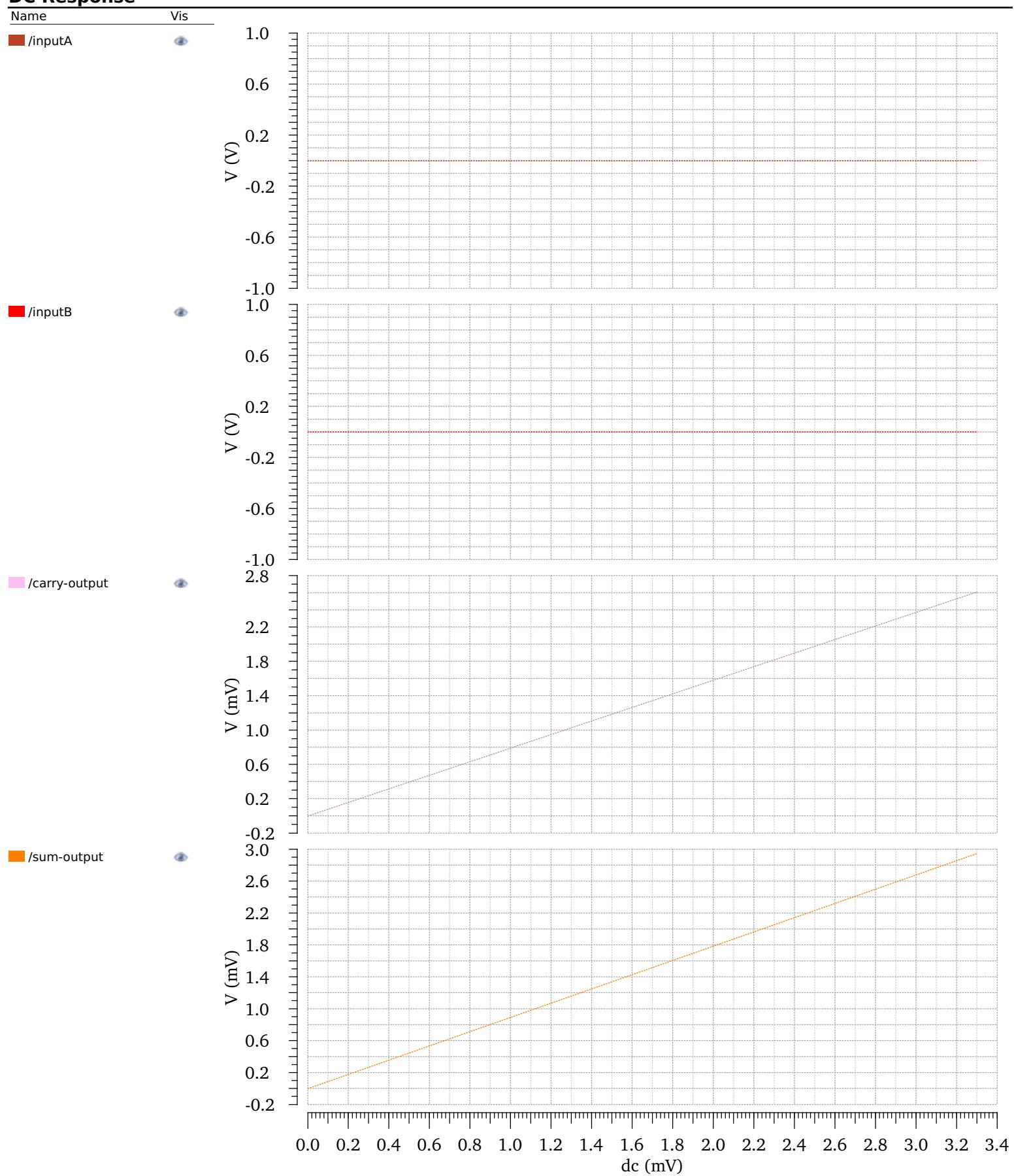
mergenet.out:

termbad.out:

prunenet.out:

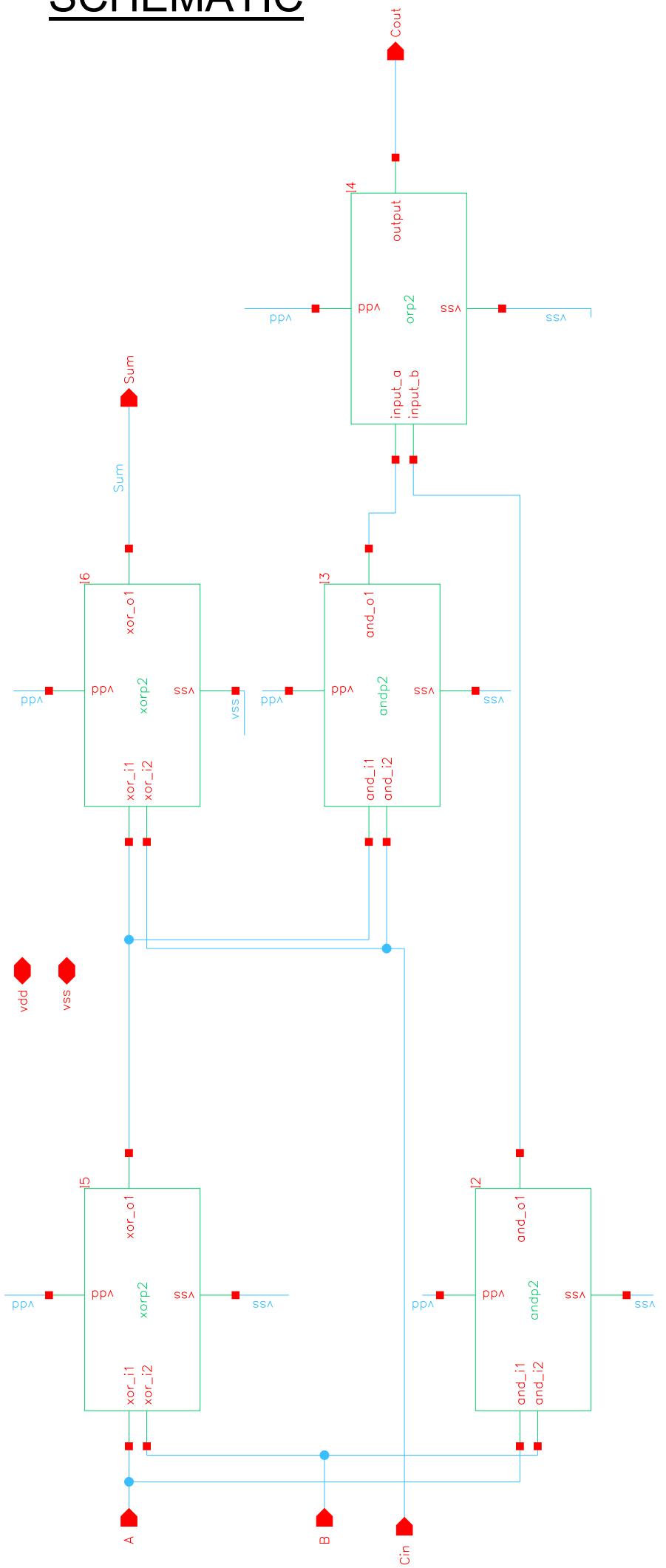
prunedev.out:

audit.out:

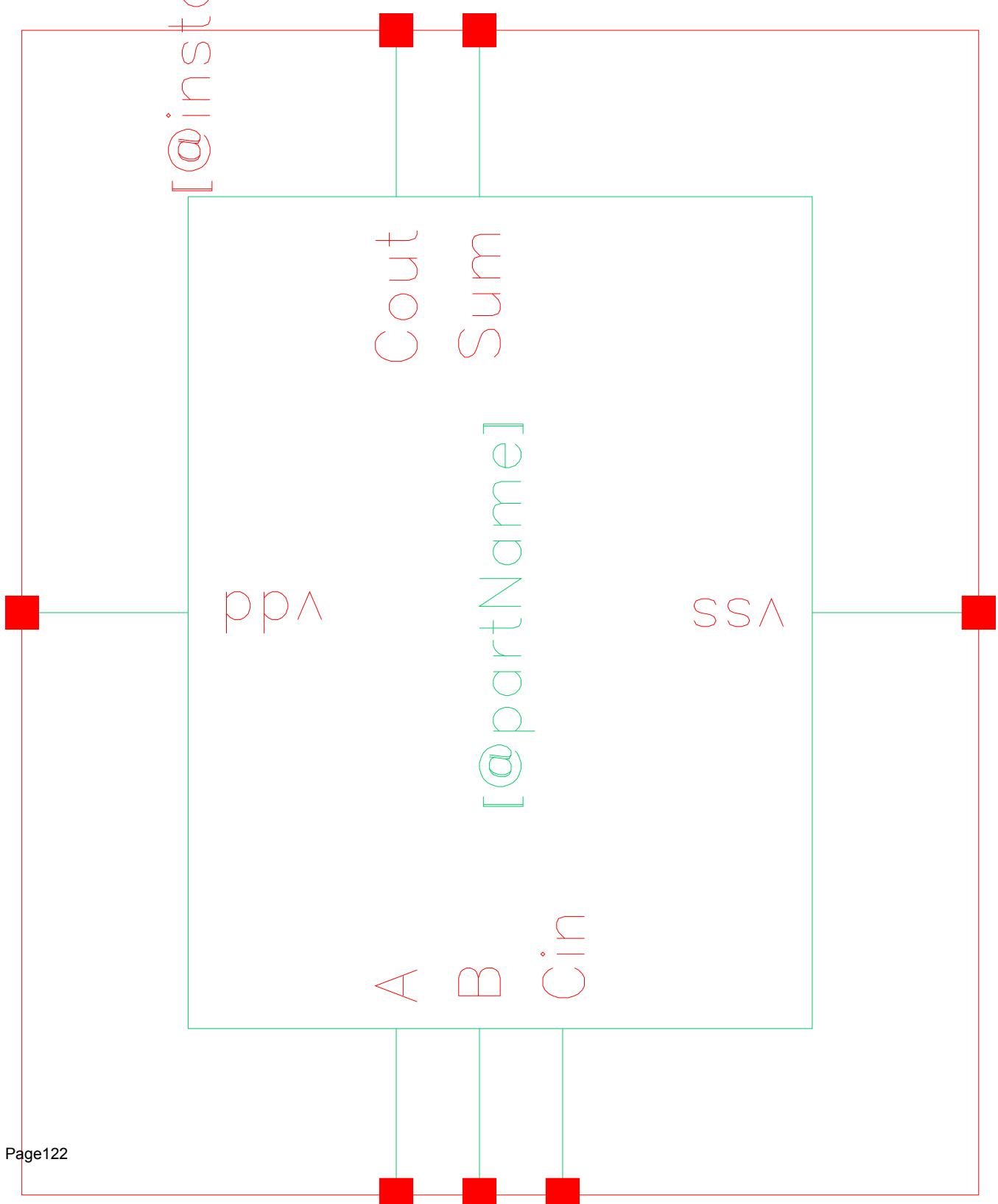
**DC Response****Fri Dec 7 03:43:42 2018**

# **FULL ADDER**

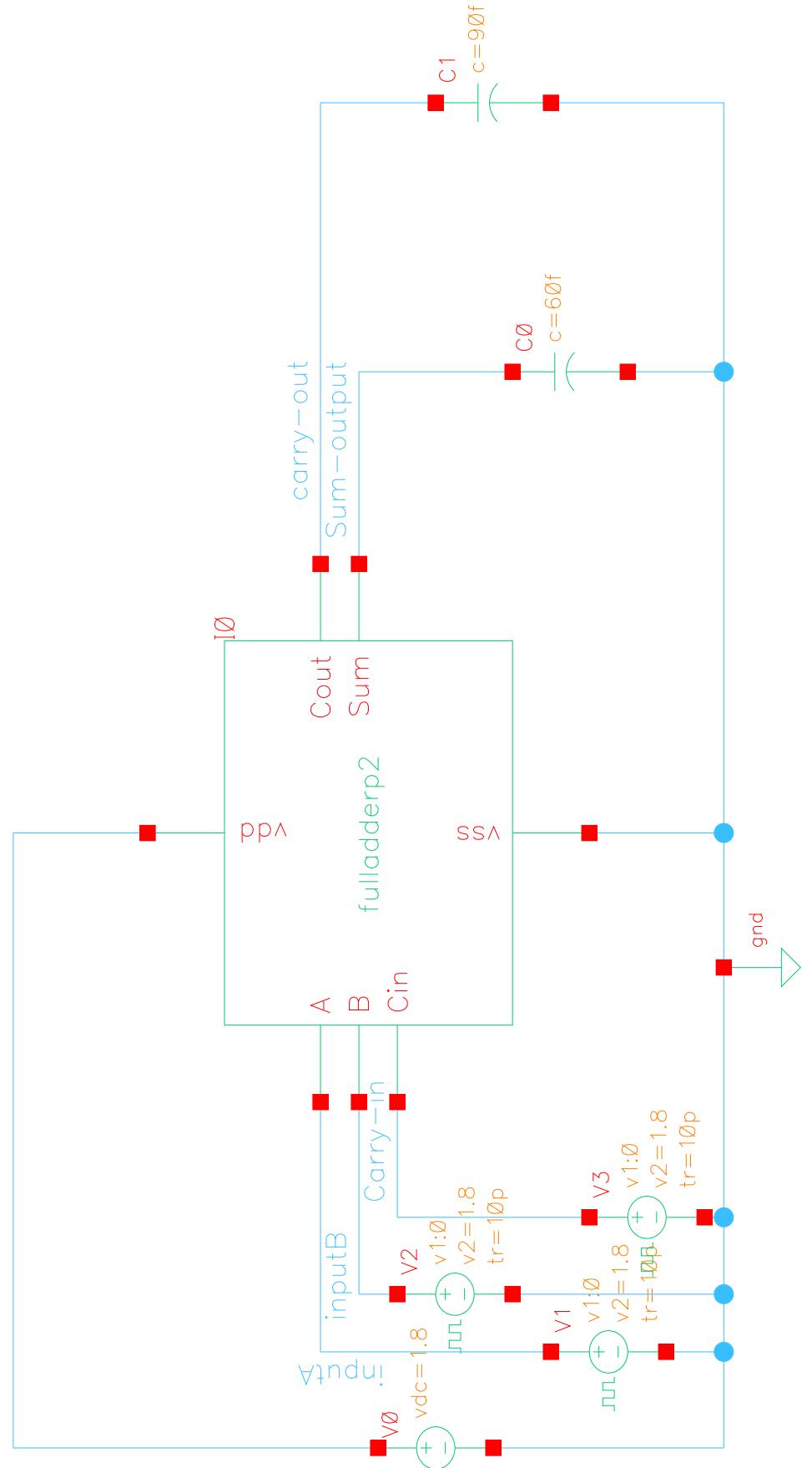
# SCHEMATIC

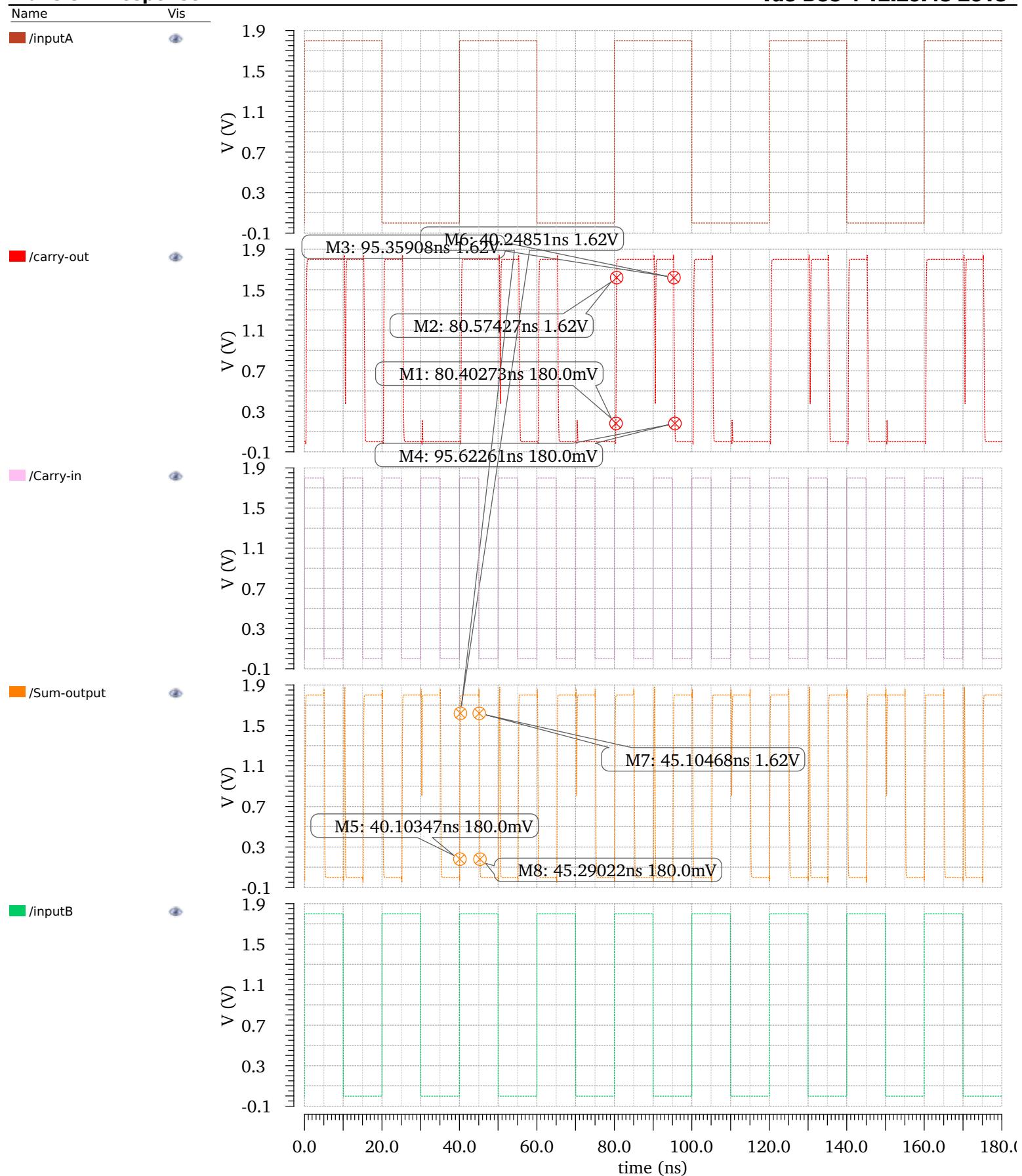


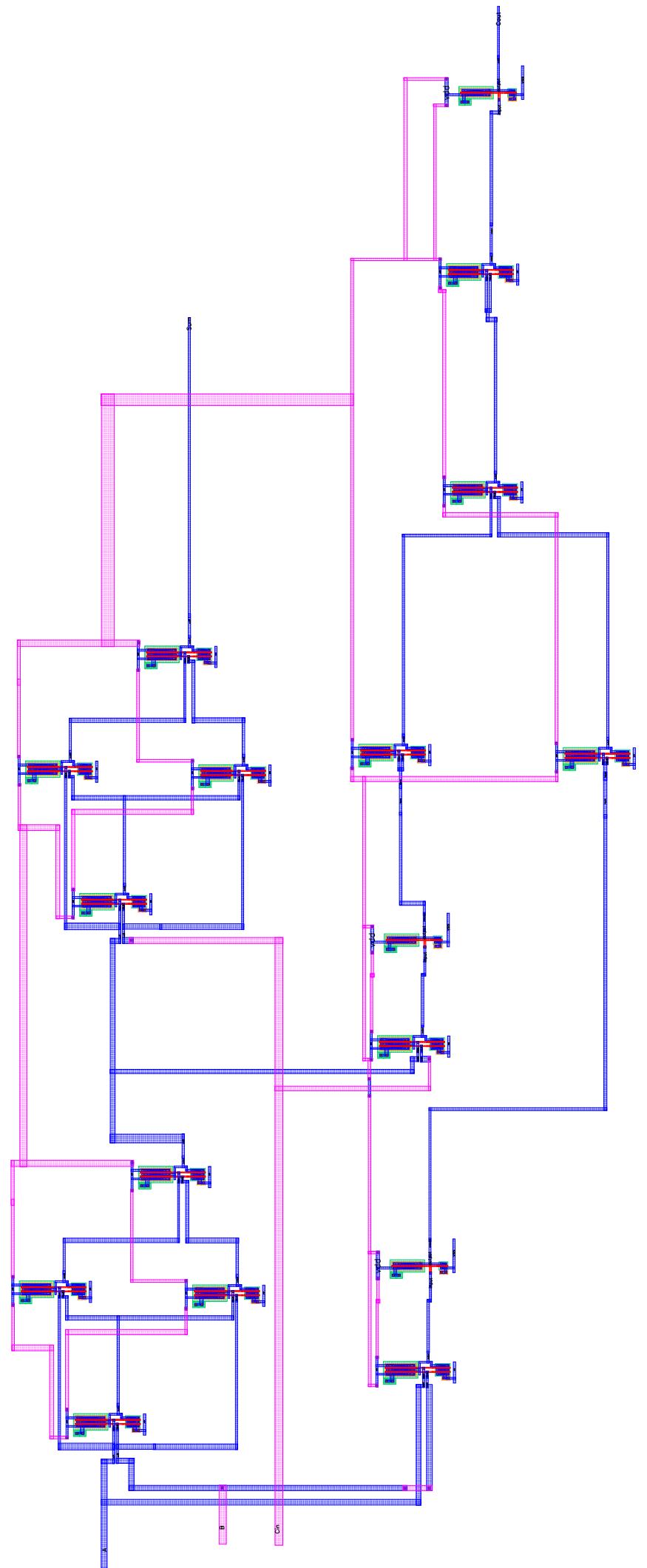
# SYMBOL

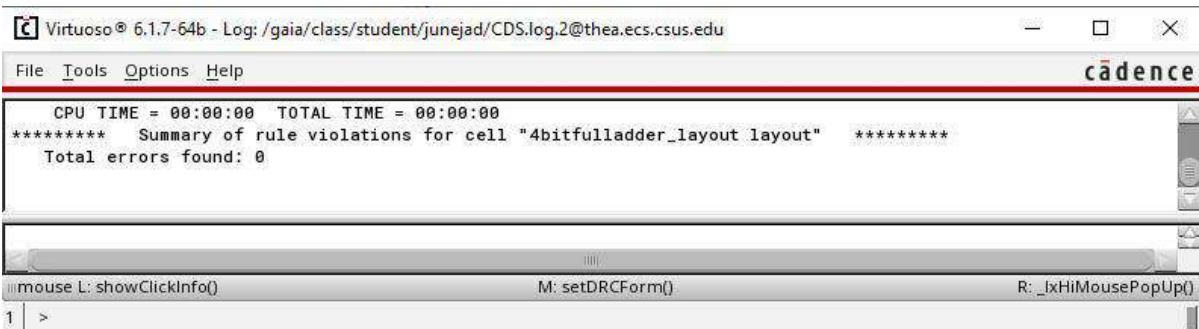


# TEST BENCH SCHEMATIC



**Transient Response****Tue Dec 4 12:29:48 2018**





```
@(#)$CDS: LVS version 6.1.7-64b 12/07/2018 19:41 (sjfhw305) $  
Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS  
-dir /gaia/class/student/junejad/demo/LVS -l -s -t  
/gaia/class/student/junejad/demo/LVS/layout  
/gaia/class/student/junejad/demo/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.
```

```
Net-list summary for /gaia/class/student/junejad/demo/LVS/layout/netlist
```

count	
36	nets
0	terminals
31	pmos
31	nmos

```
Net-list summary for /gaia/class/student/junejad/demo/LVS/schematic/netlist  
count  
36 nets  
7 terminals  
31 pmos  
31 nmos
```

```
Devices in the netlist but not in the rules:  
pmos nmos
```

```
6 net-list ambiguities were resolved by random selection.
```

```
The net-lists match.
```

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	62	62
total	62	62

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	36	36
total	36	36

	terminals	
--	-----------	--

	fulladderlvs.txt	
un-matched	0	0
matched but		
different type	0	0
total	0	7

Probe files from /gaia/class/student/junejad/demo/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/junejad/demo/LVS/layout

devbad.out:

netbad.out:

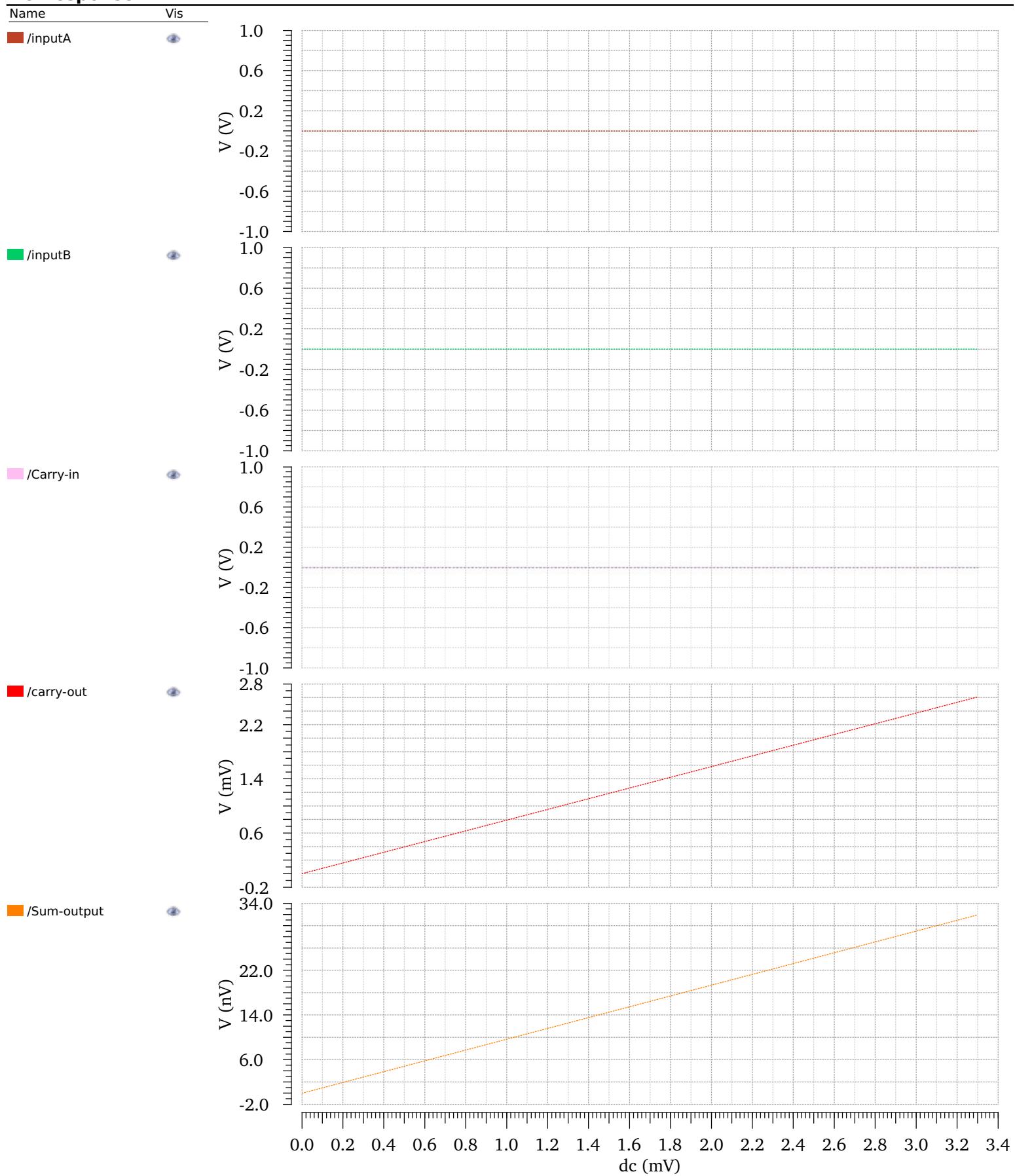
mergenet.out:

termbad.out:

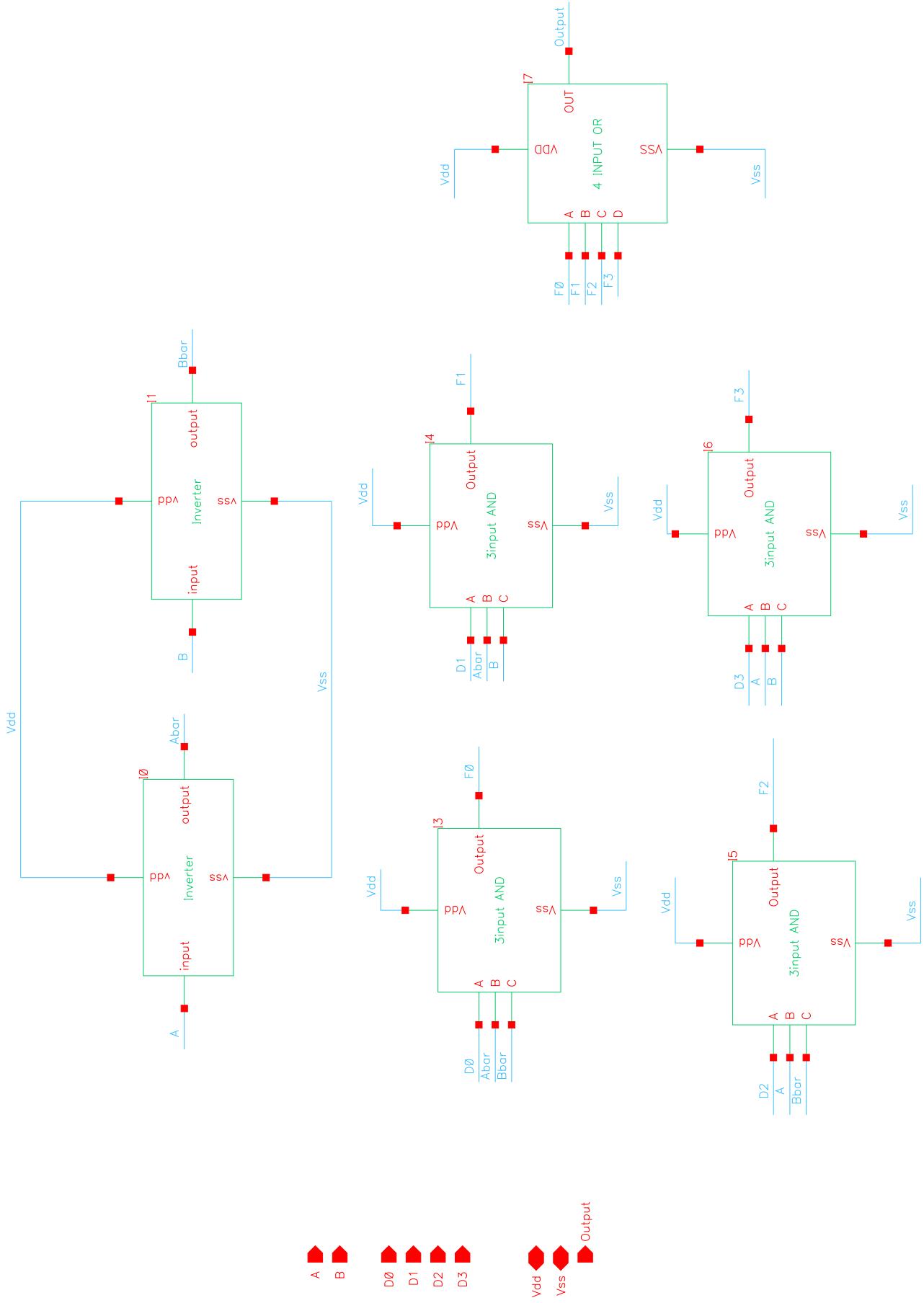
prunenet.out:

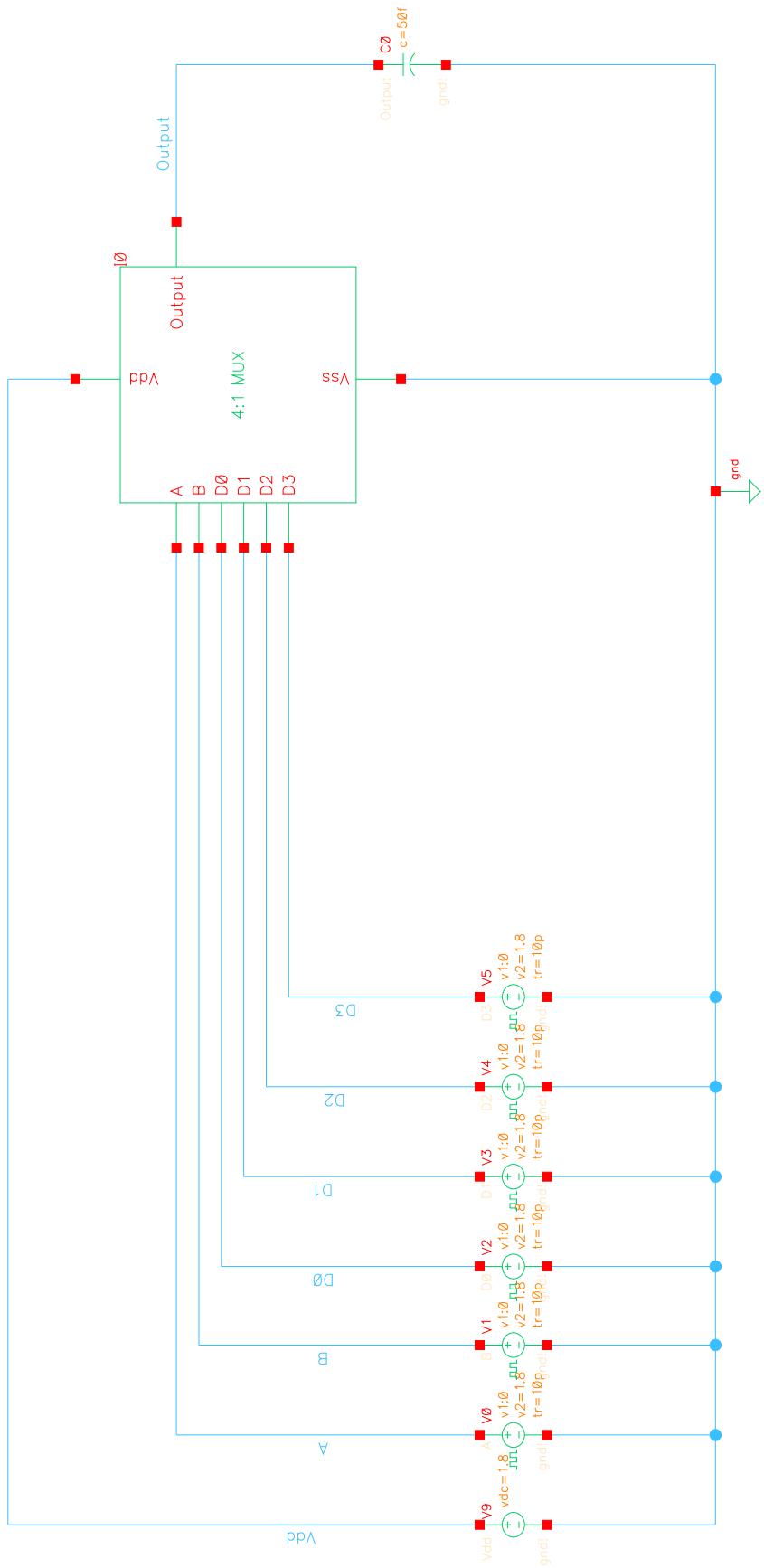
prunedev.out:

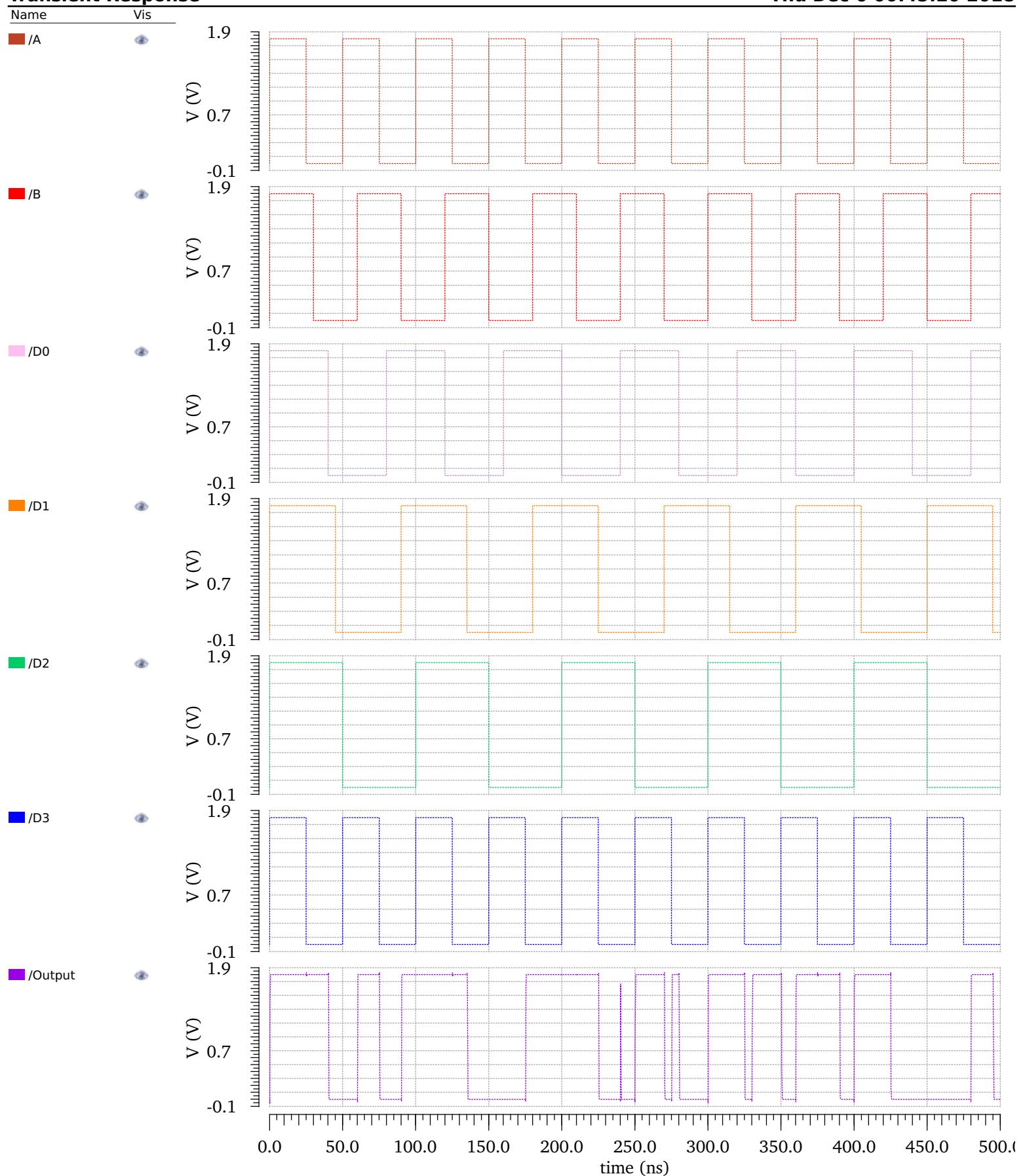
audit.out:

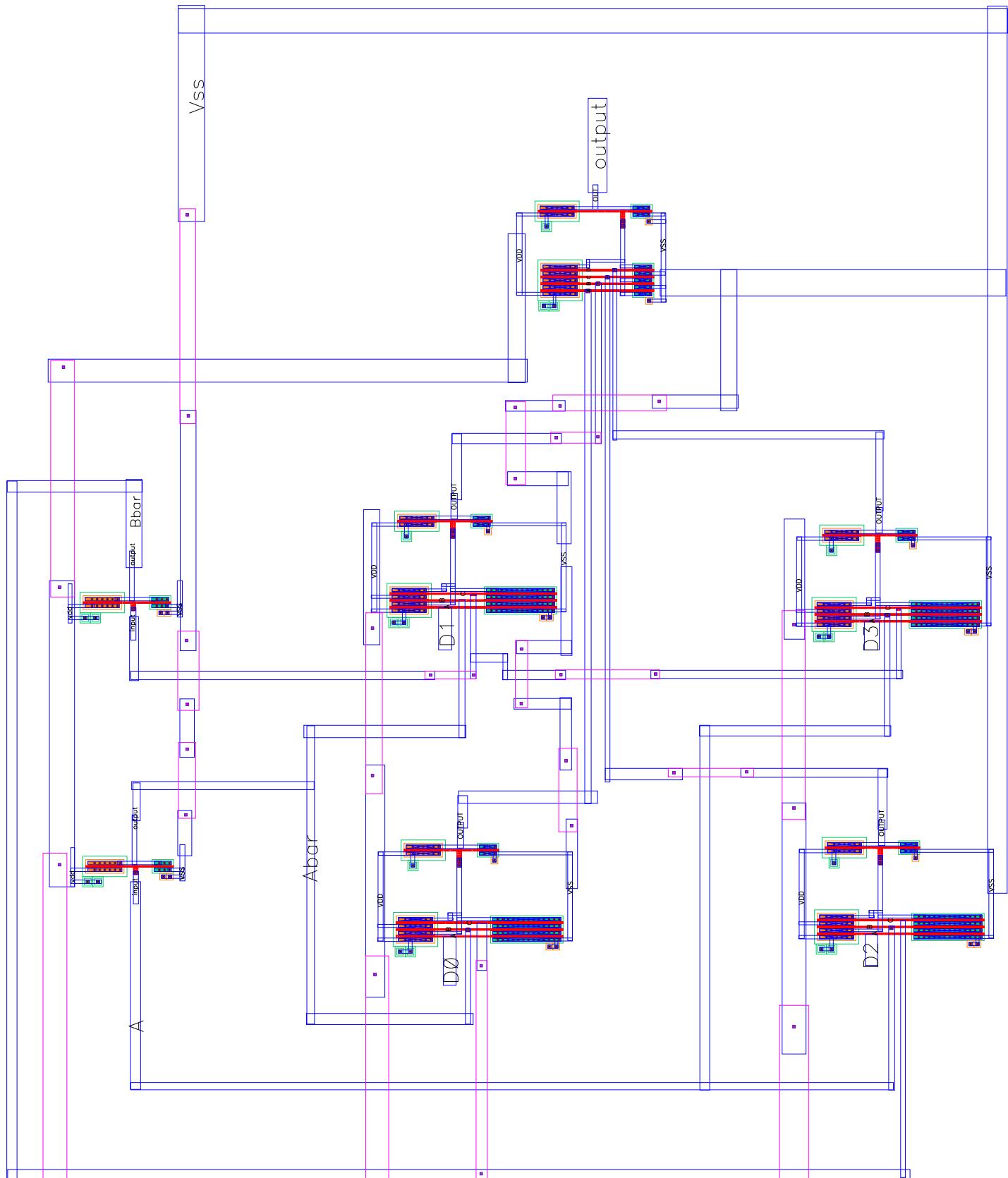
**DC Response****Fri Dec 7 05:07:58 2018**

# **4 TO 1 MUX**





**Transient Response****Thu Dec 6 00:45:20 2018**



File Tools Options Help

cadence

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

\*\*\*\*\* Summary of rule violations for cell "MUX\_L layout" \*\*\*\*\*

Total errors found: 0

Page135

mouse L: showClickInfo()

M: setDRCForm()

R: \_IxHiMousePopUp()

```
@(#)$CDS: LVS version 6.1.7-64b 12/06/2018 19:41 (sjfhw305) $
```

Command line:

```
/software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -  
dir /gaia/class/student/junejad/demo/LVS -l -s -t  
/gaia/class/student/junejad/demo/LVS/layout  
/gaia/class/student/junejad/demo/LVS/schematic
```

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

```
Net-list summary for  
/gaia/class/student/junejad/demo/LVS/layout/netlist  
count  
 21      nets  
  0      terminals  
 16      pmos  
 16      nmos
```

```
Net-list summary for  
/gaia/class/student/junejad/demo/LVS/schematic/  
netlistcount  
 21      nets  
  6      terminals  
 16      pmos  
 16      nmos
```

Devices in the rules but not in the netlist:

```
cap nfet pfet nmos4 pmos4
```

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	32	32
total	32	32

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	21	21
total	21	21

	terminals	
un-matched	0	0
matched but different type	0	0
total	0	6

Probe files from /gaia/class/student/junejad/demo/LVS/

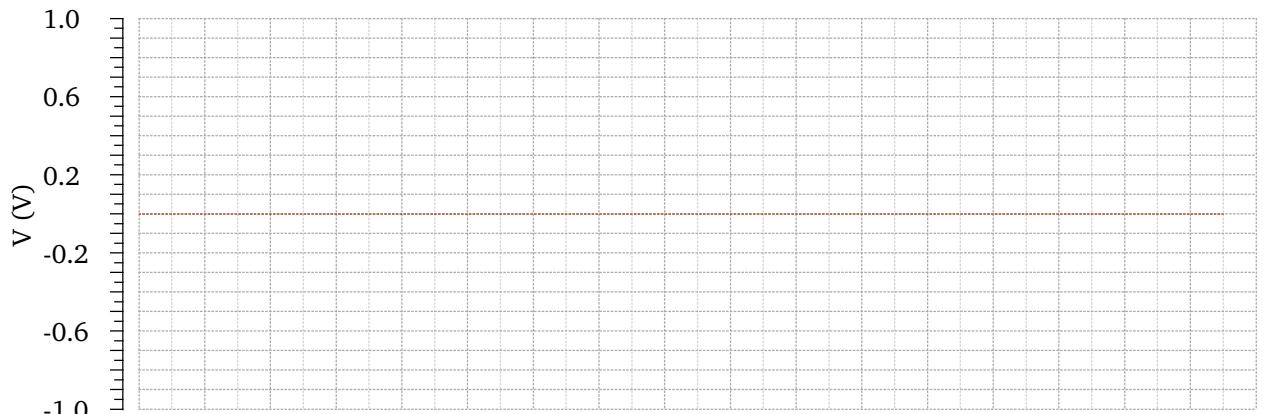
schematic devbad.out:

```
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:  
  
Probe files from /gaia/class/student/junejad/demo/LVS/  
layout devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:
```

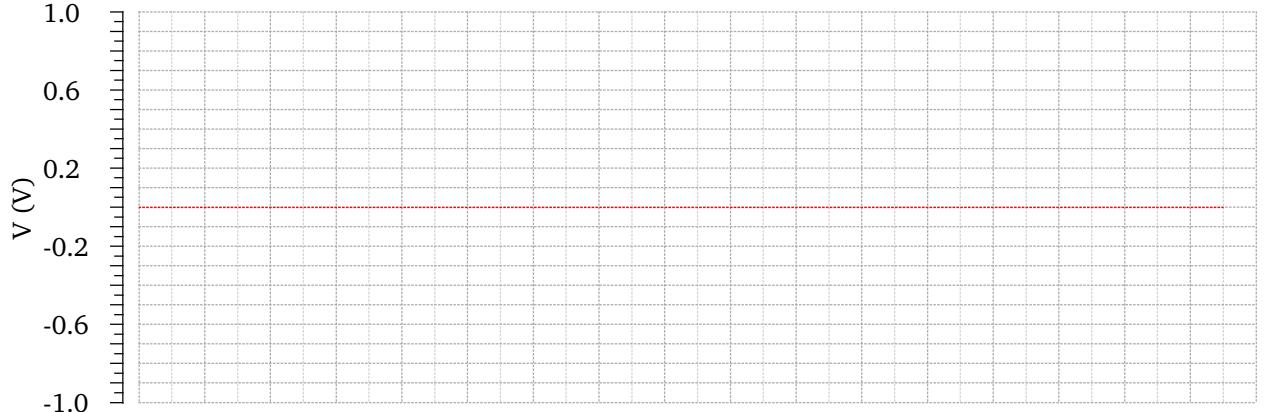
**DC Response****Fri Dec 7 14:13:28 2018**

Name Vis

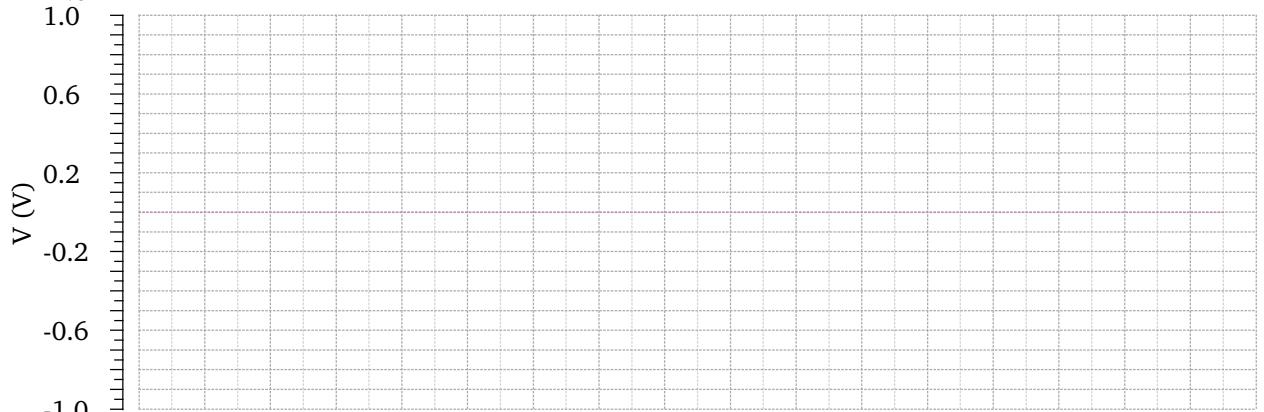
■ /d0



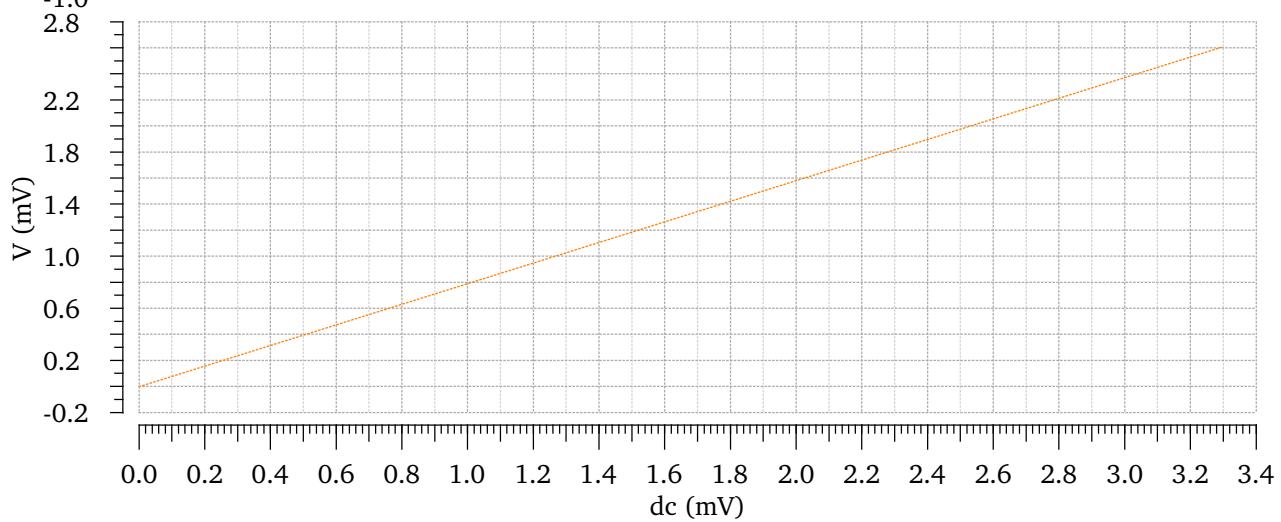
■ /d1



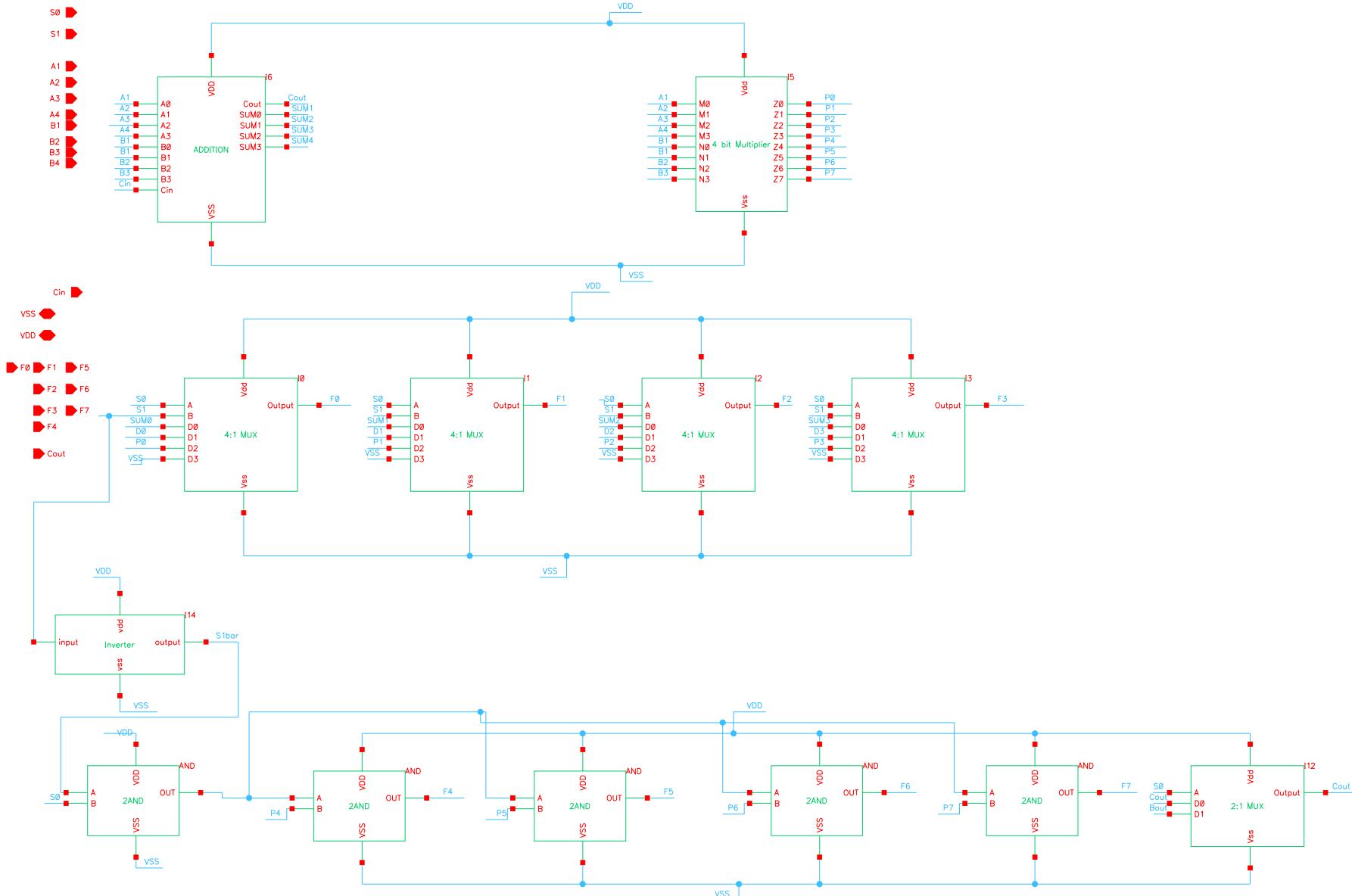
■ /s-input



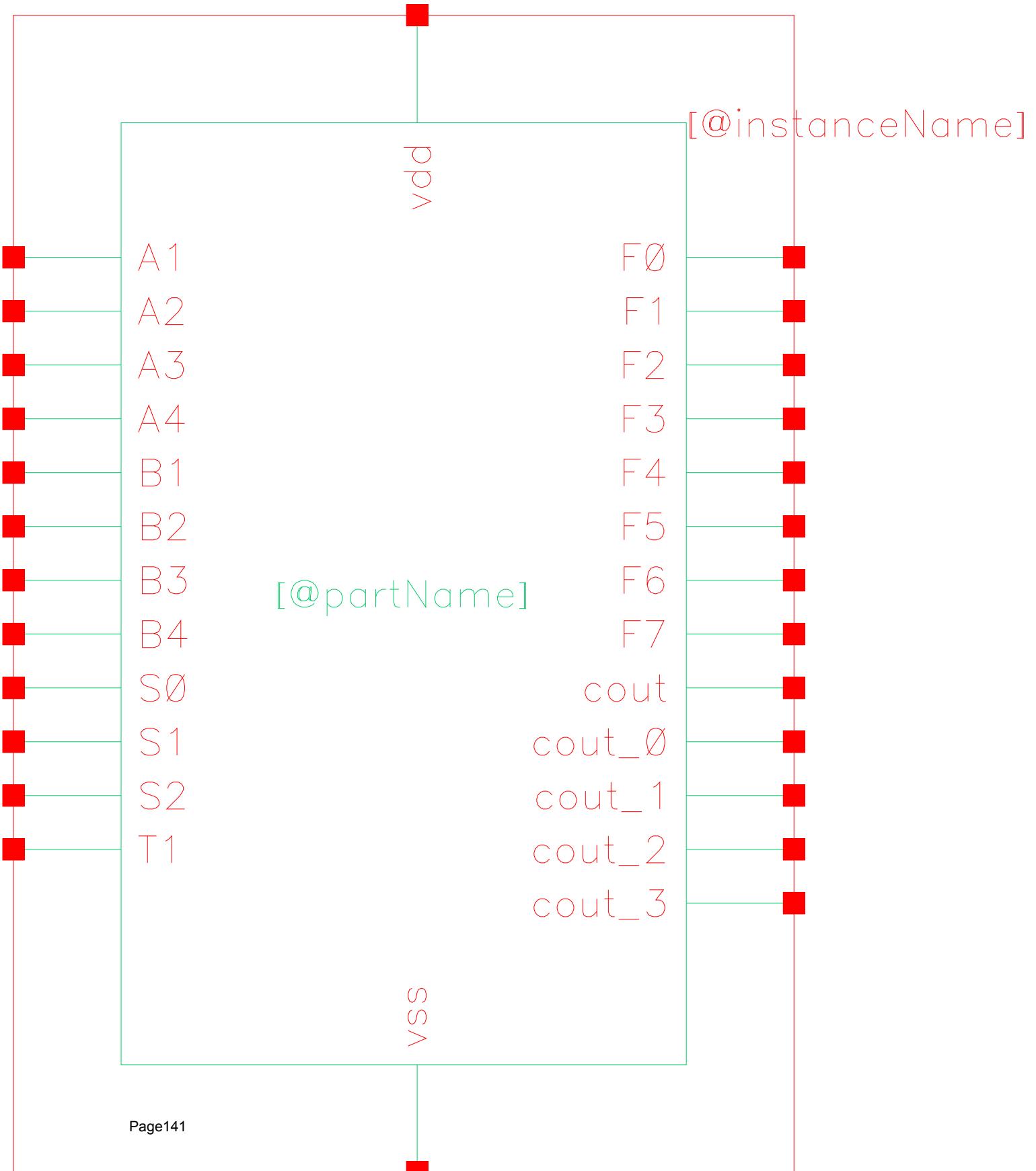
■ /output



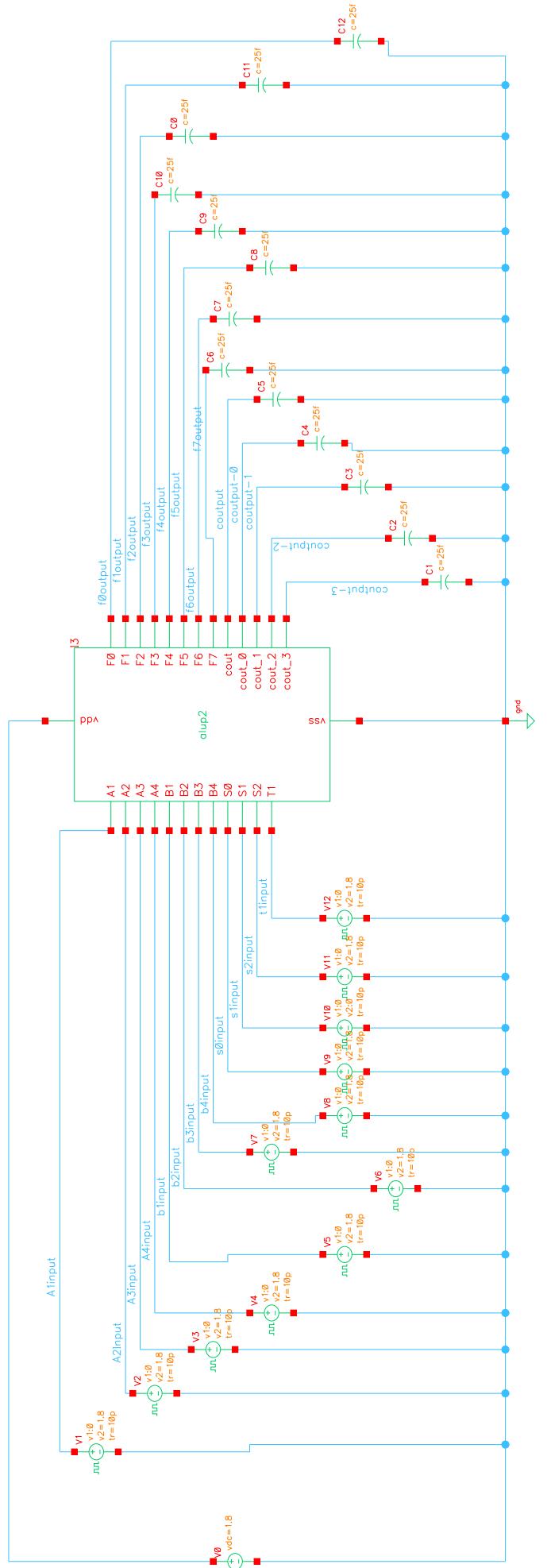
**ARITHMETIC**  
**LOGIC**  
**UNIT**



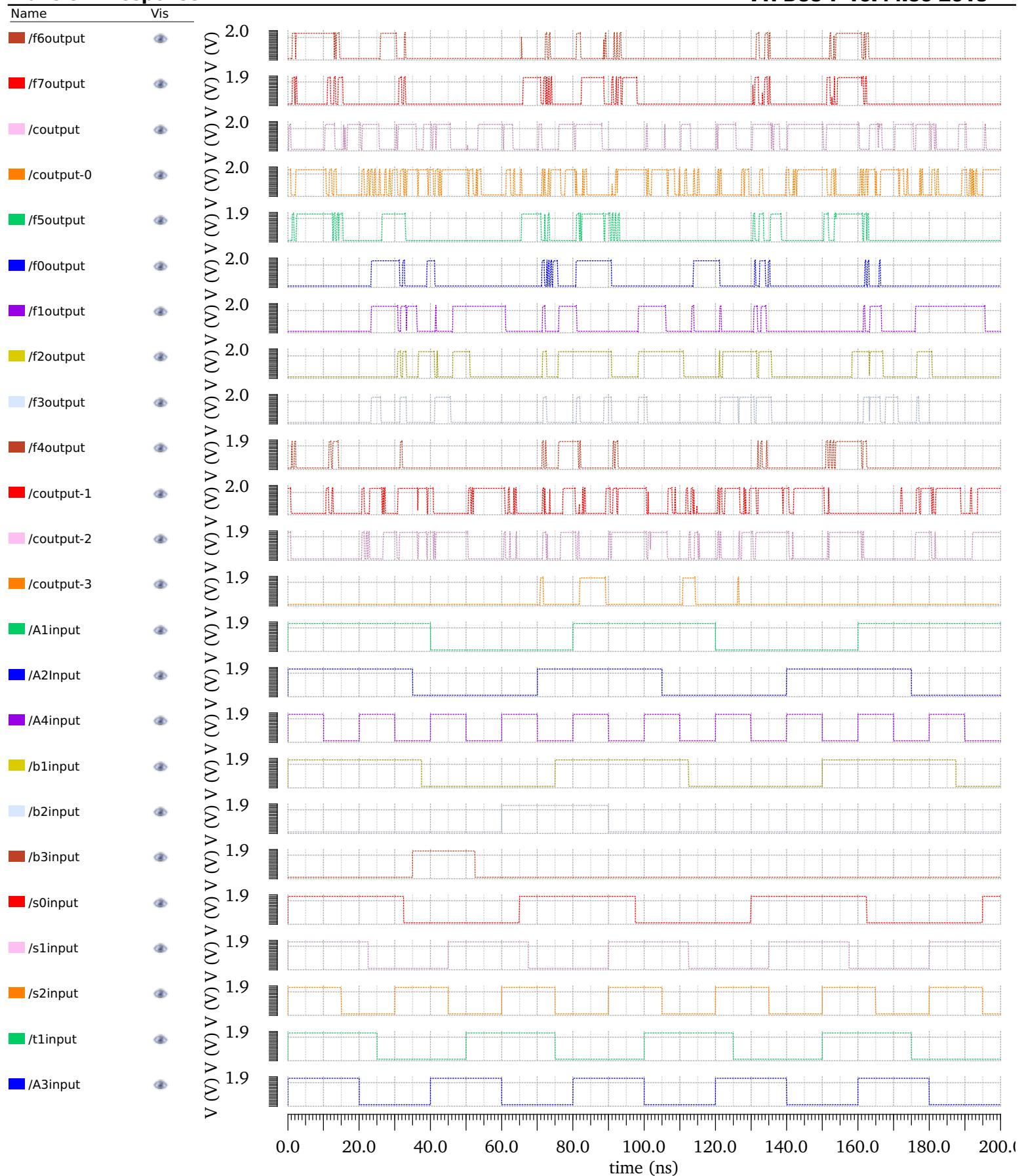
# SYMBOL



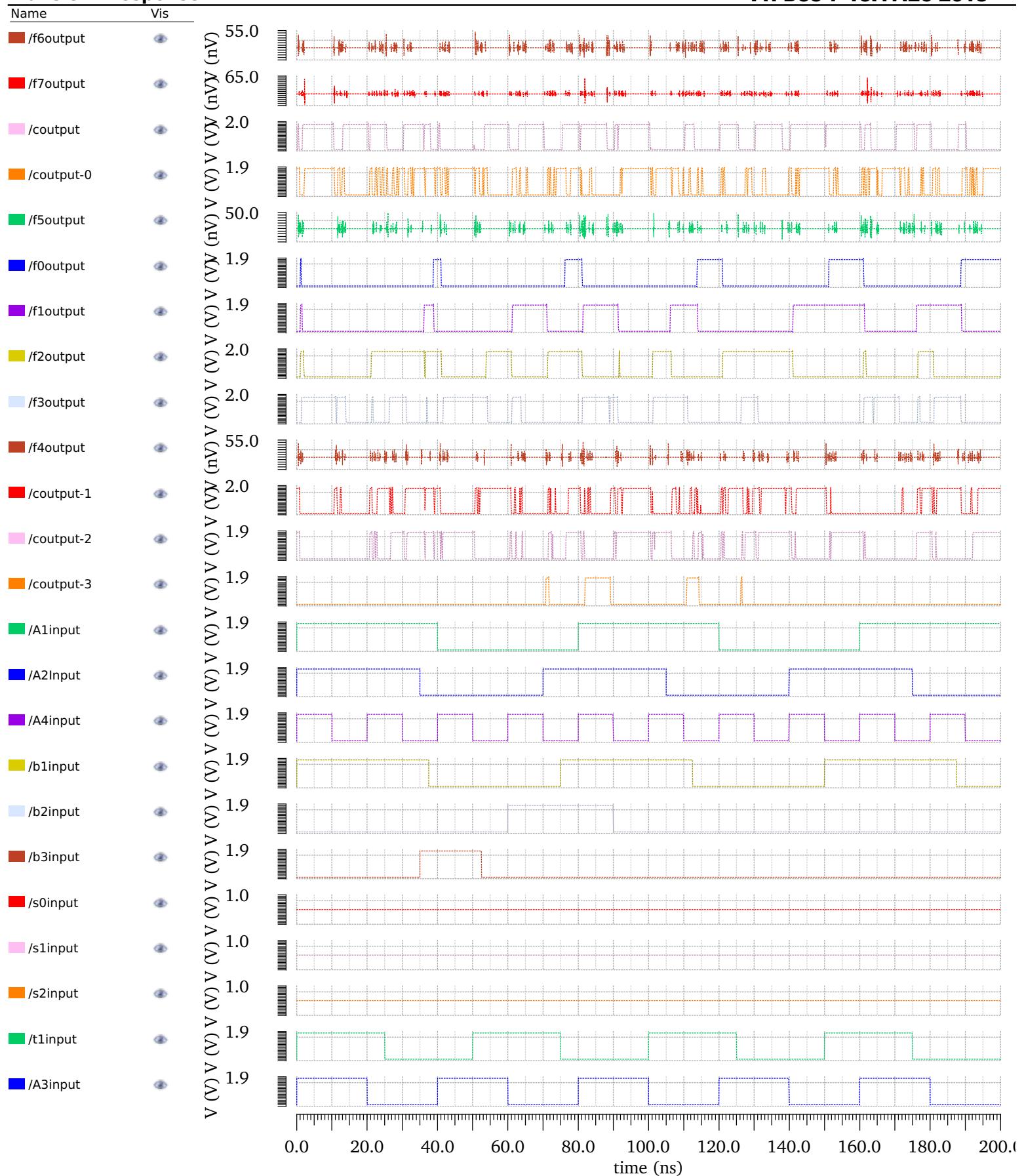
# TEST BENCH SCHEMATIC

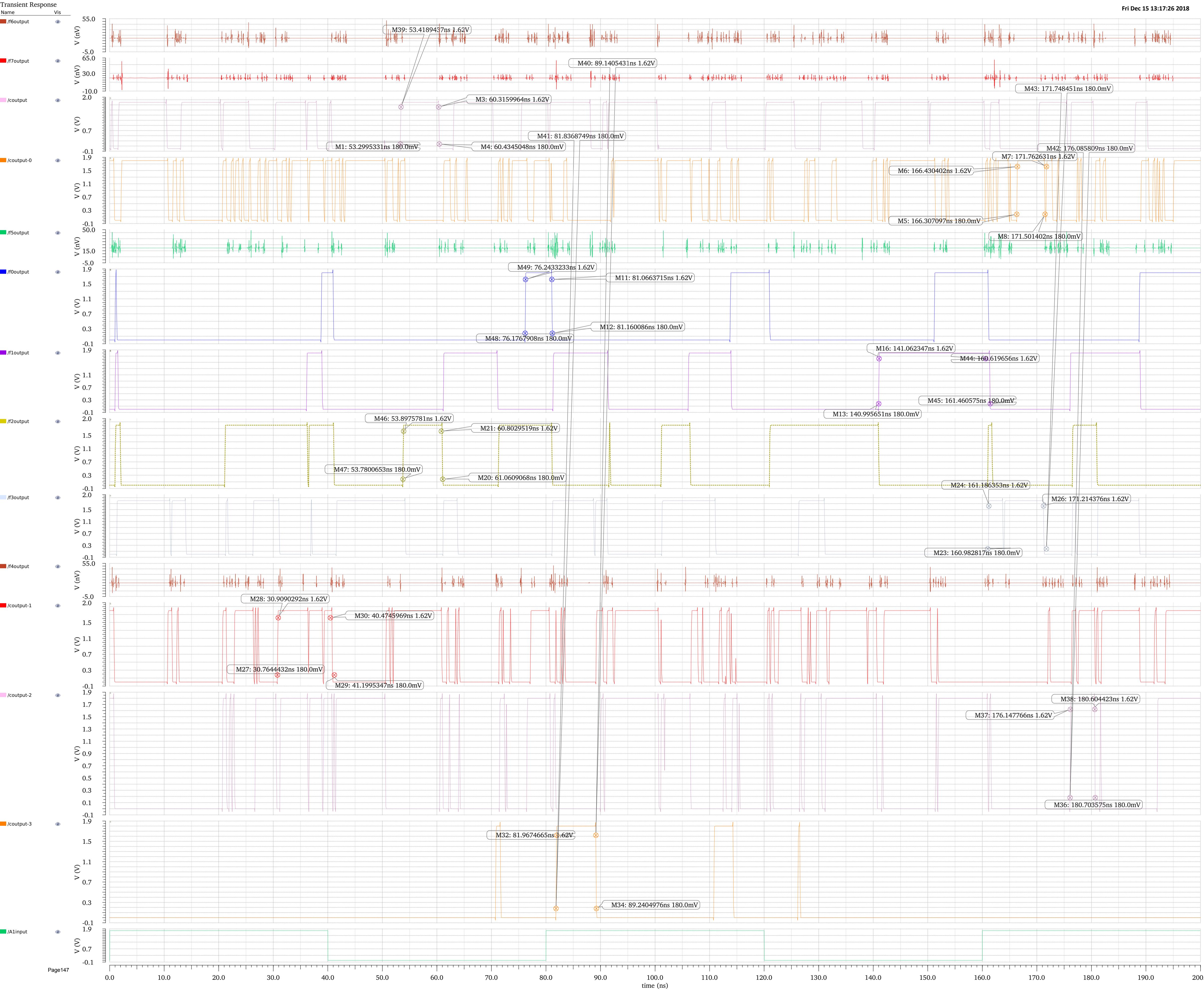


**ALU**  
**GENERAL**  
**O/P**

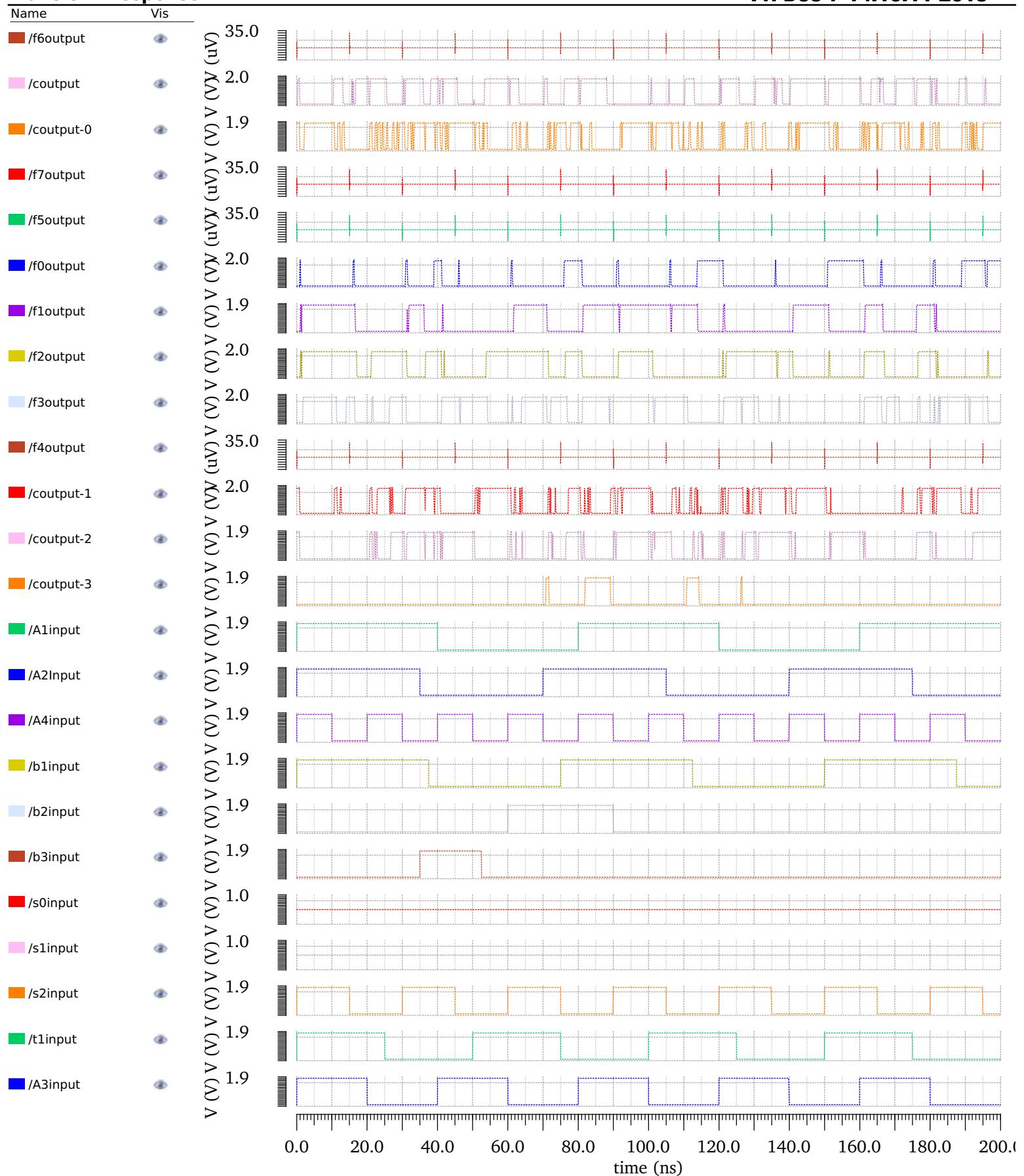
**Transient Response****Fri Dec 7 10:44:30 2018**

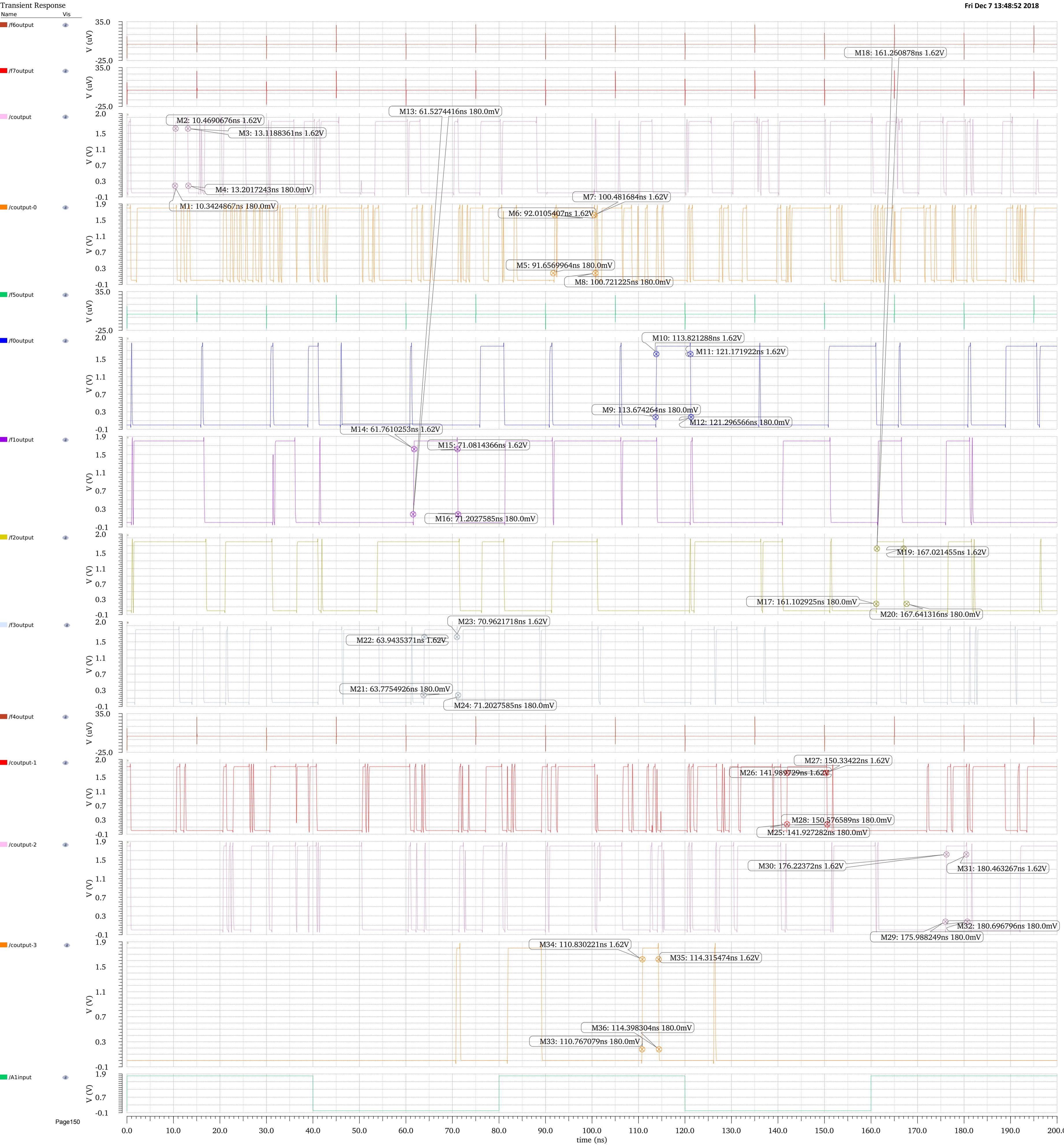
# **ALU ADD**

**Transient Response****Fri Dec 7 13:17:26 2018**



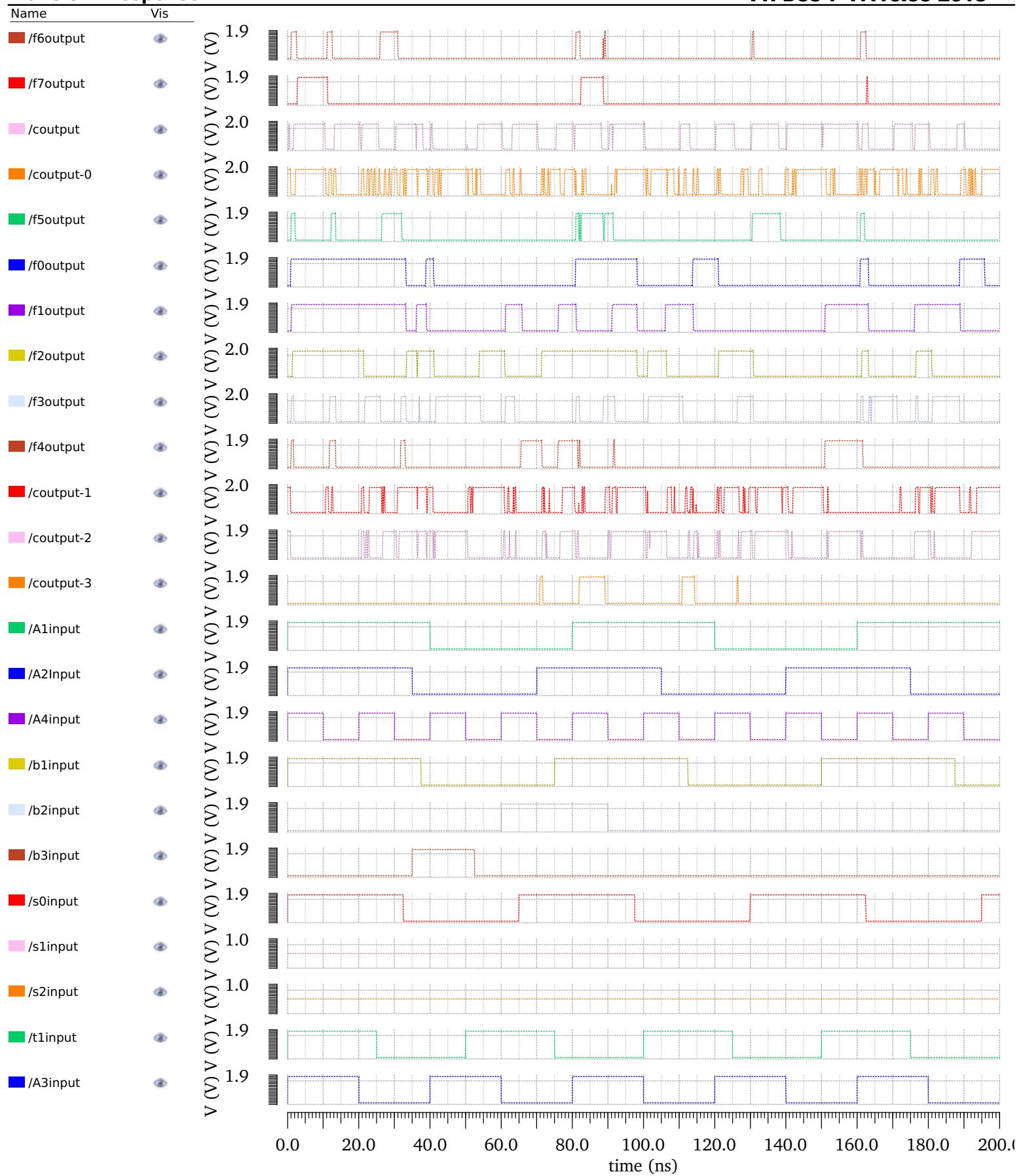
**ALU**  
**SUBTRACT**

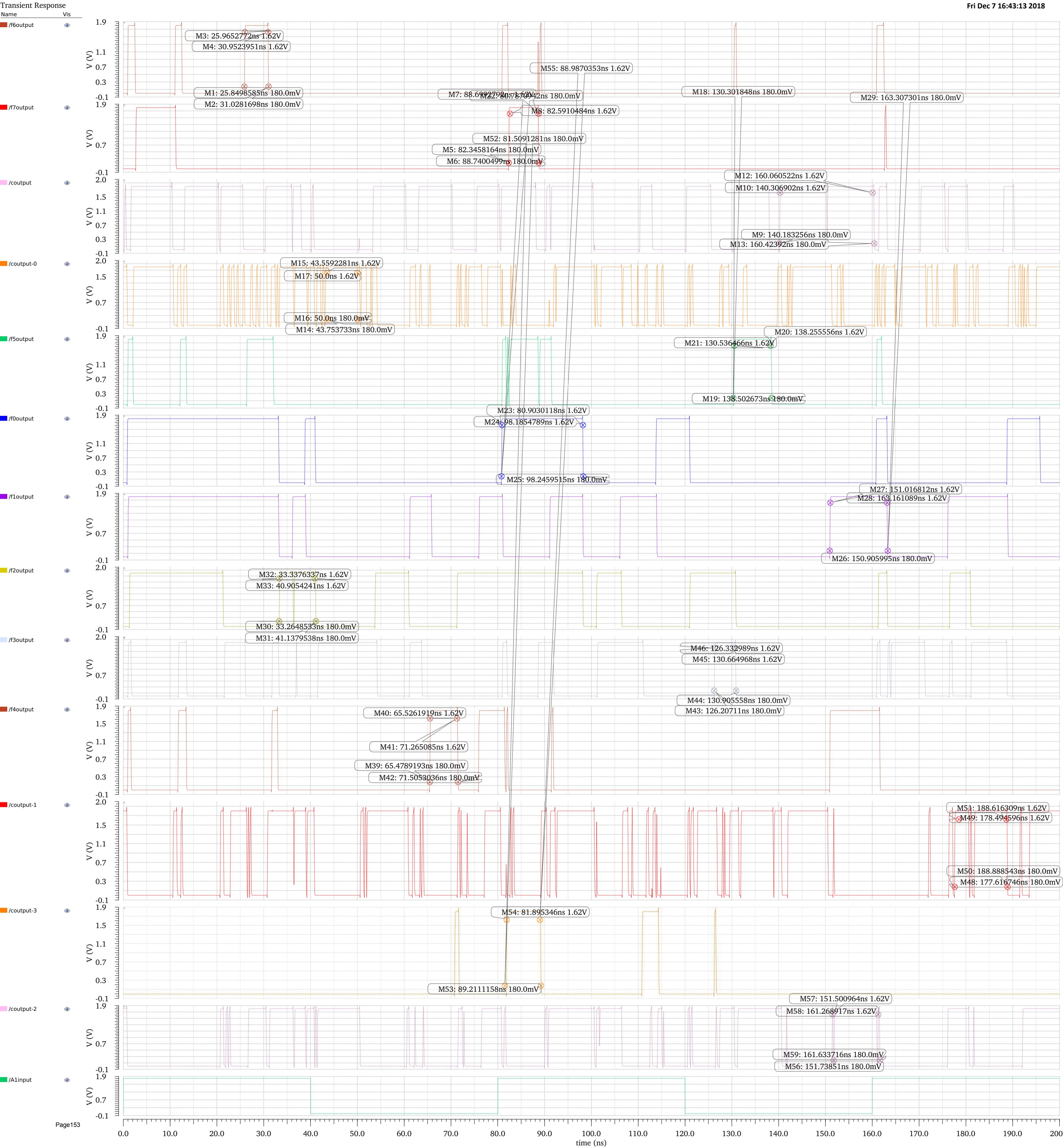
**Transient Response****Fri Dec 7 14:10:11 2018**

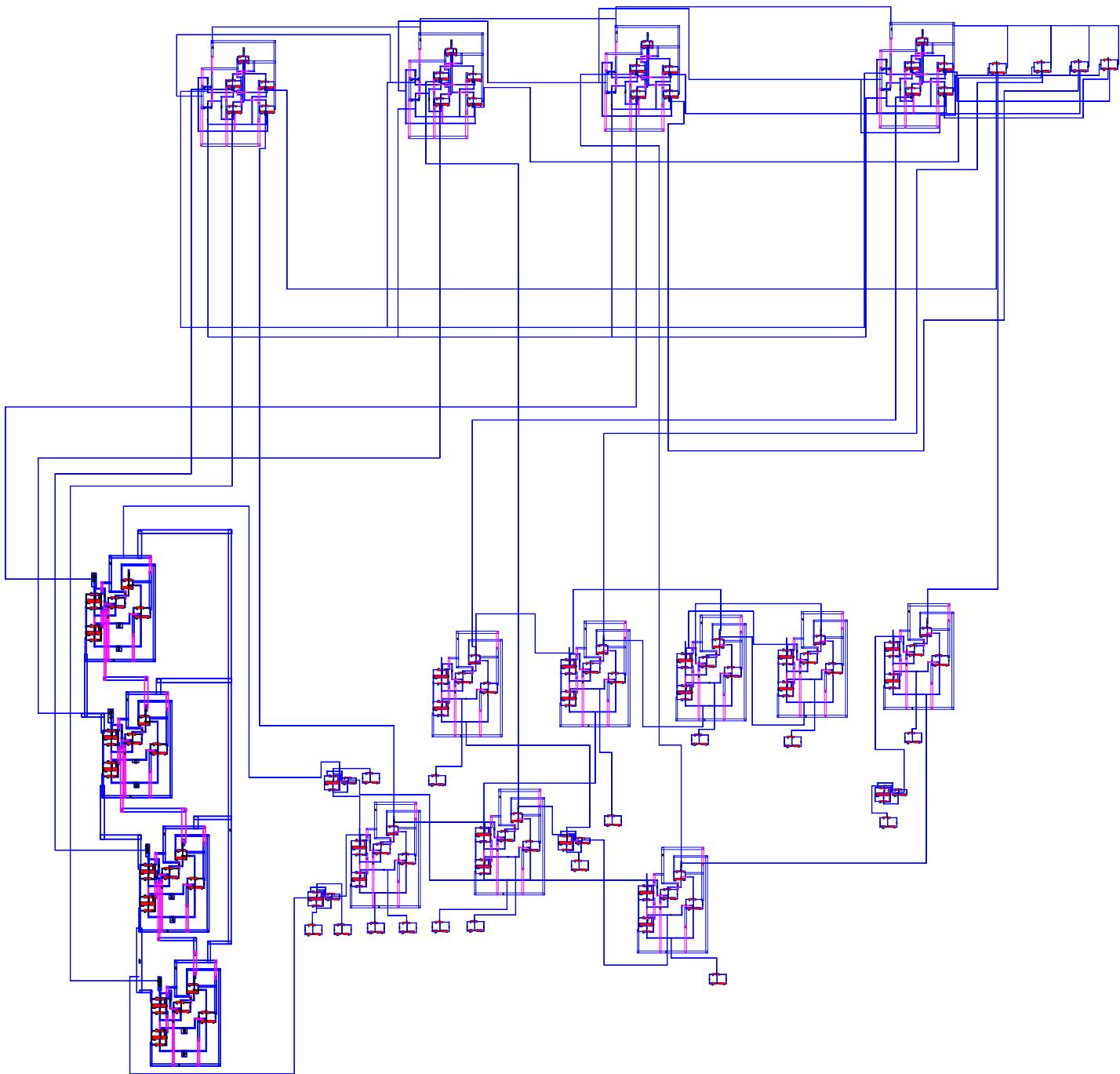


# **ALU**

# **MULTIPLICATION**

**Transient Response****Fri Dec 7 17:16:53 2018**





```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "ALU_L layout" *****
Total errors found: 0
```

mouse L: showClickInfo()

M: setDRCForm()

R: \_IxHiMousePopUp()

1 | >

```
@(#)$CDS: LVS version 6.1.7-64b 12/07/2018 19:41 (sjfhw305) $
```

Command line:

```
/software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -  
dir /gaia/class/student/junejad/demo/LVS -l -s -t  
/gaia/class/student/junejad/demo/LVS/layout  
/gaia/class/student/junejad/demo/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.  
Compiling Diva LVS rules...
```

```
Net-list summary for  
/gaia/class/student/junejad/demo/LVS/layout/netlist  
count  
    1716      nets  
    0        terminals  
    1697      pmos  
    1697      nmos
```

```
Net-list summary for  
/gaia/class/student/junejad/demo/LVS/schematic/  
netlistcount  
    1716      nets  
    32        terminals  
    1697      pmos  
    1697      nmos
```

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	3394	3394
total	3394	3394

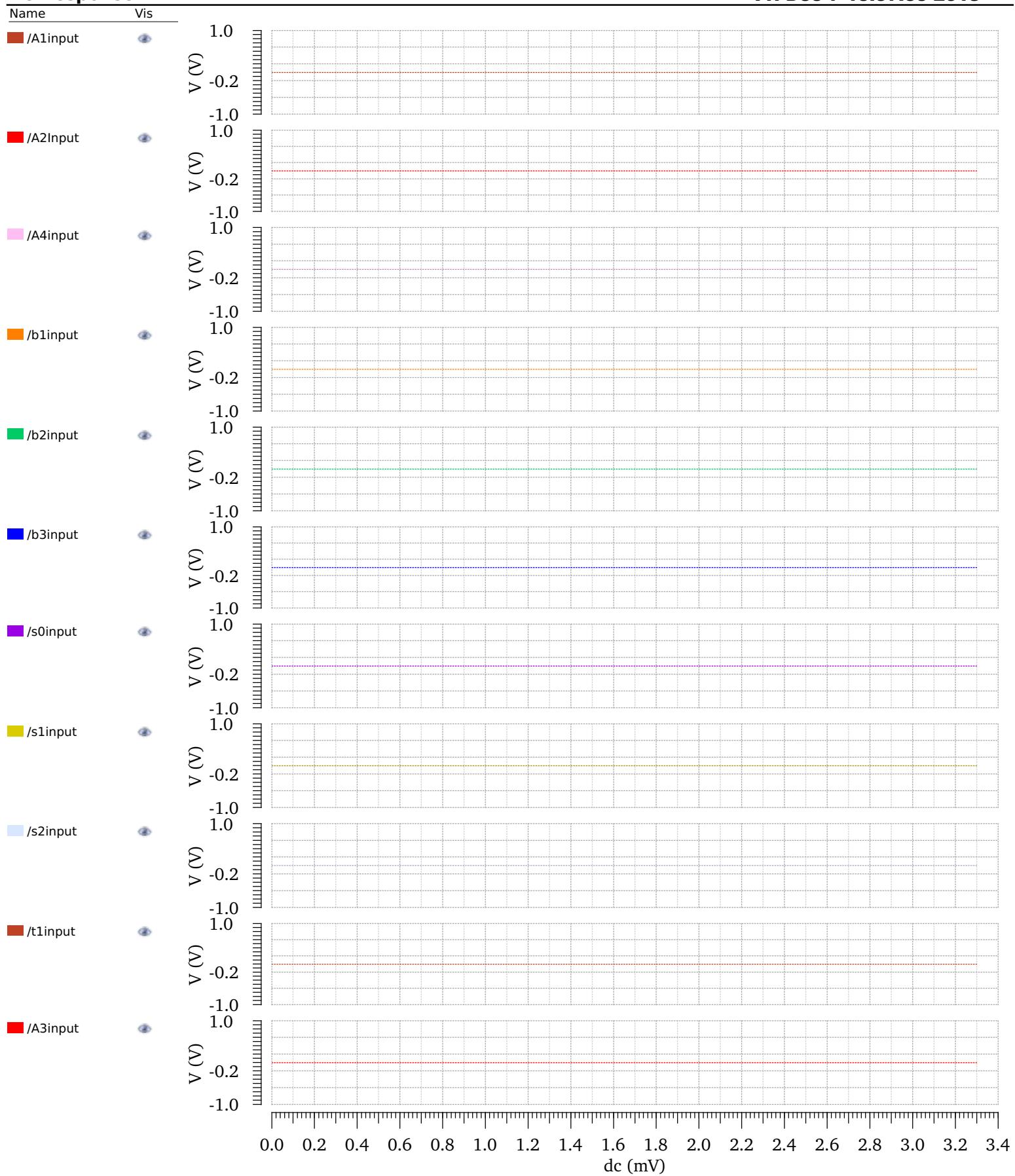
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	1716	1716
total	1716	1716

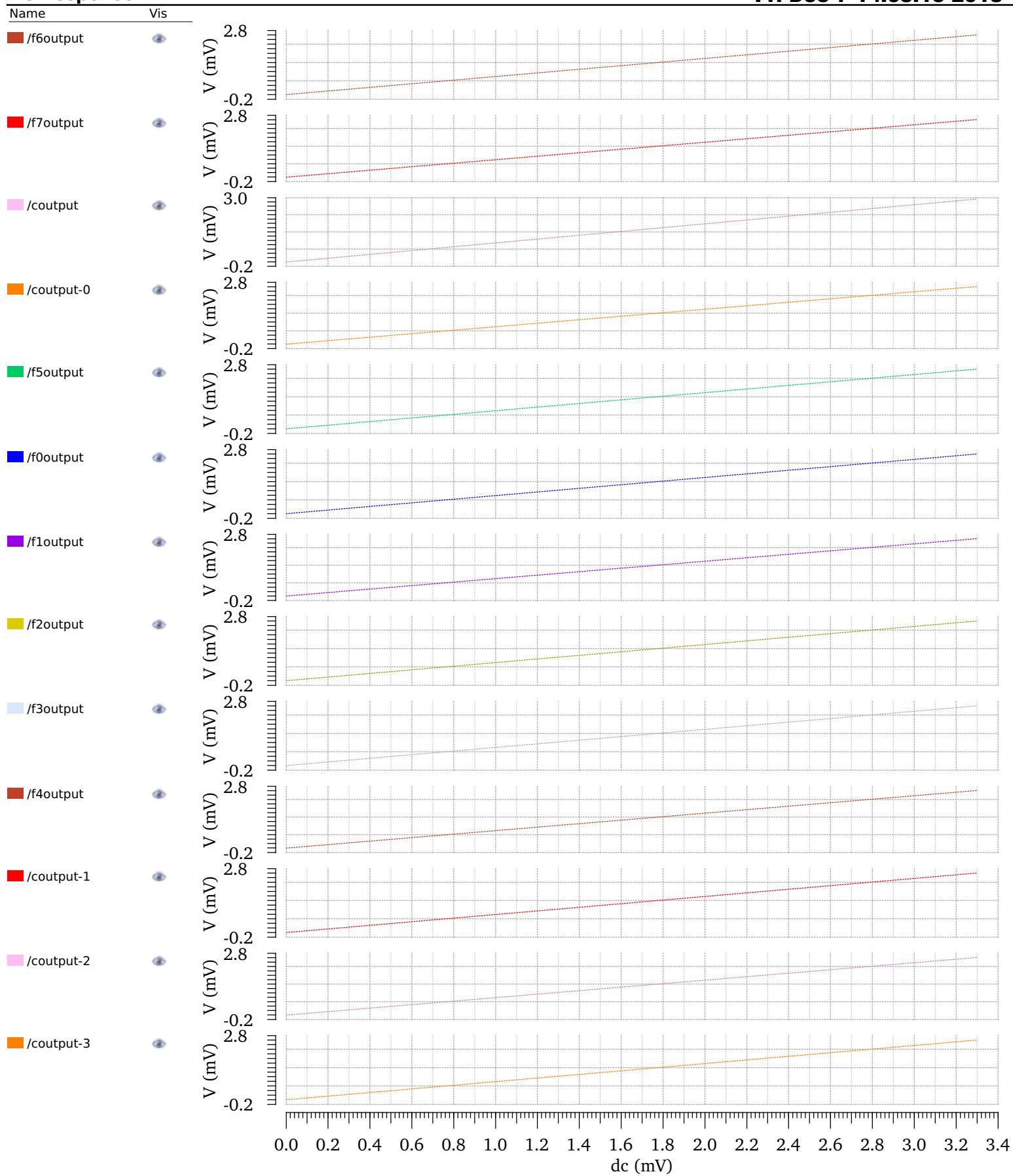
  

	terminals	
un-matched	0	0
matched but different type	0	0
total	0	32

Probe files from /gaia/class/student/junejad/demo/LVS/  
schematic devbad.out:

```
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:  
  
Probe files from /gaia/class/student/junejad/demo/LVS/  
layout devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:
```

**DC Response****Fri Dec 7 13:57:33 2018**

**DC Response****Fri Dec 7 14:08:13 2018**

## CONCLUSION

SR. NO.	DESCRIPTION	RISE TIME(ns)	FALL TIME(ns)
1	INVERTER	0.5236	0.0403
2	2-INPUT AND	40.33037	45.08135
3	3-INPUT XOR	51.08574	70.20866
4	2-INPUT OR	40.23	70.1813
5	2 INPUT NOR	30.28201	40.1856
6	D-Flip Flop	41.451	46.361
7	2-INPUT NAND	25.41916	40.08421
8	HALF ADDER	CARRY OUT:40.55442 SUM:70.1513	CARRY OUT:40.55442 SUM: 70.77502
9	FULL ADDER	CARRY OUT:80.57427 SUM: 40.24851	CARRY OUT: 95.62261 SUM: 45.10468