SACRAMENTO STATE

EEE 234

DIGITAL IC DESIGN

PROJECT NO.1

ABHISHEK CHAKRABORTY

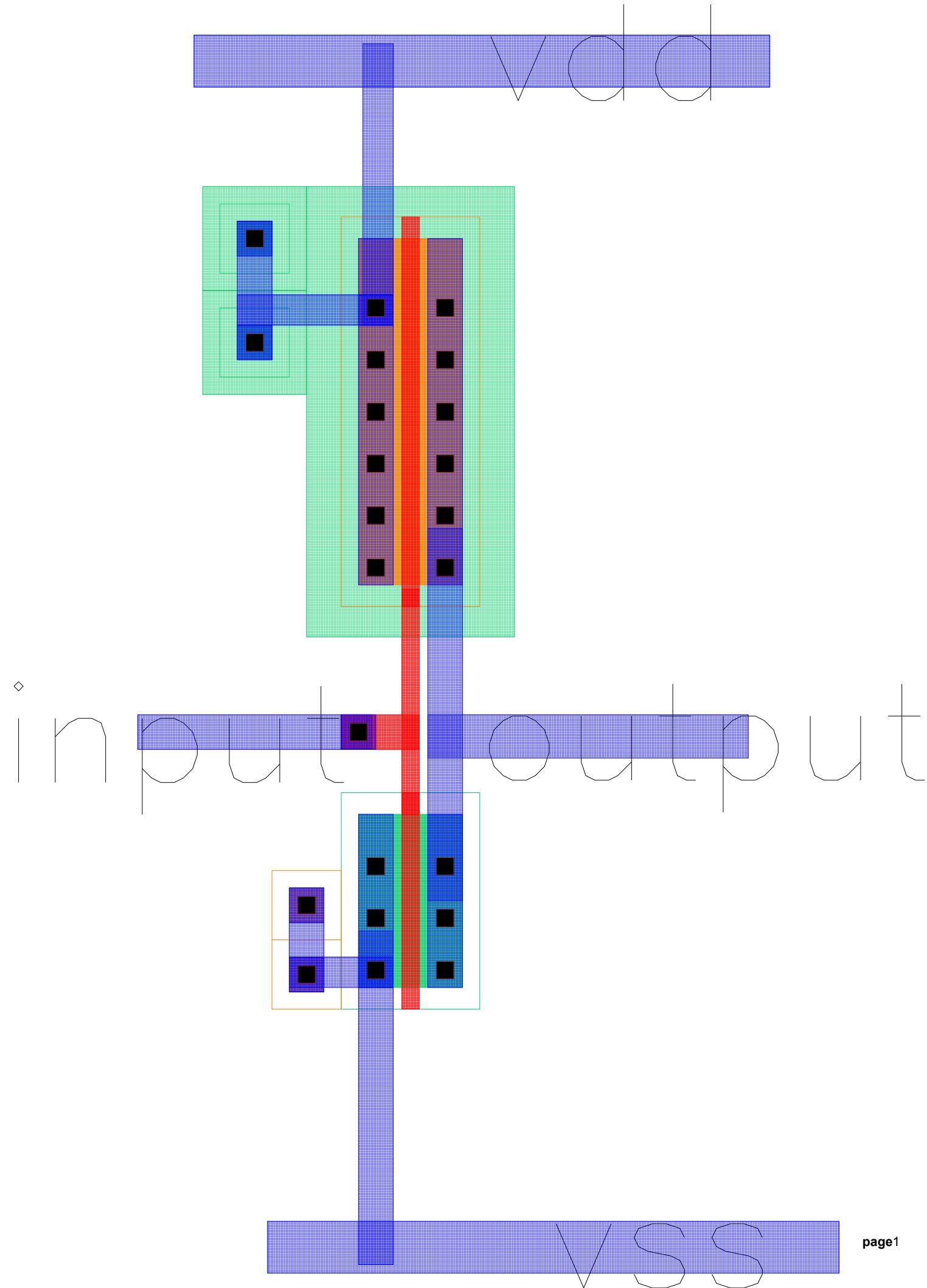
Date of Submission: 28 October, 2018

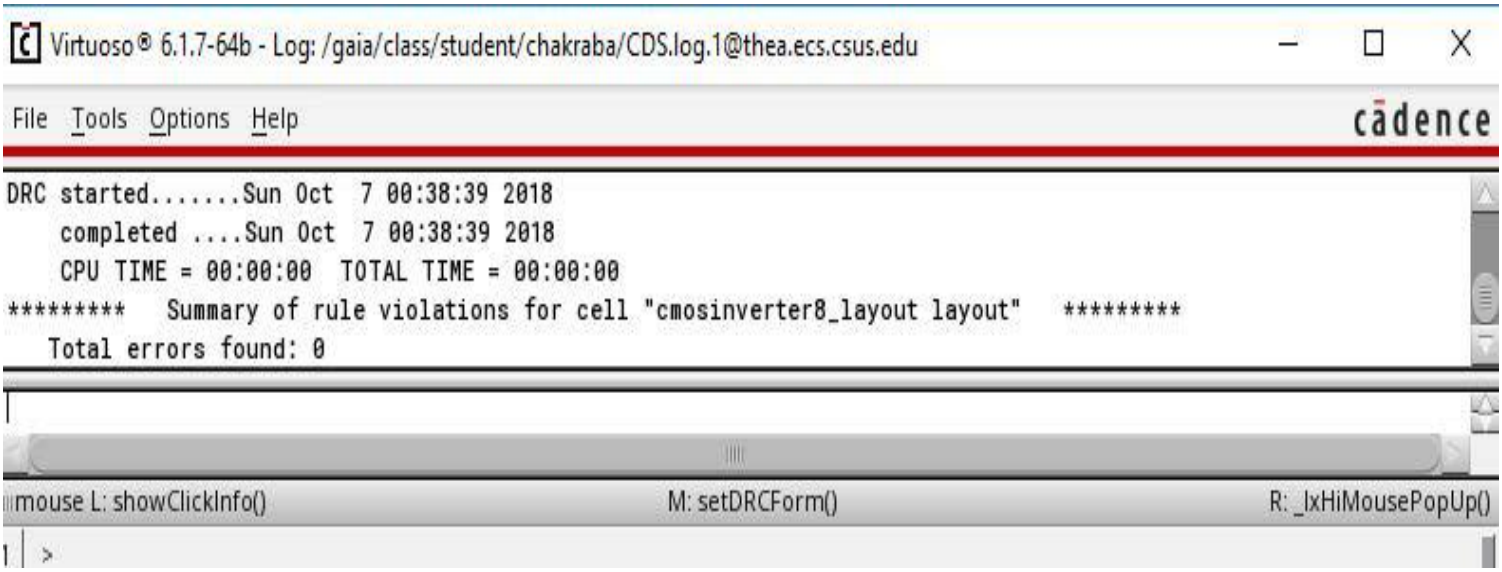
TABLE OF CONTENTS

INVERTER

(W/L)n=1.8/0.18

(W/L)p=3.6/0.18


Vcc
input
output
Vss


Virtuoso® 6.1.7-64b - Log: /gaia/class/student/chakraba/CDS.log.1@thea.ecs.csus.edu
File Tools Options Help
cadence
DRC started.....Sun Oct 7 00:38:39 2018
completed ....Sun Oct 7 00:38:39 2018
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
********* Summary of rule violations for cell "cmosinverter8_layout layout" *********
Total errors found: 0
mouse L: showClickInfo()
M: setDRCForm()
R: _lxHiMousePopUp()
>

LVS FILE INVERTER

```
@(#)$CDS: LVS version 6.1.7-64b 10/07/2018 09:41 (sjfhw305) $

Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/
LVS -dir /gaia/class/student/chakraba/project1234/LVS -l -s -t
/gaia/class/student/chakraba/project1234/LVS/layout
/gaia/class/student/chakraba/project1234/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for
/gaia/class/student/chakraba/project1234/LVS/layout/netlist
       count
        4               nets
        0               terminals
        1               pmos
        1               nmos

    Net-list summary for
/gaia/class/student/chakraba/project1234/LVS/schematic/
netlistcount
        4               nets
        4               terminals
        1               pmos
        1               nmos

Devices in the netlist but not in the rules:
        pcapacitor pmos nmos

The net-lists match.

                            layout  schematic
                               instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  2       2
        total                   2       2

                                 nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                               terminals
        un-matched              0       0
        matched but
```

different type	0	0
total	0	4

Probe files from /gaia/class/student/chakraba/project1234/LVS/

schematic devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/chakraba/project1234/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

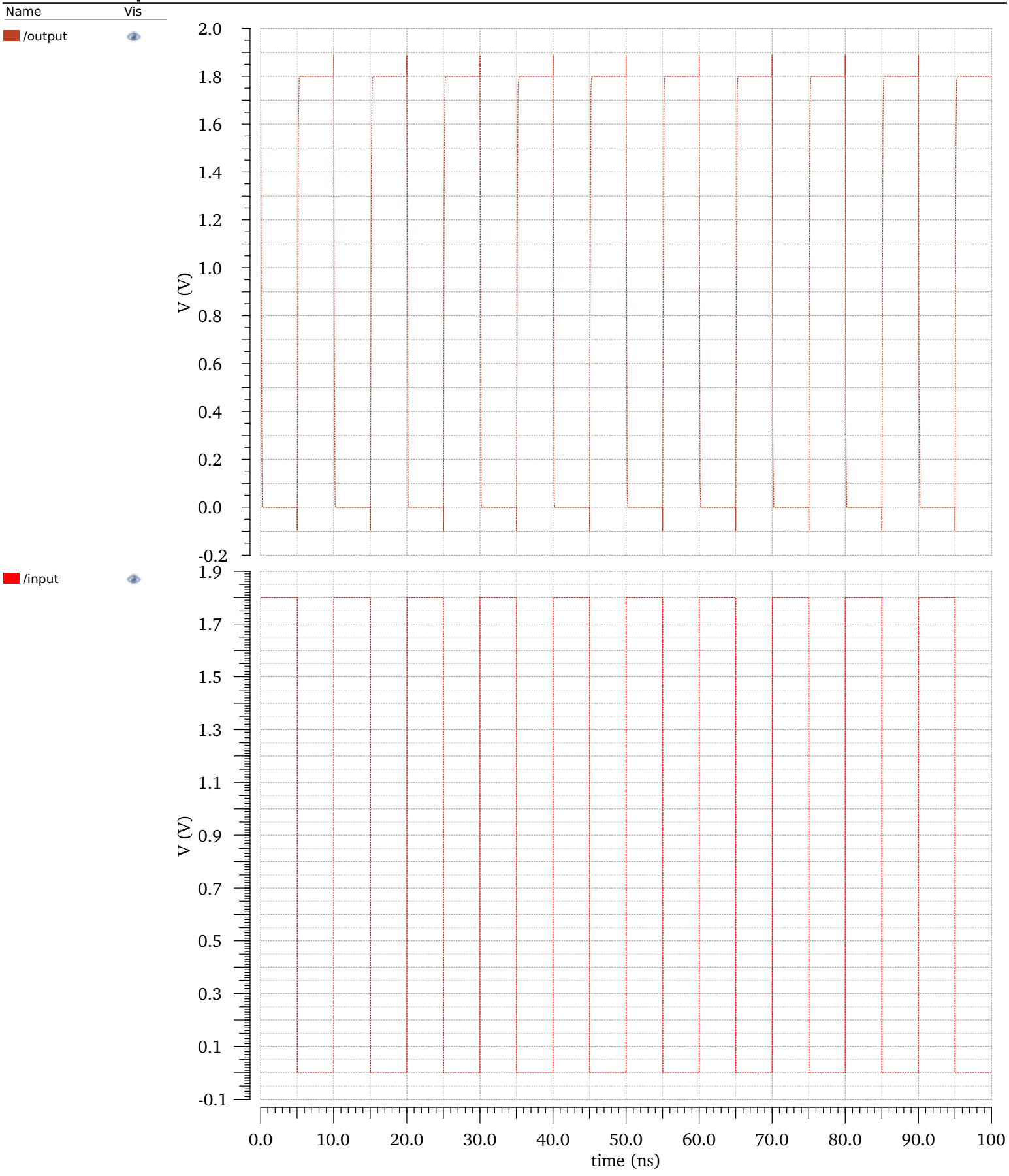
prunenet.out:

prunedev.out:

audit.out:

Transient Response

Sat Oct 6 16:40:14 2018



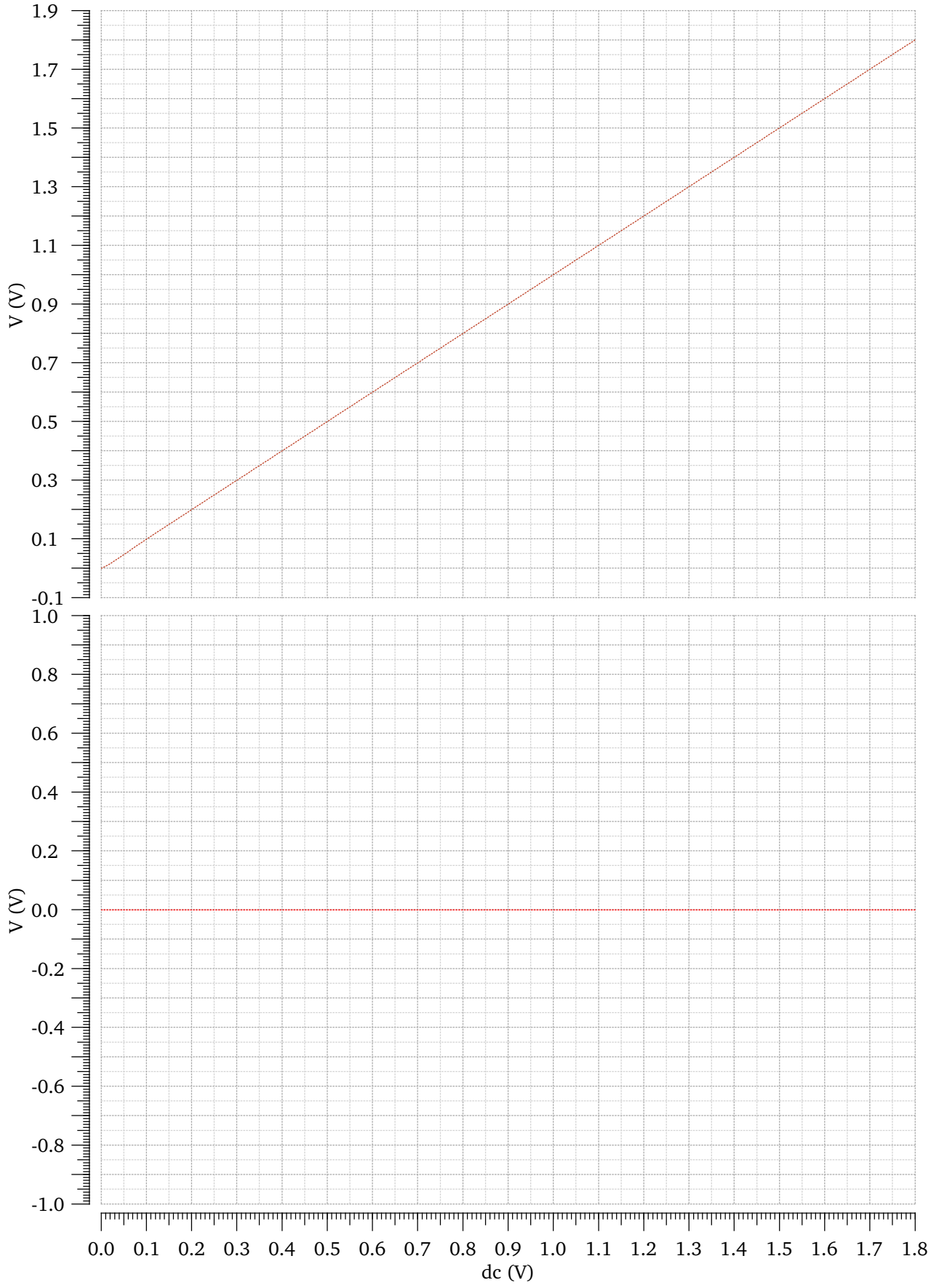
DC Response

Sat Oct 6 17:40:50 2018

Name Vis

/output

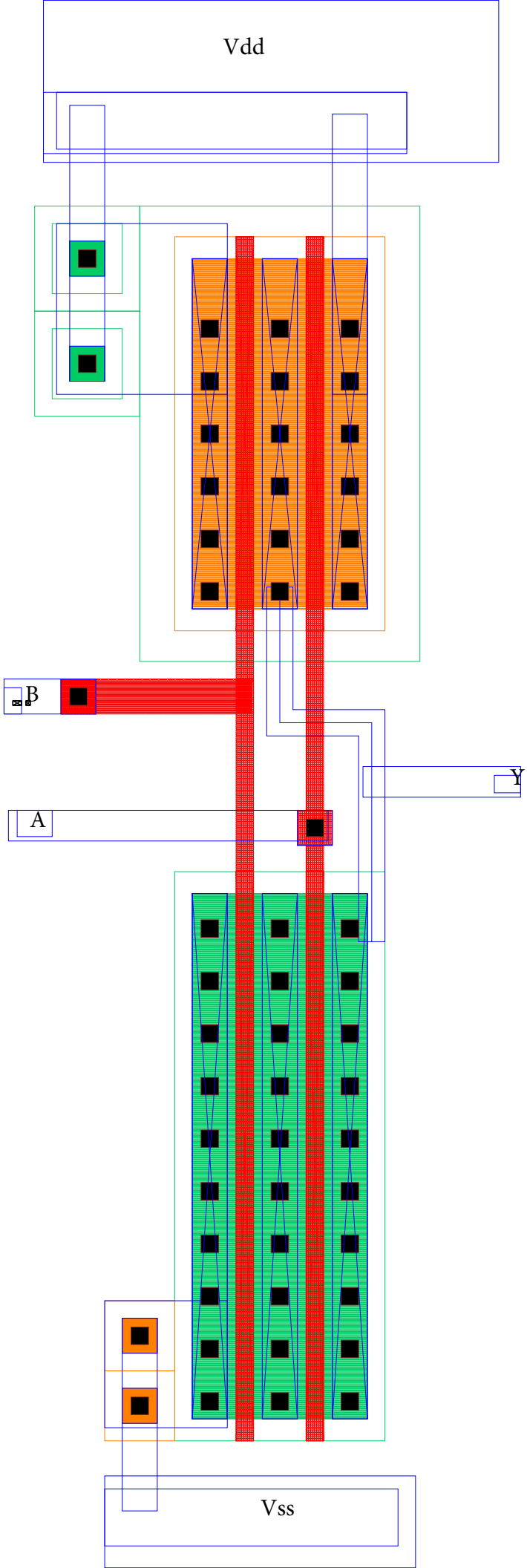
/input



2-INPUT NAND GATE

(W/L)n=5.4/0.18

(W/L)p=3.6/0.18


Vdd
B
Y
A
Vss

Virtuoso® 6.1.7-64b - Log: /gaia/class/student/chakraba/CDS.log@thea.ecs.csus.edu

File Tools Options Help

cadence

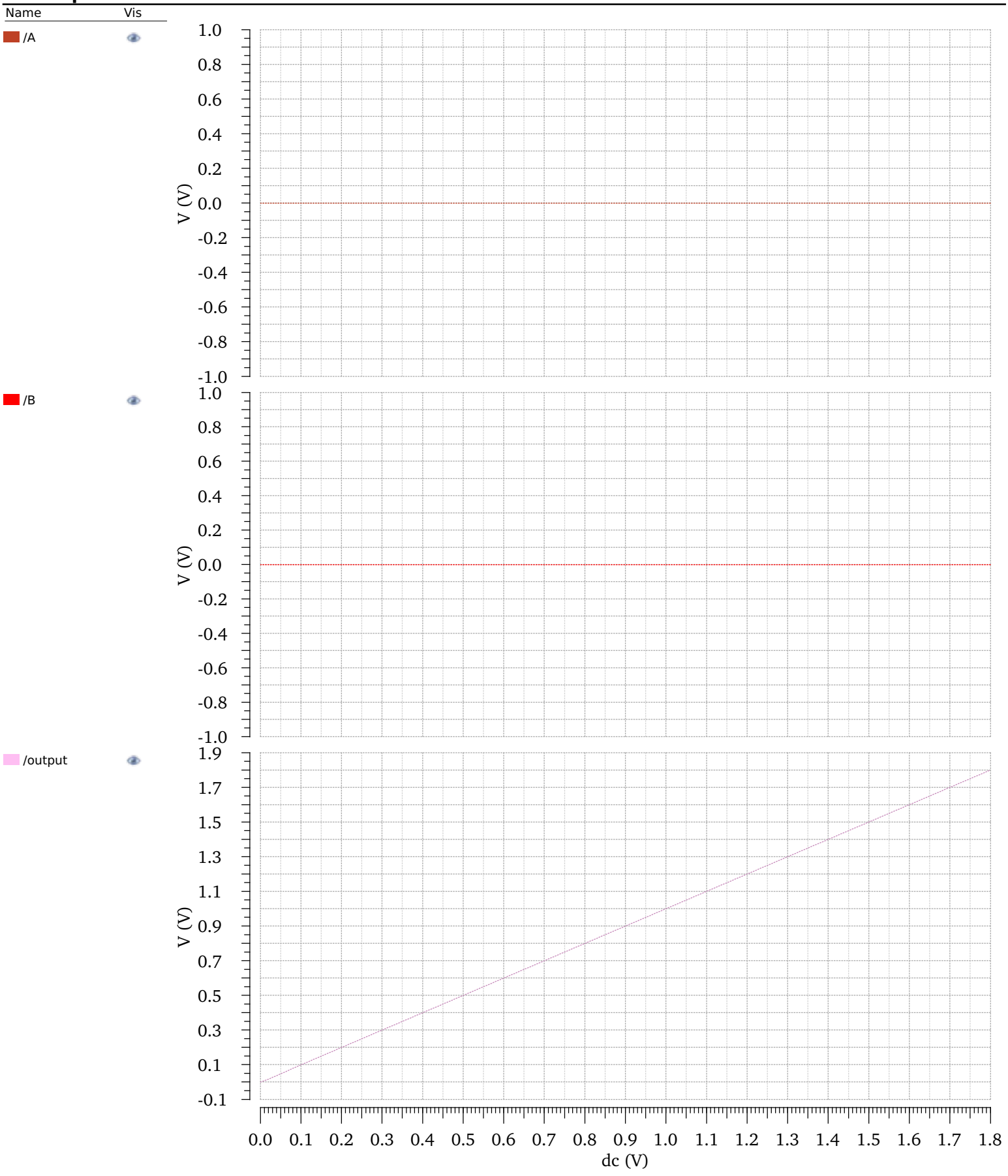
```
DRC started.......Fri Oct 26 11:56:27 2018
    completed ....Fri Oct 26 11:56:27 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "nand_testbench layout"   *********
   Total errors found: 0
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/chakraba/cmosnand/LVS -l -s -t
/gaia/class/student/chakraba/cmosnand/LVS/layout
/gaia/class/student/chakraba/cmosnand/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for /gaia/class/student/chakraba/cmosnand/LVS/layout/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos

    Net-list summary for /gaia/class/student/chakraba/cmosnand/LVS/schematic/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos


    Terminal correspondence points
    N4          N1          A
    N3          N3          B
    N5          N5          Vdd
    N1          N4          Vss
    N2          N2          Y

Devices in the netlist but not in the rules:
        pmos nmos

The net-lists match.

                             layout  schematic
                                instances
        un-matched                 0       0
        rewired                    0       0
        size errors                0       0
        pruned                     0       0
        active                     4       4
        total                      4       4

                                  nets
        un-matched                 0       0
        merged                     0       0
        pruned                     0       0
        active                     6       6
        total                      6       6

                                terminals
        un-matched                 0       0
        matched but
        different type             0       0
        total                      5       5


Probe files from /gaia/class/student/chakraba/cmosnand/LVS/schematic

devbad.out:

netbad.out:
```

```
mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/chakraba/cmosnand/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

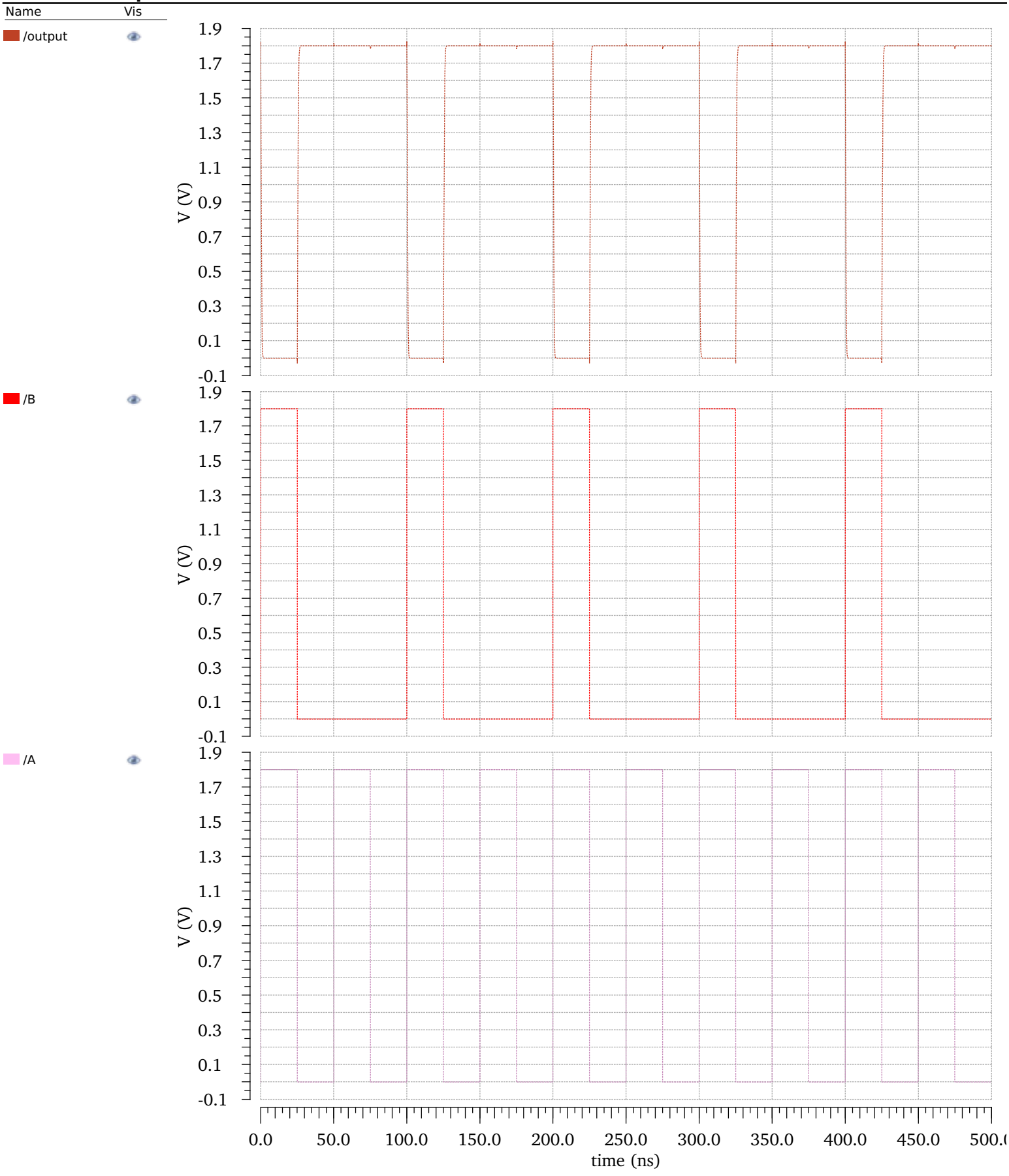
DC Response

Wed Oct 24 01:27:36 2018



Transient Response

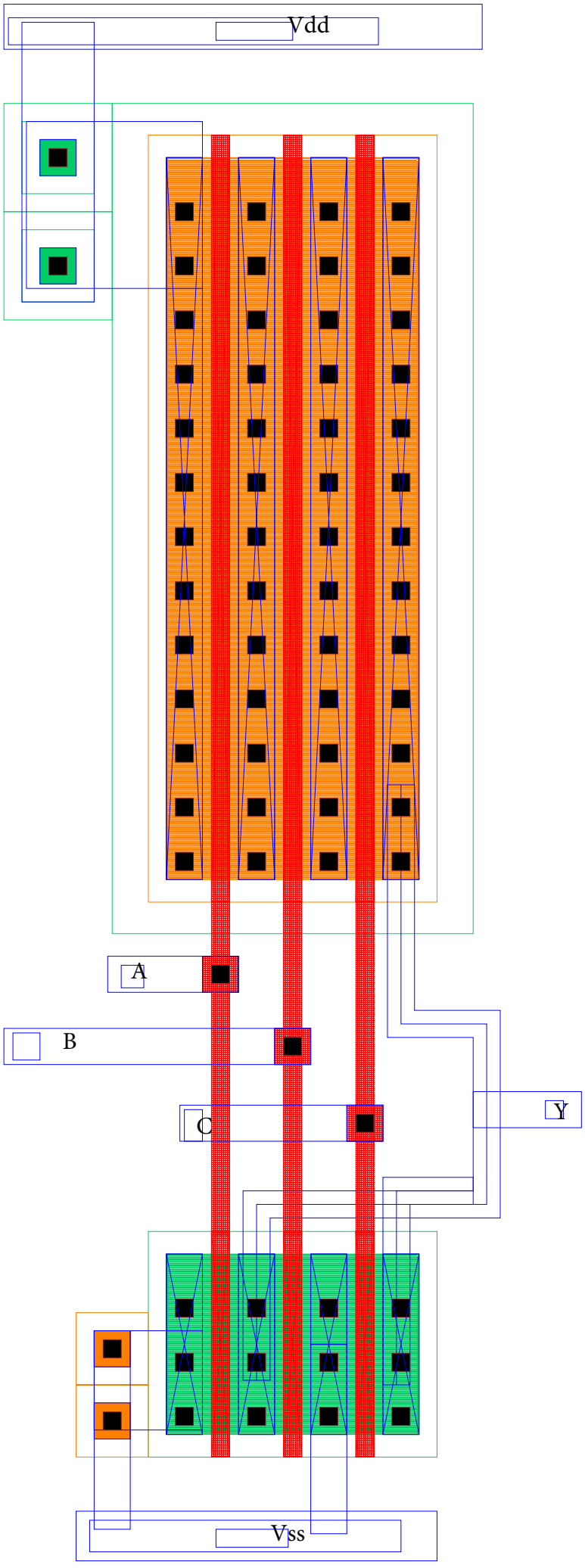
Wed Oct 24 10:15:35 2018



3-INPUT NOR GATE

(W/L)n=1.8/0.18

(W/L)p=7.2/0.18


Vdd
A
B
C
Y
Vss

Virtuoso® 6.1.7-64b - Log: /gaia/class/student/chakraba/CDS.log@thea.ecs.csus.edu

File Tools Options Help

cadence

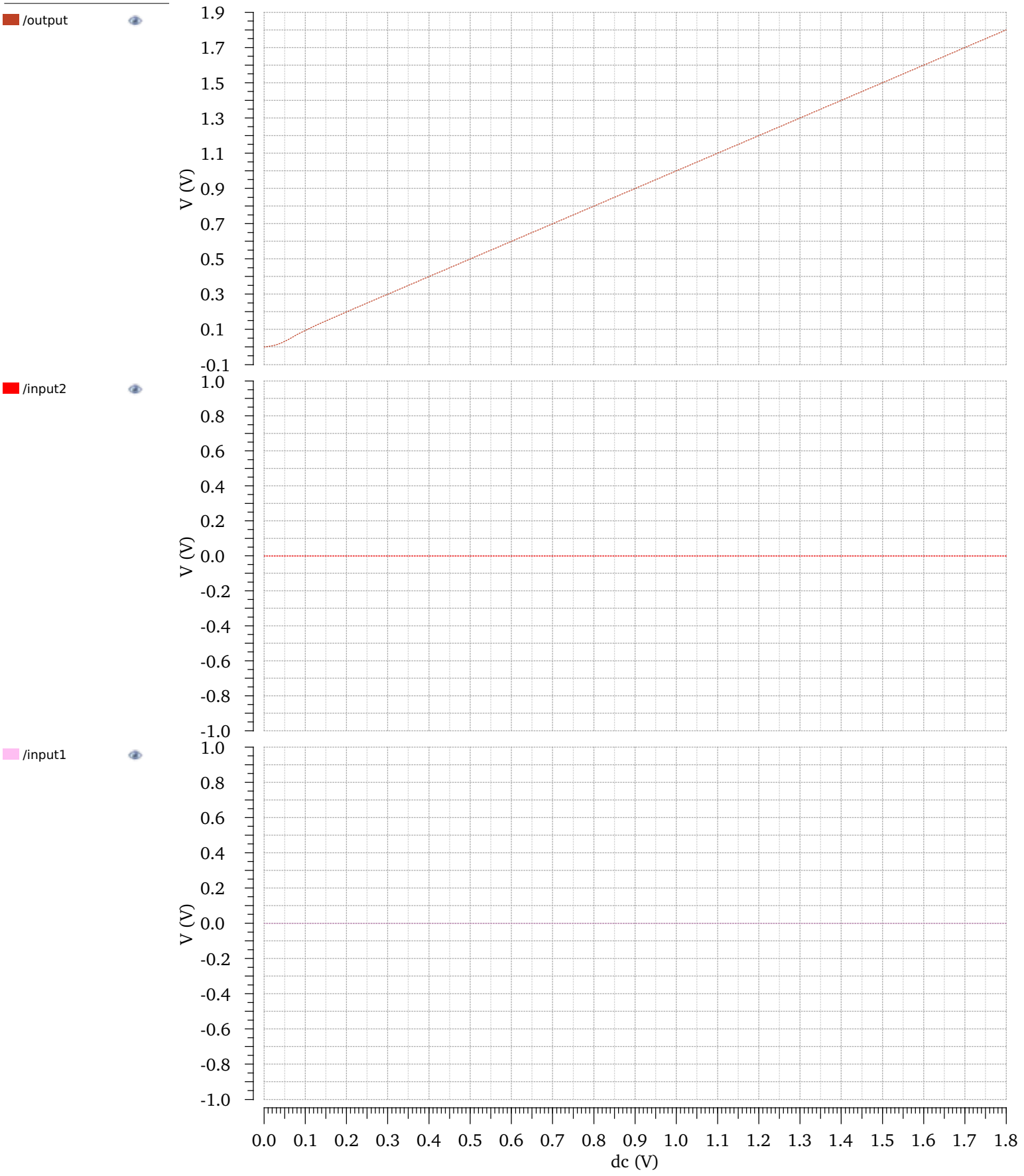
```
DRC started.......Fri Oct 26 12:01:21 2018
    completed ....Fri Oct 26 12:01:21 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "nor_layout layout"   *********
   Total errors found: 0
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/chakraba/cmosnor/LVS -l -s -t
/gaia/class/student/chakraba/cmosnor/LVS/layout
/gaia/class/student/chakraba/cmosnor/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /gaia/class/student/chakraba/cmosnor/LVS/layout/netlist
       count
        8               nets
        6               terminals
        3               pmos
        3               nmos

    Net-list summary for /gaia/class/student/chakraba/cmosnor/LVS/schematic/netlist
       count
        8               nets
        6               terminals
        3               pmos
        3               nmos


    Terminal correspondence points
    N6        N0        A
    N5        N1        B
    N4        N3        C
    N7        N7        Vdd
    N2        N6        Vss
    N3        N4        Y

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   6       6
        total                    6       6

                                 nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   8       8
        total                    8       8

                               terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    6       6


Probe files from /gaia/class/student/chakraba/cmosnor/LVS/schematic

devbad.out:
```

```
netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/chakraba/cmosnor/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

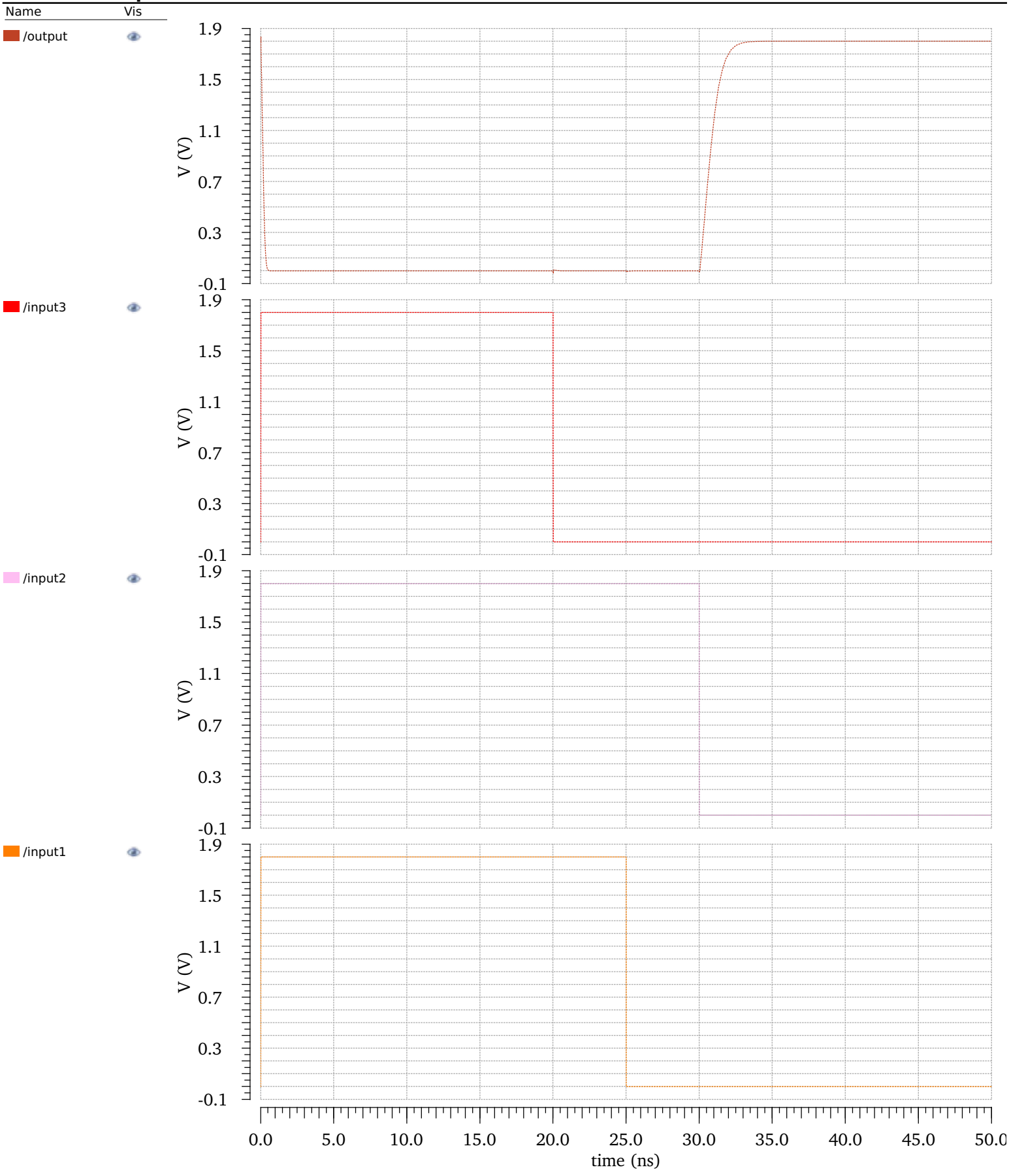
DC Response

Thu Oct 25 03:24:34 2018



Transient Response

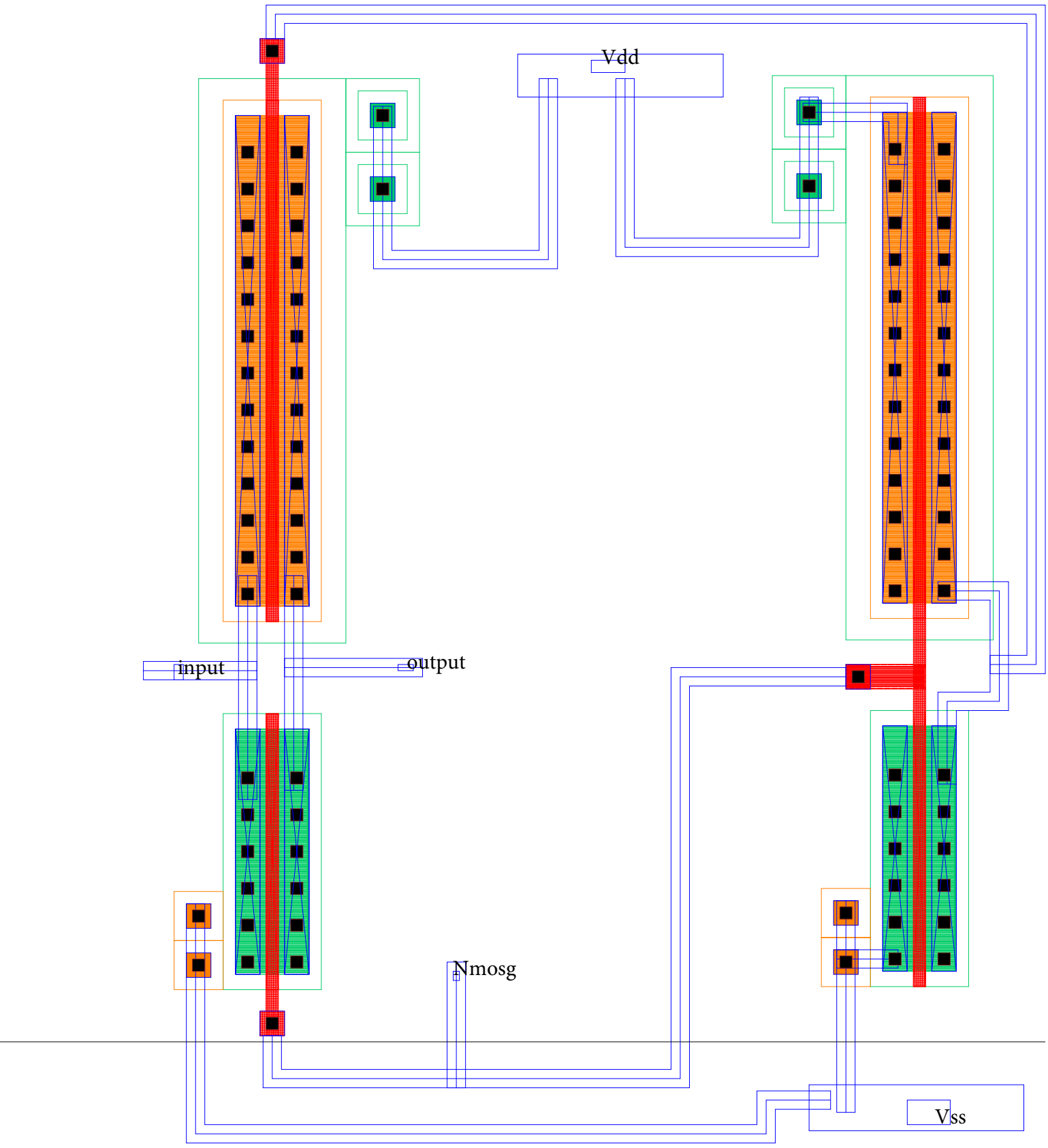
Thu Oct 25 03:32:48 2018



TRANSMISSION GATE

(W/L)n=3.6/0.18

(W/L)p=7.2/0.18


Vdd
input
output
Nmosg
Vss

Virtuoso® 6.1.7-64b - Log: /gaia/class/student/chakraba/CDS.log@thea.ecs.csus.edu

File Tools Options Help

cadence

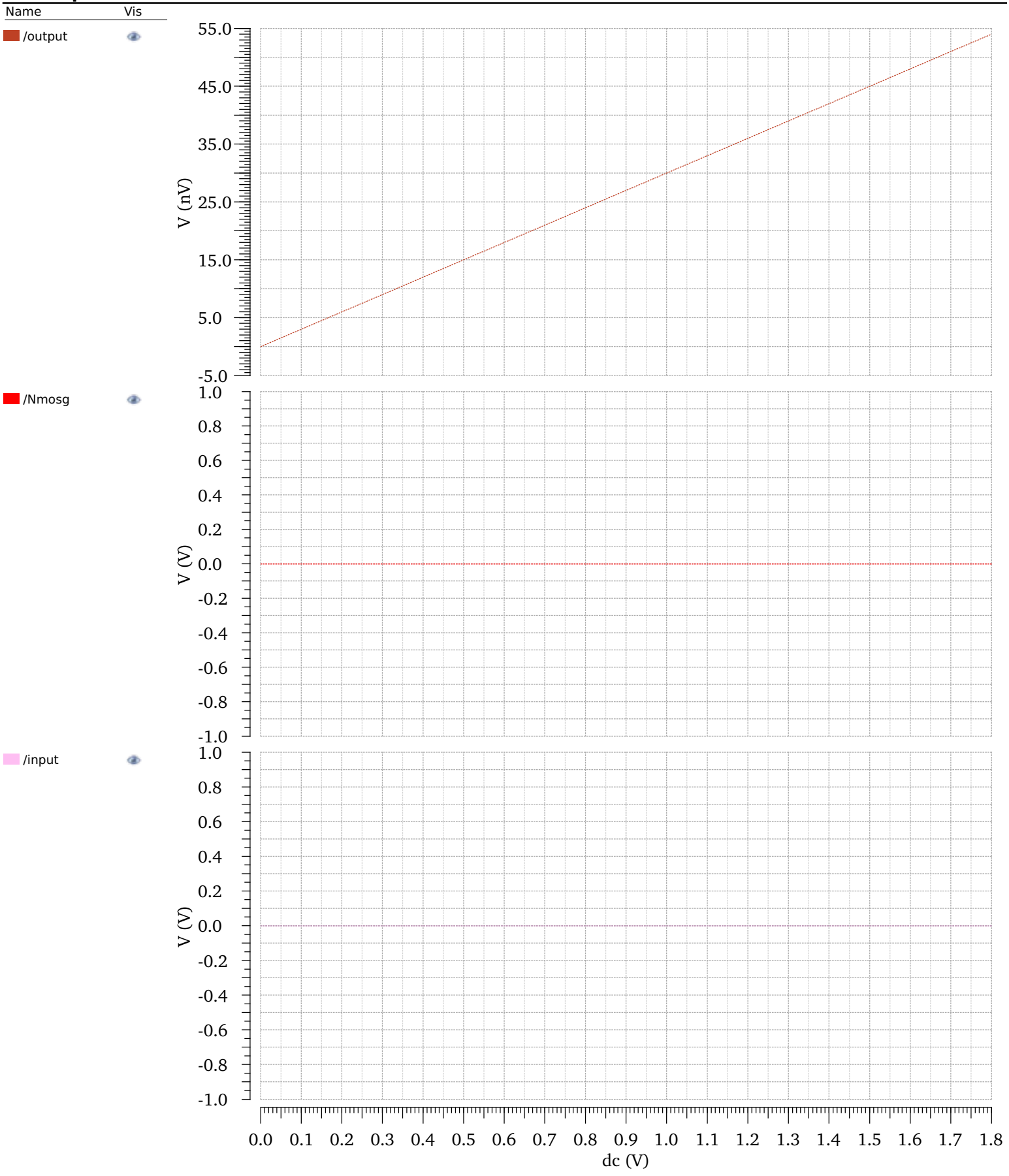
```
DRC started.......Fri Oct 26 12:04:30 2018
    completed ....Fri Oct 26 12:04:30 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "tXGATE_Layout layout"   *********
   Total errors found: 0
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/chakraba/TX/LVS -l -s -t /gaia/class/student/chakraba/TX/LVS/layout
/gaia/class/student/chakraba/TX/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /gaia/class/student/chakraba/TX/LVS/layout/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos

    Net-list summary for /gaia/class/student/chakraba/TX/LVS/schematic/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos


    Terminal correspondence points
    N4          N4          Nmosg
    N5          N3          Vdd
    N1          N0          Vss
    N3          N1          input
    N2          N5          output

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                             layout  schematic
                                instances
        un-matched                 0       0
        rewired                    0       0
        size errors                0       0
        pruned                     0       0
        active                     4       4
        total                      4       4

                                  nets
        un-matched                 0       0
        merged                     0       0
        pruned                     0       0
        active                     6       6
        total                      6       6

                                terminals
        un-matched                 0       0
        matched but
        different type             0       0
        total                      5       5


Probe files from /gaia/class/student/chakraba/TX/LVS/schematic

devbad.out:

netbad.out:
```

```
mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/chakraba/TX/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

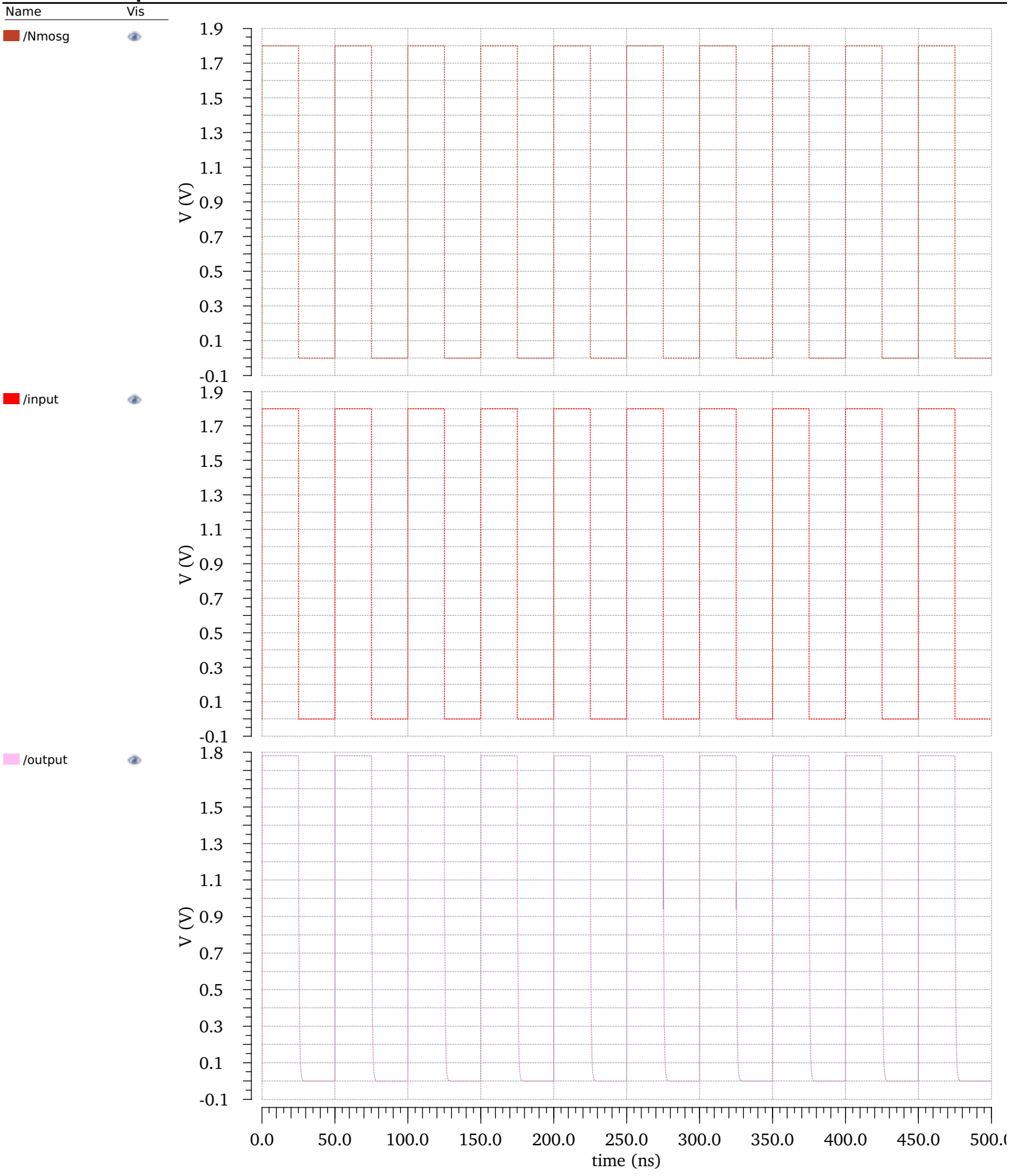
DC Response

Thu Oct 25 22:14:16 2018



Transient Response

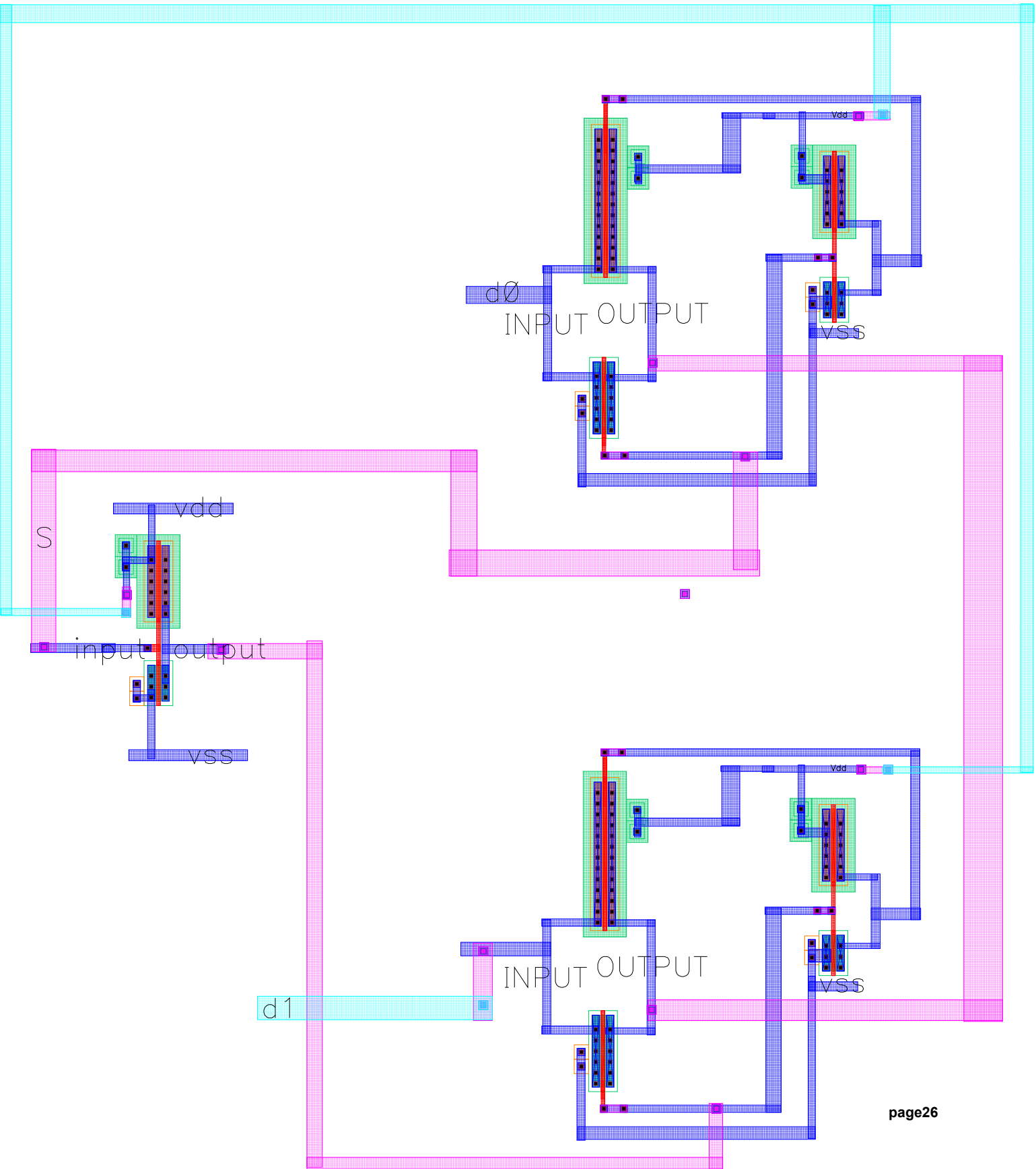
Thu Oct 25 22:23:24 2018



2:1 MUX

(W/L)n=3.6/0.18

(W/L)p=7.2/0.18


d0
INPUT
OUTPUT
Vdd
Vss
S
vdd
input
output
vss
d1
INPUT
OUTPUT
Vdd
Vss

Virtuoso® 6.1.7-64b - Log: /gaia/class/student/chakraba/CDS.log@thea.ecs.csus.edu

File Tools Options Help

cadence

```
DRC started.......Fri Oct 26 12:32:11 2018
    completed ....Fri Oct 26 12:32:12 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "mux_layout layout"   *********
   Total errors found: 0
```

LVS FILE

```
@(#)$CDS: LVS version 6.1.7-64b 10/25/2018 23:41 (sjfhw305) $

Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -
dir /gaia/class/student/chakraba/project1234/LVS -l -s -t
/gaia/class/student/chakraba/project1234/LVS/layout
/gaia/class/student/chakraba/project1234/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

   Net-list summary for /gaia/class/student/chakraba/project1234/LVS/layout/netlist
       count
        9               nets
        0               terminals
        5               pmos
        5               nmos

    Net-list summary for
/gaia/class/student/chakraba/project1234/LVS/schematic/
netlistcount
        9               nets
        6               terminals
        5               pmos
        5               nmos

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  10      10
        total                   10      10

                                 nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  9       9
        total                   9       9
```

	terminals	
un-matched	0	0
matched but different type	0	0
total	0	6

Probe files from /gaia/class/student/chakraba/project1234/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/chakraba/project1234/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

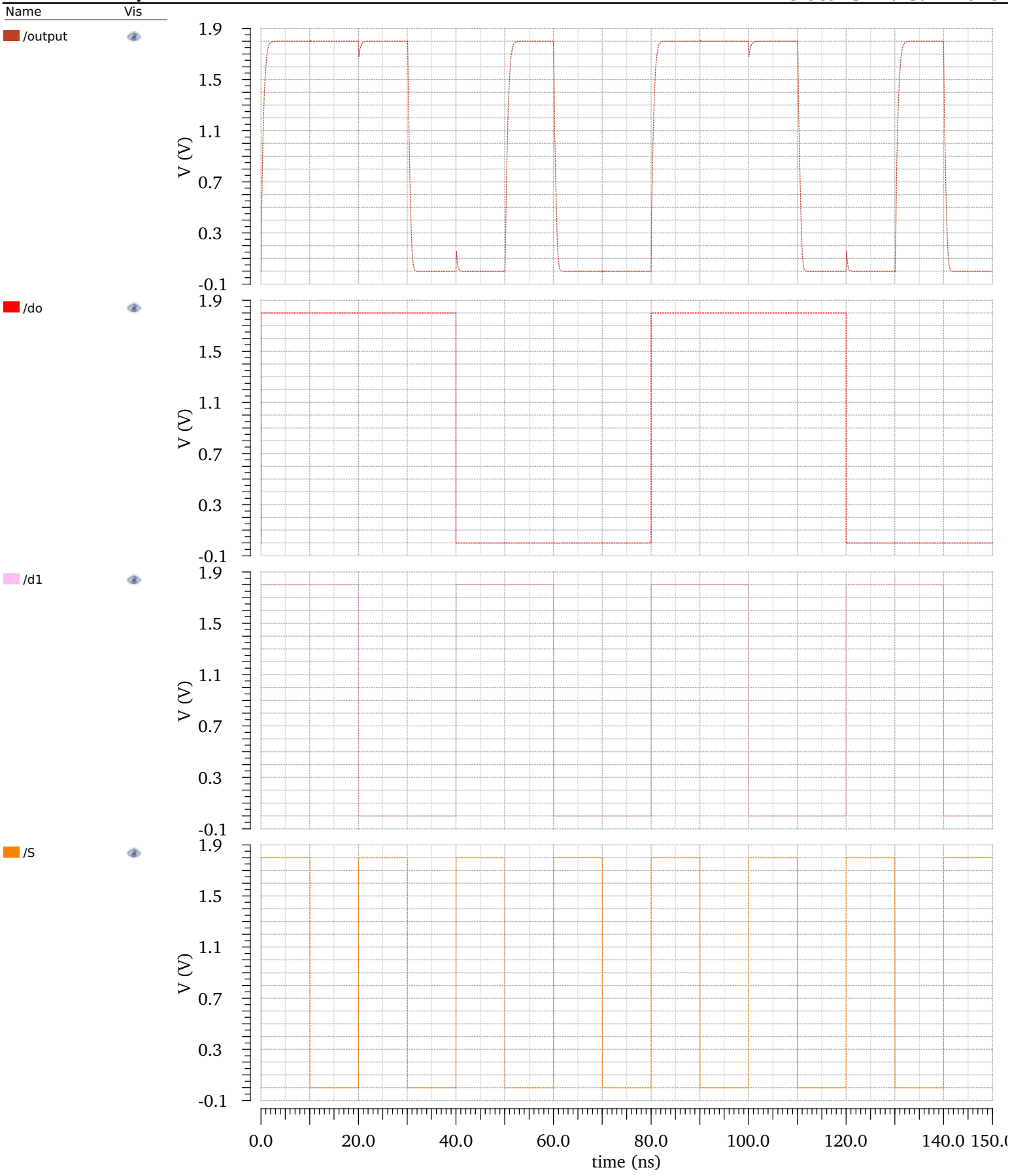
prunenet.out:

prunedev.out:

audit.out:

Transient Response

Thu Oct 25 22:23:24 2018



DC Response

Thu Oct 25 22:23:24 2018