ABHISHEK CHAKRABORTY

1100 Howe Avenue, Sacramento, California (95825), USA

Phone: +19164770425

Email: chakrabortvabhishek.89@gmail.com

LinkedIn: linkedin.com/in/abhishek-chakraborty-84003695

OBJECTIVE

Seeking an internship/co-op position in the field of VLSI, where I can use my technical skills and contribute effectively to your organization.

EDUCATION

Master of Science, Electrical and Electronics Engineering

California State University, Sacramento, CA

Bachelor of Technology, Electronics & Communication Engineering

West Bengal University of Technology, India

RELEVANT COURSEWORK

Analog & Mixed Signal IC Design, Digital IC Design, Advanced VLSI Design

TECHNICAL SKILLS

- Cadence Virtuoso, P-Spice, Xilinx, MATLAB, Multisim
- Windows 95/98/2000/XP/Vista/7/8 . LINUX basic commands
- Semiconductor Physics (Surface potential, work function, electron affinity, fermi energy level of N and P type semiconductor, detailed knowledge about MOSFET capacitance)
- Single stage amplifier, Differential amplifier, Cascade current mirror, current biasing circuit, source follower circuit
- Operation of MOSFET in sub-threshold region and Low power CMOS circuit designing techniques.

WORK EXPERIENCE

Technical Assistant, Adamas Institute of Technology, Kolkata, India

2011 - 2018

Expected: May 2020

May 2010

- I was assigned in lab classes like EDA & VLSI design, Analog and Digital Electronics, Digital Signal processing, Computer Architecture. I also handled 7 student projects as one of their team guides
- I had great association with the R&D division of the university where I handled so many state level projects that include transistor level circuit designing, implementation of low power and low voltage designing techniques, Layout generation, Post layout simulation, DRC checking and LVS report generation. I also worked with Spartan3 FPGA kit.

ACADEMIC PROJECTS

Designing of an operational Amplifier in 0.35um Technology Process (P-Spice)

Designed a Telescopic op-amp circuit for given specifications. Determined the dimensions of the transistors based on the Theoretical definition and fine- tuned the performance of the op-amp on P-Spice to achieve the desired performance metrics.

• Designing, Simulation and Layout of a 4 bit ALU (Cadence Virtuoso)

Designed an ALU which can perform operations like addition, subtraction and multiplication. Created each module(adder, subtractor and multiplier) separately using universal logic gates and integrated the modules into an ALU. Created schematic and layout for every individual universal gate and using these schematic and layout, made the layout of every module. Performed pre-layout simulation, DRC check and LVS operation, created Test Bench schematic and calculated rise and fall times.

• Mobile Jammer Circuit

Jammer circuit was designed with three basic sub-circuits-RF amplifier, Voltage controlled oscillator and tuning circuit. This circuit can block the signal within 100 meter radius. 3V power supply was used for this circuit.

• DIY Hearing AID Circuit Using 555 Timer IC

A quad op-amp IC(LM324), which has 4 integrated op-amp circuit, was used. Among 4 op-amp, only 2 op-amp were used (one as comparator and other one as unity follower). A IC555 was used in Monostable mode.

• MOSFET Audio Amplifier Circuit

Designed MOSFET audio power amplifier circuit with TL071C and 2 MOSFETS(IRF9530 & IRF530) can deliver up to 45W on 8Ω speaker or 70W on 4Ω speaker. Here, the MOSFETS must be mounted on a heat sink with at least 1K/W.

• Saw-tooth Wave Generator Using NE555 Timer and UA741 Op-amp IC

Here IC NE555 Timer is wired as an Astable Multivibrator with unequal ON and OFF times. Resistor R1,R2 and Capacitor C set the ON OFF time period. Asymmetric square wave is available at pin 3 of the IC.

• Motion Detection Using NE555 Timer

The circuit is built around 230V AC primary to 9V DC, 300mA secondary transformer, bridge rectifier DB107, 6V voltage regulator(IC7806), NE555 Timer and few other components.

PUBLICATION

Chakraborty, Abhishek, "Low Power Low Voltage Operation of Operational Amplifier", Int.J. Res. Eng. Technol 4 (2015):297-300