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Total No. of Questions : 9] [Total No. of Printed Pages : 7

(1049)

B.C.A. (CBCS) RUSA IInd Semester Examination

4387

DIGITAL ELECTRONICS

Paper : BCA-0203

Time : 3 Hours] **[Maximum Marks : 70**

Note :– Attempt *five* questions in all, selecting one question each from Unit–I to Unit–IV. Part–A (Q. No. 1) is compulsory.

Part–A

(Compulsory Question)

1. (A) Attempt all parts. Select the correct option for MCQ's.

(i) The output of an AND gate with 3-inputs A, B and C is HIGH when :

(a) A = 1, B = 1, C = 0

(b) $A = 0, B = 0, C = 0$

(c) $A = 1, B = 0, C = 0$

(d) $A = 1, B = 1, C = 1$

(ii) When used with an IC, what does the term 'QUAD' indicate ?

(a) 2 circuits

(b) 4 circuits

(c) 8 circuits

(d) 6 circuits

(iii) The format used to present the logic output for the various combinations of logic inputs to a gate is called a (an) :

(a) Boolean Constant

(b) Boolean Variable

(c) Truth Table

(d) Input Logic Function

(iv) Which of the following expressions is in the sum-of-products (SOP) form ?

(a) (A + B) (C + D)

(b) (A) B (CD)

(c) AB + CD

(d) AB (CD)

(v) The commutative law of Boolean addition states that A + B = A × B. (True/False)

(vi) The Boolean expression C + CD is equal to ..... .

(vii) When transistors are used in digital circuits they usually operate in the :

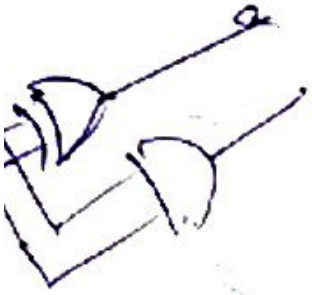
(a) active region

(b) breakdown region

(c) saturation and cutoff regions

(d) linear region

(viii) On the Master-Slave flip-flop, when it is master enabled ?



(a) When the gate is HIGH

(b) When the gate is LOW

(c) Both of these

(d) None of these

(ix) Under normal conditions a diode conducts current when it is :

(a) Reverse biased

(b) Forward biased

(c) Saturated

(d) Avalanched

(x) An *n*-type semiconductor material :

(a) is intrinsic

(b) has trivalent impurity atoms added

(c) has pentavalent impurity atoms added

(d) requires no doping $1 \times 10 = 10$

(B) Answer the following in **25** to **50** words :

(i) State the associative property of Boolean Algebra.

(ii) What is meant by Karnaugh map method ?

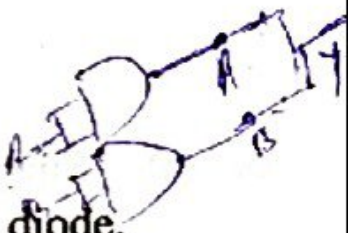
(iii) State advantages and disadvantages of TTL.

(iv) What is a Decoder ?

(v) Define Minterm and Maxterm. 4×5=20

Part–B

(Unit–I)



2. (a) Discuss the working of *p-n* junction diode.

(b) Explain energy bands in solids. 5,5

3. (a) Discuss Saturated and Non-saturated Logic.

(b) Which is faster ECL or TTL ? Explain. 5,5

Part–C

(Unit–II)

4. (a) Simplify the expressions using Boolean Algebra :

(i) $A\bar{B}C + ABC$

(ii) $(\bar{A} + B + C)(A + B + \bar{C})$

(b) Give the circuit diagram of XOR gate. Also give its truth table. 4,6

5. (a) How can you connect NAND gates to get an OR gate ?

(b) What are the two basic rules used to draw equivalent gates ? 6,4

Part–D

(Unit–III)

6. (a) Simplify the following function in sum-of-product SOP form using four variable Karnaugh's map :

$F(A, B, C, D) = \Sigma m (0, 1, 2, 3, 4, 5, 7, 11, 15)$

(b) What are redundant groups in K-map ? 8,2

7. (a) Explain how basic gates can be realized using NAND gates. Also give the diagram.

(b) What do you mean by Combinational Circuit ? 6,4

Part–E

(Unit–IV)

8. (a) What is a Multiplexer ? Explain difference between MUX and DEMUX.

   (b) What do you mean by Shift-Registers ? Discuss. 5,5

9. (a) Explain the working and circuit of a Half-Adder.

   (b) Give the design of 3 × 8 decoder. 6,4