Gowin YunYuan Software

Release Note

RN100-1.9.3.01BetaE, 01/16/2020

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1 About This Release

The release of Gowin YunYuan software V1.9.3.01Beta includes the followings:

- Device added: GW2A-55C, GW2A-18C, GW2AR-18C;
- PN added: GW1N-UV4MG132XES, GW1N-UV4MG132XC6/I5, GW1N-UV4MG132XC5/I4, GW1N-LV4MG132XES, GW1N-LV4MG132XC6/I5, GW1N-LV4MG132XC5/I4;
- IP added: AHB to APB 32 Bridge, AHB To AHB Sync, AHB To AHB APB Async, AHB Bus Arbiter;
- IP updated: PDM2PCM, Gowin_Flash_controller, Scaler, Gowin_EMPU_M1;
- IP renamed: Divider renamed as Fixed Point Divider, Wb_Async_Bridge renamed as WB Async Bridge;
- Primitives added: CLKDIV2;
- IP core supports GowinSynthesis and synplifyPro, and the default is GowinSynthesis;
- GW1NZ-1 disables DP x1, x2, x4, x8, x9 bit width;
- GW1N-9 disables DP mode.

For the complete functions and enhancements of this release, please refer to 2 Function and Enhancement Summary.

Note!

GowinSynthesis is needed to support 32-bit system.

2 Function and Enhancement Summary

The following table summarizes the functions and enhancements:

Function	Description
Yun Yuan software: V1.9.3.01Beta	
Functions	● Device added: GW2A-55C, GW2A-18C, GW2AR-18C; ● PN added: GW1N-UV4MG132XES, GW1N-UV4MG132XC6/I5, GW1N-UV4MG132XC5/I4, GW1N-LV4MG132XES, GW1N-LV4MG132XC6/I5, GW1N-LV4MG132XC5/I4; ● IP added: AHB to APB 32 Bridge, AHB To AHB Sync, AHB To AHB APB Async, AHB Bus Arbiter; ● Primitives added: CLKDIV2; ● GW1NZ-1 disables DP x1, x2, x4, x8, x9 bit width; ● GW1N-9 disables DP mode.
Enhancements	● IP updated: PDM2PCM, Gowin_Flash_controller, Scaler, Gowin_EMPU_M1; ● IP renamed: Divider renamed as Fixed Point Divider, Wb_Async_Bridge renamed as WB Async Bridge; ● IP core supports GowinSynthesis and synplifyPro, and the default is GowinSynthesis.

3 Platform Supported

The software is supported on the platforms listed below:

Windows	Windows 7/8/10(32bit/64 bit) Windows XP/7（32bit）
Linux	Centos6.8/7.0/7.5(64 bit) Ubuntu 18.04 LTS

4 Ports

Port No.	Port Type	Port Description
36545	User-defined protocol port	Used to communicate with JTAG SERVER for the GAO (Gowin Analyzer Oscilloscope) display.
36546	User-defined protocol port	Used to communicate with JTAG SERVER for the GAO (Gowin Analyzer Oscilloscope) display.
10559	User-defined protocol port	The license server port of the Gowin software back-end tool.
27020	TCP port	The license server port of the Gowin software front-end tool "synplifyPro".

5 Environment Variables Setting

LM_LICENSE_FILE Environment Variables Setting

1. Node-Locked license variable value: The license files location, such as: "D:\Synopsys\license.txt"
2. Floating license variable value: license files location, such as: 27020@192.168.31.220. "192.168.31.220" is the IP address of starting the floating license.

6 Documents

The released documents are listed in the table below and the PDF version is packaged in the installation directory.

Documents	Usage
SUG100-2.2E_Gowin YunYuan Software User Guide.pdf	PDF
SUG101-1.9E_Gowin Design Constraints User Guide.pdf	PDF
SUG114-2.0E_Gowin Analyzer Oscilloscope User Guide.pdf	PDF
SUG282-1.7E_Gowin Power Analyzer User Guide.pdf	PDF
SUG283-2.0E_Gowin Primitive User Guide.pdf	PDF
SUG284-1.9E_Gowin IP Core Generator User Guide.pdf	PDF

7 Known Issues

The following issues will be fixed in the next version.

1. It is not available to generate IP soft core using the GAO and IP Core with 32-bit system for the time being;
2. Hierarchy display does not support VHDL design parse. When adding VHDL design, the IDE output window will report error message, but synplifyPro is not affected to use;
   ERROR: Hierarchy can not support VHDL;
3. GowinSynthesis does not support VHDL design synthesis. When synthesis contains VHDL design, the IDE output window will report the error message. Please use synplifyPro for synthesis;
   Error (EXT3044): Analyze: cannot read format vhdl in this product.
   Error (EXT0304): Fail to analyze the input design file.
4. Try to reduce the number of capture signals and capture depth if there are any problems with the GAO capturing. If the problem still exists, please contact GOWINSEMI technical support;
5. For DSP rtl design synthesis, the synthesis tool does not support the followings. If the synthesis problem exists, please contact GOWINSEMI technical support;
   - ALU54D does not support ACCLOAD_REG mapping in the asynchronous mode;
   - The MULTALU36X18/MULTADDALU18X18 outputs may not be synthesized into mode 2 when passing through registers.

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