Gowin YunYuan Software

User Guide

SUG100-2.1E,11/28/2019

Disclaimer

Revision History

Date	Version	Description
09/06/2018	1.2E	Initial version published.
11/06/2018	1.3E	GW1NZ-1 and GW1NSR-2C supported.
11/15/2018	1.4E	● GW1N-6ES, GW1N-9ES and GW1NR-9ES devices removed; ● GW1N-1-MBGA160 and GW1N-1-PBGA204 packages removed; ● GW1NSR-2 supported; ● GW2AR-18-eLQFP144 package added.
02/12/2019	1.5E	● The Log file of license installed successfully added.
03/01/2019	1.6E	● Figures in this manual updated; ● The description of Convert FDC tool added; ● The function of enable/disable description added; ● The synthesis tool of GowinSynthesis added.
05/17/2019	1.7E	● GW1N-1S device supported; ● Programmer and GAO added in toolbar and Tools menu bar; ● Convert FDC removed from Tools menu bar; ● Stop function of Synthesize and PnR added; ● Hierarchy display window added; ● GW2A-18- eLQFP144 package added; ● GW1N-9- eLQFP144 package added; ● GW1NR-9-MBGA100 package added; ● GW2A-18-PBGA256C package added; ● GW2A-18-eLQFP176 package added.
08/15/2019	1.8E	● GW1N-4S, GW1NS-4 and GW1NSE-2C devices supported; ● Project added in the menu bar; ● User Flash initialization file creation supported; ● Archive Project function added.
09/26/2019	1.9E	● GW1NSR-4 and GW1NSER-4C devices supported; ● GW1N-4S device removed; ● File mode of place and route tool License loading added.
11/08/2019	2.0E	● Synplify Pro configuration options added; ● Synplify Pro attributes and the value of directives added.
11/28/2019	2.1E	● GW1NSE-2C, GW1NRF-4B and GW1NSR-4C devices supported; ● GW1N-9-UBGA169 and GW1N-9-eLQFP176 added; ● GW2A-55-UBGA324 added； ● GW2A-18-UBGA324 added； ● GW1N-1S-WLCSP30 added； ● GW1NS-4-WLCSP49 added; ● Speed GW2AR-18-eLQFP144C9/I8 added； ● Speed GW1N-9-MBGA160C6H added; ● GW1NSR-4-QFN48P and GW1NSR-4-QFN48G added; ● General option added in Place & Route: Promote Physical Constraint Warning to Error, Report Auto-Placed IO Information, Place Option, Route Option; ● Resource information display added in Hierarchy view;

		● Three "Find" options supported in netlist file in Process view; ● Function of adding and removing comments supported in IDE built-in editor.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

This manual predominantly documents Gowin software installation and operation and is designed to help users employ the software functionality to aid complex design. The software screenshots and the supported products listed in this manual are based on Windows 1.9.3Beta. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Supported Products

The information presented in this guide applies to the following products:

- GW1N series of FPGA products: GW1N-1, GW1N-1S, GW1N-2, GW1N-2B, GW1N-4, GW1N-4B, GW1N-6, GW1N-9
- GW1NR series of FPGA products: GW1NR-4, GW1NR-4B, GW1NR-9
- GW1NS series of FPGA products: GW1NS-2, GW1NS-2C, GW1NS-4
- GW1NSE series SecureFPGA products: GW1NSE-2C
- GW2A series of FPGA products: GW2A-55 and GW2A-18
- GW2AR series of FPGA products: GW2AR-18
- GW1NZ series of FPGA products: GW1NZ-1
- GW1NSR series of FPGA products: GW1NSR-2C, GW1NSR-2, GW1NSR-4
- GW1NSER series of SecureFPGA products: GW1NSER-4C
- GW1NRF series of Bluetooth FPGA products: GW1NRF-4B

1.3 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS100, GW1N series of FPGA Products Data Sheet
2. DS117, GW1NR series of FPGA Products Data Sheet
3. DS821, GW1NS series of FPGA Products Data Sheet
4. DS102, GW2A series of FPGA Products Data Sheet
5. DS226, GW2AR series of FPGA Products Data Sheet
6. DS841, GW1NZ series of FPGA Products Data Sheet

7. DS861, GW1NSR series of FPGA Products Data Sheet
8. DS871, GW1NSE series of SecureFPGA Products Data Sheet
9. DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet
10. SUG101, Gowin Design Constraints Guide
11. SUG113, Gowin FPGA Design Guide
12. SUG114, Gowin Analyzer Oscilloscope User Guide
13. SUG282, Gowin Power Analyzer User Guide
14. SUG284, Gowin IP Core Generator User Guide

1.4 Abbreviations and Terminology

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Meaning
CRC	Cyclic Redundancy Check
CS	Wafer Level Chip Scale Package
DLL	DLL
FPGA	Field Programmable Gate Array
FF	Flip-Flop
IDE	Integrated Development Environment
IP Core	Intellectual Property Core
LQ	Low-profile Quad Flat Package
MAC	Media Access Control
MG	Micro Ball Grid Array Package
PC	Personal Computer
PLL	PLL
PG	Plastic Ball Grid Array
QN	Quad Flat No-lead Package
RTL	Register Transfer Level
UG	Ultra Ball Grid Array Package
PnR	Place & Route

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

Tel: +86 755 8262 0391

2 Overview of YunYuan Software

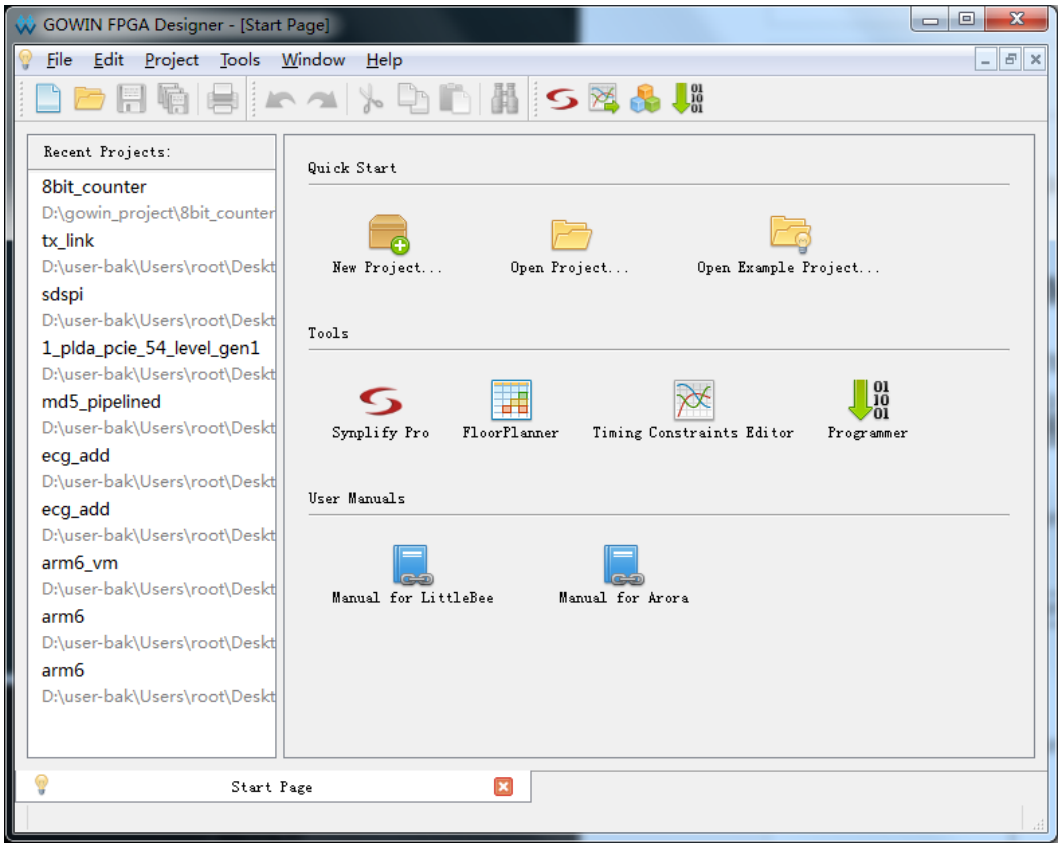
2.1 Introduction

Gowin YunYuan Software is the new hardware development design environment for Gowin products. It supports generic hardware description language, and helps users to quickly implement code synthesis, manage placement and routing, generate and download bitstreams, etc. The Gowin Yunyuan Software also incorporates the IP Core Generator, which is dedigned to help developers quickly implement complex designs and the online debug tool, Gowin Analyzer Oscilloscope, which can help users to efficiently identify and assess signal design issues.

To meet different user demands, the input file for the projects created in Gowin YunYuan Software can either be the RTL design file written in a hardware description language or the netlist file generated by user RTL synthesis.

The Gowin YunYuan Software provides a GUI for projects. Users can employ this software to quickly edit the constraints files, check the running results of Synthesize and Place & Route, and start the GOWINSEMI FPGA download tool immediately to download the bitstream to the chip and implement the required functions. The interface of Gowin YunYuan Software is as shown in Figure 2-1.

Figure 2-1 Gowin Yun Yuan Software Interface



2.2 Supported Devices

Table 2-1 lists the devices Gowin YunYuan software supports and the associated resources, packages, and speed.

Table 2-1 Devices Supported

Device	LUT4s	Flip-Flops	MULT18 x 18	PLL	Package	Speed
GW1N-1	1,152	864	0	1	WLCSP30 QFN32 QFN48 LQFN100 LQFN144	4/5/6
GW1N-1S	1,152	864	0	1	QFN32	5/6
GW1N-2	2,304	1,728	16	2	WLCSP72 QFN32 QFN88 QFN48 LQFP100 LQFP144 MBGA160 PBGA256 PBGA256M	4/5/6
GW1N-2B	2,304	1,728	16	2	WLCSP72 QFN32	

Device	LUT4s	Flip-Flops	MULT18 x 18	PLL	Package	Speed
					QFN88	
					QFN48	4/5/6
					LQFP100	
					LQFP144	
					MBGA160	
					PBGA256	
					PBGA256M	
GW1N-4	4,608	3,456	16	2	WLCSP72	4/5/6
					QFN32	
					QFN88	
					LQFP100	
					LQFP144	
					MBGA160	
					PBGA256	
					QFN48	
					PBGA256M	
GW1N-4B	4,608	3,456	16	2	WLCSP72	4/5/6
					QFN32	
					QFN88	
					LQFP100	
					LQFP144	
					MBGA160	
					PBGA256	
					QFN48	
					PBGA256M	
GW1N-4S	4608	3456	16	2	WLCSP49	5/6
					QFN48	
GW1NR-4	4608	3456	16	2	QFN88	4/5/6
					MBGA81	
GW1NR-4B	4608	3456	16	2	QFN88	4/5/6
					MBGA81	
GW1N-6	6912	5184	20	2	LQFP144	4/5/6
					UBGA332	
					PBGA256	
					LQFP100	
					QFN88	
					QFN48	
					LQFP176	
					MBGA160	
					WLCSP64	
					UBGA256	
GW1N-9	8640	6480	20	2	LQFP144	4/5/6
					UBGA332	
					eLQFP144	
					eLQFP176	
					PBGA256	

Device	LUT4s	Flip-Flops	MULT18 x 18	PLL	Package	Speed
					LQFP100	
					QFN88	
					QFN48	
					LQFP176	
					MBGA160	
					WLCSP64	
					UBGA169	
					UBGA256	
GW1NR-9	8640	6480	20	2	LQFP144	4/5/6
					MBGA100	
					QFN88	
GW1NS-2	1728	1080	0	1	WLCSP36	4/5/6
					QFN32	
					QFN48	
					LQFP144	
					QFN32U	
GW1NS-2C	1728	1080	0	1	WLCSP36	4/5/6
					QFN32	
					QFN48	
					LQFP144	
					QFN32U	
GW1NSE-2C	1728	1080	0	1	QFN48	5/6
					LQFP144	
GW1NS-4	4608	3456	16	2	WLCSP49	5/6
					QFN48	
GW1NZ-1	1152	864	0	1	WLCSP16	4/5/6
					QFN32	
GW1NSR-2	1512	1080	0	1	QFN48	4/5/6
GW1NSR-2C	1512	1080	0	1	QFN48	4/5/6
GW1NSR-4	4608	3456	16	2	MBGA64P	4/5/6
GW1NSR-4C	4608	3456	16	2	QFN48P	4/5/6
				2	QFN48G	4/5/6
				2	MBGA64P	4/5/6
GW1NSER-4C	4608	3456	16	2	QFN48P	4/5/6
				2	QFN48G	4/5/6
GW1NRF-4B	4608	3456	16	2	QFN48	4/5/6
				2	QFN48E	4/5/6
GW2A-18	20,736	15,552	48	4	PBGA484	6/7/8
					PBGA256	
					PBGA256C	
					LQFP144	
					eLQFP144	
					PBGA256S	
					UBGA324	
					MBGA196	
GW2AR-18	20,736	15,552	48	4	QFN88	6/7/8/9
					LQFP144	
					LQFP176	

Device	LUT4s	Flip-Flops	MULT18 x 18	PLL	Package	Speed
					eLQFP144	
					eLQFP176	
GW2A-55	54,720	41,040	40	6	PBGA484	6/7/8/9
					PBGA1156	
					UBGA324	
					UBGA324D	

Note!

The supported devices may vary according to the software version in use. Please refer to the software you use for more detailed device information.

3 Installation

3.1 Environment Requirement

Windows： Win7/8/10(64bit), Win7/winXP (32bit)

Linux： Centos6/7(64bit), Red Hat 6/7(64bit), SUSE 11/12(64bit)

3.2 Software Download

The Gowin YunYuan software installation packages consist of Windows and Linux versions. They are available for download on the Gowin Website:

- Installation package for Windows: Gowin Yunyuan for win(Vx.x.xbeta).exe, with the download link: http://www.gowinsemi.com/support/download_eda/.
- Installation package for Linux is compressed with the name "Gowin Yunyuan for linux(Vx.x.xbeta).rar". The download link is http://www.gowinsemi.com/support/download_eda/.

Note!

- Users need to register and log on to the Gowin website before downloading the installation package;
- "x" in the installation package "Vx.x.xBeta" means the software version.

3.3 Software Installation

Note!

- You must close anti-virus programs, such as 360 or Kingsoft AntiVirus, etc. before installing Gowin YunYuan software.
- The installation path should not contain any Chinese characters or spaces.
- Before installing any new versions of the Gowin YunYuan software, old versions should be uninstalled.
- Table 3-1 shows the product options for the installation of Gowin YunYuan for Windows.

Table 3-1 Components to Install

Components	Description	Remarks
Gowin FPGA designer GUI	Gowin YunYuan GUI	Installation directory of the corresponding executable file: \x.x\IDE\bin\gowin_ide.exe
Device programmer	Gowin devices download tool, including programmer user documents	● Installation directory of the corresponding executable file: \x.x\Programmer\bin\programmer.exe; ● The corresponding documents directory: \x.x\Programmer\doc.
Synthesis tool	Gowin synthesis tool, including user documents	● Installation directory of the corresponding executable file: \x.x\SynplifyPro\bin\synplify_pro.exe; ● The corresponding documents directory: \x.x\SynplifyPro\doc.

Windows Installation

Refer to the steps below to install the Gowin Yunyuan software on Windows.

1. Double-click on the installer to launch the installation process. Follow the install wizard to complete the installation.

   Note!

   - In the process of installation, users can change the installation directory as required.
   - After installation, the software shortcut will be created on PC desktop by default "  ".

2. Double-click the shortcut "  " to open Gowin YunYuan software.

Linux Installation

Uncompress the software and run the following command path/x.x.xBeta/IDE/bin/gw_ide to open the Software GUI on Linux.

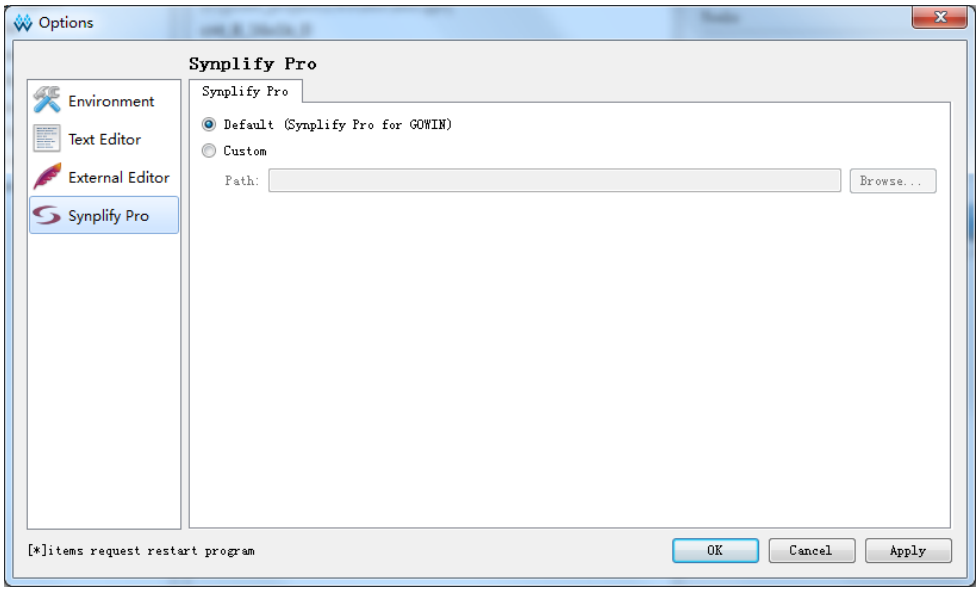
Note!

Root permission is required to start programmer.

Note!

If you have previously installed Gowin Yunyuan software, ensure the installation directory of the new Gowin Yunyuan software is the same as the call path of Select "Tools > Options" from the menu bar, and then select the installation path for SynplifyPro, as shown in Figure 3-1.

Figure 3-1 SynplifyPro Call Path



3.4 Software License Configuration

After setting environment variable "GOWIN_HOME", Gowin YunYuan software licenses are also a must. Gowin YunYuan software licenses include:

- SynplifyPro License;
- Place and Routing License;

Gowin YunYuan software licenses support node-locked license and floating license.

Users can apply for the required licenses on the Gowin website http://www.gowinsemi.com/support/license/.

For license configuration, please refer to 3.5SynplifyPro License and 3.6Place and Route License .

3.5 SynplifyPro License Loading

3.5.1 Node-Locked License

The node-locked license is based on PC MAC and is only suitable for the users of this PC. Please refer to the following steps after acquiring the SynplifyPro Node-Locked License:

Note!

If the other partner's tool was installed in the "C:\Synopsys\" directory, and there is the license file in this directory, conflict issues will occur when Gowin Synplify is searching a license. Because Synplify will search the license in this directory first by default, no matter the environment variables are configured or not.

Taking win7, 64-bit operating system for instance, please refer to the following steps to configure the environment variables.

1. Save license file

   Save the license (licensefile.txt） to the target directory, for example, "E:\Synopsys\licensefile.txt".

2. Configure the license.

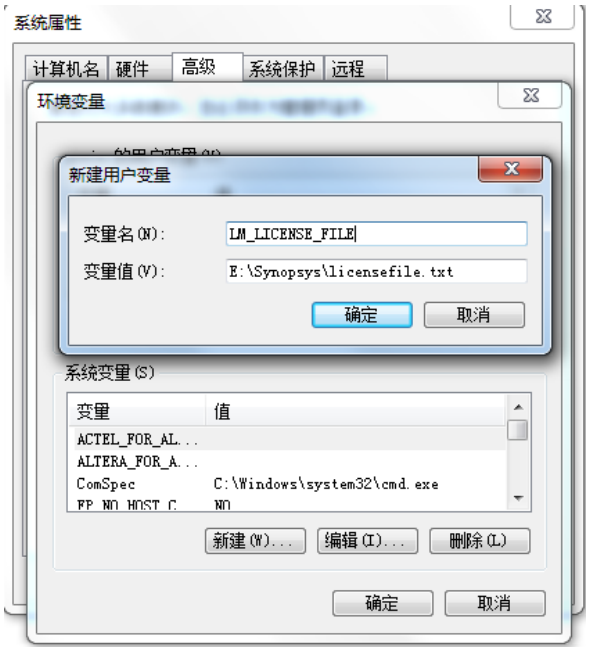
a). Right-click on the "Computer" link, select "properties", and click the "Advanced system settings" to open the "System Properties" window;

b). In the "System Properties" View, click "Advanced > Environment Variables>New" to open the "New User Variable", as shown in Figure 3-2. Enter the variable name and the value in the "New User Variable" dialog box.

- Environment variable name: LM_LICENSE_FILE.
- Variable value: License file location, such as "E:\Synopsys\licensefile.txt".

3. Click "OK".

Figure 3-2 Environment Variables Setting



3.5.2 Floating License

When this configuration is employed, Gowin YunYuan is installed on your license server. Each PC in the LAN can use the floating license. Floating licenses have a user limit.

1. First, start floating license using Synopsys Common Licensing (SCL) in the Yunyuan software installation package file "GowinLicenseServerForWindows\SCL".

   a). Click the "scl_v2018.06_windows.exe" SCL executable file to install the SCL software. Install it according to the wizard steps. Configure the "Site Information" as follows:

   - "Site ID": The "siteid" value of the SynplifyPro License file (such as synp_license.lic), such as 29247;
   - "Site Administrator": The administrator name of this PC;
   - "Contact Information": Optional, the contact information of the administrator;

   b). Select the installation path according to the wizard steps, such as "C:\Synopsys\SCL". Click "next" until the page of installation done appears. For example, the "Completing the SCL 2018.06 Setup Wizard" page appears. Click "Finish" to complete the SCL

installation.

2. Go to the "2018.06\win32\bin" folder in the SCL installation path, "C:\Synopsys\SCL \2018.06\win32\bin", for example. There are two ways to start the floating license. Take Win7, 64 bits operating system for instance:

Commands Mode

a) Modify the PC name in the floating license file and check the MAC address;
for example:
for the "SERVER hostname1 F8BC12950972 27020" content in the license file:
b) "hostname1" should be modified to the PC name;
c) "F8BC12950972" is the PC MAC;
d) "27020" is the port number, which should be modified per the PC installed SynplifyPro, such as "SERVER GaoYun-PC F8BC12950972 27020".
e) Modify the snpslmd path in the floating license file.
On the basis of the "snpslmd.exe" path in SCL, modify this line "VENDOR snpslmd /path/to/snpslmd" in the license file to "VENDOR snpslmd C:\Synopsys\SCL\2018.06\win32\bin\snpslmd.exe", for example;
f) Open the "cmd" window and run the command starting license service. The command is "path\lmgrd.exe" –c "path\licensefile" –l "path\logfile" –z –s;
g) After running, check the log file in the "path\logfile" directory to confirm that if the license has been installed successfully. If yes, the content as shown in Figure 3-3 will appear in the log file.

Figure 3-3 Log File of License Installed Successfully

```
01/28/2019 09:16:06 (snpslmd) Siteid: 29247, Server Hostid: 525400B8ABE7, Issued on: 12/18/2018
01/28/2019 09:16:06 (snpslmd) ------------------------------------------------------------------
 9:16:06 (snpslmd) SLOG: Statistics Log Frequency is 240 minute(s).
 9:16:06 (snpslmd) SLOG: TS update poll interval is 0. TS update is detected by midnight reread only.
 9:16:06 (snpslmd) SLOG: Activation borrow reclaim percentage is 0.
 9:16:06 (snpslmd) (@snpslmd-SLOG@) ================================================
 9:16:06 (snpslmd) (@snpslmd-SLOG@) === Vendor Daemon ===
 9:16:06 (snpslmd) (@snpslmd-SLOG@) Vendor daemon: snpslmd
 9:16:06 (snpslmd) (@snpslmd-SLOG@) Start-Date: Mon Jan 28 2019 09:16:06 CST
 9:16:06 (snpslmd) (@snpslmd-SLOG@) PID: 30659
 9:16:06 (snpslmd) (@snpslmd-SLOG@) VD Version: v11.14.1.3 build 212549 x64_lsb ( build 212549 (ipv6))
 9:16:06 (snpslmd) (@snpslmd-SLOG@)
 9:16:06 (snpslmd) (@snpslmd-SLOG@) === Startup/Restart Info ===
 9:16:06 (snpslmd) (@snpslmd-SLOG@) Options file used: None
 9:16:06 (snpslmd) (@snpslmd-SLOG@) Is vendor daemon a CVD: Yes
 9:16:06 (snpslmd) (@snpslmd-SLOG@) Is TS accessed: No
 9:16:06 (snpslmd) (@snpslmd-SLOG@) TS accessed for feature load: -NA-
 9:16:06 (snpslmd) (@snpslmd-SLOG@) Number of VD restarts since LS startup: 0
 9:16:06 (snpslmd) (@snpslmd-SLOG@)
 9:16:06 (snpslmd) (@snpslmd-SLOG@) === Network Info ===
 9:16:06 (snpslmd) (@snpslmd-SLOG@) Listening port: 37814
 9:16:06 (snpslmd) (@snpslmd-SLOG@) Daemon select timeout (in seconds): 1
 9:16:06 (snpslmd) (@snpslmd-SLOG@)
 9:16:06 (snpslmd) (@snpslmd-SLOG@) === Host Info ===
 9:16:06 (snpslmd) (@snpslmd-SLOG@) Host used in license file: swlicense
 9:16:06 (snpslmd) (@snpslmd-SLOG@) Running on Hypervisor: Not determined - treat as Physical
 9:16:06 (snpslmd) (@snpslmd-SLOG@) ================================================
```

SCL Configuration Mode

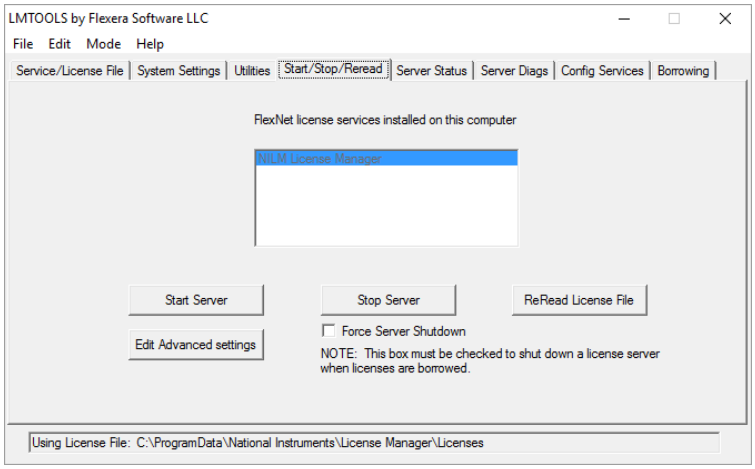
a) Modify the PC name in the floating license file and check the MAC

address;

b) Modify the snpslmd path in the floating license file.

c) Start "lmtools.exe" in snpslmd path; the GUI is as shown in Figure 3-4;

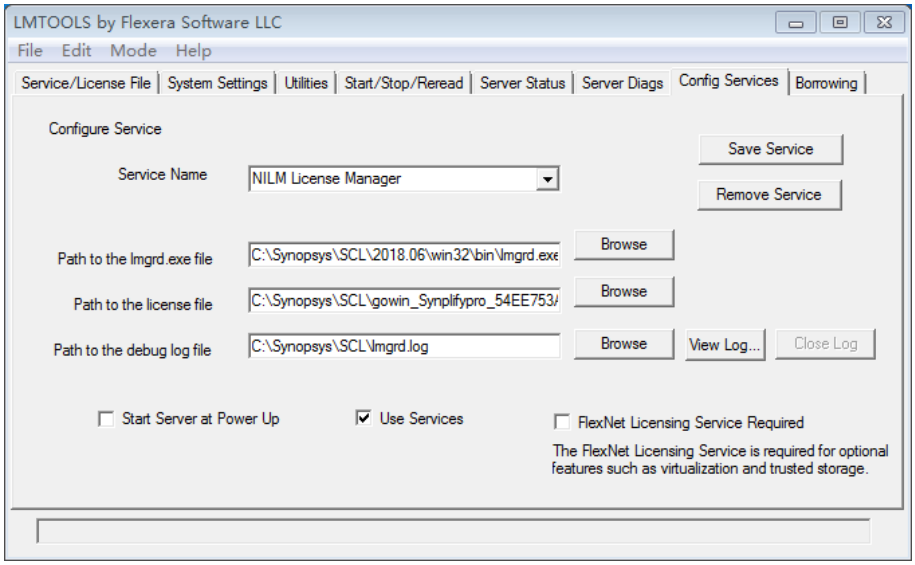
Figure 3-4 SCL Start Interface



d) In Figure 3-5, select "Config Services" to set the related files path;

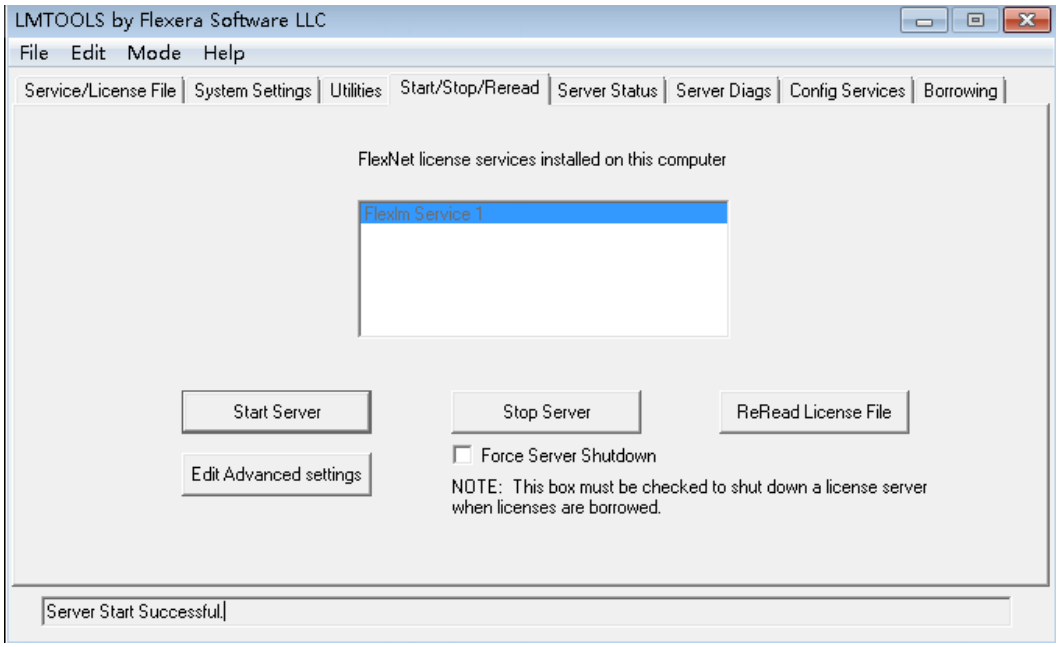
- "Path to the lmgrd.exe file": lmgrd.exe file path;
- "Path to the license file": license file path;
- "Path to the debug log file": the path of the log file after loading license. If there is no log file, the user will need to create one before configuration.

Figure 3-5 SCL Configuration Interface



e) In Figure 3-6, start the license server after configuration. Select "Start/Stop/Reread", and then click "Start Server". If "Server Start Successful" displayed, the server has started successfully. Log file can also be checked to see if the server has started successfully. Click "View Log" in Figure 3-5 to see the log file.

Figure 3-6 SCL License Start

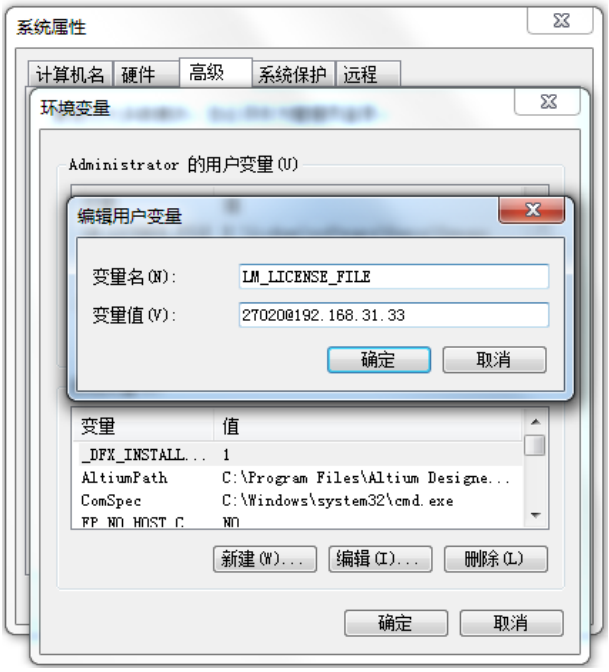


Note!

After starting server license, the system environment variable "LM_LICENSE_FILE" is required to be configured before the configuration of the SynplifyPro floating license. As shown in Figure 3-7:

- Environment Variable name: LM_LICENSE_FILE;
- Environment Variable value: License files location, such as: 27020@192.168.31.33, and "192.168.31.33" is this PC IP address.

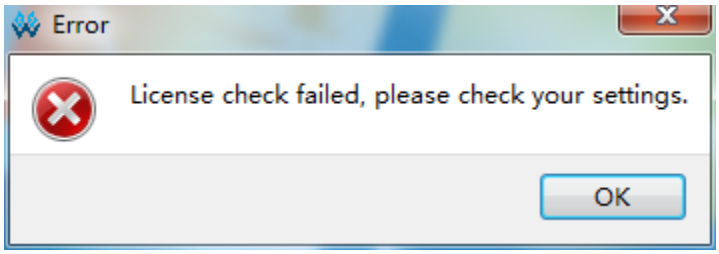
Figure 3-7 Environment Variables Setting



3.6 Place and Route License Loading

Gowin YunYuan software checks the license automatically when the user opens it. If the license is not correct, the software will not open, and an error message will be displayed, as shown in Figure 3-8.

Figure 3-8 License Error

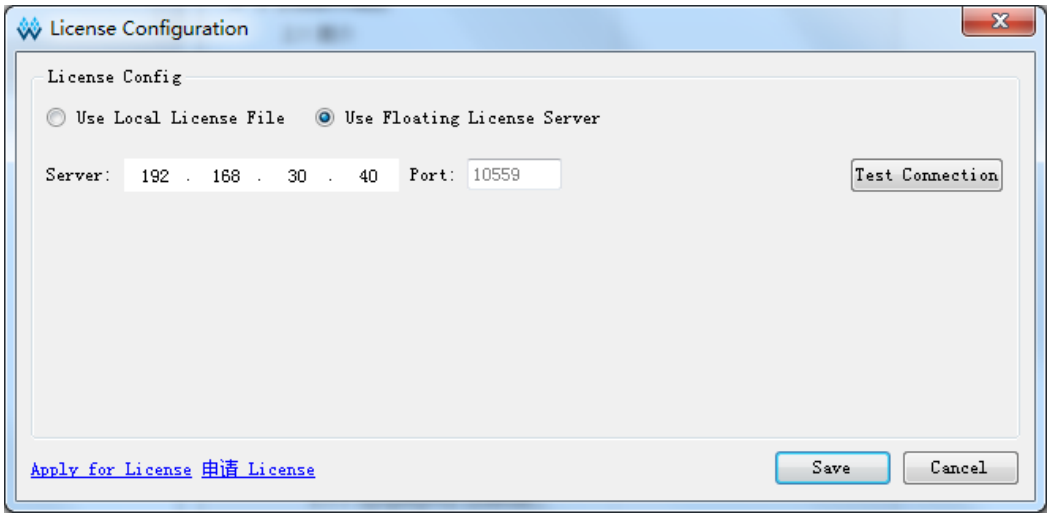


Users can configure the license after the YunYuan software has been installed. See the steps as below:

Interface Configuration Mode

1. Open Gowin YunYuan software. Click "Help> Manage License…" in the menu bar to open the "License Configuration", as shown in Figure 3-9.

Figure 3-9 Manage License options



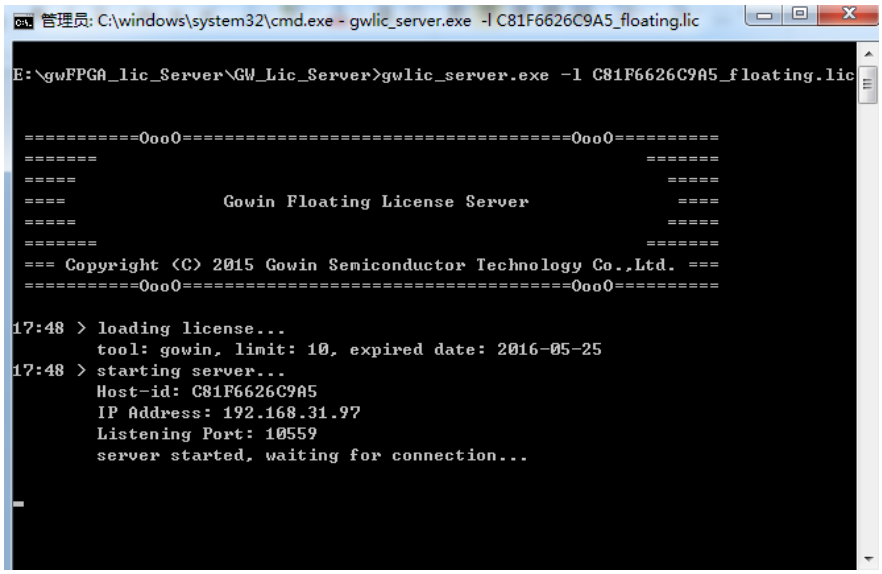
2. User can choose local license file or floating license file.
   - Use Local License File
     Select "Browse…" to add the file path for node-locked License.

     Note!

     If there is no License file, click "Apply for License" or "Shenqing License" in the lower-left of the "License Configuration" View to apply. "Apply for License" is for English, and "Shenqing License" is for Chinese.
   - Use Floating License Server
     Start floating license using PnrLicenseServer in Yunyuan software installation package file "GowinLicenseServerForWindows\PnrLicenseServer". There are two ways to start PnrLicenseServer:
     a). Doubel click on "gwlic_server.exe";
     Copy the floating license file (gowin_license.lic, for example) to "GowinLicenseServerForWindows\PnrLicenseServer". Rename the floating license file as "gowin.lic". Double click "gwlic_server.exe".
     b). Commands Mode

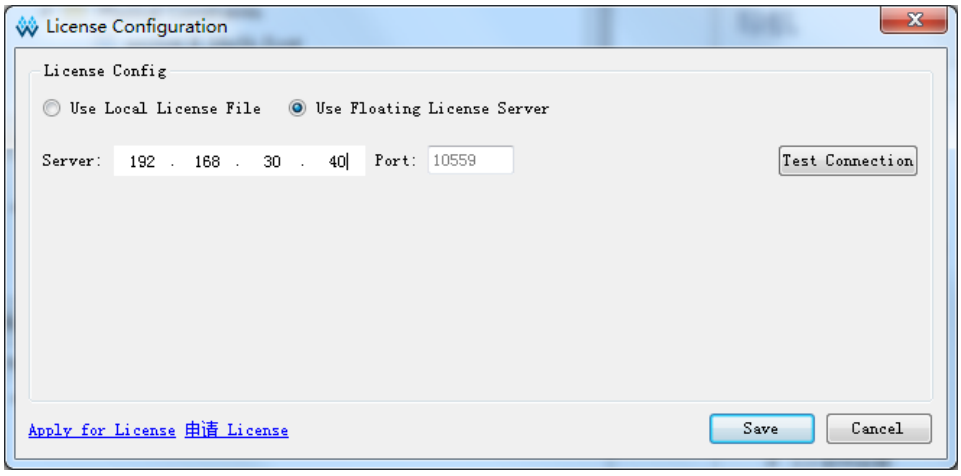
Copy the floating license file (gowin_license.lic, for example) to "GowinLicenseServerForWindows\PnrLicenseServer". In the cmd window, execute the gwlic_server.exe -l gowin_license.lic command in the directory of gwlic_server.exe. Figure 3-10 shows the view after the server has started.

Figure 3-10 Gowin Floating License Server Start Interface



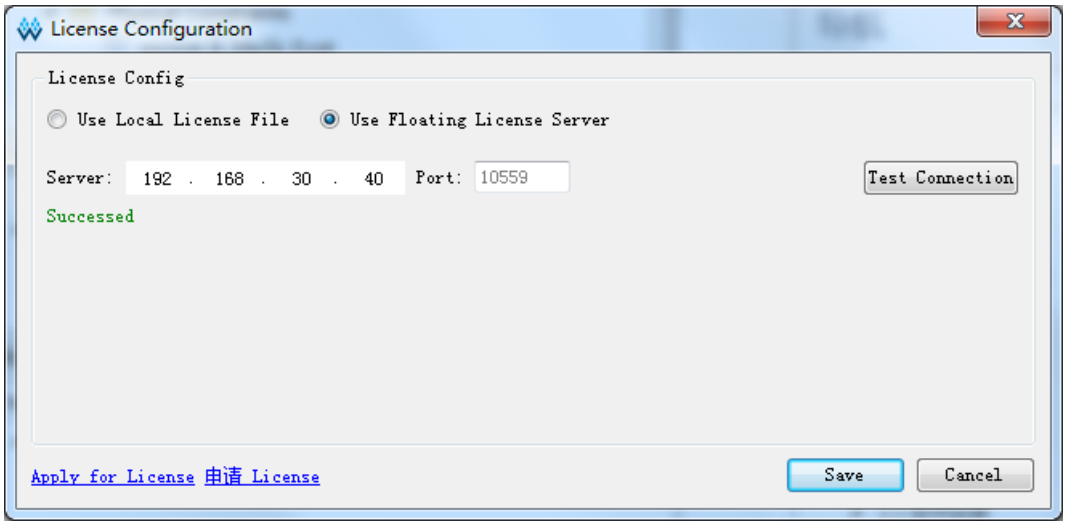
3. After successfully starting the server, input the server IP address in the "License Configuration" view, as shown in Figure 3-11.

Figure 3-11 Floating License Configuration Interface



4. Click the "License Configuration" button on the right to test whether the connection has been successful. If successful, "Successed" will appear in the "License Configuration" view, as shown in Figure 3-12.

Figure 3-12 Connection Test



File Mode

User can select local License file or floating License file and modify the configuration file in the path\IDE\bin of YunYuan software, and write the location of local License file or the IP address of server. For example,

Local License file: [license]lic="D:\Gowin\1.9.2\gowin_license.lic"

Floating License file: [license]lic="192.168.31.97:10559"

3.7 Software License Loading (Linux)

3.7.1 SynplifyPro License loading

In the Linux version of the software, only floating licenses are available for SynplifyPro. Save the license.txt file to the lmgrd path. If it's saved to the other directory, absolute path needs to be used.

Take 64-bit Linux, Ubuntu for an instance, refer to the following steps to configure the license (only the floating license is supported):

1. Obtain SCL folder from official website.
2. Confirm and modify the license file:
   a) Modify PC name and confirm MAC address.
   In the floating license file, modify "hostname1" in "SERVER hostname1 000C293B1A2B 27020" to the PC name. "000C293B1A2B" is "HWaddr", and "27020" is the port number. Modify the license according to the PC on which SynplifyPro is installed, such as: "SERVER gaoyun 000C293B1A2B 27020".
   b) Modify snpslmd path.
   On the basis of the "SCL\linux64\bin\snpslmd" path in SCL, modify this line "VENDOR snpslmd /path/to/snpslmd" in the license file to the local snpslmd path; for example: "VENDOR snpslmd path/scl_lic_server_linux/v2018.06/linux64/bin/snpslmd".
3. Configure the License using SCL
   In the lmgrd path (SCL\linux64\bin\lmgard), execute the "./lmgrd -c license.txt -l lic.log" command to generate the log file "lic.log". View the lic.log to verify whether the configuration has been successful. If yes,

the file content as shown in Figure 3-3 will appear in the log file.

4. Configure the Environment Variable:
   a) Configure the "LM_LICENSE_FILE" environment variable. Open /etc/profile file and type environment variable in this file. The value format should be "Port number @ Host name", for example: export LM_LICENSE_FILE=27020@gaoyun. Exit and save the modified file and restart the computer to make the environment variable effective.
   b) The default port number is 27020 during License installation. It can be modified by finding the character string "27020" in the license file and replacing this string with the designated port.

Note!

All the commands should be executed in the path of the license installation directory. Furhter license commands are as follows:

- Configure license——"./lmgrd –c licensefile –l lic.log"；
- Stop license——"./lmdown -c licensefile"；
- Check license status——"./lmstat -a -c port number@ host name".

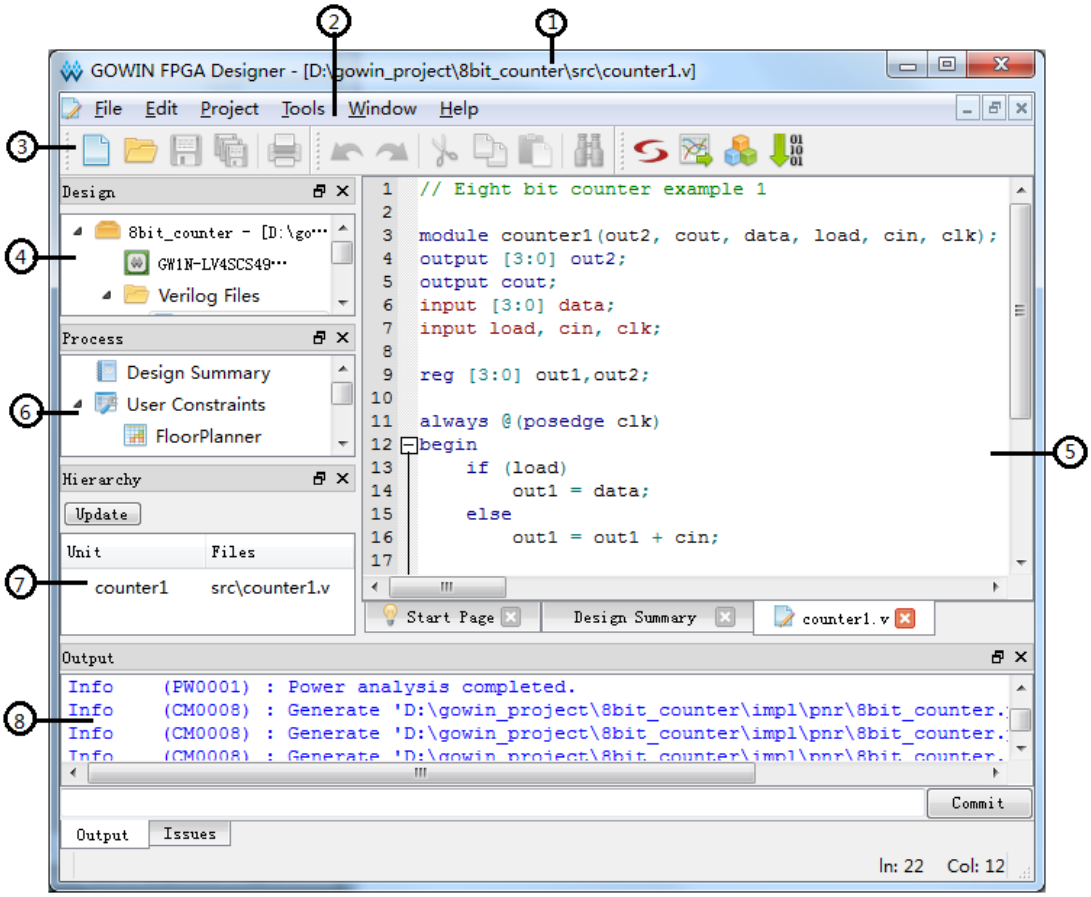
3.7.2 Place and Route License Loading

In Linux, the Gowin License configuration is different to that of Windows, please refer to 3.6 Place and Route License Configuration.

4 Yun Yuan Software User Interface

Figure 4-1 shows the YunYuan software GUI. It consists of the title bar, menu bar, tool bar, project area (Design View), process area (Process View), source file editing area, and information output area (Output).

Figure 4-1 Software User Interface



① Title Bar
② Menu
③ Tool Bar
④ Project Area
⑤ Source File Editing Area
⑥ Process Area
⑦ Design Hierarchy Area
⑧ Information Output Area

4.1 Title Bar

Title bar shows the current project path, name, and the name of the file that is currently open.

4.2 Menu

The menu bar contains links to the tools and functionality that are commonly used in projects, including the File, Edit, Project, Tools, Window, and Help options. See the following for details:

File

- New: Create a new file and project;
- Open: Open a new file and project;
- Save: "Save" the project files;
- Save As…: "Save as" the project files;
- Save All: Save all the project files;
- Close: Close projects or the project file and page;
- Close All: Close all project files and pages;
- Close Project: Close the current project;
- Print Preview;
- Recent Files: Show the files that were recently open. The user can click on the names of these files to reopen them;
- Recent Projects: Show the names of the projects that were recently open. The user can click on the names of these projects to reopen them;
- Exit: Exit and close the Gowin YunYuan software.

Edit

- Undo;
- Redo;
- Cut;
- Copy;
- Paste;
- Select All;
- Find: Find or substitute key words;
- Toggle Comment Selection: Add comments to the selection;
- Macros;

Project

- Archive Project;
- Restore Archive Project;
- Set Device: Set device of current project;
- Configuration: Open configuration interface;
- Design Summary: Show detailed information of current project.

Tools

- Start Page;
- Synplify Pro: Front-end integration software;
- Gowin Analyzer Oscilloscope;
- IP Core Generator;

- Programmer: FPGA programmer;
- FloorPlanner: Physical constraints editor;
- Timing Constraints Editor;
- Options: Used to open the required tools or set IDE parameters.

  Note!

  For the Synplify Pro options in "Options" view, if "Custom" is selected, the local defined Synplify Pro will be used whether the software will be updated or not; if "Default" is selected, the SynplifyPro in the current software path will be used.

Window

- Full Screen: Full screen display;
- Tile: Tile display;
- Cascade: Cascade display;
- Reset Layout: Restore initial settings;
- Panels: Select whether to display GUI models or not;
- Start Page: Start page display in the source file edit area;
- Design Summary: Design page display in the source file edit area;

Help

- View Help: View help docments;
- Contact Us;
- Manage License;
- About: Show software version and copyright information.

4.3 Tool Bar

The Tool bar contains quick access buttons. These are as follows (from left to right): New File or Project, Open File or Project, Save, Save All, Print, Undo, Redo, Cut, Copy, Paste, Find, Synplify Pro, Gowin Analyzer Oscilloscope, IP Core Generator and Programmer.

4.4 Project Area (Design)

The project area shows projects and the related files. Users can check or change the project device information, user design files, user constraints files, configuration files, etc.

4.5 Process Area (Process)

The process area provides FPGA design flow, including synthesis, place & route, and download bitstream files (program device). Users can also double click timing constraints editor and physical constraints editor to edit the constraints files.

4.6 Design Hierarchy Area (Hierarchy)

After loading the design files, IDE will parse the design files first. The hierarchy window shows the hierarchy of current project. The Unit column shows module hierarchy of the design files. The Files column shows the file where the module definition is.

If there is an error in hierarchy parse of the project file, the optinal "Hierarchy panel error" marked in red will be displayed at the top right of

the hierarchy window as shown in Figure 4-2. Click "Hierarchy panel error" and Hierarchy Panel Error window will pop up as show in Figure 4-3.

Figure 4-2 Hierarchy panel error Prompt

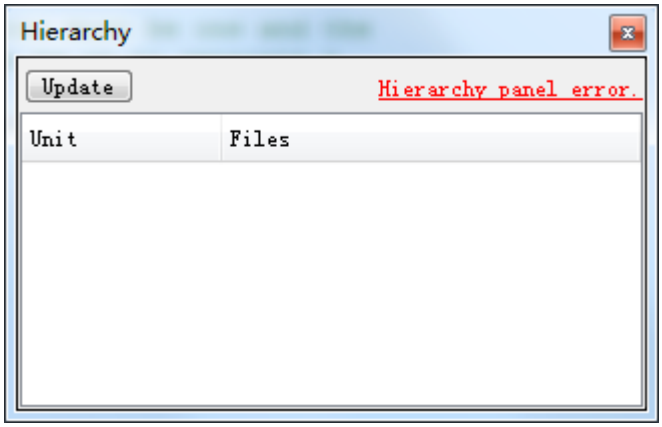
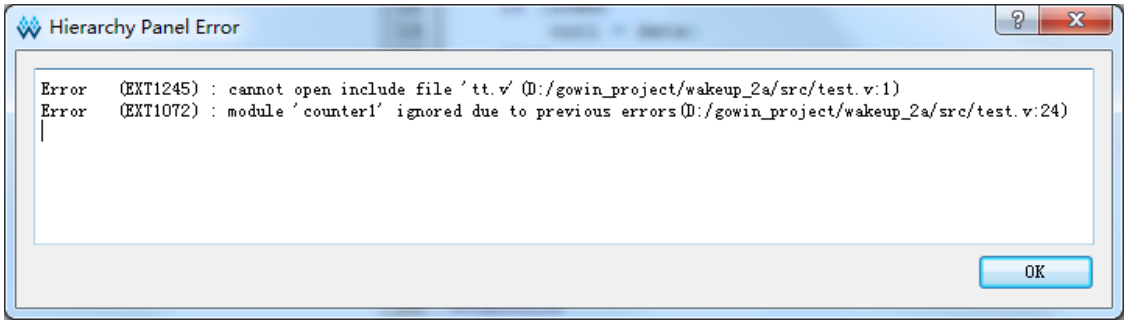


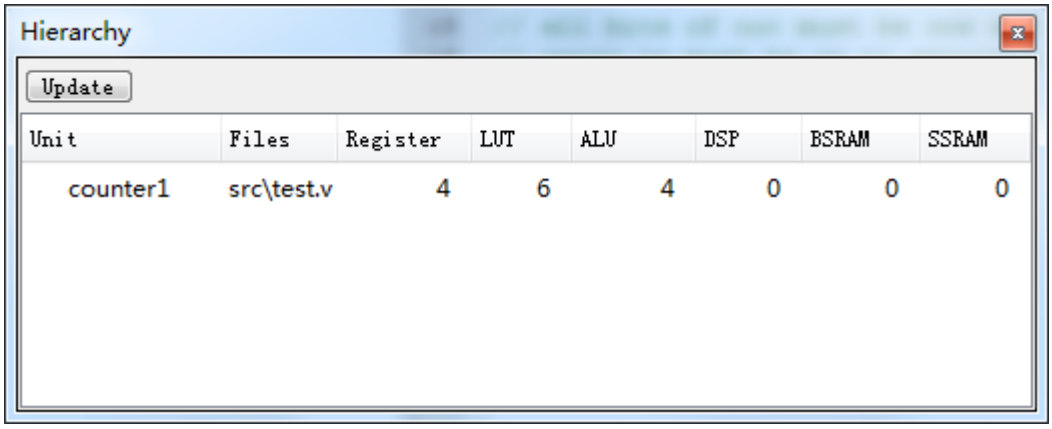
Figure 4-3 Hierarchy Panel Error View



It can locate the module definition and instantiation in the design file by "Goto Module Instantiation" and "Goto Module Definition" in the right-click menu. In the hierarchy window, every module supports "Set As Top Module" by right-clicking. The module set as the top will be marked "  " to indicate that the current module is the top module, and the original hierarchy remains unchanged.

The Hierarchy window will automatically display the resource information of the current project after synthesis if selecting Gowin Synthesis, as shown in Figure 4-4. If selecting Synplify Pro, the Hierarchy window will not display the resource information.

Figure 4-4 Resource Information in Hierarchy View



Note!

The hierarchy window does not support parsing VHDL files at present. If loading VHDL files, it is normal that Hierarchy panel error will display in IDE.

4.7 Source File Editing Area

Users can view and edit source files in the source file editing area.

The source file editing area shows different files, including new files or opened files, the generated files after synthesis or Place & Route, the "Start Page" and "Design Summary".

If the file currently displayed is modified, the term "File Changed" will appear in the file editing area, as shown in Figure 4-5. Select "Reload" to reload the file.

Figure 4-5 File Changed

To close the file currently displayed, click "File > Close", or click on the icon " " that appears in the upper-right of the file editing area.

To close all the files in the file editing area, click "File > Close All".

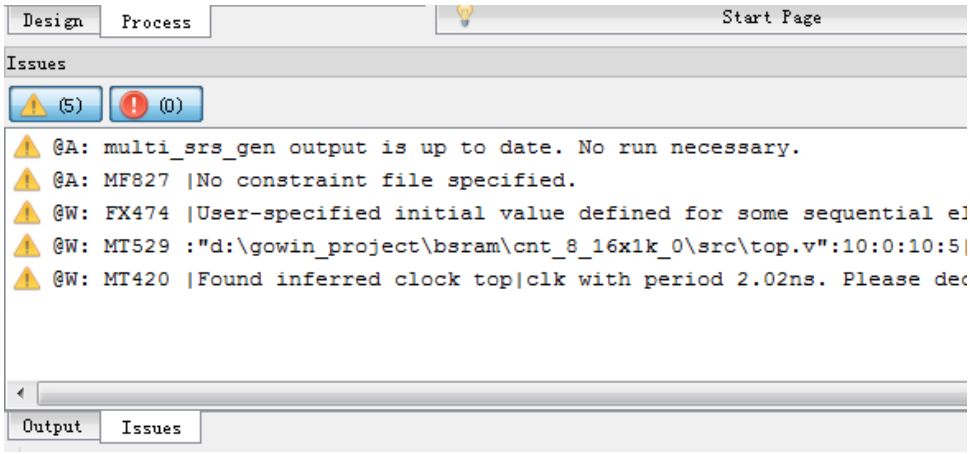
4.8 Information Output area

The information output area displays the processing information when the software is running. Users can verify different outputs by manually switching between the tabs:

- Output: All information
- Issues: Issues information

In the output tab, right-click and select "Clear" to clear all the information in the tab. "Issues" includes two sub-options of "Warning" and "Error". Users can configure the "Issues" page to display warnings only or errors only. The number of Warnings and Errors will be recorded and shown on each of the corresponding tabs, as shown in Figure 4-6. Right-click and select "Clear" on "Issues" page to clear the current page information.

Figure 4-6 Information Output View



After selecting certain Error or Warning message reported by PnR, right-click and select "Help" or press the shortcut key "F1", the "GOWIN Help" of this error or warning will pop up, and the help information of this error or message will be described in details in the document.

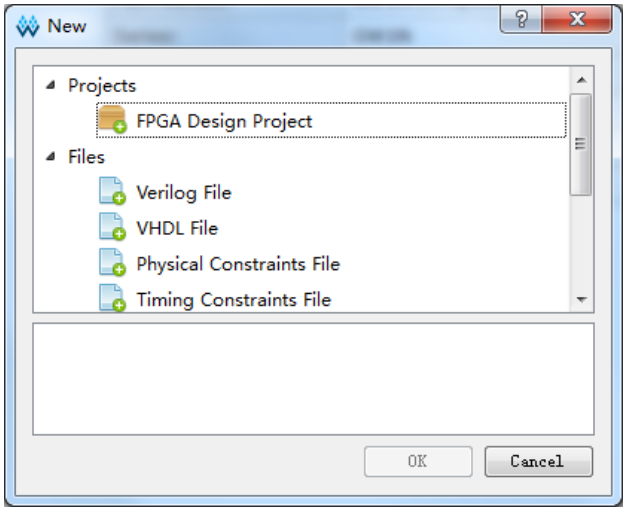
5 Operation

Gowin YunYuan is available in Windows and Linux. It supports GUI running mode and commands running mode. Take the GUI running mode in Windows for instance. Please refer to the following for the operation details.

5.1 Create a New Project

1. From the File menu, choose "File> New…" to open the "New"dialog, as shown in Figure 5-1.

Figure 5-1 Create a New Project



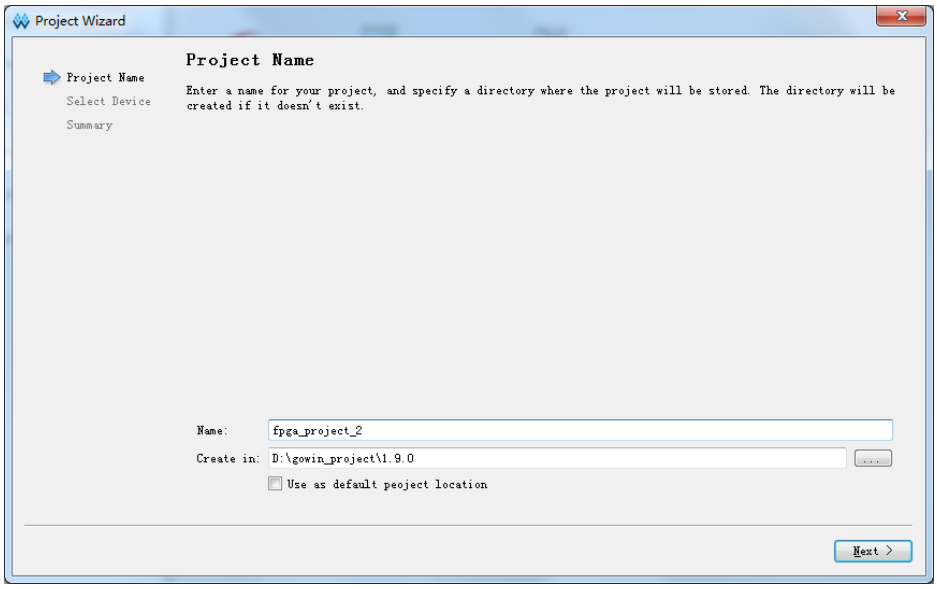
Note!

There are different ways to open a "New" dialog:

- Using the "Ctrl+N" short cut;
- Clicking on the "New File or Project" icon in the toolbar;
- By selecting "Quick Start>New Project" on the Start Page.

2. Select "FPGA Design Project", and then click "OK" to open "Project Wizard", as shown in Figure 5-2.

Figure 5-2 Create a New Project Wizard

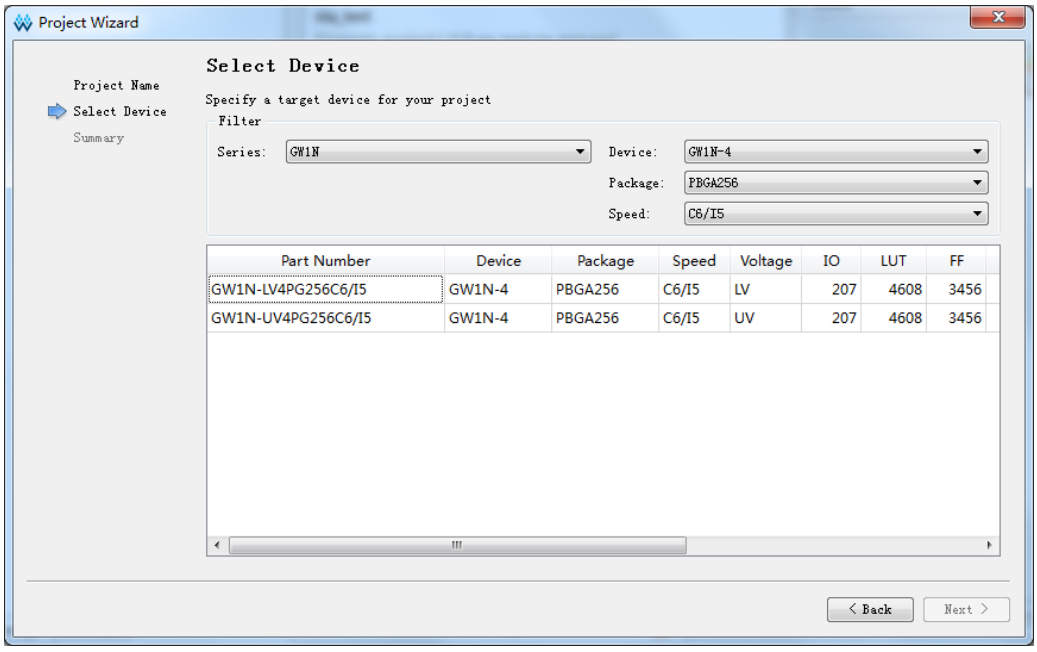


3. Create the project "Name" and "Create in", as shown in Figure 5-2;
   - Enter the project name in the "Name" field;
   - Click on the "..." icon to choose the project path.

   Note!

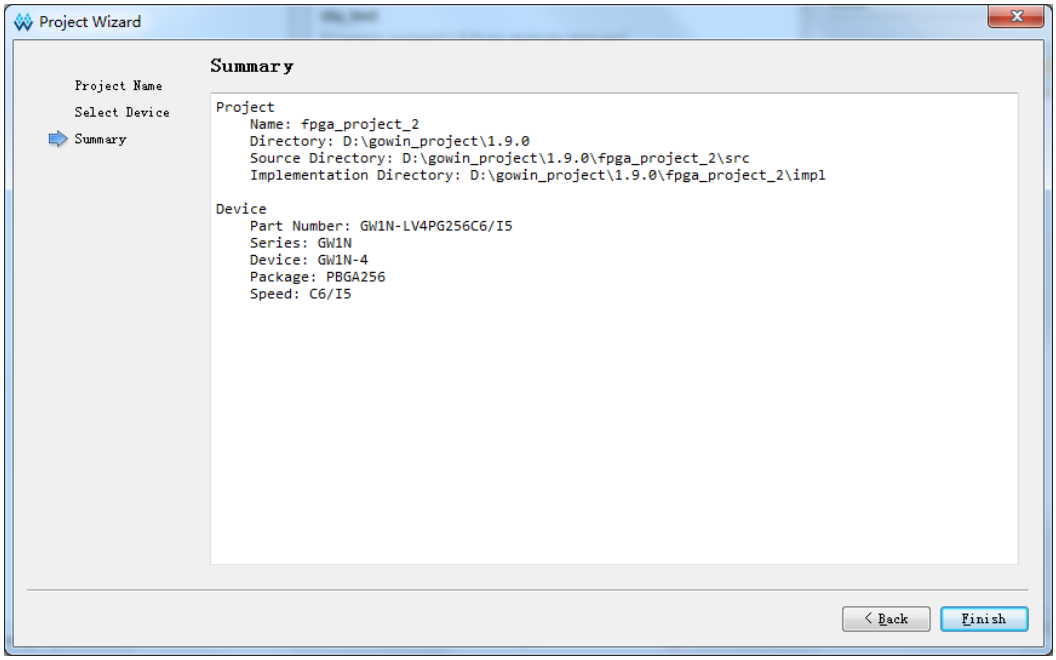
   - No Chinese characters or spaces can be included in the project path.
   - The file path length is limited in both Windows and Linux. You cannot delete or copy the files with the length going over the limits;
   - The path separator is "\" in Windows; for example, E:\Gowin\ide;
   - If users select "Use as default project location", the project location will be set as the default location, and all later projects you create will be saved to this location.
4. Click "Next" to select the device, as shown in Figure 5-3 Select Device:
   - In this step, users can select the target device series, package, and speed.
   - Choose package type from the "Package" drop-down list;
   - Choose speed grade from the "Speed" drop-down list;
   - Choose the detailed part number from the "Part Number" sub-window. It displays the detailed resource information related to the selected device.

Figure 5-3 Select Device



5. Click "Next" to open the Project Information Summary window, as shown in Figure 5-4.

Figure 5-4 Project Information Summary



6. Click "Finish". The project now is created.

Note!

- The device can be changed after the project has been created. Please refer to 5.3Edit a Project>05.3.1 Modify Project Device for further details.
- Users can add source files and constraints files after the project has been created. Please refer to 5.3Edit a Project > 5.3.2 Edit a Project File for the details.

5.2 Open an Existing Project

Use one of the following four methods to open an existing project:

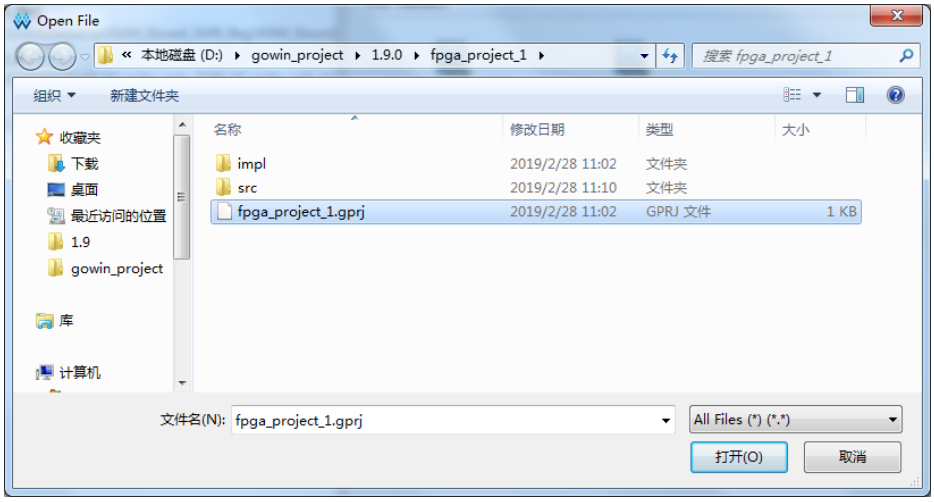
Method 1

1. From the File menu, select "File> Open …" to open the "Open File" dialog box, as shown in Figure 5-5.

Note!

Users can also click on the " " icon in the tool bar to open the "Open File" dialog box.

Figure 5-5 Open an Existing Project



2. Choose the project file (*.gprj) and click "Open" to open the existing project.

Method 2

1. On the start page, click " " to open "Open Project" dialog box,
2. Click "Open" to open the project.

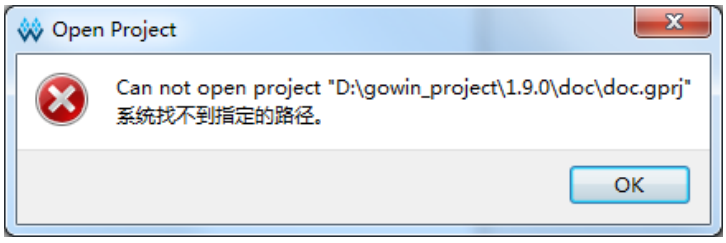
Method 3

From the File menu, click "File> Recent Projects", to open your required project.

Note!

- Users can also open recent projects from the projects list that is displayed on the left side of the start page.
- Recent Projects shows the recently opened projects. Users can click on the names of the files to re-open them;
- If the project was deleted, the "Open Project" dialog box will appear, as shown in Figure 5-6.

Figure 5-6 Project Deleted Prompt Box



Method 4

Find the project you established and find the *.gprj file. Doule-click on *.gprj file to open the project with Gowin YunYuan software automatically.

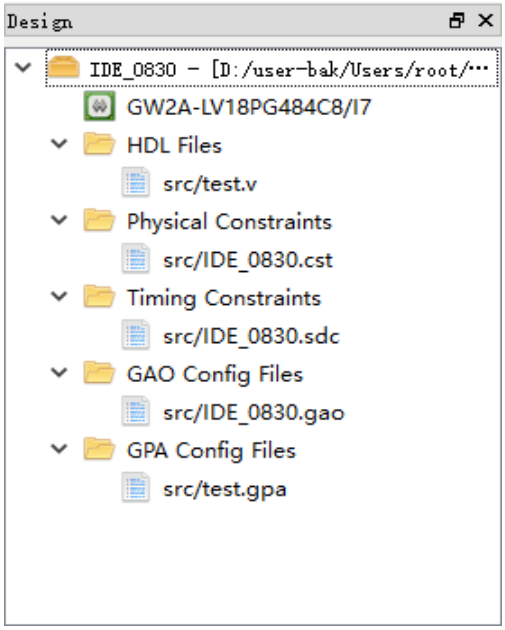
5.3 Edit a Project

After creating or opening a project, users can edit the device information and the related files in the project design area, as shown in Figure 5-7.

The Project Design Area contains the following:

- The project path;
- Chip info: Chip type, package type, and speed;
- The current project files, including user design files, physical constraints files (.cst.), timing constraints files (.sdc), GAO config files (.gao), and GPA config files (.gpa), etc.

Figure 5-7 Project Design Area



5.3.1 Modify Project Device

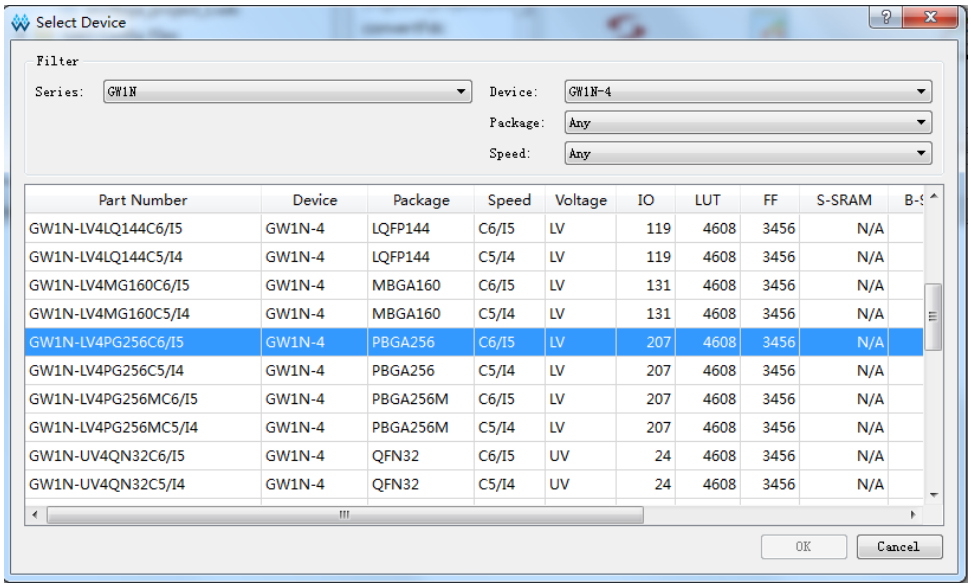
The second line in the project design area shows the device info. for the current project. Refer to the steps as below to modify the current project device.

1. As shown in Figure 5-7, double-click "GW1N-LV4PG256C6/I5" to open the "Select Device" view, as shown in Figure 5-8;
2. In the "Select Device"view, select "Series" and "Device", select "Package" from the package drop-down list and select "Speed" from the speed drop-down list, and then select the detailed part number from the "Part Number" sub-window. Click "OK".

   Note!

   The "Part Number" sub-window displays the detailed resource information related to the selected device.

Figure 5-8 Project Device Infromation



5.3.2 Edit a Project File

Files that need to be added in projects include design files (Source Files), constraints files, and configuration files. Constraints files contain the Physical Constraints File and Timing Constraints File; configuration files contain the GAO Config File and GPA Config File.

A project can have multiple design files; however, only one physical constraints file and one timing constraints file can be active at a time.

Refer to the following sections to edit the project files.

1. Create a New Project File

   a) As shown in Figure 5-9, right-click on a blank area of the project design area, select "New File…" to open the "New" dialog box, as shown in Figure 5-10;

   b) As shown in Figure 5-10, select the file type and click "OK" to create a new file.

Figure 5-9 Right-click Menu

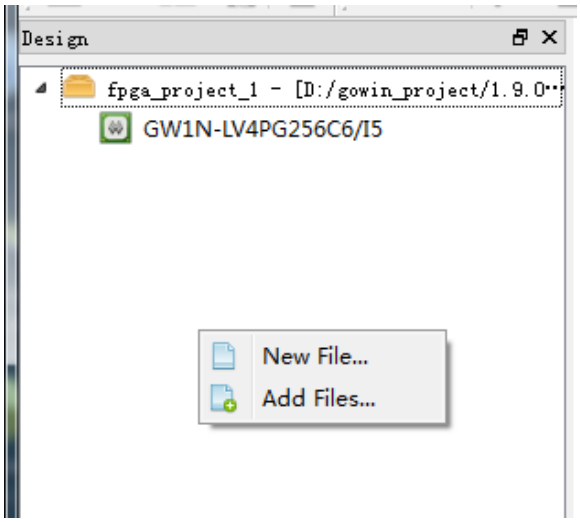
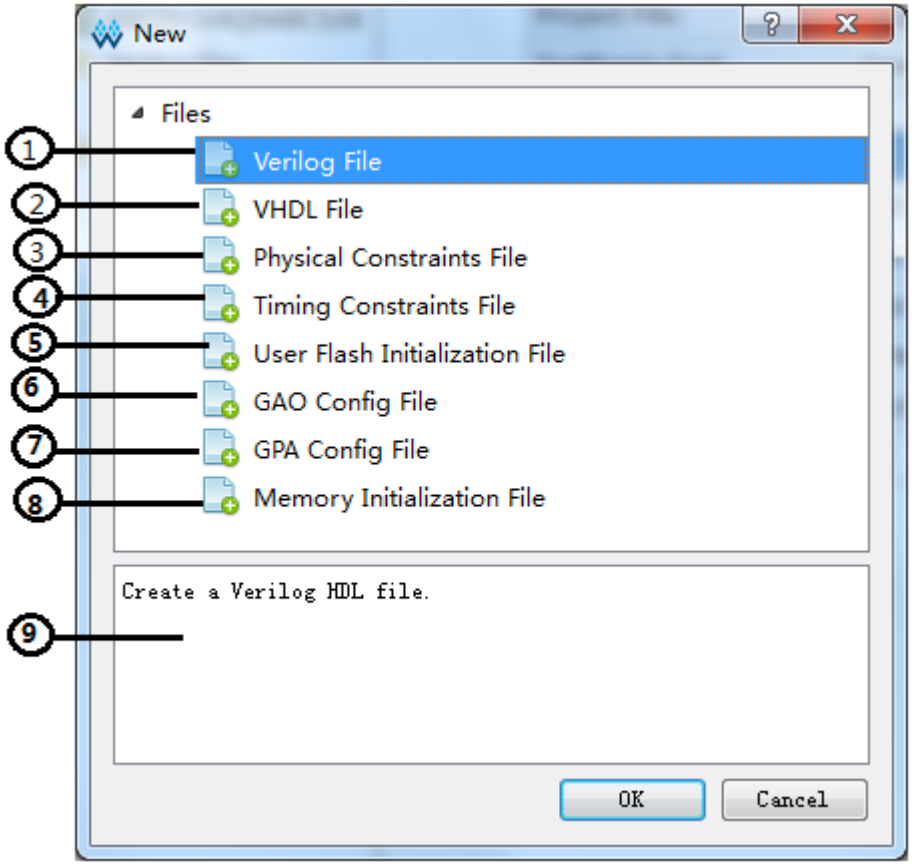


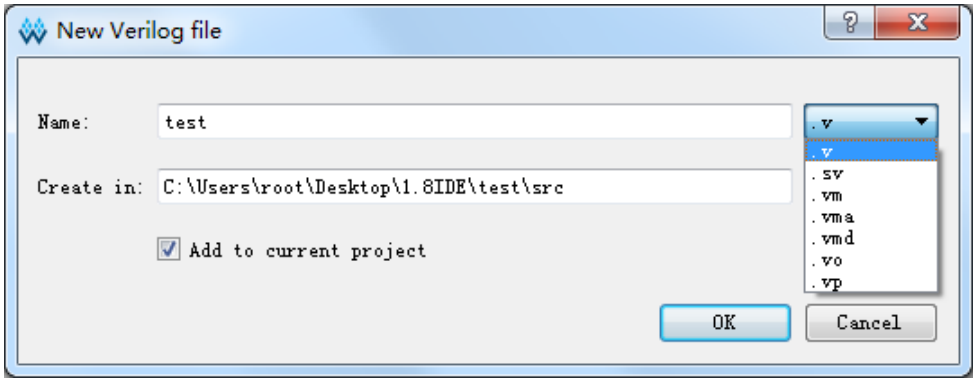
Figure 5-10 Create a New File



① Verilog File
② VHDL File
③ Physical Constraints File
④ Timing Constraints File
⑤ User Flash Initialization File
⑥ GAO Config File
⑦ GPA Config File
⑧ Memory Initialization File
⑨ File Description

c) Take creating a Verilog File, for instance. Select "Verilog File" and click "OK" to open the Verilog File view, as shown in Figure 5-11.

Figure 5-11 Create a Verilog File



d) Enter the file name and click "OK".

Note!

- Users can select file extensions from the drop-down list. "Add to current project"

is selected by default.

- User can open and edit the newly created blank file in the source file editing area.

2. Create a Configuration File

a) As shown in Figure 5-9, right-click on a blank area of the project design area, select "New File…" to open the "New" dialog box, as shown in Figure 5-10;
b) As shown in Figure 5-10, select the file type and click "OK" to create a new file. Take creating a GPA Config File, for instance. Select "GPA Config File" and click "OK" to open the GPA Config File view, as shown in Figure Figure 5-12.
c) The newly created Config File will not be directly opened in the source file editing area directly. Users need to double-click the Config File in the project Design area to open and edit the blank Config File, as shown in Figure 5-13.

Figure 5-12 Create a Config File

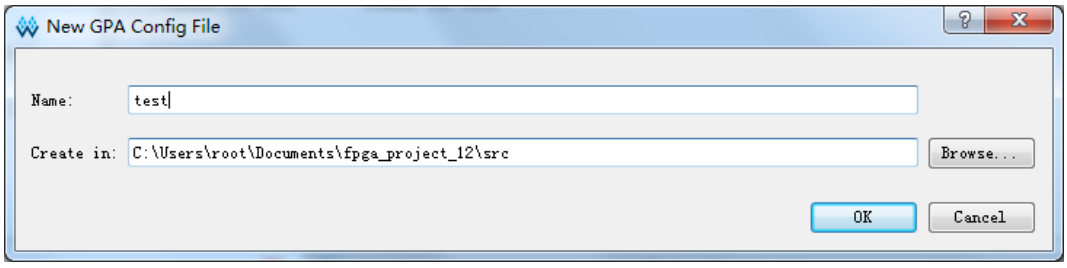
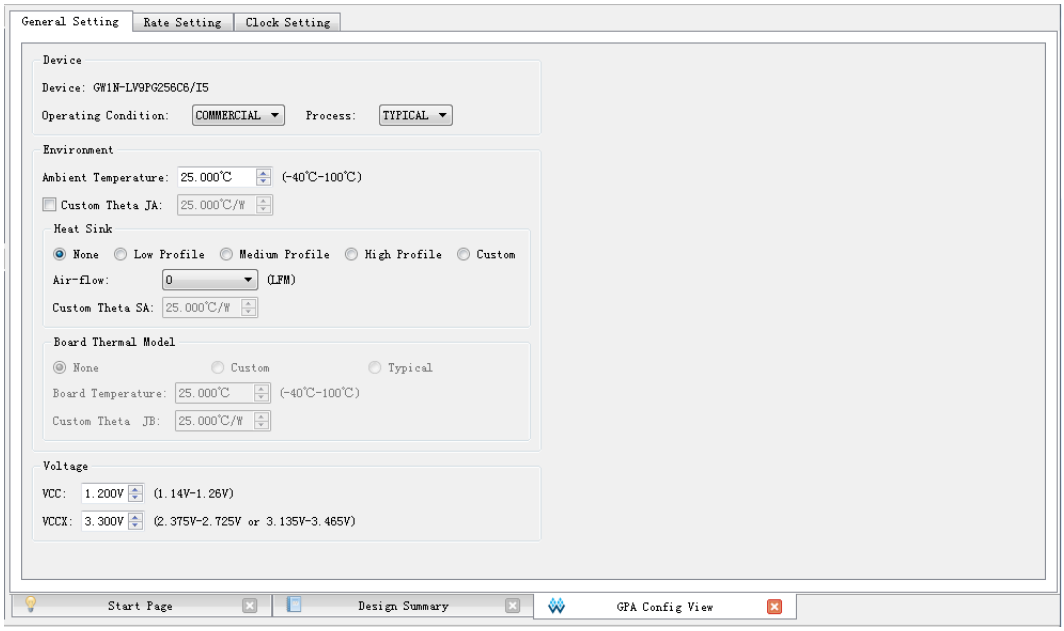


Figure 5-13 GPA Config File



Note!

- If the newly added Verilog File has the same name as an existing file, the same name prompt will appear, as shown in Figure 5-14;
- If the newly added Constraint files already exist, a warning message will be displayed, as shown in Figure 5-15.
- If the newly added Config files already exist, a warning message will be displayed, as per Figure 5-16.

Figure 5-14 Same Name Prompt

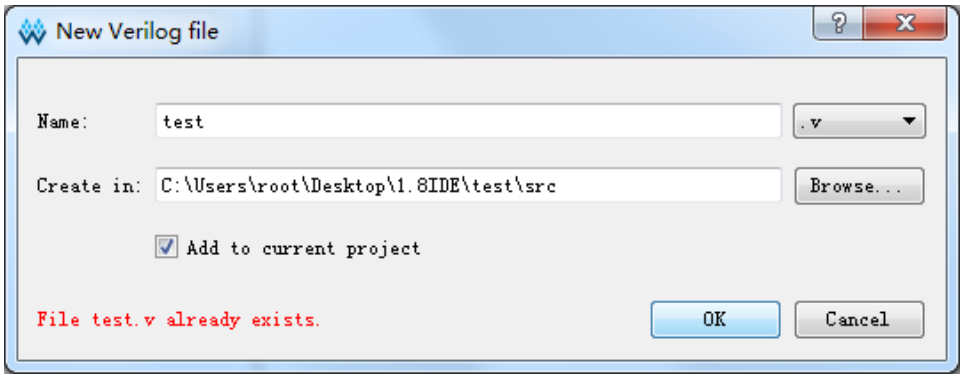


Figure 5-15 Constraints Files Existence

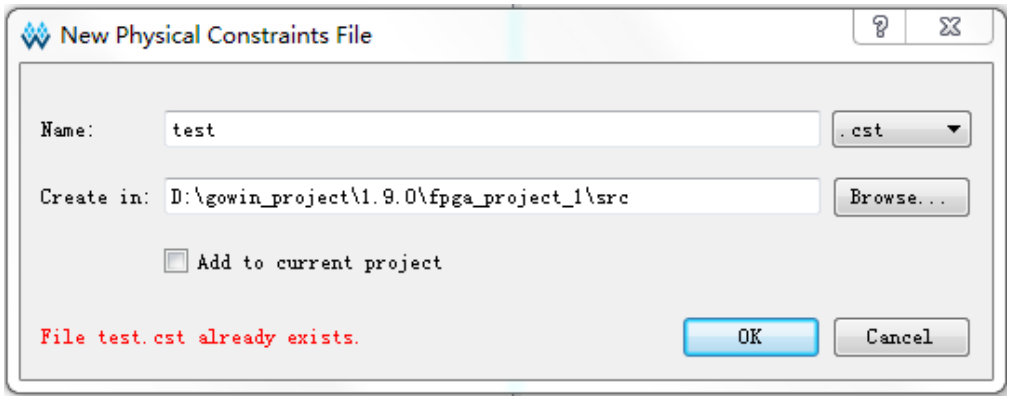
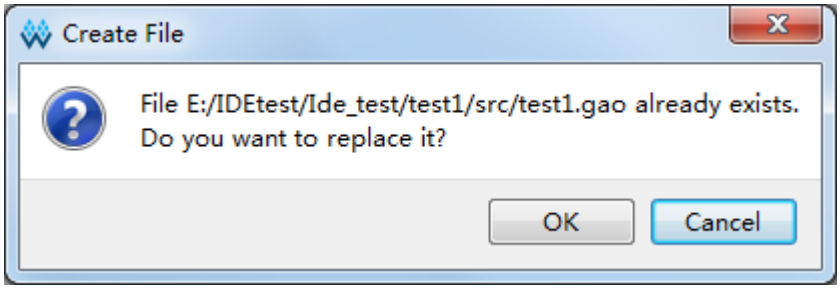


Figure 5-16 Config Files Existence



3. Add Project Files

   a) As shown in Figure 5-17, right-click in the blank of the project design area, select "Add Files…" to open the "Select Files" dialog box;

   b) Select single or multiple project files to add.

   Note!

   - If the added files are not the project files, Figure 5-18 will pop up to confirm whether the user needs to copy them into the project source directory.
   - If the users add RTL files and constraints files at the same time, YunYuan will automatically classify the files in the project design area;
   - If the added files are neither RTL design files nor constraint files, GPA, GAO configuration files, "Other Files" will be added in the project design area.

Figure 5-17 Right-click Actions in Design View

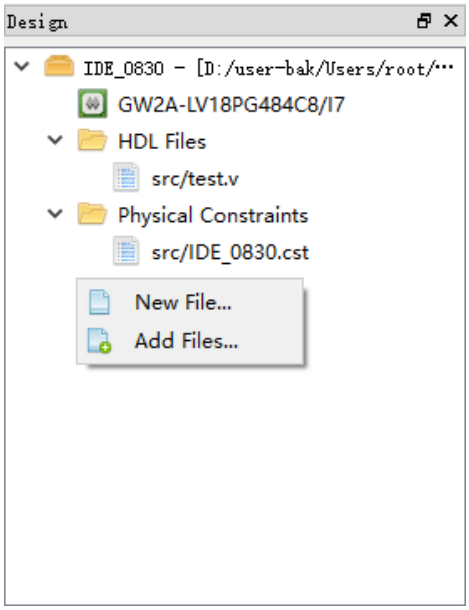
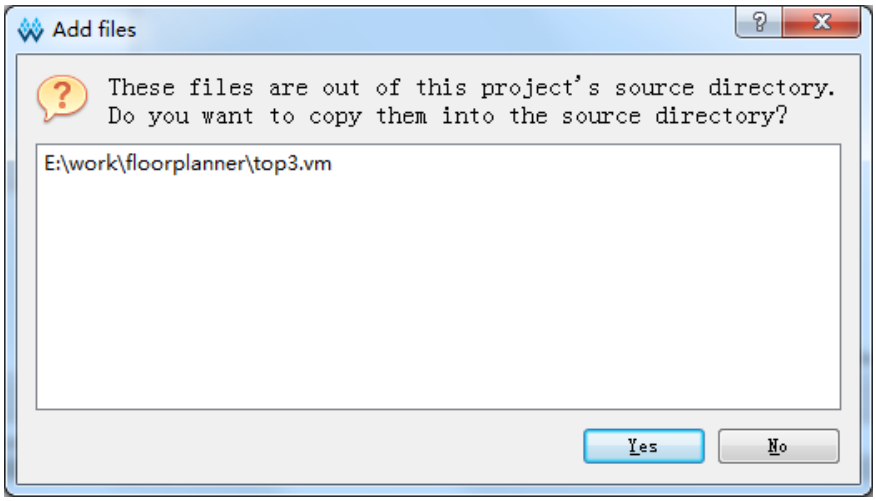


Figure 5-18 Copy File

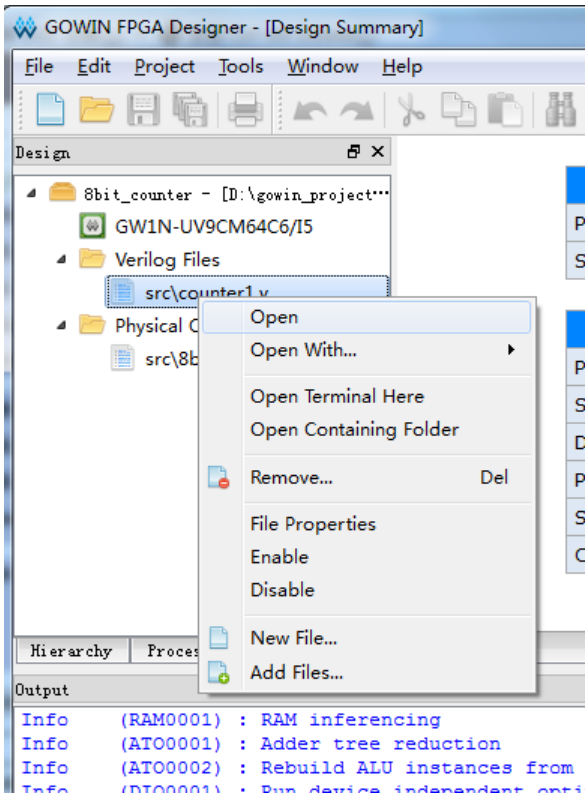


4. Modify Project Files

Use the following two methods to open and modify the project files, as shown in Figure 5-19:

a) Double-click any file in the project design area; the file will open in the source file editing area;
b) Right-click on the name of the file that is to be modified and select "Open".

Figure 5-19 Project Files Editing Actions



Note!

- Users can also select "Open With>Add External Editor" to add an external editor, as shown in Figure 5-20. Users can add external editors according to their needs.
- Select "Open Containing Folder" to open the file folder;
- Select "Open Terminal Here" to open the command line window. Command liine mode can be used;
- If users modify and save a file that has been opened in YunYuan software, the Gowin YunYuan software wiill generate a change notice, as shown in Figure 5-21.
- If users modify and close unsaved files, they will be prompted to save the change as shown in Figure 5-22.

Figure 5-20 External Editor

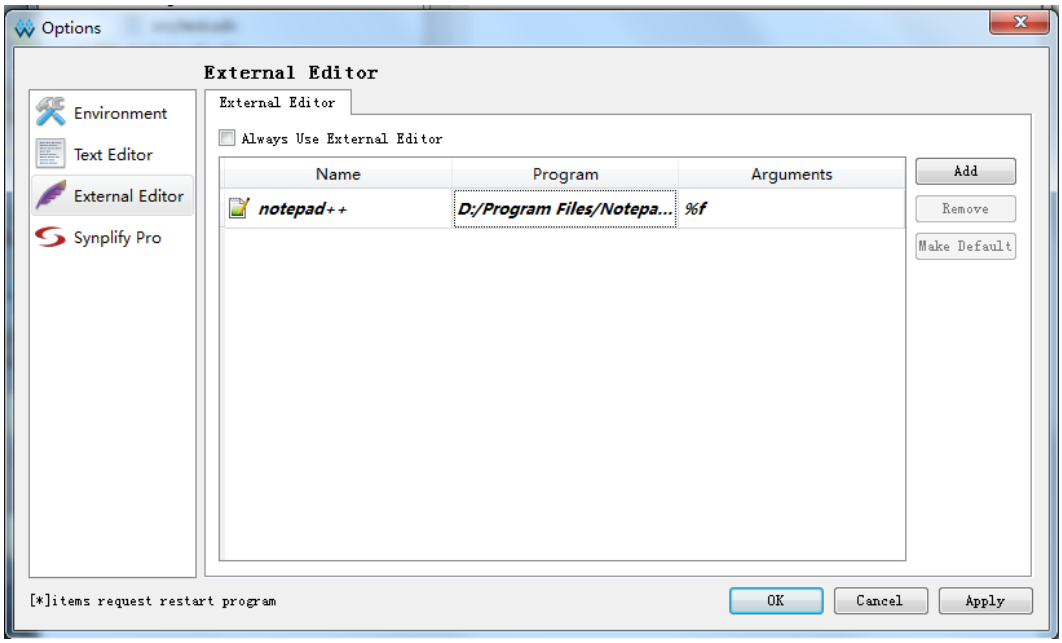
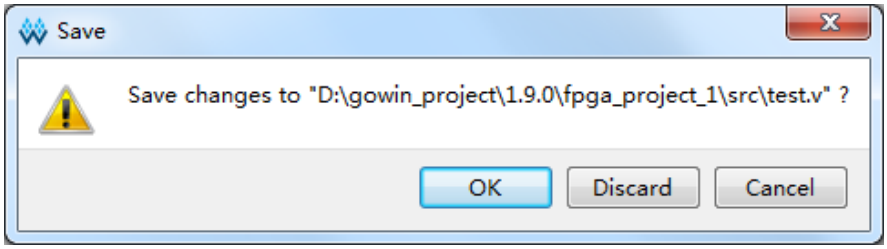


Figure 5-21 Project File Change

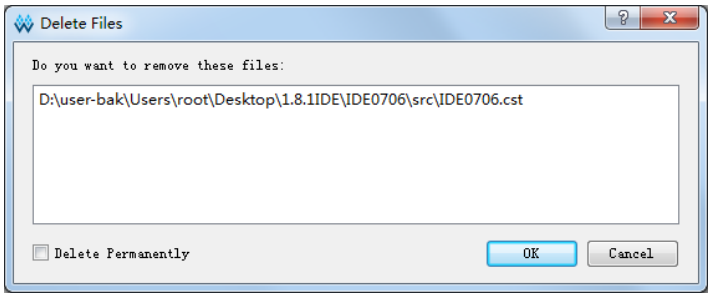
Figure 5-22 Project File Save



5. Delete Project Files

   a) Select the file in the project design area;
   b) Right-click and select "Remove" or press "Delete" on the keyboard. The "Delete File" dialog box will be displayed, as shown in Figure 5-23. If the user selects "Delete Permanently", the file will be deleted from the current project and the disk. If "Delete Permanently" is not selected, the file will only be deleted from the current project.

Figure 5-23 File Delete Confirm



Note!

If the file that is open in the editing area is deleted, the delete file notice will pop up, as shown in Figure 5-24.

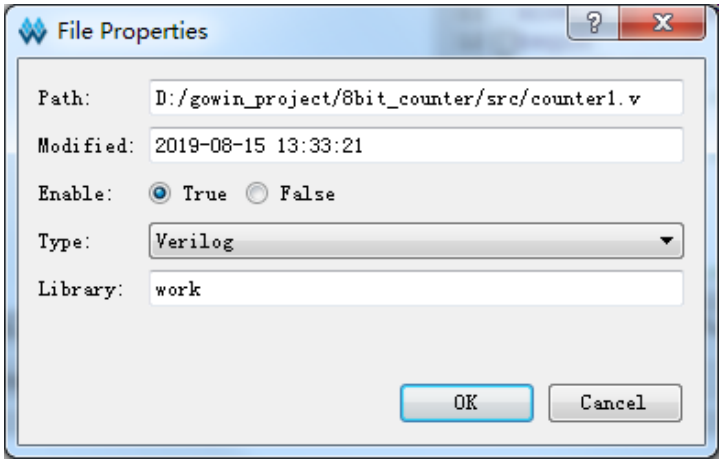
Figure 5-24 File Delete Notice

6. View File Properties

Rigut-click any file in the project management and select File Properties from the right menu list, as shown in Figure 5-25. The path, modified time, Enable, Type, and Library information are displayed in the dialogue.

The file type can be modified in the Type drop-down menu. After clicking OK, the file will automatically move to the selected type in the Design window

Figure 5-25 File Properties



7. Enable/Disable Function of Project Files

Users can see the "Enable" and "Disable" options by righting click on any files in the project design area, as shown in Figure 5-19. After setting Enable / Disable, Synthesize and Place & Route can read the enable file.

a) Set Enable / Disable by right-clicking actions, including single file setting and setting of batch files;
b) If multiple design files (hdl files) are selected, "Enable" and "Disable" are all enabled;

c) If multiple constraints files or configuration files are selected, "Enable" is disabled, and "Disable" is enabled, as shown in Figure 5-26.

d) For multiple constraints files or configuration files, only one file can be in "Enable" state. When you create or add a new file of same type, the previous one will be disabled; when multiple files with different types are selected, both "Enable" and "Disable" are disabled, as shown in Figure 5-27.

Figure 5-26 Right-clicking Actions of Selecting Same Type Files

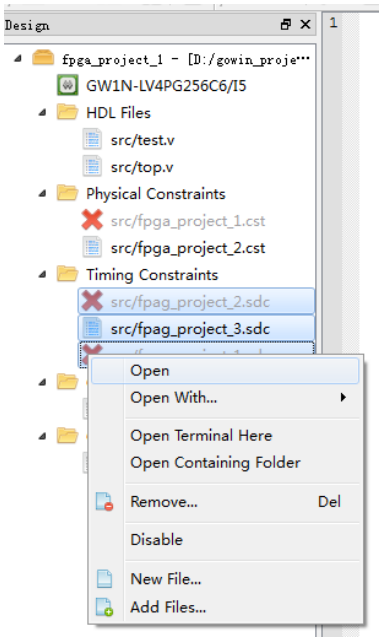
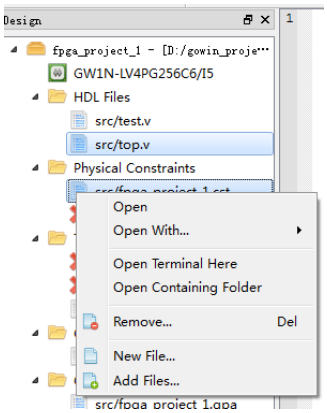


Figure 5-27 Right-clicking Actions of Selecting Different Type Files

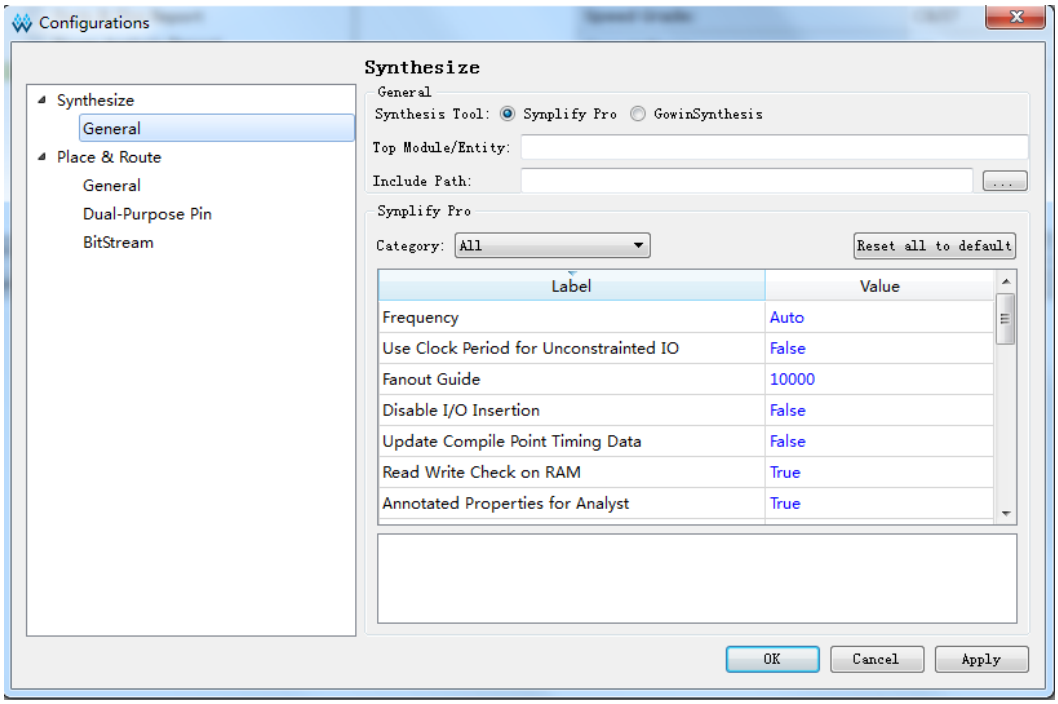


5.3.3 Modify Project Configuration

Right-click on "Synthesize" or "Place & Route" in the Project Design area;

Select "Configuration" to open the project configuration view, as shown in Figure 5-28.

Figure 5-28 Project Configuration View



As shown in Figure 5-28, the project configuration contains the Synthesis configuration and Place & Route configuration. The Place & Route configuration includes General, Dual-Purpose Pin, and BitStream configuration:

- Synthesize: Used to configure the parameters for optimizing user design with Synplify;
- General: Used to configure parameters for placing and routing;
- Dual-Purpose Pin: Used to configure duplicated pins;
- BitStream: Used to configure download speed and enable CRC check, compress, etc.

See the information presented below for further details.

Synthesize

Select Synthesize in project configuration view. In General view, users can select Synthesis Tool: Synplify Pro or GowinSynthesis.

If Synplify Pro is selected as the Synthesis Tool,

- Top Module/Entity and Include Path can be configured;
- Select the parameters options from the "Category" drop-down list. The default value is "All";
- Select the parameter that needs to be configured in "Lable". The corresponding description shows at the bottom of "Configuration" view;
- Double-click the corresponding value and configure based on your requirements. Click "Apply" to put the current configuration into effect. Click "OK" to complete all configuration.

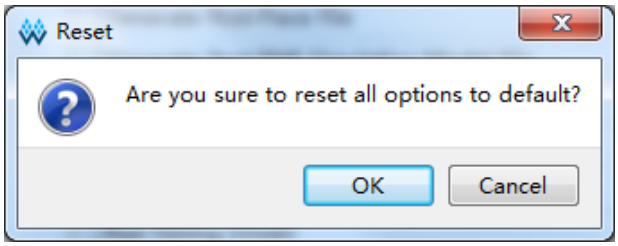
Note!

- For further details about how to configure common parameters, please refer to Appendix A SynplifyPro Attributes and Directives;
- For further details about the configuration methods, please refer to the

SynplifyPro manuals in the YunYuan installation directory: installPatj\SynplifyPro\doc;

- Reset all to default: Reset all configuration on this page to default values; "Reset" will pop up when you click it, as shown in Figure 5-29.

Figure 5-29 Reset

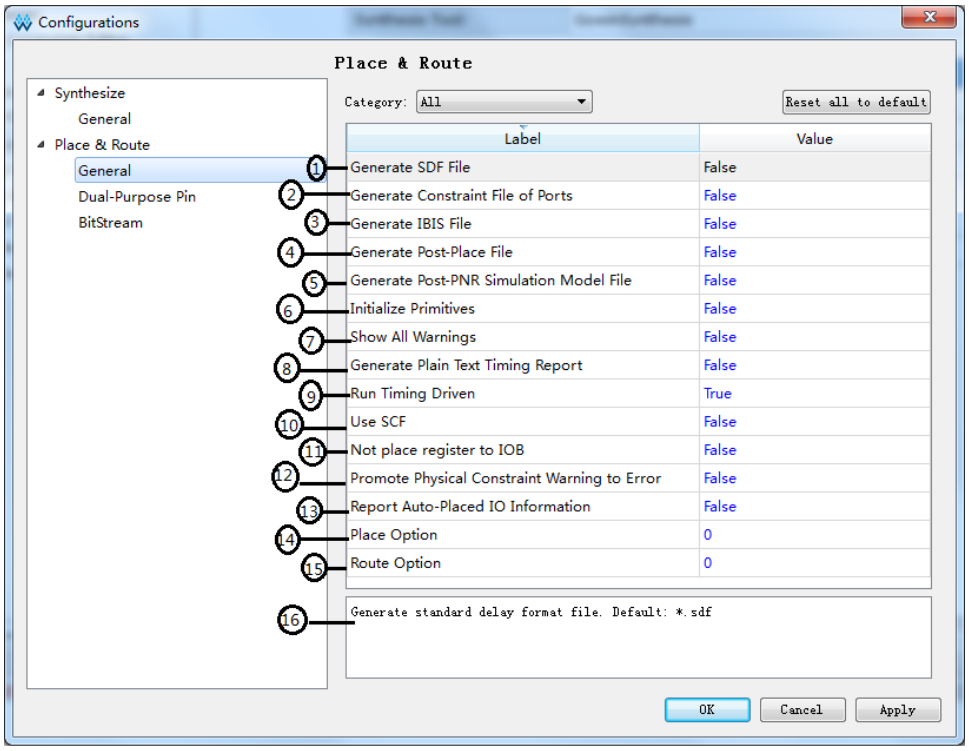


If GowinSynthesis is selected as the Synthesis Tool, Top Module/Entity and Include Path and Verilog Language can be specified. There are three options for Verilog Language: System Verilog 2017, Verilog 2001 and Verilog 95.

Place & Route

"General" configuration in Place & Route, which was independently designed by Gowin, is compatible with Gowin YunYuan software. Users can modify the value configuration, as shown in Figure 5-30.

Figure 5-30 Place&Route Configuration



① Generate SDF file
② Generate Constraints Files of Ports
③ Generate IBIS Files
④ Generate Post-Place file
⑤ Generate Post-PNR Simulation Model file
⑥ Initialize Primitives
⑦ Show all Warnings
⑧ Generate Plain Text

⑨ Run Timing Driven
⑩ Use SCF Timing Report
⑪ Not Place Register to IOB
⑫ Promote Physical Constraint Warning to Error
⑬ Report Auto-Placed IO Information
⑭ Place Option
⑮ Route Option
⑯ Attributive Explanation

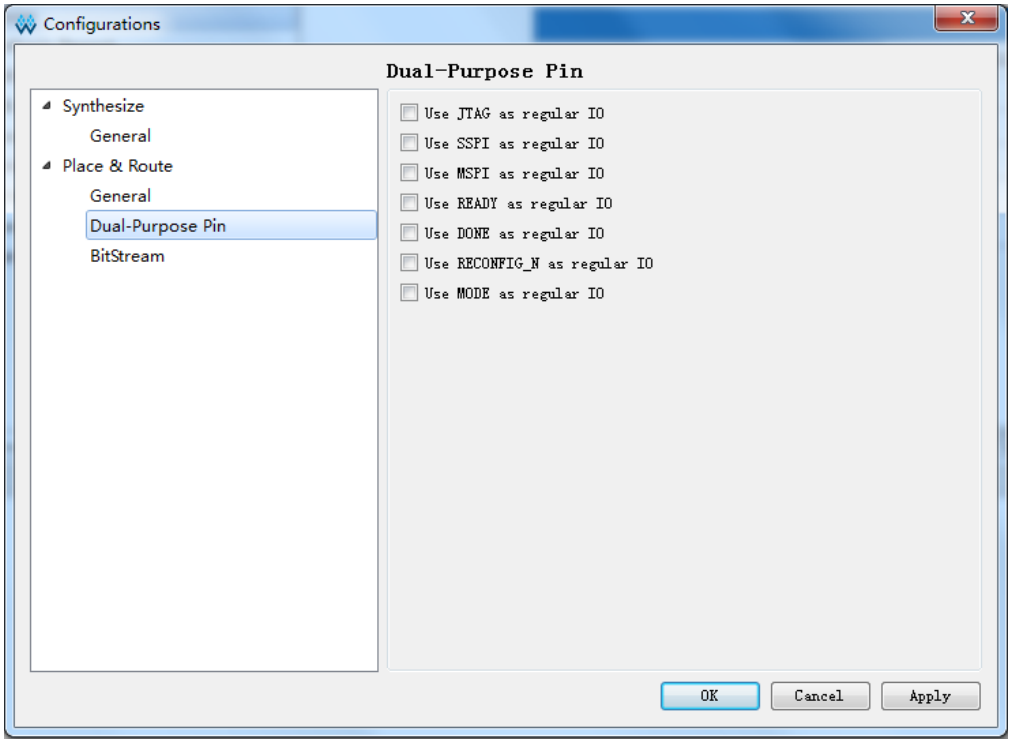
Note!

Reset all to default: Resets all configurations on the page to the default values.

Dual-Purpose Pin

In the Dual-Purpose Pin tab, users can configure the multiplexing pins in different modes for the selected device; Please refer to Figure 5-31 for the detailed configuration options.

Figure 5-31 Configure Multiplexing Pins



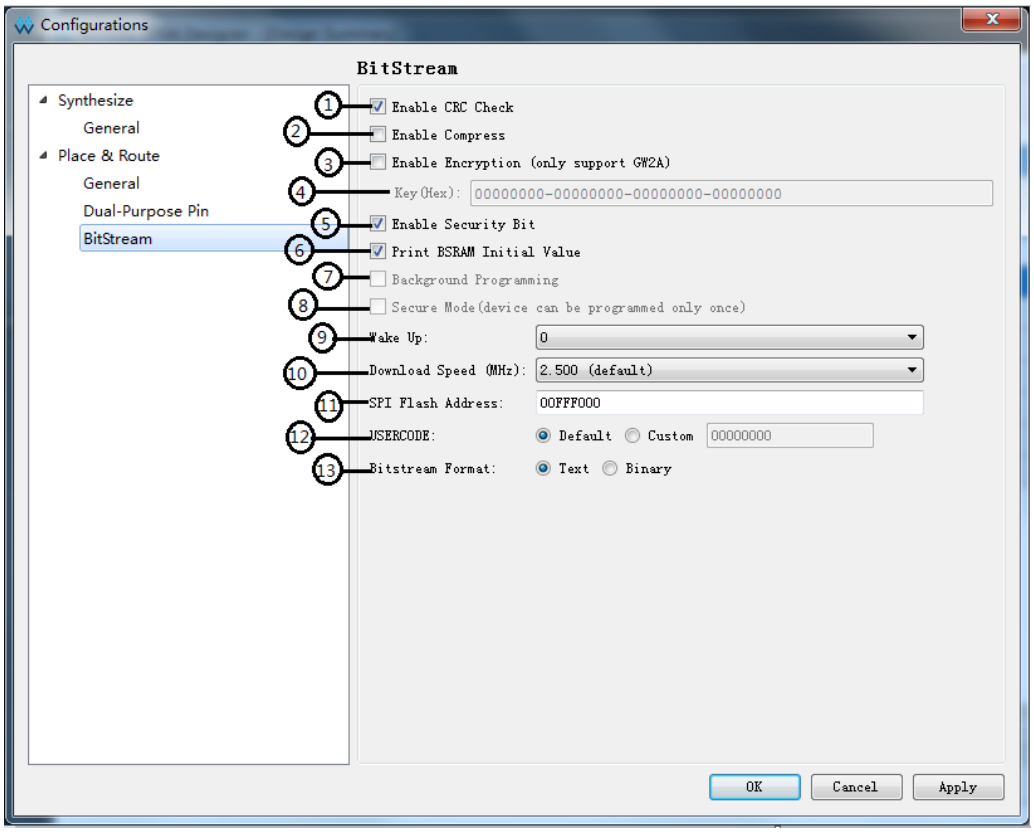
Note!

The JTAGSEL_N and JTAG pins are exclusive. When the JTAG pin is not checked, the JTAGSEL_N pin will be checked by default. When the JTAG pin is checked, the JTAGSEL_N pin will not be checked by default.

Bitstream

Users can configure the bitstream files format or frequency, etc. See Figure 5-32 for the detailed options.

Figure 5-32 Configure Bitstream File



① Enable CRC Check
② Enable Compress
③ Enable Encryption (only supports GW2A)
④ User Defined Key (Hex)
⑤ Enable Security Bit
⑥ Print BSRAM Initial Value
⑦ Background Programmimg
⑧ Secure Mode
⑨ Wake Up
⑩ Download Speed (MHz)
⑪ SPI Flash Address
⑫ User Code
⑬ Bitstream Format

Note!

- The SPI Flash address refers to the initial address to which the bitstream will be loaded for the next multiboot. For further details, please refer to *Gowin Programmer User Guide*.
- The secure mode only supports GW1NSE-2C. When checked, JTAG pins are automatically set to GPIO, and bitstream files can only be programmed to the device once

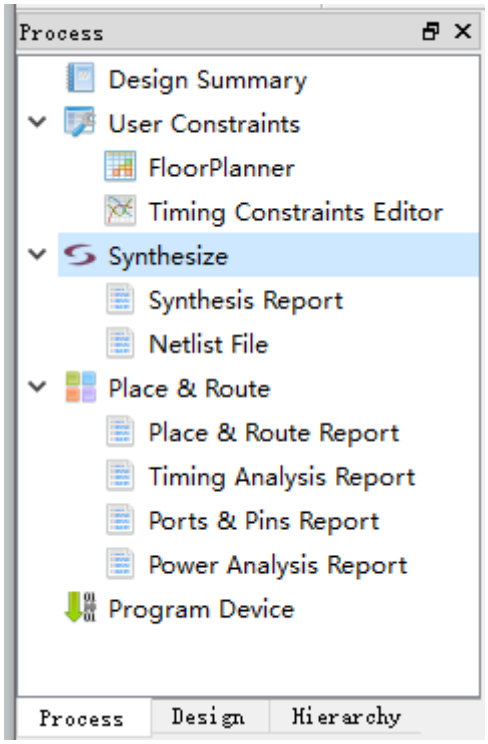
5.4 Manage Project

The Process view provides a system-level overview of the FGPA design flow, as shown in Figure 5-33. The Process View incorporates the following actions:

- View design summary;
- Start FloorPlanner;
- Start timing constraints editor;
- Implement Synthesis;
- View post Place & Route report;
- Implement Place & Route;

- Check the report generated after Place & Route;
- Start GOWINSEMI FPGA programmer, etc.

Figure 5-33 Project Process View



5.4.1 Design Summary

When you create a project, YunYuan software will provide a project summary, as shown in Figure 5-34. Use one of the following three methods to open the design summary.

- From the menu bar, select "Window > Design Summary";
- In the Process View, double-click "Design Summary";
- In the Process View, right-click "Design Summary", and then select "Open".

Figure 5-34 Project Summary

General	
Project File:	D:\gowin_project\1.9.0\fpga_project_1\fpga_project_1.gprj
Synthesis Tool:	SynplifyPro

Target Device	
Part Number:	GW1N-LV4PG256C6/I5
Series:	GW1N
Device:	GW1N-4
Package:	PBGA256
Speed Grade:	C6/I5
Core Voltage:	LV

5.4.2 User Constraints

User constraints provide quick access to and creation of constraints files. For the detailed operation, please refer to the *Gowin Design and*

Constraint User Guide.

User constraints contain the FloorPlanner and Timing Constraints Editor.

Please follow the steps outlined below to use the FloorPlanner:

1. Double-click "FloorPlanner" or select "Run" from the right-clicking menu. If the project has not been synthesized, the prompt dialog box will appear, as shown in Figure 5-35. After synthesis, double-click "FloorPlanner" or select "Run" from the right-clicking menu to open the Physical Constraints Editor;
2. If the physical constraints file already exists in the project, the editor will read it directly when the editor is opened.
3. If the existing physical constraints file (.cst) is modified and saved, click on the  icon in the Physical Constraints Editor to reload the modified constraints file;
4. If the project does not include the corresponding constraints file, and when users double-click FloorPlanner after synthesis, YunYuan will prompt the user to create a constraints file, as shown in Figure 5-36;
5. If the project does not include a physical constraints file, but a constraints file with the same name exists in the source file directory, a warning dialoge box will appear and ask whether you want to override it or not, as shown in Figure 5-37.

Note!

Users can open the Floor Planner and Timing Constraints Editor directly instead of implementing design files synthesis by selecting "Tools > Floor Planner/Timing Constraints Editor".

Figure 5-35 Run Synthesize First

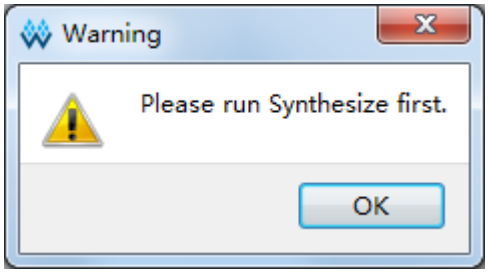


Figure 5-36 Constraint File Creation Prompt

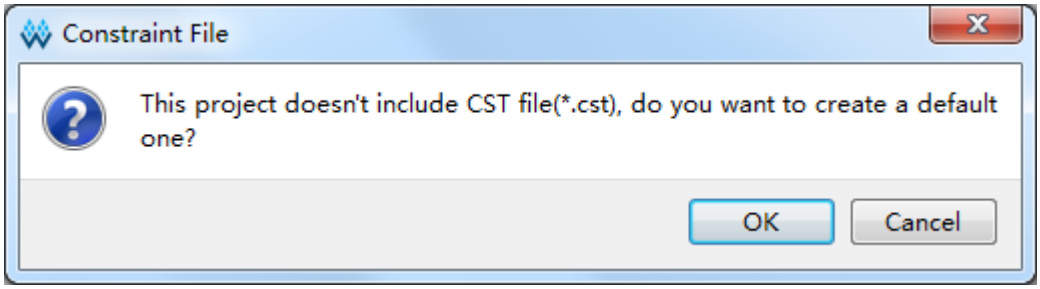
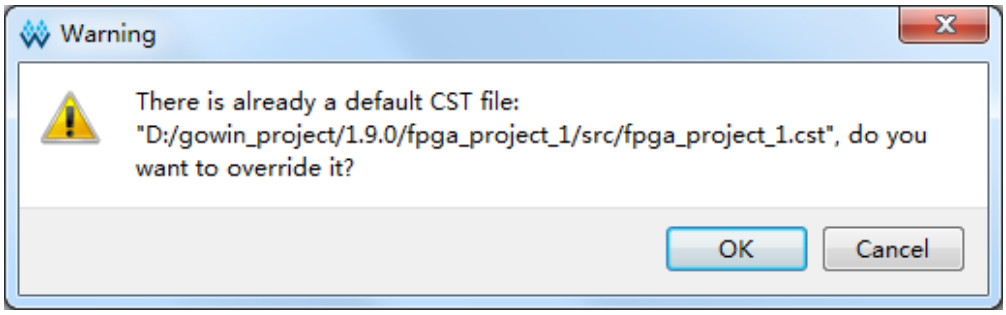


Figure 5-37 Warning - Same Constraints File



Refer to the following steps to use the Timing Constraints Editor:

1. Double-click "Timing Constraints Editor" or select "Run" from the right-clicking menu. If the project has not been synthesized, the prompt dialog box will appear, as shown in Figure 5-35. After synthesis, double-click "Timing Constraints Editor" or select "Run" from the right-clicking menu to open the Physical Constraints Editor;
2. If the timing constraints file (.sdc) exists in the project, the editor will read it directly when the editor is opened.
3. If the project does not include the corresponding constraints file, YunYuan will prompt users to create a constraints file, as shown in Figure 5-38;
4. If the project does not include a physical constraints file, but a constraints file (.sdc) with the same name exists in the source file directory, a warning dialoge box will appear and ask whether you want to override it or not, as shown in Figure 5-39.

Figure 5-38 Timing Constraint File

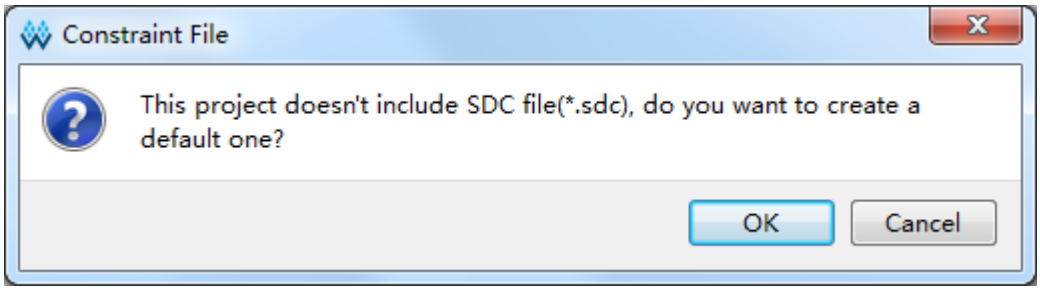
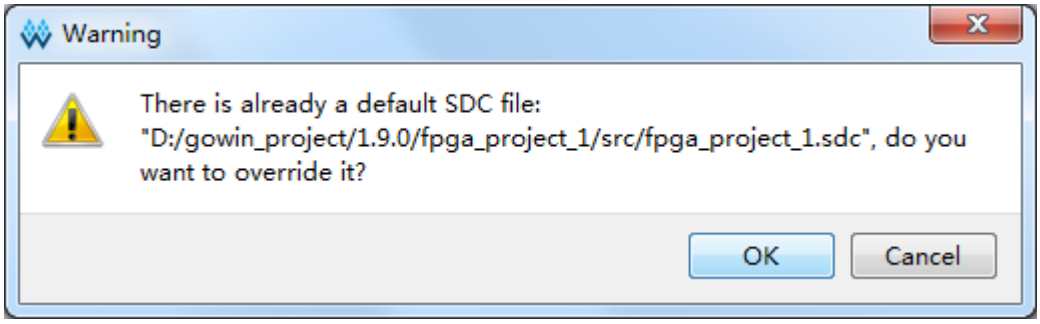


Figure 5-39 Warning - Same Timing Constraints File



5.4.3 Synthesize

Gowin YunYuan software offers two synthesis tools: Synplify Pro and GowinSynthesis. If users do not selected, the default synthesis tool is

Synplify Pro.

Right-click "Synthesize" and select "Configuration" in the Project Design area to open the configuration view, as shown in Figure 5-28.

Synplify Pro is the FPGA synthesis software customized by Synopsys for GOWINSEMI. It supports GOWINSEMI library files implementation, VHDL, and Verilog, etc.

GowinSynthesis is the synthesis tool developed by Gowin. It supports GOWINSEMI library files and their implementations. It only supports System Verilog 2017, Verilog 2001and Verilog 95 currently.

Synthesize provides functions of running synthesis, setting synthesis parameters, and managing Netlist File and Synthesis Report.

Refer to the following steps to run Synthesize:

1. Configure synthesis attributes. Users can select Synplify Pro or GowinSynthesis as the synthesis tool;
2. To configure the Synthesis attributes configuration, please refer to 05.3.3 Modify Project Configuration;
3. Run Synthesize;
4. In Process View, double click "Synthesize" or right-click "Synthesize > Run" to start synthesis of source files.
   If successful, the status icon appears before Synthesize; if not, the status icon appears.
5. After synthesis has been completed successfully, double click "Netlist Report" or right-click and select "Open" to view the Netlist Report, and the netlist file name is the same as the project name. If the synthesis tool selects Synplify Pro, the generated integrated netlist file is *.vm. If the synthesis tool selects GowinSynthesis, the generated integrated netlist file is *.vg.
6. Open the generated netlist file, and you can open "Find & Replace" view by shortcut ctrl+f or clicking "Find" in the toolbar. There are three options in "Find All": Current File, Open Files and Current Project, as shown in Figure 5-40. After clicking "Find All", "Search Result" view will pop up in IDE and the search will be highlighted, as shown in Figure 5-41.

Figure 5-40 Find & Replace View

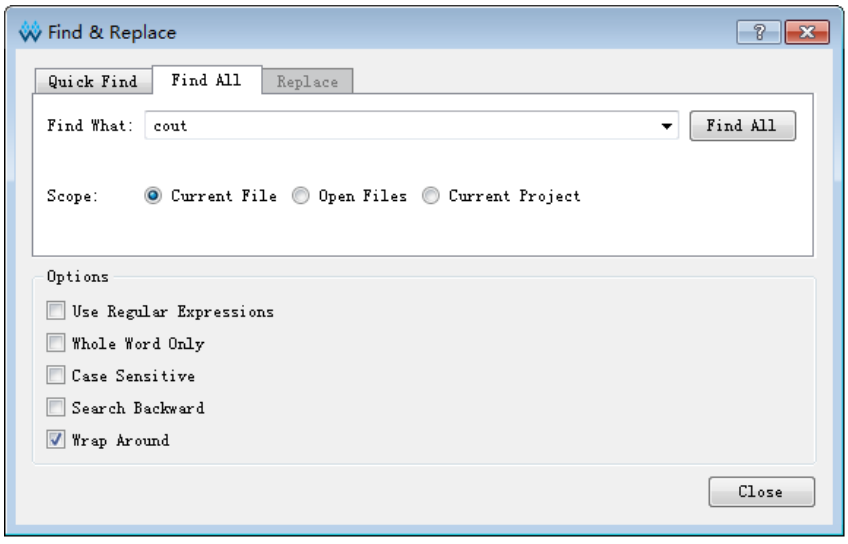
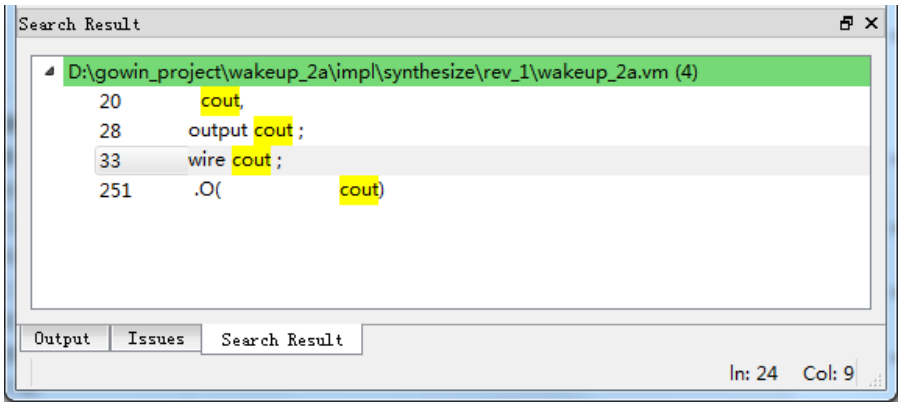


Figure 5-41 Search Result View



Note!

- If the Synthesize icon is before synthesis, double click "Netlist File" or right click to select "Open" to synthesize first, and the netlist file opens after successful synthesis;
- If the synthesize icon is before synthesis, double-click "Synthesis Report" or right-click and select "Open" to synthesize first. The Synthesis Report will open after successful synthesis.

Right-clicking actions of Synthesize, as shown in Figure 5-42

- Run: Only when the icon before Synthesize is , , or , you can select Run to start synthesis of source files;
- Rerun: No matter what Synthesize status is, you can select Rerun to restart synthesis of source files;
- Rerun All: If selecting this option, the source file will be synthesized and placed & routed again no matter what state of the Synthesize and Place & Route is.
- Stop: Stop Synthesize;
- Clean: Select to clean all the generated files and file folders in Synthesize folder, as shown in Figure 5-43;
- Configuration: Used to configure Synthesis parameters.

Figure 5-42 Right-clicking Synthesize

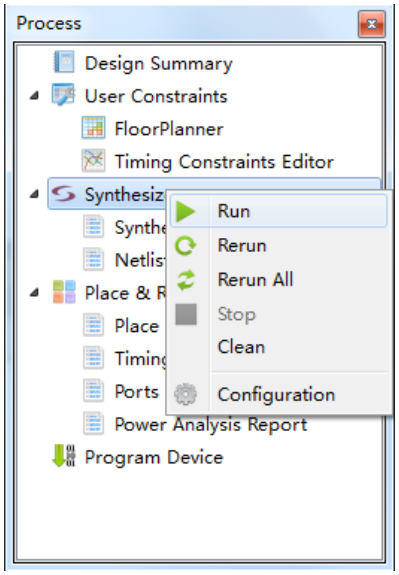
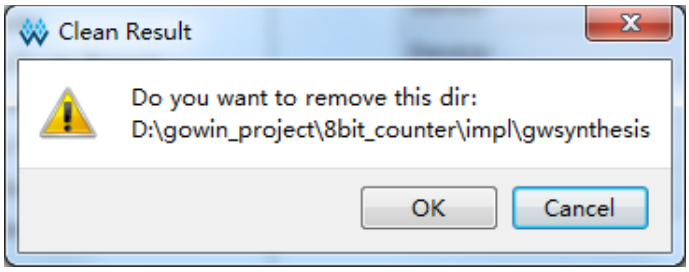


Figure 5-43 Left-clicking Clean



5.4.4 Place & Route

Place and route includes the functionality required to run Place & Route, set the place and route parameters, and manage the post-P&R report.

Note!

Place & Route will be implemented after Synthesize is run. Refer to the following steps to run Place & Route:

1. Configure Place & Route attributes;
2. To configure the Place & Route attributes, please refer to "05.3.3 Modify Project Configuration";
3. Run Place & Route;
4. Double-click "Place&Route", right-click and select "Place & Route > Run" to generate bitstream files and related reports. If running successfully, the ✔ icon will appear before Place & Route. Otherwise, the ❗ will appear;
5. After Place & Route has been run successfully, double-click on "View Post PnR Report" or right-click and select "Open" to view the report.
6. Users can view four kinds of files: Place & Route Report, Timing Analysis Report, Ports & Pins Report, and Power Analysis Report. These reports can not be edited.

   Note!

   - If the report is already opened and is regenerated by implementing Place & Route, YunYuan will ask the users whether they would like the report to be updated.;
   - Before implementing Place & Route, if the status icon before Place & Route is , double click the report or right-click and select "Open" to run Place & Route first. The report will open after Place & Route has been successfully.

Right-clicking actions of Place&Route:

- Run: Users can only select "Run" to start Place & Route only when the icon before Place&Route is , , or ;
- Rerun: Regardless of the Place&Route status, users can select Rerun to rerun Place&Route;
- Rerun All: If selecting this option, the source file will be synthesized and placed & routed again no matter what state of the Synthesize and Place & Route is.
- Stop: Stop Place & Route;
- Clean: Clean all the generated files and file folders in pnr folder. A

prompt box will pop up when clicking this option ;

- Configuration: Configure Place & Route parameters.

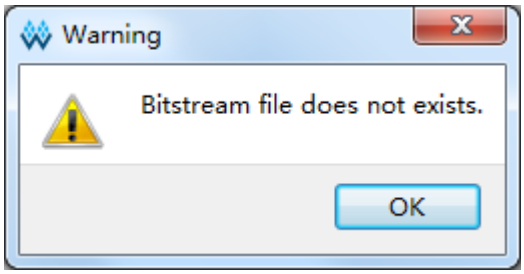
5.4.5 Program Device

Bitstream files will be generated (.fs file) after Gowin YunYuan software has run placement and routing. Start Gowin FPGA programmer to download the bitstream files to the chip to realize user-required functions.

Note!

Bitstream generation will be implemented after running Synthesize and implementing Place & Route. If users do not run synthesize and implement Place & Route first, warnings as shown in Figure 5-44 will appear.

Figure 5-44 Warning

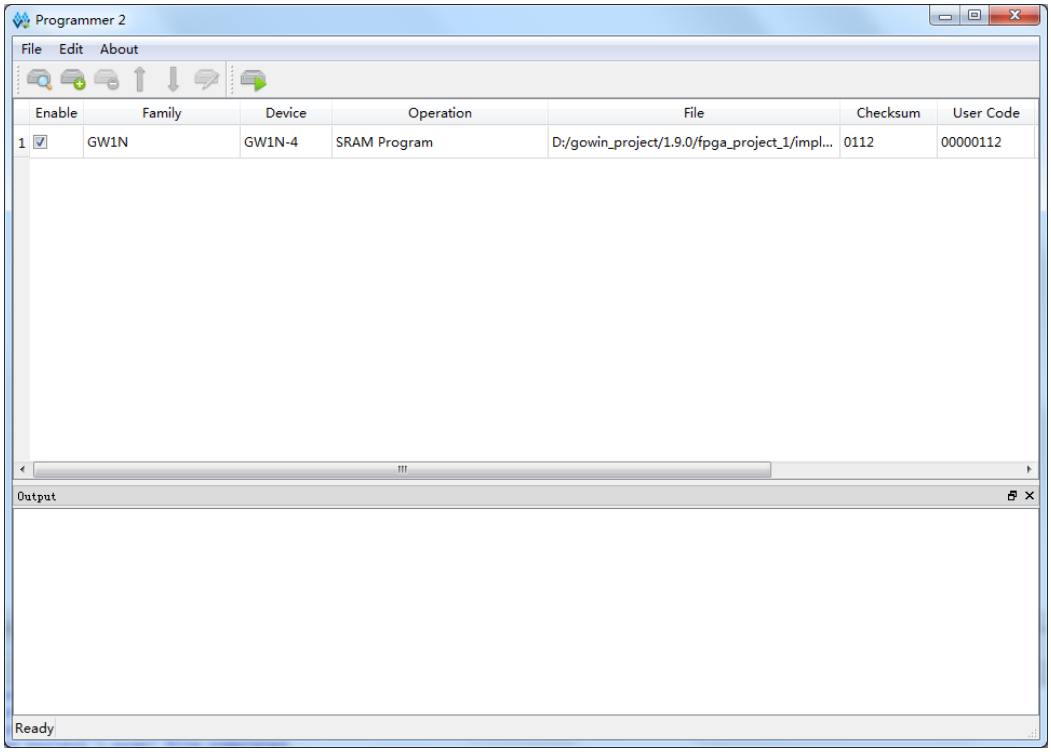


Double-click "Program Device" or right click and select "Run" to open the Gowin FPGA Programmer, as shown in Figure 5-45.

Note!

The programmer in the Linux installation package is Red Hat 5.10. If you need the Red Hat 6/7 programmer, please download it from the Gowin website, rename it as "Programmer", and replace the programmer in the Gowin YunYuan software installation package.

Figure 5-45 Gowin Programmer



For detailed instructions on how to use the Gowin programmer, please refer to *Gowin Programmer User Guide*.

5.5 Archive Project and Loading

IDE supports archive project and restore archived project by clicking Project in the menu bar.

5.5.1 Archive Project

A dialogue will pop up when clicking Project>Archive Project, as shown in Figure 5-46.

- Archive File Name is the archived file name. The default name is the same as the current archived project name with .gar suffix.
- Create In is the path for the archived file, and the default is the current project path.
- The File Types includes Project source files (checked by default), GowinSynthesis files, SynplifyPro files, PnR files and Programming files.
- When a file type is checked, the source file, path and size of the current project are displayed below.
- Add and Remove can be used to add and remove archived files.
- After clicking Archive, a prompt box will pop up if the files in the project are not saved.
- A prompt window will pop up, indicating whether archived successfully or not, as shown in Figure 5-47.
- When the archive is completed, two files are generated under the "Create In" path: the archive project *.gar and the archived file *.garlog.The file with gar suffix compresses and stores all the archived files. The log file with *.garlog suffix is used for checking which files are archived and whether the archive is successful.

Figure 5-46 Archive Project Interface

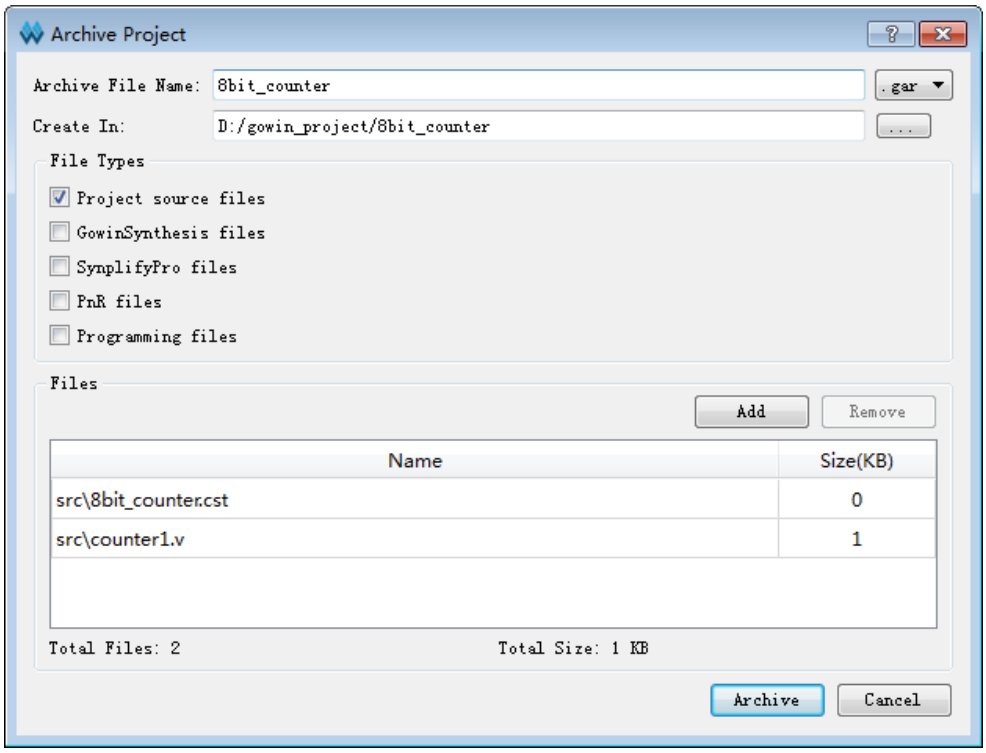
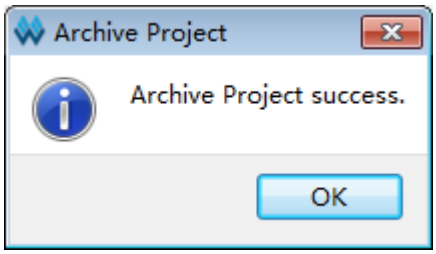


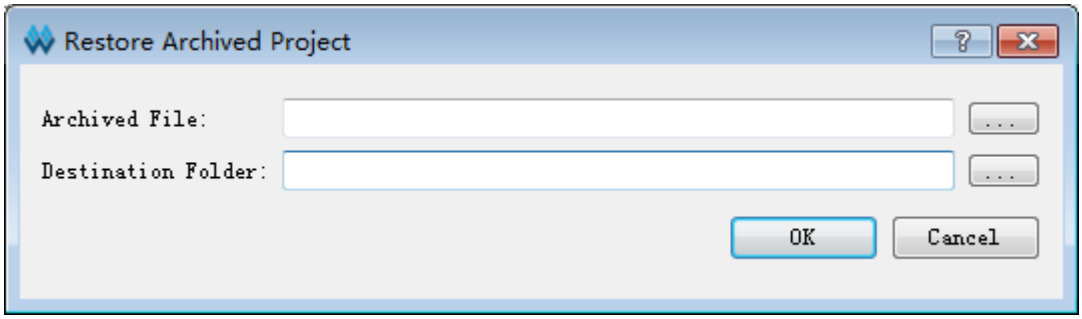
Figure 5-47 Archive Project Prompt



5.5.2 Restore Archived Project

Restore Archived Project dialogue will pop up when clicking Project in the menu bar, as shown in Figure 5-48.

Figure 5-48 Restore Archived Project Interface



Click the button on the right side of Archived File to select the archive file to restore. After selecting, "Destination Folder" is automatically updated to the path where the archive file is. Click OK and a dialog box will pop up.

5.6 Exit IDE

Use the following two methods to exit IDE:

1. Select "File > Exit" from the File menu;
2. Click the "  " icon on the upper right of the IDE.

Note!

- If files are not saved, IDE will prompt you to save the files first;
- Save, Save All, and Save As…are only available for text editing actions;
- Project configuration modification and project files addition and deletion will not be saved to project configuration files in time; they will be saved automatically when the user exits the IDE;
- If the software is running, uses cannot exit IDE by clicking the icon.

6 Tools in YunYuan Software

6.1 Synplify Pro

Synplify Pro is the FPGA synthesis software customized by Synopsys for GOWINSEMI. It supports GOWINSEMI library files implementation, VHDL, and Verilog, etc.

For more detailed information about the operation of Synplify Pro, please refer to the manuals in the *"Help" drop-down list that appears on the Synplify Pro menu bar.*

6.2 FloorPlanner

The Gowin FloorPlanner is Gowin self-developed tool used for Place & Route and physical constraints editing. It supports attributes and location reading and modification of I/O, Primitive, block, and Group, etc. It also supports the generation of new layout and constraints files per user configuration. The files define I/O attributes, primitives, module location, etc. Gowin FloorPlanner supports all GOWINSEMI FPGA devices.

FloorPlanner can be started using two methods:

1. If no FPGA project is created, users can select "Tools > FloorPlanner" directly from the menu bar. The user will need to add netlist files, constraints files, and devices information by selecting "File > New";
2. If an FPGA project is already created, run Synthesize, then double-click "FloorPlanner" directly in the Process View. The Floorplanner will then load the project files directly before displaying them.

The FloorPlanner contains Chip Array and Package View. Please refer to Figure 6-1 and Figure 6-2 for examples. For more detailed operation of FloorPlanner, please refer to the *Gowin Design Constraints Guide*. The FloorPlanner also supports timing optimization.

Figure 6-1 Chip Array View

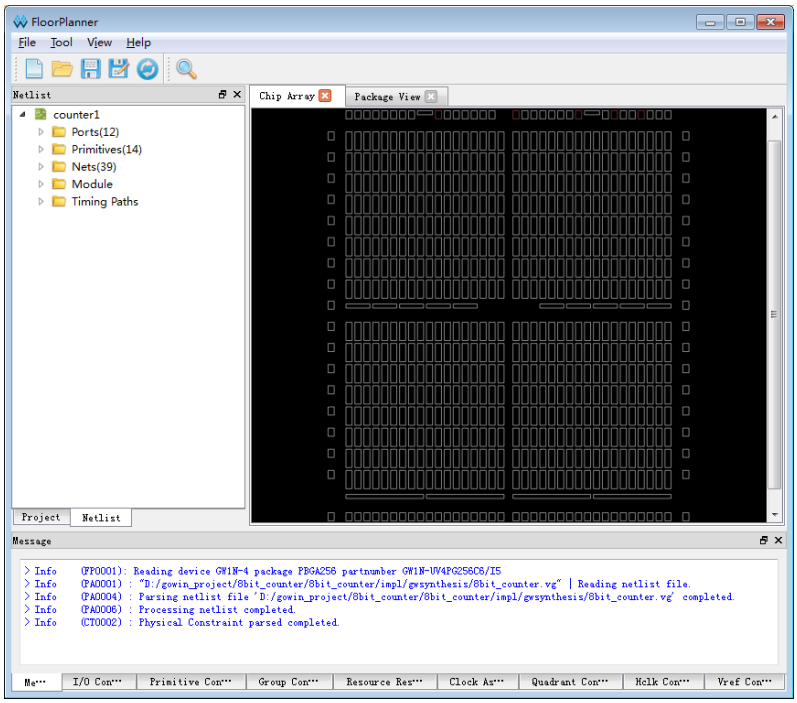
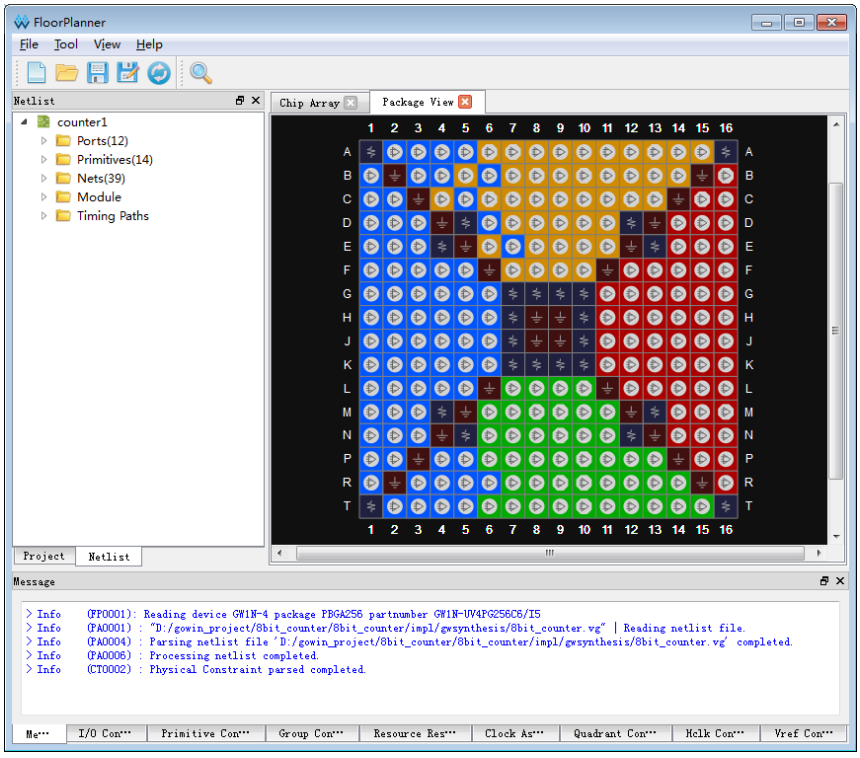


Figure 6-2 Package View



6.3 Timing Constraints Editor

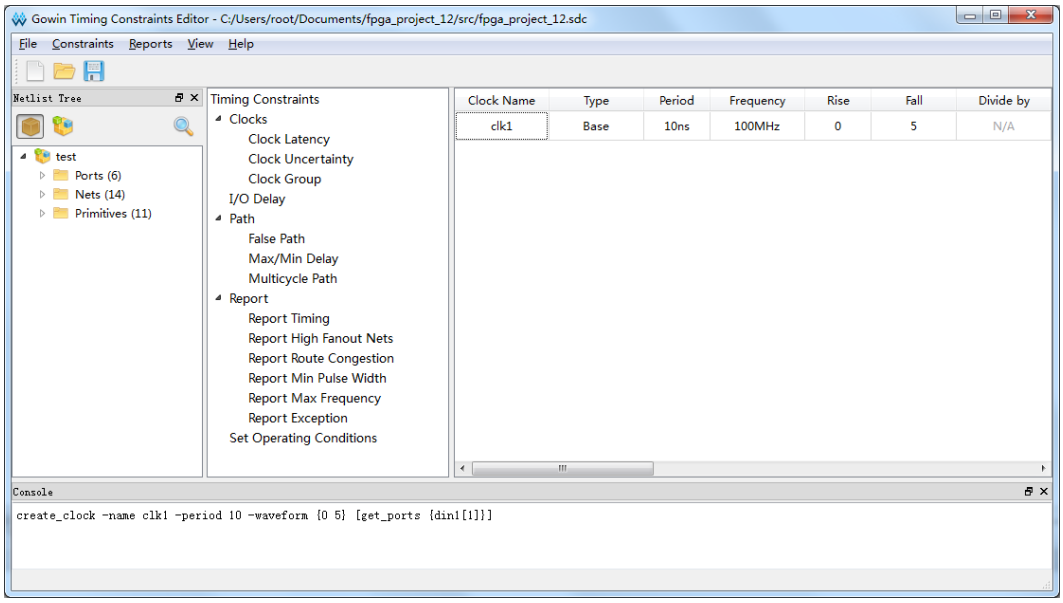
The Gowin Timing Constraints Editor supports multiple timing constraints commands editing, including clock constraints, I/O constraints, path constraints, and clock report constraints. The Timing Constraints Editor allows an easy and quick timing constraints editing. It supports all GOWINSEMI FPGA devices.

Timing Constraints Editor can be started using two methods:

1. If no FPGA project is created, users can select "Tools > Timing Constraints Editor" from the menu bar. Add netlist files by selecting "File > New";
2. If an FPGA project is already created, run Synthesize, double-click "Timing Constraints Editor", and the Timing Constraints Editor will load project files directly and display them, as shown in Figure 6-3.

For the detailed operation, please refer to *Gowin Design and Constraint User Guide.*

Figure 6-3 Clock Creation Interface



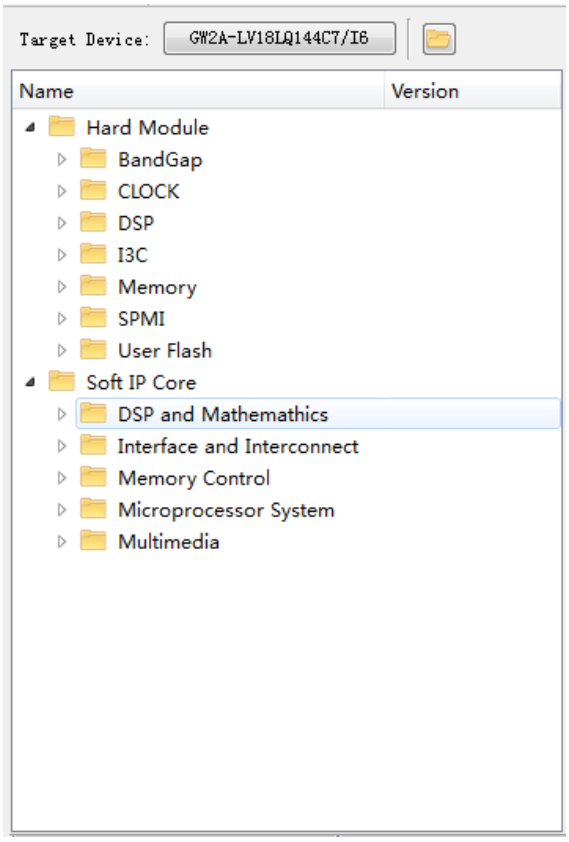
6.4 IP Core Generator

The IP Core Generator in Gowin software is mainly used to generate instantiation components and IPs, which the users can call to implement the required functions. As such, they provide users with a convenient method of creating complex designs. The IP Core Generator includes the modules associated with primitives and the IP Cores associated with reference designs, as shown in Figure 6-4.

Start the IP Core Generator by selecting "IP Core Generator" from the Tools menu.

For further details about the each IP call method, please refer to *Gowin IP Core Generator User Guide.*

Figure 6-4 IP Core Generator Page



Note!

The current device does not support the Module and IP Cores which are displayed as grey.

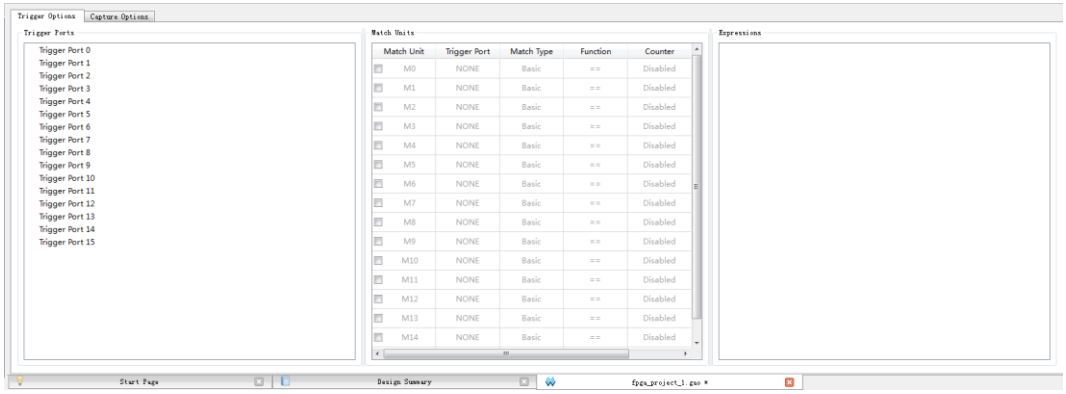
6.5 Gowin Analyzer Oscilloscope

The Gowin Analyzer Oscilloscope (GAO) is a digital signal analyzer that was independently designed by Gowin. It helps users to analyze signal timing in design more easily, and quickly conduct system analysis and fault location, thereby improving design efficiency.

The GAO includes the Gowin GAO and the Gowin Analyzer Oscilloscope. The Gowin GAO is mainly used to insert position information into the design, which is predominantly based on the sampling clock, trigger unit, and trigger expression. The Gowin Analyzer Oscilloscope connects software and target hardware through the JTAG interface, and visually displays the data for the sampled signal set by Gowin Core Inserter with waveform.

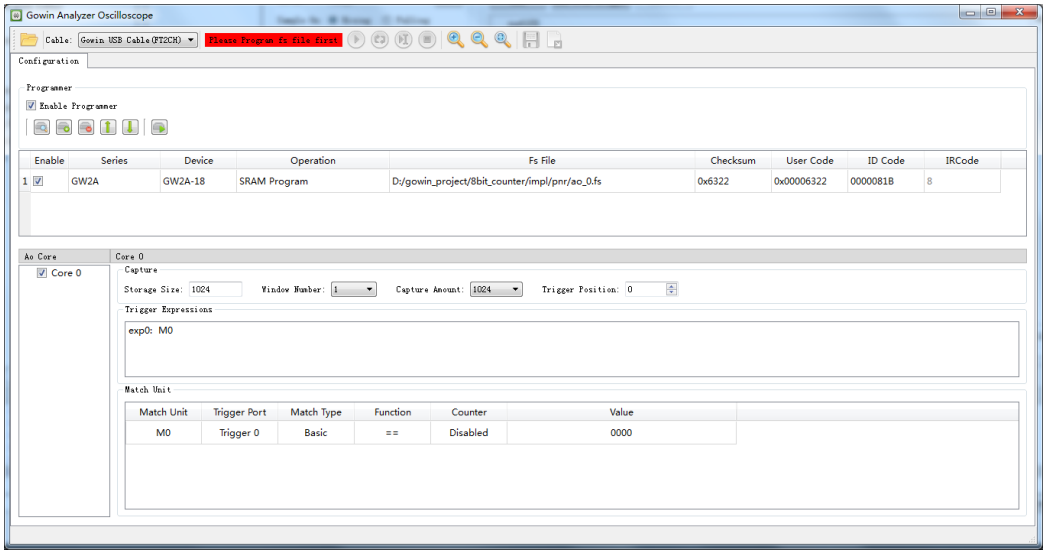
Before starting the GAO, create the GAO configuration file (.gao) in the Project View to open the GAO configuration view, as shown in Figure 6-5.

Figure 6-5 GAO Configuration View



After the configuration file has been created, select "Tools > Gowin Analyzer Oscilloscope" from the menu bar to open the Gowin Analyzer Oscilloscope, as shown in Figure 6-6.

Figure 6-6 GAO



For further details about how to use the Gowin Analyzer Oscilloscope, please refer to the *Gowin Analyzer Oscilloscope User Guide*.

6.6 Gowin Power Analyzer

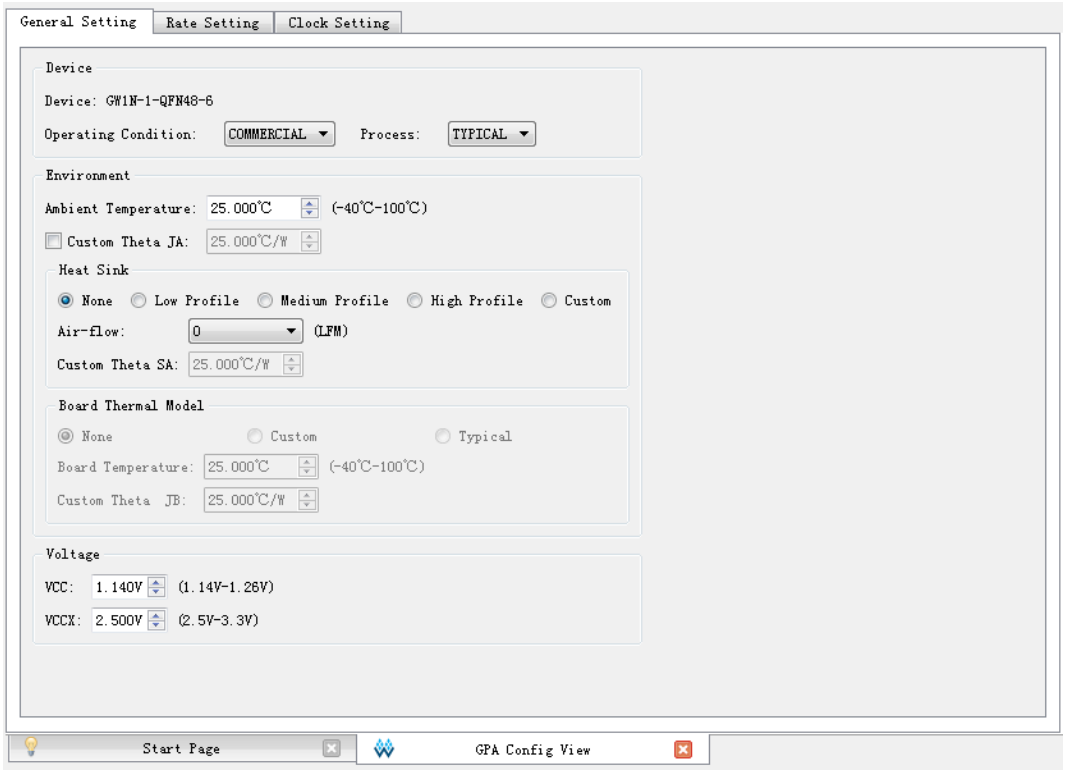
The Gowin Power Analyzer (GPA) estimates the power dissipation for your design and provides rich user configuration options. It should be configured per the actual design. The closer the configuration is to the actual design, the more accurate the power dissipation analysis will be.

Based on the new configuration file (.gpa), follow the steps outlined below to start the GPA:

1. In the File menu, select "File> New…" to open a "New" dialog box;
2. Select "GPA Config File" and enter "Name" in the pop-up "New GPA Config File" ;
3. Click "OK", and the new GPA config file will be displayed in the Project Design View;

4. Double click on the file name to open the GPA Config view, as shown in Figure 6-7.

Figure 6-7 GPA Config View



For further details about how to use the GPA, please refer to the *Gowin Power Analysis User Guide*.

6.7 Memory Initialization File Editor

The Memory Initialization File is an ASCII file with an .mi suffix. You can generate the corresponding Initialization File according to your design to specify the initial value for the memory of each address.

Each line in the Memory Initialization File correlates with one memory. The number of lines is the number of memories and also the memory address depth. The number of columns represents each memory bit; that is, the memory data width. The address decreases from top to bottom with the most significant bit first for each line.

The Gowin Memory Initialization File supports the Bin File, Hex File, and Address-Hex File formats. The following are examples of the .mi file format.

Bin File

Bin file is a text file that consists of the 0 and 1 binary numbers. The line represents address depth, and the column represents data width.

#File_format=Bin

#Address_depth=16

#Data_width=32

00001100000100000000100100010000

10000000010010000100000001000000

01000000100000001000000010000000

00100000100001001100000011000000

00000100000001000000010000000100

01000010001010100000101000001010

00100010010001000000010001000110

01000101000001110000010101000001

01100100001001001000010000100100

01001001010010010010100101001001

01100101001001010000010100100101

11000001101001010000010110100101

01001000100010000010110000001100

10000101001011010100110100101101

01101100001100110000011100011001

00001001001010010100000110010000

Hex File

The Hex file is similar to the Bin file. It consists of hexadecimal numbers 0~F. The line represents the address depth, and the binary bits in each line represents data width.

#File_format=Hex

#Address_depth=8

#Data_width=16

3A40

A28E

0B52

1C49

D602

0801

03E6

4C18

Address-Hex File

Address-Hex file is the file that includes both the data and the address with data record. The address and the data is composed of the hexadecimal number of 0~F. In each line, the address is located before the colon, and the data is located after the colon. The address with no data record is 0 by default.

```
#File_format=AddrHex
#Address_depth=256
#Data_width=16
9:FFFF
23:00E0
2a:001F
30:1E00
```

Based on the new configuration file (.mi), refer to the following steps to use the initialization file editor:

1. In the File menu, select "File> New…" to open the "New" dialog box;
2. Select "Memory Initialization File", as shown in Figure 6-8. Click "OK" and enter the initialization file name in the pop-up "New File" window, and then click "OK", as shown in . The Initialization File Configuration View is as shown in Figure 6-9;
3. Start the file initialization view as shown in Figure 6-10. Enter the initial value on the left side and configure the initialization file format and depth/width and view on the right side;
4. On the right side, configure the depth and width for the initialization file and the format for the address and initial values in the left table.
   - The depth and width values should be same as the Block Memory or Shadow Memory address depth and data width set in the IP Core Generator. If the address depth and data width in the initialization file are greater than the values set in the IP Core Generator, the IP Core Generator will display the error message. If the depth and width values are less than the BSRAM address depth and data width set in the IP Core Generator, the value of the unassigned address will be initialized to 0 by default. Click "Update" after configuration.
   - The display format of address and numbers on the left can be configured as binary, hexadecimal, and address- hexadecimal, etc.
5. Enter the initial value on the left table, and set the view layout.
   - Right-click on the table header to configure the column number which can be displayed as 1, 8, or16, as shown in Figure 6-11.
   - Double-click and enter the initial value, or right-click to set the value. "Fill with 0" means the initial value is 0, "Fill with 1" means each bit of the initial value is 1, and "Custom Fill" means you can write according to your needs or batch setting, as shown in Figure 6-12.
6. Save the file.

Figure 6-8 New Memory Initialization File

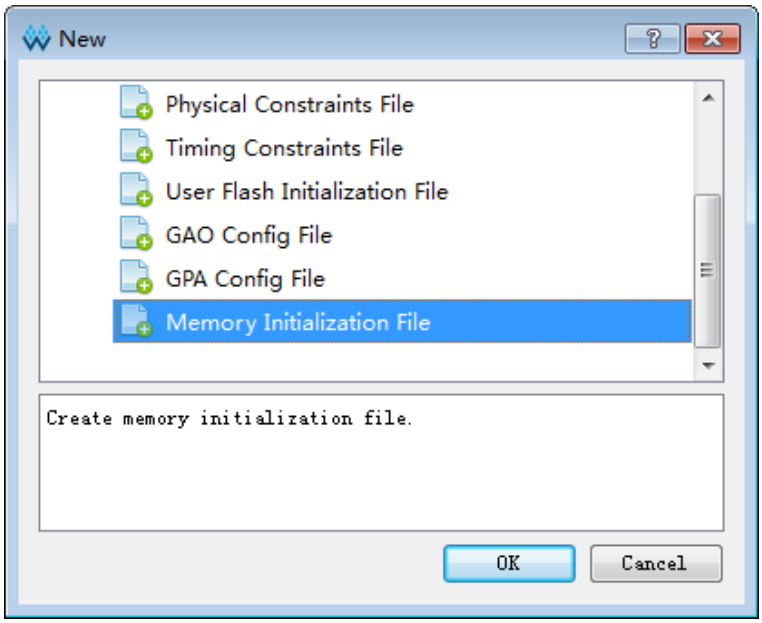


Figure 6-9 New File

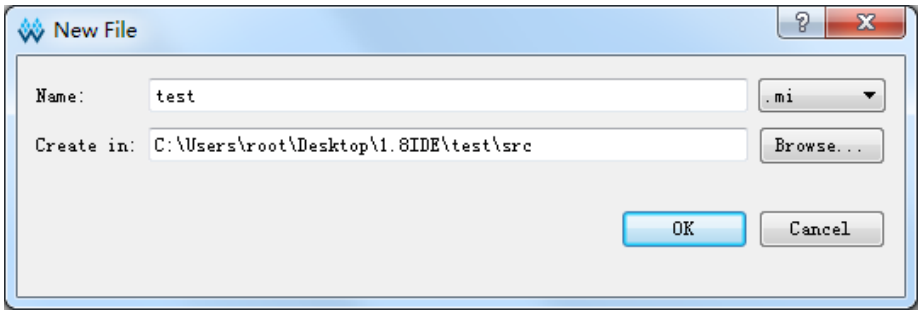


Figure 6-10 Initialization File Configuration

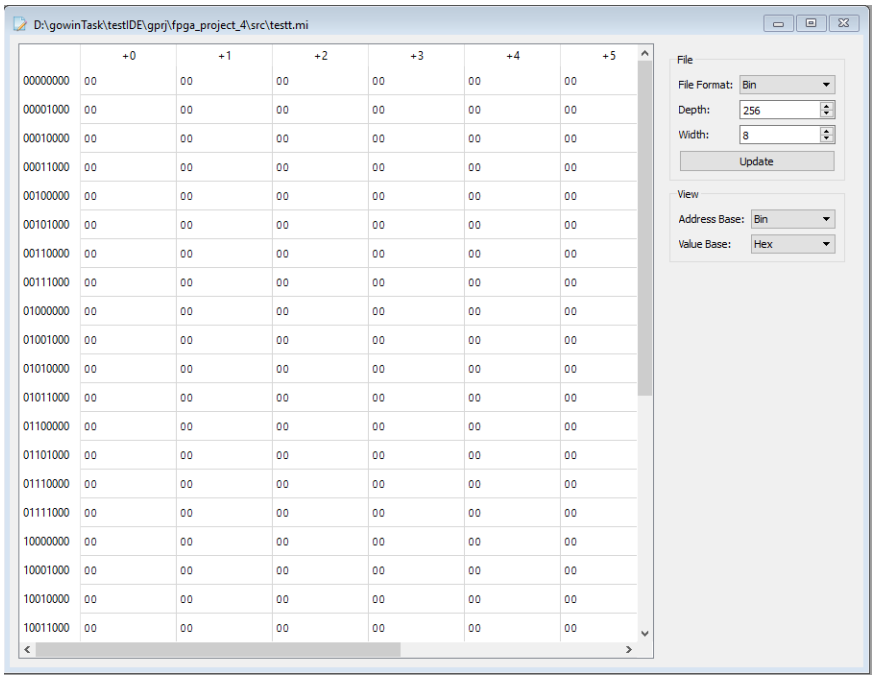


Figure 6-11 Column Setting

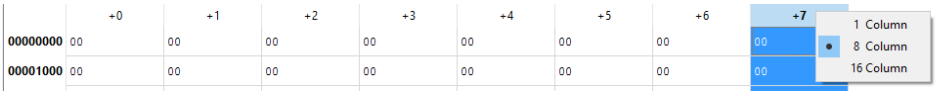
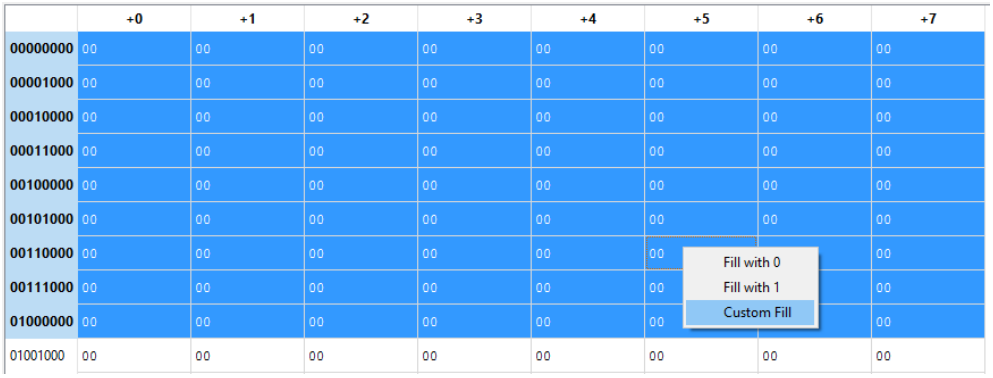


Figure 6-12 Batch Setting



7 Description of Gowin YunYuan Output Files

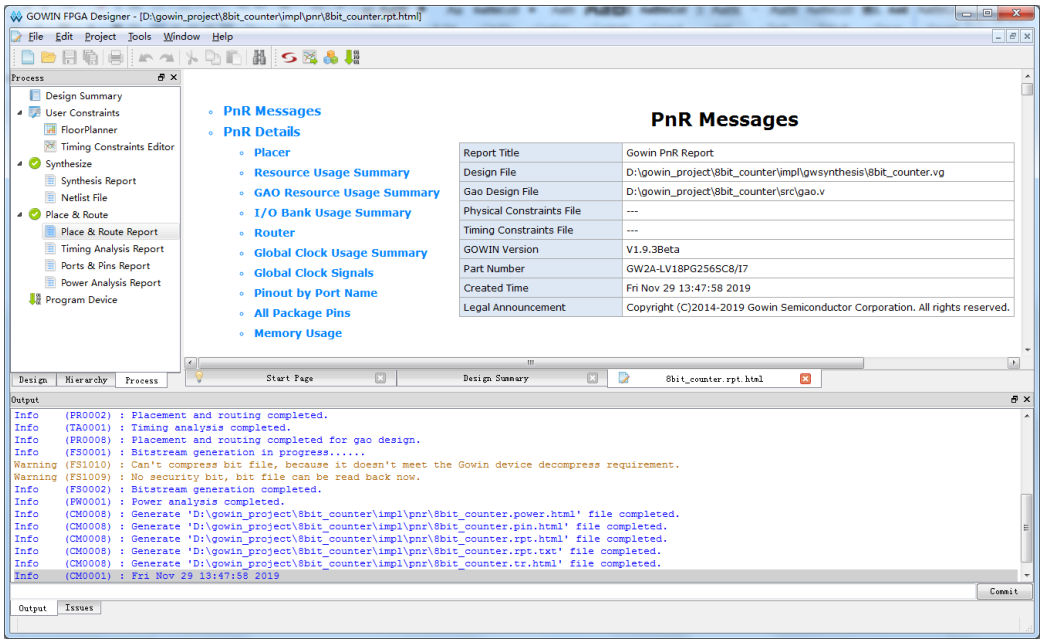
In the process of FPGA design, Gowin YunYuan software generates bitstream files, and pin constraints location files (io.cst), and also generates multiple reports depending on different parameters. The reports include the place&route report, timing report, and power analysis report. In addition, you can right-click on Place & Route to modify the configuration and attributes and generate pins constraints, physical netlist files, etc.

7.1 Place & Route Report

The Place & Route Report describes the resource, memory consumption, time consumption, etc. occupied by the user design, with the file suffix as .rpt.html. Check the *.rpt.html file for further detailed information.

Double-click "Place & Route Report" in the Process View to open the project that corresponds to the Place & Route report, as shown in Figure 7-1.

Figure 7-1 Place & Route Report

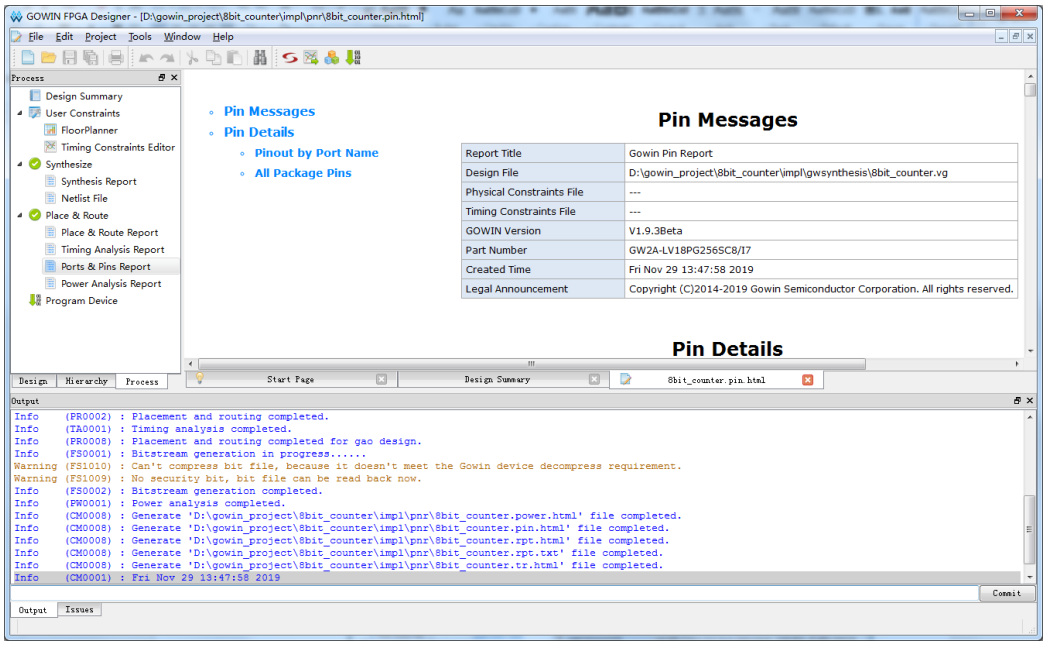


7.2 Ports and Pins Report

The Ports and Pins Report is the output of the ports and pins files output after placement. It includes ports type, attributes, and ports locations, etc. The generated file is saved with the .pin.html extension. Check the .pin.html file for further details.

Double-click "Ports & Pins Report" in the Process View to open the report corresponding to the project, as shown in Figure 7-2.

Figure 7-2 Ports & Pins Report



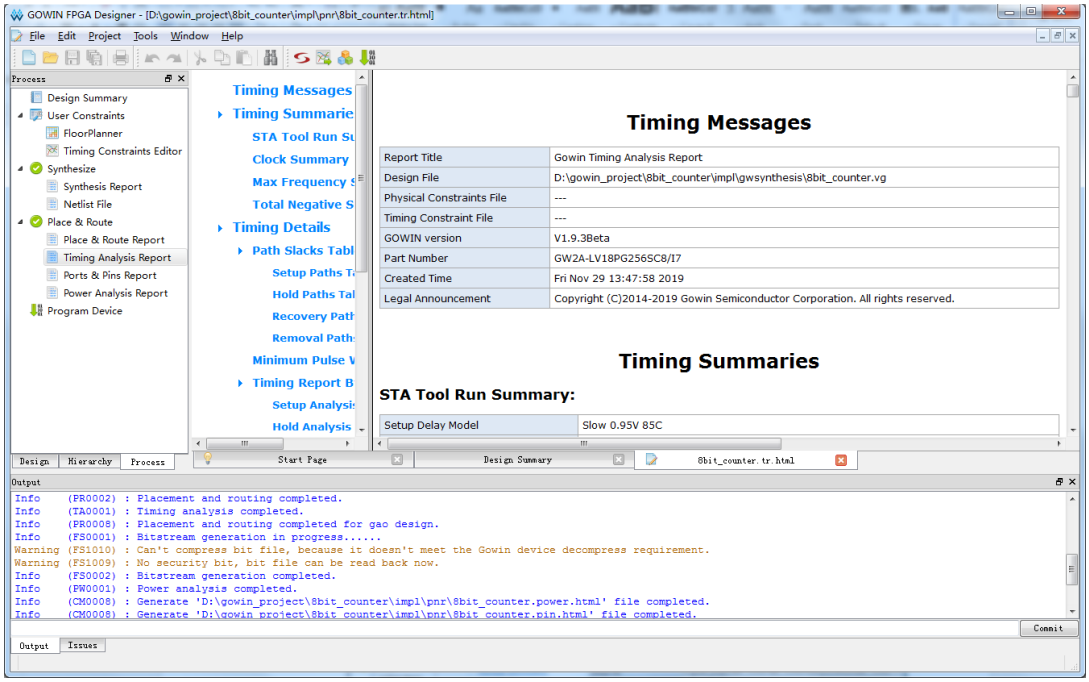
7.3 Timing Report

The timing report is available in web format and text format. The default is web format.

The Timing report includes set-up time check, hold-time check, restoring time check, removal time check, Min. clock pulse check, max. fan out path, Place&Route congestion report, etc. by default. The timing report also includes the Max. frequency report.

Double-click "Timing Analysis Report" in the Process View to open the timing analysis report for the project, as shown in Figure 7-3.

Figure 7-3 Timing Report



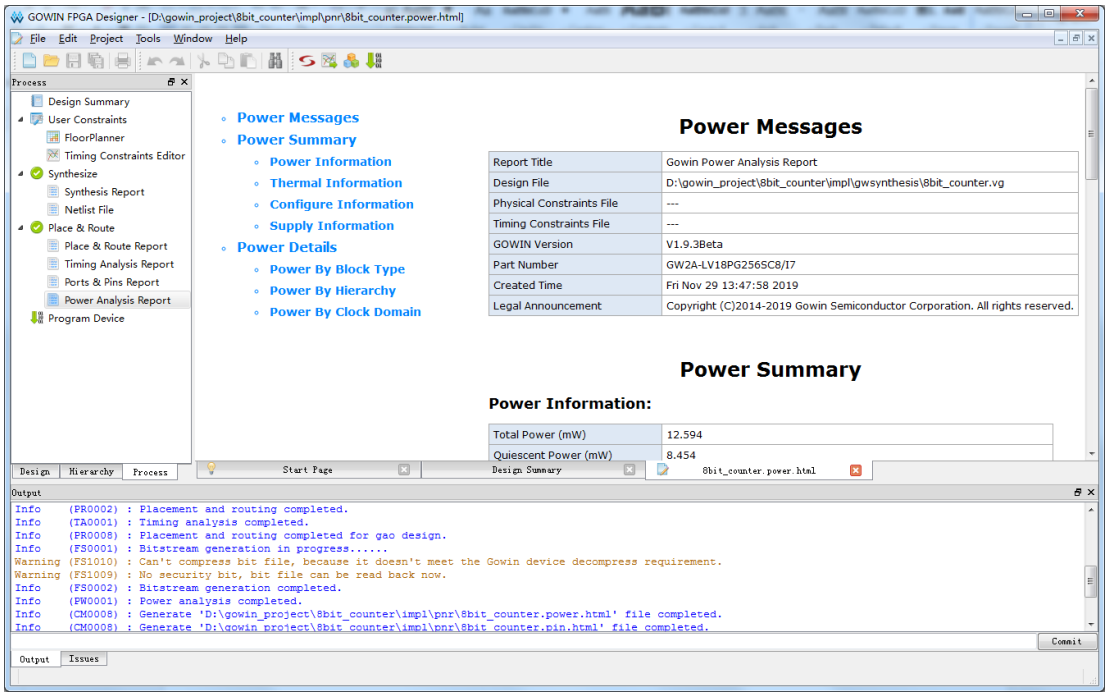
7.4 Power Analysis Report

The Power Analysis Report mainly includes the power dissipation estimation for your design. It is designed to help you evaluate the basic power consumption of your design.

Double-click "Power Analysis Report" in the Process View to open the analysis report that corresponds to the project, as shown in Figure 7-4.

To adjust the factors that influence power dissipation, please refer to *Gowin Power Analysis User Guide*.

Figure 7-4 Power Analysis Report



Appendix A SynplifyPro Attributes and Directives

A.1 Attributes and Directives

full_case

Indicate that all possible values have been given, and that no additional hardware is needed to preserve the signal values for Verilog designs only.

Syntax

object /* synthesis full_case */ ;

Description

"object" can be a case, casex, or casez statement.

parallel_case

Forces a parallel-multiplexed structure rather than a priority-encoded structure for Verilog designs only.

Syntax

object /* synthesis full_case */ ;

Description

"object" can be a case, casex, or casez statement.

translate_on/translate_off

Synthesize designs originally written for use with other synthesis tools without needing to modify the source code. Allow you to synthesize designs originally written for use with other synthesis tools without needing to modify source code. All source code that is between these two directives is ignored during synthesis.

Syntax

/* synthesis translate_off */

code

/* synthesis translate_on */

syn_encoding

Overrides the default FSM Compiler encoding for a state machine and applies the specified encoding.

Syntax

object /* synthesis syn_encoding = "value" */ ;

Description

- object defines the state register;
- value includes:
  - default: The default is that the tool automatically picks an encoding style that results in the best performance.
  - onehot: Only two bits of the state register change (one goes to 0, one goes to 1) and only one of the state registers is hot (driven by 1) at a time;
  - gray: Adopts gray encoding style;
  - sequential: Adopts natural encoding style;
  - safe: This implements the state machine in the default encoding and adds reset logic to force the state machine to a known state if it reaches an invalid state.
  - original: This respects the encoding you set, but the software still does state machine and reachability analysis.

syn_keep

Preserves the specified net and keeps it intact during optimization and synthesis.

Syntax

object /* synthesis syn_keep = 0|1 */ ;

Description

- object is the object of net.
- Syn_keep values include:
  - 0:Net is involved in optimization.
  - 1: Preserves the net without optimizing it away.

syn_hier

Control the amount of hierarchical transformation across boundaries on module or component instances during optimization.

Syntax

In an FDC file:

define_attribute {object } syn_hier { value }

define_global_attribute syn_hier {flatten}

In a Verilog file:

object /* synthesis syn_hier = " value " */ ;

In a VHDL file:

attribute syn_hier of object : architecture is " value " ;

Description

syn_hier value includes:

- soft（default value）: Synplify decides the optimum boundary, affecting the specified design cell only;

- firm: Preserve the design cell interface, and the cell is allowed to across boundary, affecting the specified design cell only;
- hard: Preserve the design cell interface strictly, affecting the specified design cell only;
- fixed: Preserve the design cell interface, fix all the cross boundaries during optimization, and preserve the ports interface;
- remove: Remove the hierarchy of property-declaration, but not affecting the lower hierarchy cells;
- macro: Preserve the design cell interface and content strictly;
- flatten: Use flatten combined with other values.

loop_limit

Specify a loop iteration limit for the loop in a Verilog design when the loop index is variable, not constant.

Syntax

beginning_of_loop_statement /* synthesis loop_limit integer */;

syn_looplimit

Specify a loop iteration limit for a for loop in a VHDL design when the loop index is a variable, not a constant.

Syntax

attribute syn_looplimit : integer;

attribute syn_looplimit of labelName : label is value;

syn_noprune

Prevent optimizations for instances and black-box modules (including technology-specific primitives) with unused output ports. By default, the synthesis tool removes any module that does not drive logic as part of the synthesis optimization process.

Syntax

In an FDC file:

define_attribute {module|instance} syn_noprune {0|1}

In a Verilog file:

object /* synthesis syn_noprune = 1 */ ;

In a VHDL file:

attribute syn_noprune : boolean

Description

- The object can be module, declaration, or instances.
- syn_noprune values include:
  - 0: Allows instances with unused output ports to be optimized away.
  - 1: Prevents optimizaiton for instances with unused output ports.

syn_preserve

Prevent sequential optimizations such as constant propagation, inverter push-through, and FSM extraction.

Syntax

In a Verilog file:

object /* synthesis syn_preserve = 0 |1 */

In a VHDL file:

attribute syn_preserve of object : objectType is true | false;

Description

- object can be register signal or Module.
- syn_preserve values can be:
  - 0: Optimizes registers as needed.
  - 1: Preserves register logic.

A.2 Mapping Attributes and Directives

syn_allow_retiming

Determine if registers can be moved across combinational logic to improve performance.

Syntax

In an FDC file:

define_attribute {register} syn_allow_retiming {1|0}

define_global_attribute syn_allow_retiming {1|0}

In a Verilog file:

object /* synthesis syn_allow_retiming = 0 | 1 */;

In a VHDL file:

attribute syn_allow_retiming of object : objectType is true | false;

syn_ramstyle

Specify the implementation for an inferred RAM. Can be mapped to registers signal driven by RAM or RAM instances.

Syntax

In an FDC file:

define_attribute { signalname [bitRange]} -syn_ramstyle {registers | block_ram | distributed_ram | no_rw_check | rw_check | no_rw_check_diff_clk}

define_global_attribute syn_ramstyle {registers | block_ram | distributed_ram | no_rw_check | rw_check | no_rw_check_diff_clk}

In a Verilog file:

object /* synthesis syn_ramstyle =value */

In a VHDL file:

attribute syn_ramstyle of object : objectType is value;

syn_romstyle

You can infer ROM architectures using a case statement in your code. For the synthesis tool to implement a ROM, at least half of the available addresses in the case statement must be assigned a value.

Syntax

In an FDC file:

define_attribute { romPrimitive } syn_romstyle {logic | block_ram | distributed}

In a Verilog file:

object /* synthesis syn_romstyle = "logic | block_ram | distributed" */;

In a VHDL file:

attribute syn_romstyle of object : objectType is "logic | block_ram | distributed ";

syn_replicate

Control replication of registers during optimization.

Syntax

In an FDC file:

define_global_attribute syn_replicate {0 | 1};

In a Verilog file:

object /* synthesis syn_replicate = 1 | 0 */;

In a VHDL file:

attribute syn_replicate : boolean;

attribute syn_replicate of object : signal is true|false;

syn_direct_enable

Control the assignment of a clock enable net to the dedicated enable pin of a storage element (flip-flop).

Syntax

In an FDC file:

efine_attribute {object} syn_direct_enable {0|1};

In a Verilog file:

object /* synthesis syn_direct_enable = 0|1 */;

In a VHDL file:

attribute syn_direct_enable of object : objectType is true;

syn_direct_reset

Control the assignment of a net to the dedicated reset pin of a synchronous storage element (flip-flop).

Syntax

In an FDC file:

define_attribute syn_direct_reset {0|1};

In a Verilog file:

object /* synthesis syn_direct_reset = 0|1*/;

In a VHDL file:

attribute syn_direct_reset : boolean;

attribute syn_direct_reset of Object : signal is true|false;

syn_direct_set

Control the assignment of a net to the dedicated set pin of a synchronous storage element (flip-flop).

Syntax

In an FDC file:

define_attribute syn_direct_set {0|1};

In a Verilog file:

object /* synthesis syn_direct_set = 0|1*/;

In a VHDL file:

attribute syn_direct_set : boolean;

attribute syn_direct_set of Object : signal is true|false;

syn_black_box

Specify that a module or component is a black box for synthesis. A black box module has only its interface defined for synthesis, its contents are not accessible and cannot be optimized during synthesis. A module can be a black box whether or not it is empty.

Syntax

In an FDC file:

define_attribute { object }{syn_black_box}{1}

In a Verilog file:

object /* synthesis syn_black_box */ ;

In a VHDL file:

attribute syn_black_box of object : objectType is true;

syn_maxfan

Overrides the default (global) fanout guide for an individual input port, net, or register output.

Syntax

In an FDC file:

define_attribute {object} syn_maxfan {integer}

In a Verilog file:

object /* synthesis syn_maxfan = "value" */;

In a VHDL file:

attribute syn_maxfan of object : objectType is "value";

syn_pipeline

Specify that registers that are outputs of multipliers can be moved to improve timing.

Syntax

In an FDC file:

define_attribute { register } syn_pipeline {0|1}

In a Verilog file:

object /* synthesis syn_pipeline = {1|0} */ ;

In VHDL file:

attribute syn_pipeline of object : objectType is {true|false};

syn_probe

Inserts probe points for testing and debugging the internal signals of a design.

Syntax

In an FDC file:

define_attribute {n:netName} syn_probe{probePortname|1|0}

In a Verilog file:

object /* synthesis syn_probe = "string" | 1 | 0 */;

In a VHDL file:

attribute syn_probe of object : signal is "string" | 1 | 0;

syn_useenables

Controls the use of clock-enable registers within a design.

Syntax

In an FDC file:

define attribute {register|signal} syn_useenables {0|1}

In a Verilog file:

object /* synthesis syn_useenables = "0|1" */;

In a VHDL file:

attribute syn_useenables of object : objectType is "true|false";

syn_netlist_hierarchy

Determine if the generated netlist is to be hierarchical or flat.

Syntax

In an FDC file:

define_global_attribute syn_netlist_hierarchy {0 | 1}

In a Verilog file:

object /* synthesis syn_netlist_hierarchy = 0 | 1 */;

In a VHDL file:

attribute syn_netlist_hierarchy of object : objectType is true | false;

Appendix B Design Example

Take the user design demo.v, for instance. Refer to the following use of Gowin YunYuan Software:

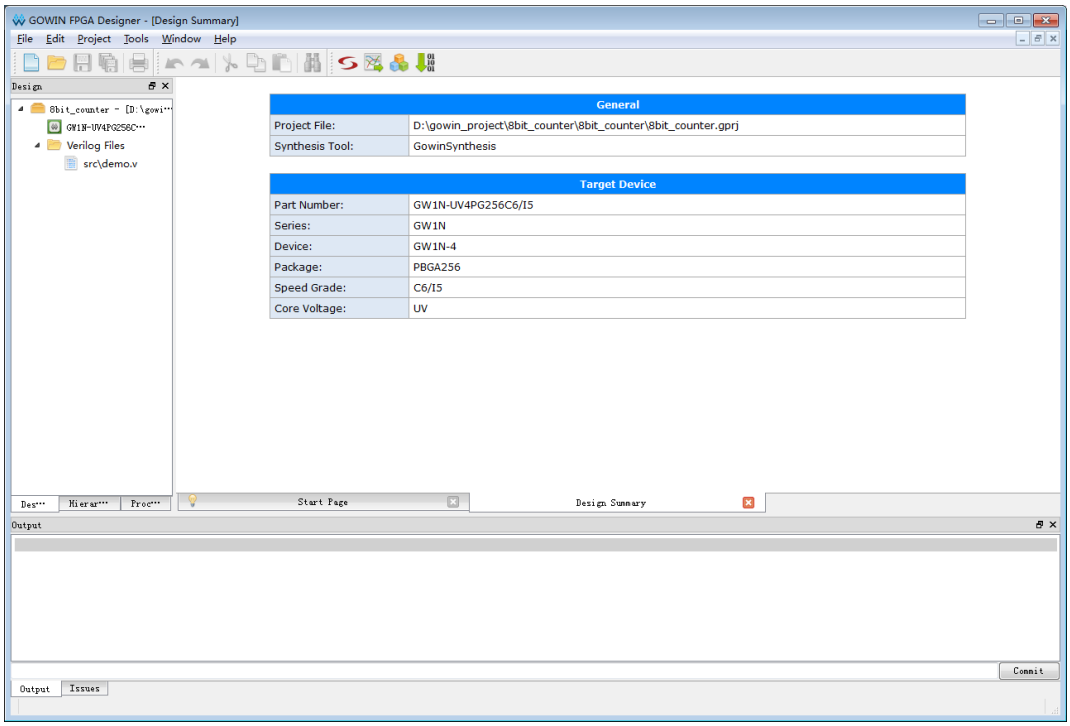
```
module demo (clk_50M, rst_n,led);
input clk_50M;
input   rst_n;
output[3:0] led;
reg[3:0]      led;
reg[24:0]   cnt;
reg        clk_led;

always@(posedge clk_50M or negedge rst_n) begin
  if (!rst_n) begin
       clk_led   <= 1'b0;
       cnt  <= 25'd0;
  end
  else begin
    if (cnt == 25'd2499_9999) begin
          clk_led   <= ~clk_led;
          cnt  <= 25'd0;
    end
    else begin
      cnt  <= cnt + 25'd1;
    end
  end
end
```

```
always@(posedge clk_led or negedge rst_n) begin
  if(!rst_n) begin
        led  <=  4'h1;
  end
  else begin
        led  <=  {led[2:0],led[3]};
  end
end
endmodule
```

B.1 Create a Project

Refer to 5.1Create a New Project and 5.2Open an Existing Project. Open YunYuan software, create a project and add demo.v to the project, and configure design parameters, as shown in Figure B-0-1.

Figure B-0-1 Gowin YunYuan IDE

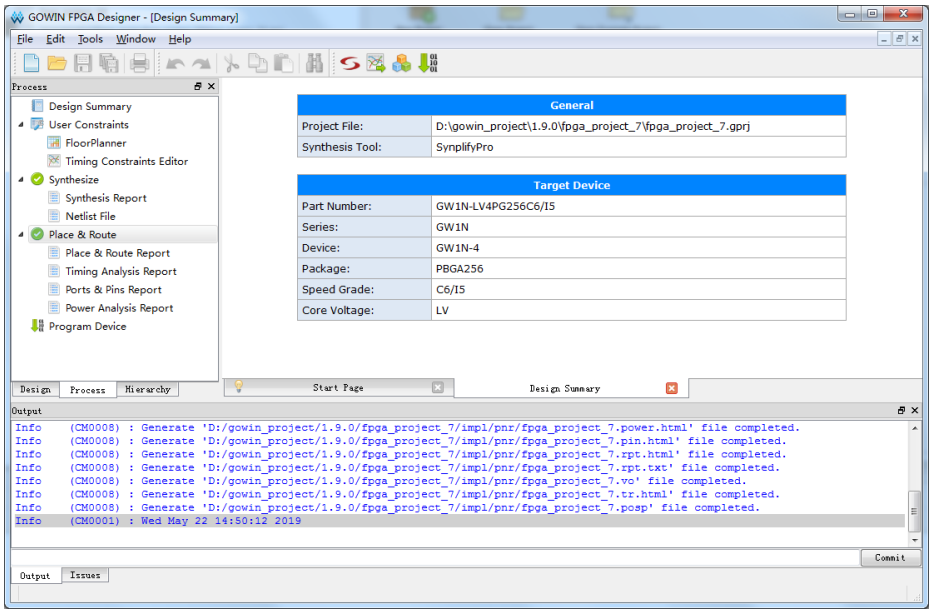


B.2 Implement a Project

See the instructions presented below to implement a project:

1. In Process View, double click "Synthesize" or right-click and select "Run" to synthesize your design;
2. After synthesis, double click "Place & Route" or right-click and select "Run" for logic netlist placement and routing and bitstream file generation, as shown in Figure B-0-2.

Figure B-0-2 Implement a Project



B.3 Download Bitstream

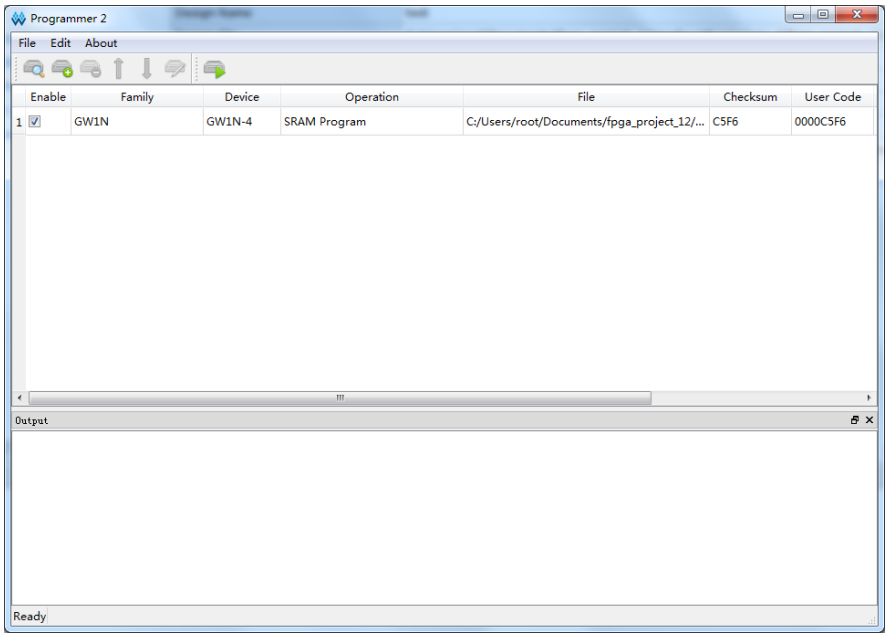
Refer to the following steps to download bitstream:

1. After running placement and routing, double click "Program Device" or right-click "Run" in the "Process" view to open the Gowin Programmer, as shown in Figure B-0-3. The Gowin Programmer will automatically load bitstream files to the downloader.
2. Click "  " to download bitstream.

Note!

- You can also use the two methods described below to download bitstream files:
- Use short cut F5.

Figure B-0-3 Downloader View



Appendix C TcL Command Description

1.9.1 IDE commands include two types: projects management related commands and process execution commands.

C.1 Start Command Line

C.1.1 gw_sh.exe

Syntax

Command: Under the installation directory \x.x\IDE\bin\gw_sh.exe

Parameter: None

[script file]

[-help]

Parameter is null: Enter the command line console mode directly;

script file: Execute a specified script file;

-help: Print help information

Application Example:

```
#Start command line mode
gw_sh
  #Execute script file
gw_sh.exe script_file
#Print help information
gw_sh.exe –help
```

C.2 Project Management Command

C.2.1 set_option

Syntax

Command: set_option

Parameter: [-out_dir <working dir>]

<-device <gowin device>>

[-pn <gowin part number>]
[-prj_name <project name>]
[-synplify <file>]
[-synthesis_tool <synthesis tool>]

Note!

[ ] means it is optional

- **-out_dir**: set the working home directory. Working dir is a given absolute or relative path.The default is the current run directory.
- **-device**: set device
- **-pn**: set part number.Gowin part number is the pn value.
- **-prj_name**: set the project name. The default is gowin.
- **-synplify**: set the full path of synplify executable file. The default is synplify_pro under relative path. Users can define it by themselves.
- **-synthesis_tool**: set the source files synthesis tool. Synthesisi tool only supports "synplify_pro" and "gowinsynthesis". The default is synplify_pro.

Application Example:

```
#Set working home directory to relative directory. "./test " is the current running directory by default.
set_option –out_dir ./test
#Set project device
set_option -device GW1N-4-LQFP144-6
#Set part number
set_option -pn GW1N-LV4LQ144C5/I4
#Set project name
set_option -prj_name dsp_project
#Set the full path of synplify executable file
set_option -synplify /home/test/ synplify_pro
#Set the source files synthesis tool
set_option -synthesis_tool synplify_pro
```

C.2.2 add_file

Syntax

Command: add_file

Parameters: [-hdl< file>]
[-vm< file>]
[-cst <file>]
[-sdc<file>]
[-cfg<file>]
[-gpa<file>]
[-gsc<file>]
[-fdc< file>]
[-gao<file>]

Note!

[ ] means it is optional

-hdl< file>: Add full path HDL file
-vm< file>: Add full path netlist file
-cst <file>: Add full path physical constraints file
-sdc<file>: Add full path timing constraints file
-cfg<file>: Add full path device.cfg file
-gpa<file>: Add full path power analysis configuration file
-gsc<file>: Add full path gowinsynthesis constraints file
-fdc< file>: Add full path synplify_pro constraints file
-gao<file>: Add full path gao file

Application Example

```
#Add HDL design file
add_file -hdl /user/Desker/test.vhdl
#Add cst constraints file
add_file -cst /user/Desker/test.cst
```

Add other types of files, of which usage is similar to it.

C.2.3 rm_file

Syntax

Command: rm_file
Parameter: < file>
< file> : Remove the design file with the specified path. File is required, representing the specified full path file This command does not delete disk files and supports relative and absolute paths.

Application Example

```
#Remove physical constraints file
rm_file /user/Desker/test.cst
```

C.2.4 load_script

Grammar

Command: load_script
Parameter: < file>
< file> : file is the script file to load the run, and the content is the supported script command.

Application Example

```
#Run script file
load_script /user/Desker/script.log
#The content of script.log is as the following:
set_option -device GW1N-4-LQFP144-5
set_option -pn GW1N-LV4LQ144C5/I4
set_option -prj_name dsp_project
set_option -synthesis_tool synplify_pro
add_file -hdl /home/test/top.v
```

C.2.5 export_script

Syntax

Command: export_script
Parameter: < file>
< file> : file is the specified full path file exported, including the file name.If the path does not exist, it needs to create

Application Example

#Export project information
export_script /user/Desker/log

C.3 Process Execution Command

C.3.1 run_synthesis

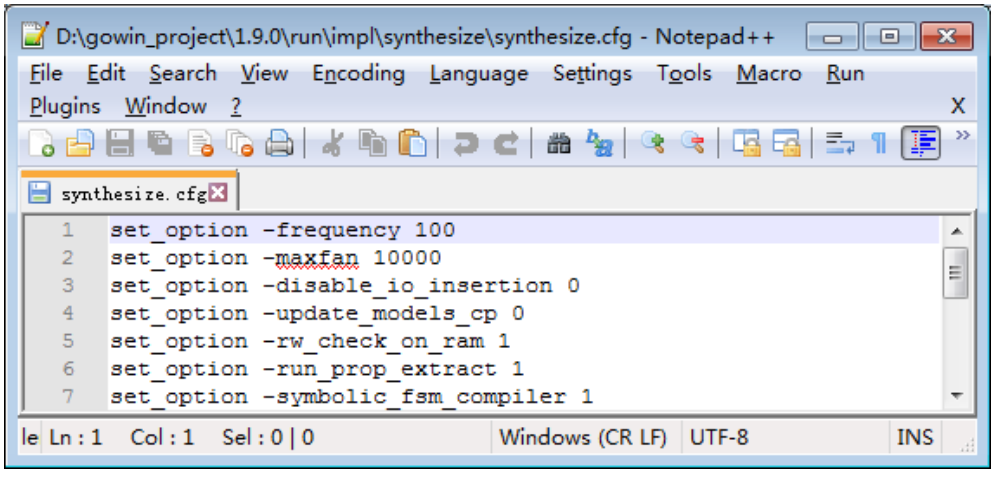
Syntax

Command: run_synthesis
Parameter: [-opt <file>]

Note!

[ ] means it is optional
-opt <file>: File is the specified customized synplify_pro or gowinsynthesis option file. As shown in Figure C-, each command, option, and parameter should have an exclusive line. When the file is specified, it is used for synthesis, and if not specified in GUI mode, the default option file is used.Please refer to the synplify_pro help manual for the command and syntax supported by synplify_pro.

Figure C-0-1 synplify_pro Option File



Application Example

#Execute synthesis using default options
run_synthesis
Use the option files to synthesize, with a frequency of 100 and the maximum fanout of 1000
run_synthesis -opt synthesize.cfg
#The content of synthesize.cfg is as the following:

```
set_option -frequency 100
set_option –maxfan 1000
```

C.3.2 run_pnr

Syntax

Command: run_pnr

Parameters: [-opt <file>]

[-tt]

[-ibs]

[-oc]

[-posp]

[-o]

[-timing]

[-warning_all]

[-reg_not_in_iob]

[-sdf]

[-init_all]

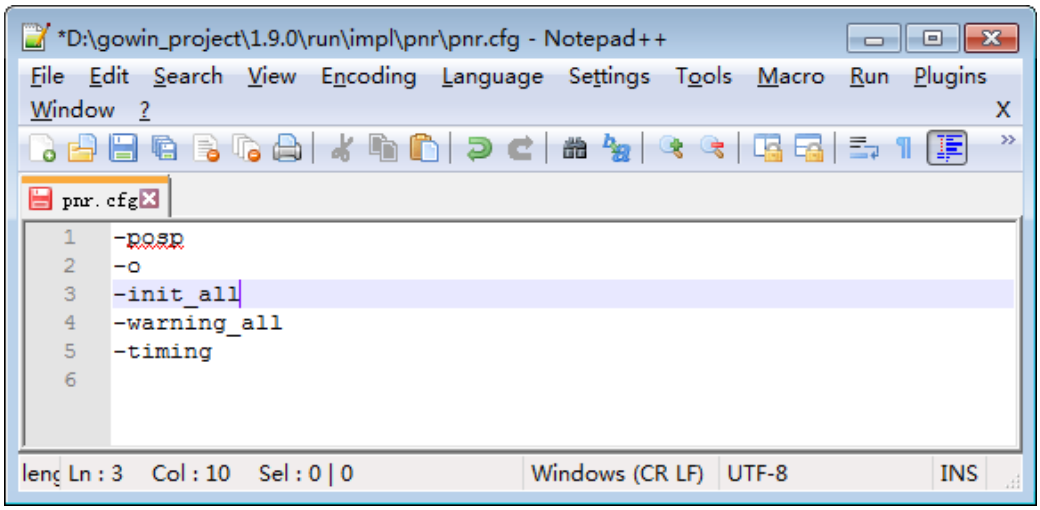
Note!

[ ] means it is optional

-opt <file> : file is the specified customized gowin option file, as shown in Figure C-0-2, and each option should have an exclusive line. When the file is specified, it is used for place & route, and the default option file is used in GUI mode if not specified.

-tt: generate timing report, TXT format, suffix. Tr.
-ibs: generate ibs file, suffix. Ibs.
-oc: generate the actual constraints file, suffix.io.cst.
-posp: generate posp file used by floorplanner, suffix. Posp.
-o: generate vo file, suffix. vo.
-timing: timing driver.
-warning_all: open all warnings.
-reg_not_in_iob: disable placing DFF on IOblock.
-sdf: generate standard delay format files.
-init_all: increase the default initial value for the module

Figure C-0-2 pnr Option File



Application Example

#Execute place & route, generate timing report and posp files in txt format.

run_ pnr -opt pnr.cfg

#The content of pnr.cfg is as following:

-posp

-tt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