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Synplify Pro® for GoWin Release Notes

Version P-2019.09G Beta 2, January 2020

Release Note Topics

About this Release

This P-2019.09G Beta 2 release includes software improvements and enhancements for the Synplify Pro® for GoWin product. Synopsys recommends that everyone download this version to obtain the latest software improvements.

Feature and Enhancement Highlights

The following table summarizes the features and enhancements included in the release.

Feature	Description
Features in the P-2019.09G Beta 2 Release	
Inference support for Block RAM primitives	SDPB, SDPX9B, DPB, DPX9B
VHDL 2019 Support	VHDL 2019 supports the following features: • Conditional analysis of the VHDL code, using the VHDL 2019 language updates (VHDL 2019 LRM, section 24.2). The keywords supported are ‘if, ‘else, ‘elsif, and ‘end. • Inferring constraints from initial values for signals and variables. • Initial values with conditional expressions. For details, see VHDL 2019 Support, on page 3.
Features in the P-2019.03G-1 Beta 1 Release	
New Features	• Instantiation support for Block RAM primitives SDPB, SDPX9B, DPB and DPX9B • Support for Block ROM primitives pROM and pROMX9 • Changes in DSP Resource Management support for GW1N* and GW2A* devices. Now, DSP Resource Management depends on the resource count of individual DSP primitives, not on the total DSP resource count in a device.
Features in the P-2019.03G Release	
DSP Resource Management Support	DSP resource management is now supported for GoWin technologies.

Feature and Enhancement Descriptions

This section explains the features.

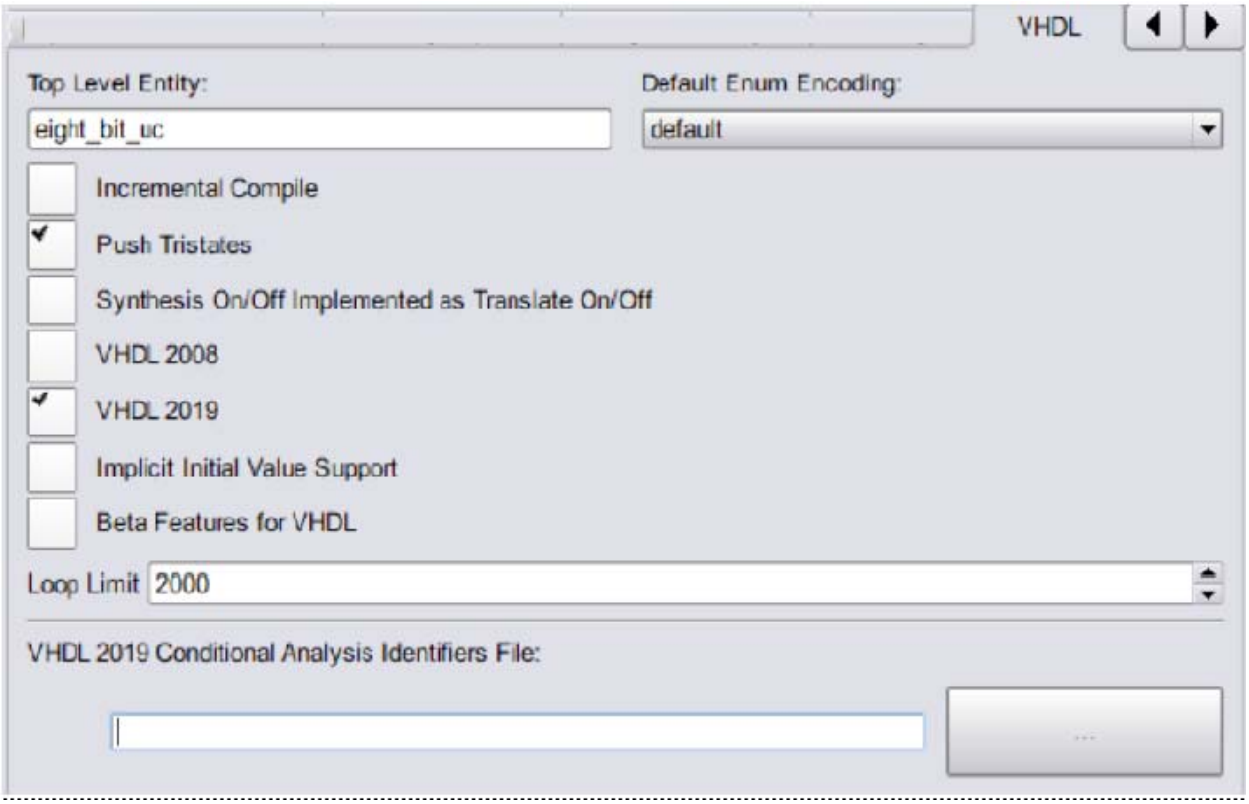
VHDL 2019 Support

VHDL 2019 supports the following features.

VHDL 2019 Conditional Analysis

This section describes how to implement VHDL 2019 conditional analysis identifiers and values:

1. Open the Implementation Options dialog box and select the VHDL tab.
2. Select the VHDL 2019 option to specify VHDL analysis.



3. Use the VHDL 2019 Conditional Analysis Identifiers File text box to set the file containing user-provided identifier/string pairs.
   - The format is one identifier and one value per line.
   - The values must be strings, enclosed in quotes. An example of lines from a file is given below:

```
VHDL_VERSION "2019"
TOOL_TYPE "SYNTHESIS"
DEBUG_LEVEL "2"
```

The VHDL 2019 LRM includes pre-defined identifiers:

```
VHDL_VERSION <value>
TOOL_TYPE <value>
TOOL_VENDOR <value>
TOOL_NAME <value>
TOOL_EDITION <value>
TOOL_VERSION <value>
```

The <*value*> for these pre-defined identifiers depends on the version of the Synplify tool used. Override these pre-defined identifiers values by providing a file (VHDL 2019 Conditional Analysis Identifiers file) containing the identifier/value pairs.

For example, the values from a Synplify project log file for the message CL324 are given below.

@N:CL324 : | Built-in conditional analysis identifier 'vhdl_version' has value "2019"
@N:CL324 : | Built-in conditional analysis identifier 'tool_type' has value "SYNTHESIS"
@N:CL324 : | Built-in conditional analysis identifier 'tool_vendor' has value "SYNOPSYS"
@N:CL324 : | Built-in conditional analysis identifier 'tool_name' has value "FPGA_COMPILER”
@N:CL324 : | Built-in conditional analysis identifier 'tool_edition' has value "SYNPLIFY"

Inferring constraints from initial values for signals and variables

In VHDL 2019, constraints are automatically inferred from the initialization expression.

Example: Subtype of the product is determined from the initial value expression.

```
variable product: sfixed := in1 * in2;
```

Initial values with conditional expressions

The when-else VHDL 2019 constructs can be correctly recognized and processed by the compiler.

Example: Use of when-else construct in initial value expression.

```
variable zvar: signed(3 downto 0) := in1 when ival > 3
else in2 when ival=3
else in3
```

Recommended Versions of Compatible Tools

The FPGA design tool is tested with specific versions of compatible Synopsys tools.

Compatible Version for Synopsys Tools

The following table lists the recommended version of VCS:

Tool	Recommended Version
VCS®	O-2018.09

Platforms

The software is supported on the platforms listed below:

Windows[1]	• Windows 10 Professional or Enterprise (64-bit) • Windows 8.1 Professional or Enterprise (64-bit) • Windows 7 Professional or Enterprise (64-bit) • Windows Server 2016 (64-bit) • Windows Server 2012 R2 (64-bit) • Windows Server 2008 R2 (64-bit)
Linux	All Linux platforms require 32-bit compatible libraries. • CentOS 6.6 or later/7.1 or later (64-bit) • Red Hat Enterprise Linux 6.6 or later/7.1 or later (64-bit) • SUSE Linux Enterprise 11-SP4/12 or later (64-bit)[2]

1. This is the final release that supports the Windows 8.1 platform.
2. The final release supporting SUSE Linux Enterprise 11-SP4 is September 2019.

Documentation

The following product documents are included with the Synopsys FPGA design tool. Documents can be accessed through the online help (HTML) and as PDF documents.

Document	Access
User Guide	Online help, PDF
Reference Manual	Online help, PDF
Attribute Reference Manual	Online help, PDF
Command Reference Manual	Online help, PDF
Language Support Reference Manual	Online help, PDF
Messages Reference Manual	Online help

Known Problems and Solutions

The following problems apply to supported features in the Synplify Pro tool.

Windows Certificate Installer Message

A Synopsys Common Licensing (SCL) change was issued by Synopsys in December 2018, that contained Tamper Resistant Licensing (TRL) cryptography. This change was implemented as part of the ongoing process of enhancing the security of the Synopsys software. The Installer checks if the required certificates are installed and issues a message if an update is needed.

Solution: Contact Synopsys support for the licensing certificate.

Software Does Not Open After Installation

If your software does not open after installation, check if you need to update your Synopsys Common Licensing (SCL) certificates. A SCL change was issued by Synopsys in December 2018, that contained TRL cryptography. This change was implemented as part of the ongoing process of enhancing the security of the Synopsys software.

Solution: To find out if you are missing any required certificates, go to the /bin directory of your installation and run the following:

```
whatscl.exe  --check-cert
```

If certificates are listed as missing, contact Synopsys support to update the required licensing certificates.

Change in Behavior for Sequential Optimizations

In the N-2018.03-SP1 release, the default behavior changed in RAM implementation. If sequential optimizations are disabled (set_option no_sequential_opt 1), you may see Block RAM utilization increase (LUT utilization may decrease) in area estimation and in FPGA synthesis.

Default Behavior:

Version	RAMs with read address registered	RAMs with output registered
N-2018.03 or older	Block RAM	LUT RAM (select RAM)
N-2018.03-SP1 or later	Block RAM	Block RAM

Solution: A new option has been added to control the behavior of Block RAM packing when disable sequential optimization is ON.

```
set_option no_sequential_opt_bram_mapping inreg|both
```

inreg - Read address registered RAMs will be packed to Block RAMs (prior default behavior).

both - Default. Both read address registered and output registered RAMs will be packed to Block RAMs.

The following is a list of what is impacted by disabling sequential optimization. Use `no_sequential_opt 1` understanding its impact.

- If you are disabling sequential optimizations with GSV to obtain better naming correlation, you may not see RAM output registers that were seen in the GSV database in prior versions.
- No gated clock conversion and no ICG latch removal
- May increase area
- Limited design performance
- May increase congestion

False Flagging of Product Executables as Malware

On Microsoft Windows, some endpoint protection systems could flag executables as similar to malware threats. These are false positives, as Synopsys thoroughly scans all released files.

Solution: If your endpoint system blocks a Synopsys file, white-list it so that it is not flagged. Also, open a CASE so that Synopsys can investigate.

Adobe Reader Error About Opening PDF Files (Linux)

Random links in the document PDFs on the Linux platform do not work. Adobe Reader generates an error message about not being able to find the appropriate PDF file. This does not happen on Windows platforms.

Solution: This is a problem with Adobe Reader on Linux. Work around it by first opening all the PDFs, and then trying the link again.

GUI Processing Can Fail on Windows 7 for the Synthesis Tool

The synthesis tool GUI might intermittently stop responding on Windows 7.

Solution: To resolve this issue, apply the hotfix from Microsoft by going to suppport.microsoft.com/kb/2718841/.

Limitations

The following limitations apply to supported features in Synplify Pro.

Fault Injection Feature for Mixed HDL Designs

When using fault injection techniques for mixed HDL designs, RTL instrumentation is not supported. Only SRS instrumentation is supported for mixed HDL designs.

Page Could Not Be Found Message When Invoking Online Help

When online help is first invoked, it creates a cached version of the compiled help file in a local hierarchy to allow you to save preferences, bookmarks, and full-text search information. This cached version records the path to the installed version. If the same product version is subsequently re-installed in a new directory, invoking online help displays a message, "*The page could not be found*," because the cached version does not recognize the path to the re-installed product.

Solution: Go to the platform-specific directory and clear the cached help files:

Windows:
C:\Users*username*\AppData\Local\assistant\Synopsys*product*

Linux:
~/.local/share/data/assistant/Synopsys/Synplify/

- Delete any/all directories named “online*” from the cache directory.
- Restart help. This creates a new cache and correctly displays the online help.

Online Search Does Not Handle Hyphens as Expected

If the search term includes a hyphen (for example, *byte-enable*), online help does not produce the search hits you expect, because it searches for *byte* and *enable*. This limitation does not affect underscores.

It is limited to online help search and does not affect search in PDF documents.

Solution: Here are some workarounds:

- Basic Search—Use the \ character before the hyphen to escape the hyphen
- Try the index
- Basic Search—Try using the * wildcard
- Basic Search, and Advanced Search with exact term: Try the term with a space in place of the hyphen

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save the project file from the synthesis GUI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project GUI.