Gowin Power Analyzer

User Guide

SUG282-1.7E,05/17/2019

Disclaimer

Revision History

Date	Version	Description
01/30/2018	1.2E	Initial version published.
08/16/2018	1.3E	● The value range of V_{CC} and V_{CCX} updated; ● Interface screenshots updated.
10/26/2018	1.4E	● GW1NZ-1 and GW1NSR-2C supported.
11/15/2018	1.5E	● GW1NSR-2 supported; ● GW1N-6ES, GW1N-9ES and GW1NR-9ES removed;
02/25/2019	1.6E	● The working voltage configuration updated ● VCD File configuration supported ● Specified IO slew rate configuration removed
05/17/2019	1.7E	GW1N-1S supported.

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1 About This Guide

1.1 Purpose

This guide describes how to use the Gowin Power Analyzer. It provides a basic introduction to the tools that are available and the analysis of the power consumption report. It is designed to help users estimate and analyze power consumption more easily. The software screenshots and supported products listed in this guide, please refer to 1.9.1 Beta version. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Supported Products

The information presented in this guide applies to the following products:

1. GW1N series of FPGA products: GW1N-1, GW1N-2, GW1N-2B, GW1N-4, GW1N-4B, GW1N-6, GW1N-9, GW1N-1S;
2. GW1NR series of FPGA products: GW1NR-4, GW1NR-4B, GW1NR-9;
3. GW1NS series of FPGA products: GW1NS-2, GW1NS-2C;
4. GW2A series of FPGA products: GW2A-18, GW2A-55;
5. GW2AR series of FPGA products: GW2AR-18;
6. GW1NZ series of FPGA products: GW1NZ-1;
7. GW1NSR series of FPGA products: GW1NSR-2C, GW1NSR-2.

1.3 Related Documents

The user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

Gowin YunYuan Software User Guide

1.4 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology that is used in this guide.

Table 1-1 Abbreviations and Terminologies

Terminology and Abbreviations	Full Name
FPGA	Field Programmable Gate Array
JTAG	Joint Test Action Group
IO	Input/Output
GPA	Gowin Power Analyzer
GPC	Gowin Power Calcaulator

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail:support@gowinsemi.com

+Tel: +86 755 8262 0391

2 Introduction

The GPA tool was independently researched and developed by Gowin. It was designed to analyze FPGA power consumption; as such, it can help users evaluate system power consumption as accurately as possible and improve the performance and reliability of Gowin devices.

FPGA power consumption includes static power consumption and dynamic power consumption.

- Static power consumption mainly refers to the power consumption caused by leakage current with no activity in the device. It is determined by the structure, package, process, voltage, and working environment of the chip.
- Dynamic power consumption refers to the power consumption during normal operation, which is determined by the user-designed logic circuit and the characteristics of the circuit activity.

2.1 Principle

Users set the chip type, working environment, resource utilization, and signal toggle rate parameters according to their requirements. The arrangement of these parameters impact chip power consumption. The GPA automatically estimates the customized power consumption and produces a power consumption analysis report according to the user-input parameters.

2.2 Features

The GPA offers the following features:

- Supports setting environment temperature, airflow, heat sink performance, and development board heat dissipation mode that affect static power consumption;
- Supports setting the customized thermal impedance parameters;
- Supports specifying the toggle rate of I/O and the net signal. According to the waveform files generated by the simulation, calculates signal toggle rate by adopting default toggle rate and non-vector estimation, etc.;

- Enables/disables working clock, B-SRAM, I/O, and DFF;
- The generated power consumption analysis report supports the analysis of the power consumption in terms of block type, hierarchy relation, clock domain, etc.
- Supports GW1N using BG to reduce power consumption.

3 GPA

The GPA helps users accurately estimate the power consumption associated with a given design by configuring chip type, working environment factors, working voltage, signal toggle rate in design file, and clock enable.

3.1 Start the GPA

Before starting the GPA, you need to create or load the Config File (.gpa).

3.1.1 Create/Load Config File

Create Config File

Follow the steps outlined below to create a standard mode GAO:

1. In the "Design" view, right-click and select "New File...".
   The "New" dialog box pops up;
2. Create"GPA Config File", as shown in Figure 3-1;
3. Click "OK". The "New GPA Config File" dialog box will open, as shown in Figure 3-2;
4. Enter Config File name and select to create path, then click "OK". See GPA Config File in"Design > GPA Config Files".

Figure 3-1 Create Config File

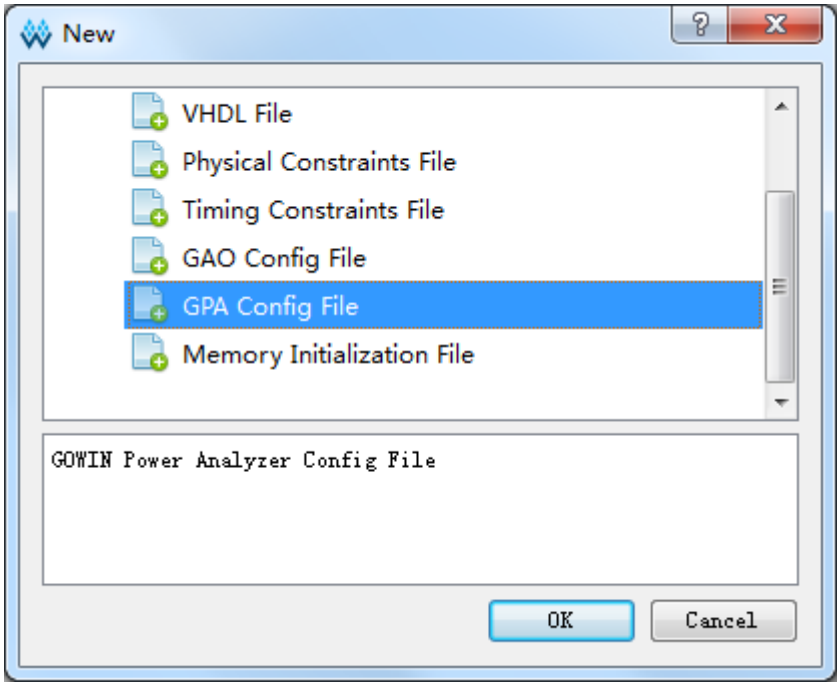
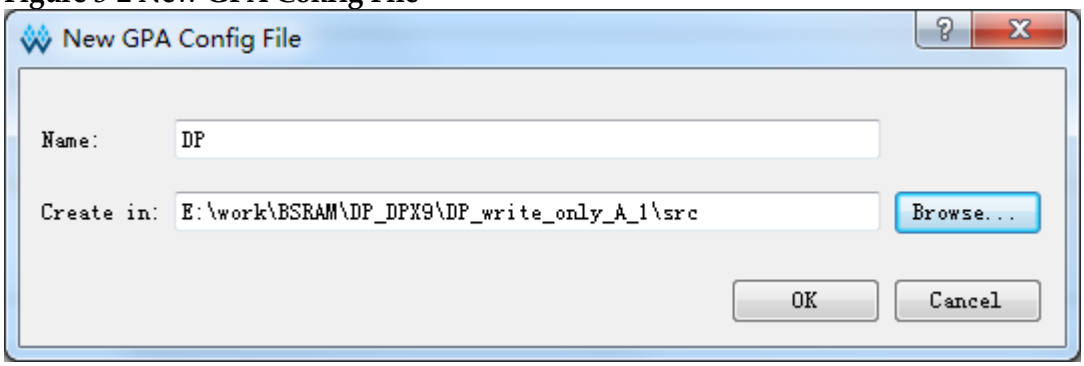


Figure 3-2 New GPA Config File

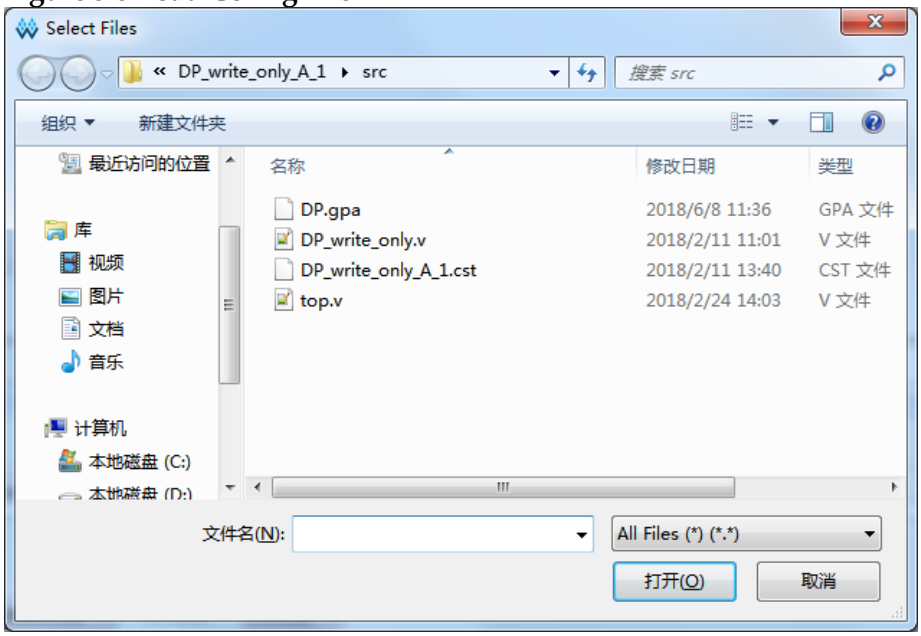


Add Config File

Follow the steps outlined below to create a standard mode GAO:

1. In "Design", right-click and select ″Add Files...″, The ″Select Files″ window will open;
2. Select the loaded existing Config File (.gpa), as shown in Figure 3-3, click"Open″. See"Design > gpa Config Files"for GPA Config File.

Figure 3-3 Load Config File

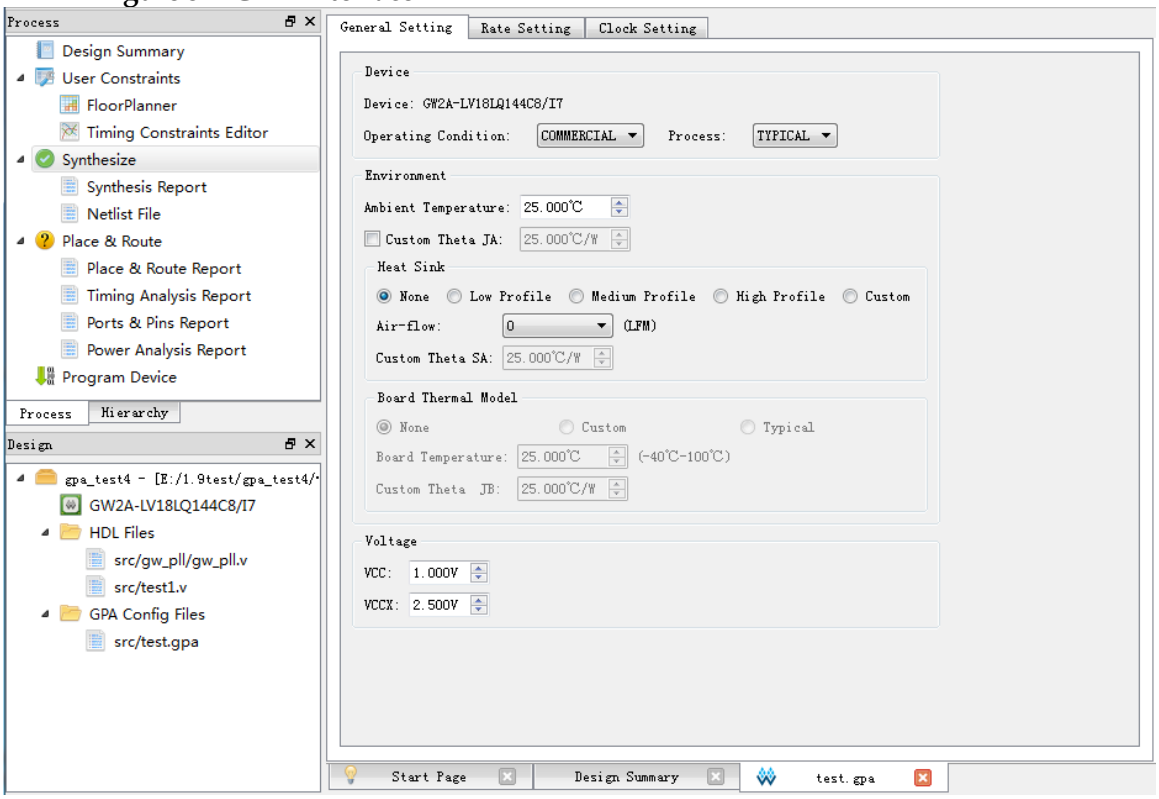


3.1.2 Start the GPA

Double-click the Config File (.gpa) in "Design" window, and the configuration windowpops up, and GPA starts, as shown in Figure 3-4.

The "GPC View" Configuration window includes"General Setting" (used for configuring working conditions for chip), "Rate Setting" (used for configuring signal transition rate) and "Clock Setting" (used for configuring Clock enable).

Figure 3-4 GPA Interface



Note!

- GPA supports power consumption analysis for netlists after synthesizing or layout;
- To use RTL, start the tool only after synthesizing;

3.2 Configuration

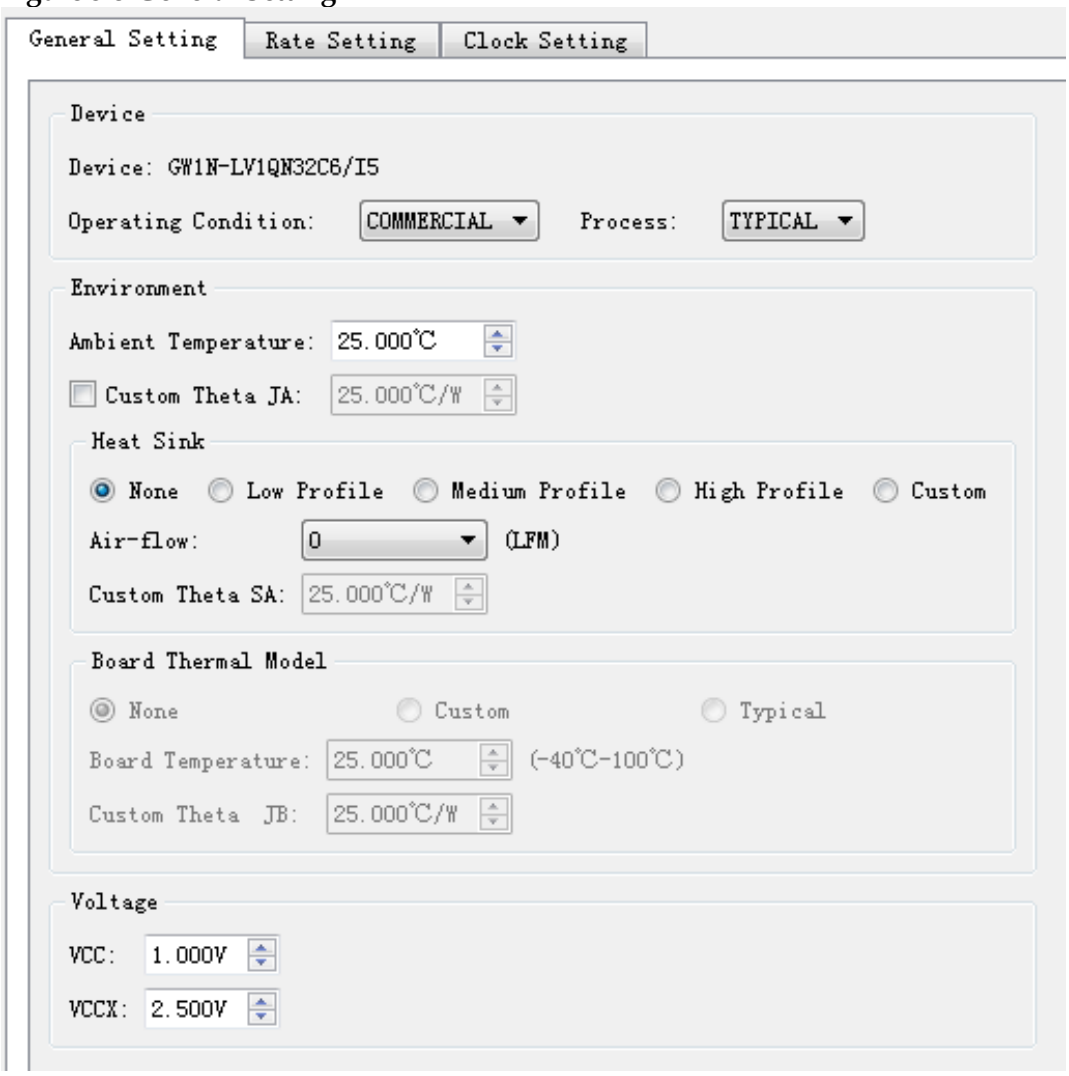
To ensure the accuracy of the power consumption analysis, it is necessary to set the chip working conditions, toggle the rate of the signal in the design file, and enable/disable clock, B-SRAM, I/O, DFF etc. according to the actual design.

3.2.1 Operating conditions

The ″General Setting″ view is mainly used to display the characteristic parameters of the chip, package, speed level and configuring temperature grade, thermal impedance, and voltage.

As shown in Figure 3-5, the "General Setting" view includes “Device” for setting the chip type, “Environment” for setting the chip working conditions, and “Voltage” for setting the chip working voltage.

Figure 3-5 General Setting



Parameter

1. Device

The parameters details are as follows:

- Device: Information on family, device, package, and speed level of chip;
- Operating Condition: The operating condition includes COMMERCIAL and INDUSTRIAL. And the operating condition setting affects the minimum and maximum working temperature of the chip. The min. working temperature of commercial device is 0 ℃, and the max. working temperature is 85 ℃; the min. working temperature of industrial devices is minus 40 ℃, and the max. working temperature is 100 ℃;
- Process The process of the chip is divided into TYPICAL or WORST.

2. Environment

"Environment" is mainly used to set factors related to the environmental temperature, air flow, heat sink, development board, and heat dissipation mode of the chip. Working environment mainly affects static power consumption. Different working environments will affect the FPGA chip temperature and static power consumption of the chip in different ways. Air flow mainly affects the heat dissipation performance of the chip.The heat sink is used for the heat dissipation of the specified chip through the auxiliary device;The circuit board heat dissipation mode is used for the heat dissipation of the specified chip through the board.

Junction temperature is determined by external temperature, chip power consumption, and thermal impedance. Please refer to Appendix A Calculation Principle for Junction Temperature for calculation principle of junction temperature. Details of Environment configuration parameters are as follows:

- Ambient Temperature: environment temperature. The unit is ℃. The range is to from minus 40 ℃ ~ 100 ℃, and the default is 25.000 ℃;
- Custom Theta JA: The user specifies the thermal impedance θ_{JA}between the chip and surrounding environment. The unit is ℃ / W. The range is from 0.001 ℃/W ~ 100 ℃ / W, and the default is 25.000 ℃ / W;
- Heat Sink: Heat Sink contains 5 modes: None, Low Profile, Medium Profile, High Profile and Custom. "None" indicates heat sink is unused, and only thermal impedance θ_{JA}influences junction temperature; Custom indicates that the user specifies the thermal impedance $\theta_{SA}$from the heat sink to the surrounding environment; Low Profile, Medium Profile and High Profile modes represent $\theta_{JA}$is automatically calculated by the power analyzer.
- Air Flow: The unit of measurement is LFM or m/s. The unit displayed in the user interface is LFM. There are four selection modes, including 0LFM, 100LFM (0.5 m/s), 200 LFM (1.0 m/s), 400 LFM (2.0 m/s); The larger the Air Flow is, the smaller the thermal impedance from the shell to the Air is, and the smaller the junction temperature is.
- Custom Theta JA: thermal impedance θ_{SA}between Heat Sink and surrounding environment. The unit is ℃ / W. The range is from

0.001 ℃/W ~ 100 ℃ / W, and the default is 25.000 ℃ / W;

- Board Thermal Model: heat dissipation mode of development board. Thermal impedance model of the development board is the path that dissipating heat from the development board to outside; which includes three modes: None, Custom, and Typical. None means heat dissipation of development board is not to be considered; Custom indicates the user specifies thermal impedance $\theta_{JB}$from device to development board; Typical indicates $\theta_{JB}$is automatically determined by chip package.
- Board Temperature:
- CustomTheta JB: thermal impedance $\theta_{JB}$from junction to board. The user can specify only if selects Custom from Board Thermal Model.

3. Voltage

   Details of parameters are as follows:

   - V_{CC}: Device kernel voltage. The unit is V, and the voltage range of each series device is shown Table 3-1 in detail.

     V_{CCX}: Device auxiliary voltage. The unit is V, and the voltage range of each series device is shown Table 3-1 in detail.

Table 3-1 Recommended range of voltage for each series device

Series	Voltage	V_{CC}: Voltage operation range	V_{CCX}: Voltage operation range
GW1N	LV	1.14V-1.26V	2.375V-2.625V or 3.135V-3.465V
	UV	2.375V-2.625V or 3.135V-3.465V	2.375V-2.625V or 3.135V-3.465V
GW1NR	LV	1.14V-1.26V	2.375V-2.625V or 3.135V-3.465V
	UV	2.375V-2.625V or 3.135V-3.465V	2.375V-2.625V or 3.135V-3.465V
GW1NS	LX	1.14V-1.26V	1.71V-1.89V
	UX	1.14V-1.26V	2.375V-2.625V or 3.135V-3.465V
GW1NSR	LX	1.14V-1.26V	1.71V-1.89V
	UX	1.14V-1.26V	2.375V-2.625V or 3.135V-3.465V
GW1NZ	LV	1.14V-1.26V	1.71V-1.89V or 2.375V-2.625V or 3.135V-3.465V
	ZV	0.855V-0.945V	1.71V-1.89V or 2.375V-2.625V or 3.135V-3.465V
GW2A	LV	0.95V-1.05V	2.375V-2.625V or 3.135V-3.465V
GW2AR	LV	0.95V-1.05V	2.375V-2.625V or 3.135V-3.465V

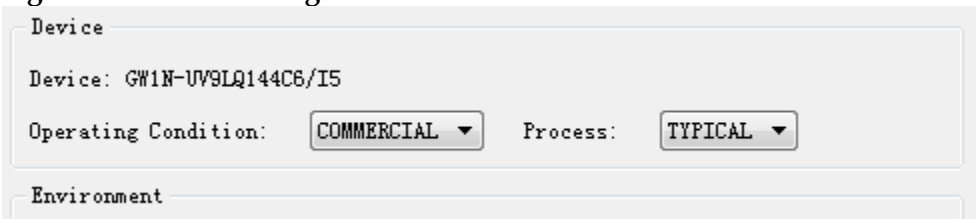
Configure Device

The Device configuration area can display the package information and speed level of the working chip, as well as set the temperature level and process of the chip, as shown in the Figure 3-6.

1. Set Operating Condition:
   Click "Operating Condition" and select COMMERCIAL or INDUSTRIAL in drop-down list;

2. Set Process;
   Click "Process" and select TYPICAL or WORST in the drop-down list.

Figure 3-6 Device Configuration Area



Configure Environment

1. Set ambient temperature.

Set ambient temperature by entering environment temperature in Ambient Temperature, or adding and reducing the temperature value through the upper and lower buttons on the right side of text box or sliding mouse wheel.

2. Set heat impedance if no heat sink in chip.

Thermal impedance θ_{JA}can be specified by the user or determined by package information and air flow in non-radiator mode.

a). Custom Theta JA Check"Custom Theta JA″ and enter the specified thermal impedance value in text box, adding and reducing the thermal impedance values. As shown in Figure 3-7.

Note!

You can also add and reduce the thermal impedance value using the upper and lower buttons on the right side of text box or by sliding mouse wheel.

Figure 3-7 Specify Thermal Impedance θ_{JA}

b). Thermal Impedance θJA is determined by package information and air flow. In the Heat Sink configuration area, click "None" and choose not to use the Heat Sink mode. Click "air-flow" and select

Air flow 0, 100, 200, or 400 from the drop-down list, as shown in Figure 3-8.

Figure 3-8 Package information and air flow determine Thermal impedance θ_{JA}

Note!

- Custom Theta JA has a higher priority than that specified by package information and air flow. If Thermal impedance is specified, Heat Sink and the Board Thermal Model is grayed out and not available;
- If there is no heat sink, Board Thermal Model is not available.

3. If there is heat sink, but does not consider the heat dissipation of the development board, set the thermal impedance.

In heat sink mode, considered the heat dissipation of the development board, thermal impedance θ_{JA}can be specified by user or determined through heat sink mode.

User specifies. User can specify the thermal impedance in following two ways:

a). Check"Custom Theta JA″ and enter the specified thermal impedance value in text box, adding and reducing the thermal impedance values. As shown in Figure 3-7.

Note!

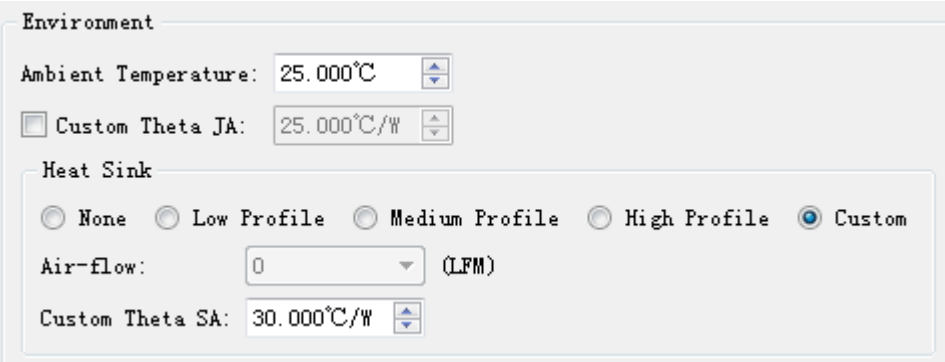
You can also add and reduce the thermal impedance value using the upper and lower buttons on the right side of text box or by sliding mouse wheel.

b). In Heat Sink, click ″Custom″ and enter the specified thermal impedance value θ_{SA}in Custom Theta SA, as shown in Figure 3-9.

Note!

You can also add and reduce the thermal impedance value using the upper and lower buttons on the right side of text box or by sliding mouse wheel.

Figure 3-9 User Specifies Thermal Impedance θ_{SA}



Note!

- Specify θ_{SA}only when Custom Theta JA and Heat Sink are not in Custom mode;
- When specifying thermal impedance θ_{SA}, θ_{SA}contains air flow influence, Air-flow box will be grayed out and not available.

Set heat sink. In "Heat` Sink", click "Low Profile", "Medium Profile" and "High Profile" according to Heat Sink, select the corresponding heat dissipation mode; click air-flow and select air flow 0, 100, 200, or 400 in drop-down list, as shown in Figure 3-8; select″None" in "Board Thermal Model" without regard to heat dissipation condition on development board.

4. Set thermal impedance if a heat sink is configured in chip and considers heat dissipation of development board,.

In heat sink mode, thermal impedance θ_{JA} can be specified by user or determined through heat sink mode according to heat dissipation of development board; Thermal impedance θ_{JB} can be specified by user, or determined through heat dissipation mode.

To specify thermal impedance θ_{JA}, please efer to the method b) specified in article 3 for Parameter Settings.

Setting heat sink mode to determine thermal impedance θ_{JA}, please refer to methods a) and b) specified in article 3 for Parameter Settings.

To specify thermal impedance θ_{JB} in Board Thermal Model, click "Custom" and enter the circuit board temperature of the device in Board Temperature; Enter the specified thermal impedance value θ_{SA} in Custom Theta JB text box, as shown in Figure 3-10.

Note!

You can also add and reduce the temperature value or thermal impedance value of development board by the upper and lower buttons on the right side of text box or by sliding mouse wheel.

Figure 3-10 User specifies thermal impedance θ_{JA}

Note!

Specify Board Thermal Model only if Custom Theta JA is unspecified and Heat Sink is not in None mode.

Set heat dissipation mode of circuit board to determine thermal impedance θ_{JB}. Heat dissipation mode of development board is in Typical mode by clicking "Typical" in Board Thermal Model; enter temperature of development board where device is located in text box, adding and reducing the temperature value or thermal impedance value, and as shown in Figure 3-11.

Figure 3-11 Determining thermal impedance θ_{JB} by setting heat dissipation mode

Note!

- You can also add and reduce the thermal impedance value of development board by the upper and lower buttons on the right side of text box or by sliding mouse wheel.
- If select the thermal impedance θ_{JB} specified by users, Custom Theta JB text box is grayed out and not available.
- Specify Board Thermal Model only if Custom Theta JA is not specified and Heat Sink is not in None mode.

Configure Working Voltage

- Set V_{CC}: enter core voltage directly in V_{CC}, add and reduce the voltage value;

  Note!

  You can also add and reduce voltage value by using the upper and lower buttons on the right side of the text box or by sliding mouse wheel.
- Set V_{CCX}: enter auxiliary voltage directly in V_{CCX}, add and reduce the voltage value;

  Note!

  You can also add and reduce voltage value by using the upper and lower buttons on the right side of the text box or by sliding mouse wheel.

3.2.2 Signal Toggle Rate Setting

Rate Setting is used for configuring signal toggle rate, which can directly set toggle rate of IO or Net, or adopt default toggle rate.

As shown in Figure 3-12, Rate setting windows includes Net Rate, VCD File and Default Rate Setting.

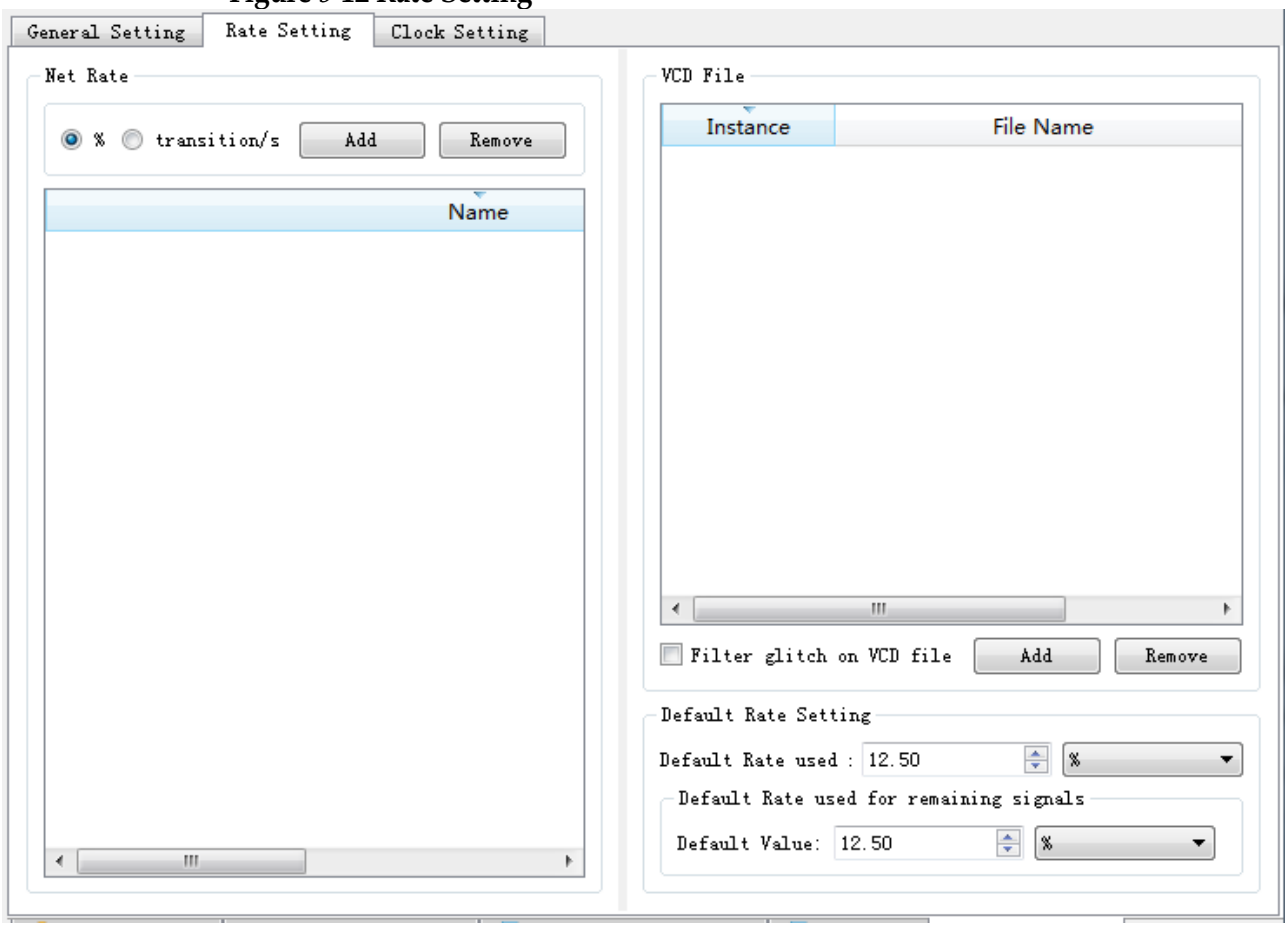
Functions of each configuration are as follows:

- Net Rate is used to configure specified Net toggle rate;
- VCD File is used to load simulation generated waveform files;
- Default Rate Setting is used to configure general Default toggle rate for IO and Net.

Note!

Preferentially select Net and IO toggle rate specified by users, finally select general IO and Net transition by default.

Figure 3-12 Rate Setting

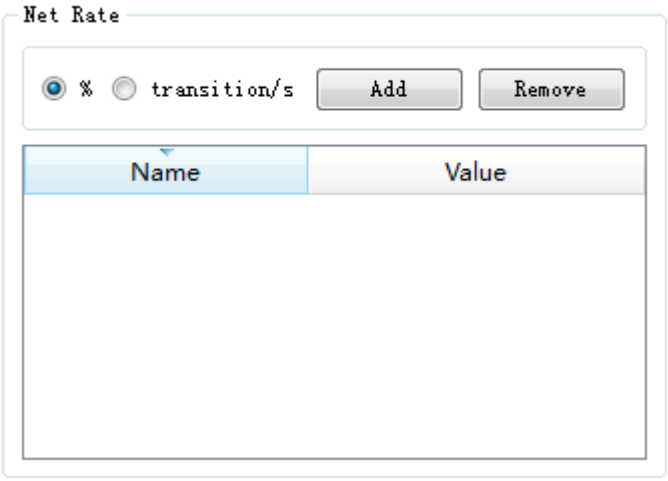


Configure the specified Net toggle rate

Net Rate is used to set Net signal toggle rate specified by users, as shown in Figure 3-13. Net signal toggle rate settings include TOGGLE RATE mode and SIGNAL RATE mode.

Click″%″ to select TOGGLE RATE mode; Or click "transition/s" to select SIGNAL RATE mode.

Figure 3-13 Net Rate



Note!

- TOGGLE RATE mode: Value represents the ratio of signal toggle rate to clock rate, unit: %;
- SIGNAL RATE mode: Value represents signal toggle rate, unit: transition/s.

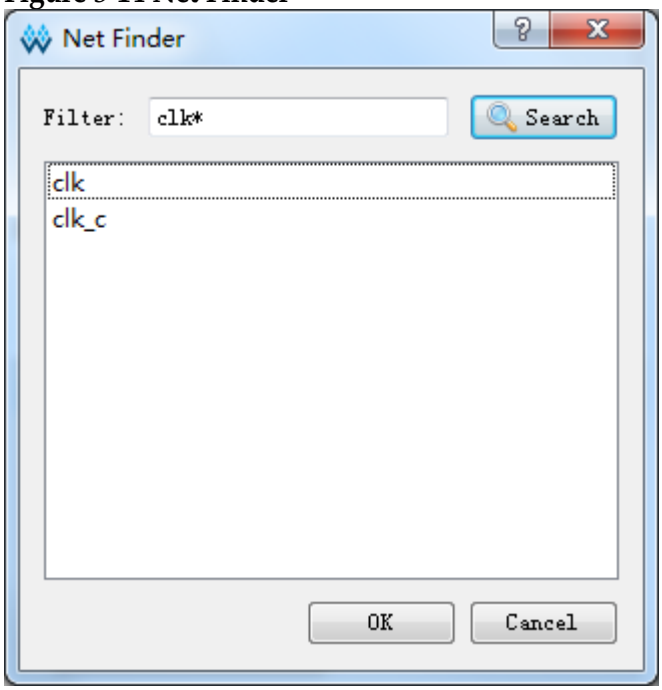
Select Net signal. Follow the steps outlined below to create a standard mode GAO:

1. Click "Add" , "Net Finder" dialog box pops up, as shown in Figure 3-14;
2. Enter Net name in Filter, click ″Search″;
3. Select the specified Net in list;
4. Click ″OK″ to finish selecting Net signal.

Note!

You can also right click in edit zone of table and select "Add" in the pop-up menu.

Figure 3-14 Net Finder

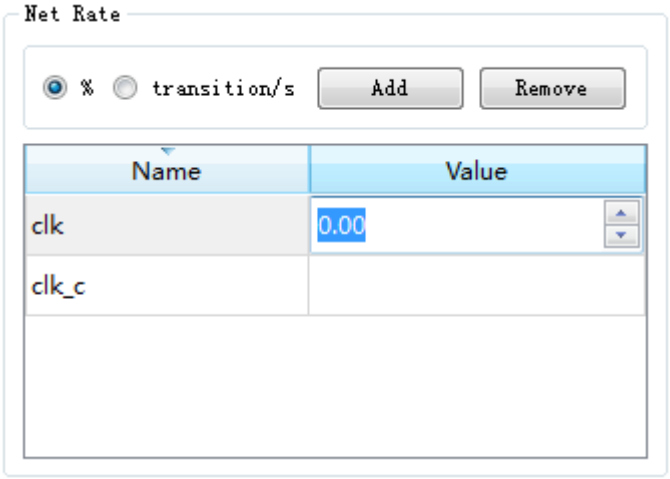


Note!

- "Filter" supports wildcard screening;
- The list supports options of left-click, Shift + left, and Ctrl + left.

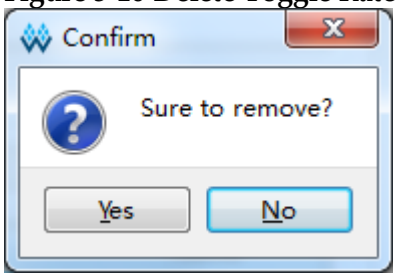
5. See Net signals in Net Rate table, double-click the corresponding Value column and enter signal toggle rate, as shown in Figure 3-15.

Figure 3-15 Set Net toggle Rate



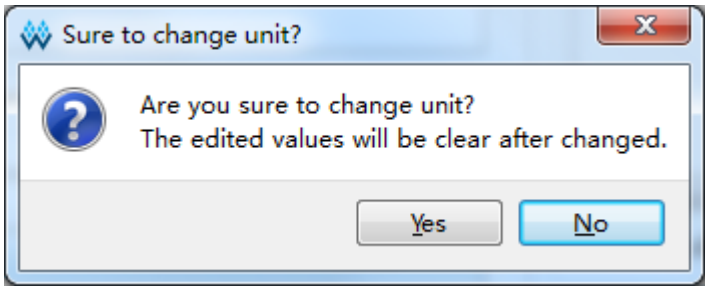
6. Select the row needed to delete in the editing area table, click″Remove″ or right-click to select ″Remove″ in the pop-up menu, and the ″Confim" dialog box will pop up, click ″Yes″ to delete the Net turnover rate setting. As shown in Figure 3-16.

Figure 3-16 Delete Toggle Rate



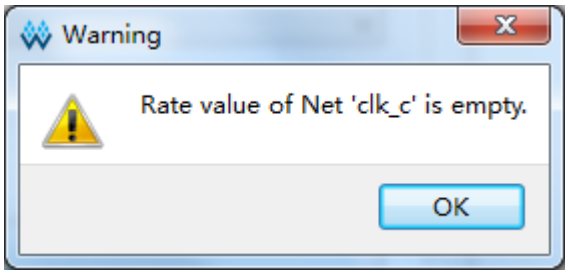
7. For the Net toggle rate that has been set, conversion between TOGGLE RATE and SIGNAL RATE is not supported. If another setting is selected, ″Sure to change the unit″ will pop up to prompt the user that the Net toggle rate that has been set will be removed if set mode is changed, as shown in Figure 3-17.

Figure 3-17 Change Settings



8. For the Net added in table, Value should be set, or else when clicking "save", a "Warning" dialog box will pop up, as shown in Figure 3-18.

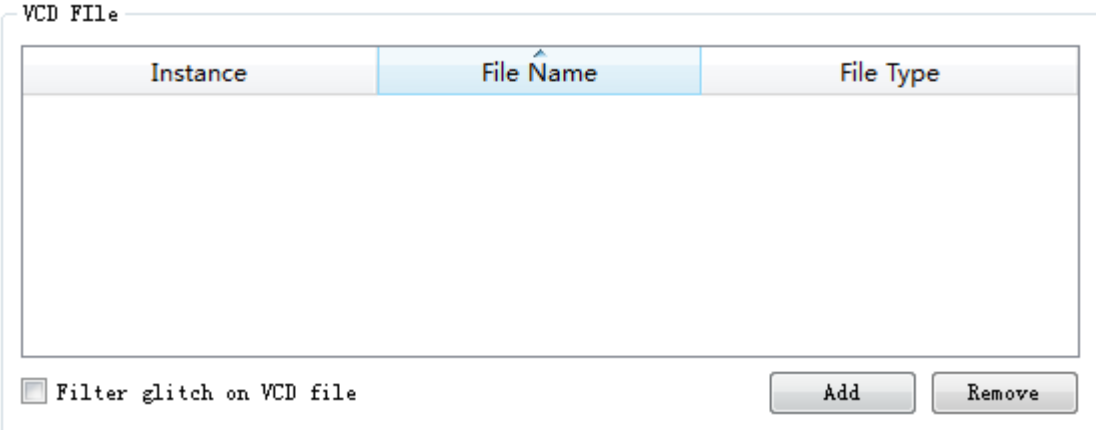
Figure 3-18 Dialog for Empty toggle rate



Load Simulation Waveform File

VCD File is used to load simulation generated waveform files, as shown in Figure 3-19. Waveform files are the basis for calculating IO and NET toggle rates. Two types of waveform files generated by VCS or modelsim simulation tools are supported: VCD (Value Change Dump) and SAIF (Switching Activity Interchange) files.

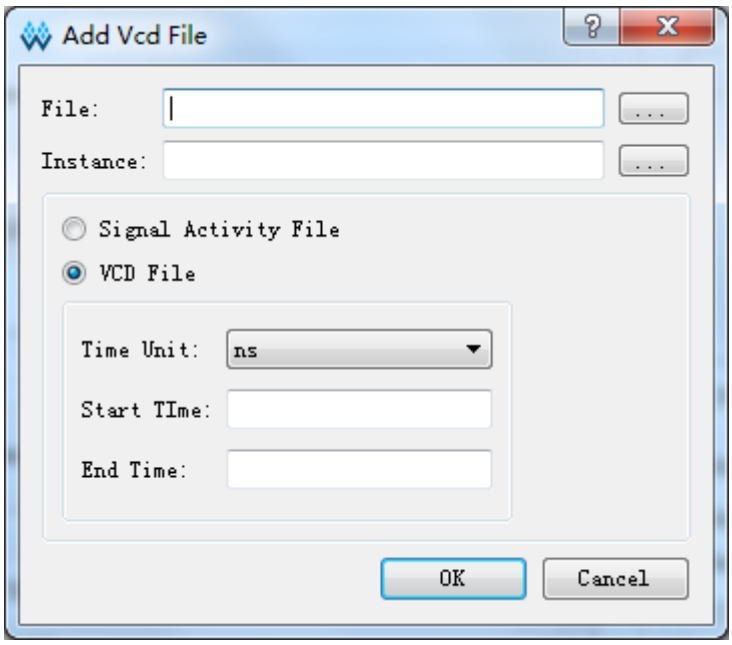
Figure 3-19 VCD File Configuration



The operation steps of loading the simulation waveform files are as follows:

1. Click “Add”，“Add Vcd File” dialog box pops up, as shown in Figure 3-20;

Figure 3-20 Add Vcd File dialog box



Note!

You can also right-click in table and select "Add Input File" in the pop-up menu.

2. Click the ... button on the right of "File", and the "Select VCD File" dialog box pops up, as shown in Figure 3-21; Select the *.vcd or *.saif file to be loaded and click the "OK" button to complete the selection of the waveform file.
3. Click the ... button on the right of "Instance", and the "Select Instance" dialog box pops up, as shown in Figure 3-22. Select the Instance to be loaded, and click the "OK" button.
4. If "File" loads *.saif file, select "Signal Activity File"; If "File" loads *.vcd file, select "VCD File";
5. When "VCD File" is selected, the time configuration is highlighted, and part of the time period in the VCD File can be set as the basis for power analysis. Click the drop-down box at Time Unit and select the Time Unit s, ms, us, ns or ps in the drop-down list, as shown in Figure 3-23. Enter the start Time in the "Start Time" text box and the end time in the "End Time" text box.
6. Click the "OK" button to complete the loading the waveform file. The configured Instance name, waveform File name, and File type are displayed in the VCD File configuration zone.
7. As shown in Figure 3-19, check the check box in front of "Filter glitch on VCD file" to filter out the glitches in the loaded waveform file.

Figure 3-21 Select VCD File Dialog Box

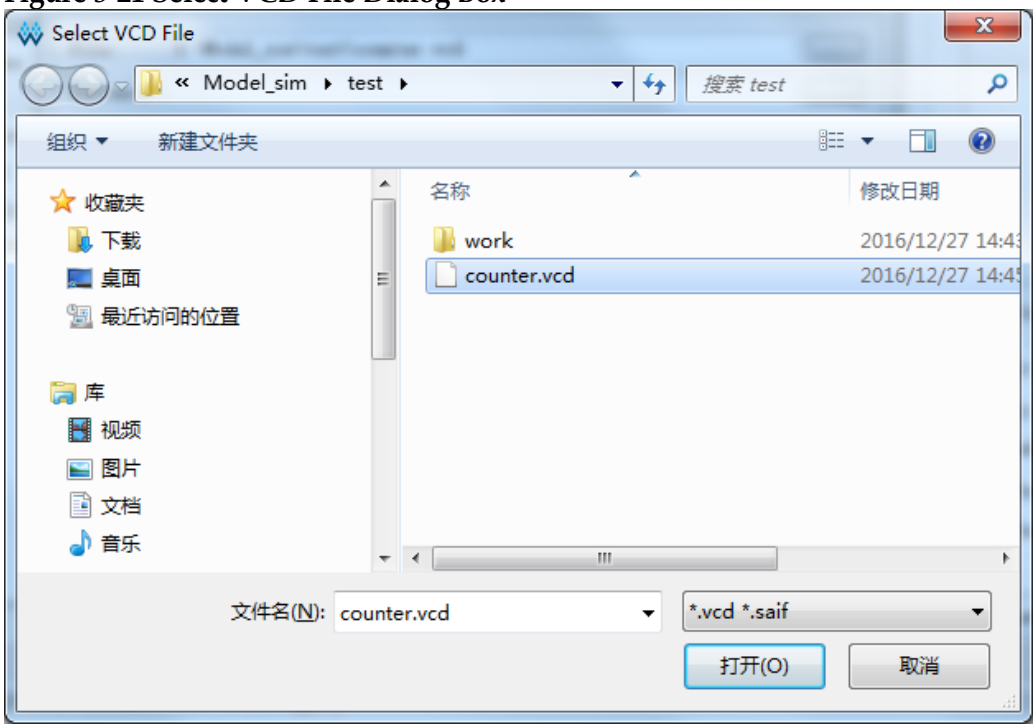


Figure 3-22 Select Instance Dialog Box

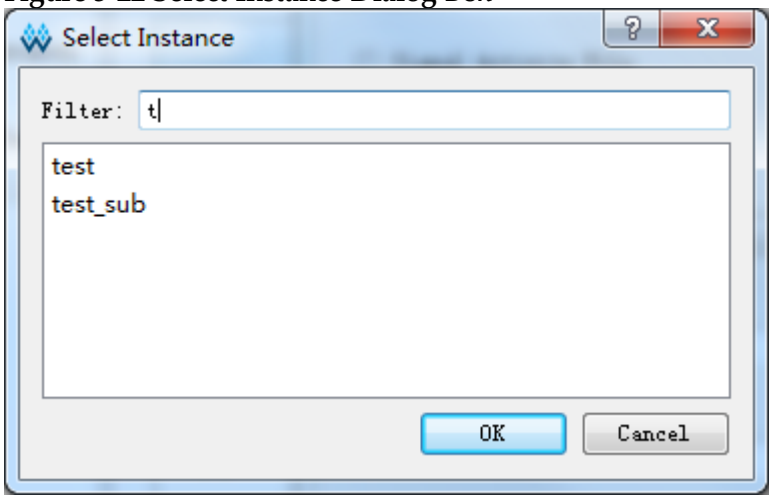
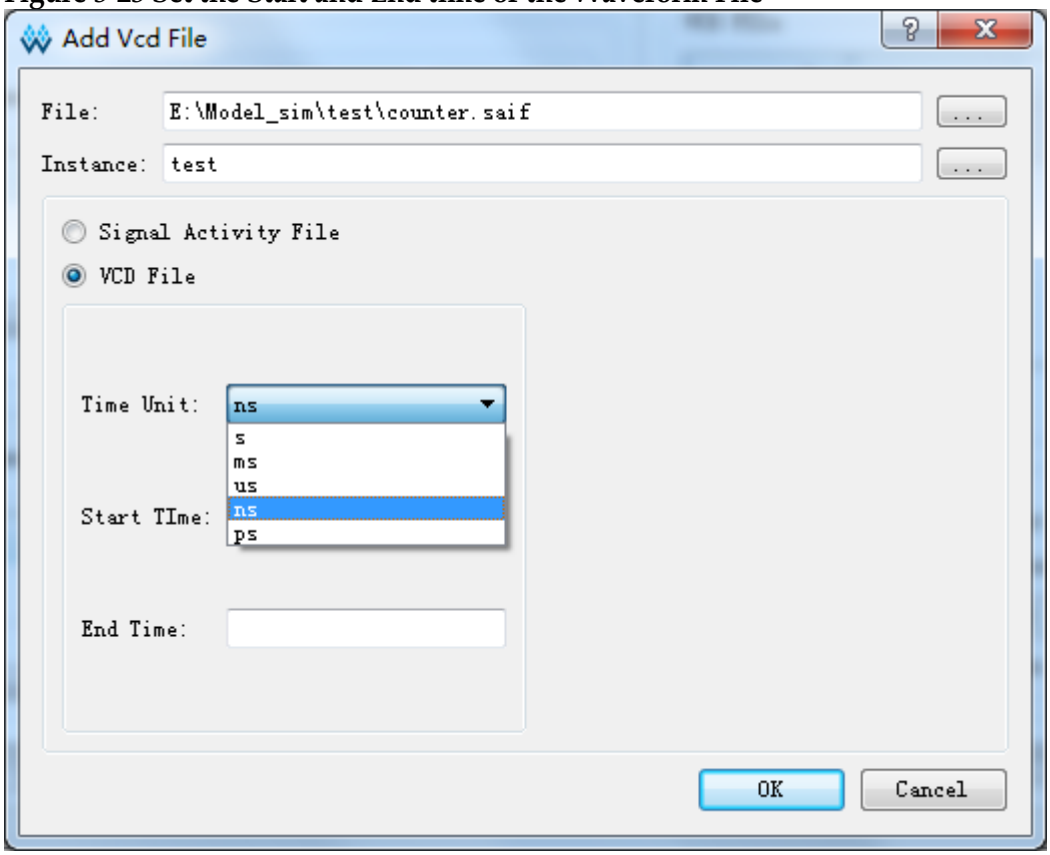


Figure 3-23 Set the Start and End time of the Waveform File

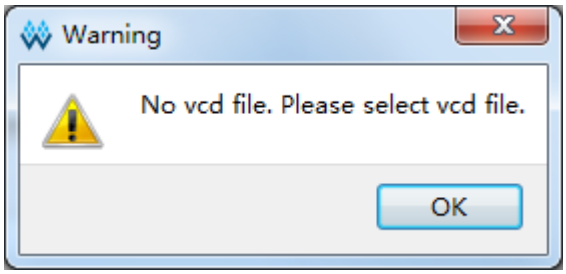


Note!

1. "Signal Activity File" and "VCD File" are used for the specified type of loaded file, which should be consistent with the type of loaded waveform.
2. When clicking the "Signal Activity File" button, the time unit and the start and end time are in an unconfigurable state.

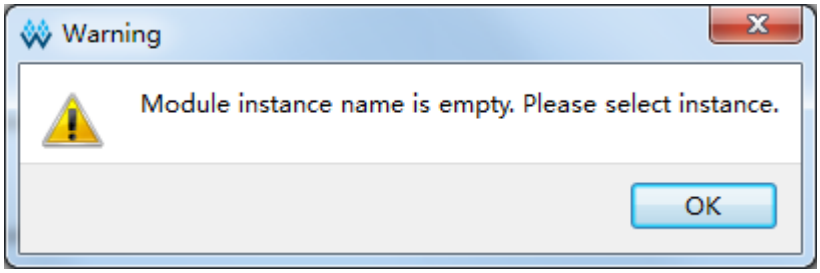
In the "ADD VCD File" dialog box, if the "Filter" configuration item is empty, click the "OK" button to pop up a prompt box without VCD files, as shown in Figure 3-24.

Figure 3-24 No VCD File Prompt Box



In the "ADD VCD File" dialog box, if the "Instance" configuration item is empty, click the "OK" button to pop up a prompt box with the Instance empty, as shown in Figure 3-25.

Figure 3-25 Instance Empty Prompt Box



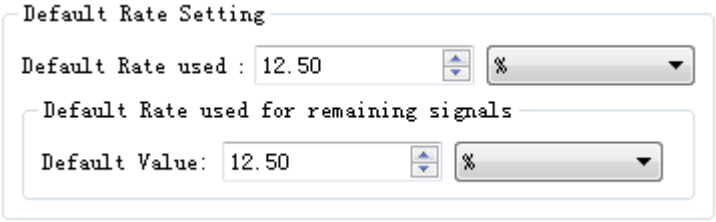
Configure Global Default Toggle Rate

Default Rate Setting is used to set global default toggle rate of I/O and Net signals, as shown in Figure 3-26.

Enter toggle rate of I/O input signals in "Default Rate used for I/O input signals" text box, click the drop-down box on the right side and select the toggle rate unit "%" (TOGGLE RATE mode) or "transition/s" (SIGNAL RATE mode) in drop-down list.

Click "Use default value″, enter I/O (except I/O input signal) and default toggle rate (Net is unspecified) in text box, click the drop-down box on the right side and select toggle rate unit "%" (TOGGLE RATE mode) or "transition/s" (SIGNAL RATE mode).

Figure 3-26 Default Rate Setting



Note!

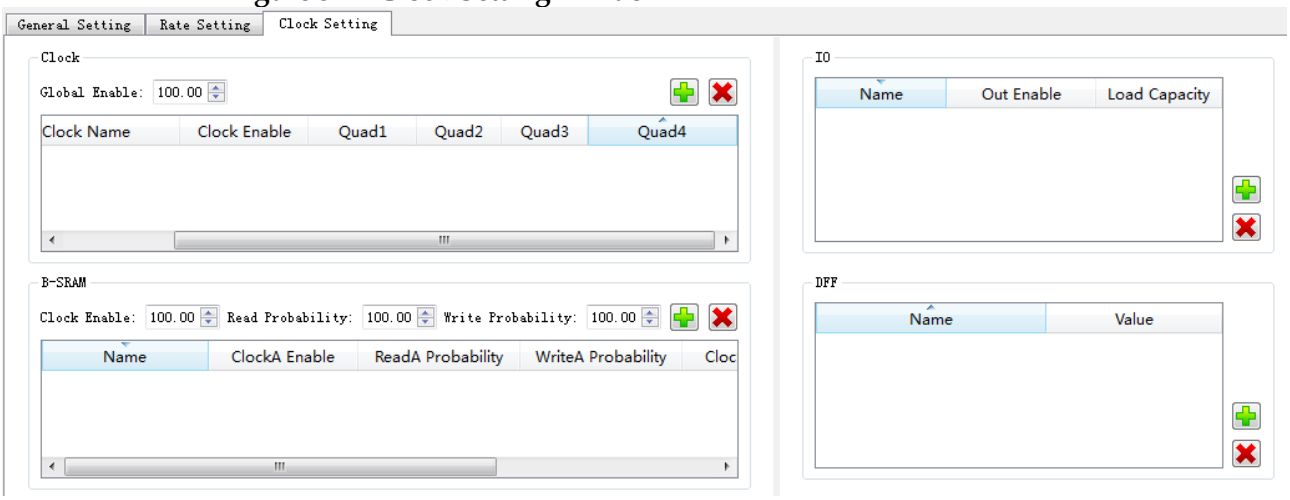
- TOGGLE RATE mode: Value represents the ratio of signal toggle rate to clock rate, unit: %;
- SIGNAL RATE mode: Value represents toggle rate of signal, unit: transition/s;
- In other cases, toggle rate of I/O and Net is determined by the priority of toggle rate of signal in each configuration zone.

3.2.3 Clock Enable

″Clock Setting″ is mainly used to configure clock and enable features of B-SRAM, I/O and DFF.

As shown inFigure 3-27, ″Clock Setting″ includes Clock, B-SRAM, I/O and DFF.

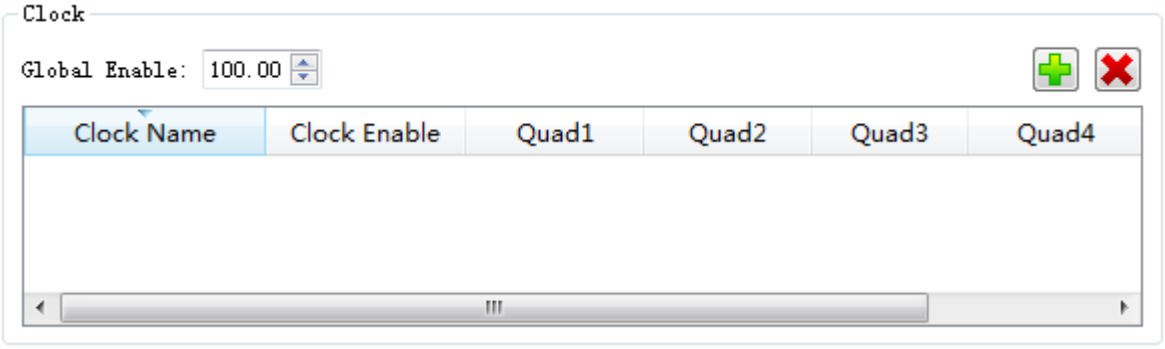
Figure 3-27 Clock Setting Window



Enable features of configuring work clock

″Clock″ is used to configure enable feature of work clock, as shown in Figure 3-28. Work clock is specified from SDC timing constraint file. The user can globally enable all clocks or the specified clock, or set clock according to quadrant. The priority of settings is quadrant, specified clock, and clock global enable.

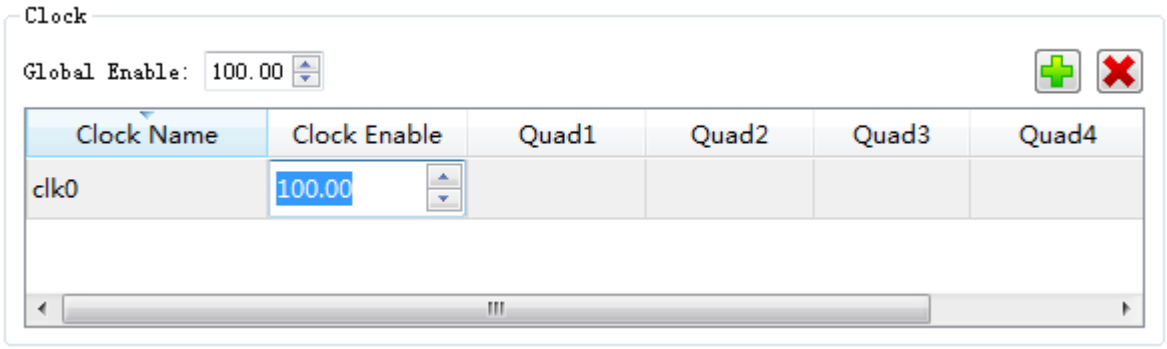
Figure 3-28 Clock



Steps of Clock operation are as follows:

1. Enter rate of global enable time for all clocks in "Global Enable";
2. Click "  " to add a row of editable table in table, as shown in Figure 3-29;
3. Specify a row, double-click cell corresponding to "Clock Name" and enter clock Name;
4. Double-click the cell corresponding to "Clock Enable", enter rate of clock enable time;
5. Double click cells corresponding to "Quad1", "Quad2", "Quad3" and "Quad4", and set enable time rate of clock in 4 quadrants.

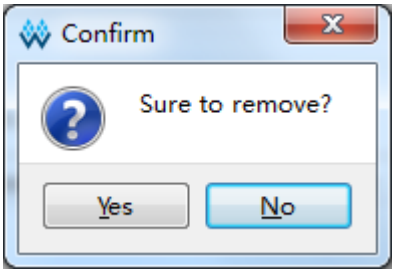
Figure 3-29 Clock Enable Setting



- Note! You can also add a row of editable table in edit section by right clicking in the blank space of table and selecting "Add" in menu.
- Clock Name should be consistent with the Name in SDC timing constraint file.

Select the line needed to be remove in edit zone, click ″  ″, and "Confirm" dialog will pop up, as shown in Figure 3-30, click "Yes" to remove enable setting for clock.

Figure 3-30 Removing Clock Enable



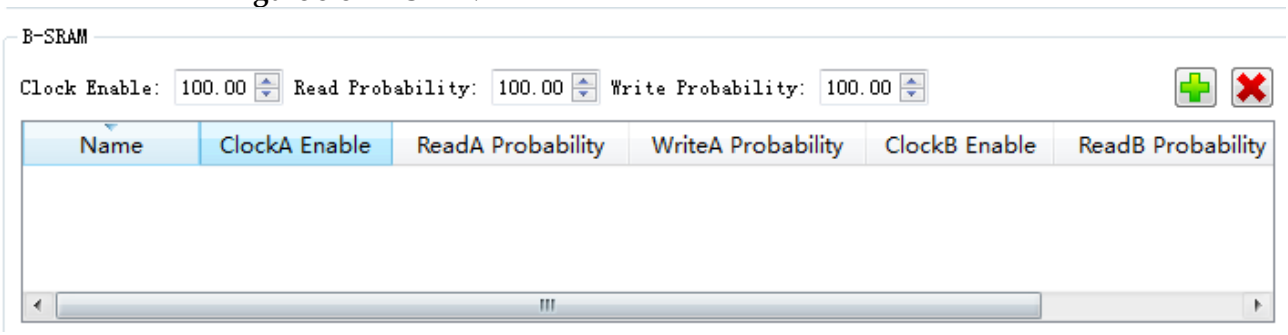
Note!

Right clicking, select ″Remove″ in menu, and "Confirm" pops up.

B-SRAM Enable Setting

″B-SRAM″ is mainly used to set enable features of B-SRAM clock and Read-Write, as shown in Figure 3-31. The user can set global enable for all B-SRAM clocks and read-write in design file, or set a specified B-SRAM. Enable setting specifying a single B-SRAM takes priority over all B-SRAM global enable settings.

Figure 3-31 B-SRAM

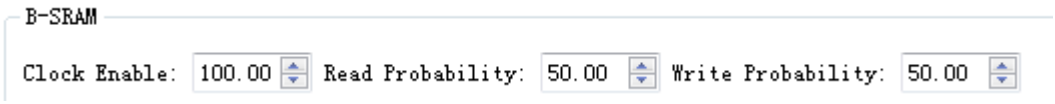


- Set enable for all B-SRAM Settings

As shown in Figure 3-32, the relevant Settings are as follows:

1. Enter rate of B-SRAM work clock enable time in ″Clock Enable″;
2. Enter rate of B-SRAM read data time in ″Read Probability″;
3. Enter rate of B-SRAM write data time in ″Write Probability″;

Figure 3-32 Set Clock Enable for all B-SRAM



Note!

- Clock Enable, Read Probability, and Write Probability parameters are valid for all B-SRAM in design file;
- If no read function exists for B-SRAM, ignore Read Probability parameter; if no write function exists, ignore Write Probability parameter.

- Enable Setting for Specified B-SRAM

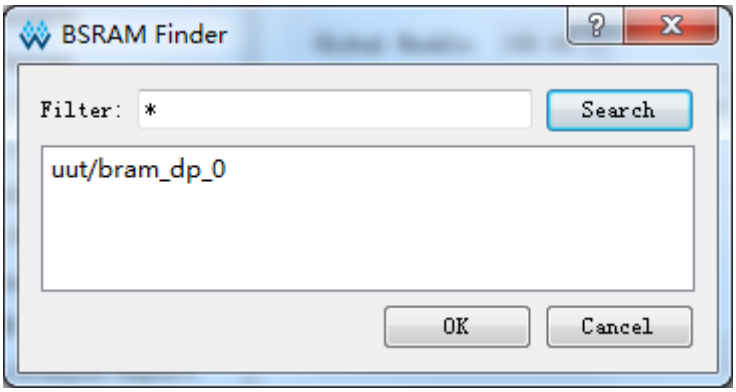
  Set enable for the specified B-SRAM after adding B-SRAM .

  Add B-SRAM

  Click ″  ″, "BSRAM Finder" dialog will pop up, as shown in Figure 3-33;

1. Enter instantiation name of B-SRAM in Filter, click "Search";
2. Select the specified B-SRAM in list, and click "OK" to finish adding B-SRAM.

Figure 3-33 BSRAM Finder Enable



Note!

- You can also right-click in the blank space of table and select "Add" in menu, dialog "BSRAM Finder" will pop up.
- "Filter" supports wildcard screening;
- The list supports options of left-click, Shift + left, and Ctrl + left.

Setting B-SRAM Enable

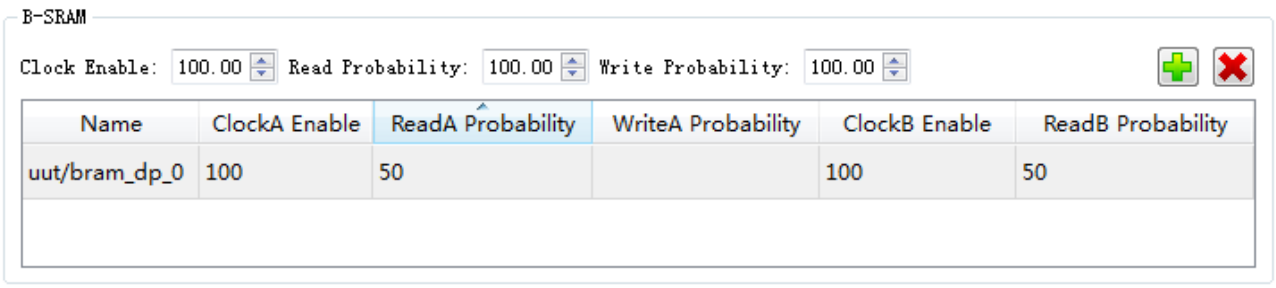
See the instantiation name of added B-SRAM in B-SRAM table. As shown in Figure 3-34, steps are as follows:

1. Select a row, double-click cell corresponding to ″ClockA Enable″, enter the time percentage of B-SRAM CLKA enable;
2. Double-click the cell corresponding to ″ReadA Probability″, enter rate

of B-SRAM CLKA read data time;

3. Double-click the cell corresponding to ″WriteA Probability″, enter rate of B-SRAM CLKA write data time;
4. Double-click the cell corresponding to ″ClockB Enable″, enter rate of B-SRAM CLKB enable time;
5. Double-click the cell corresponding to ″ReadB Probability″, enter rate of B-SRAM CLKB read data time;
6. Double-click the cell corresponding to ″WriteB Probability″, enter rate of B-SRAM CLKB write data time;

Figure 3-34 Set Specified B-SRAM Clock Enable



Note!

- If no read function of port A exists for specified B-SRAM, ReadA Probability can not be edited. If no write function of port A exists, WriteA Probability can not be edited.
- If no CLKB exists in the specified B-SRAM, the ClockB Enable can not be edited; if no read enable of B port, the ReadB Probability can not be edited; if no write enable of B port, the ReadB Probability can not be edited.

- Remove B-SRAM Enable

1. Select the row needed to be removed in table, click ″ ″, and the ″Confirm″ dialog box will pop up, as shown in Figure 3-30;
2. Click ″Yes″ to remove B-SRAM Enable Setting.

Note!

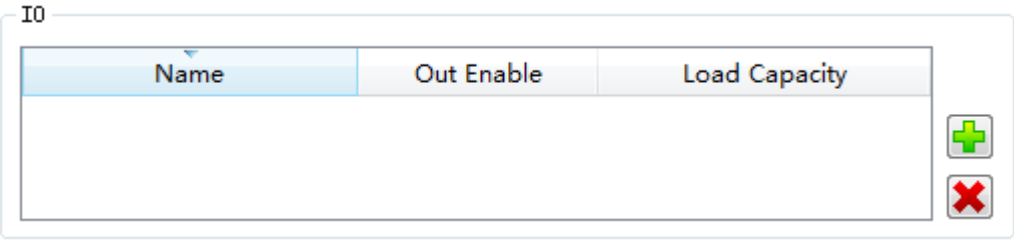
You can also select "Remove" in menu using right clicking, and "Confirm" dialog will pop up.

Configure I/O Enable Features

"I/O" is mainly used to configure OEN enable and output load features of I/O, as shown in Figure 3-35.

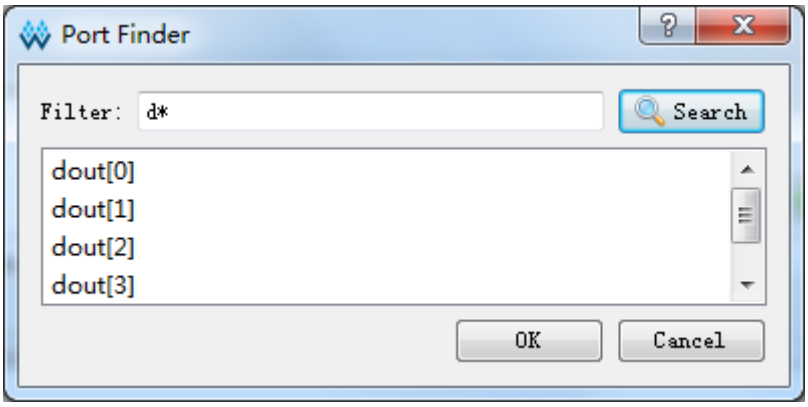
You can specify to set OEN enable rate for PORT of IOBUF or TBUF in design file, to calculate I/O power consumption. If not specified, take the fault value "50%"; You can specify to set BUF load capacitance value of TLVDS in the design file (unit pF) for calculating output power consumption, if not specified, take default value "5pF".

Figure 3-35 I/O Configuration



1. Click ″  ″, and "Port Finder" dialog box will pop up, as shown in Figure 3-36;
   a). Enter Port name in Filter, click ″Search″;
   b). Select the specified port in list, click "OK" to finish adding Port.

Figure 3-36 Port Finder

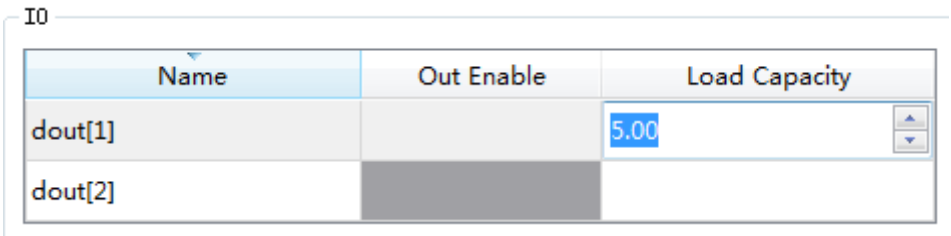


Note!

- You can also right click in blank space of table, select "Add" in menu, "Port Finder" dialog will pop up;
- "Filter" supports wildcard screening;
- The list supports options of left-click, Shift + left, and Ctrl + left.

2. Specify I/O to Set Enable Features
   a). See the added Port names in table of I/O, as shown in Figure 3-37;
   b). Specify a row, double-click cell corresponding to ″Out Enable″, and enter rate of OEN enable time;
   c). Double-click cell corresponding to ″Load Capacity″, and enter load capacitance value.

Figure 3-37 Specify I/O to Set Enable Features



Note!

If no OEN function exists for the specified BUF, "Out Enable" is unavailable.

3. Remove I/O Enable Setting

a). Select the row needed to be removed in table, click "  ", "Confirm" dialog will pop up, as shown in Figure 3-30;

b). Click "Yes" to remove I/O enable setting.

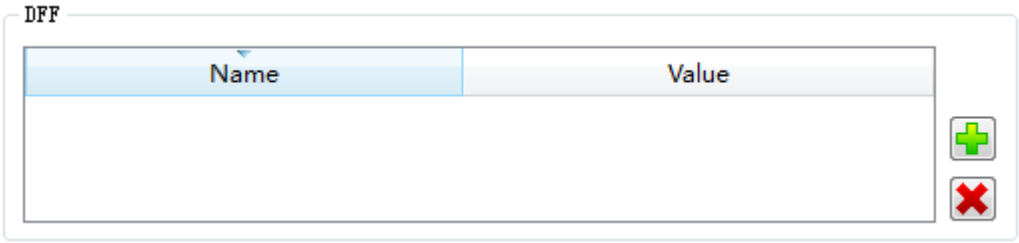
Note!

You can also right click to select ″Remove″ in menu, and the ″Confirm″ dialog box will pop up.

Configure DFF Enable

"DFF" is mainly used to configure DFF clock enable, as shown in Figure 3-38.

Figure 3-38 DFF Configuration



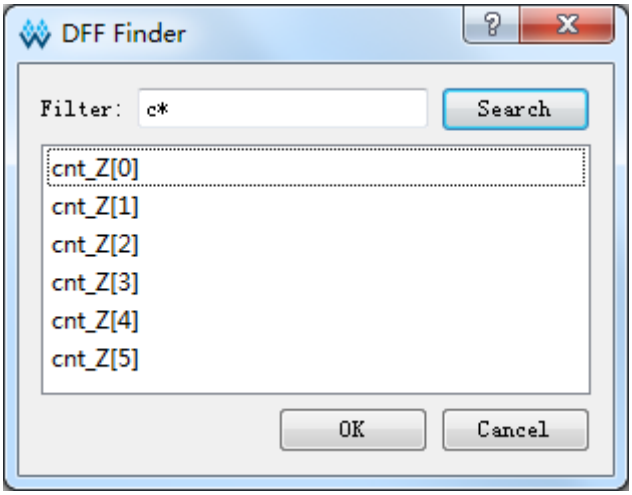
1. Add DFF

a). Click ″  ″, "BSRAM Finder" dialog will pop up, as shown in Figure 3-39;

b). Enter instantiation name of DFF in Filter, click "Search";

c). Select the specified DFF in list and click "OK" to finish adding DFF.

Figure 3-39 DFF Finder



Note!

- You can also right-click in the blank space of table, select "Add" in menu. "DFF Finder" dialog will pop-up;
- "Filter" supports wildcard screening;
- The list supports options of left-click, Shift + left, and Ctrl + left.

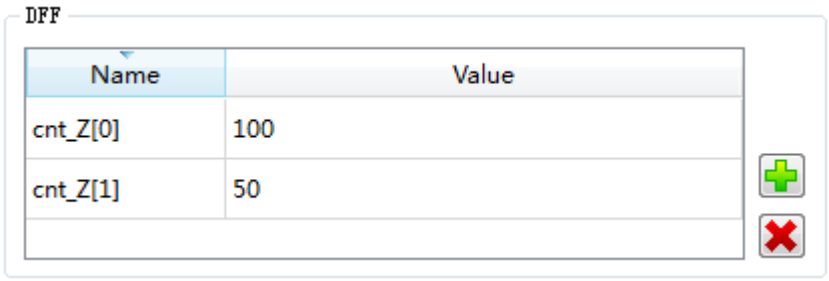
2. Specify and set DFF enable

a). See instantiation name of the added DFF in DFF table, as shown in

Figure 3-40;

b). Specify a row, double-click cell corresponding to "Value", enter rate of DFF clock enable time.

Figure 3-40 Specify and Set DFF Enable



3. Remove DFF clock enable setting

a). Select the row needed to be removed in table, click ″ ″, and the ″Confirm″ dialog box pops up, as shown in Figure 3-30;

b). Click ″Yes″ to remove DFF clock enable.

Note!

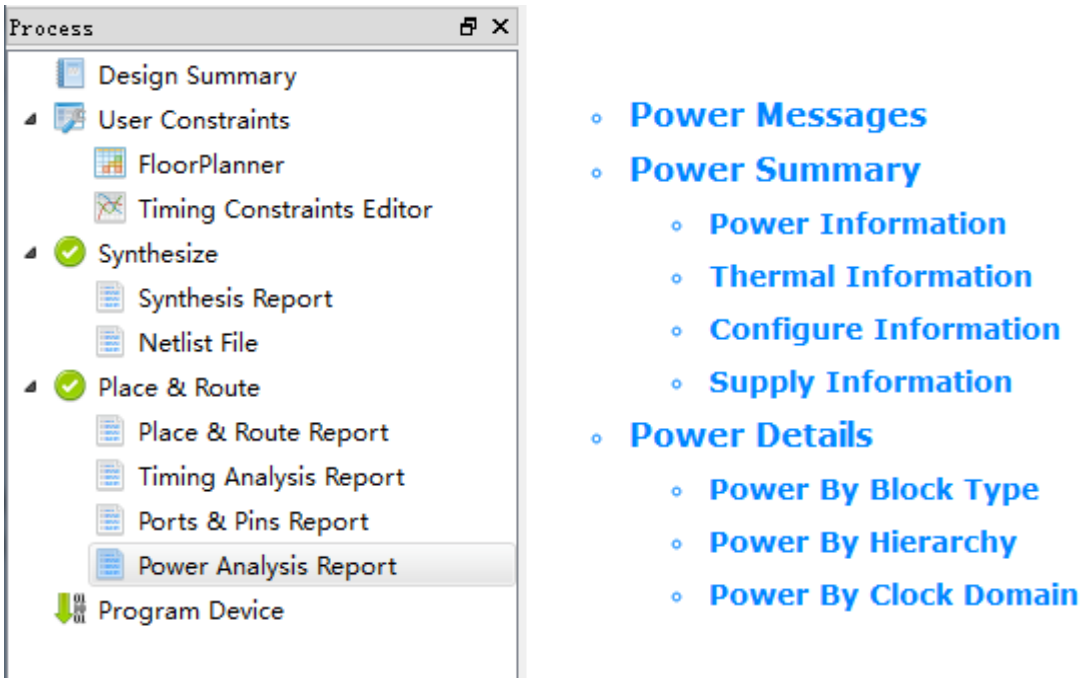
Right clicking, select ″Remove″ in menu, and "Confirm" pops up.

3.3 Generate GPA Power Analysis Report

After configuring GPA file, click ″ ″ to save. Double-click ″Place&Route″ in Process, to perform the whole place&route and produce GPA Report.

Double-click ″Place&Route > Power Analysis Report″ in Process, GPA Report will pop up in main window, as shown in Figure 3-41.

Figure 3-41 Open GPA Report



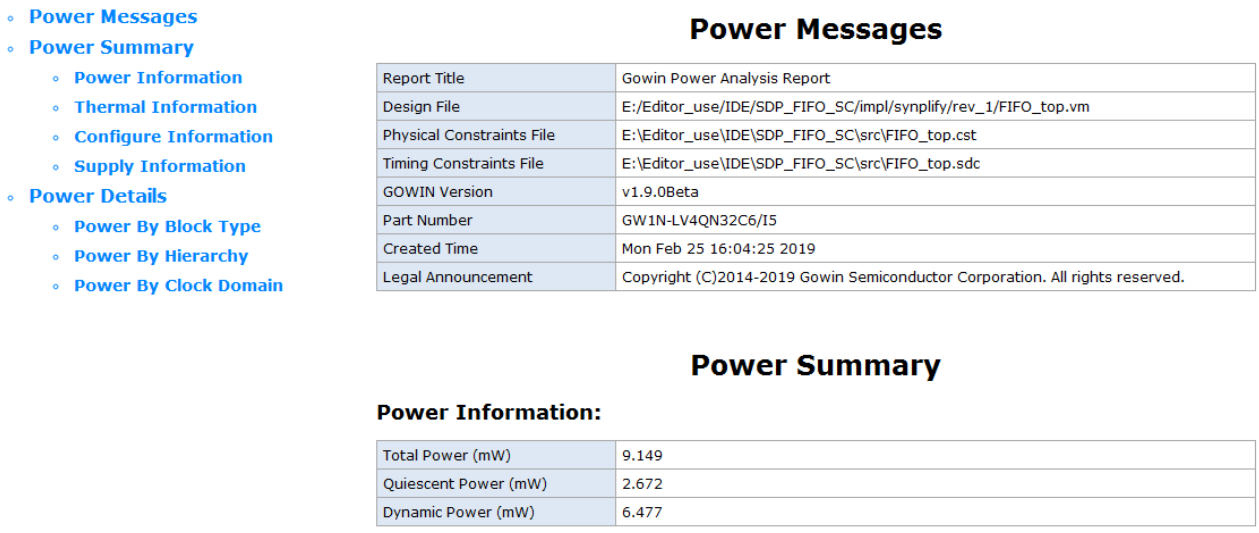
4 Power Analysis Report

GPA report shows the estimated result of power consumption calculated by the user-defined parameters, which helps users more easily to analyze and design power dissipation, to solve the calculating problem for user.

GPA report includes two parts: Navigation tree and text content, as shown in Figure 4-1. Title navigation tree is used to hierarchically display report titles using hyperlinks with text content, which helps users to find the required content more easily.

Power Analysis Report content is divided into three parts: Power Message, Power Summary and Power Details. Power Messages mainly introduces the device and design engineering files; Power Summary mainly introduces parameters set by the user and power consumption result by calculating. Power Detail mainly introduces the power consumption of Block type, design hierarchy, and clock domain.

Figure 4-1 GPA Report



4.1 Power Message

Power Message contains title, tool version, device type, package, speed, temperature range, process, user design name, design file, constraint file information, power report file and created time, command line and legal announcement, as shown in Figure 4-2.

Figure 4-2 Power Message

Power Messages

Report Title	Gowin Power Analysis Report	①
Design File	E:/Editor_use/IDE/SDP_FIFO_SC/impl/synplify/rev_1/FIFO_top.vm	②
Physical Constraints File	E:\Editor_use\IDE\SDP_FIFO_SC\src\FIFO_top.cst	③
Timing Constraints File	E:\Editor_use\IDE\SDP_FIFO_SC\src\FIFO_top.sdc	④
GOWIN Version	v1.9.0Beta	⑤
Part Number	GW1N-LV4QN32C6/I5	⑥
Created Time	Mon Feb 25 16:04:25 2019	⑦
Legal Announcement	Copyright (C)2014-2019 Gowin Semiconductor Corporation. All rights reserved.	⑧

① Report Title
② Design File
③ Physical Constraint File
④ Timing Constraints File
⑤ YunYuan software tool version
⑥ Device
⑦ Created Time
⑧ Legal Announcement

4.2 Power Summary

Power Summary includes Power Information for reporting total power consumption, Thermal Information for reporting thermal impedance, Configure Information for reporting configuring environmental, and Supply Information for reporting voltage.

4.2.1 Power Information

Power Information is used to report total power consumption, total static power consumption, and total dynamic power consumption, as shown in Figure 4-3.

Figure 4-3 Power Information

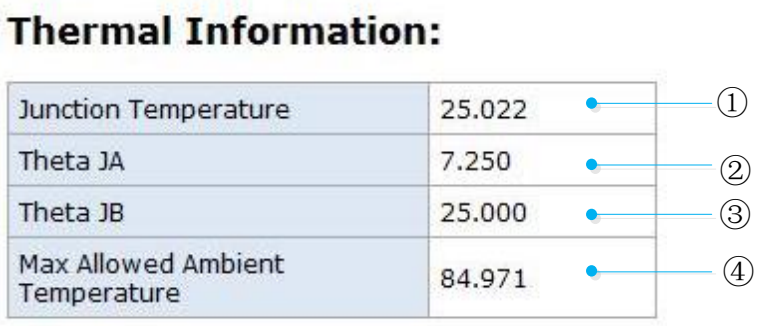
Power Information:

Total Power (mW)	5.357
Quiescent Power (mW)	3.167
Dynamic Power (mW)	2.189

4.2.2 Thermal Information

Thermal Information is used to report junction temperature, Theta $\theta_{JA,}$ θ_{JB} and allowed max. ambient temperature, as shown in Figure 4-4.

Figure 4-4 Thermal Information



①Junction Temperature ②Theta JA

③Theta JB ④Allowed Max. Ambient Temperature

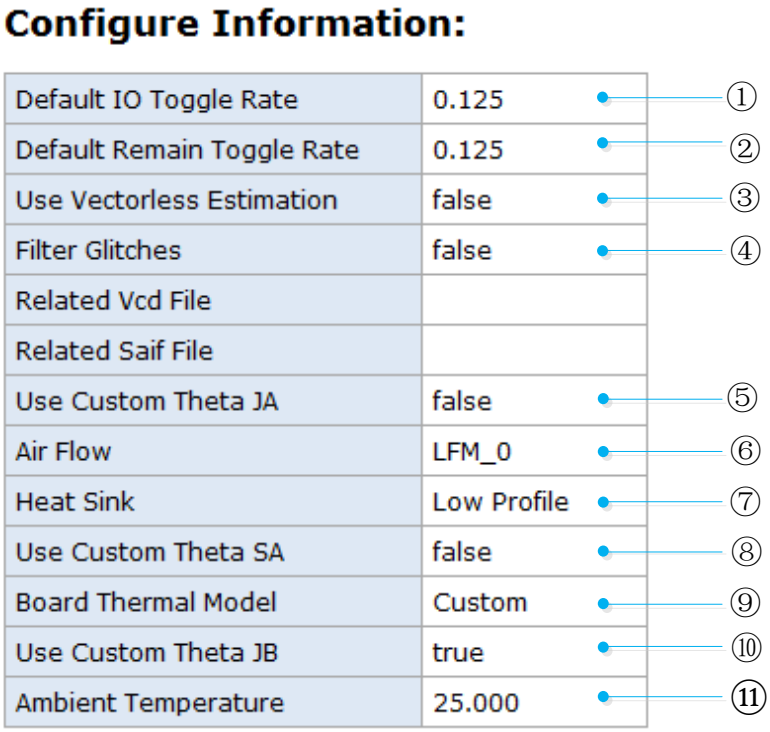
Note!

- Junction Temperature: Operating temperature of bare chip;
- Theta JA: thermal resistance θ_{JA}, dissipate chip heat from shell to outside;
- the ambient temperature set by the user is higher than the maximum allowable ambient temperature, the junction temperature is red.

4.2.3 Configure Information

Configure Information is used for reporting default I/O toggle rate, default remain toggle rate, use vectorless estimation, filter glitches, user defined thermal θ_{JA}, air flow, heat sink, user defined thermal θ_{SA}, board thermal model, user defined thermal θ_{JB} and ambient temperature, as shown in Figure 4-5.

Figure 4-5 Configure Information



① Default I/O toggle rate

② Default Remain toggle rate

③ Use ***vectorless*** Estimation

④ Filter Glitches

⑤ Use Custom Thermal θ_{JA}

⑥ Air Flow

⑦ Heat Sink

⑧ Use Defined Thermal θSA

⑨ Board Thermal Model

⑩ Use Defined Thermal θJB

⑪ Ambient Temperature

4.2.4 Supply Information

Supply Information is used for reporting the voltage, dynamic current, quiescent current and power consumption of core, auxiliary voltage, dynamic current, quiescent current and its power consumption of device, voltage, dynamic current, quiescent current and power consumption of device output, as shown in Figure 4-6.

Figure 4-6 Supply Information

Supply Information:

Voltage Source	Voltage	Dynamic Current(mA)	Quiescent Current(mA)	Power(mW)
VCC	1.000	1.054	1.602	2.655
VCCX	3.300	0.182	0.088	0.890
VCCO18	1.800	0.181	0.087	0.483

4.3 Power Details

Power Details include Power By Block Type for reporting power consumption by Block, Power By Hierarchy for reporting power consumption by hierarchy, and Power By Clock Domain for reporting power consumption by clock domain.

4.3.1 Power By Block Type

Power By Block Type reports total power consumption of Blocks, static power, and average toggle rate included in file according to Block, as shown in Figure 4-7. Block includes Logic, /IO, B-SRAM, DSP, PLL, DLL, DQS, DLLDLY and so on.

Figure 4-7 Power By Block Type

Power By Block Type:

Block Type	Total Power(mW)	Static Power(mW)	Average Toggle Rate(millions of transitions/sec)
Logic	0.205	NA	12.500
IO	1.645	0.536	21.250

Note!

NA indicates that the parameter is not considered.

4.3.2 Power By Hierarchy

Power By Hierarchy is used for reporting dynamic Power consumption of the total Power consumption, dynamic Power consumption and wiring resources generated from top to bottom module in design file according to hierarchical relationship in design file, as shown in Figure 4-8.

Figure 4-8 Power By Block Type

Power By Hierarchy:

Hierarchy Entity	Total Power(mW)	Block Dynamic Power(mW)	Routing Dynamic Power(mW)
top	0.868	0.205(0.002)	0.663(0.149)
top/uut/	0.152	0.002(0.000)	0.149(0.000)

4.3.3 Power By Clock Domain

Power By Clock Domain is used for reporting the name, frequency, and dynamic Power consumption of working Clock based on Clock Domain, as shown in Figure 4-9.

Figure 4-9 Power By Block Type

Power By Clock Domain:

Clock Domain	Clock Frequency(Mhz)	Total Dynamic Power(mW)
DEFAULT_CLK	100.000	0.871

Appendix A Calculation Principle for Junction Temperature

Junction temperature (TJ) refers to the working temperature of bare chip, which is determined by external temperature (TA), power consumption (P) and heat dissipation features of chip and outside. The temperature of bare chip is balanced by heat dissipation and external environment. Heat dissipation includes two types: heat sink and non-heat sink.

- Non-heat sink

The model mainly dissipates heat through development board and CASE, thermal impedance (θ_{JA}) means rising temperature corresponding to power consumption, unit (℃ / W), which is influenced by air flow; In Non-heat sink mode, The relationships between power P and thermal impedance θ_{JA}, TJ, TA are shown in Formula 1.

$$P = (TJ - TA) / \theta_{JA} \quad \text{(Formula 1)}$$

- Heat Sink

Through CASE, chip heat dissipates by means of heat sink via media materials, and the total thermal impedance of the path is called θ_{JA}. The chip heat also can dissipate by means of development board, and the thermal impedance of the path is called θ_{JB}.

θ_{JA} consists of three parts: heat impedance theta θ_{JC} from chip to CASE, heat sink thermal impedance θ_{CS} from CASE to and thermal impedance θ_{SA} from heat sink into the surrounding environment, calculation formula is as shown in formula 2:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad \text{(Formula 2)}$$

The relationship between power P and thermal impedance θ_{JA}, TJ, TA, TB (plate temperature) is shown in formula 3:

$$P = (TJ - TA) / \theta_{JA} + (TJ - TB) / \theta_{JB} \quad \text{(Formula 3)}$$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