

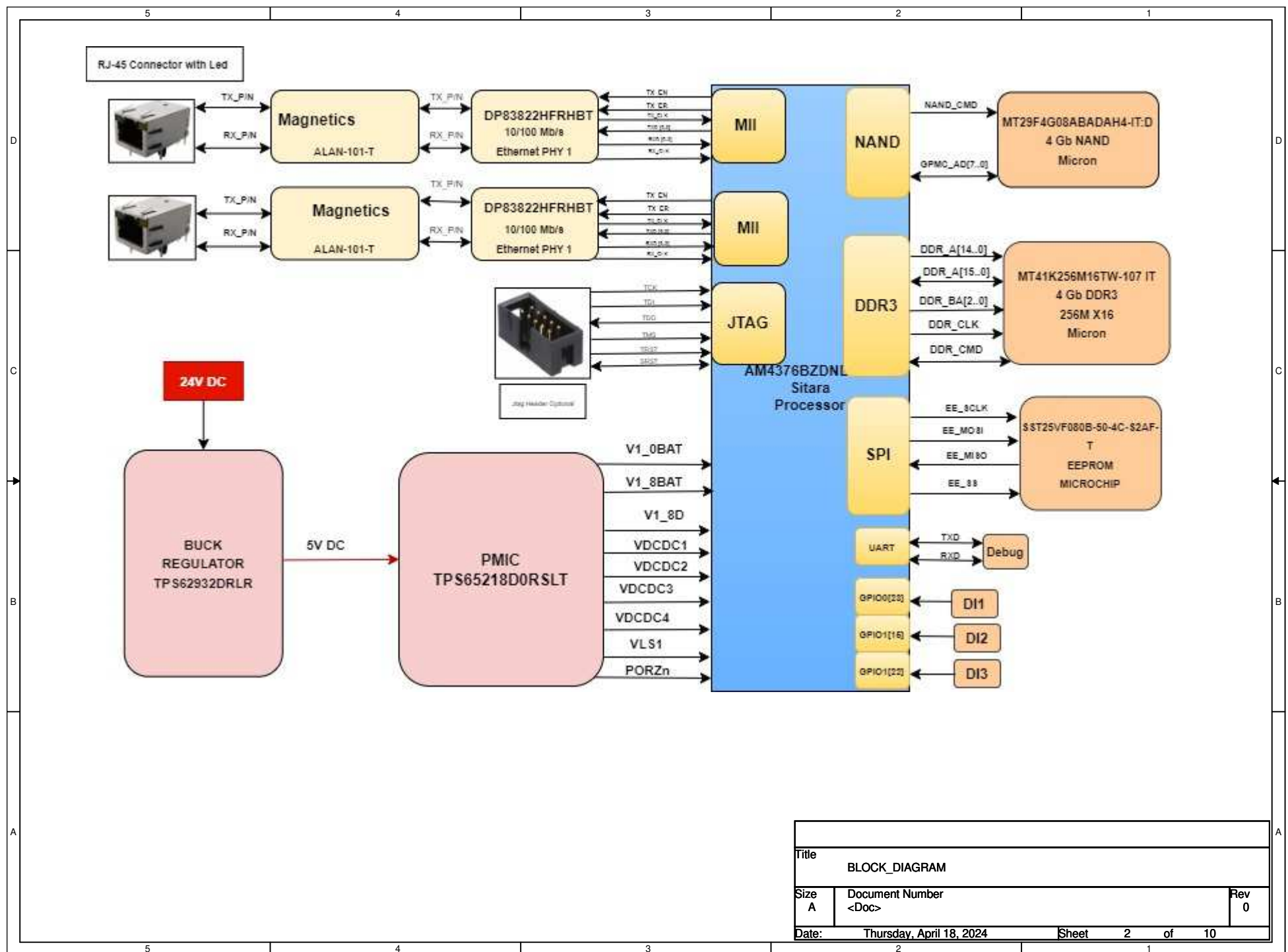
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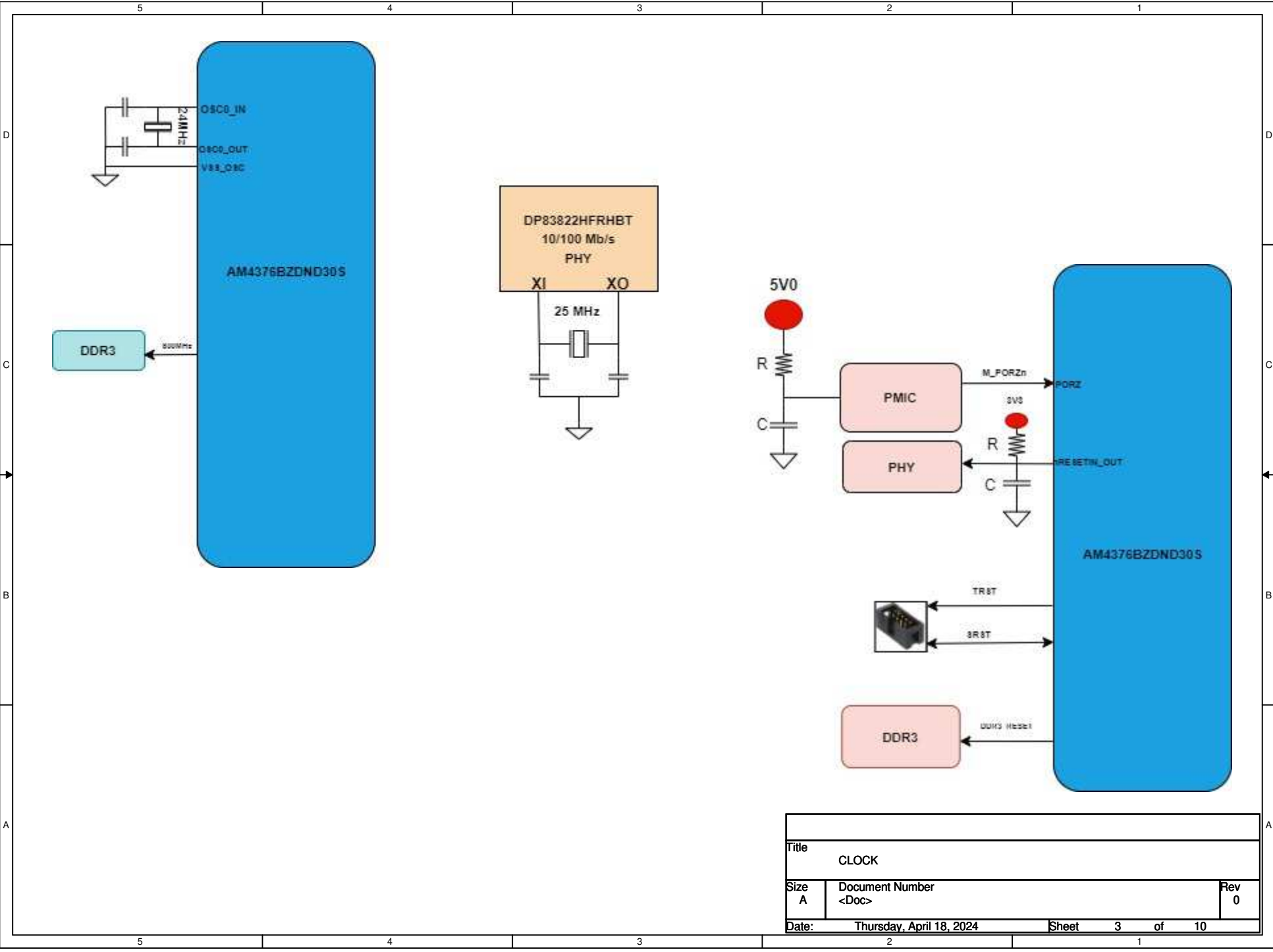
PROJECT NAME: Pearl EIP Comm Module  
CAT NO:

## REVISION HISTORY

Sr.No.	REVISION	REV DATE	PREPERED BY	REVIEWED BY	APPROVED BY
1	0	06-FEB-2024	VY/RK	GS	

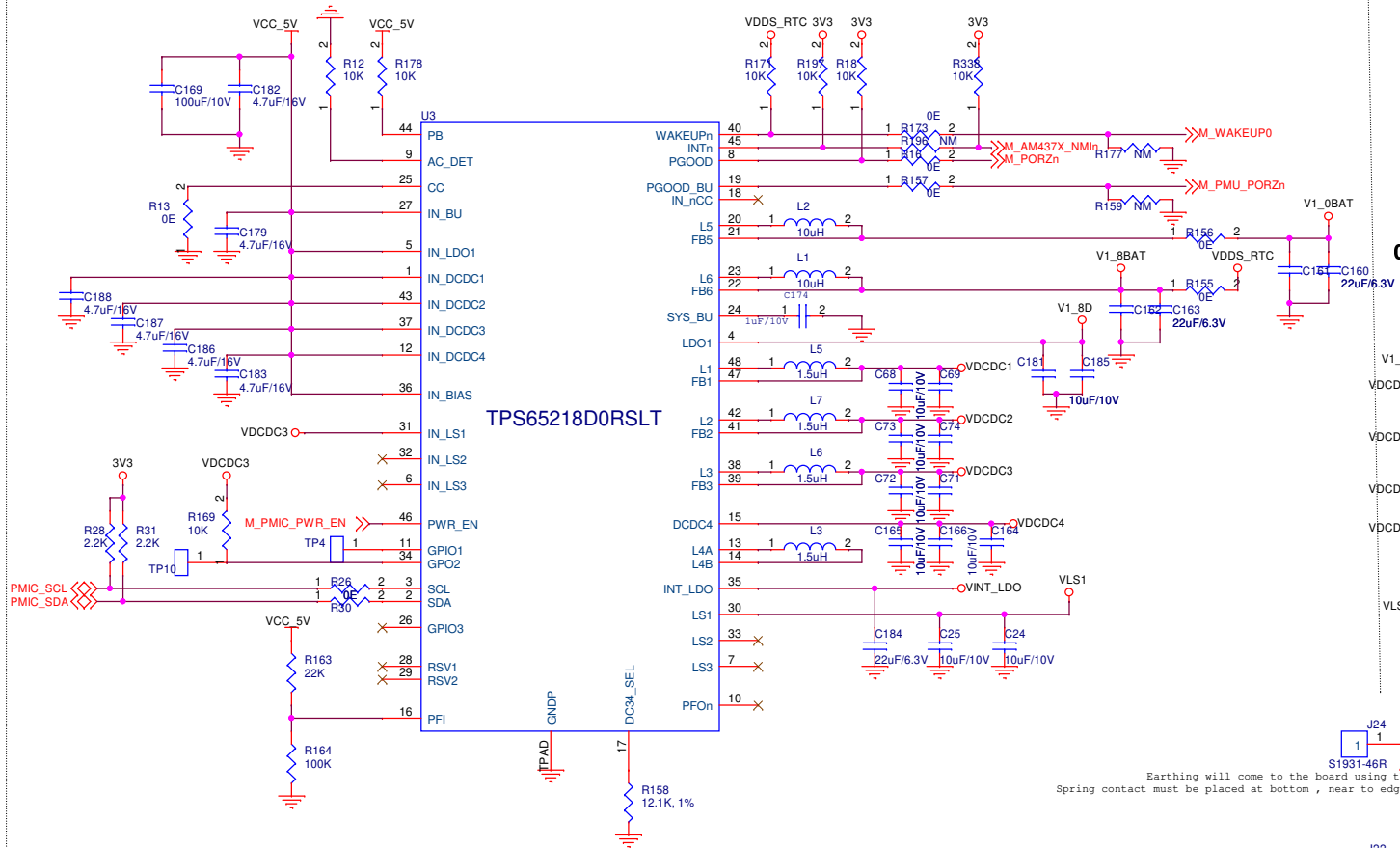


Title		
BLOCK_DIAGRAM		
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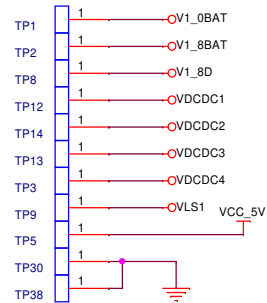


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CLOCK		
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## POWER MANAGEMENT - PMIC

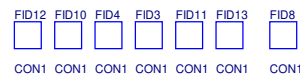


### Test Points



On Bottom side  
Place One GND TP on  
TOP & BOT

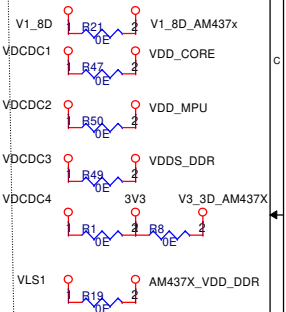
### Fiducial



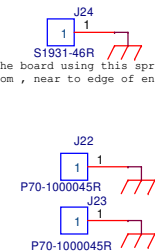
### Mounting Holes



### OE for PMIC TESTING



Earthing will come to the board using this spring contact.  
Spring contact must be placed at bottom, near to edge of enclosure mating

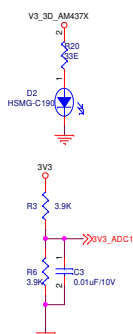
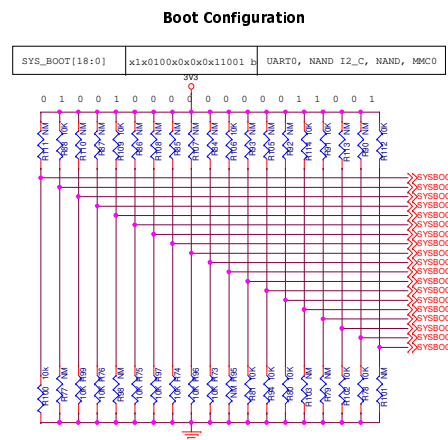
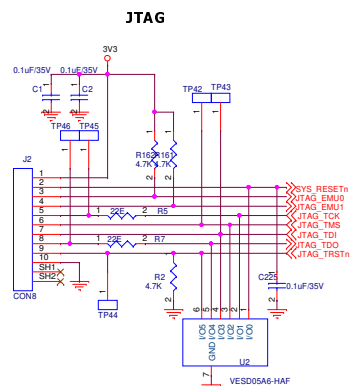
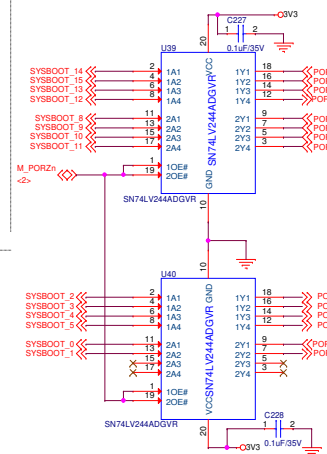
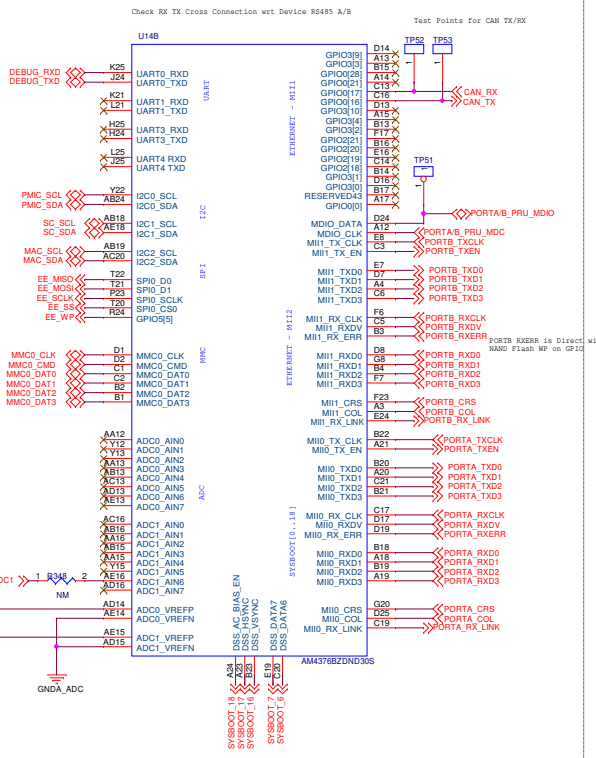
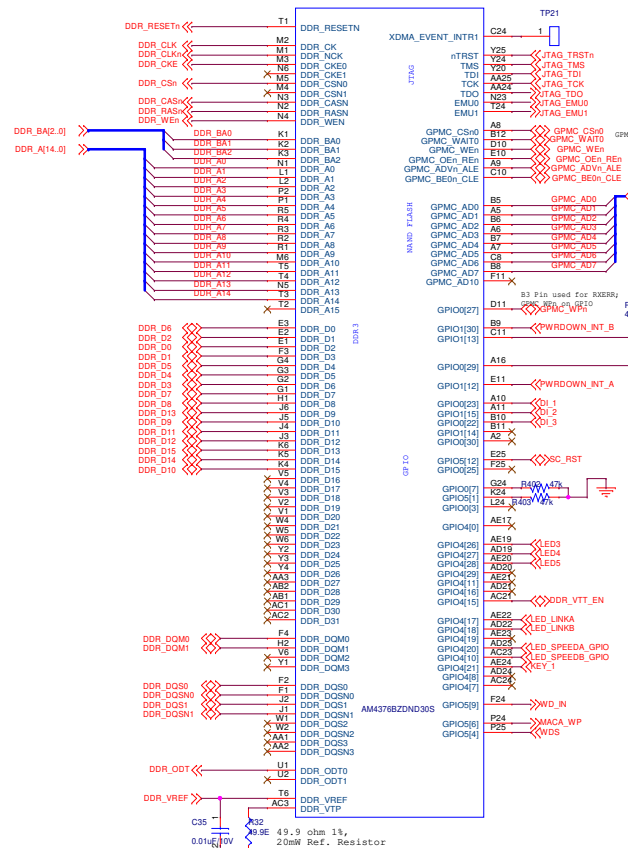


Pogo pins must be kept just below ethernet connector of PS card.  
Placement of pogo pins should not be under spring contact of ethernet connector

Pearl Ethernet Main Card Schematic			
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PMIC			
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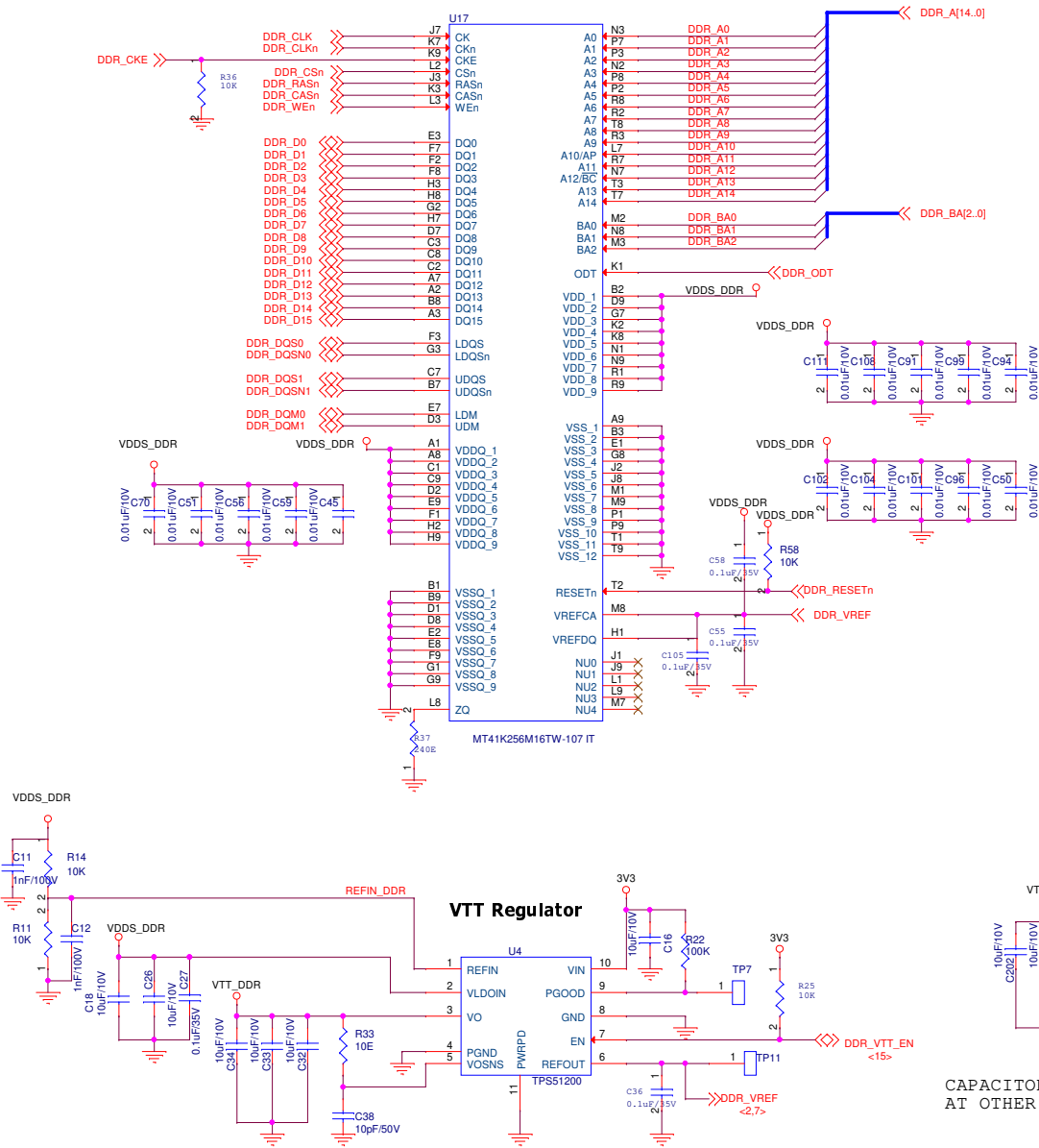
## PROCESSOR SUBSYSTEM



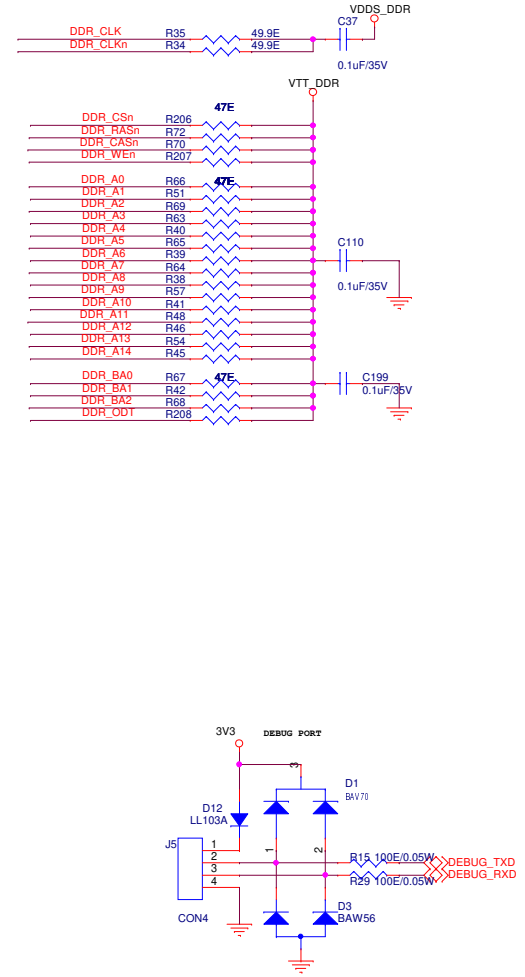
Check Connection & Sequence with  
EMULATOR and Probe to be used

## DDR3 INTERFACE

**4 Gb DDR3 SDRAM**

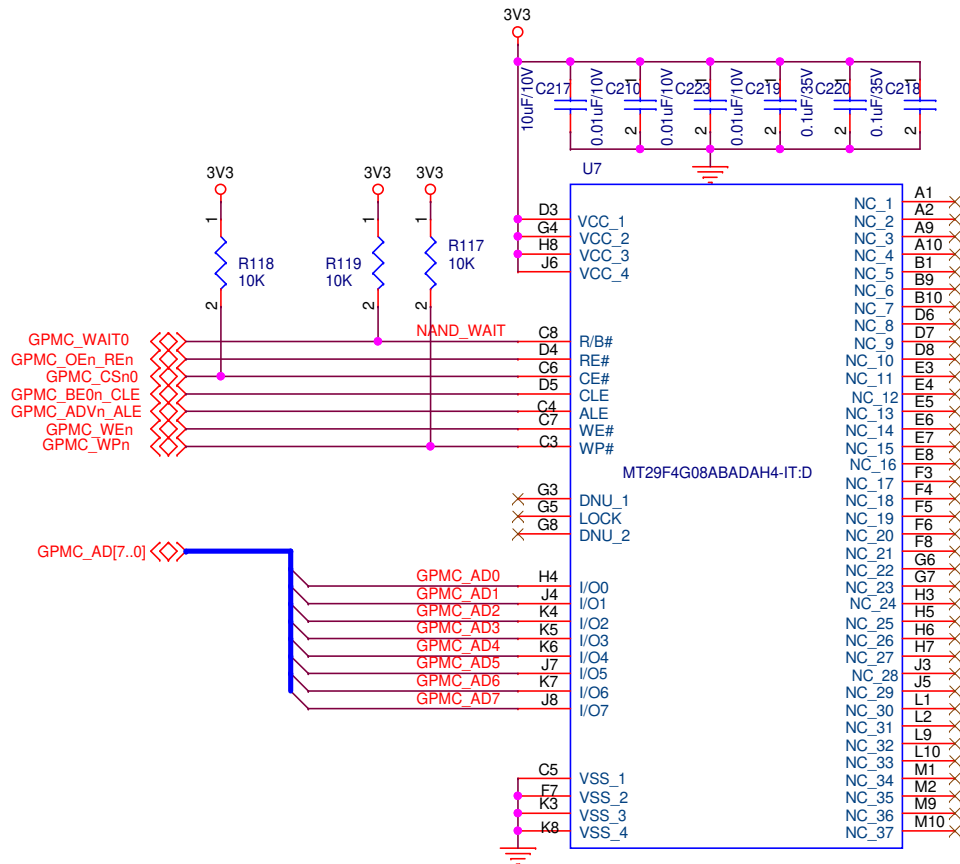


## Terminations



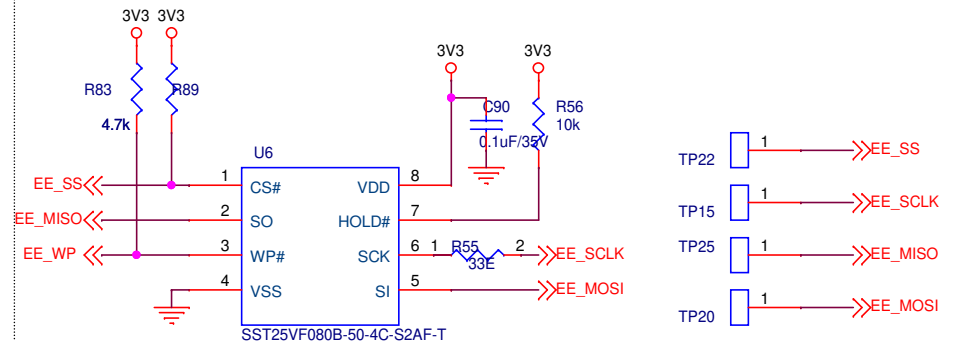
CAPACITOR TO BE PLACED  
AT OTHER END OF VTT PLANE

## 4Gb NAND Interface



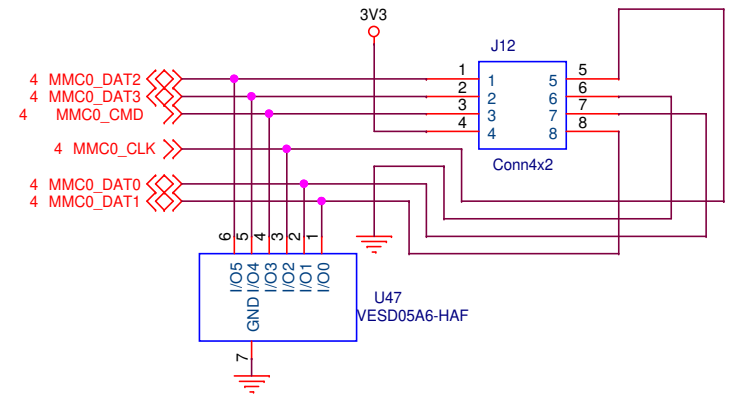
NAND WPn is TAKEN FROM GPIO0[27]  
Check boot condition of IO WP/RXERROR select; Use Pull up; Pull down; NO\NC Accordingly

## FLASH/EEPROM



Place 33E on SCLK close to Processor

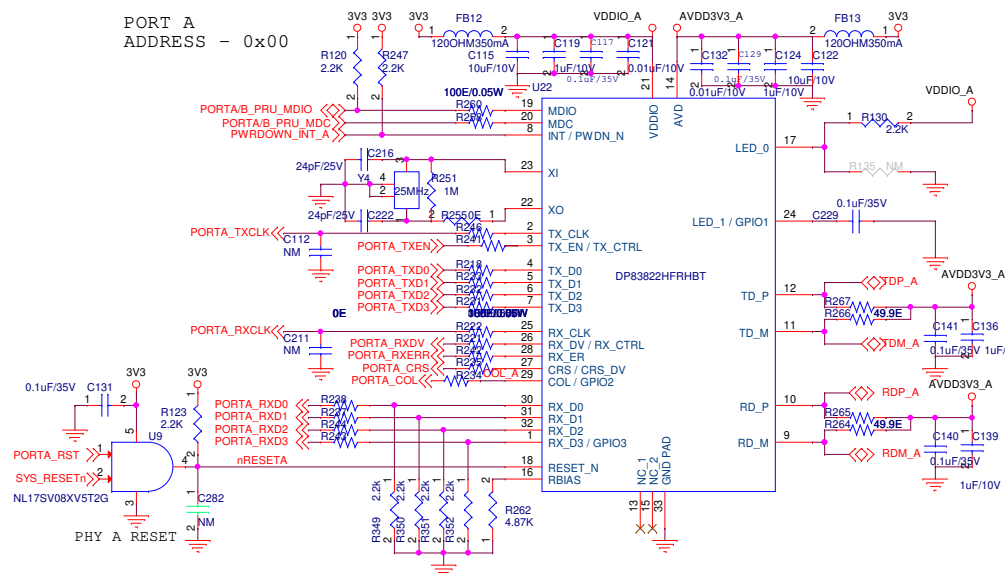
## MMC PROVISION



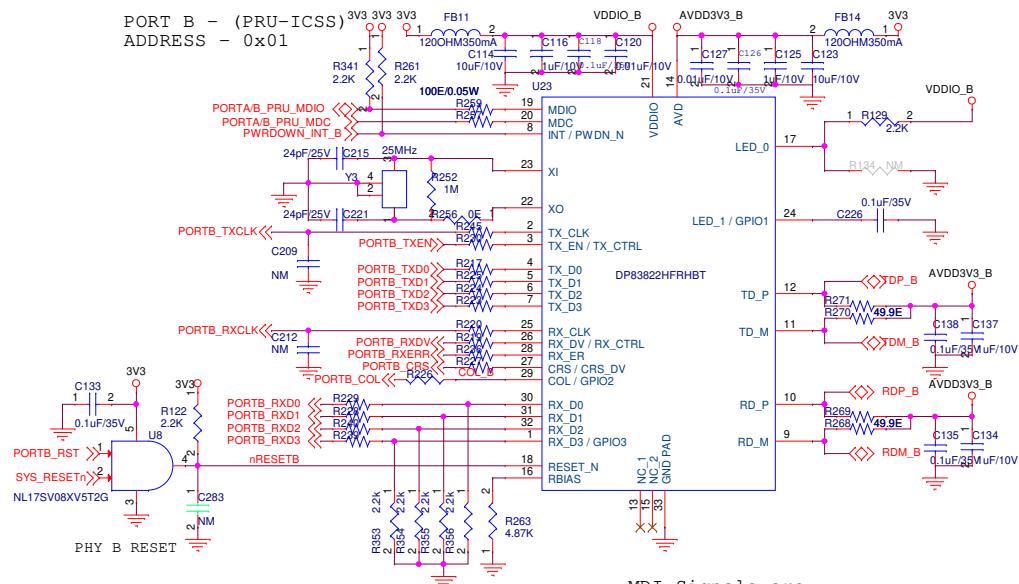
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FLASH NAND VS EEPROM			
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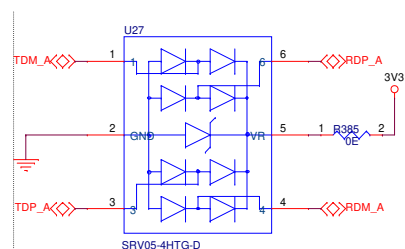
PORT A  
ADDRESS - 0x00



PORT B - (PRU-ICSS)  
ADDRESS - 0x01

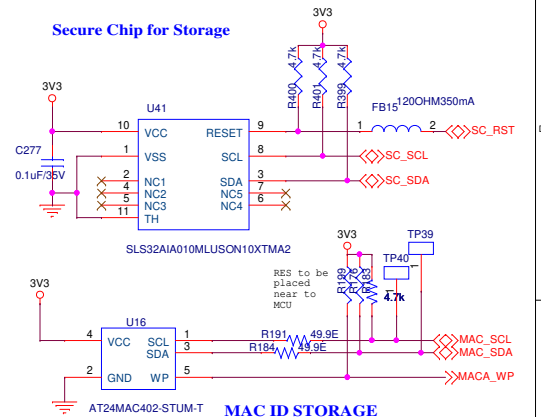


MDI Signals are  
100 Ohm Differential Signals

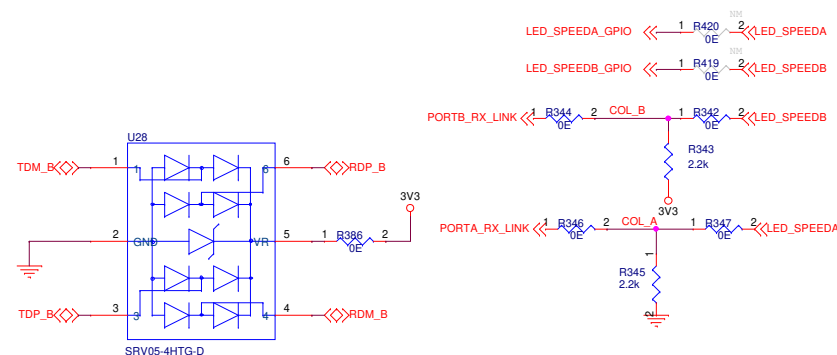


MODBUS TCP/IP PHYSICAL INTERFACE

Secure Chip for Storage

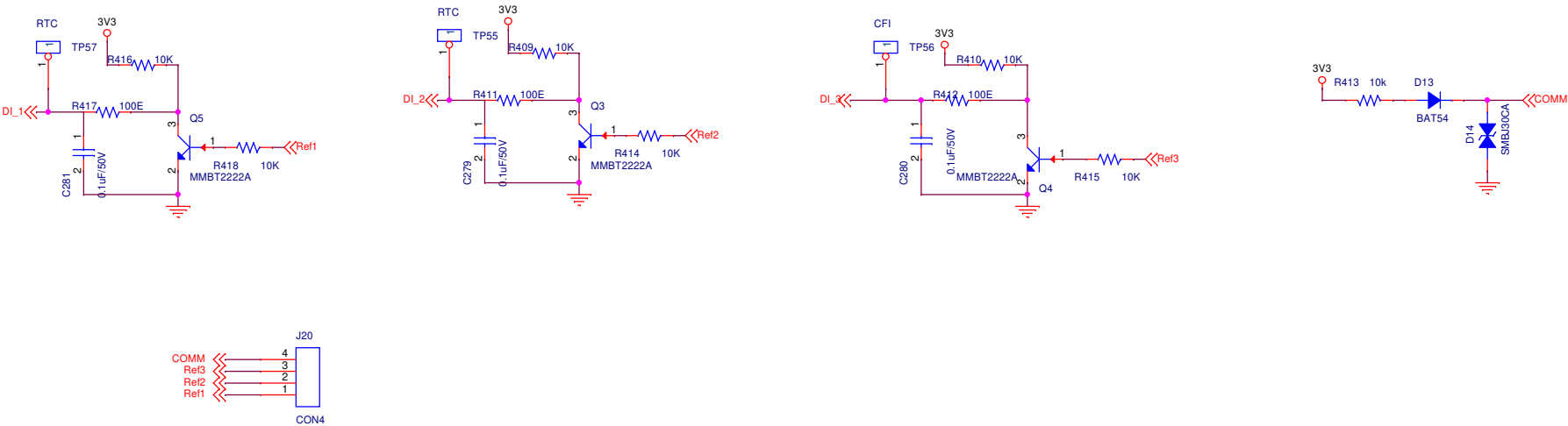


MAC ID STORAGE



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Dual Phy Interface			
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Digital Input Interface and its circuitry



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