cadence™

Analog & Mixed Signal Labs

Revision 2.0
IC615
Assura 410
Incisive Unified Simulator 102

Developed By
University Support Team
Cadence Design Systems, Bangalore

Objective

Objective of this lab is to learn the Virtuoso tool as well learn the flow of the Full Custom IC design cycle. You will finish the lab by running DRC, LVS and Parasitic Extraction on the various designs. In the process you will create various components like inverter, differential amplifier, operational amplifier, R-2R based DAC and Mixed signal design of SAR based ADC, but we won't be designing every cell, as the time will not be sufficient, instead we will be using some ready made cells in the process.

You will start the lab by creating a library called "**myDesignLib**" and you will attach the library to a technology library called "**gpdk180**". Attaching a technology library will ensure that you can do front to back design.

You will create a new cell called "**Inverter**" with schematic view and hence build the inverter schematic by instantiating various components. Once inverter schematic is done, symbol for "**Inverter**" is generated. Now you will create a new cell view called "**Inverter_Test**", where you will instantiate "**Inverter**" symbol. This circuit is verified by doing various simulations using spectre. In the process, you will learn to use spectre, waveform window options, waveform calculator, etc...

You will learn the Layout Editor basics by concentrating on designing an "**Inverter**" through automatic layout generation. Then you will go ahead with completing the other layouts. After that, you will run DRC, LVS checks on the layout, Extract parasitics and back-annotate them to the simulation environment.

After completing the parasitic back- annotation flow, design is ready for generating GDSII.

Table of Contents

General Notes

There are a number of things to consider before beginning these lab exercises. Please read through this section completely, and perform any needed steps in order to ensure a successful workshop. These labs were designed for use with Incisive Unified Simulator82, IC613 and Assura32.

Before running any of these labs, ensure that you've set up IUS82, IC613, MMSIM71 and Assura32 correctly:

```
%> setenv CDSHOME <IC613-installation-home>
%> setenv MMSIMHOME <MMSIM71-installation-home>
%> setenv PVHOME <Assura32-installation-home>
%> setenv AMSHOME <IUS82-installation-home>
```

You will also need to ensure that the IUS82 is setup correctly for lab 5.

To setup the lab environment, please perform the following steps:

1. Ensure the software mentioned above is correctly setup.
2. Source the C-Shell related commands file i.e. (cshrc file).

These labs were designed to be run using Cadence Virtuoso tool and Assura tool.

Lab Getting Started

1. Log in to your workstation using the username and password.
The home directory has a **cshrc** file with paths to the Cadence installation.

2. In a terminal window, type **csh** at the command prompt to invoke the C shell.
>csh
>source cshrc

3. To verify that the path to the software is properly set in the **cshrc** file, type the below command in the terminal window and enter:
>which virtuoso

It gives the complete path of IC613 tool Installation.
>**which spectre**

It gives the complete path of MMSIM71 tool Installation.

>**which assura**

It gives the complete path of Assura32 tool Installation.

>which ncsim

It gives the complete path of IUS82 tool Installation.

Starting the Cadence Software

Use the installed database to do your work and the steps are as follows:

1. Change to the course directory by entering this command:
> **cd ~/Database/cadence_analog_labs_613**

You will start the Cadence Design Framework II environment from this directory because it contains cds.lib, which is the local initialization file. The library search paths are defined in this file.

The **Cadence_Analog_labs_613** directory contains Solutions folder and also Work folder. Inside Work folder you can create new cell / modifications of the cell locally without affecting your Source cell present inside Solutions directory.

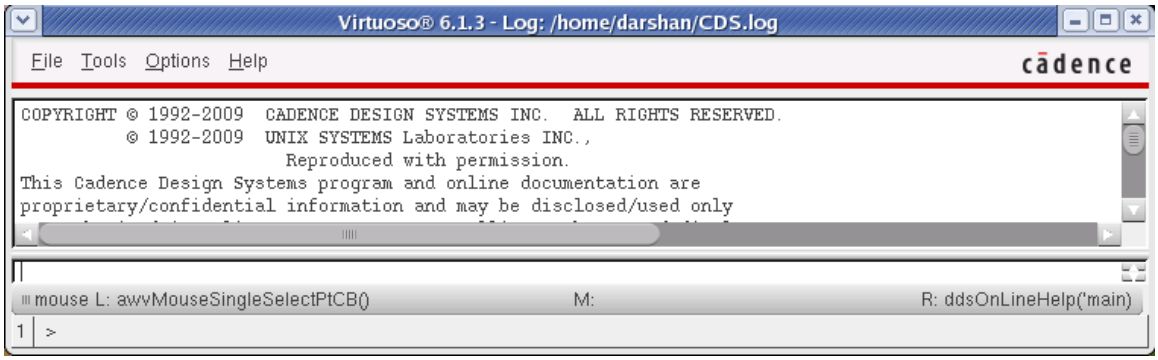
Lab directory details:

. /Solutions	Contains a local copy of all the lab experiments including test circuit for simulation.
. /libs.cdb	Contains a technology library for the design (gpdk180nm).
. /models	Contains spectre models of components for simulation in gpdk180nm technology.
. /stream	Contains layer map file for GDSII format
. /pv	Containing the Assura and Diva verification files
. /techfiles	Contains ASCII versions of the oa22 techfiles
. /dig_source	Contains verilog codes for SAR register and clock
. /cds.lib	File containing pointer to the Cadence OA22 initialization file**.**

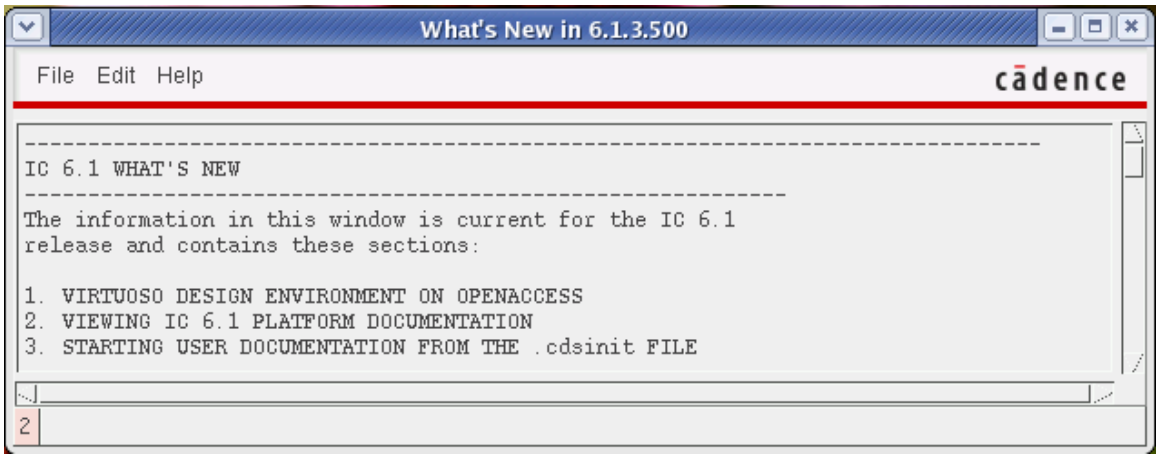
. /hdl.var File defines the work library for AMS simulation

. /docs Reference manual and user manual for gpdk180nm technology.

2. In the same terminal window, enter:
> **virtuoso &**
The virtuoso or Command Interpreter Window (CIW) appears at the bottom of the screen.



3. If the "What's New ..." window appears, close it with the **File— Close** command.

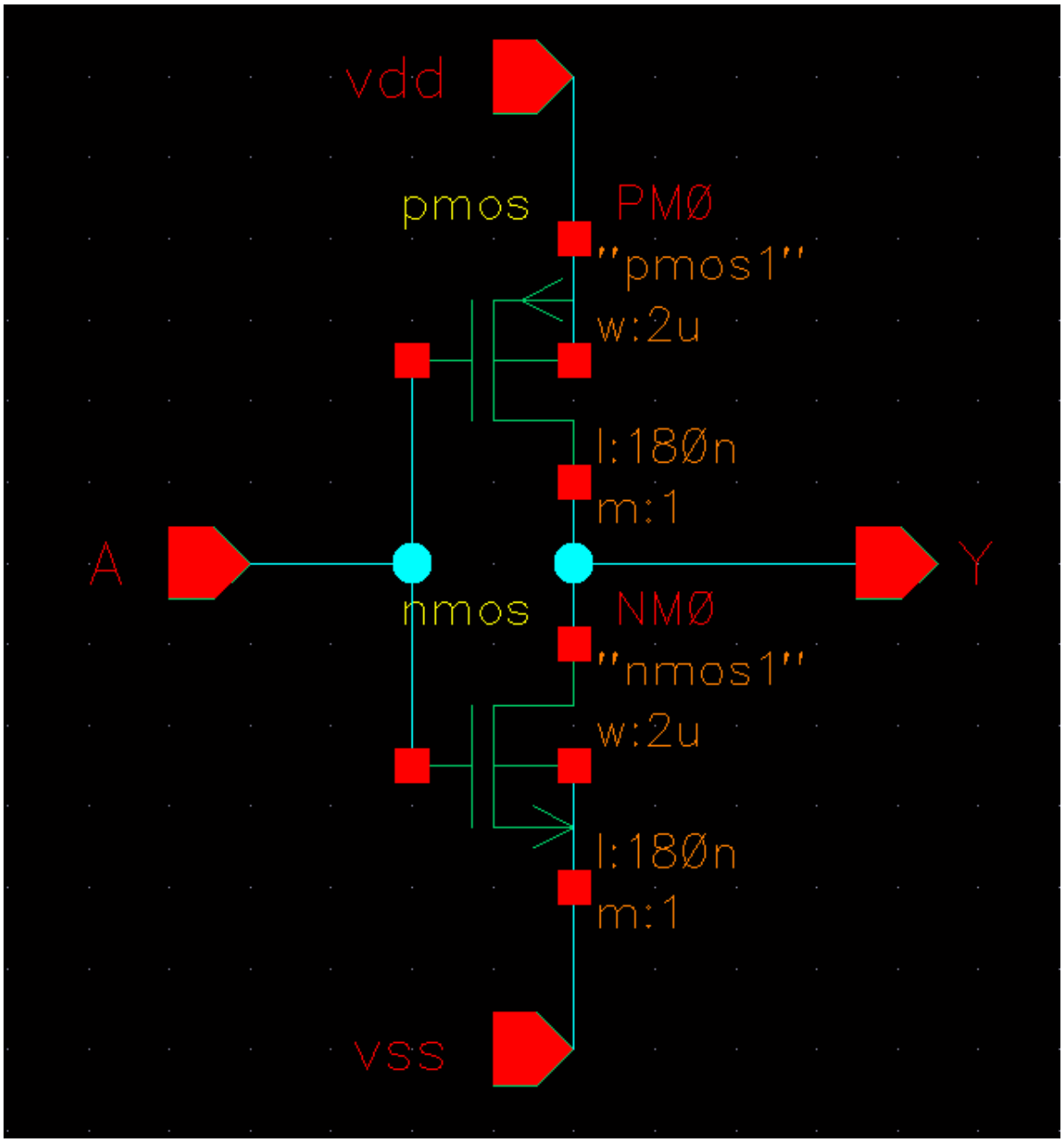


4. Keep opened CIW window for the labs.

End of General Notes

Lab 1: AN INVERTER

Schematic Capture



Schematic Entry

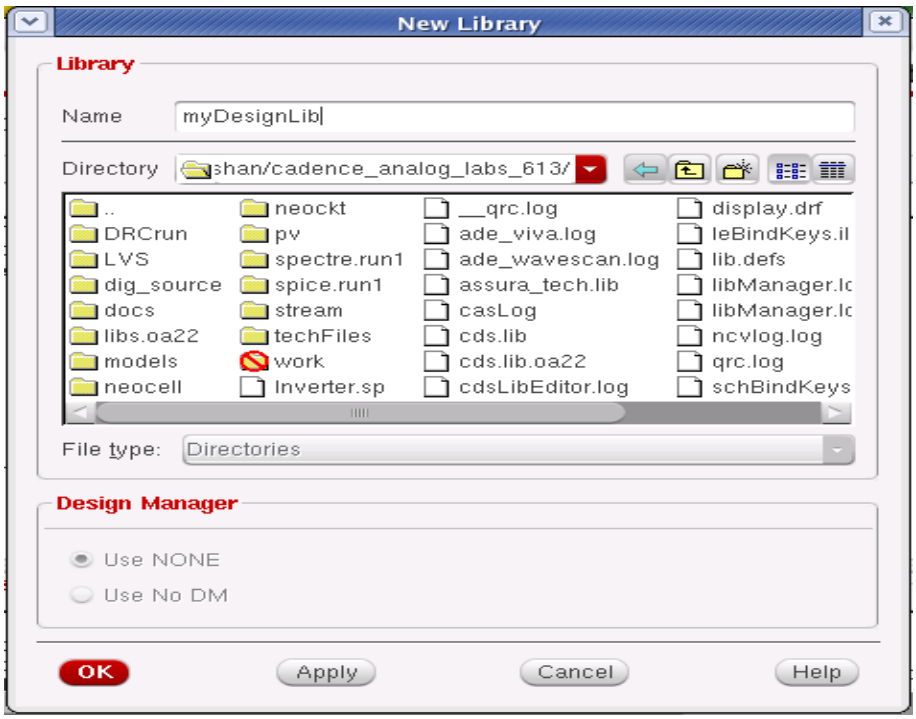
Objective: To create a library and build a schematic of an Inverter

Below steps explain the creation of new library "**myDesignLib**" and we will use the same throughout this course for building various cells that we going to create in the next labs. Execute **Tools – Library Manager** in the CIW or Virtuoso window to open Library Manager.

Creating a New library

1. In the Library Manager, execute **File - New – Library**. The new library form appears.

2. In the "New Library" form, type "**myDesignLib**" in the Name section.



4. In the field of Directory section, verify that the path to the library is set to **`~/Database/cadence_analog_labs_613`** and click **OK**.

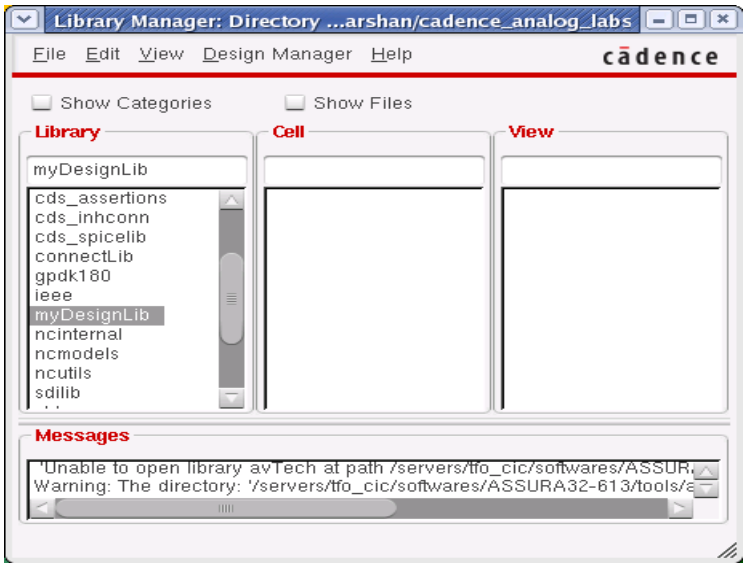
Note: A technology file is not required if you are not interested to do the layouts for the design

5. In the next "**Technology File for New library**" form, select option **Attach to an existing techfile** and click **OK**.

6. In the "**Attach Design Library to Technology File**" form, select **gpdk180** from the cyclic field and click **OK**.

7. After creating a new library you can verify it from the library manager.

8. If you right click on the "**myDesignLib**" and select properties, you will find that **gpdk180** library is attached as techlib to "**myDesignLib**".

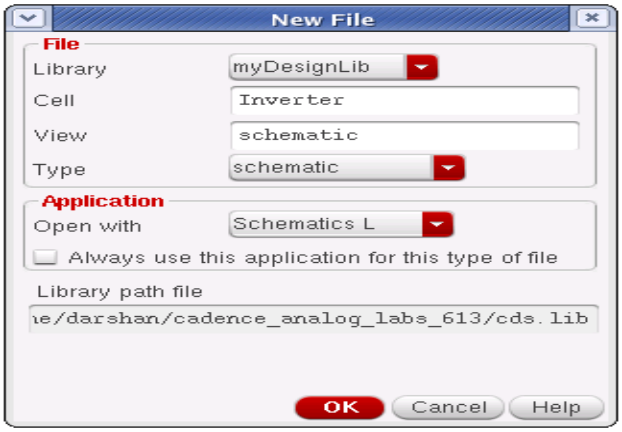


Creating a Schematic Cellview

In this section we will learn how to open new schematic window in the new "**myDesignLib**" library and build the inverter schematic as shown in the figure at the start of this lab.

1. In the CIW or Library manager, execute **File – New – Cellview**.

2. Set up the New file form as follows:



Do not edit the **Library path file** and the one above might be different from the path shown in your form.

3. Click **OK** when done the above settings. A blank schematic window for the **Inverter** design appears.

Adding Components to schematic

1. In the Inverter schematic window, click the **Instance** fixed menu icon to display the Add Instance form. 

Tip: You can also execute **Create — Instance** or press **i**.

2. Click on the **Browse** button. This opens up a Library browser from which you can select components and the **symbol** view .

You will update the Library Name, Cell Name, and the property values given in the table on the next page as you place each component.

3. After you complete the Add Instance form, move your cursor to the schematic window and click **left** to place a component.

This is a table of components for building the Inverter schematic.

Library name	**Cell Name**	**Properties/Comments**
gpdk180	pmos	For M0: Model name = pmos1, **W= wp**, L=180n
gpdk180	nmos	For M1: Model name = nmos1, W= 2u, L=180n

If you place a component with the wrong parameter values, use the **Edit— Properties— Objects** command to change the parameters. Use the **Edit— Move** command if you place components in the wrong location.

You can rotate components at the time you place them, or use the **Edit— Rotate** command after they are placed.

4. After entering components, click **Cancel** in the Add Instance form or press **Esc** with your cursor in the schematic window.

Adding pins to Schematic

1. Click the **Pin** fixed menu icon in the schematic window.

You can also execute **Create — Pin** or press ***p***.

The Add pin form appears.

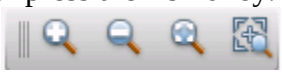
2. Type the following in the Add pin form in the exact order leaving space between the pin names.

Pin Names	**Direction**
vin	Input
vout	Output

Make sure that the direction field is set to **input/output/inputOutput** when placing the **input/output/inout** pins respectively and the Usage field is set to **schematic**.

3. Select **Cancel** from the Add – pin form after placing the pins.

In the schematic window, execute **Window— Fit** or press the **f** bindkey.



Adding Wires to a Schematic

Add wires to connect components and pins in the design.

1. Click the **Wire (narrow)** icon in the schematic window.

You can also press the ***w*** key, or execute **Create — Wire (narrow).**

2. In the schematic window, click on a pin of one of your components as the first point for your wiring. A diamond shape appears over the starting point of this wire.

3. Follow the prompts at the bottom of the design window and click **left** on the destination point for your wire. A wire is routed between the source and destination points.

4. Complete the wiring as shown in figure and when done wiring press **ESC** key in the schematic window to cancel wiring.

Saving the Design

1. Click the ***Check and Save*** icon in the schematic editor window.

2. Observe the CIW output area for any errors.

Symbol Creation

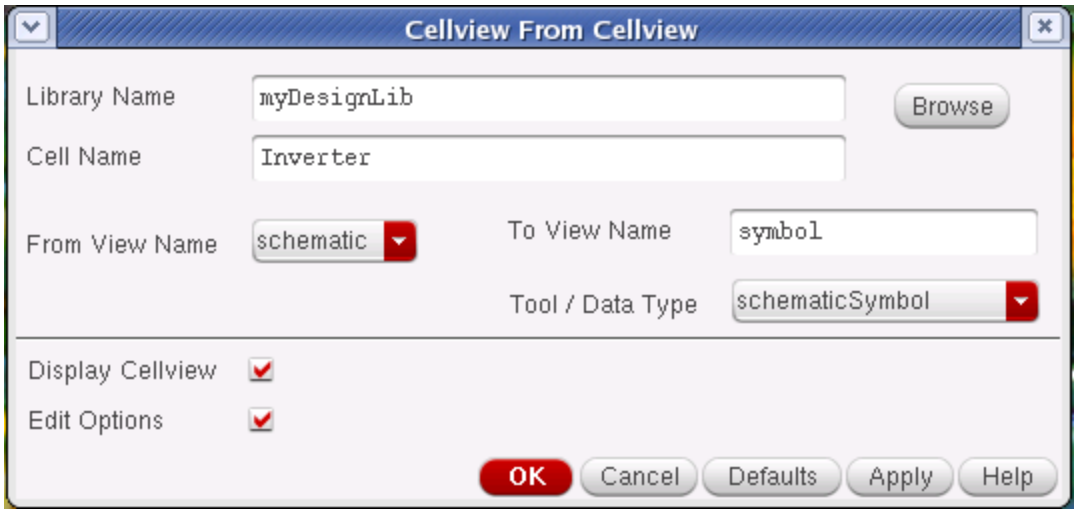
Objective: To create a symbol for the Inverter

In this section, you will create a symbol for your inverter design so you can place it in a test circuit for simulation. A symbol view is extremely important step in the design process. The symbol view must exist for the schematic to be used in a hierarchy. In addition, the symbol has attached properties (cdsParam) that facilitate the simulation and the design of the circuit.

1. In the Inverter schematic window, execute
Create — Cellview— From Cellview.

The **Cellview From Cellview** form appears. With the Edit Options function active, you can control the appearance of the symbol to generate.

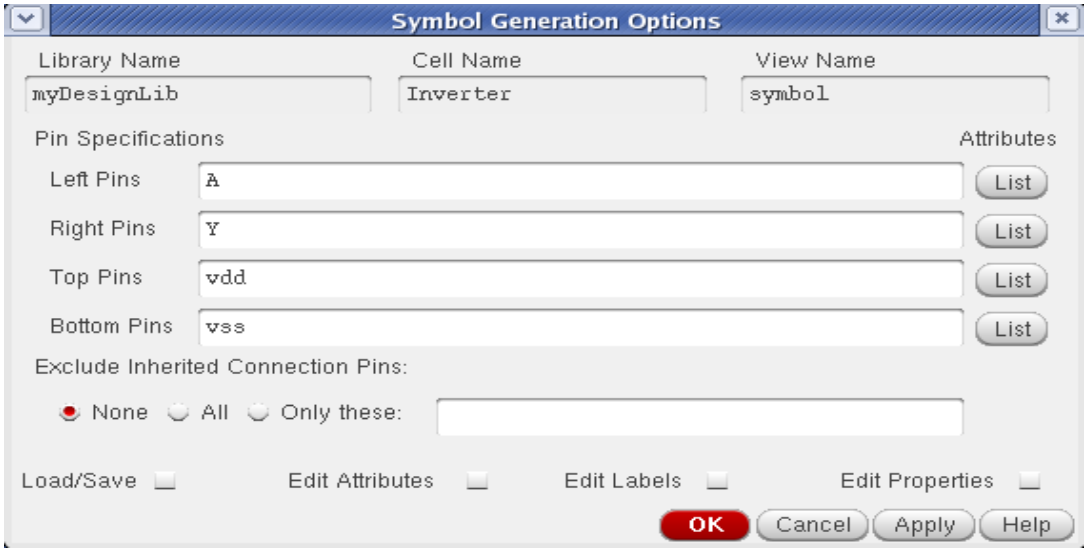
2. Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is set to **symbol**, with the **Tool/Data Type** set as **SchematicSymbol**.



3. Click **OK** in the **Cellview From Cellview** form.

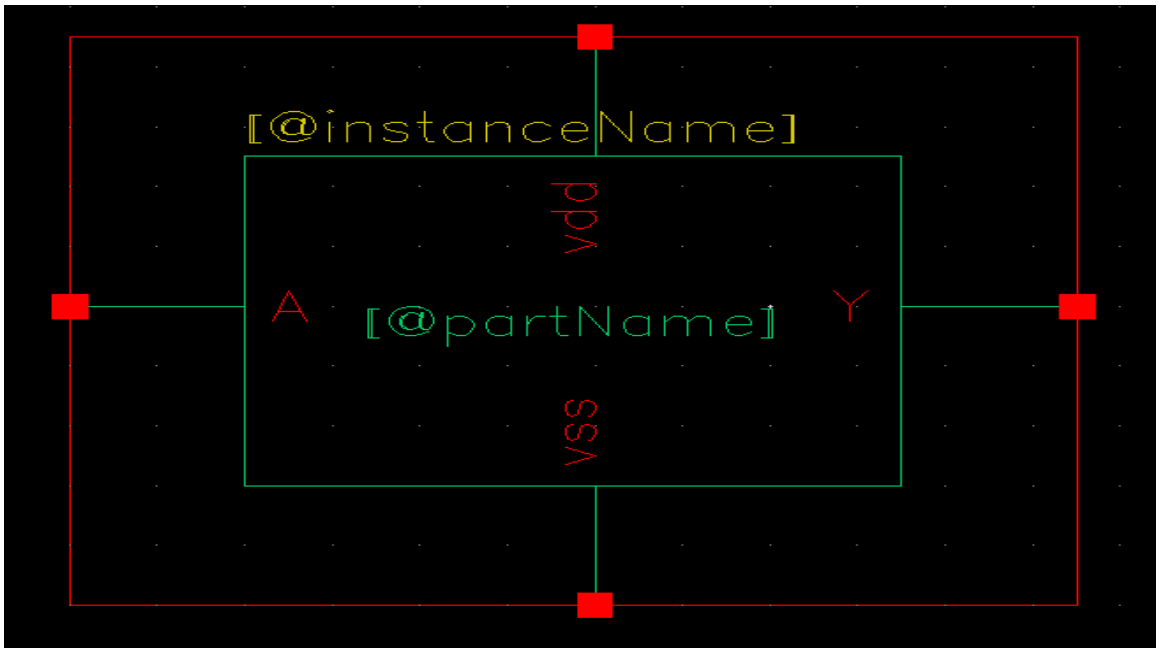
The Symbol Generation Form appears.

4. Modify the **Pin Specifications** as follows:



5. Click **OK** in the Symbol Generation Options form.

6. A new window displays an automatically created Inverter symbol as shown here.



Editing a Symbol

In this section we will modify the inverter symbol to look like a Inverter gate symbol.

1. Move the cursor over the automatically generated symbol, until the green rectangle is highlighted, click **left** to select it.

2. Click **Delete** icon in the symbol window, similarly select the red rectangle and delete that.

3. Execute **Create – Shape – polygon**, and draw a shape similar to triangle.

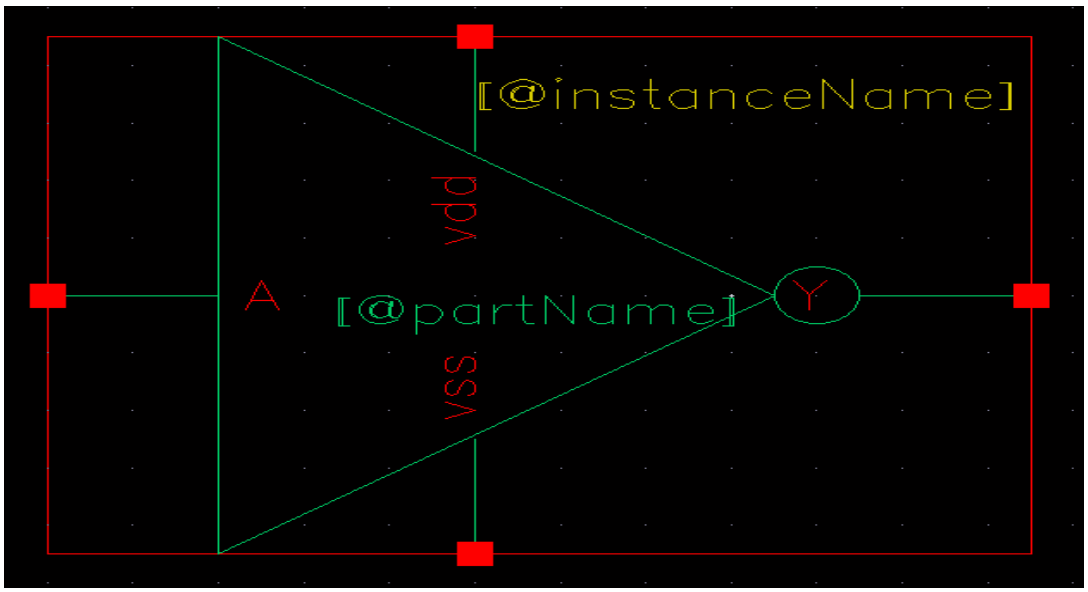
4. After creating the triangle press ***ESC*** key.

5. Execute **Create – Shape – Circle** to make a circle at the end of triangle.

6. You can move the pin names according to the location.

7. Execute **Create — Selection Box**. In the Add Selection Box form, click **Automatic**. A new red selection box is automatically added.

8. After creating symbol, click on the ***save*** icon in the symbol editor window to save the symbol. In the symbol editor, execute **File — Close** to close the symbol view window.



Building the Inverter_Test Design

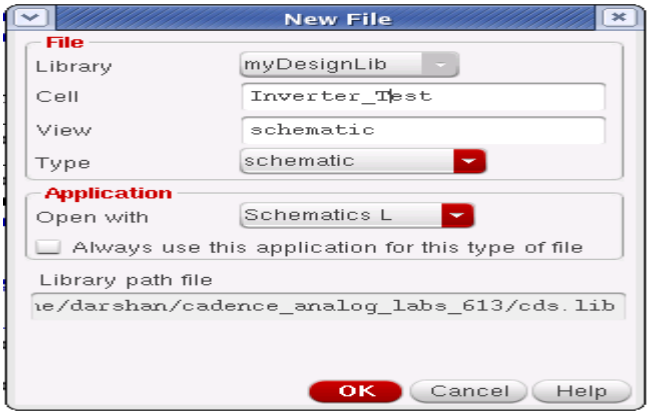
Objective: To build an Inverter Test circuit using your Inverter

Creating the Inverter_Test Cellview

You will create the Inverter_Test cellview that will contain an instance of the Inverter cellview. In the next section, you will run simulation on this design

1. In the CIW or Library Manager, execute **File— New— Cellview**.

2. Set up the New File form as follows:



3. Click **OK** when done. A blank schematic window for the **Inverter_Test** design appears.

Building the Inverter_Test Circuit

1. Using the component list and Properties/Comments in this table, build the **Inverter_Test** schematic.

Library name	Cellview name	Properties/Comments
myDesignLib	Inverter	Symbol
analogLib	vpulse	v1=0, v2=1.8,td=0 tr=tf=1ns, ton=10n, T=20n
analogLib	vdc, gnd	vdc=1.8

Note: Remember to set the values for **VDD** and **VSS**. Otherwise, your circuit will have no power.

2. Add the above components using **Create — Instance** or by pressing **I**.

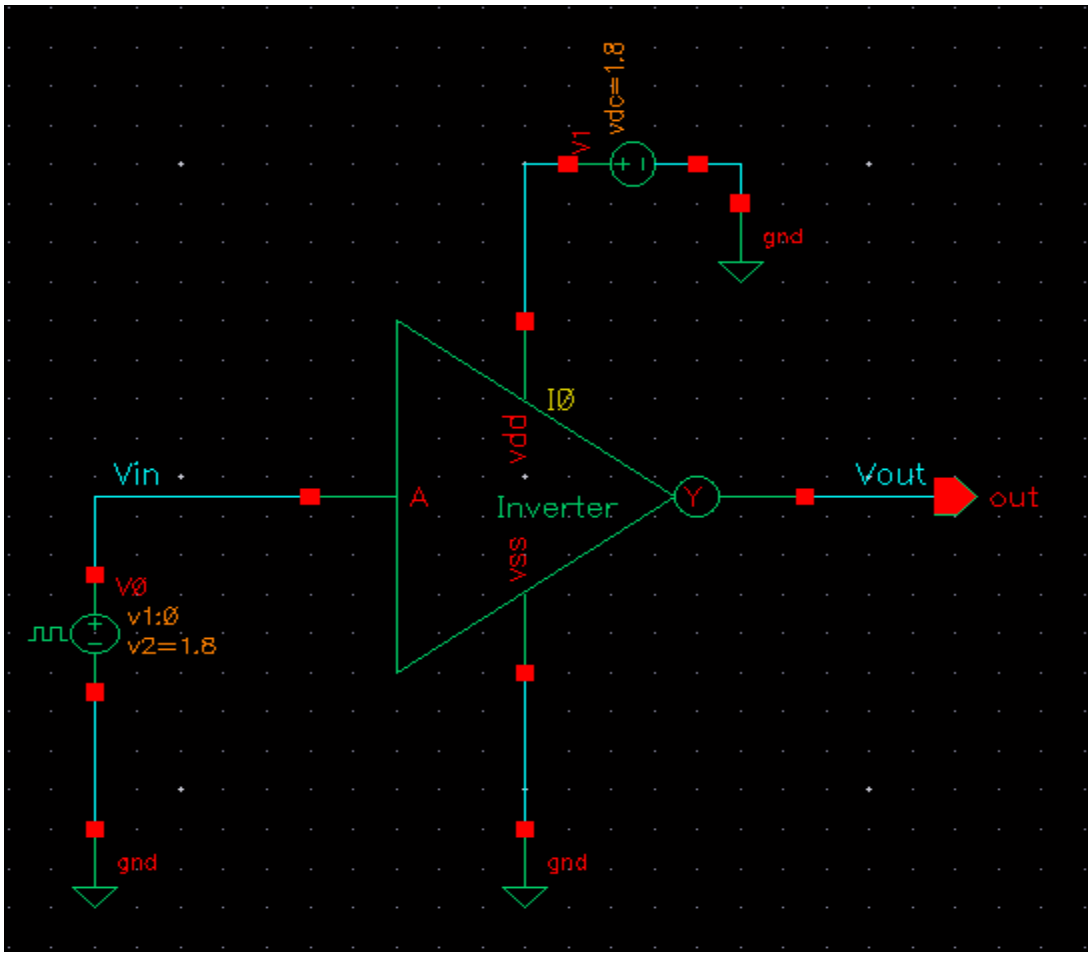
3. Click the **Wire (narrow)** icon and wire your schematic.

Tip: You can also press the **w** key, or execute **Create— Wire (narrow)**.

4. Click **Create — Wire Name** or press **L** to name the input **(Vin)** and output **(Vout)** wires as in the below schematic.

4. Click on the ***Check and Save*** icon to save the design.

5. The schematic should look like this.



6. Leave your **Inverter_Test** schematic window open for the next section.

Analog Simulation with Spectre

Objective: To set up and run simulations on the Inverter_Test design

In this section, we will run the simulation for Inverter and plot the transient, DC characteristics and we will do Parametric Analysis after the initial simulation.

Starting the Simulation Environment

Start the Simulation Environment to run a simulation.

1. In the **Inverter_Test** schematic window, execute
Launch – ADE L

The **Virtuoso Analog Design Environment (ADE)** simulation window appears.

Choosing a Simulator

Set the environment to use the **Spectre® tool**, a high speed, highly accurate analog simulator. Use this simulator with the **Inverter*_Test*** design, which is made-up of analog components.

1. In the simulation window (ADE), execute
Setup— Simulator/Directory/Host.

2. In the Choosing Simulator form, set the Simulator field to **spectre** (Not spectreS) and click **OK**.

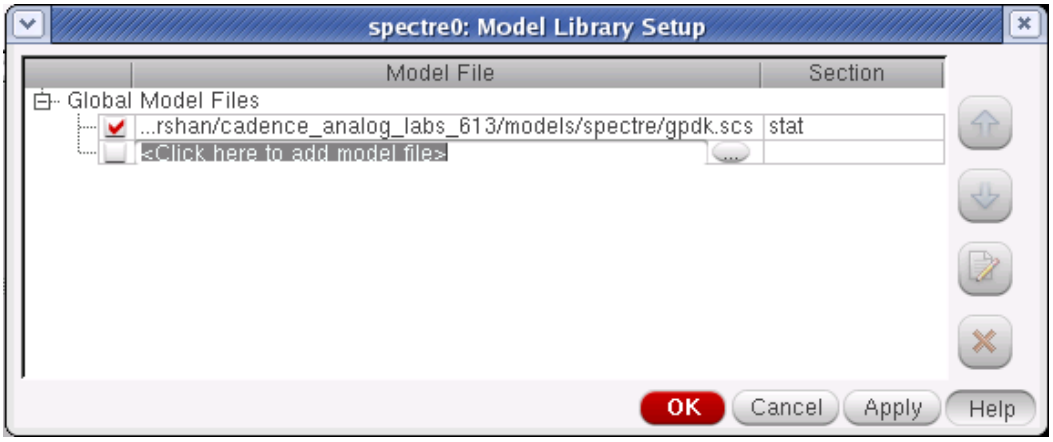
Setting the Model Libraries

The Model Library file contains the model files that describe the nmos and pmos devices during simulation.

1. In the simulation window (ADE),
Execute **Setup - Model Libraries.**

The Model Library Setup form appears. Click the **browse** button  to add **gpdk.scs** if not added by default as shown in the **Model Library Setup** form. Remember to select the section type as **stat** in front of the gpdk.scs file.

Your Model Library Setup window should now looks like the below figure.



To view the model file, highlight the expression in the Model Library File field and Click **Edit File**.

2. To complete the Model Library Setup, move the cursor and click **OK**.

The Model Library Setup allows you to include multiple model files.
It also allows you to use the Edit button to view the model file.

Choosing Analyses

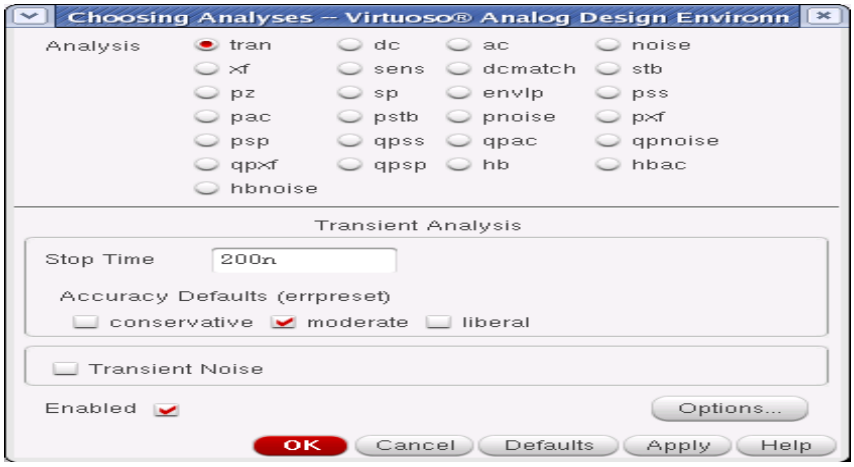
This section demonstrates how to view and select the different types of analyses to complete the circuit when running the simulation.

1. In the Simulation window (ADE), click the **Choose - Analyses** icon.
You can also execute **Analyses - Choose.**

The Choosing Analysis form appears. This is a dynamic form, the bottom of the form changes based on the selection above.

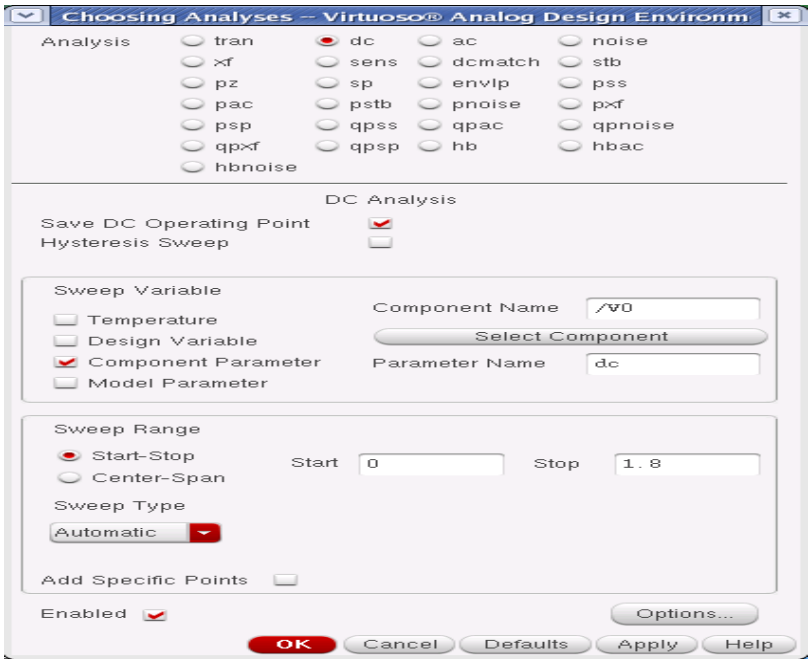
2. To setup for transient analysis

a. In the Analysis section select **tran**
b. Set the stop time as **200n**
c. Click at the **moderate** or **Enabled** button at the bottom, and then click **Apply**.



3. To set up for DC Analyses:

a. In the Analyses section, select **dc**.
b. In the DC Analyses section, turn on **Save DC Operating Point.**
c. Turn on the **Component Parameter**.
d. Double click the **Select Component**, Which takes you to the schematic window.
e. Select input signal **vpulse source** in the test schematic window.
f. Select **"DC Voltage"** in the **Select Component Parameter** form and click OK.
f. In the analysis form type **start** and **stop** voltages as **0** to **1.8** respectively.
g. Check the enable button and then click **Apply.**



4. Click ***OK*** in the Choosing Analyses Form.

Setting Design Variables

Set the values of any design variables in the circuit before simulating.
Otherwise, the simulation will not run.

1. In the Simulation window, click the **Edit Variables** icon.
The Editing Design Variables form appears.

2. Click **Copy From** at the bottom of the form.
The design is scanned and all variables found in the design are listed.
In a few moments, the **wp** variable appears in the Table of Design variables section.

3. Set the value of the **wp** variable:
With the **wp** variable highlighted in the Table of Design Variables,
click on the variable name **wp** and enter the following:

Value(Expr)	2u

Click **Change** and notice the update in the Table of Design Variables.

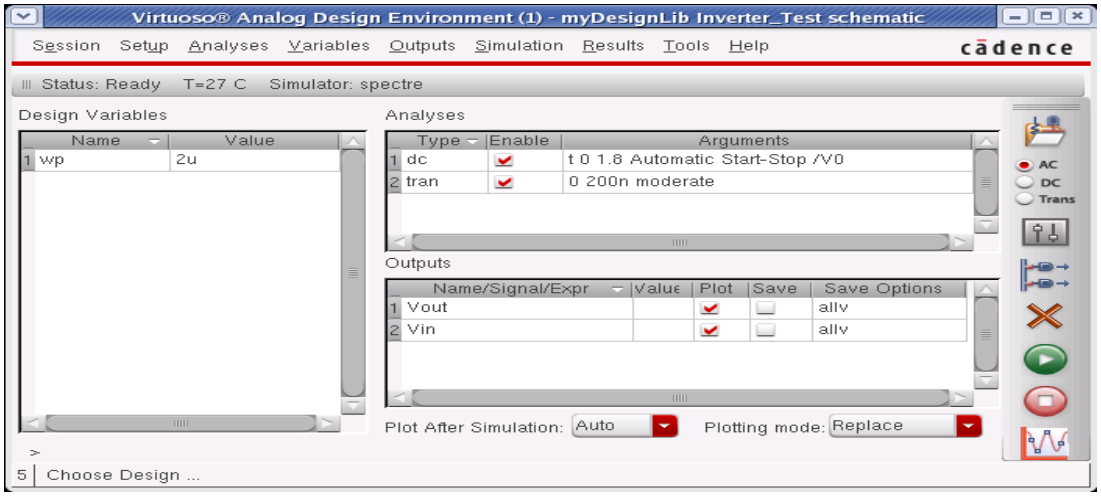
3. Click **OK** or **Cancel** in the Editing Design Variables window.

Selecting Outputs for Plotting

1. Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.

2. Follow the prompt at the bottom of the schematic window, Click on output net **Vout**, input net **Vin** of the Inverter. Press **ESC** with the cursor in the schematic after selecting it.

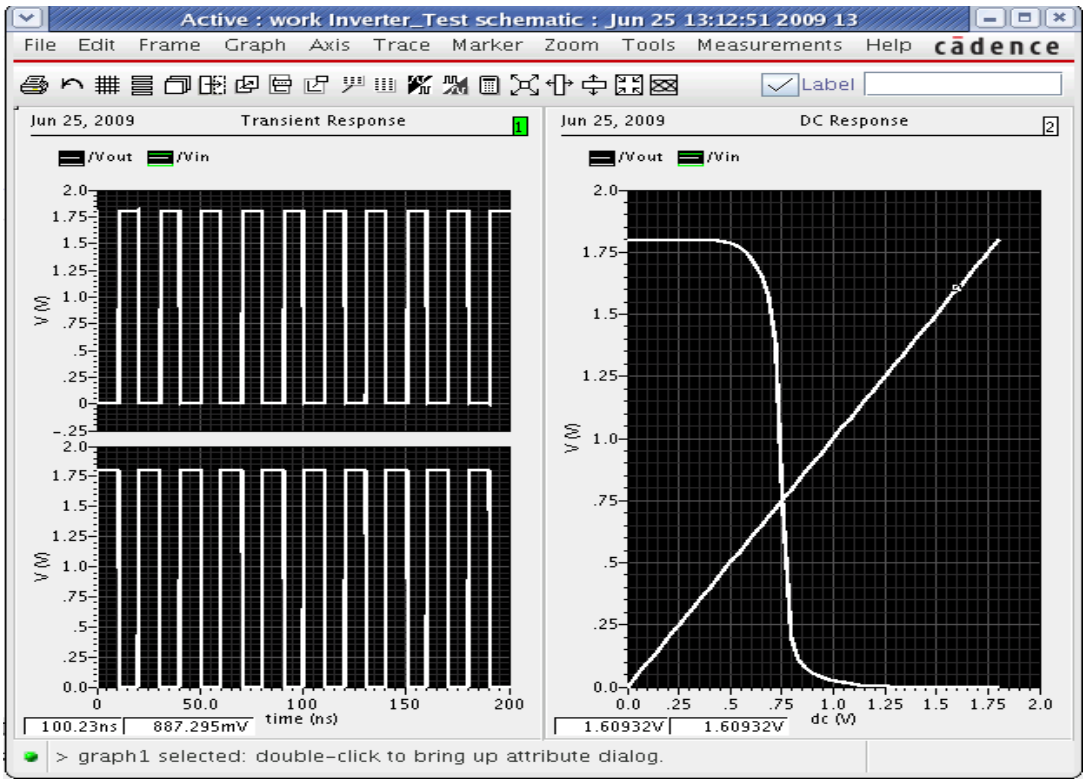
Does the simulation window look like this?



Running the Simulation

1. Execute **Simulation – Netlist and Run** in the simulation window to start the Simulation or the icon, this will create the netlist as well as run the simulation.

2. When simulation finishes, the Transient, DC plots automatically will be popped up along with log file.



Saving the Simulator State

We can save the simulator state, which stores information such as model library file, outputs, analysis, variable etc. This information restores the simulation environment without having to type in all of setting again.

1. In the Simulation window, execute **Session – Save State**.
The Saving State form appears.

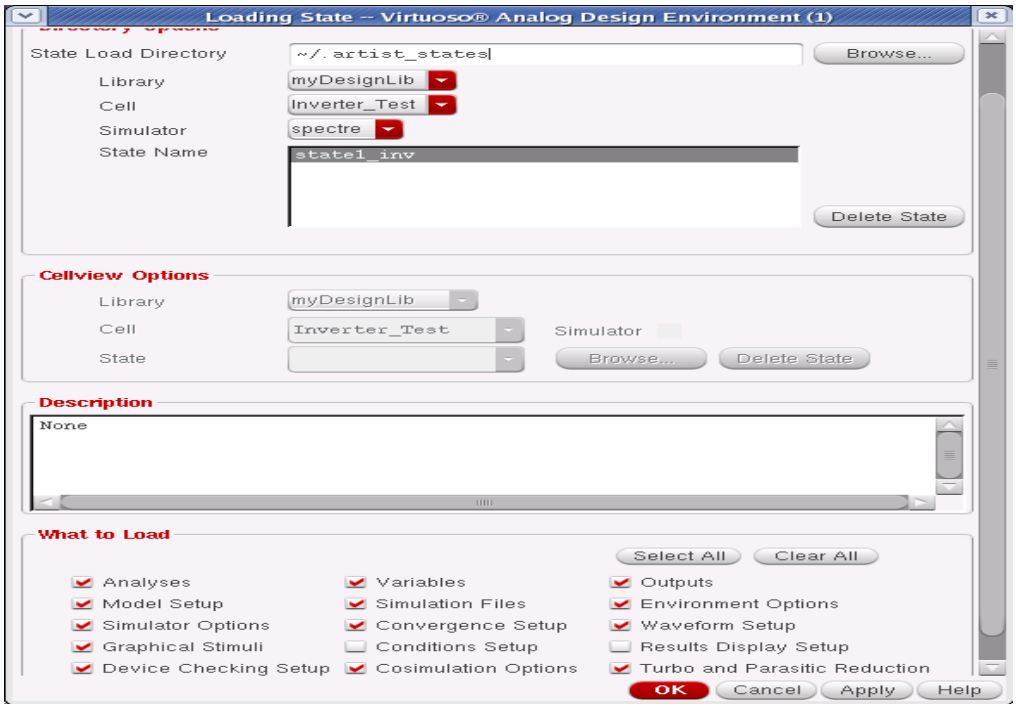
2. Set the **Save as** field to **state1_inv** and make sure all options are selected under what to save field.

3. Click **OK** in the saving state form. The Simulator state is saved.

Loading the Simulator State

1. From the ADE window execute **Session – Load State.**

2. In the Loading State window, set the State name to **state1_inv** as shown



3. Click **OK** in the Loading State window.

Parametric Analysis

Parametric Analysis yields information similar to that provided by the Spectre® sweep feature, except the data is for a full range of sweeps for each parametric step. The Spectre sweep feature provides sweep data at only one specified condition.

You will run a parametric DC analysis on the **wp** variable, of the PMOS device of the Inverter design by sweeping the value of **wp**.

Run a simulation before starting the parametric tool. You will start by loading the state from the previous simulation run.

Run the simulation and check for errors. When the simulation ends, a single waveform in the waveform window displays the DC Response at the **Vout** node.

Starting the Parametric Analysis Tool

1. In the Simulation window, execute **Tools—Parametric Analysis**.
The Parametric Analysis form appears.

2. In the Parametric Analysis form, execute
Setup—Pick Name For Variable—Sweep 1.

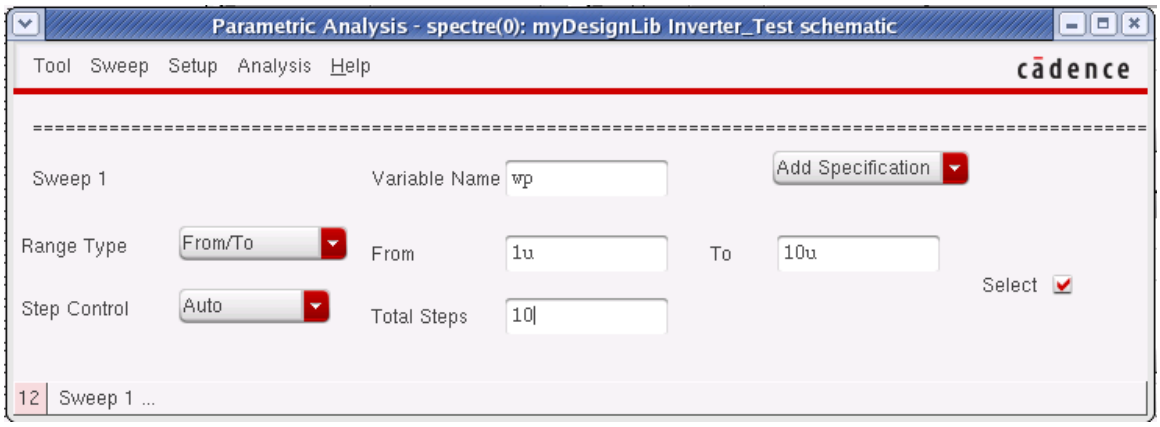
A selection window appears with a list of all variables in the design that you can sweep. This list includes the variables that appear in the Design Variables section of the Simulation window.

3. In the selection window, double click left on **wp**.
The Variable Name field for Sweep 1 in the Parametric Analysis form is set to **wp**.

4. Change the Range Type and Step Control fields in the Parametric Analysis form as shown below:

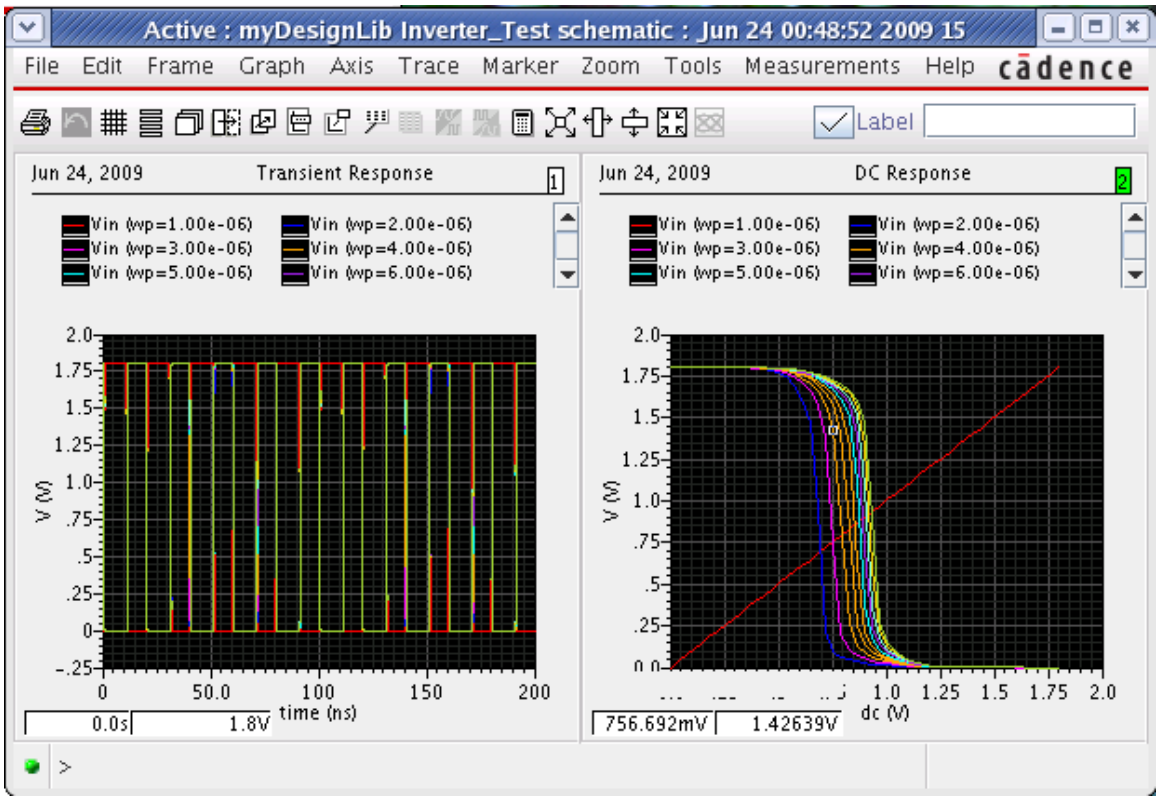
Range Type	**From/To**	From	**1u**	To	**10u**
Step Control	**Auto**	Total Steps	**10**		

These numbers vary the value of the **wp** of the pmos between 1um and 10um at ten evenly spaced intervals.



5. Execute **Analysis—Start**.

The Parametric Analysis window displays the number of runs remaining in the analysis and the current value of the swept variable(s). Look in the upper right corner of the window. Once the runs are completed the wavescan window comes up with the plots for different runs.



Note: Change the wp value of pmos device back to 2u and save the schematic before proceeding to the next section of the lab. To do this use edit property option.

Creating Layout View of Inverter

1. From the **Inverter** schematic window menu execute **Launch – Layout XL**. A **Startup Option** form appears.

2. Select ***Create New*** option. This gives a New Cell View Form

3. Check the Cellname **(Inverter)**, Viewname **(layout).**

4. Click **OK** from the New Cellview form.

LSW and a blank layout window appear along with schematic window.

Adding Components to Layout

1. Execute **Connectivity – Generate – All from Source** or click the icon  in the layout editor window, **Generate Layout** form appears. Click **OK** which imports the schematic components in to the Layout window automatically.

2. Re arrange the components with in PR-Boundary as shown in the next page.

3. To rotate a component, Select the component and execute **Edit –Properties**. Now select the degree of rotation from the property edit form.

4. To Move a component, Select the component and execute **Edit -Move** command.

Making interconnection

1. Execute **Connectivity –Nets – Show/Hide selected Incomplete Nets** or click  the icon in the Layout Menu.

2. Move the mouse pointer over the device and click **LMB** to get the connectivity information, which shows the guide lines (or flight lines) for the inter connections of the components.

3. From the layout window execute **Create – Shape – Path/ Create wire** or **Create – Shape – Rectangle (**for vdd and gnd bar**)** and select the appropriate Layers from the **LSW** window and Vias for making the inter connections

Creating Contacts/Vias

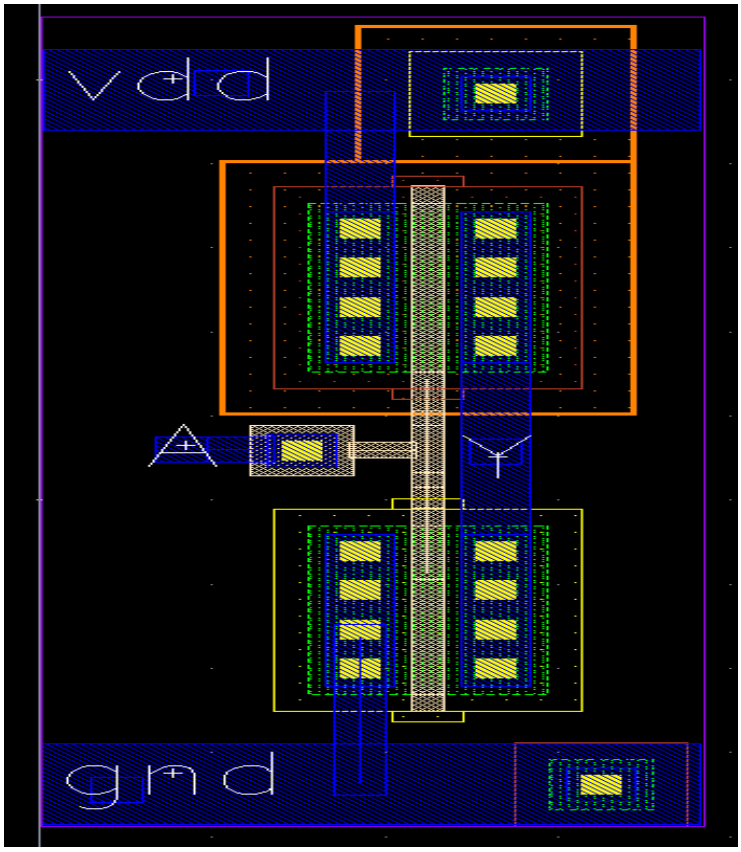
You will use the contacts or vias to make connections between two different layers.

1. Execute **Create — Via** or select  command to place different Contacts, as given in below table

Connection	Contact Type
For Metal1- Poly Connection	Metal1-Poly
For Metal1- Psubstrate Connection	Metal1-Psub
For Metal1- Nwell Connection	Metal1-Nwell

Saving the design

1. Save your design by selecting **File — Save** or click  to save the layout, and layout should appear as below.



Physical Verification

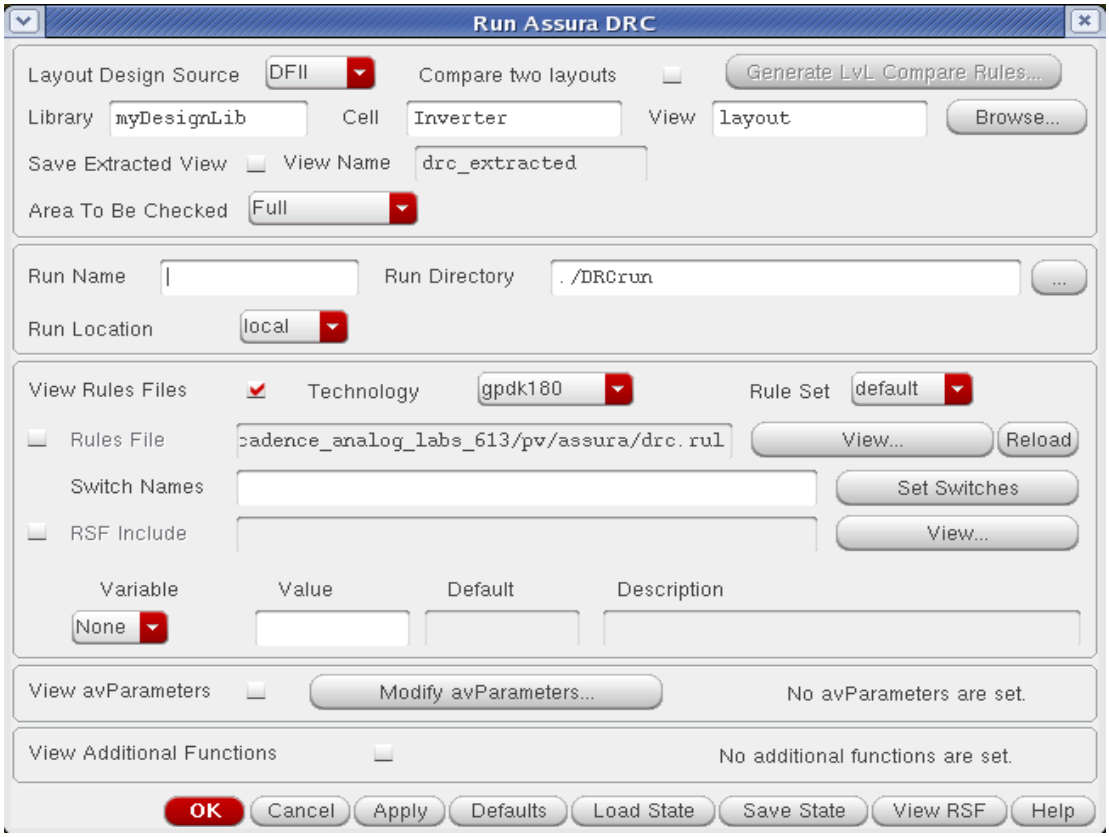
Assura DRC

Running a DRC

1. Open the Inverter layout form the CIW or library manger if you have closed that. Press **shift – f** in the layout window to display all the levels.

2. Select **Assura - Run DRC** from layout window.

The DRC form appears. The Library and Cellname are taken from the current design window, but rule file may be missing. Select the Technology as **gpdk180.** This automatically loads the rule file.
Your DRC form should appear like this



3. Click **OK** to start DRC.

4. A Progress form will appears. You can click on the watch log file to see the log file.

5. When DRC finishes, a dialog box appears asking you if you want to view your DRC results, and then click **Yes** to view the results of this run.

6. If there any DRC error exists in the design **View Layer Window** (VLW) and **Error Layer Window** (ELW) appears. Also the errors highlight in the design itself.

7. Click **View – Summary** in the ELW to find the details of errors.

8. You can refer to rule file also for more information, correct all the DRC errors and **Re – run** the DRC.

9. If there are no errors in the layout then a dialog box appears with **No DRC errors found** written in it, click on **close** to terminate the DRC run.

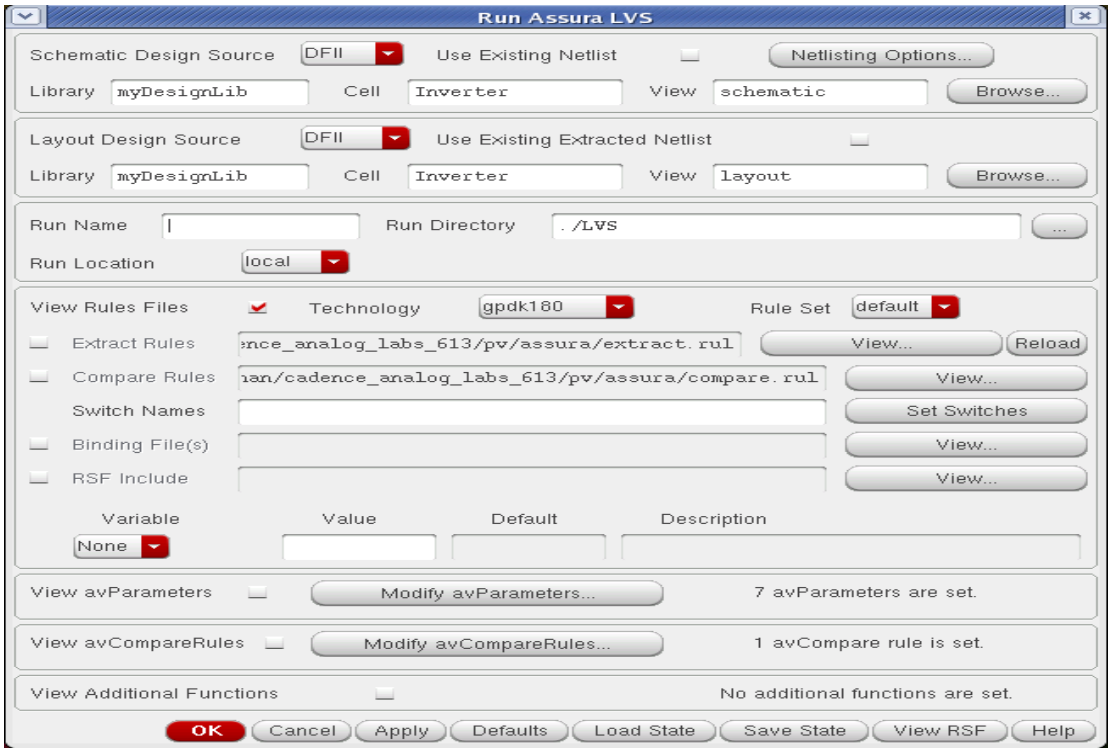
ASSURA LVS

In this section we will perform the LVS check that will compare the schematic netlist and the layout netlist.

Running LVS

1. Select **Assura – Run LVS** from the layout window.
The Assura Run LVS form appears. It will automatically load both the schematic and layout view of the cell.

2. Change the following in the form and click **OK**.



3. The LVS begins and a Progress form appears.

4. If the schematic and layout matches completely, you will get the form displaying **Schematic and Layout Match**.

5. If the schematic and layout do not matches, a form informs that the LVS completed successfully and asks if you want to see the results of this run.

6. Click **Yes** in the form.
LVS debug form appears, and you are directed into LVS debug environment.
7. In the **LVS debug form** you can find the details of mismatches and you need to correct all those mismatches and **Re – run** the LVS till you will be able to match the

schematic with layout.

Assura RCX

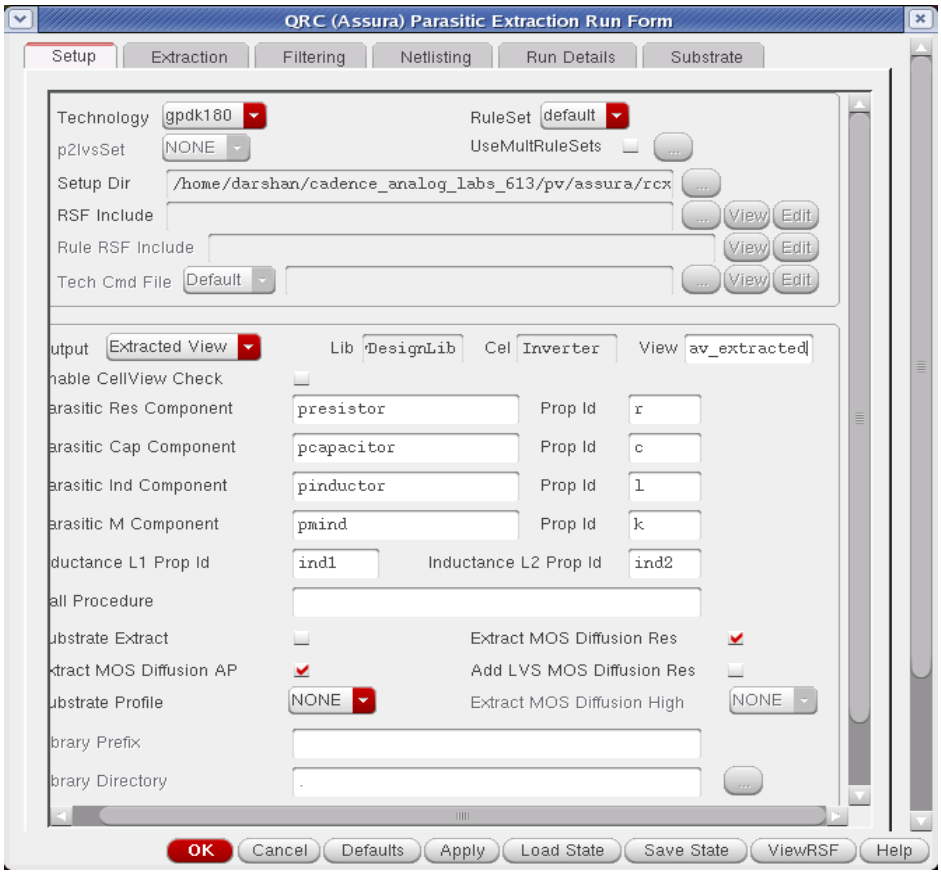
In this section we will extract the RC values from the layout and perform analog circuit simulation on the designs extracted with RCX.

Before using RCX to extract parasitic devices for simulation, the layout should match with schematic completely to ensure that all parasites will be backannoted to the correct schematic nets.

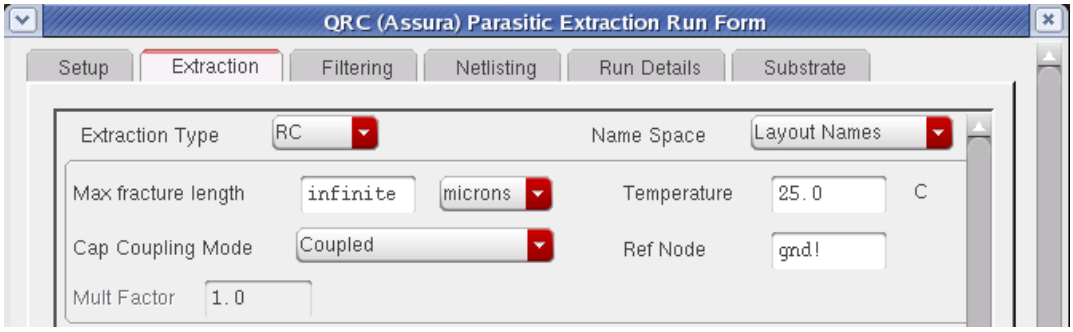
Running RCX

1. From the layout window execute **Assura – Run RCX**.

2. Change the following in the Assura parasitic extraction form. Select **output** type under **Setup** tab of the form.



3. In the **Extraction** tab of the form, choose Extraction type, Cap Coupling Mode and specify the Reference node for extraction.



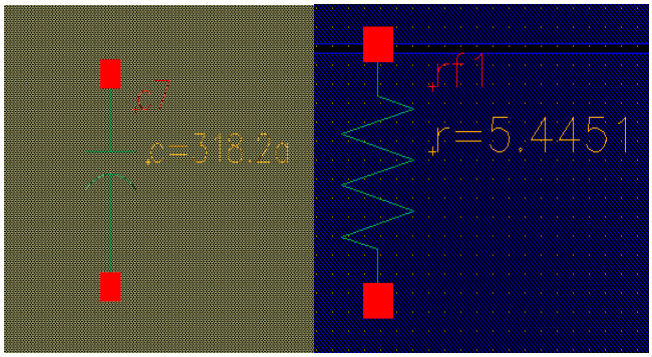
4. In the **Filtering** tab of the form, **Enter Power Nets** as **vdd!, vss!** and **Enter Ground Nets** as **gnd!**

5. Click **OK** in the Assura parasitic extraction form when done.

The RCX progress form appears, in the progress form click **Watch log file** to see the output log file.

5. When RCX completes, a dialog box appears, informs you that **Assura RCX run Completed successfully.**

6. You can open the **av_extracted** view from the library manager and view the parasitic.

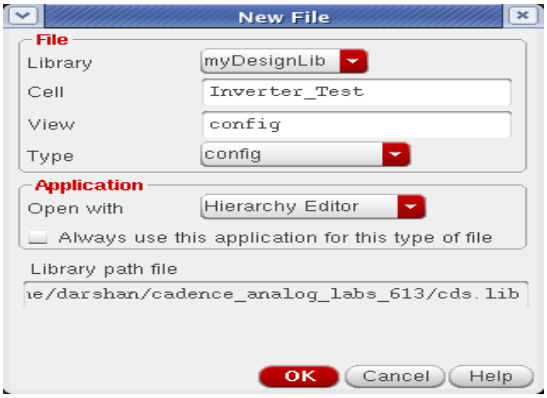


Creating the Configuration View

In this section we will create a config view and with this config view we will run the simulation with and without parasitic.

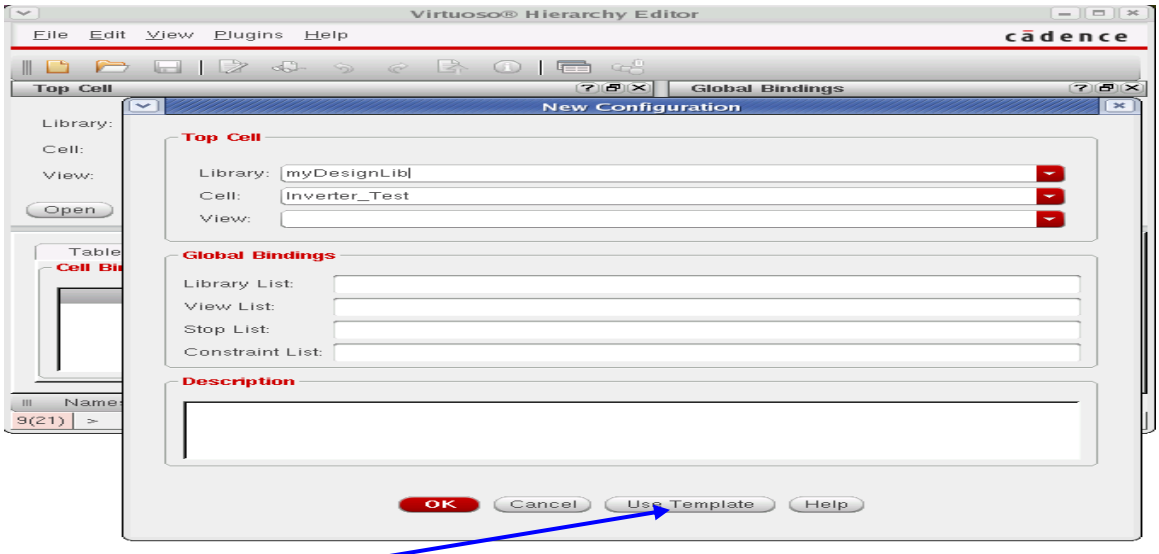
1. In the CIW or Library Manager, execute **File – New – Cellview**

2. In the Create New file form, set the following:



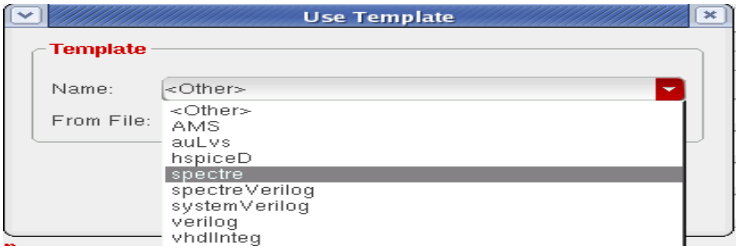
3. Click **OK** in create **New File** form.

The **Hierarchy Editor** form opens and a **New Configuration** form opens in front of it.



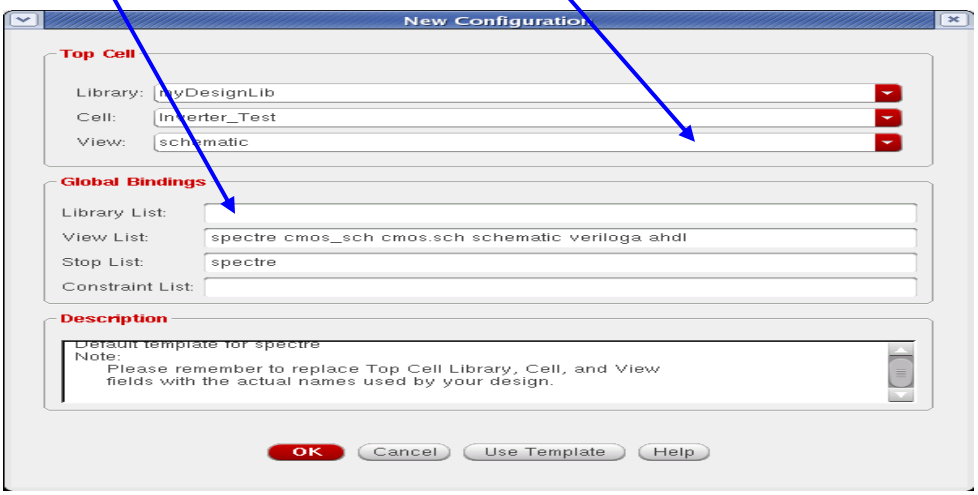
4. Click **Use template** at the bottom of the **New Configuration** form and select **Spectre** in the cyclic field and click **OK**.

The Global Bindings lists are loaded from the template.

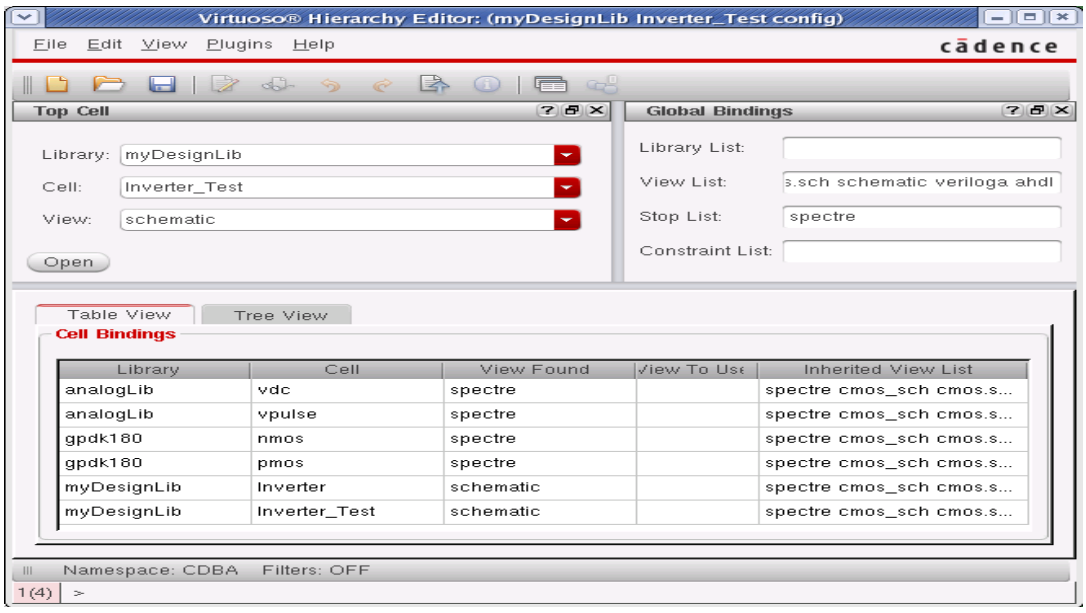


5. Change the **Top Cell** View to **schematic** and remove the default entry from the **Library List** field.

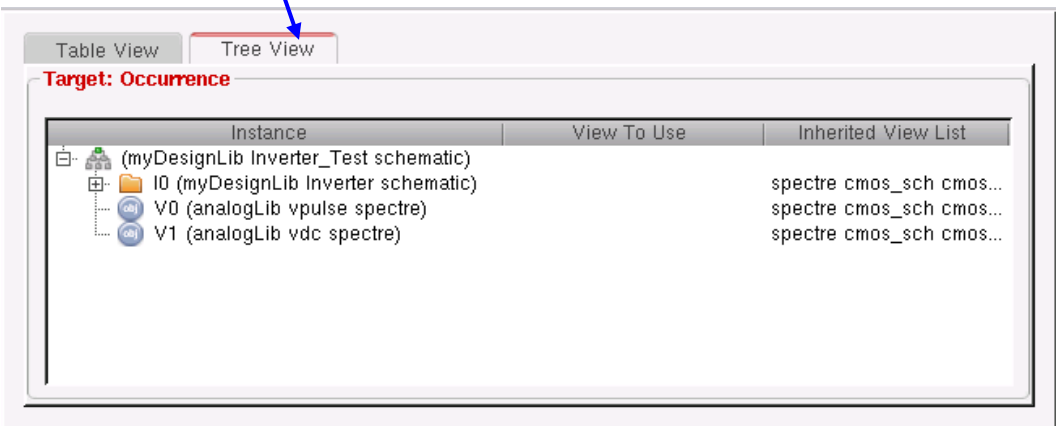
6. Click **OK** in the New Configuration form.



The hierarchy editor displays the hierarchy for this design using table format.



7. Click the **Tree View** tab. The design hierarchy changes to tree format. The form should look like this:

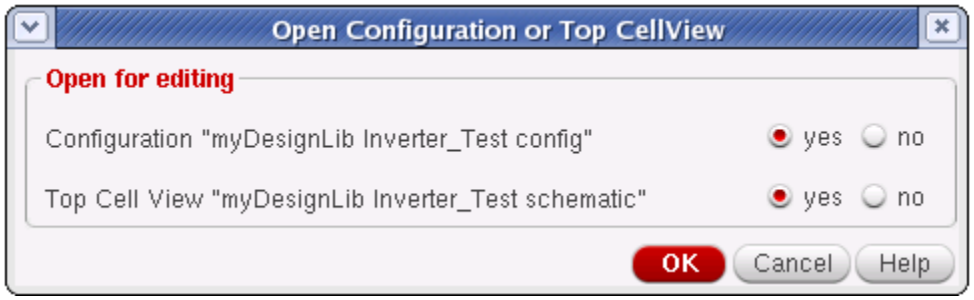


8. ***Save*** the current configuration. 

9. Close the Hierarchy Editor window. Execute **File – Close Window**.

To run the Circuit without Parasites

1. From the Library Manager open **Inverter_Test** Config view.
Open Configuration or Top cellview form appears.



2. In the form, turn on the both cyclic buttons to **Yes** and click **OK.**
The Inverter_Test schematic and Inverter_Test config window appears. Notice the window banner of schematic also states **Config: myDesignLib Inverter_Test config.**

3. Execute **Launch – ADE L** from the schematic window.

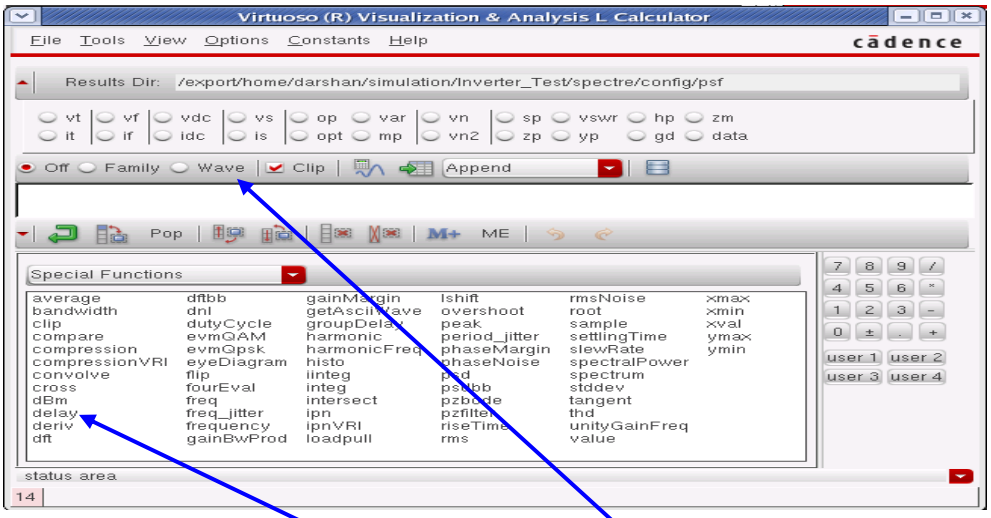
4. Now you need to follow the same procedure for running the simulation. Executing **Session– Load state,** the Analog Design Environment window loads the previous state.

5. Click **Netlist and Run** icon to start the simulation. 
The simulation takes a few seconds and then waveform window appears.

6. In the CIW, note the netlisting statistics in the **Circuit inventory** section. This list includes all nets, designed devices, source and loads. There are no parasitic components. Also note down the circuit inventory section.

Measuring the Propagation Delay

1. In the waveform window execute **Tools – Calculator.** 
The calculator window appears.



2. From the functions select **delay,** this will open the delay data panel.

3. Place the cursor in the text box for Signal1, select the **wave** button and select the input waveform from the waveform window.

4. Repeat the same for Signal2, and select the output waveform.

5. Set the **Threshold value 1** and **Threshold value 2** to 0.9, this directs the calculator to calculate delay at 50% i.e. at 0.9 volts.

6. Execute **OK** and observe the expression created in the calculator buffer.

7. Click on **Evaluate the buffer icon**  to perform the calculation, note down the value returned after execution.

8. Close the calculator window.

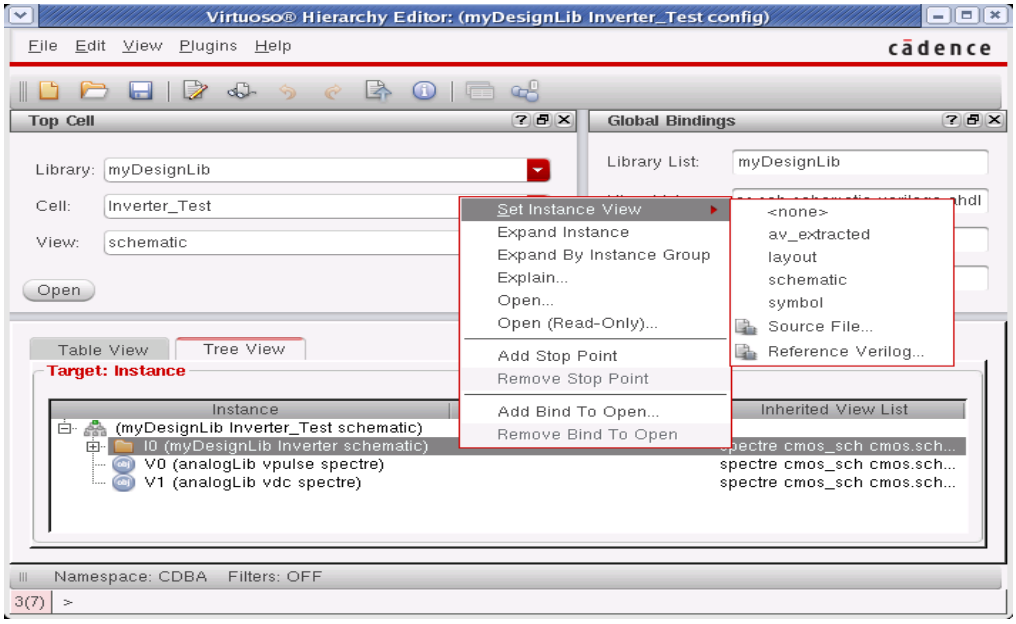
To run the Circuit with Parasites

In this exercise, we will change the configuration to direct simulation of the **av_extracted** view which contains the parasites.

1. Open the same Hierarchy Editor form, which is already set for Inverter_Test config.

2. Select the **Tree View** icon: this will show the design hierarchy in the tree format.

3. Click **right** mouse on the Inverter schematic.
A pull down menu appears. Select **av_extracted** view from the **Set Instance view** menu, the View to use column now shows av_extracted view.



4. Click on the **Recompute the hierarchy** icon,  the configuration is now updated from schematic to av_extracted view.

6. From the **Analog Design Environment** window click **Netlist and Run**  to start the simulation again.

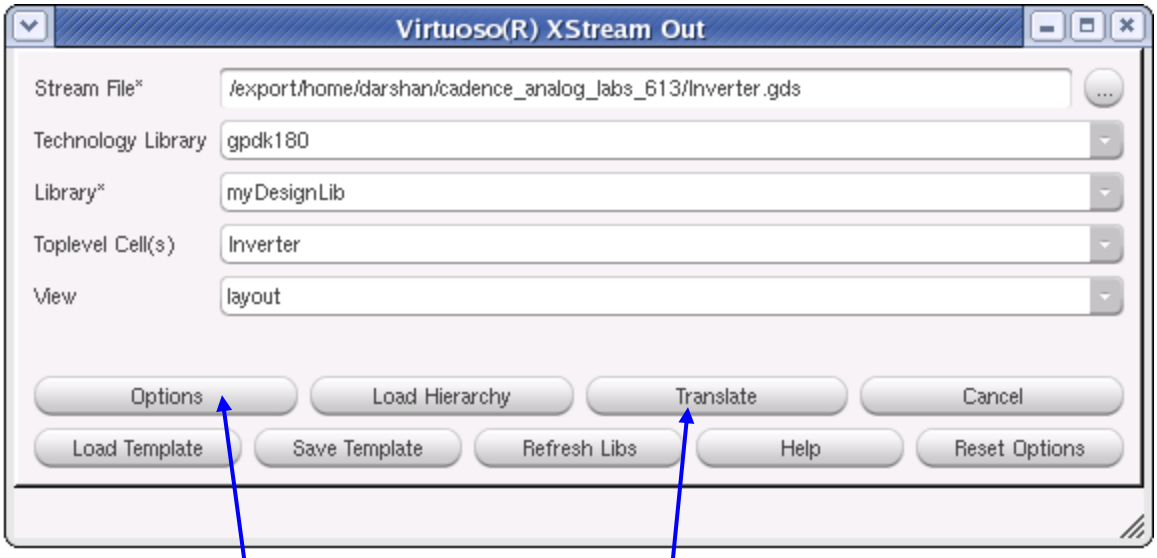
7. When simulation completes, note the **Circuit inventory conditions**, this time the list shows all nets, designed devices, sources and parasitic devices as well.

8. Calculate the delay again and match with the previous one. Now you can conclude how much delay is introduced by these parasites, now our main aim should to minimize the delay due to these parasites so number of iteration takes place for making an optimize layout.

Generating Stream Data

Streaming Out the Design

1. Select **File – Export – Stream** from the CIW menu and **Virtuoso Xstream out** form appears change the following in the form.



2. Click on the **Options** button.

3. In the **StreamOut-Options** form select 

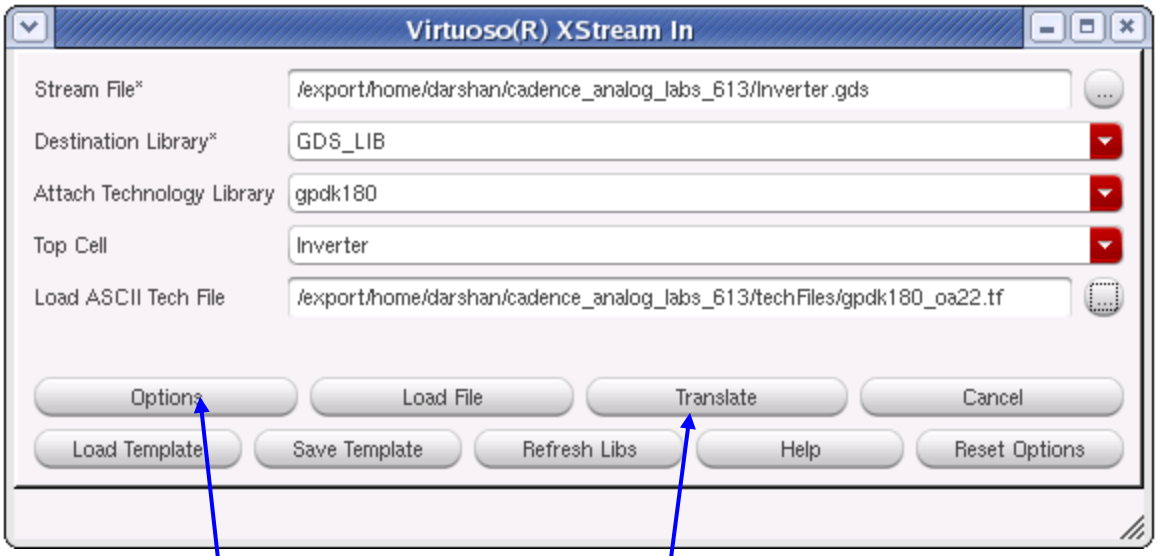
under **Layers** tab and click **OK.**

4. In the **Virtuoso XStream Out** form, click **Translate** button to start the stream translator.

5. The stream file Inverter.gds is stored in the specified location.

Streaming In the Design

1. Select **File – Import – Stream** from the CIW menu and change the following in the form.



You need to specify the **gpdk180_oa22.tf** file. This is the entire technology file that has been dumped from the design library.

2. Click on the **Options** button.

3. In the **StreamOut-Options** form select 

under **Layers** tab and click **OK.**

4. In the **Virtuoso XStream Out** form, click **Translate** button to start the stream translator.

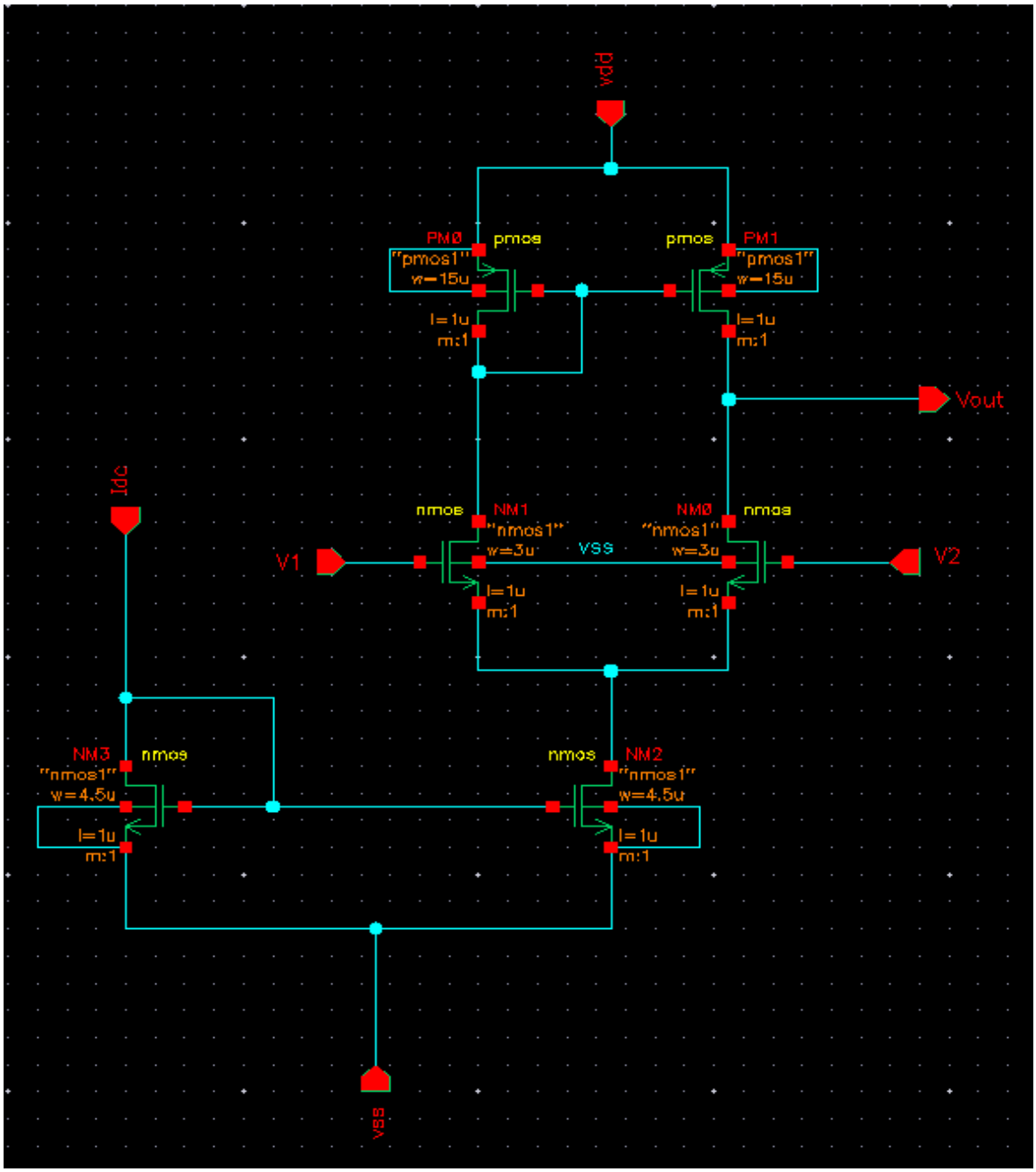
5. From the Library Manager open the **Inverter** cellview from the **GDS_LIB** library and notice the design.

6. Close all the windows except CIW window, which is needed for the next lab.

END OF LAB 1

Lab 2: DIFFERENTIAL AMPLIFIER

Schematic Capture



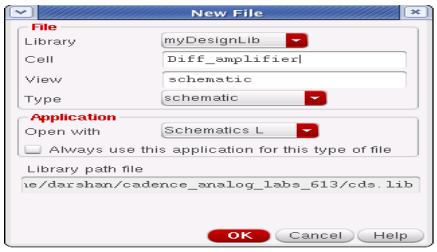
Schematic Entry

Objective: To create a new cell view and build Differential Amplifier

Creating a Schematic cellview

Open a new schematic window in the **myDesignLib** library and build the Differntial_Amplifier design.

1. In the CIW or Library manager, execute **File – New – Cellview**. Set up the Create New file form as follows:



3. Click **OK** when done. A blank schematic window for the design appears.

Adding Components to schematic

1. In the Differential Amplifier schematic window, execute **Create— Instance** to display the Add Instance form.

2. Click on the **Browse** button. This opens up a Library browser from which you can select components and the **Symbol** view .

You will update the Library Name, Cell Name, and the property values given in the table on the next page as you place each component.

3. After you complete the Add Instance form, move your cursor to the schematic window and click **left** to place a component.

This is a table of components for building the Differential Amplifier schematic.

Library name	Cell Name	Properties/Comments
gpdk180	nmos	Model Name = nmos1 (NM0, NM1) ; W= 3u ; L= 1u
gpdk180	nmos	Model Name =nmos1 (NM2, NM3) ; W= 4.5u ; L= 1u
gpdk180	pmos	Model Name =pmos1 (PM0, PM1); W= 15u ; L= 1u

3. After entering components, click **Cancel** in the Add Instance form
or press **Esc** with your cursor in the schematic window

Adding pins to Schematic

Use **Create – Pin** or the menu icon to place the pins on the schematic window.

1. Click the **Pin** fixed menu icon in the schematic window.
You can also execute **Create – Pin** or press **p**. The Add pin form appears.

2. Type the following in the Add pin form in the exact order leaving space between the pin names.

Pin Names	Direction
Idc,V1,V2	Input
Vout	Output
vdd, vss,	InputOutput

Make sure that the direction field is set to **input/ouput/inputoutput** when placing the **input/output/inout** pins respectively and the Usage field is set to **schematic**.

3. Select **Cancel** from the Add pin form after placing the pins.

In the schematic window, execute **View— Fit** or press the **f** bindkey.

Adding Wires to a Schematic

Add wires to connect components and pins in the design.

1. Click the **Wire (narrow)** icon in the schematic window.
You can also press the **w** key, or execute **Create - Wire (narrow).**

2. Complete the wiring as shown in figure and when done wiring press ***ESC*** key in the schematic window to cancel wiring.

Saving the Design

1. Click the **Check and Save** icon in the schematic editor window.

2. Observe the **CIW** output area for any errors.

Symbol Creation

Objective: To create a symbol for the Differential Amplifier

1. In the Differential Amplifier schematic window, execute **Create — Cellview— From Cellview**.

The **Cellview from Cellview** form appears. With the Edit Options function active, you can control the appearance of the symbol to generate.

2. Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is set to **symbol**, with the Tool/Data Type set as **SchematicSymbol.**

3. Click **OK** in the Cellview from Cellview form. The **Symbol Generation Form** appears.

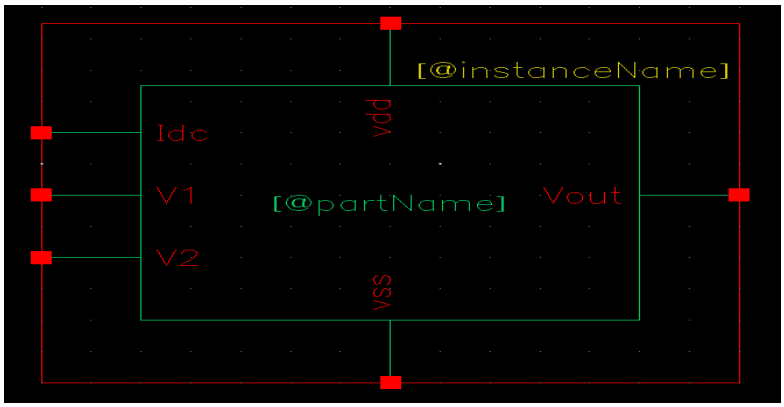
4. Modify the **Pin Specifications** as in the below symbol.

5. Click **OK** in the Symbol Generation Options form.

6. A new window displays an automatically created Differential Amplifier symbol.

7. Modifying automatically generated symbol so that it looks like below Differential Amplifier symbol.

8. Execute **Create— Selection Box**. In the Add Selection Box form, click **Automatic.** A new red selection box is automatically added.



9. After creating symbol, click on the **save** icon in the symbol editor window to save the symbol. In the symbol editor, execute **File— Close** to close the symbol view window.

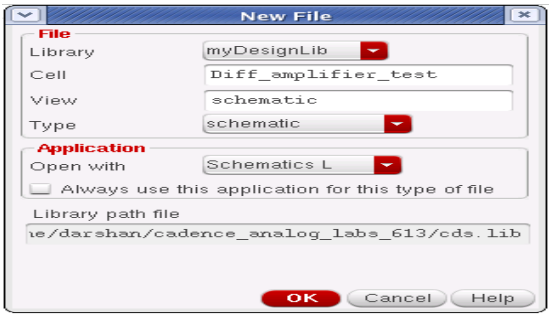
Building the Diff_amplifier_test Design

Objective: To build Differential Amplifier Test circuit using your Differential Amplifier

Creating the Differential Amplifier Test Cellview

1. In the CIW or Library Manager, execute **File— New— Cellview**.

2. Set up the Create New File form as follows:



3. Click **OK** when done. A blank schematic window for the Diff_ amplifier_test design appears.

Building the Diff_amplifier_test Circuit

1. Using the component list and Properties/Comments in this table, build the Diff_amplifier_test schematic.

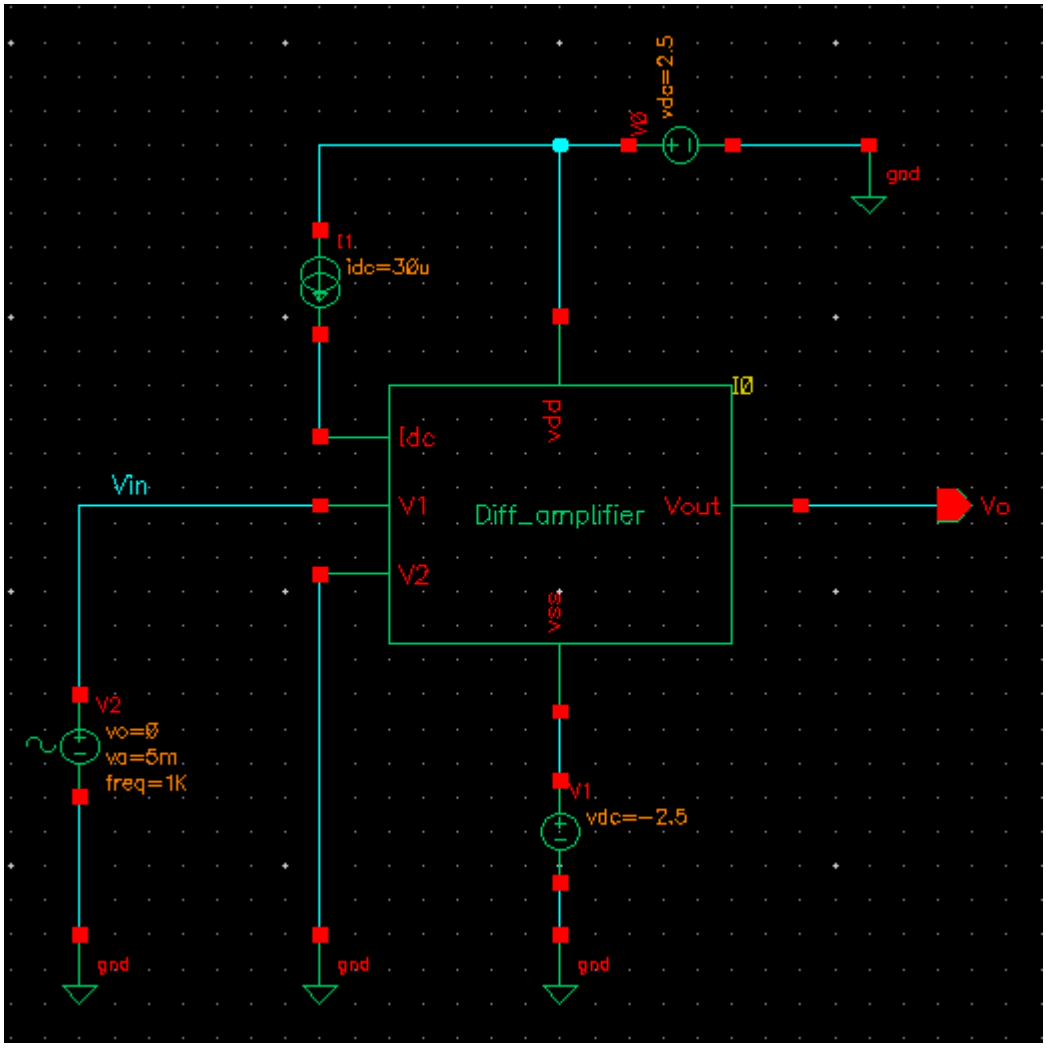
Library name	Cellview name	Properties/Comments
myDesignLib	Diff_amplifier	Symbol
analogLib	vsin	Define specification as AC Magnitude= 1; Amplitude= 5m; Frequency= 1K
analogLib	vdd, vss, gnd	Vdd=2.5 ; Vss= -2.5
analogLib	Idc	Dc current = 30u

Note: Remember to set the values for **VDD** and **VSS**. Otherwise your circuit will have no power.

3. Click the **Wire (narrow)** icon and wire your schematic.
Tip: You can also press the **w** key, or execute **Create— Wire (narrow).**

4. Click on the **Check and save** icon to save the design.

5. The schematic should look like this.



6. Leave your Diff_amplifier_test schematic window open for the next section.

Analog Simulation with Spectre

Objective: To set up and run simulations on the Differential Amplifier Test design.

In this section, we will run the simulation for Differential Amplifier and plot the transient, DC and AC characteristics.

Starting the Simulation Environment

1. In the Diff_amplifier_test schematic window, execute **Launch – ADE L**. The Analog Design Environment simulation window appears.

Choosing a Simulator

1. In the simulation window or ADE, execute
Setup— Simulator/Directory/Host.

2. In the **Choosing Simulator** form, set the Simulator field to **spectre** (Not spectreS) and click **OK**.

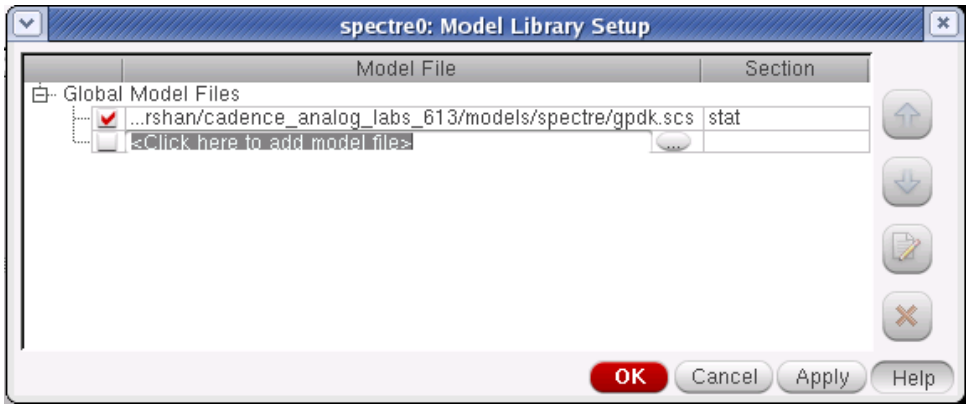
Setting the Model Libraries

1. Click **Setup - Model Libraries.**

Note: Step 2 should be executed only if the model file not loaded by default.

2. In the Model Library Setup form, click **Browse** and find the **gpdk180.scs** file in the **./models/spectre** directory.

Select **stat** in Section field, click **Add** and click **OK.**



Choosing Analyses

1. In the Simulation window, click the **Choose - Analyses** icon.
You can also execute **Analyses - Choose.**

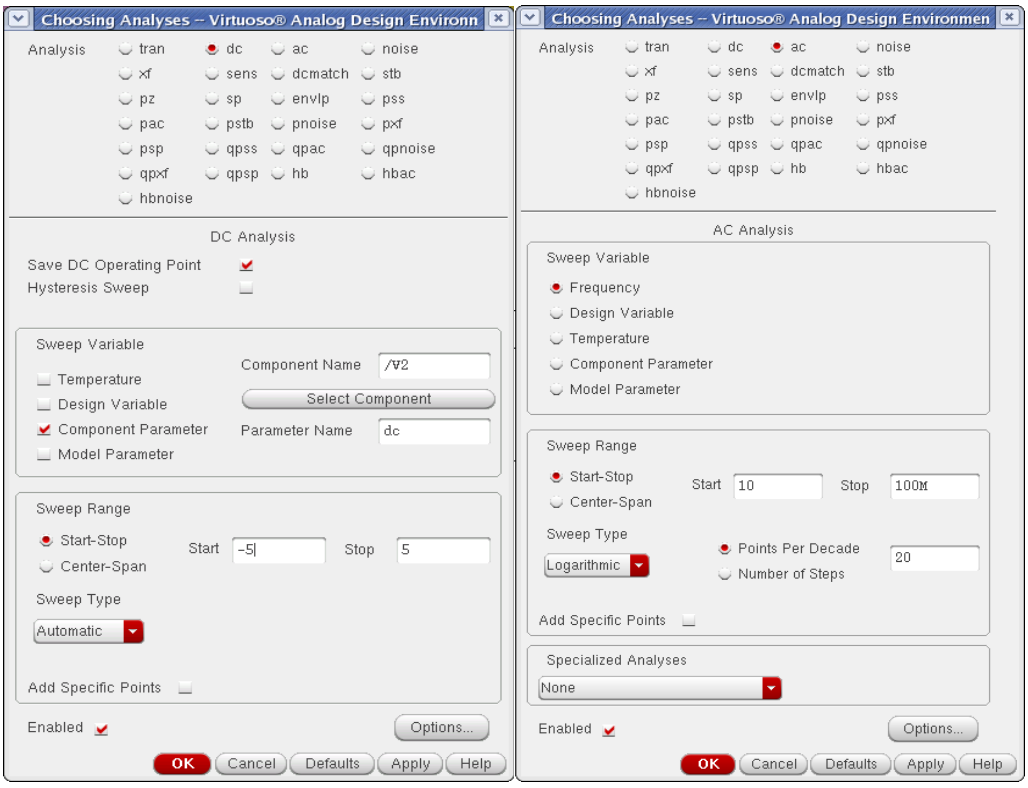
The Choosing Analysis form appears. This is a dynamic form, the bottom of the form changes based on the selection above.

2. To setup for transient analysis

   a. In the Analysis section select **tran**
   b. Set the stop time as **5m**
   c. Click at the **moderate** or **Enabled** button at the bottom, and then click **Apply.**

3. To set up for DC Analyses:

   a. In the Analyses section, select **dc**.
   b. In the DC Analyses section, turn **on** Save DC Operating Point.
   c. Turn on the **Component Parameter**
   d. Double click the **Select Component**, Which takes you to the schematic window.
   e. Select input signal **Vsin** for dc analysis.
   f. In the analysis form, select **start** and **stop** voltages as **-5** to **5** respectively.
   g. Check the enable button and then click **Apply**.



4. To set up for AC Analyses form is shown in the previous page.

   a. In the Analyses section, select **ac**.
   b. In the AC Analyses section, turn on **Frequency.**
   c. In the Sweep Range section select **start** and **stop** frequencies as **150** to **100M**
   d. Select Points per Decade as **20**.
   e. Check the enable button and then click **Apply**.

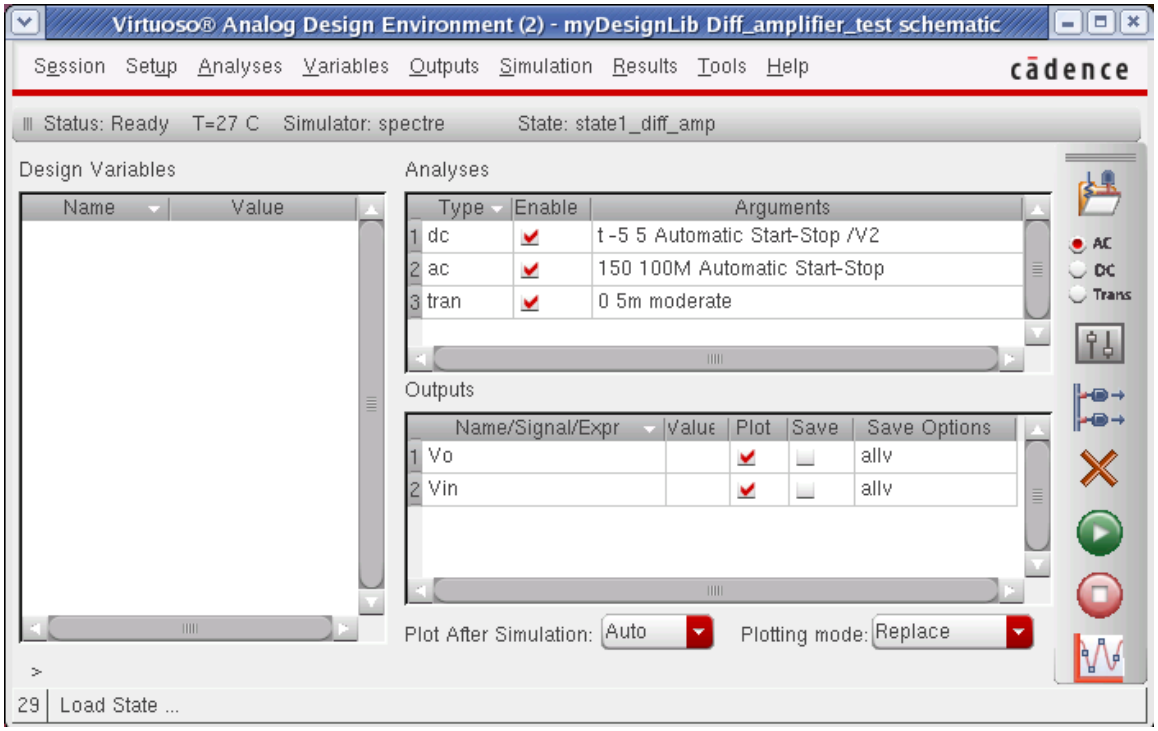
5. Click **OK** in the Choosing Analyses Form.

Selecting Outputs for Plotting

Select the nodes to plot when simulation is finished.

1. Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.
2. Follow the prompt at the bottom of the schematic window, Click on output net **Vo,** input net **Vin** of the Diff_amplifier. Press **ESC** with the cursor in the schematic after selecting node.

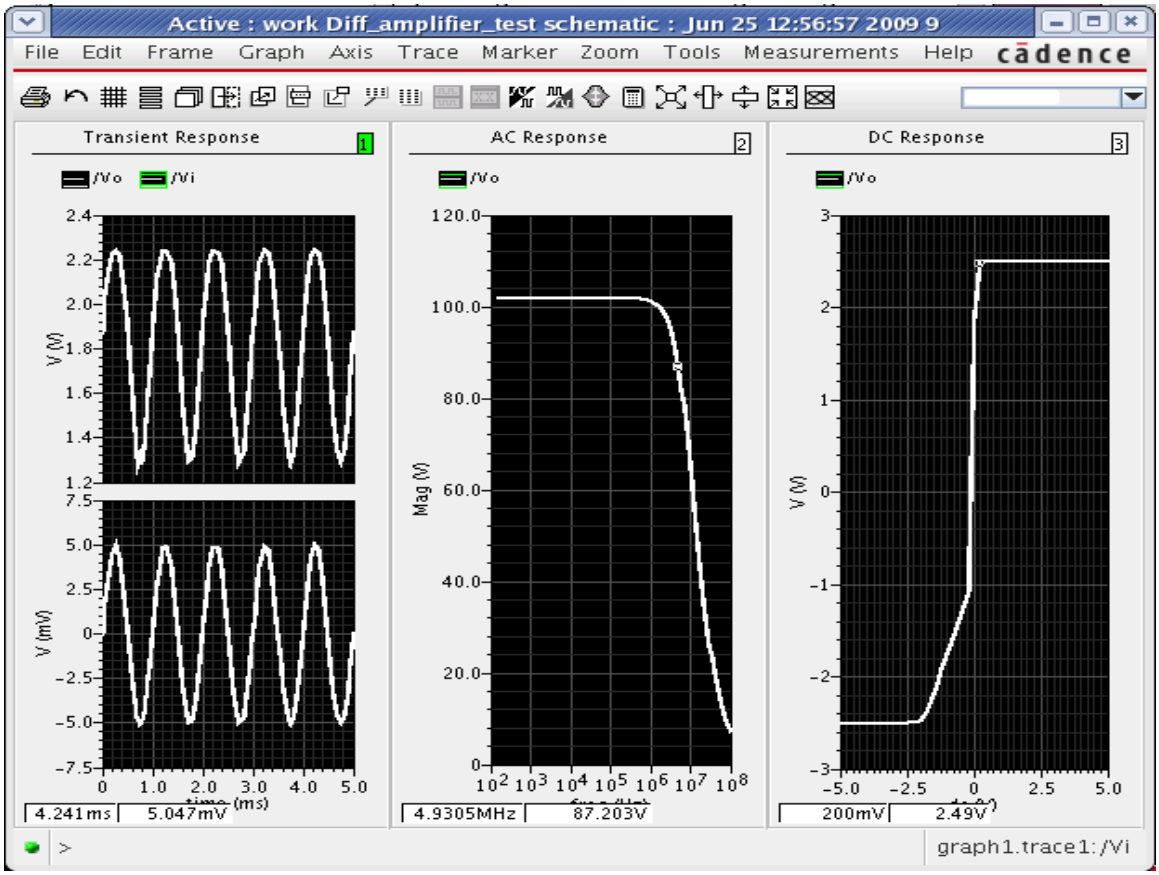
Does the simulation window look like this?



Running the Simulation

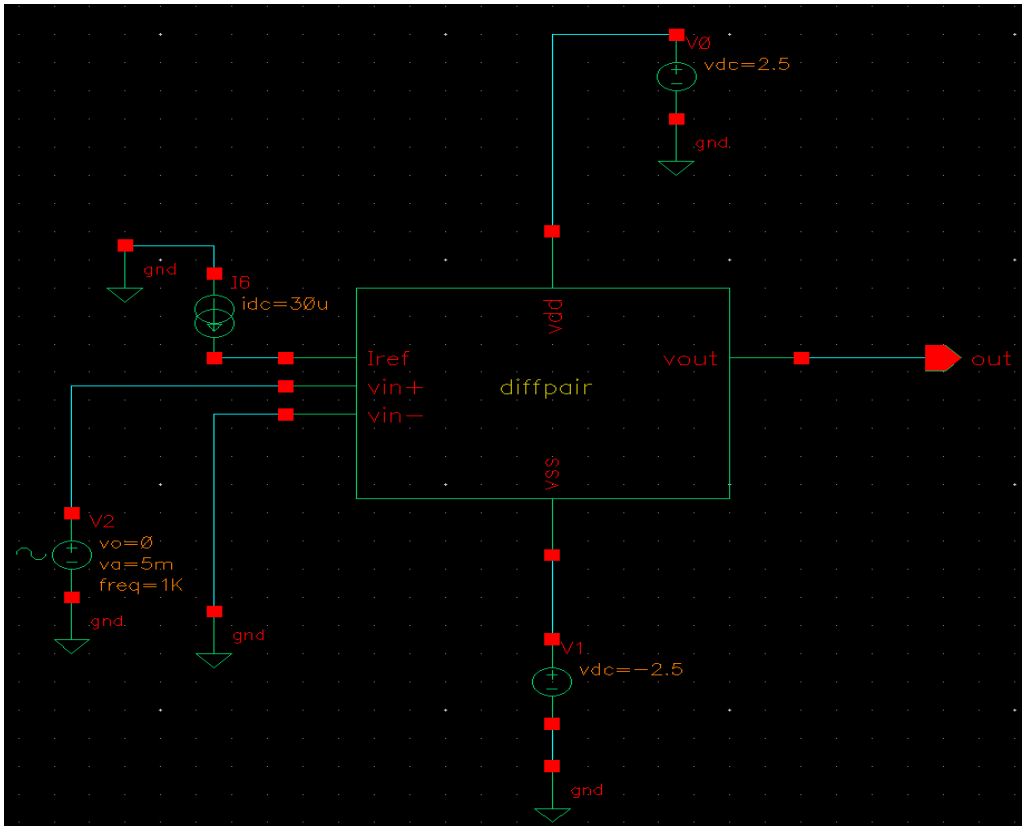
1. Execute **Simulation – Netlist and Run** in the simulation window to start the simulation, this will create the netlist as well as run the simulation.

2. When simulation finishes, the Transient, DC and AC plots automatically will be popped up along with netlist.

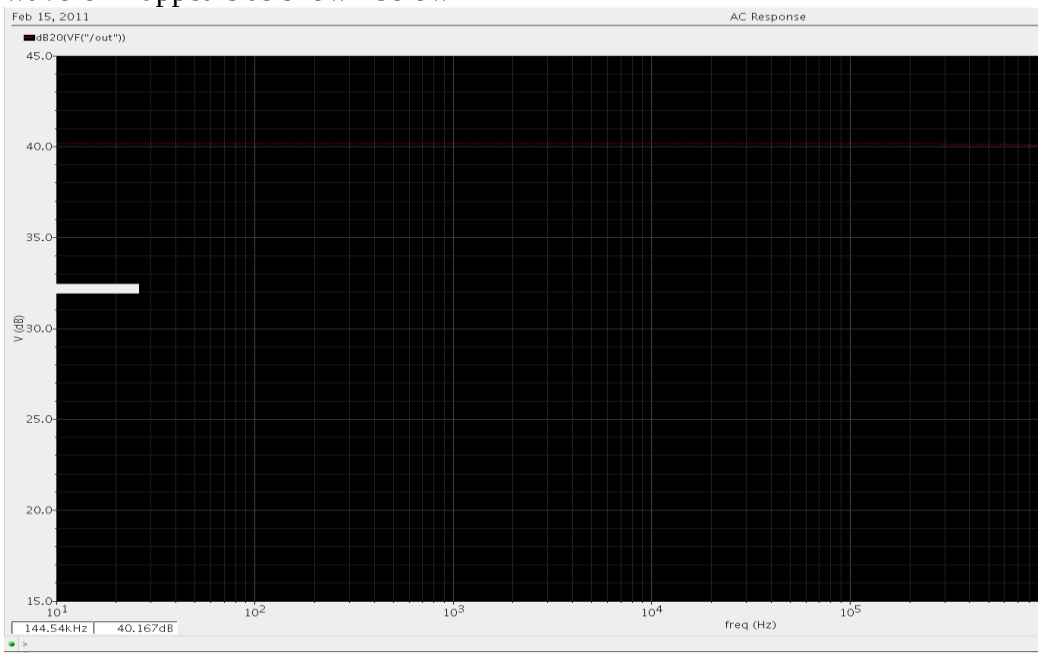


To Calculate the gain of Differential pair:

Configure the Differential pair schematic as shown below –

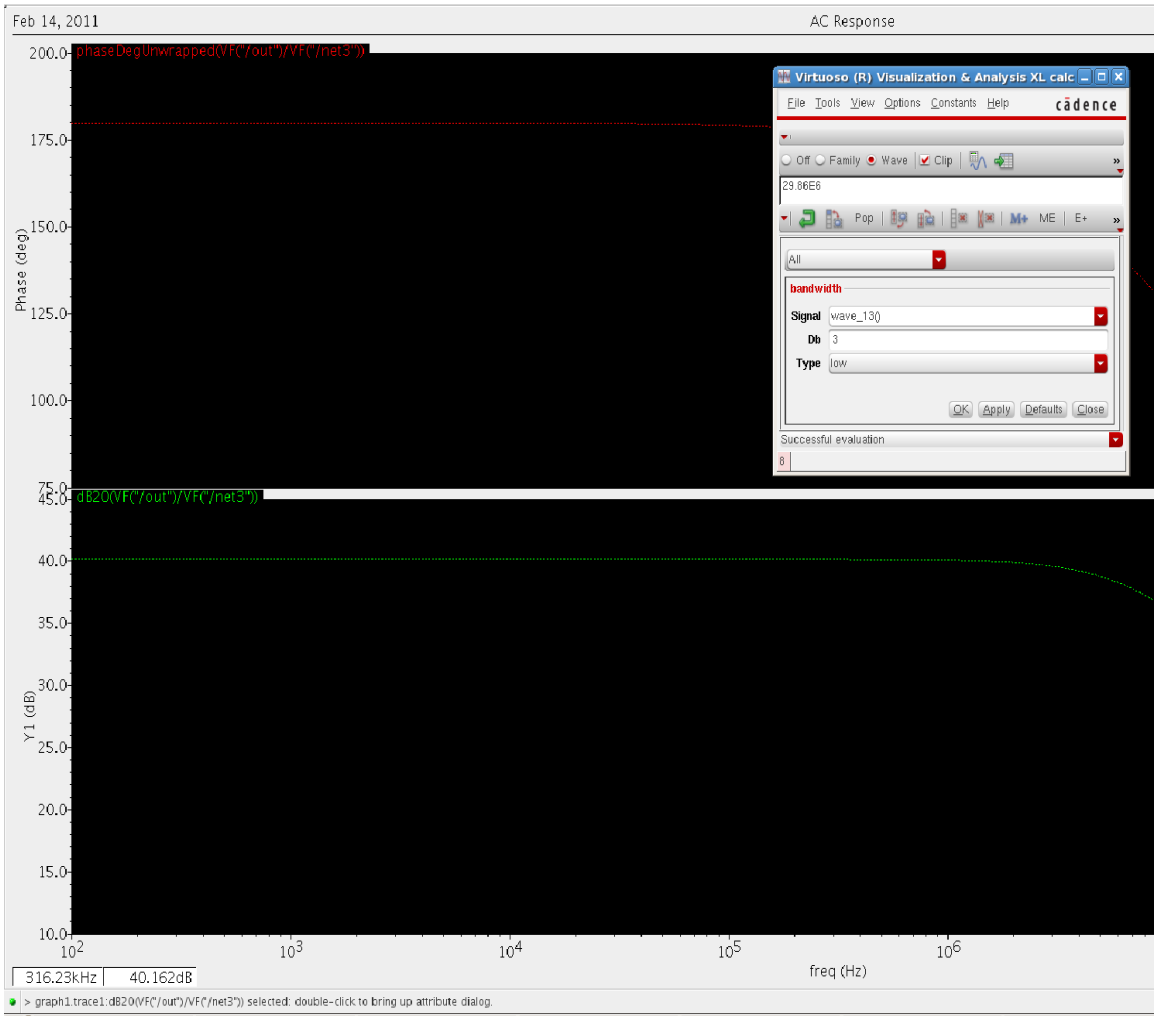


Now, open the ADE L, from **LAUNCH →ADE L** , choose the analysis set the ac response and run the simulation, from **Simulation →Run.** Next go to **Results→Direct plot** select AC dB20 and output from the schematic and press escape. The following waveform appears as shown below –



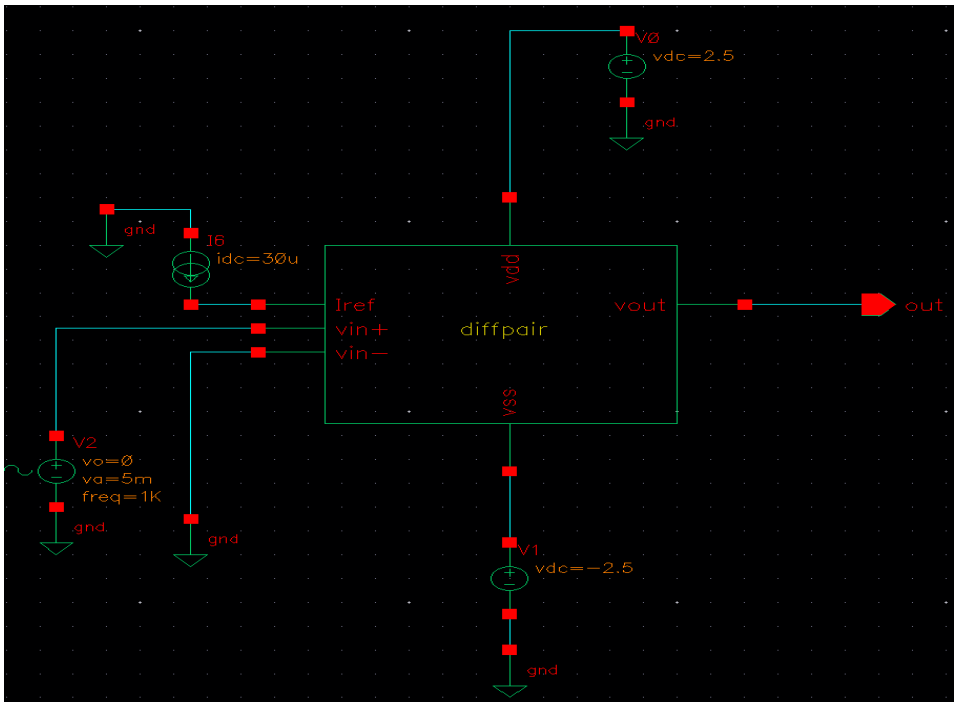
To Calculate the BW of the Differential pair :

Open the calculator and select the bandwidth option, select the waveform of the gain in dB and press Evaluate the buffer -

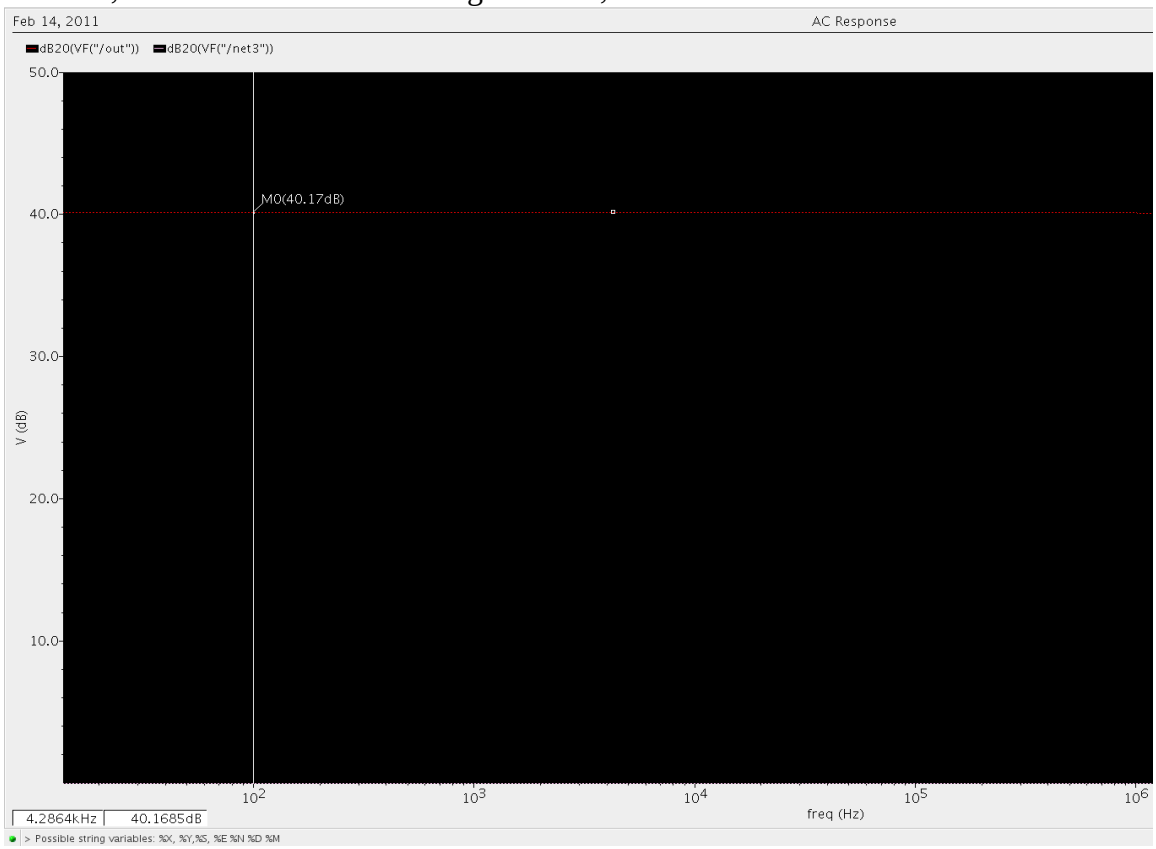


To Calculate the CMRR of the Differential pair :

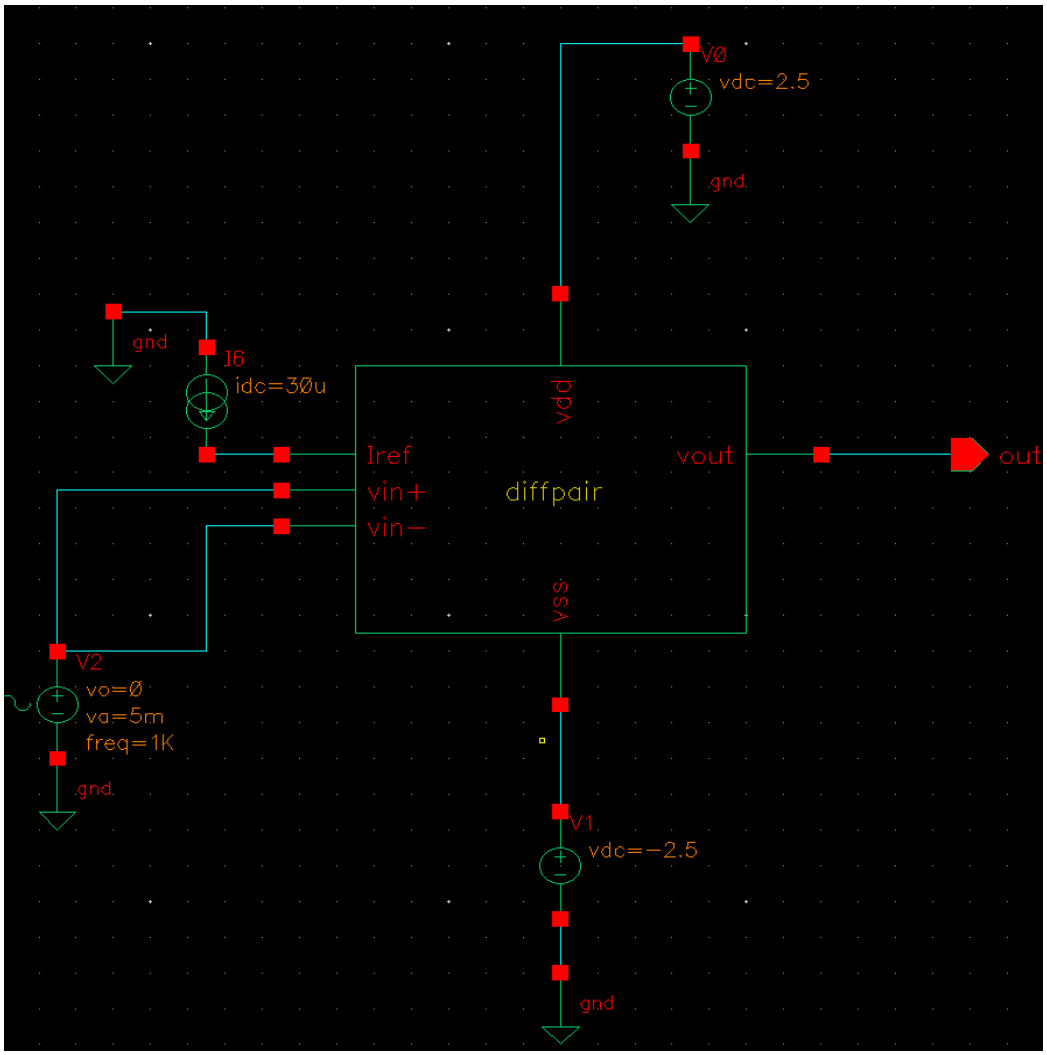
Configure the Differential pair schematic to calculate the differential gain as shown below –



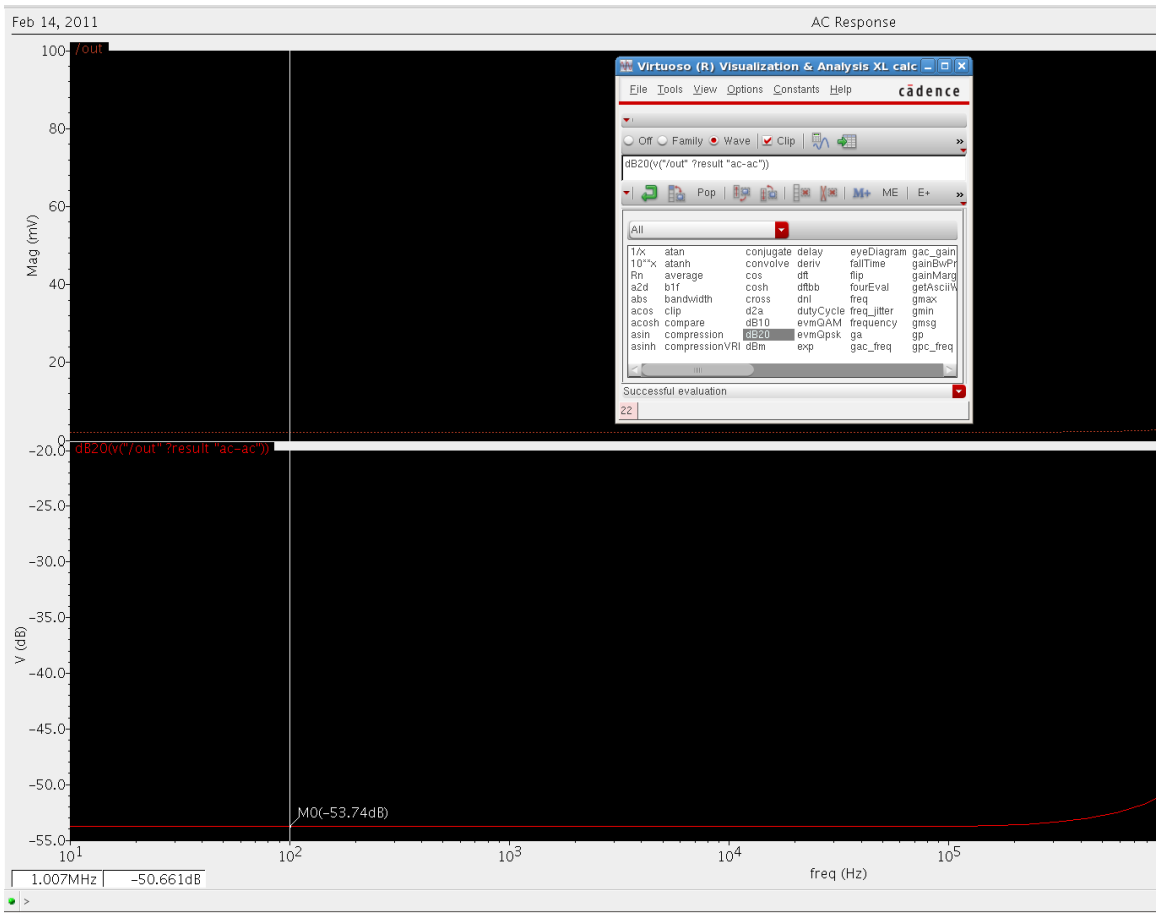
In the ADE L, plot the ac response with gain in dB. Measure the gain at 100hz and at 100Mhz,note down the value of the gain in dB, as shown below –



Configure the Differential pair schematic to calculate the common-mode gain as shown below –



In the ADE L, plot the ac response with gain in dB. Measure the gain at 100hz and at 100Mhz, note down the value of the gain in dB, as shown below –



Calculate the CMRR = $\left|\frac{Ad}{Ac}\right|$, add the gains in dB i.e., A_d – ($-A_c$). For the output impedance note down the output resistance of the pmos and nmos transistors at the ouput side, and use the necessary equation like $r_{01} \| r_{02}$.

Saving the Simulator State

We can save the simulator state, which stores information such as model library file, outputs, analysis, variable etc. This information restores the simulation environment without having to type in all of setting again.

1. In the Simulation window, execute **Session – Save State**.
The Saving State form appears.

2. Set the **Save as** field to **state1_diff_amp** and make sure all options are selected under what to save field. Click **OK** in the saving state form. The Simulator state is saved.

Creating a Layout View of Diff_ Amplifier

1. From the Diff_amplifier schematic window menu execute **Launch – Layout XL**. A **Startup Option** form appears.

2. Select **Create New** option. This gives a New Cell View Form

3. Check the Cellname **(Diff_amplifier)**, Viewname **(layout).**

4. Click **OK** from the New Cellview form.

LSW and a blank layout window appear along with schematic window.

Adding Components to Layout

1. Execute **Connectivity – Generate – All from Source** or click the icon  in the layout editor window, **Generate Layout** form appears. Click **OK** which imports the schematic components in to the Layout window automatically.

2. Re arrange the components with in PR-Boundary as shown in the next page.

3. To rotate a component, Select the component and execute **Edit –Properties**. Now select the degree of rotation from the property edit form.

4. To Move a component, Select the component and execute **Edit -Move** command.

Making interconnection

1. Execute **Connectivity –Nets – Show/Hide selected Incomplete Nets** or click  the icon in the Layout Menu.

2. Move the mouse pointer over the device and click **LMB** to get the connectivity information, which shows the guide lines (or flight lines) for the inter connections of the components.

3. From the layout window execute **Create – Shape – Path** or **Create – Shape – Rectangle (**for vdd and gnd bar**)** and select the appropriate Layers from the **LSW** window and Vias for making the inter connections

Creating Contacts/Vias

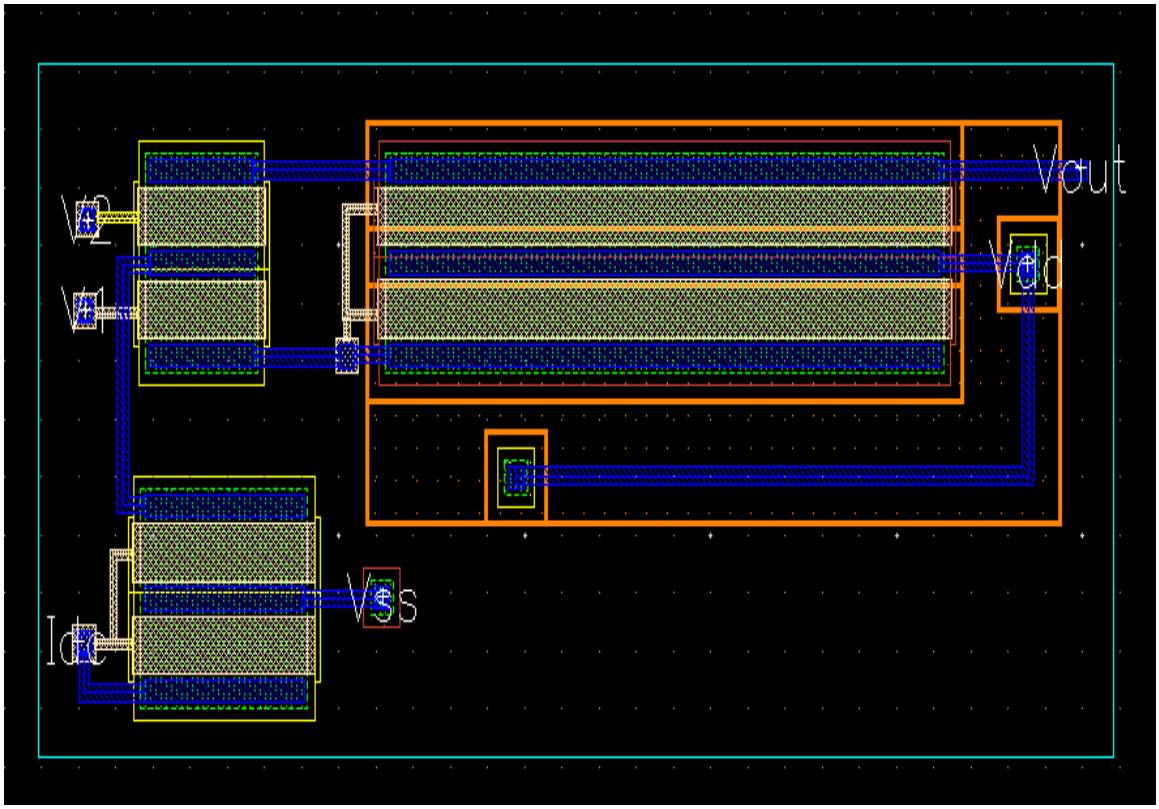
You will use the contacts or vias to make connections between two different layers.

1. Execute **Create — Via** or select  command to place different Contacts, as given in below table

Connection	Contact Type
For Metal1- Poly Connection	Metal1-Poly
For Metal1- Psubstrate Connection	Metal1-Psub
For Metal1- Nwell Connection	Metal1-Nwell

Saving the design

1. Save your design by selecting **File — Save** or click  to save the layout and layout should appear as below.



Physical Verification
Assura DRC

Running a DRC

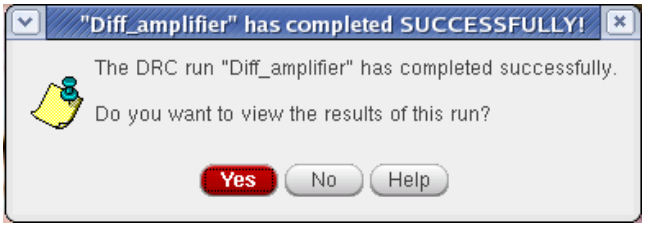
1. Open the Differential_Amplifier layout form the CIW or library manger if you have closed that.Press **shift – f** in the layout window to display all the levels.

2. Select **Assura - Run DRC** from layout window.
The DRC form appears. The Library and Cellname are taken from the current design window, but rule file may be missing. Select the Technology as **gpdk180.** This automatically loads the rule file.

3. Click **OK** to start DRC.

4. A Progress form will appears. You can click on the watch log file to see the log file.

5. When DRC finishes, a dialog box appears asking you if you want to view your DRC results, and then click **Yes** to view the results of this run.

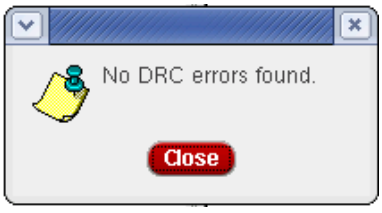


6. If there any DRC error exists in the design **View Layer Window** (VLW) and **Error Layer Window** (ELW) appears. Also the errors highlight in the design itself.

7. Click **View – Summary** in the ELW to find the details of errors.

8. You can refer to rule file also for more information, correct all the DRC errors and **Re – run** the DRC.

9. If there are no errors in the layout then a dialog box appears with **No DRC errors found** written in it, click on **close** to terminate the DRC run.



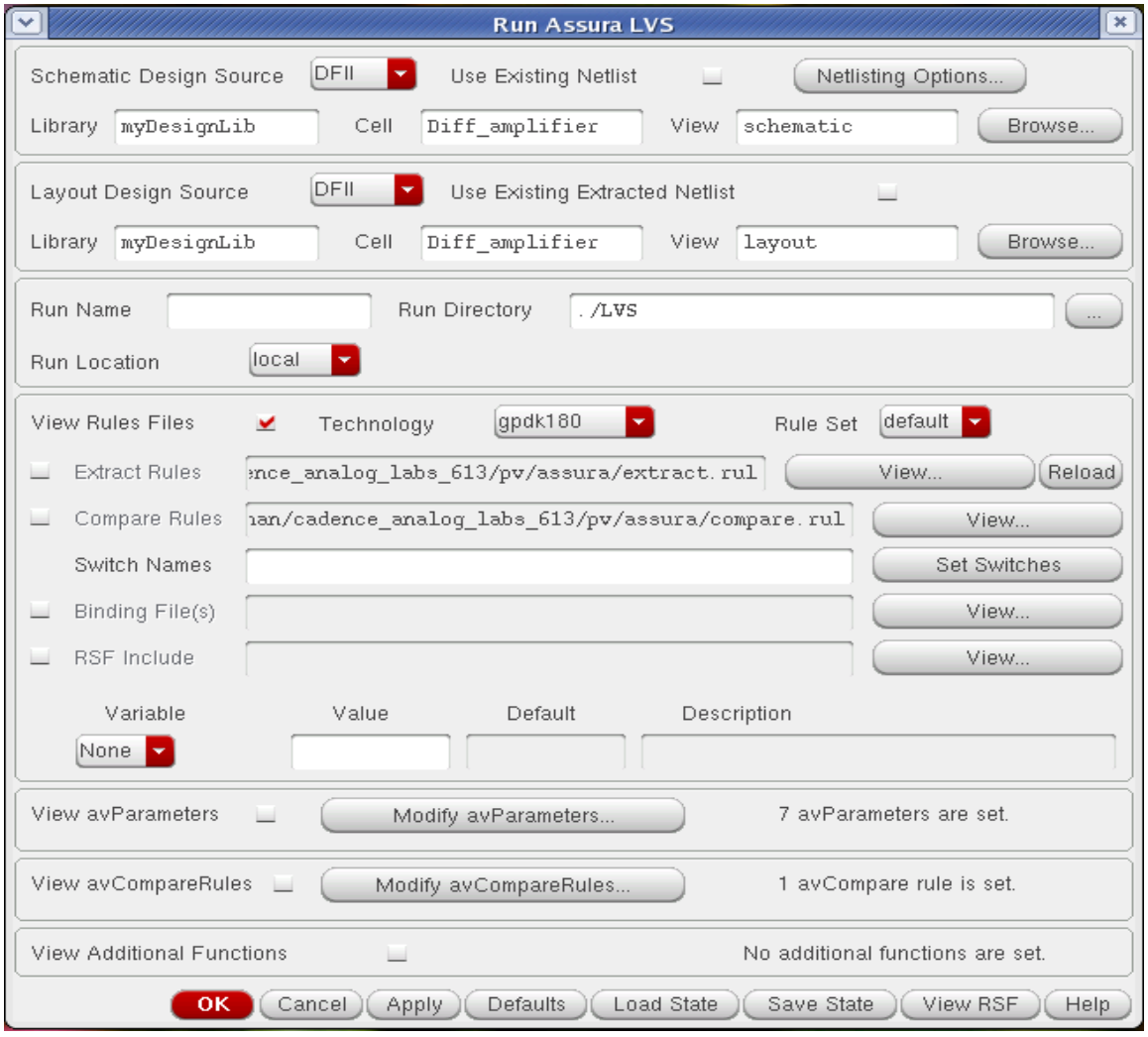
ASSURA LVS

In this section we will perform the LVS check that will compare the schematic netlist and the layout netlist.

Running LVS

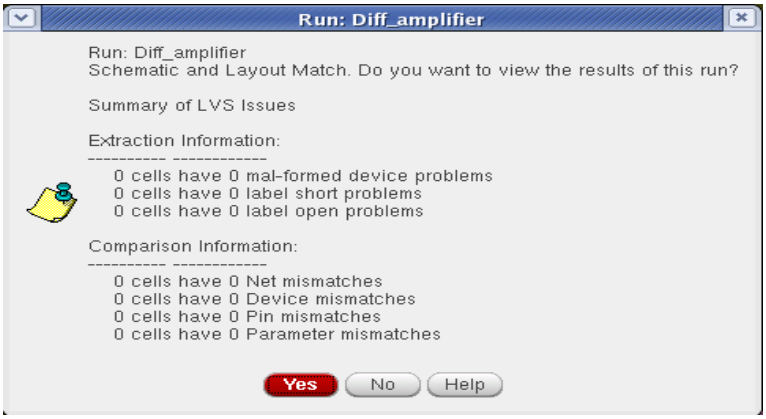
1. Select **Assura – Run LVS** from the layout window.
The Assura Run LVS form appears. The layout name is already in the form. Assura fills in the layout name from the cellview in the layout window.

2. Verify the following in the Run Assura LVS form.

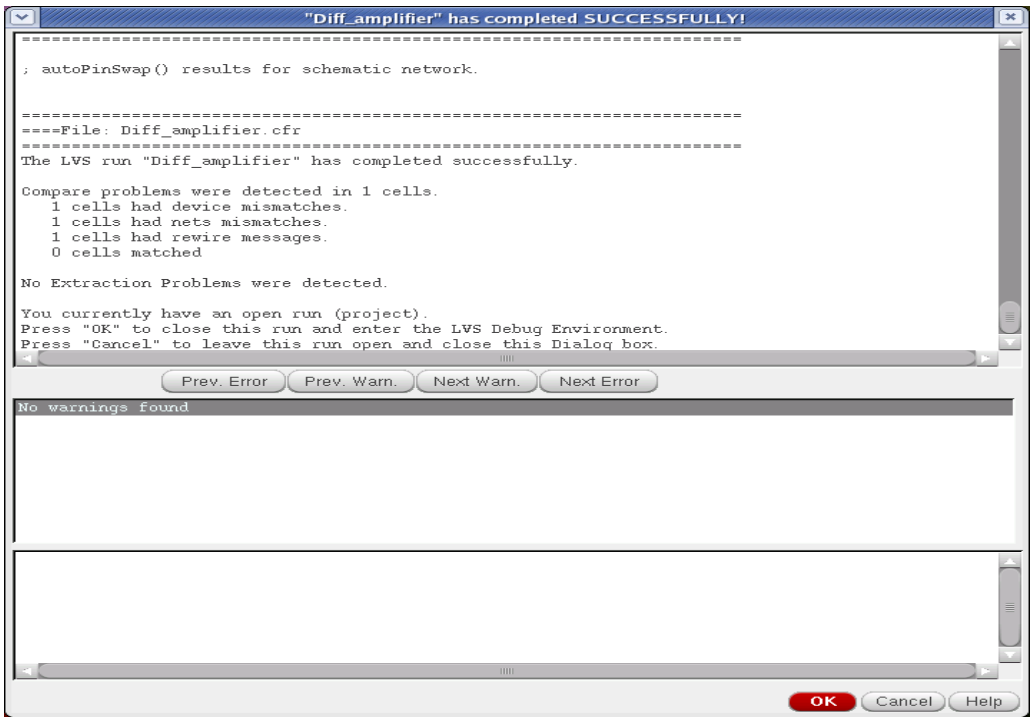


3. The LVS begins and a Progress form appears.

4. If the schematic and layout matches completely, you will get the form displaying **Schematic and Layout Match**.



5. If the schematic and layout do not matches, a form informs that the LVS completed successfully and asks if you want to see the results of this run.



6. Click **Yes** in the form.LVS debug form appears, and you are directed into LVS debug environment.

7. In the **LVS debug form** you can find the details of mismatches and you need to correct all those mismatches and **Re – run** the LVS till you will be able to match the schematic with layout.

Assura RCX

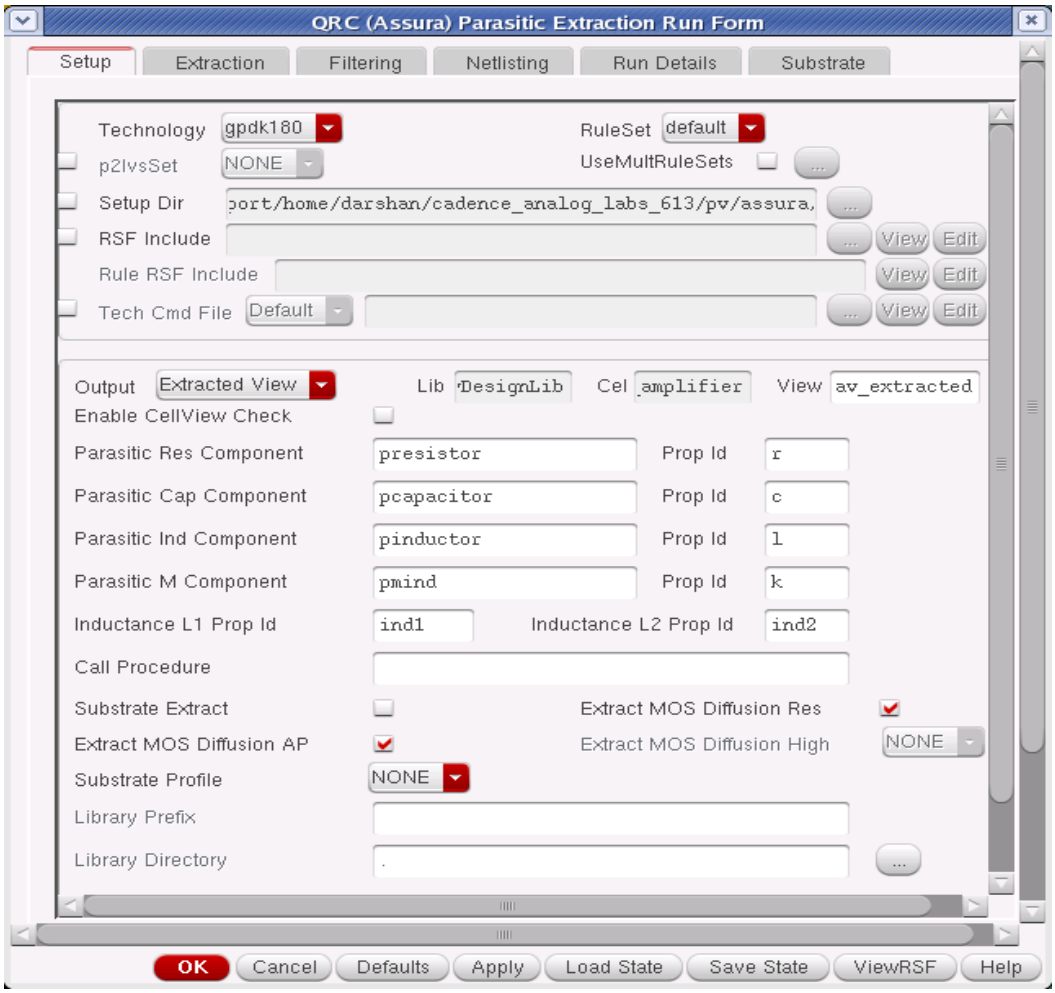
In this section we will extract the RC values from the layout and perform analog circuit simulation on the designs extracted with RCX.

Before using RCX to extract parasitic devices for simulation, the layout should match with schematic completely to ensure that all parasites will be backannoted to the correct schematic nets.

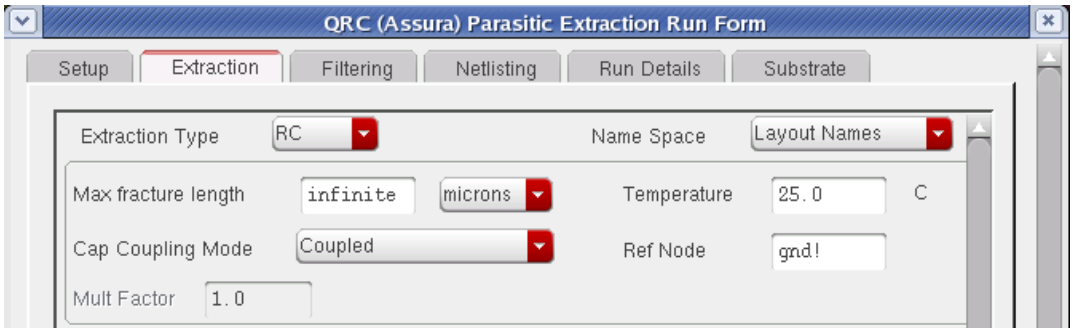
Running RCX

1. From the layout window execute **Assura – Run RCX**.

2. Change the following in the Assura parasitic extraction form. Select **output** type under **Setup** tab of the form.



3. In the **Extraction** tab of the form, choose Extraction type, Cap Coupling Mode and specify the Reference node for extraction.



4. In the **Filtering** tab of the form, **Enter Power Nets** as **vdd!, vss!** and **Enter Ground Nets** as **gnd!**

5. Click **OK** in the Assura parasitic extraction form when done.

The RCX progress form appears, in the progress form click **Watch log file** to see the output log file.

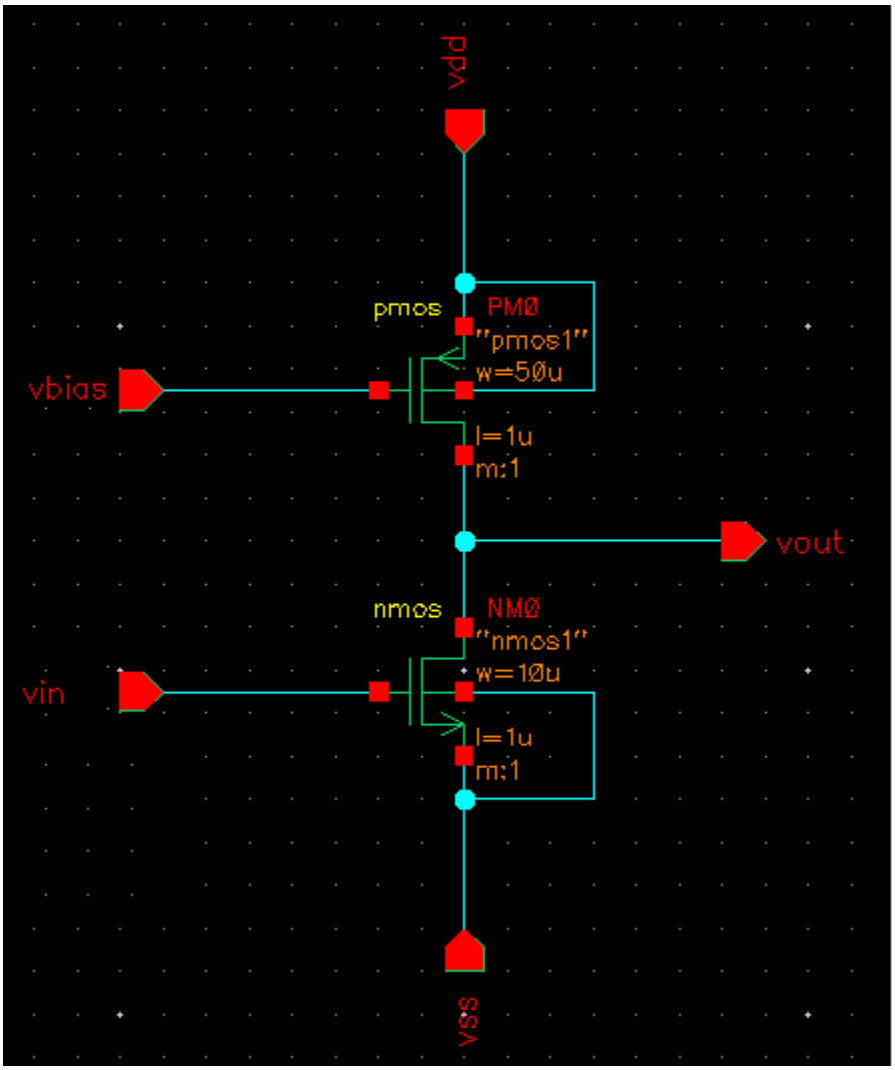
5. When RCX completes, a dialog box appears, informs you that **Assura RCX run completed successfully.**

6. You can open the **av_extracted** view from the library manager and view the parasitic.

END OF LAB 2

COMMON SOURCE AMPLIFIER

Schematic Capture



Schematic Entry

Objective: To create a new cell view and build Common Source Amplifier

Use the techniques learned in the Lab1 and Lab2 to complete the schematic of Common Source Amplifier.
This is a table of components for building the Common Source Amplifier schematic.

Library name	Cell Name	Properties/Comments
gpdk180	Pmos	Model Name = pmos1; W= 50u ; L= 1u
gpdk180	Nmos	Model Name =nmos1; W= 10u ; L= 1u

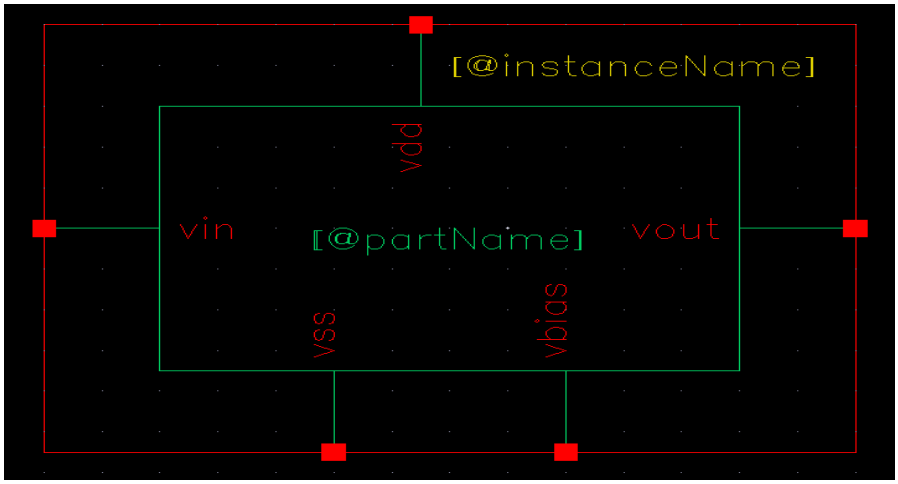
Type the following in the ADD pin form in the exact order leaving space between the pin names.

Pin Names	Direction
vin vbias	Input
vout	Output
vdd vss	Input

Symbol Creation

Objective: To create a symbol for the Common Source Amplifier

Use the techniques learned in the Lab1 and Lab2 to complete the symbol of cs-amplifier

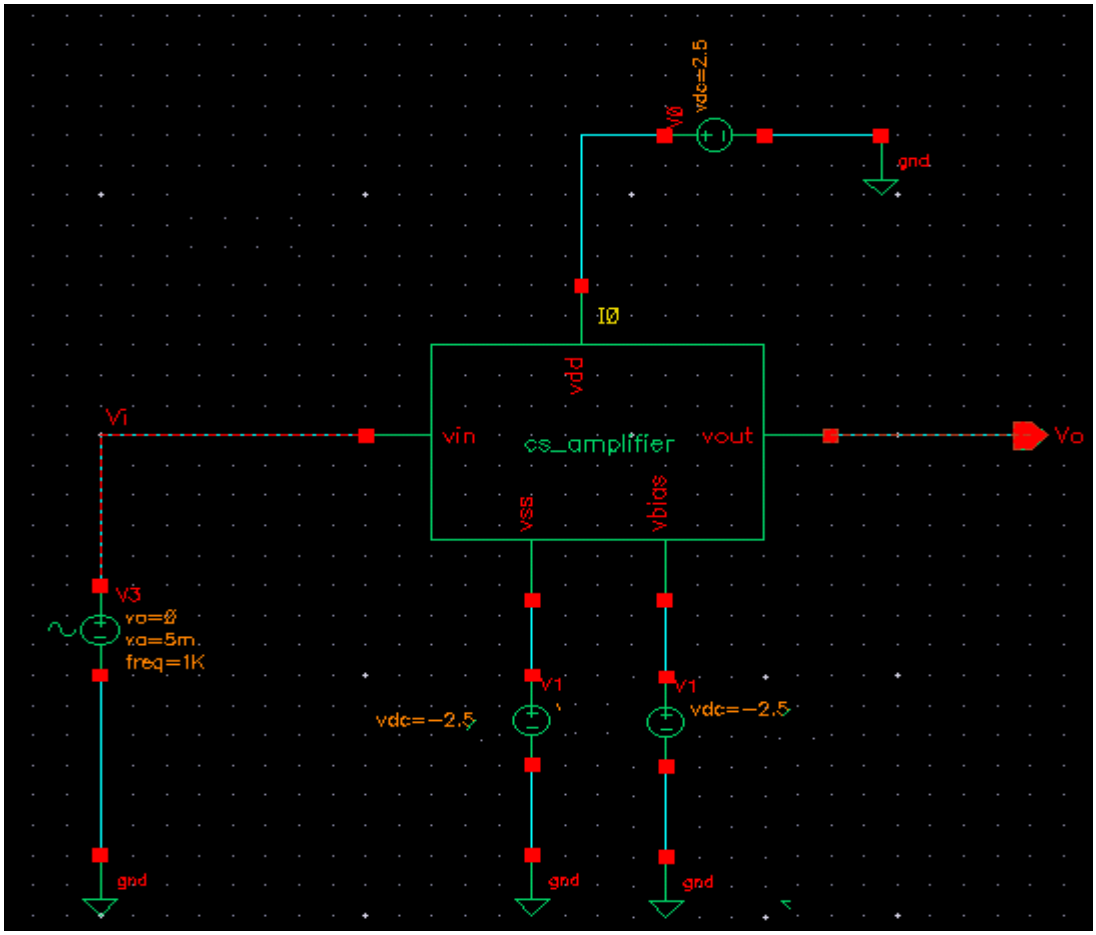


Building the Common Source Amplifier Test Design

Objective: To build cs_amplifier_test circuit using your cs_amplifier

Using the component list and Properties/Comments in the table, build the cs-amplifier_test schematic as shown below.

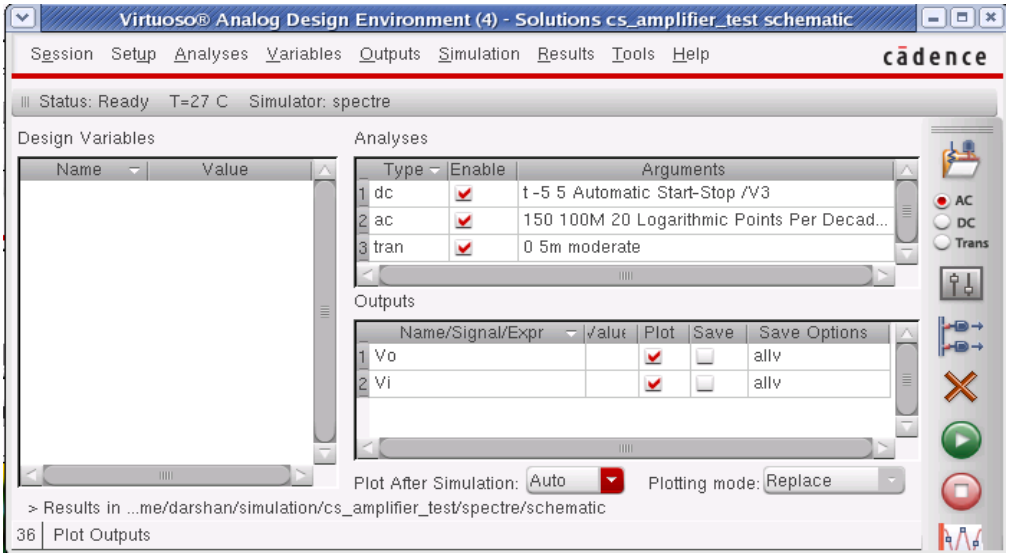
Library name	Cellview name	Properties/Comments
myDesignLib	cs_amplifier	Symbol
analogLib	vsin	Define pulse specification as AC Magnitude= 1; DC Voltage= 0; Offset Voltage= 0; Amplitude= 5m; Frequency= 1K
analogLib	vdd,vss,gnd	vdd=2.5 ; vss= -2.5 vbias=-2.5

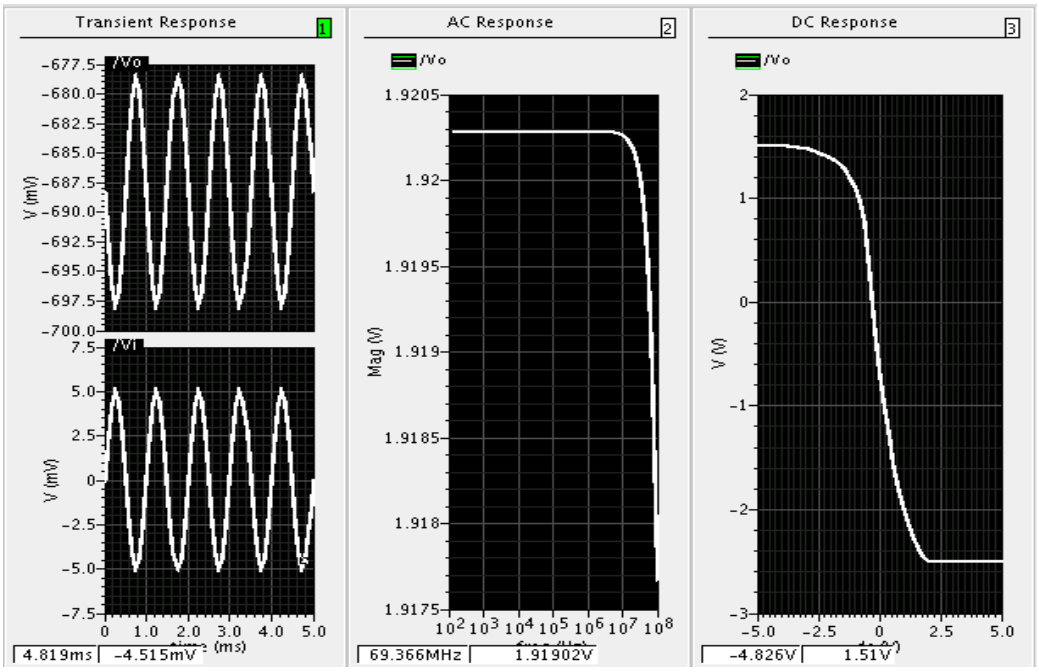


Analog Simulation with Spectre

Objective: To set up and run simulations on the cs_amplifier_test design.

Use the techniques learned in the Lab1 and Lab2 to complete the simulation of cs_amplifier, ADE window and waveform should look like below.



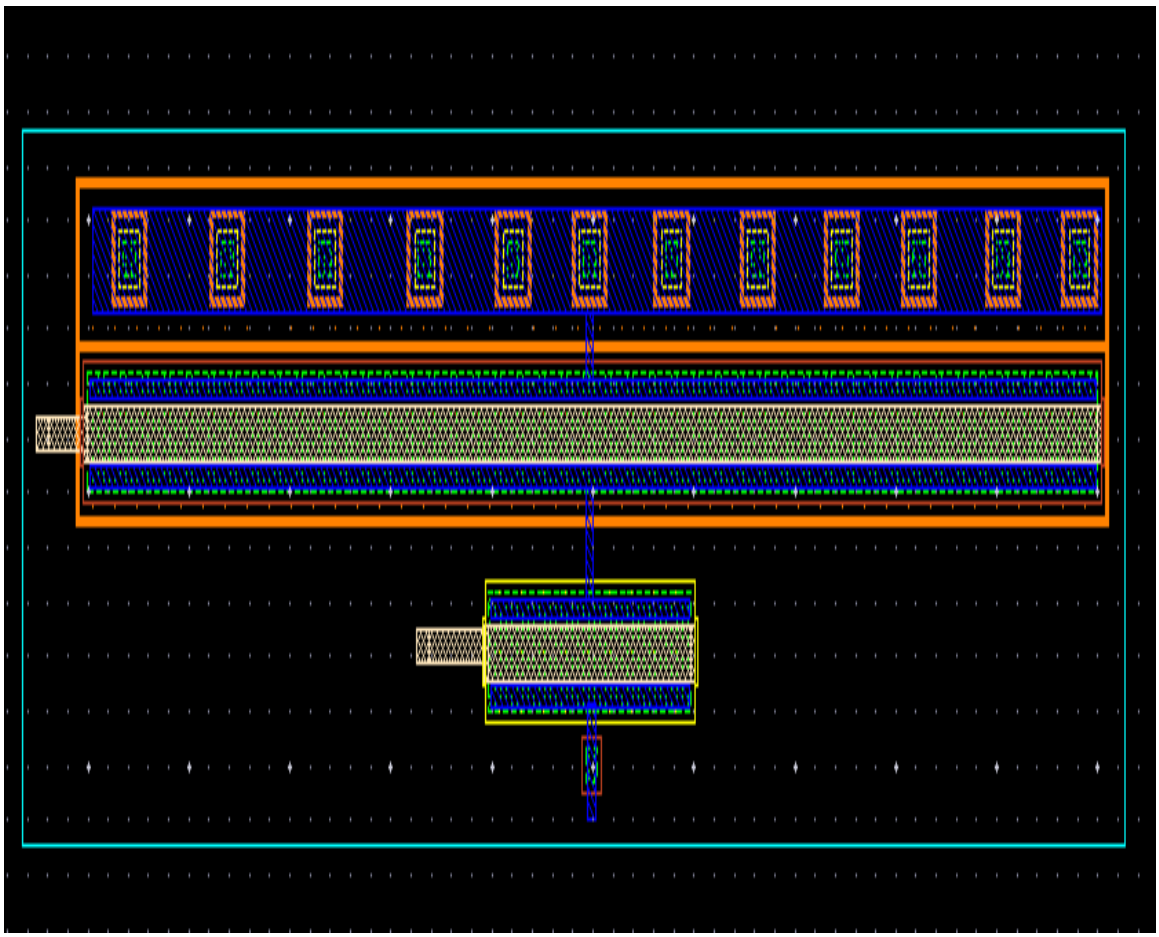


Creating a layout view of Common Source Amplifier

Use the techniques learned in the Lab1 and Lab2 to complete the layout of cs_amplifier.

Complete the DRC, LVS check using the assura tool.

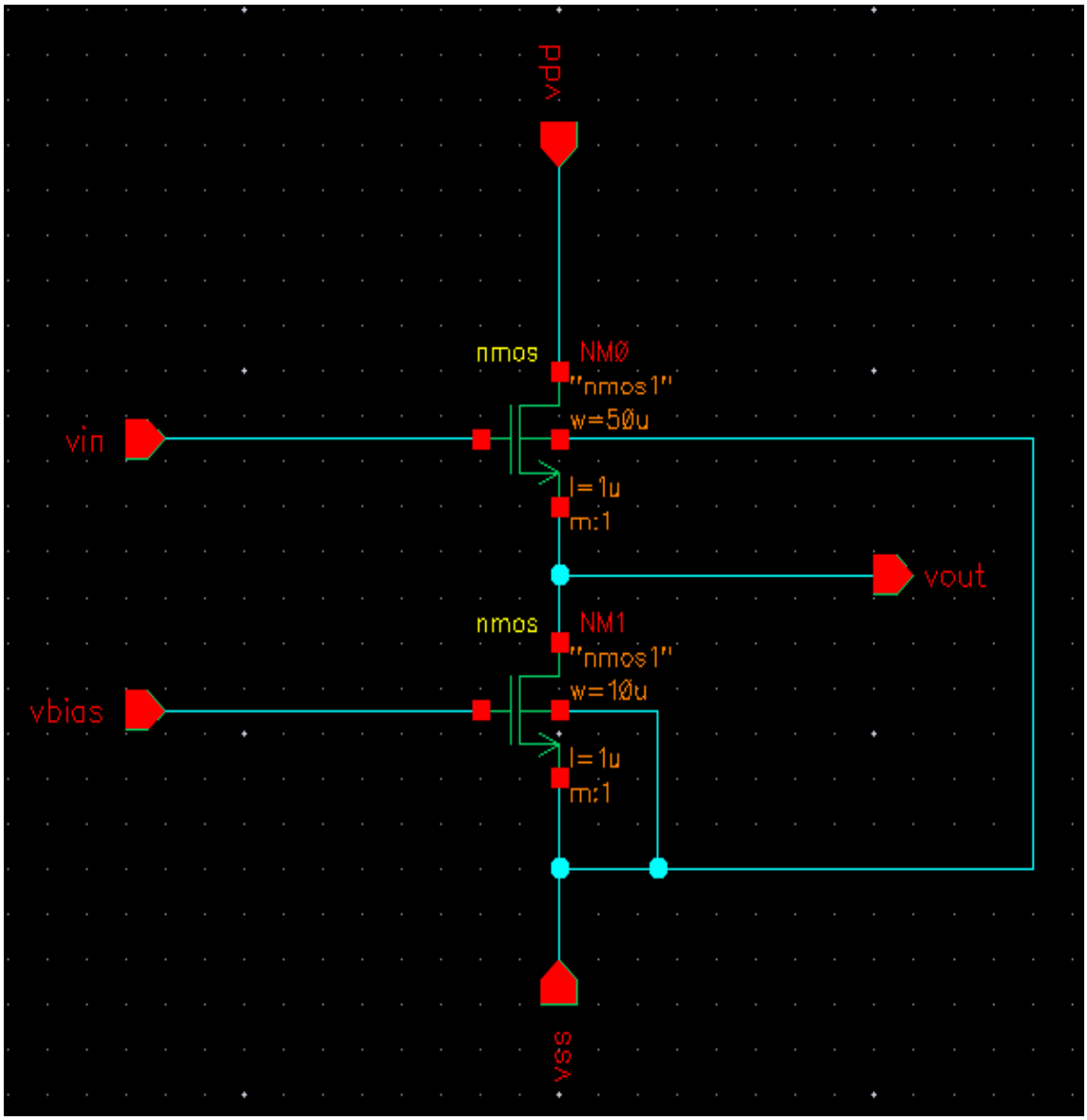
Extract RC parasites for back annotation and Re-simulation.



END OF LAB 3

Lab 4: COMMON DRAIN AMPLIFIER

Schematic Capture



Schematic Entry

Objective: To create a new cell view and build Common Drain Amplifier

Use the techniques learned in the Lab1 and Lab2 to complete the schematic of Common Drain Amplifier.
This is a table of components for building the Common Drain Amplifier schematic.

Library name	Cell Name	Properties/Comments
gpdk180	nmos	Model Name = nmos1; W= 50u ; L= 1u
gpdk180	nmos	Model Name = nmos1; W= 10u ; L= 1u

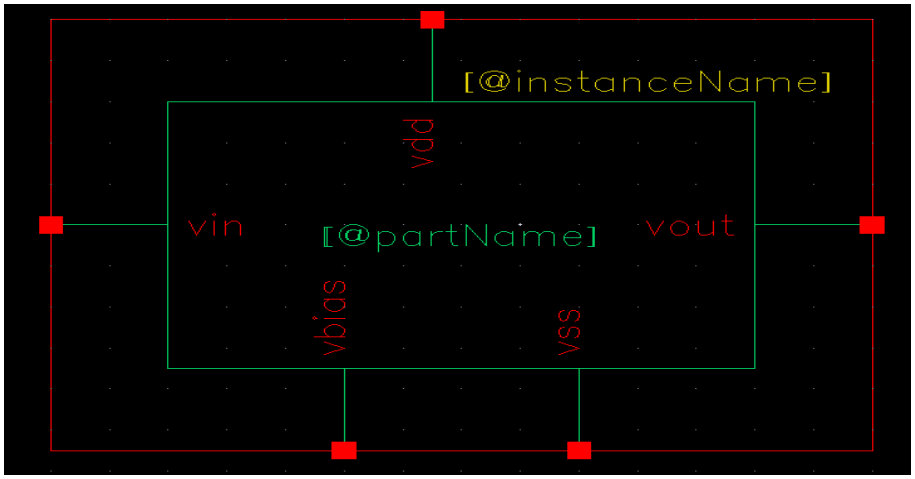
Type the following in the ADD pin form in the exact order leaving space between the pin names.

Pin Names	Direction
vin, vbias	Input
vout	Output
vdd vss	Input

Symbol Creation

Objective: To create a symbol for the Common Drain Amplifier

Use the techniques learned in the Lab1 and Lab2 to complete the symbol of cd-amplifier

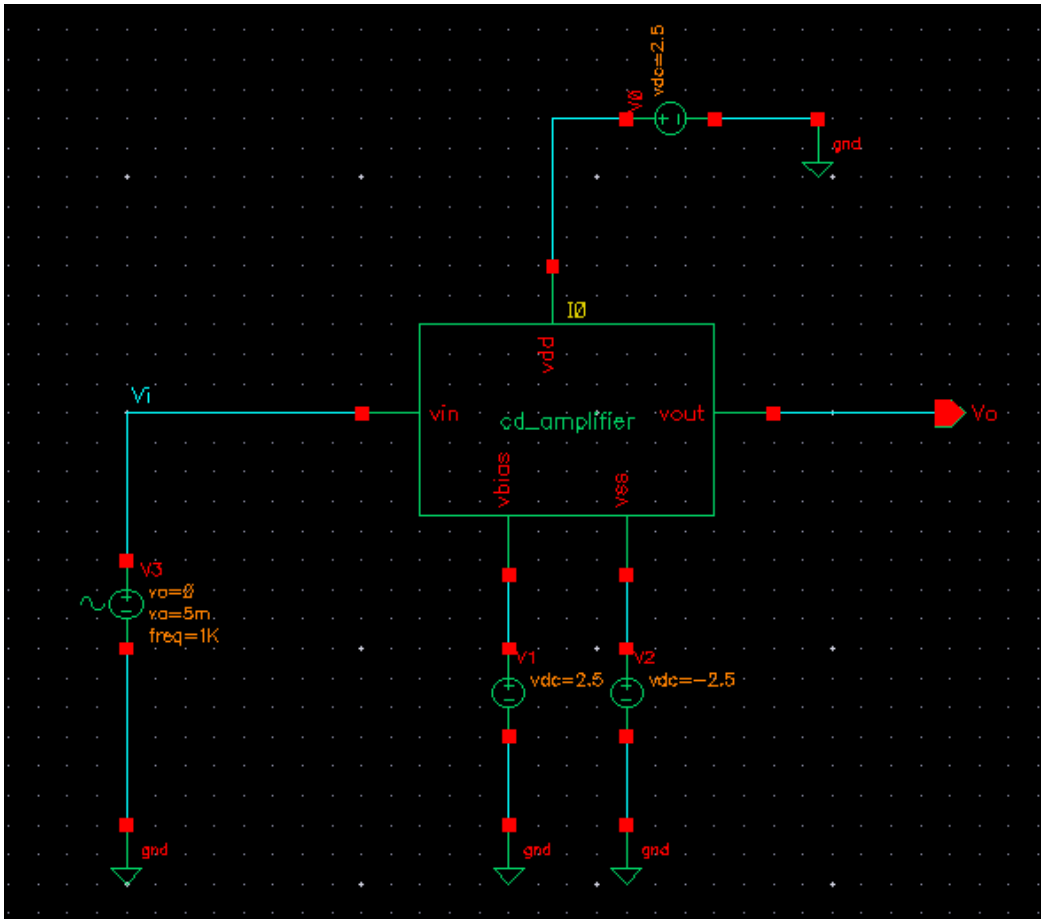


Building the Common Drain Amplifier Test Design

Objective: To build cd_amplifier_test circuit using your cd_amplifier

Using the component list and Properties/Comments in the table, build the cd-amplifier_test schematic as shown below.

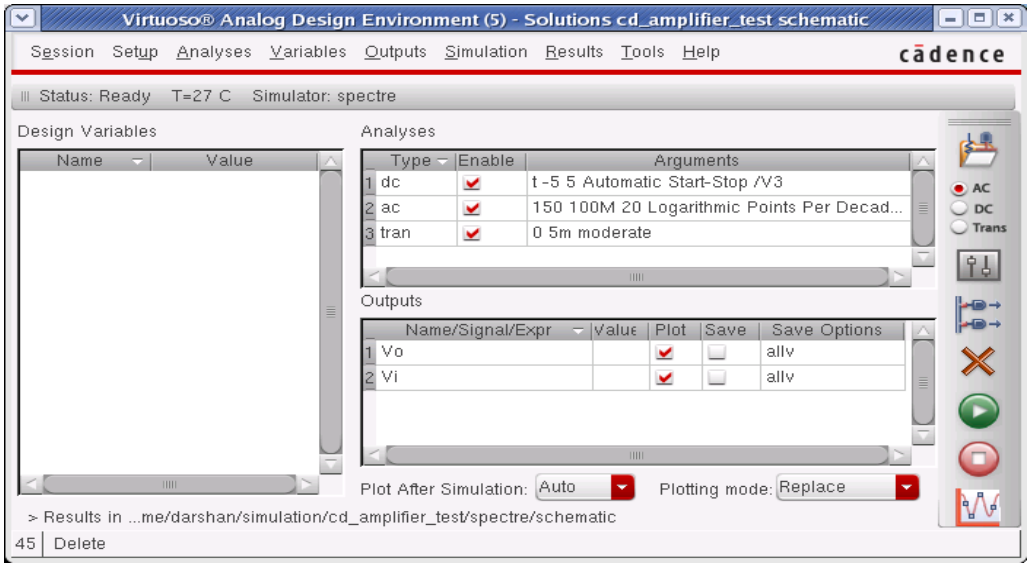
Library name	Cellview name	Properties/Comments
myDesignLib	cd_amplifier	Symbol
analogLib	vsin	Define pulse specification as AC Magnitude= 1; DC Voltage= 0; Offset Voltage= 0; Amplitude= 5m; Frequency= 1K
analogLib	vdd,vss,gnd	vdd=2.5 ; vss= -2.5

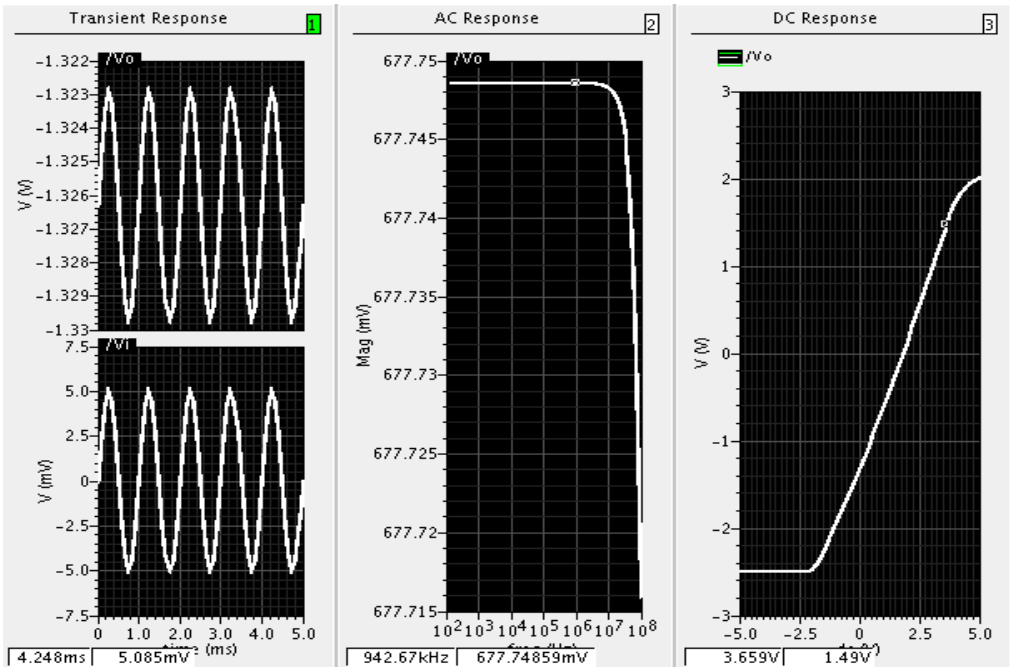


Analog Simulation with Spectre

Objective: To set up and run simulations on the cd_amplifier_test design.

Use the techniques learned in the Lab1 and Lab2 to complete the simulation of cd_amplifier, ADE window and waveform should look like below.



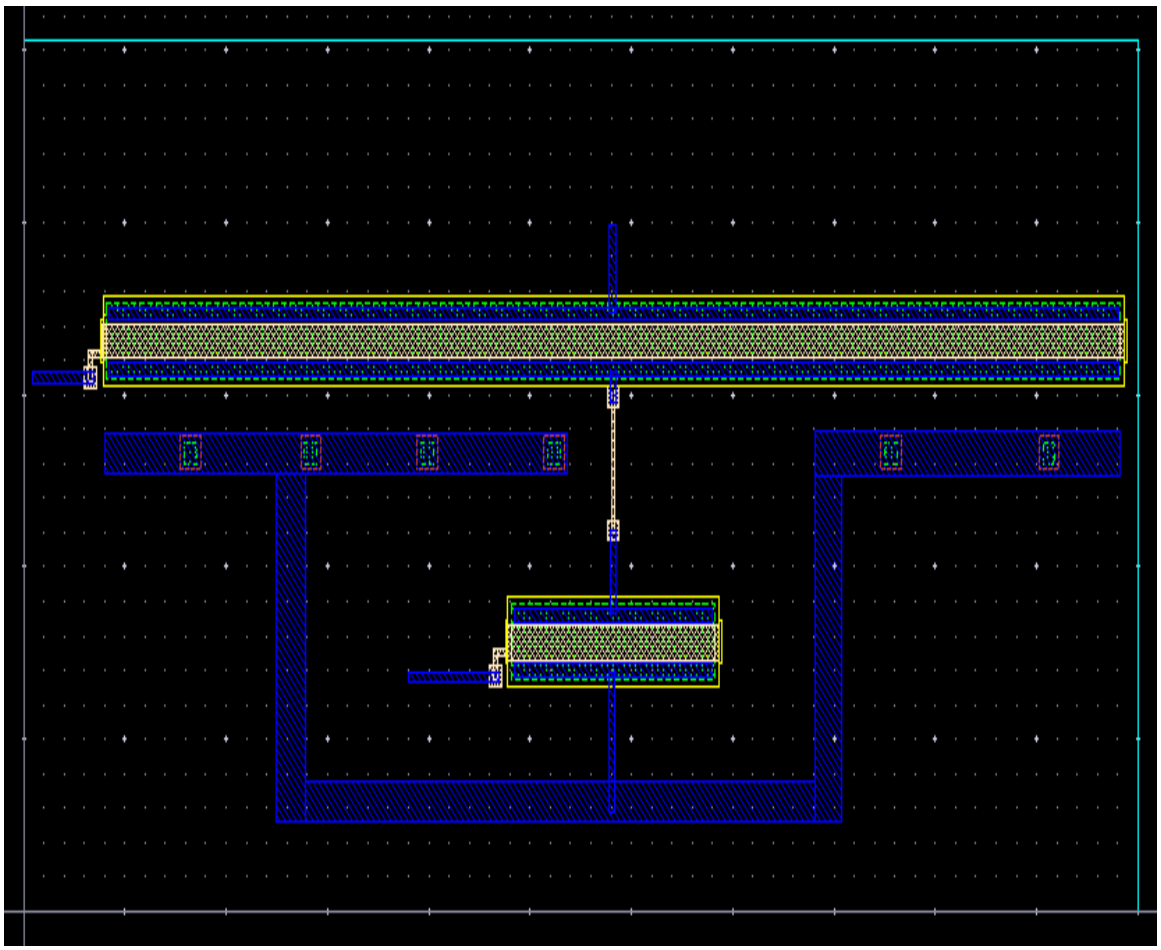


Creating a layout view of Common Drain Amplifier

Use the techniques learned in the Lab1 and Lab2 to complete the layout of cd_amplifier.

Complete the DRC, LVS check using the assura tool.

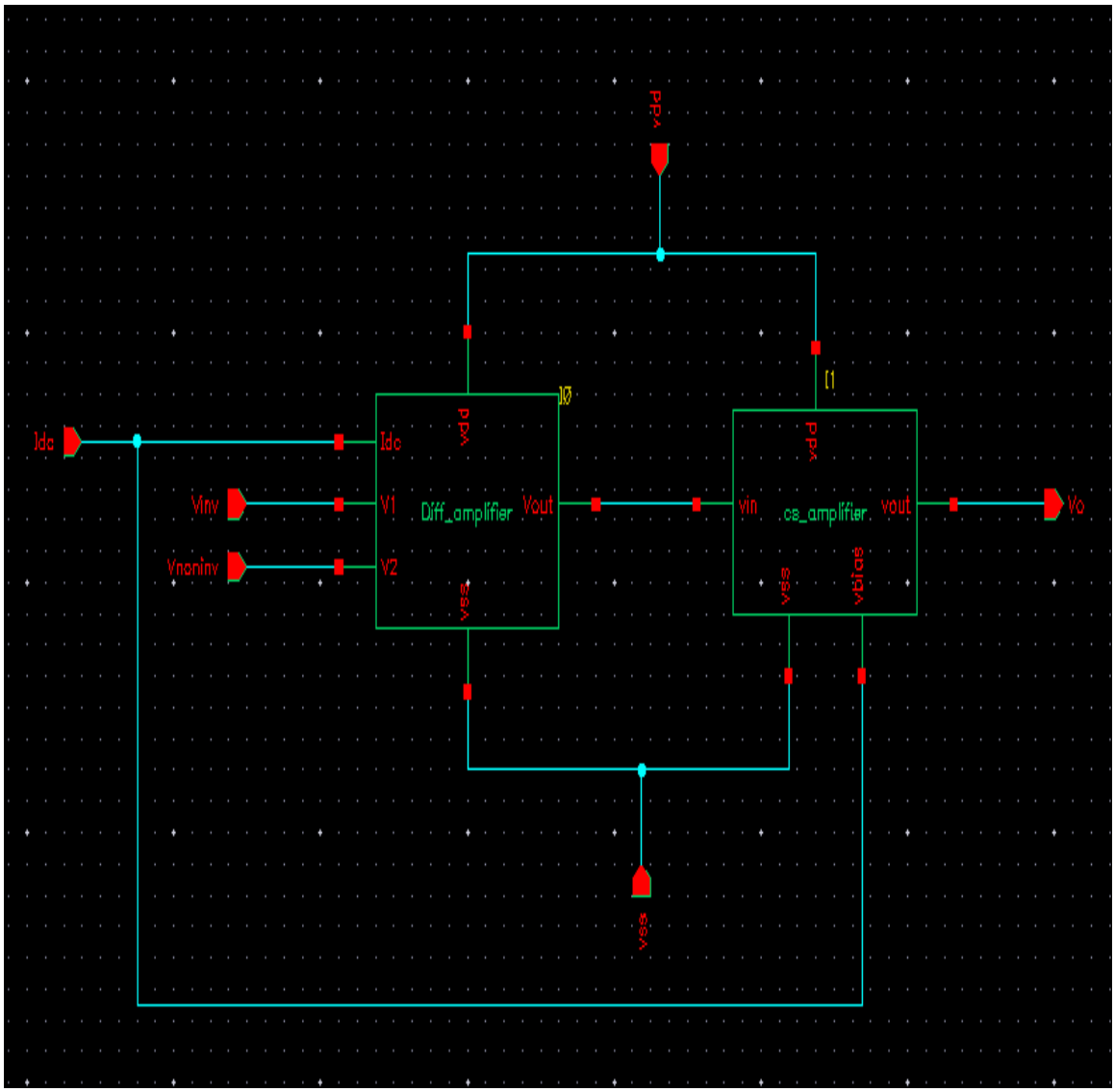
Extract RC parasites for back annotation and Re-simulation.



END OF LAB 4

Lab 5: OPERATIONAL AMPLIFIER

Schematic Capture



Schematic Entry

Objective: To create a new cell view and build Operational Amplifier

Use the techniques learned in the Lab1 and Lab2 to complete the schematic of Operational Amplifier.
This is a table of components for building the Operational Amplifier schematic.

Library name	Cell Name	Properties/Comments
myDesignLib	Diff_amplifier	Symbol
myDesignLib	cs_amplifier	Symbol

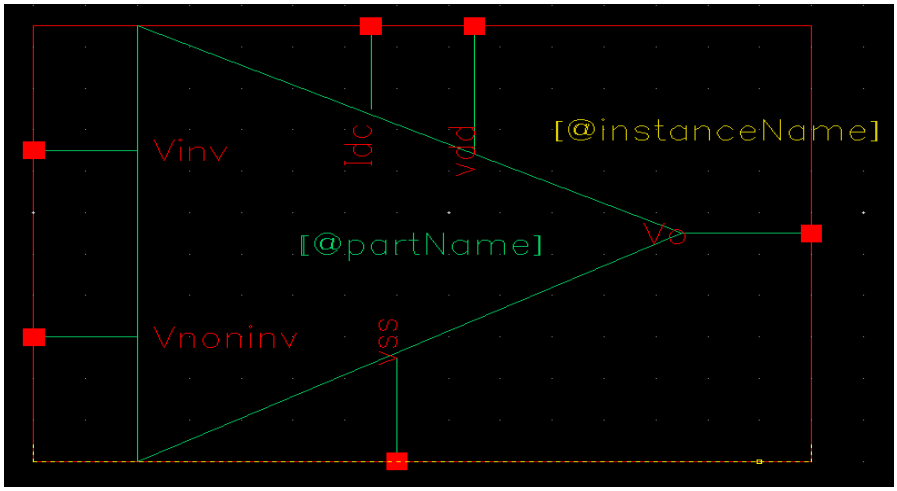
Type the following in the ADD pin form in the exact order leaving space between the pin names.

Pin Names	Direction
Idc,Vinv,Vnoninv	Input
Vo	Output
vdd, vss	Input

Symbol Creation

Objective: To create a symbol for the Operational Amplifier

Use the techniques learned in the Lab1 and Lab2 to complete the symbol of op-amp.



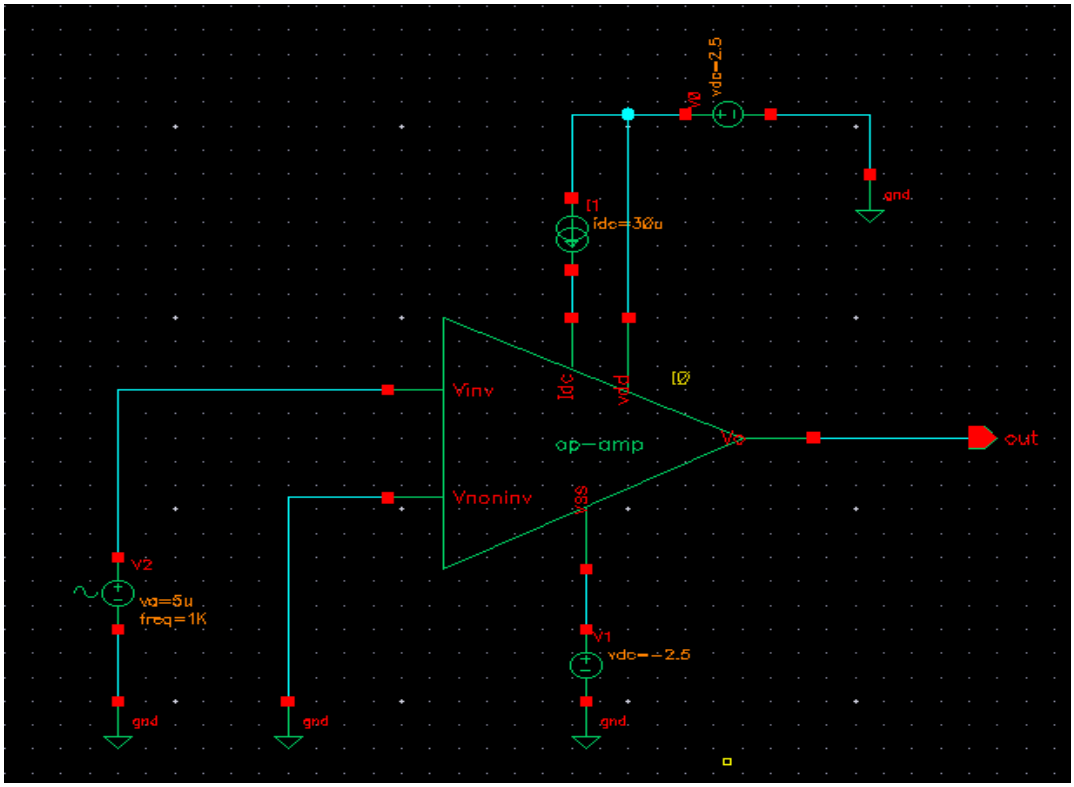
Building the Operational Amplifier Test Design

Objective: To build op-amp_test circuit using your op-amp

Using the component list and Properties/Comments in the table, build the op-amp_test schematic as shown below.

Library name	Cellview name	Properties/Comments
myDesignLib	op-amp	Symbol
analogLib	vsin	Define pulse specification as AC Magnitude= 1; DC Voltage= 0; Offset Voltage= 0; Amplitude= 5m; Frequency= 1K
analogLib	vdc, gnd	vdd=2.5 ; vss= -2.5
analogLib	Idc	Dc current = 30u

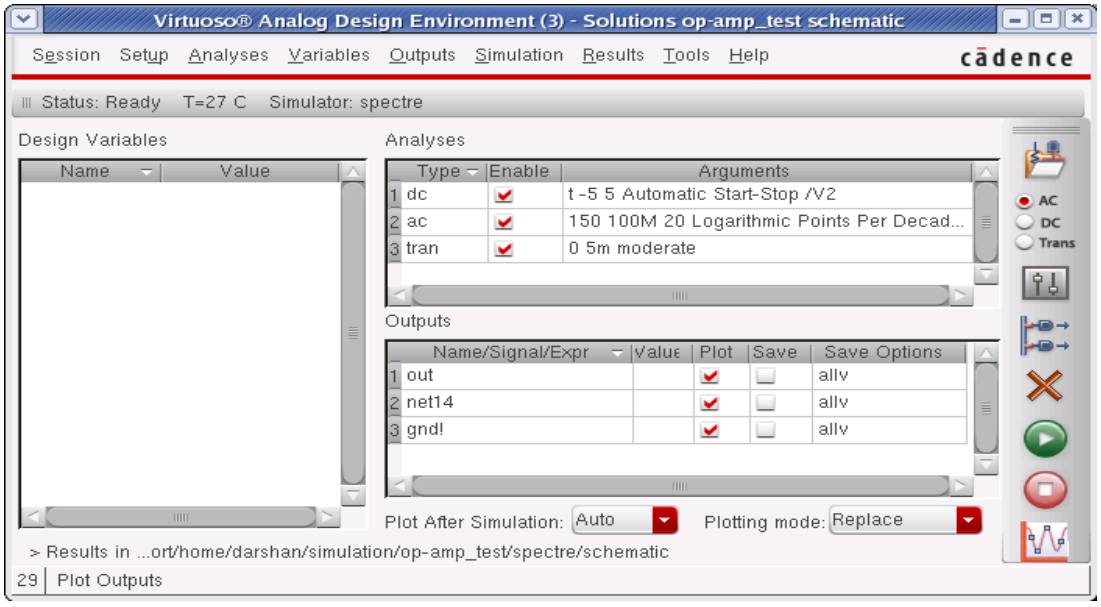
Note: Remember to set the values for **vdd** and **vss**. Otherwise your circuit will have no power.

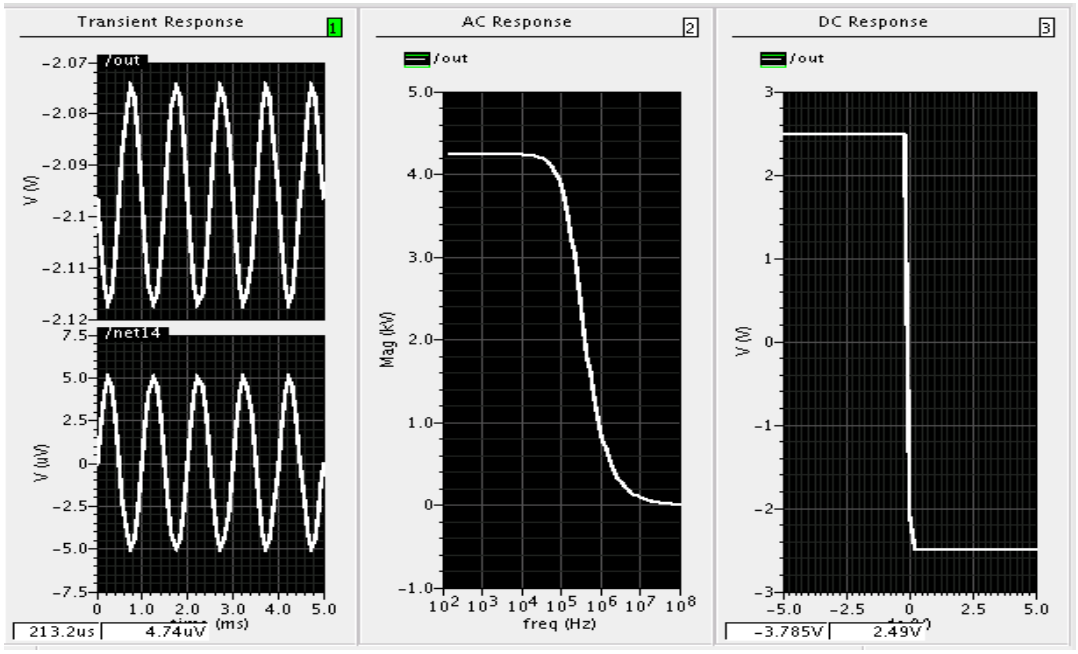


Analog Simulation with Spectre

Objective: To set up and run simulations on the op-amp_test design.

Use the techniques learned in the Lab1 and Lab2 to complete the simulation of op-amp, ADE window and waveform should look like below.



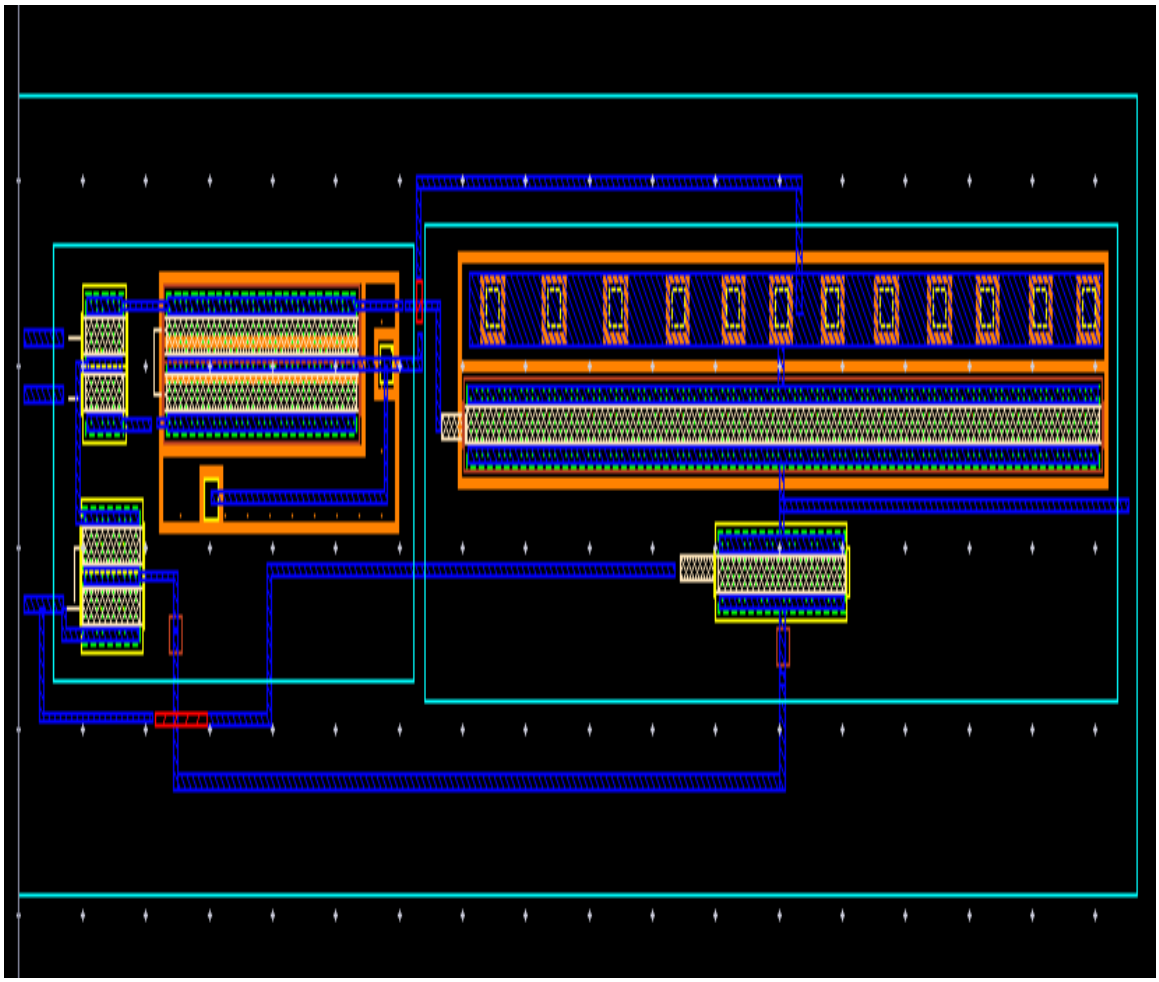


Creating a layout view of Operational Amplifier

Use the techniques learned in the Lab1 and Lab2 to complete the layout of op-amp.

Complete the DRC, LVS check using the assura tool.

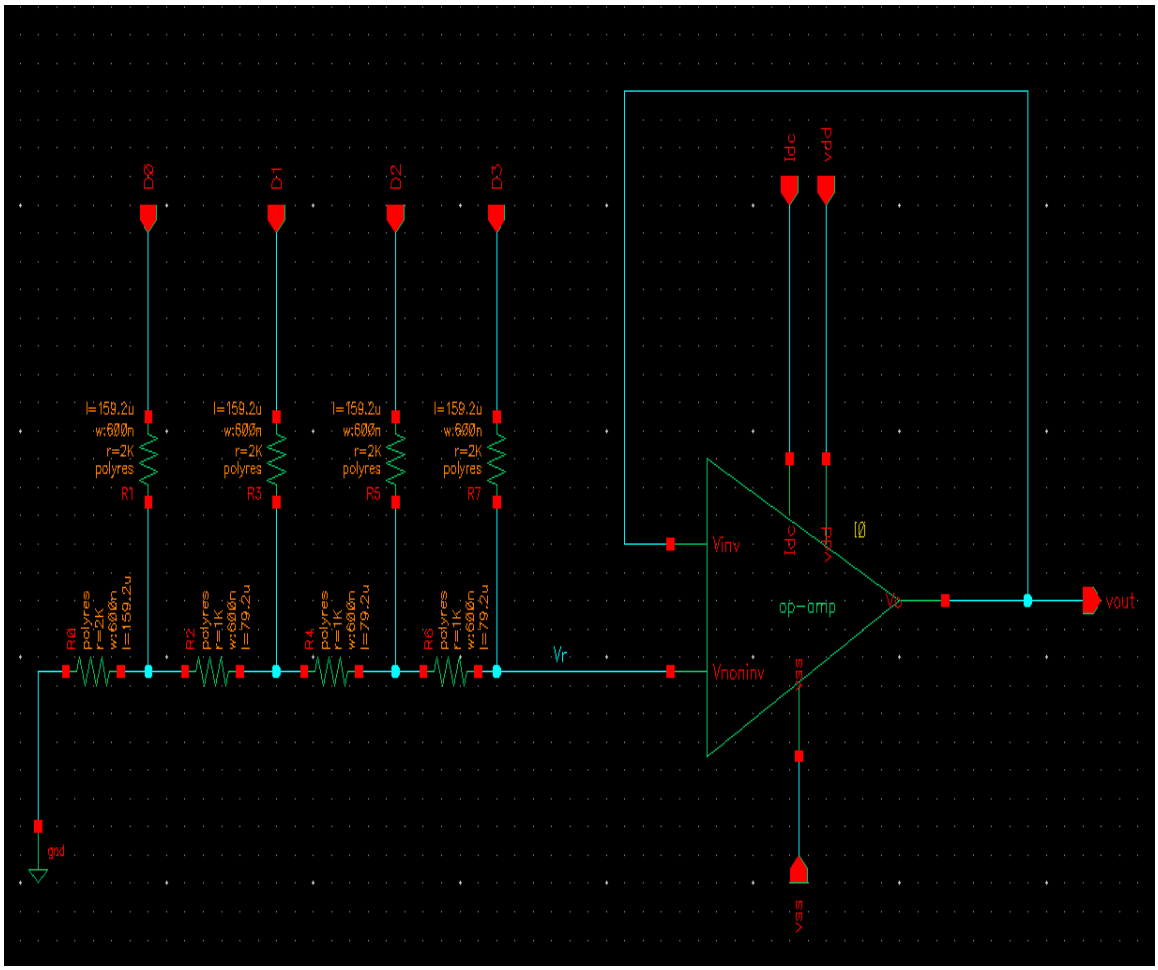
Extract RC parasites for back annotation and Re-simulation.



END OF LAB 5

Lab 6: R-2R DAC

Schematic Capture



Schematic Entry

Objective: To create a new cell view and build R-2R DAC

Use the techniques learned in the Lab1 and Lab2 to complete the schematic of R-2R DAC.
This is a table of components for building the R-2R DAC schematic.

Library name	Cell Name	Properties/Comments
gpdk180	polyres	R = 2k
gpdk180	polyres	R = 1k
MyDesignLib	op-amp	Symbol
analogLib	Idc, gnd	idc = 30u

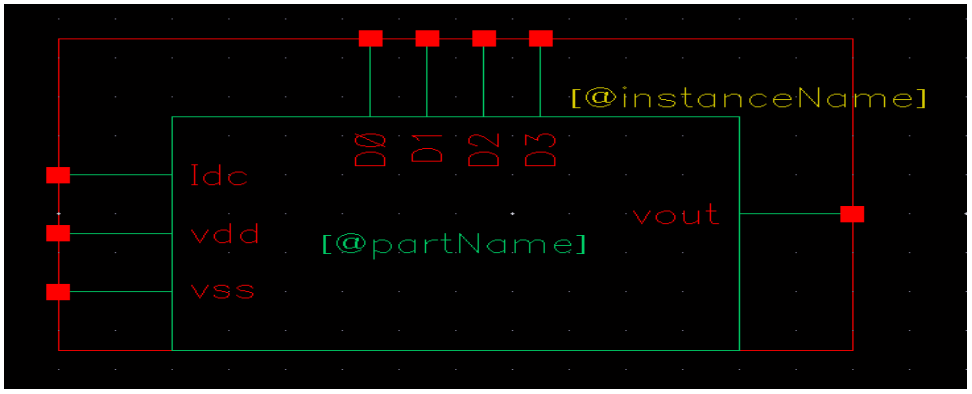
Type the following in the ADD pin form in the exact order leaving space between the pin names.

Pin Names	Direction
Do D1 D2 D3	Input
Vout	Output
vdd, vss	Input

Symbol Creation

Objective: To create a symbol for the R-2R DAC

Use the techniques learned in the Lab1 and Lab2 to complete the symbol of R-2R DAC.



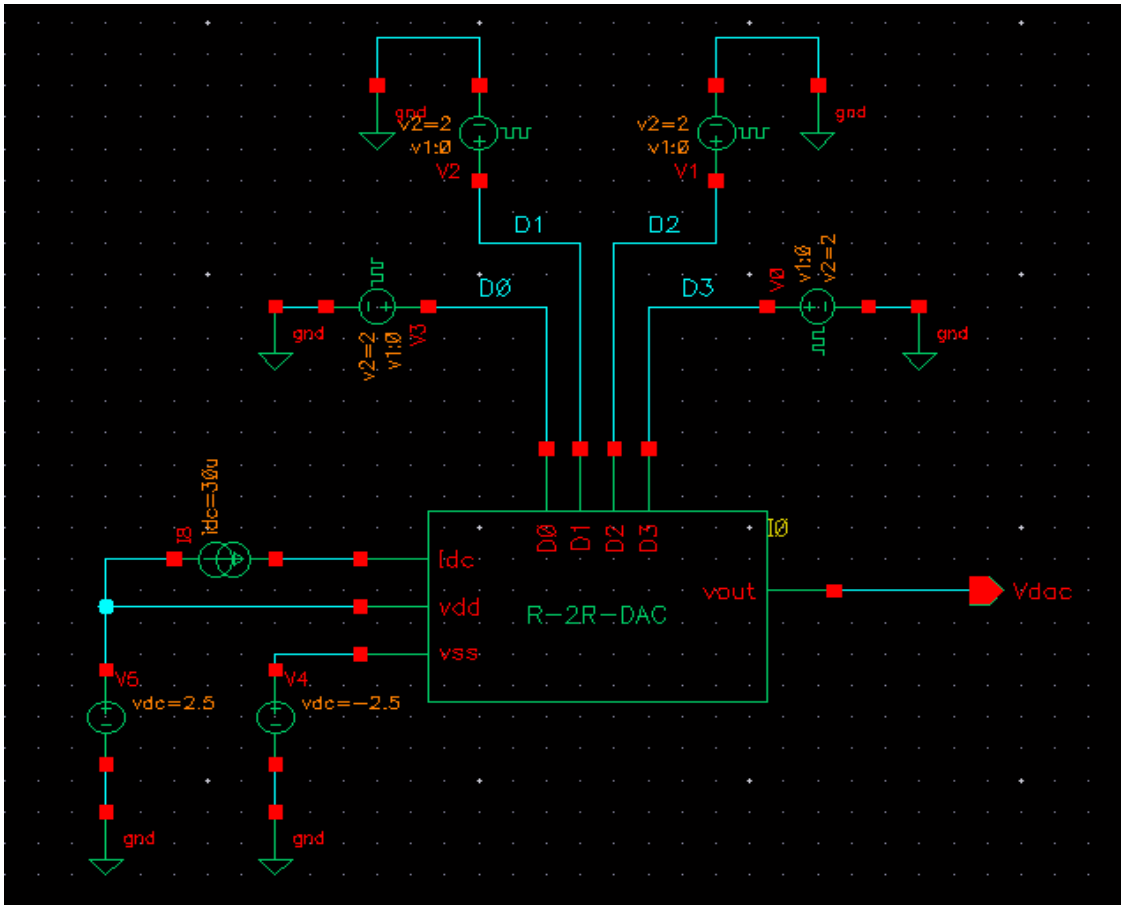
Building the R-2R DAC Test Design

Objective: To build R-2R DAC Test circuit using your R-2R DAC

Using the component list and Properties/Comments in the table,
build the R-2R-DAC_test schematic as shown below.

Library name	Cellview name	Properties/Comments
myDesignLib	R-2R-DAC	Symbol
analogLib	vpulse	For V0: v1= 0 v2 = 2 Ton = 5n T = 10n For V1: v1= 0 v2 = 2 Ton = 10n T = 20n For V2: v1= 0 v2 = 2 Ton = 20n T = 40n For V3: v1= 0 v2 = 2 Ton = 40n T = 80n
analogLib	vdc, gnd	vdd = 2 vss = -2

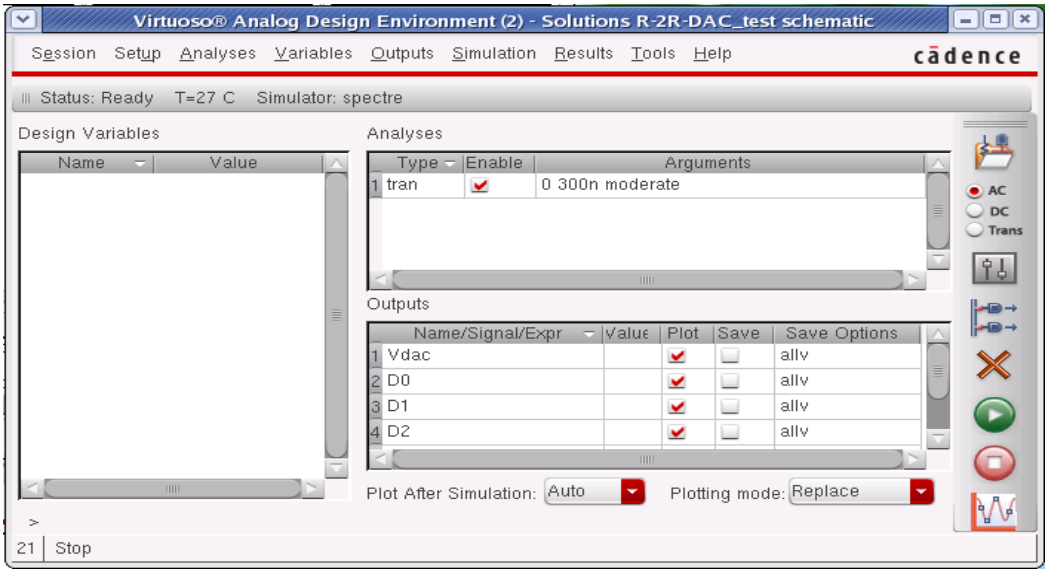
Note: Remember to set the values for **vdd** and **vss**. Otherwise your circuit will have no power.

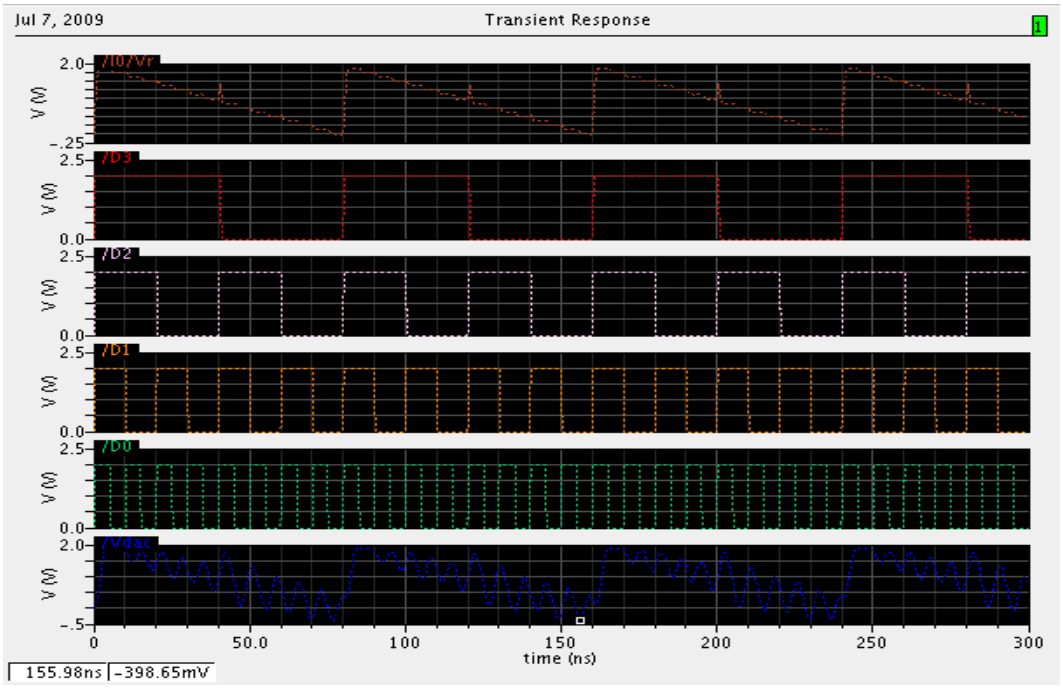


Analog Simulation with Spectre

Objective: To set up and run simulations on the R-2R-DAC_Test design.

Use the techniques learned in the Lab1 and Lab2 to complete the simulation of R-2R-DAC and ADE window and waveform should look like below.



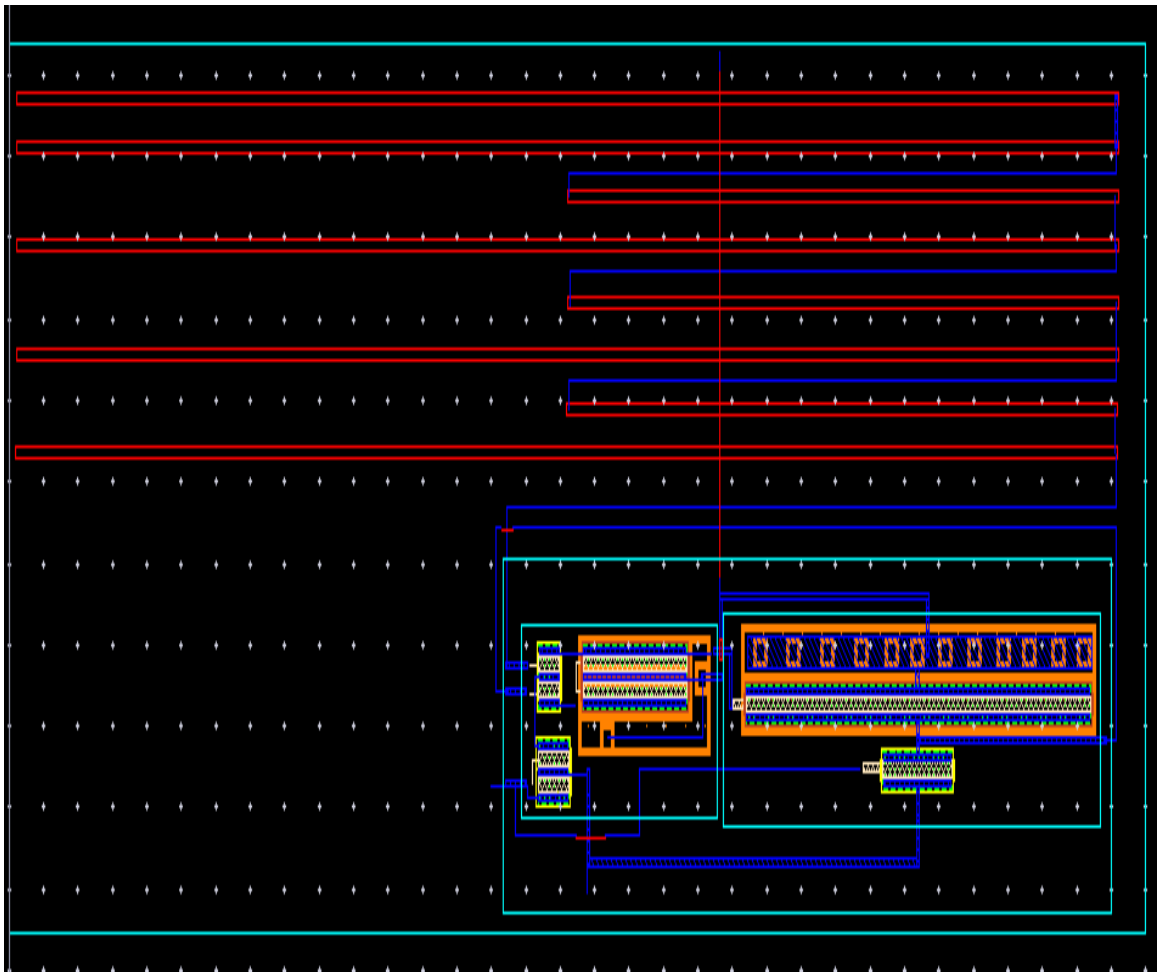


Creating a layout view of R-2R DAC

Use the techniques learned in the Lab1 and Lab2 to complete the layout of R-2R-DAC.

Complete the DRC, LVS check using the assura tool.

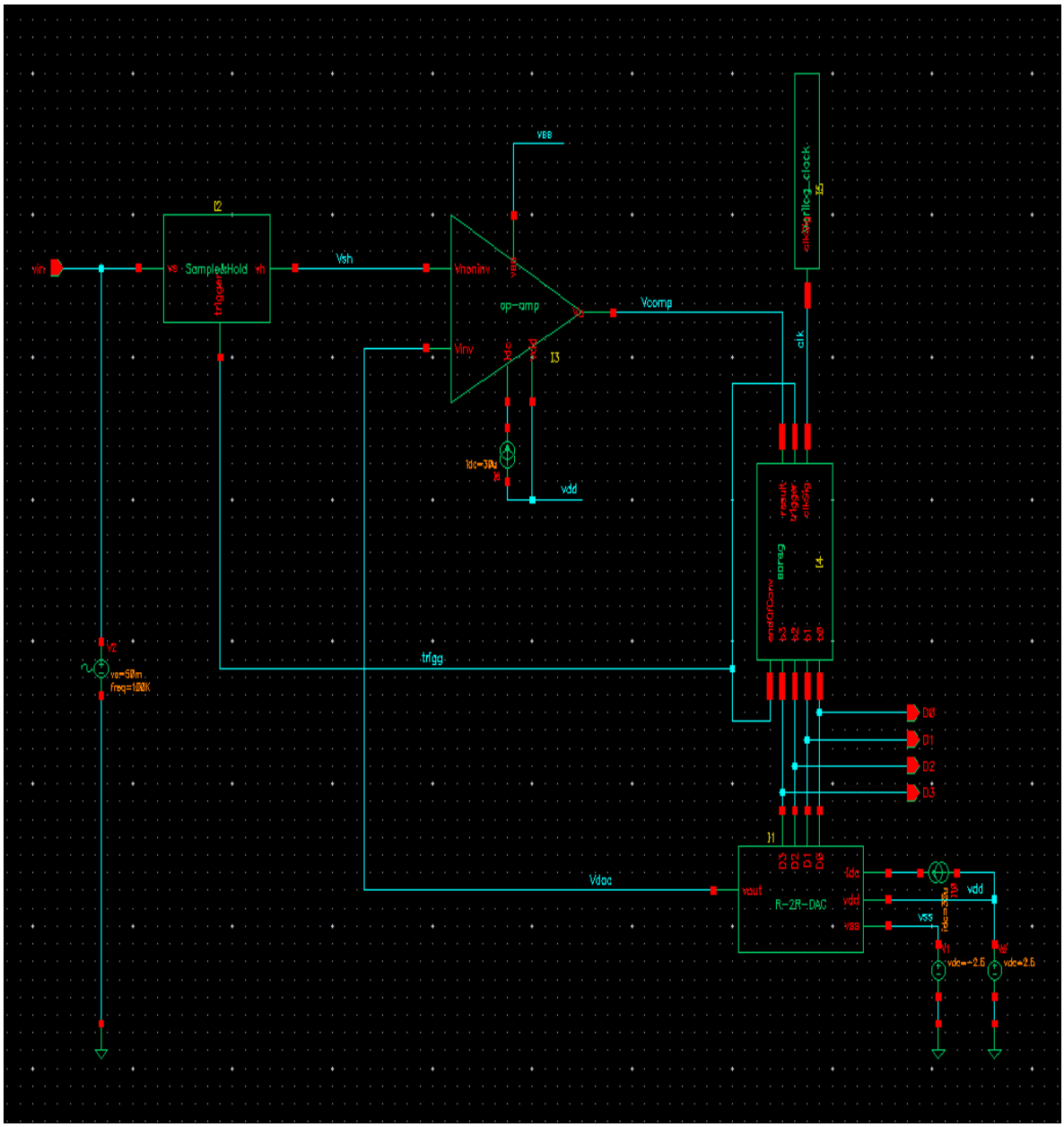
Extract RC parasites for back annotation and Re-simulation.



END OF LAB 6

Lab 7: SAR BASED ADC

Schematic Capture



Design Information

The SAR Based ADC used in this tutorial is a mixed-signal circuit that includes both a schematic database and verilog code. The analog components include a vsin signal source, a sample and hold circuit(S/H), a comparator and a R-2R DAC all based on the schematic. The successive approximation register (SAR) and clock generator are RTL-level verilog modules.

The key files and directories required are:

1. The cds.lib file defines the design libraries and associates logical library names with physical library locations.

2. The hdl.var file defines the variables that affect the behavior of tools and utilities.

3. The myDesignLib library stores the Digital blocks for the schematic database.

4. The dig_source directory stores the behavioral Verilog code for SAR and Clock generator.

The AMS Designer Simulator

The Virtuoso® AMS simulator is a mixed-signal simulator that supports the Verilog®-AMS language standard.

Import the Verilog Module into ADE Using Verilog In

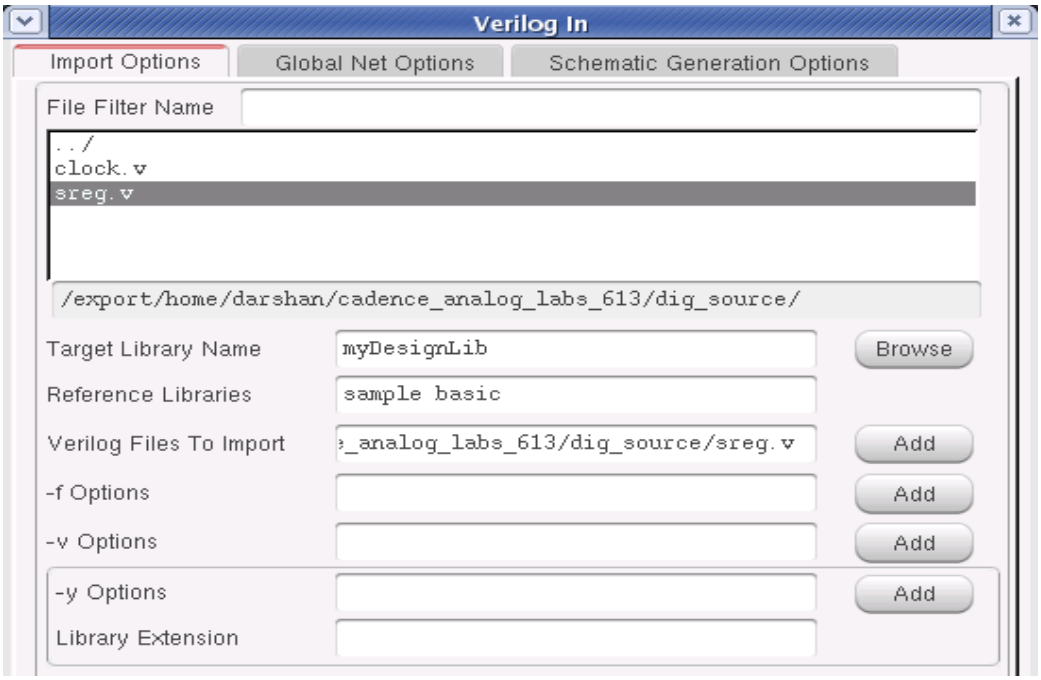
1. In a terminal window, change directory to the dig_source directory where there are 2 Verilog modules.

sreg.v ------------------------------ Succesive Approximation Register
clock.v ------------------------------ Divider with factor 2, used for SAR input clock

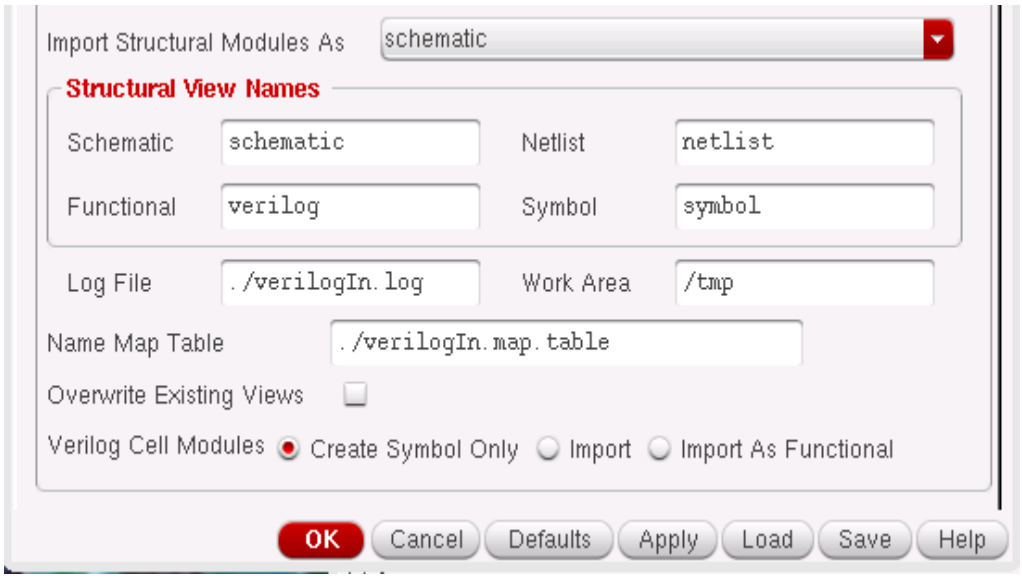
2. In the **CIW or Virtuoso** window, click **File — Import — Verilog**

A **Verilog In** form appears.

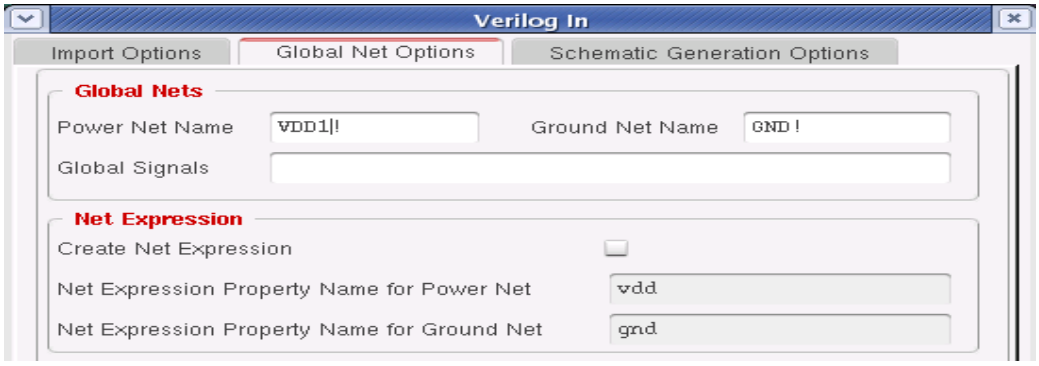
3. In the Verilog In form, **double-click on the dig_source directory**, then click on the **sreg.v** file, type **myDesignLib** in the Target Library Name field (or use the browser to specify it) and click **Add** to the right of the **Verilog Files To Import field**. The full path of this verilog file appears in the field. Next click **clock.v** file and click **Add** next to the same verilog files to Import field. **clock.v** will be added to the field after the **sreg.v** file.



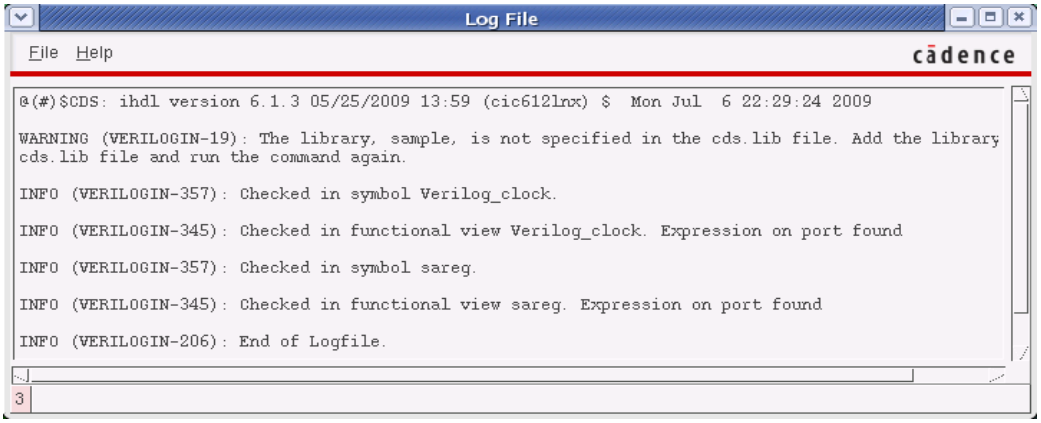
4. Scroll down the form to Structural View Names and change the view name in the Functional field to **verilog.**



5. In the **Power Net Name** field under **Global Net Option** tab of the **Verilog In** form, change **VDD!** to **VDD1!** and click **OK** in the **Verilog In** form.



6. When the import is complete, a message appears asking if you want to see the log file. Click **Yes** to display the log file window.



You see error or warning messages in this log file if something is wrong during the import process.

7. Close the log file window. Click **Tools — Library Manager** to open the Library Manager. Click **View — Refresh**.

In the Library column, click **myDesignLib** to show all the cells in it. In the Cell column, two new cells (**sreg** and **Verilog_clock**) are generated.

Schematic Entry

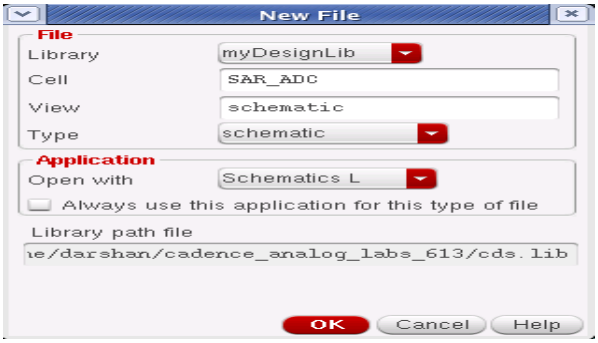
Objective: To create a new cell view and build SAR Based ADC

Creating a Schematic cellview

Open a new schematic window in the **myDesignLib** library and build the SAR Based ADC design.

1. In the CIW or Library manager, execute **File – New – Cellview**.

2. Set up the Create New file form as follows:



3. Click **OK** when done. A blank schematic window for the design appears.

Adding Components to schematic

1. In the SAR_ADC schematic window, execute **Create— Instance** or  to display the Add Instance form.

2. Click on the **Browse** button. This opens up a Library browser from which you can select components and the **Symbol** view .

You will update the Library Name, Cell Name, and the property values given in the table on the next page as you place each component.

3. After you complete the Add Instance form, move your cursor to the schematic window and click **left** to place a component.

This is a table of components for building the **SAR_ADC** schematic.

Library name	Cell Name	Properties/Comments
myDesignLib	Sample&Hold	Symbol
myDesignLib	Op-amp	Symbol
myDesignLib	Verilog_clock	Symbol
myDesignLib	sareg	Symbol
myDesignLib	R-2R-DAC	Symbol
analogLib	vdc, idc, gnd	vdc=2.5, idc=30u
analogLib	vsin	mag =1, amp=50m, f=100k

3. After entering components, click **Cancel** in the Add Instance form
or press **Esc** with your cursor in the schematic window

Adding pins to Schematic

Use **Create – Pin** or the menu icon to place the pins on the schematic window.

1. Click the **Pin** fixed menu icon in the schematic window. 
You can also execute **Create – Pin** or press **p**. The Add pin form appears.

2. Type the following in the Add pin form in the exact order leaving space between the pin names.

Pin Names	Direction
Vin	Input
D0 D1 D2 D3	Output

Make sure that the direction field is set to **input/ouput/inputoutput** when placing the **input/output/inout** pins respectively and the Usage field is set to **schematic**.

3. Select **Cancel** from the Add pin form after placing the pins.
In the schematic window, execute **View— Fit** or press the **f** bindkey.

Adding Wires to a Schematic

Add wires to connect components and pins in the design.

1. Click the **Wire (narrow)** icon in the schematic window. 
You can also press the **w** key, or execute **Create - Wire (narrow).**

2. Complete the wiring as shown in figure and when done wiring press **ESC** key in the schematic window to cancel wiring.

Saving the Design

1. Click the ***Check and Save*** icon in the schematic editor window.

2. Observe the CIW output area for any errors.

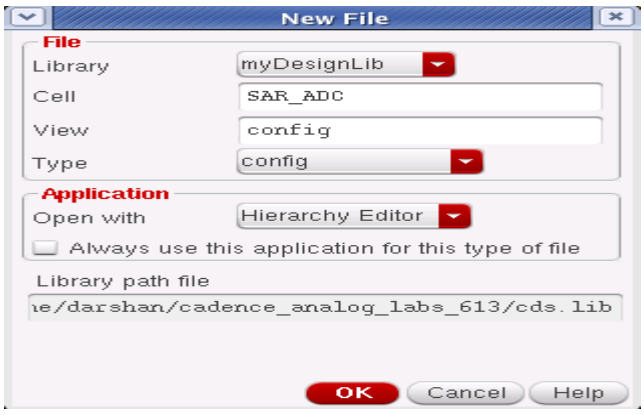
Mixed Signal Simulation Using AMS in ADE

Set Up a Configuration to Run Simulations from ADE

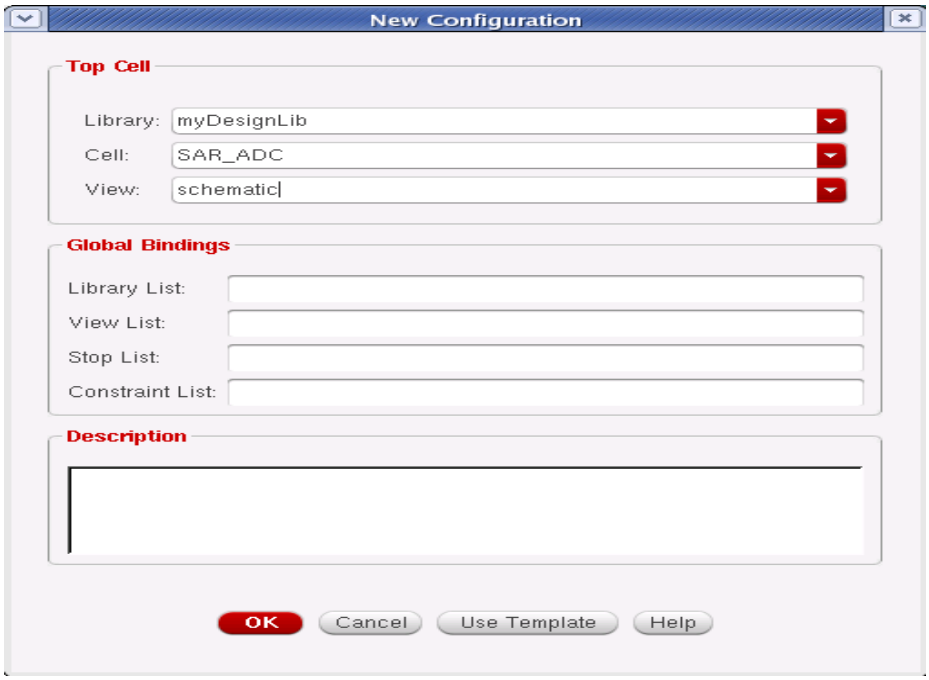
1. In the Library Manager, click the library: **myDesignLib**, cell: **SAR_ADC**.

2. Highlight SAR_ADC schematic in the Library Manager
and click **File — New — Cell View.**

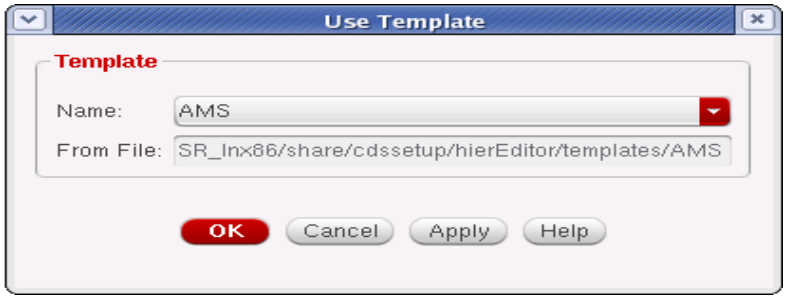
3. In **Create New File** form, select **config** option in the **Type** field. The form should look like the following figure:



4. Click **OK**. A New Configuration form opens. Enter schematic as the Top Cell View or click **Browse** button to select it. Next, click **Use Template** at the bottom of the form**.**



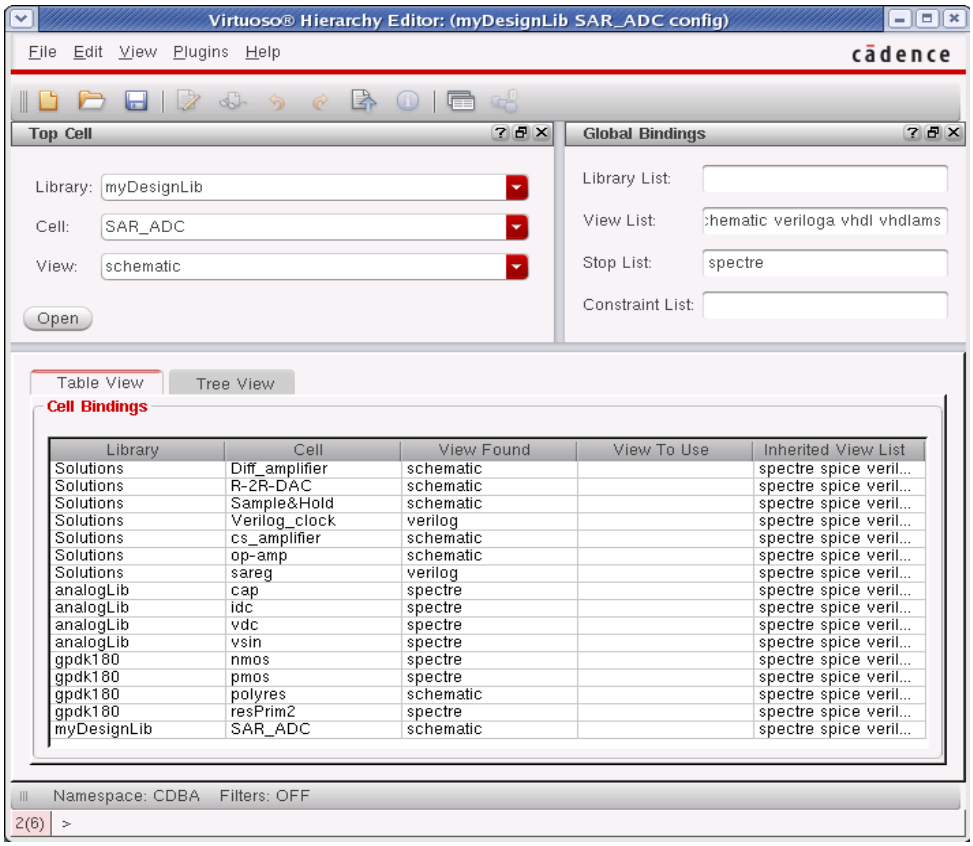
5. Select **AMS** in the Template Name field and click **OK**. Click **OK** on the **New Configuration** form as well.



The hierarchy editor is filled with values for global bindings taken from the **New Configuration** form. The cells in the design are bound to views depending on

- Which views of the cell exist
- Which existing view comes first in the view list

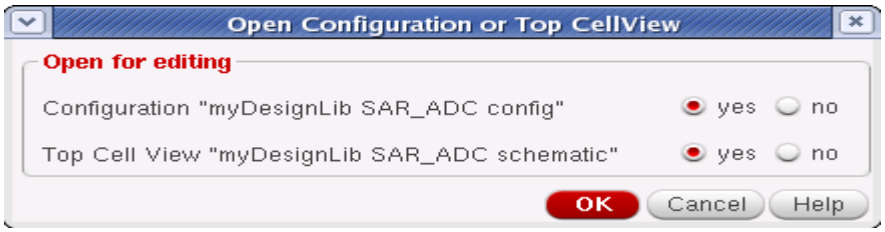
6. Click **File - Save (Needed)** to save the configuration. The update icon in the menu changes as shown in the hierarchy editor. Click the update icon.



7. Close the schematic and exit the hierarchy editor.

Set Up ADE Options and Customize the Connect Module

1. In the Library Manager, double-click config view in the View column.
The **Open Configuration or Top CellView** form opens.

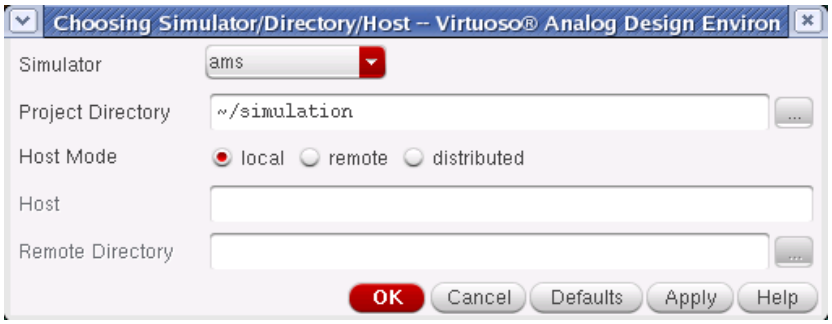


2. Under Open for editing, click **yes** for configuration “SAR_ADC_Test config” and click **yes** for open the Top Cell View “SAR_ADC_Test schematic” and click **OK**.

Both Configuration and schematic window appears.

3. Execute **Launch – ADE L** from schematic window to open the Analog Design Environment (ADE) window.

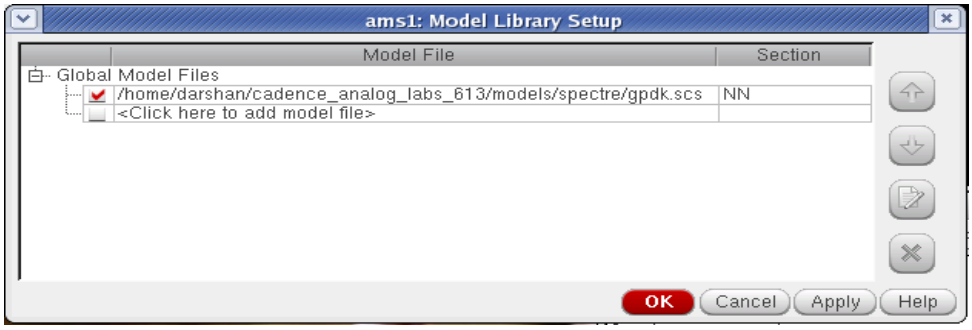
4. In the ADE window, click **Setup Simulator/Directory/Host** and set the simulator to **ams** in the Simulator cyclic field. Click **OK**.



In the upper right corner of the ADE window, confirm that simulator is ams(Spectre). If not, click **Simulation — Solver**, change the solver to spectre and click **OK**.

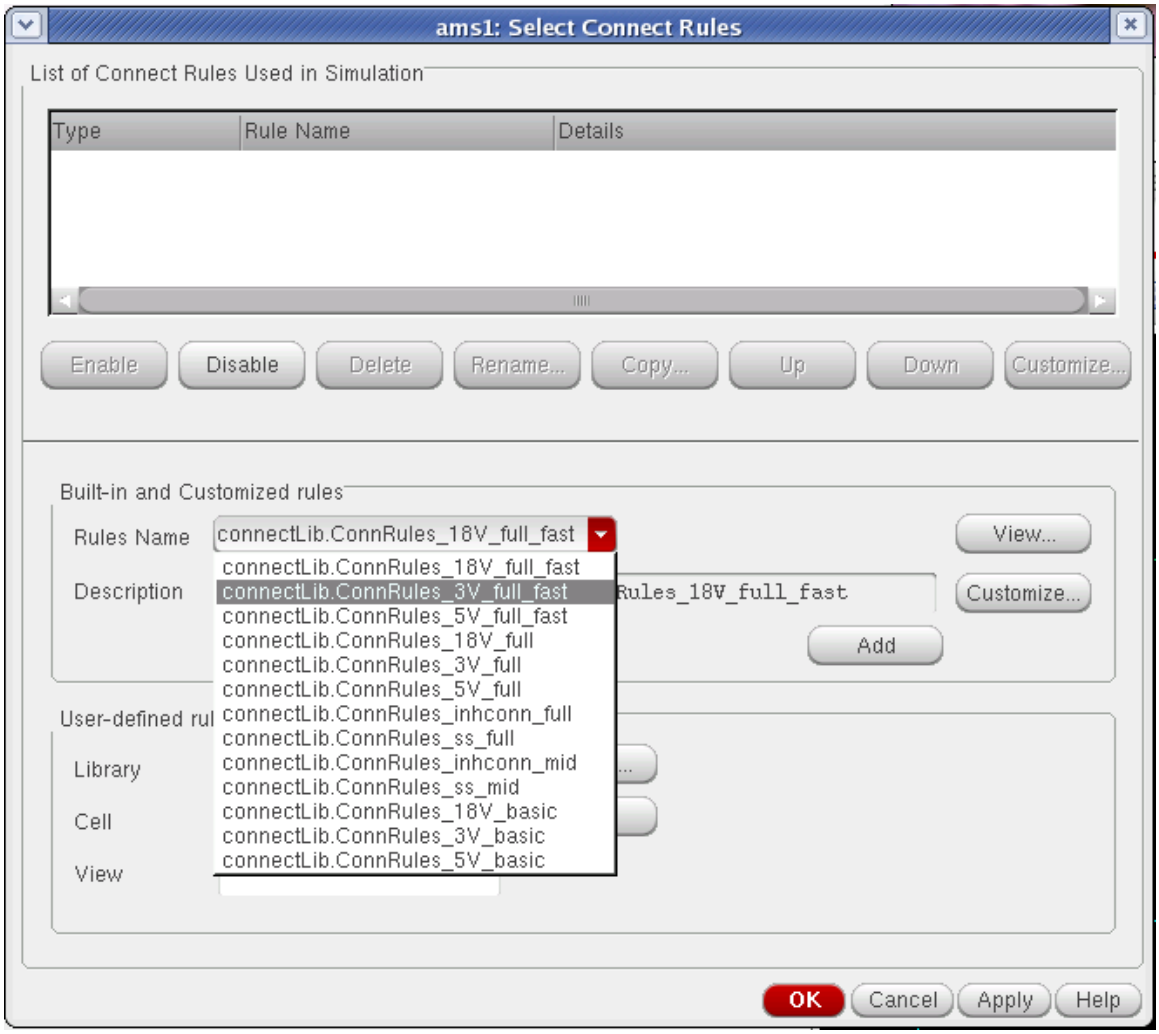
5. Click **Analyses — Choose**. Then type **30u** in **Stop Time** field of **tran** analysis. Click **Enabled** and click **OK**.

6. Click **Setup - Model Libraries**. In the Model Library Setup form, click Browse and find the **gpdk180.scs** file in the **./models/spectre** directory. Type **NN** in Section field, click **Add** and click **OK**.



7. Click **Setup — Connect Rules**. In the Select Connect Rules form, highlight **ConnRules_18V_full_fast** in the **List of Connect Rules Used in Simulation** and click **Delete** to remove the default selection. In the **Built-in rules** section, click **connectLib. ConnRules_3V_full_fast** in the Rules Name cyclic field.

Because the power supply in this SAR is **2.5V**, which doesn't exist in the Built-in rules list, you need to customize the rule.

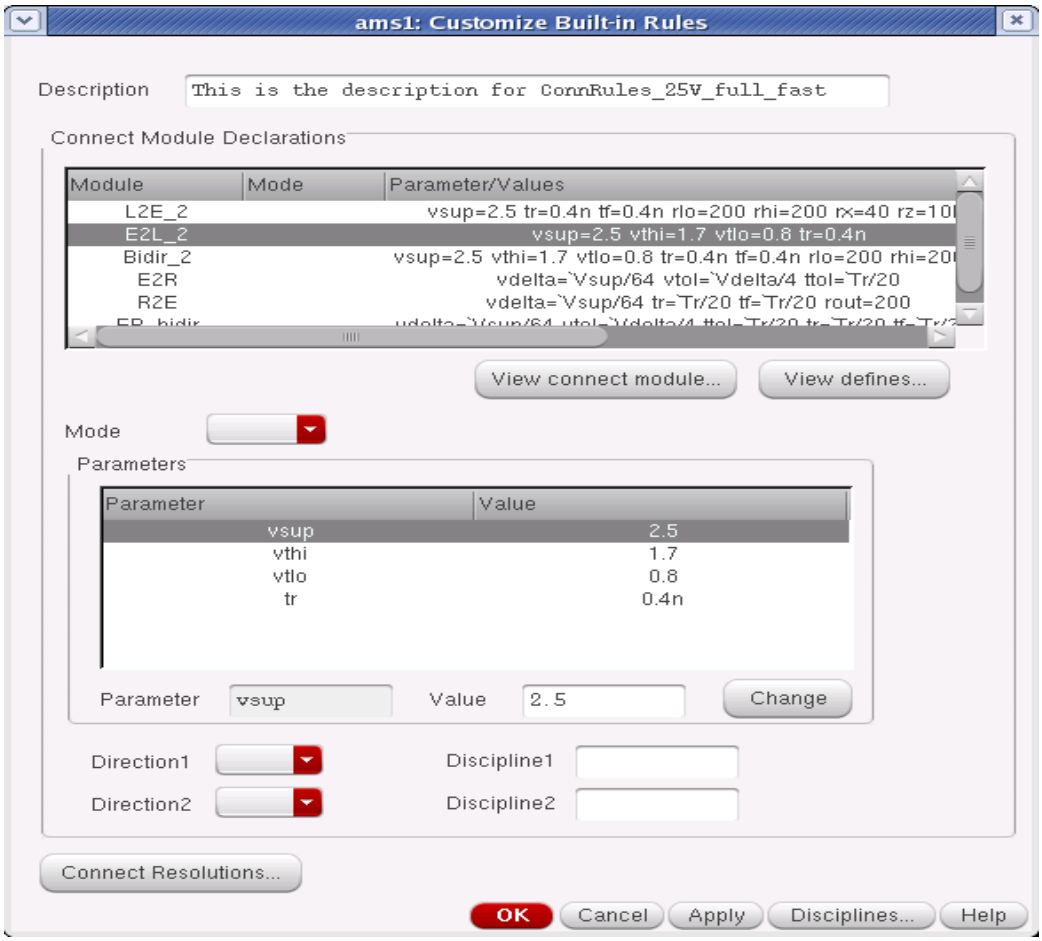


8. Click **Customize** in the above form. In the Customize Built-in Rules form, change the Description to "**This is the description for My_ConnRules_25V_full_fast**"
In the Connect Module Declarations list, click on **L2E_2**.
In the Parameters list, click **vsup**, change **3.3** to **2.5** in Value field and click **Change**.

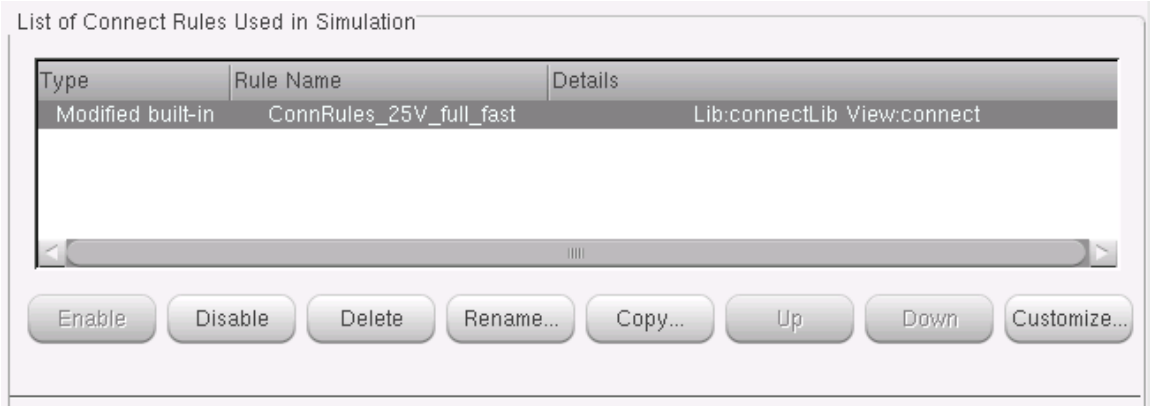
Next highlight both **E2L_2** and **Bidir_2** and change the values of the following parameters:

E2L_2	**vsup=2.5**	**vthi=1.7**	**vtlo=0.8**
Bidir_2	**vsup=2.5**	**vthi=1.7**	**vtlo=0.8**

Click **OK**. In the Information form, which reminds you to add the customized connect rules to the list, click **OK**.

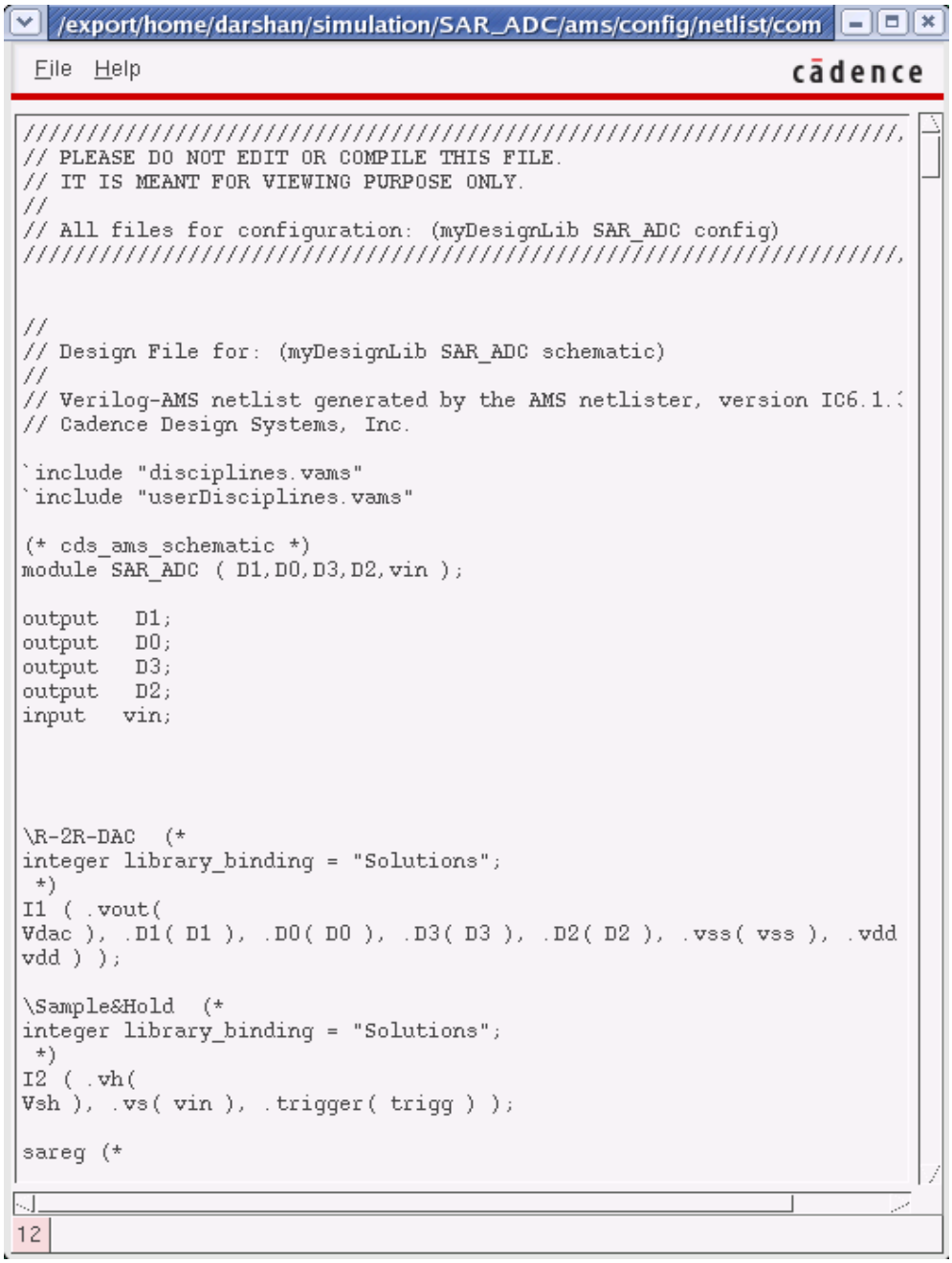


9. In the **Select Connect Rules** form, click **Add** and select the new modified connect rules. Click **Rename** and edit the rule name to **My_ConnRules_25V_full_fast**. Click **OK**.



10. In the ADE window, click **Outputs — To Be Plotted — Select on Schematic** and click **vsin, D0, D1, D2, D3**, **Vsh, Vcomp, clk, trigg and Vdac** in the SAR_ADC Schematic.

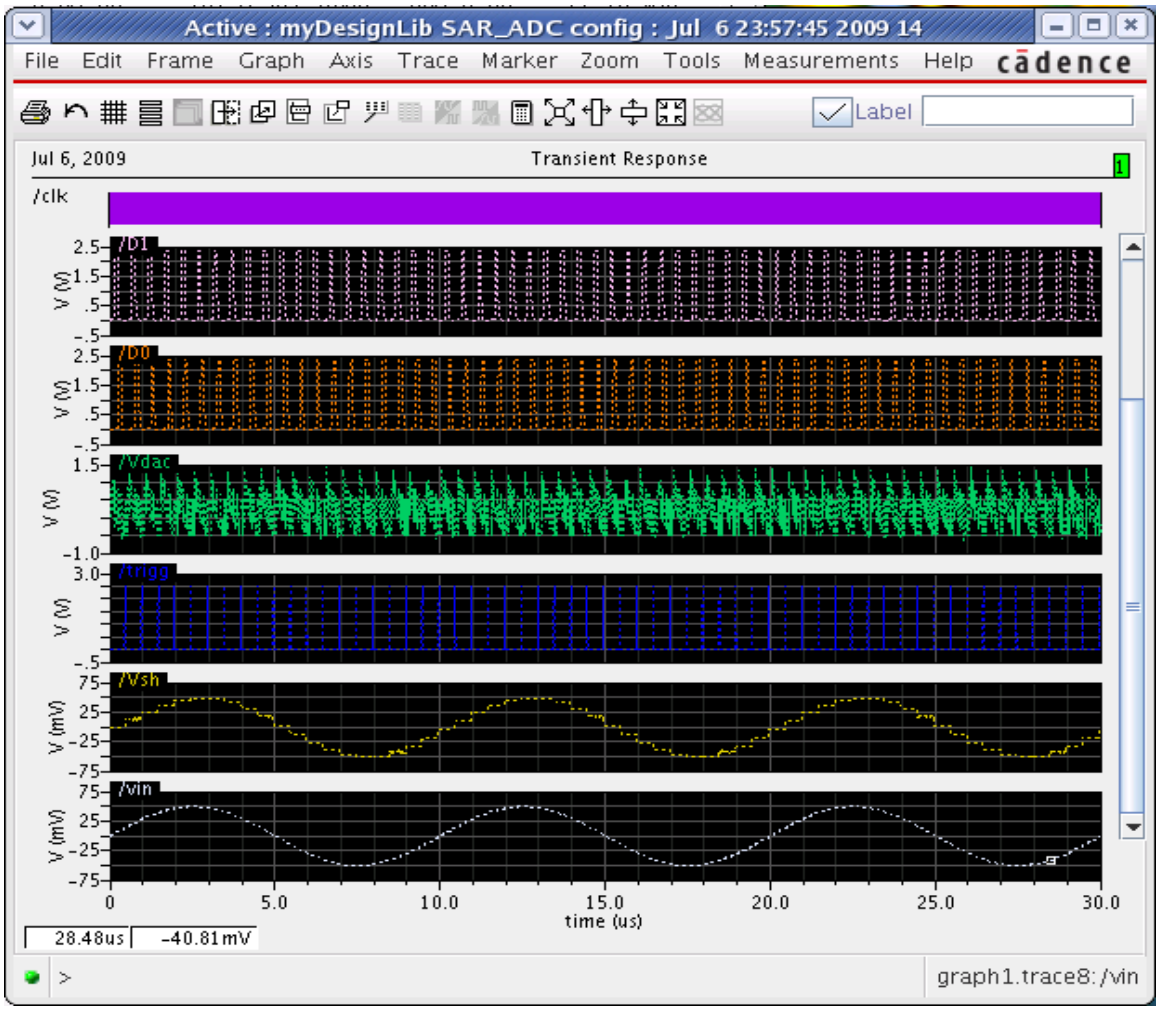
11. In the Schematic window, click **Simulation — Netlist — Create**. After the netlist process is finished, click **Simulation — Netlist — Display** to display the Verilog-AMS format netlist.



12. Click **Session — Save State**. In the Saving State form, change the name in State Save Directory field to artist_states, change the state name to **state_ams** in the Save As field and click **OK**.

13. In the upper right corner of the ADE window, confirm that simulator is ams(Spectre). Click **Simulation — Netlist and Run** Options.

After the simulation finishes running, the VIVA automatically shows the plotted waveforms.



14. Exit virtuoso, execute **File — Exit.**

End of Lab 7