buffer chips slow down the DIMM and are not effective at higher speeds. For this reason, all PC systems use unbuffered DIMMs. The voltage is simple—DIMM designs for PCs are almost universally 3.3v. If you install a 5v DIMM in a 3.3v socket, it would be damaged, but fortunately, keying in the socket and on the DIMM prevents that.

Modern PC systems use only unbuffered 3.3v DIMMs. Apple and other non-PC systems can use the buffered 5v versions. Fortunately, the key notches along the connector edge of a DIMM are spaced differently for buffered/unbuffered or 3.3v/5v DIMMs, as shown in Figure 6.8. This prevents inserting a DIMM of the wrong type into a given socket.

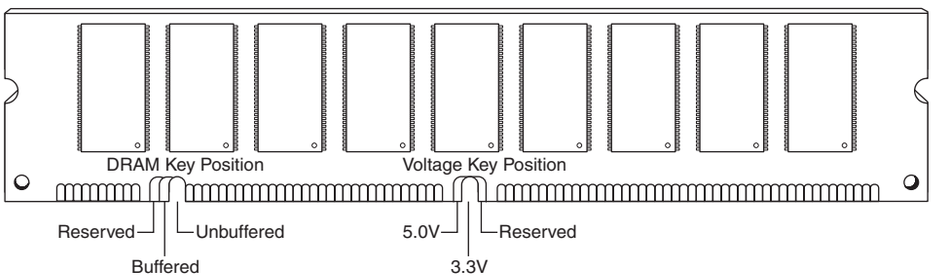


**Figure 6.8** 168-pin DRAM DIMM notch key definitions.

## DDR DIMM Pinouts

Table 6.14 shows the pinout configuration of a 184-pin DDR SDRAM DIMM. Note again that the pins on each side of the DIMM are different.

**Table 6.14 184-Pin DDR DIMM Pinouts**

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|
| 1 | Reference +1.25v | 47 | Data Strobe 8 | 93 | GND | 139 | GND |
| 2 | Data Bit 0 | 48 | Address Bit 0 | 94 | Data Bit 4 | 140 | Data Strobe 17 |
| 3 | GND | 49 | Parity Bit 2 | 95 | Data Bit 5 | 141 | Address Bit 10 |
| 4 | Data Bit 1 | 50 | GND | 96 | I/O +2.5v | 142 | Parity Bit 6 |
| 5 | Data Strobe 0 | 51 | Parity Bit 3 | 97 | Data Strobe 9 | 143 | I/O +2.5v |
| 6 | Data Bit 2 | 52 | Bank Address 1 | 98 | Data Bit 6 | 144 | Parity Bit 7 |
| 7 | +2.5v | 53 | Data Bit 32 | 99 | Data Bit 7 | 145 | GND |
| 8 | Data Bit 3 | 54 | I/O +2.5v | 100 | GND | 146 | Data Bit 36 |
| 9 | NC | 55 | Data Bit 33 | 101 | NC | 147 | Data Bit 37 |
| 10 | NC | 56 | Data Strobe 4 | 102 | NC | 148 | +2.5v |
| 11 | GND | 57 | Data Bit 34 | 103 | AddressBit 13 | 149 | Data Strobe 13 |
| 12 | Data Bit 8 | 58 | GND | 104 | I/O +2.5v | 150 | Data Bit 38 |
| 13 | Data Bit 9 | 59 | Bank Address 0 | 105 | Data Bit 12 | 151 | Data Bit 39 |
| 14 | Data Strobe 1 | 60 | Data Bit 35 | 106 | Data Bit 13 | 152 | GND |
| 15 | I/O +2.5v | 61 | Data Bit 40 | 107 | Data Strobe 10 | 153 | Data Bit 44 |
| 16 | Clock 1 | 62 | I/O +2.5v | 108 | +2.5v | 154 | RAS# |

**Table 6.14 Continued**

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|
| 17 | Clock 1# | 63 | WE# | 109 | Data Bit 14 | 155 | Data Bit 45 |
| 18 | GND | 64 | Data Bit 41 | 110 | Data Bit 15 | 156 | I/O +2.5v |
| 19 | Data Bit 10 | 65 | CAS# | 111 | Clock Enable 1 | 157 | S0# |
| 20 | Data Bit 11 | 66 | GND | 112 | I/O +2.5v | 158 | S1# |
| 21 | Clock Enable 0 | 67 | Data Strobe 5 | 113 | Bank Address 2 | 159 | Data Strobe 14 |
| 22 | I/O +2.5v | 68 | Data Bit 42 | 114 | Data Bit 20 | 160 | GND |
| 23 | Data Bit 16 | 69 | Data Bit 43 | 115 | Address Bit 12 | 161 | Data Bit 46 |
| 24 | Data Bit 17 | 70 | +2.5v | 116 | GND | 162 | Data Bit 47 |
| 25 | Data Strobe 2 | 71 | S2# | 117 | Data Bit 21 | 163 | S3# |
| 26 | GND | 72 | Data Bit 48 | 118 | Address Bit 11 | 164 | I/O +2.5v |
| 27 | Address Bit 9 | 73 | Data Bit 49 | 119 | Data Strobe 11 | 165 | Data Bit 52 |
| 28 | Data Bit 18 | 74 | GND | 120 | +2.5v | 166 | Data Bit 53 |
| 29 | Address Bit 7 | 75 | Clock 2# | 121 | Data Bit 22 | 167 | FETEN |
| 30 | I/O +2.5v | 76 | Clock 2 | 122 | Address Bit 8 | 168 | +2.5v |
| 31 | Data Bit 19 | 77 | I/O +2.5v | 123 | Data Bit 23 | 169 | Data Strobe 15 |
| 32 | Address Bit 5 | 78 | Data Strobe 6 | 124 | GND | 170 | Data Bit 54 |
| 33 | Data Bit 24 | 79 | Data Bit 50 | 125 | Address Bit 6 | 171 | Data Bit 55 |
| 34 | GND | 80 | Data Bit 51 | 126 | Data Bit 28 | 172 | I/O +2.5v |
| 35 | Data Bit 25 | 81 | GND | 127 | Data Bit 29 | 173 | NC |
| 36 | Data Strobe 3 | 82 | +2.5vID | 128 | I/O +2.5v | 174 | Data Bit 60 |
| 37 | Address Bit 4 | 83 | Data Bit 56 | 129 | Data Strobe 12 | 175 | Data Bit 61 |
| 38 | +2.5v | 84 | Data Bit 57 | 130 | Address Bit 3 | 176 | GND |
| 39 | Data Bit 26 | 85 | +2.5v | 131 | Data Bit 30 | 177 | Data Strobe 16 |
| 40 | Data Bit 27 | 86 | Data Strobe 7 | 132 | GND | 178 | Data Bit 62 |
| 41 | Address Bit 2 | 87 | Data Bit 58 | 133 | Data Bit 31 | 179 | Data Bit 63 |
| 42 | GND | 88 | Data Bit 59 | 134 | Parity Bit 4 | 180 | I/O +2.5v |
| 43 | Address Bit 1 | 89 | GND | 135 | Parity Bit 5 | 181 | SPD Address 0 |
| 44 | Parity Bit 0 | 90 | SPD Write Protect | 136 | I/O +2.5v | 182 | SPD Address 1 |
| 45 | Parity Bit 1 | 91 | SPD Data | 137 | Clock 0 | 183 | SPD Address 2 |
| 46 | +2.5v | 92 | SPD Clock | 138 | Clock 0# | 184 | SPD +2.5v |

*Gnd = Ground* *SPD = Serial presence detect*

*NC = No connection*

DDR DIMMs use a single key notch to indicate voltage, as shown in Figure 6.9.

184-pin DDR DIMMs use two notches on each side to enable compatibility with both low- and high-profile latched sockets. Note that the key position is offset with respect to the center of the DIMM to prevent inserting it backward in the socket. The key notch is positioned to the left, centered, or to the right of the area between pins 52 and 53. This is used to indicate the I/O voltage for the DDR DIMM and to prevent installing the wrong type into a socket that might damage the DIMM.