Finite State Machine (FSM) Vending Machine – Timing Diagrams & Verification

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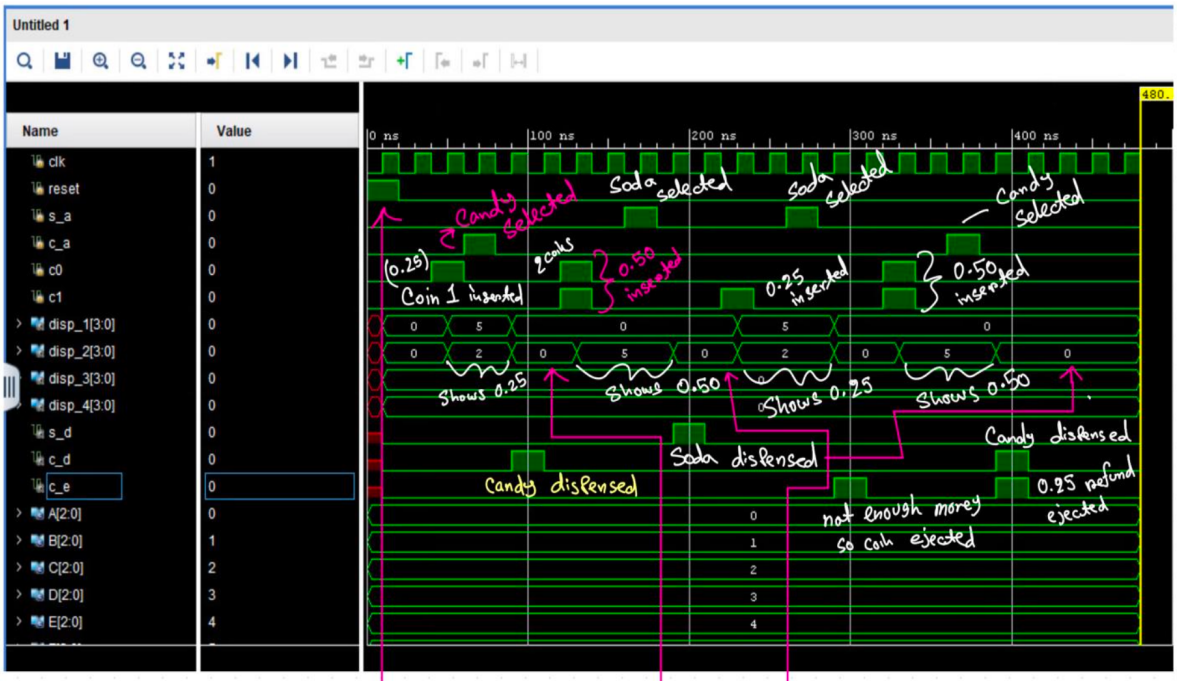
Highlights:

- Timing diagrams generated from **Vivado** behavioral simulation
- Shows correct **state transitions**, **coin accumulation**, and **combo logic**
- Verifies FSM design prior to **FPGA deployment**

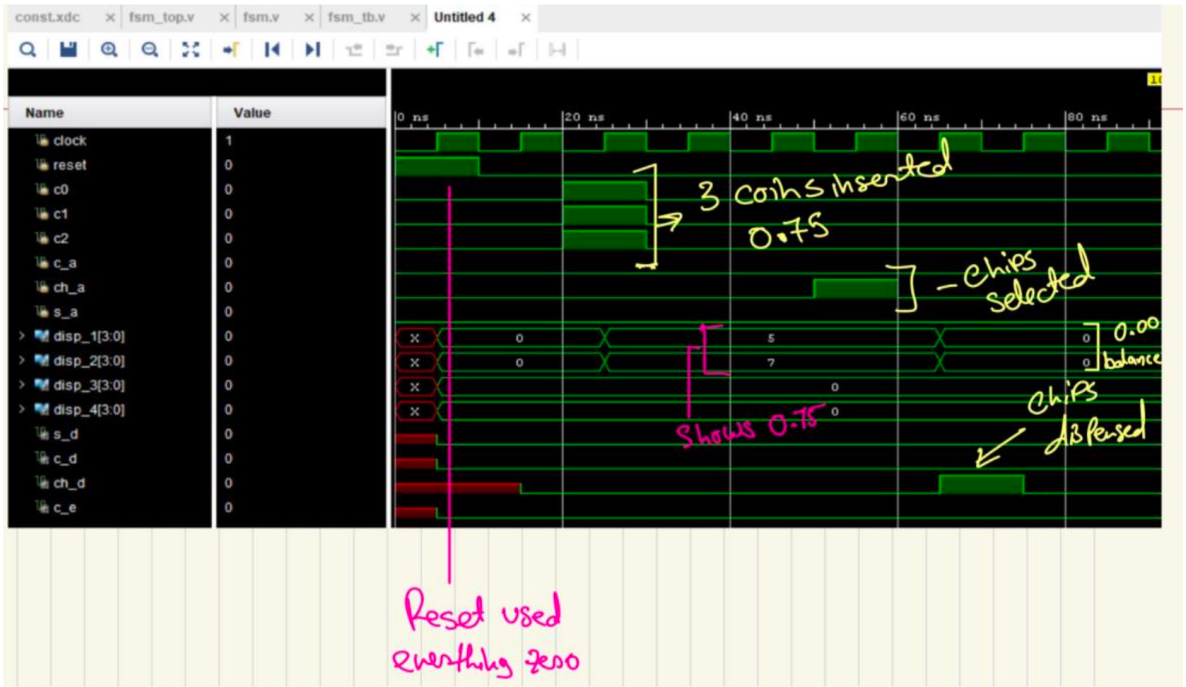
Hardware & Tools

- **Language:** Verilog HDL
- **Simulation: Vivado** Design Suite
- **Hardware: Nexys A7 FPGA** (Artix-7 100T)



Reset button
All inputs & outputs are zero.
And displays 0000

Displays 0000
Because item has been purchased



Reset used
everything zero