Finite State Machine (FSM) Vending Machine — Schematic / Block Diagram

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Board: Digilent Nexys A7 (Artix-7 100T, XC7A100T-1CSG324C)

Tools: Verilog HDL, Vivado Design Suite

Highlights:

• Clean RTL partition: Clock Divider (human-visible timing) → FSM Core → Disp_Hex_Mux (7-seg)

• Clear signal flow: coins/reset → credit accumulate → vend decision → display/dispense

• Credit ladder: $0.25 → $0.50 → $0.75 with combo logic at $0.75

• Explicit IDLE, accumulate, vend/dispense, and return-to-idle paths

• Hardware-verified on FPGA; behavior matched simulation timing

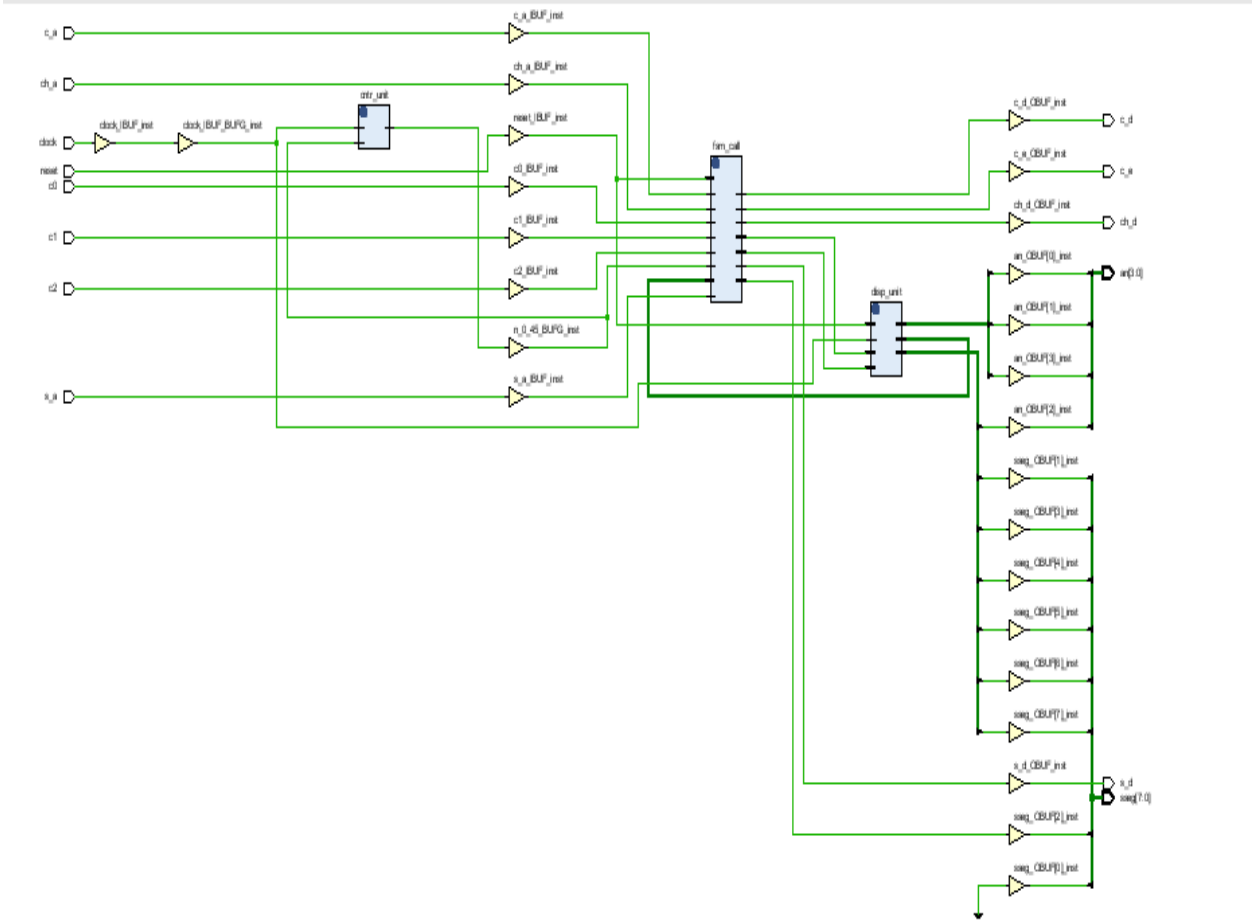
Diagram Notes:

• Moore-style outputs for stable indicators (e.g., display updates, dispense pulse shaping)

• Inputs (c0, c1, c2) treated as coin pulses; purchase button ch_a sampled on clock

• Reset returns system to a safe IDLE state; invalid/overlap inputs handled gracefully

• Display path: FSM nibbles → Disp_Hex_Mux → anodes/segments (time-multiplexed)


c_u
ch_u
clock
reset
c0
c1
c2
s_u
clock_IBUF_inst
clock_IBUF_BUFG_inst
cntr_unit
c_u_IBUF_inst
ch_u_IBUF_inst
reset_IBUF_inst
c0_IBUF_inst
c1_IBUF_inst
c2_IBUF_inst
n_0_45_BUFG_inst
s_u_IBUF_inst
fsm_cell
disp_unit
c_d_OBUF_inst
c_d
c_u_OBUF_inst
c_u
ch_d_OBUF_inst
ch_d
an_OBUF[0]_inst
an[3:0]
an_OBUF[1]_inst
an_OBUF[3]_inst
an_OBUF[2]_inst
seg_OBUF[1]_inst
seg_OBUF[3]_inst
seg_OBUF[4]_inst
seg_OBUF[5]_inst
seg_OBUF[6]_inst
seg_OBUF[7]_inst
s_d_OBUF_inst
s_d
seg[7:0]
seg_OBUF[2]_inst
seg_OBUF[0]_inst