

# EE 4341 Homework 3

Alex Biedny

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**Problem 1.**

- (a)  $\text{SYSCLK} = 10\text{MHz} * (1/2) * 16 * (1/4) = 20\text{MHz}$   $\text{PBCLK} = 20\text{MHz}$
- (b)  $\text{SYSCLK} = 8\text{MHz} * (1/2) * 16 * (1/2) = 32\text{MHz}$   $\text{PBCLK} = 16\text{MHz}$
- (c)  $\text{SYSCLK} = 10\text{MHz}$   $\text{PBCLK} = 10\text{MHz}$

**Problem 2.**

- (a) The flow of the function depends on a global buffer `U2STAbits.UTXBF`. It is possible for an interrupt to hit right after the `while(U2STAbits.UTXBF)` line passes, and the interrupt may change the value of `U2STAbits.UTXBF`.
- (b) The middle two lines of the function are critical, as they contain the check if the transmit buffer is full, and then the loading of the transmit buffer which can only occur after this check. If interrupts were disabled for the critical section then it would guarantee that the buffer full check is accurate when the buffer is loaded.
- (c) `uint16_t SEMAPHORE1 = 1, SEMAPHORE2 = 0;`

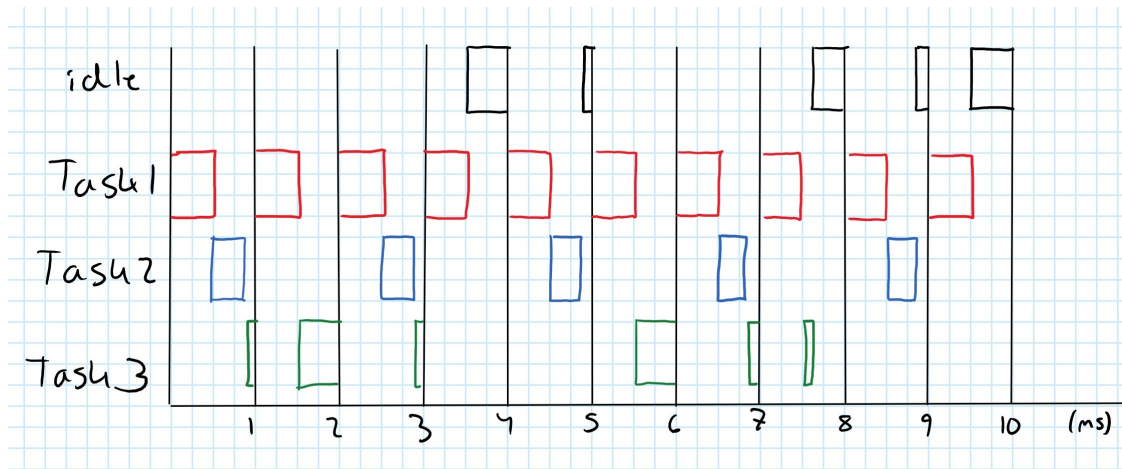
```
//Thread 1
wait(SEMAPHORE2);
put_out(data);
signal(SEMAPHORE1);
```

```
//Thread 2
wait(SEMAPHORE1);
put_out(data);
signal(SEMAPHORE2);
```

- (d) `uint16_t SEMAPHORE1 = 1, SEMAPHORE2 = 0;`

**Problem 3.**

- (a) 0.84



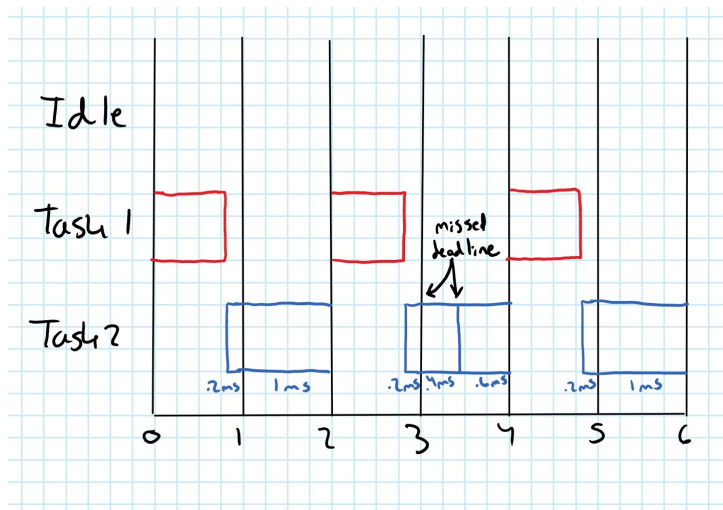
(b)

(c) Task 1 has no latency, task 2 has 0.5ms max, and task 3 has 2.9ms max. No deadlines are missed.

(d) Around 0.72ms.

### Problem 4.

(a) 1.8ms



(b)

There are 5 context switches. The deadline for task 2 is missed once every hyperperiod.

(c) 1.4ms

