EE 4341 Homework 1

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Problem 1.

(a) With no bypassing, it will take 9 instruction cycles to completely execute both instructions. This is because the value of $t2$ will not be available until after the first instruction finishes the W stage, meaning the second isntruction cannot start executing until the first instruction is in the W stage.

(b) With bypassing, it will take 6 instruction cycles to completely execute both instructions, becuase the value of $t2$ will be ready right after the E stage of the first instruction.

Problem 2.

(a) Memory region: KSEG1
Physical addr of instruction: 0x00000028
Type: Boot flash
Registers: sp = r29

(b) Memory region: KSEG0
Physical addr of instruction: 0x00000108
Type: Program flash
Registers: sp = r29, t1 = r9

(c) Memory region: KSEG1
Physical addr of instruction: 0x000001a0
Type: Boot flash
Registers: t0 = r8

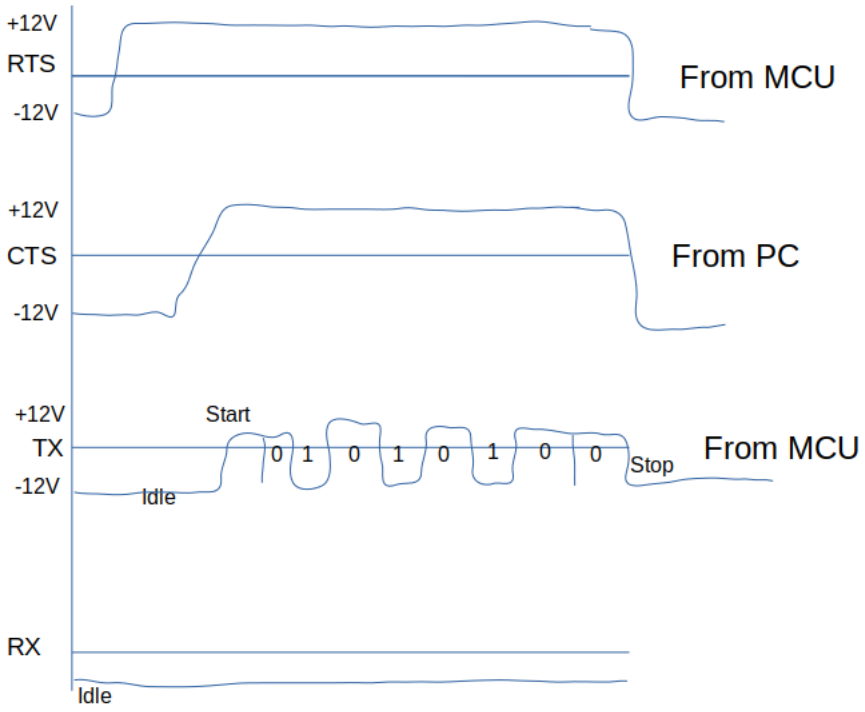
Problem 3.

(a)
```
unsigned int MemVal(unsigned int address) {
  unsigned int *ptr = (unsigned int *) address;
  return *ptr;
}
```

(b) No, it will cause an unaligned address exception.

Problem 4.

(a) RX, pin 2: Serial line that a signal will be recieved on.
TX, pin 3: Serial line that signals are sent on.
RTS, pin 7: Line indicating data is ready to send.
CTS, pin 8: Line indicating data is clear to send.



(b)

(c) About 1/960 seconds for all 10 bits (8 bit char plus start, stop)