Problem 1

P&H

5.2.1, 5.2.2 (given as word addresses but the cache is a byte address)
5.3.1, 5.3.2

Problem 2

Fill in the following table (assume 1 valid bit and 1 dirty bit):

Address Bits	Cache Size	Block Size	Associativity	Tag Bits	Index Bits	Offset Bits	Bits Per Row
16	4KB	4B	1				
16	16KB	8B	2				
16	32KB	8B	4				
16			2		8	2	
32	8KB	8B	1024				
32	32KB	16B	2				
32	64KB			16	12	4	146
32	512KB		4		10		
64	512KB		2			8	
64				26		8	
64	2MB						1069

Address Bits	Cache Size	Block Size	Associativity	Tag Bits	Index Bits	Offset Bits	Bits Per Row
64		128B	1		14		
64	4MB		2		16		