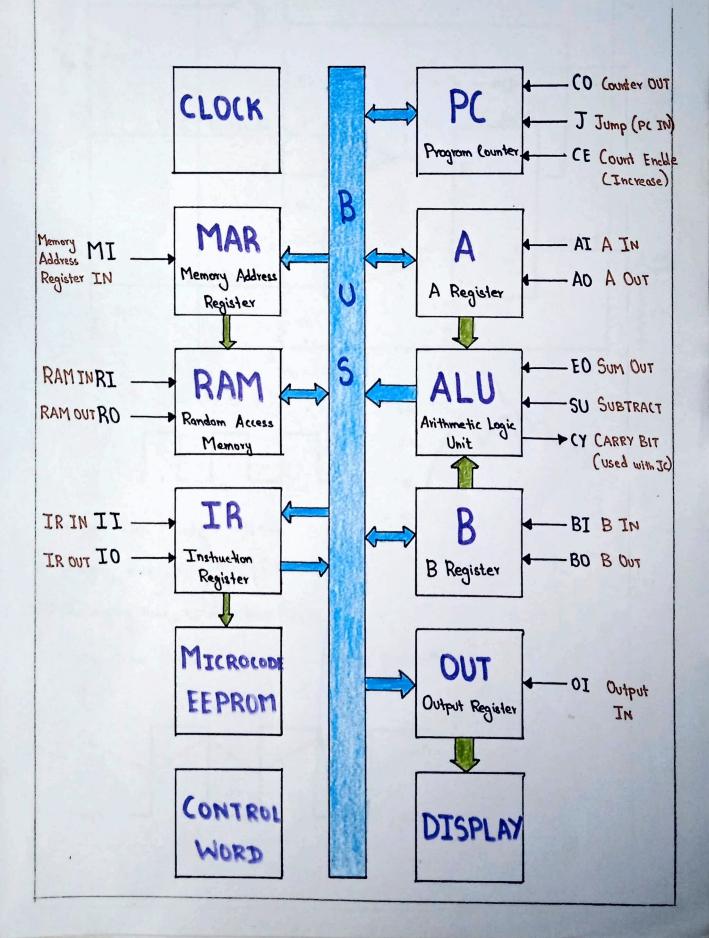
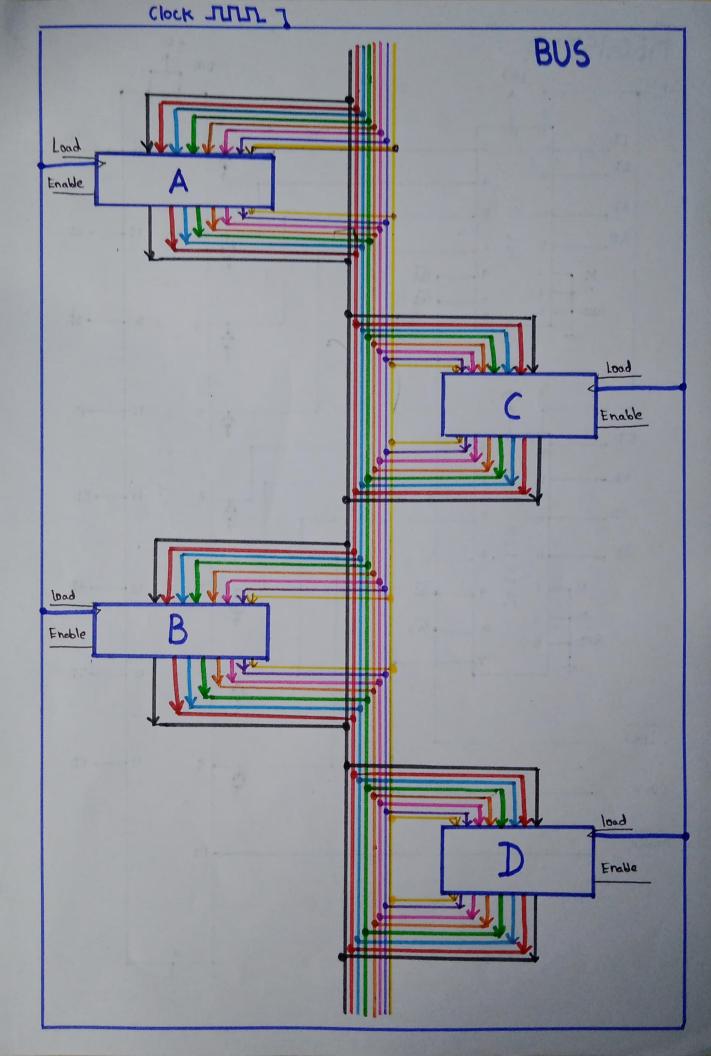
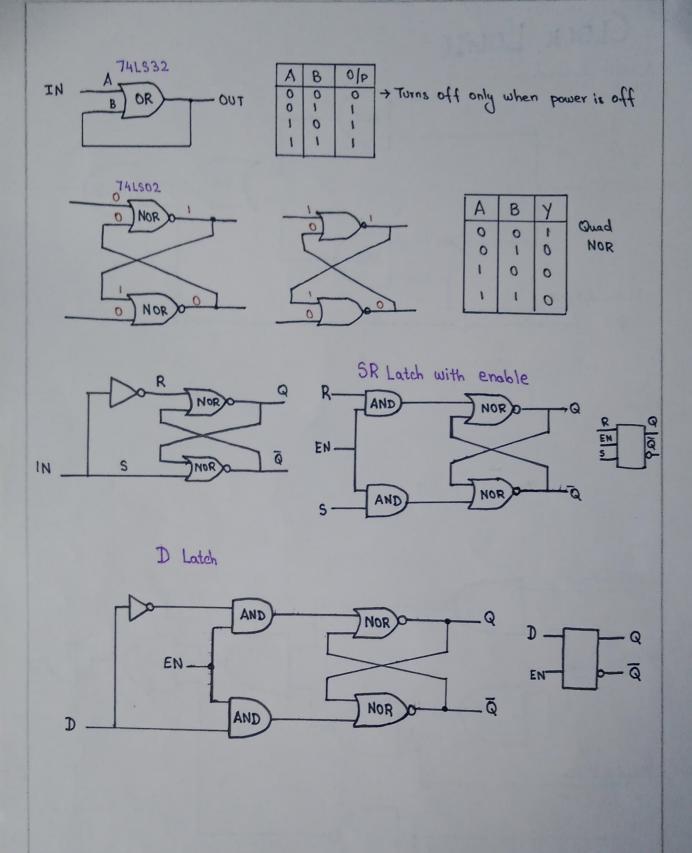
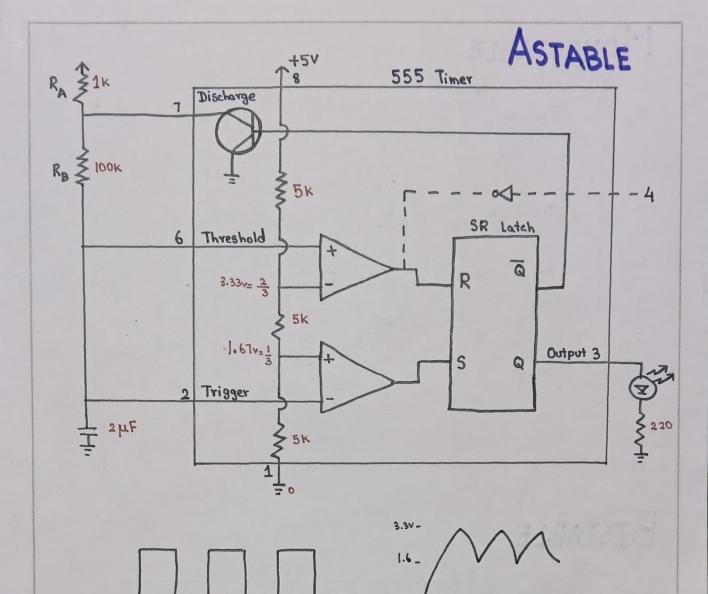
## 8 BIT CPU CONTROL SIGNAL







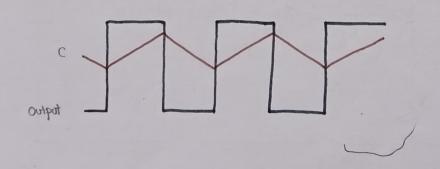


To find Time Period, T = t1+t2

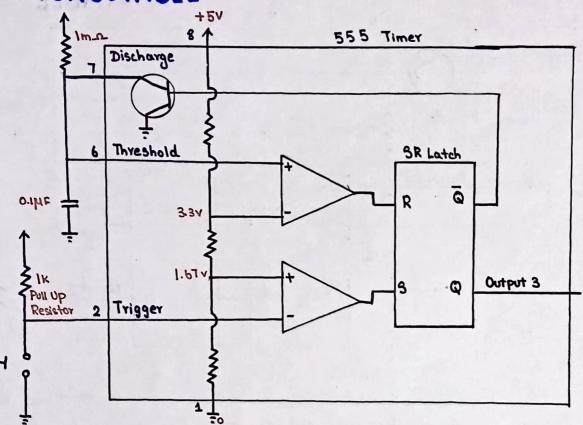
Charging time, t1 = 0.693 (RA+RB) C

discharging time, t2 = 0.693 (RB) C

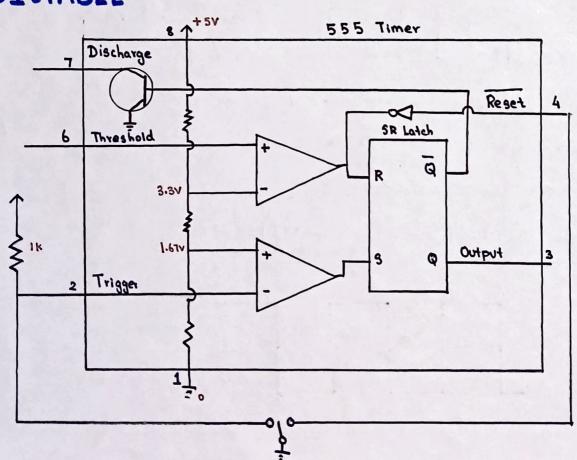
Total Time Period, T = t1 + t2 = 0.693 (RA + 2RB) C.

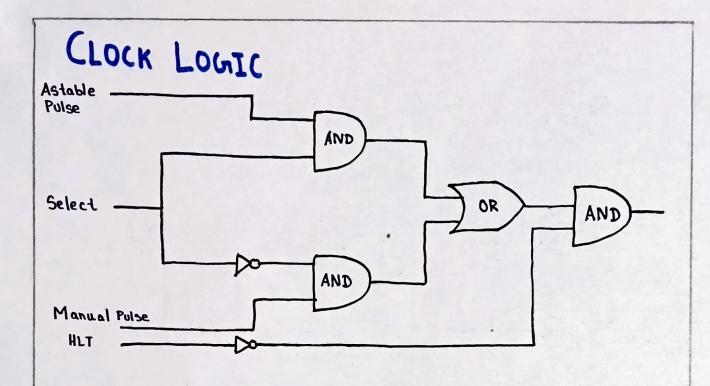


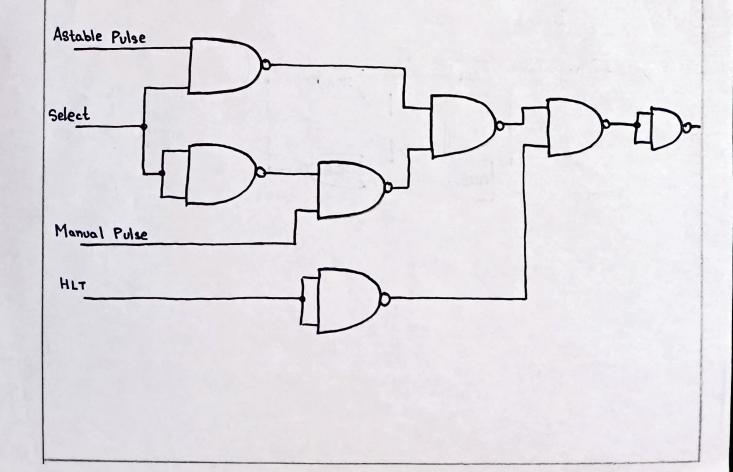
### MONOSTABLE

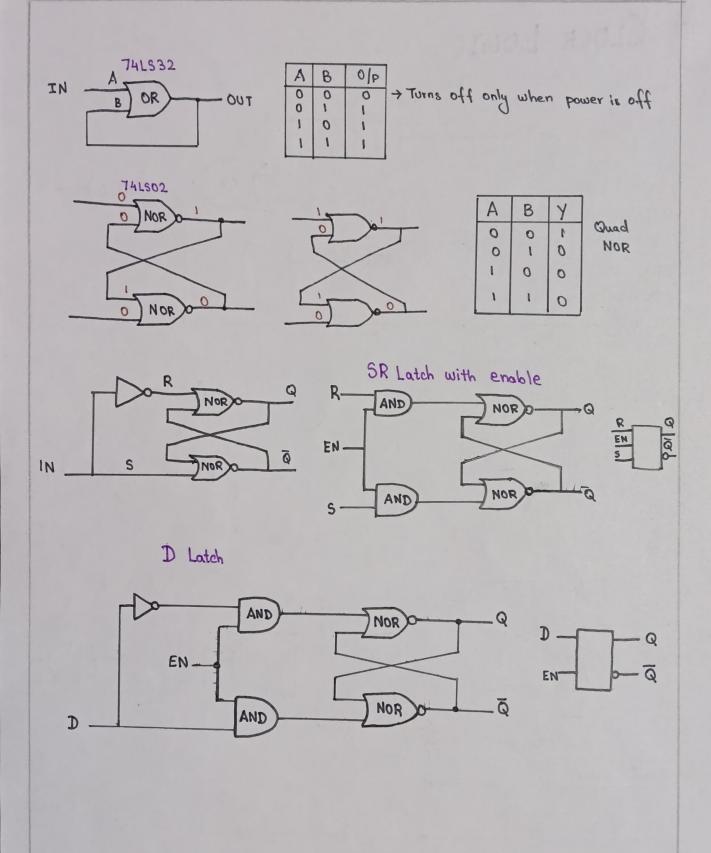


### BISTABLE

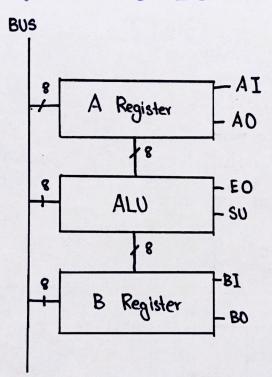




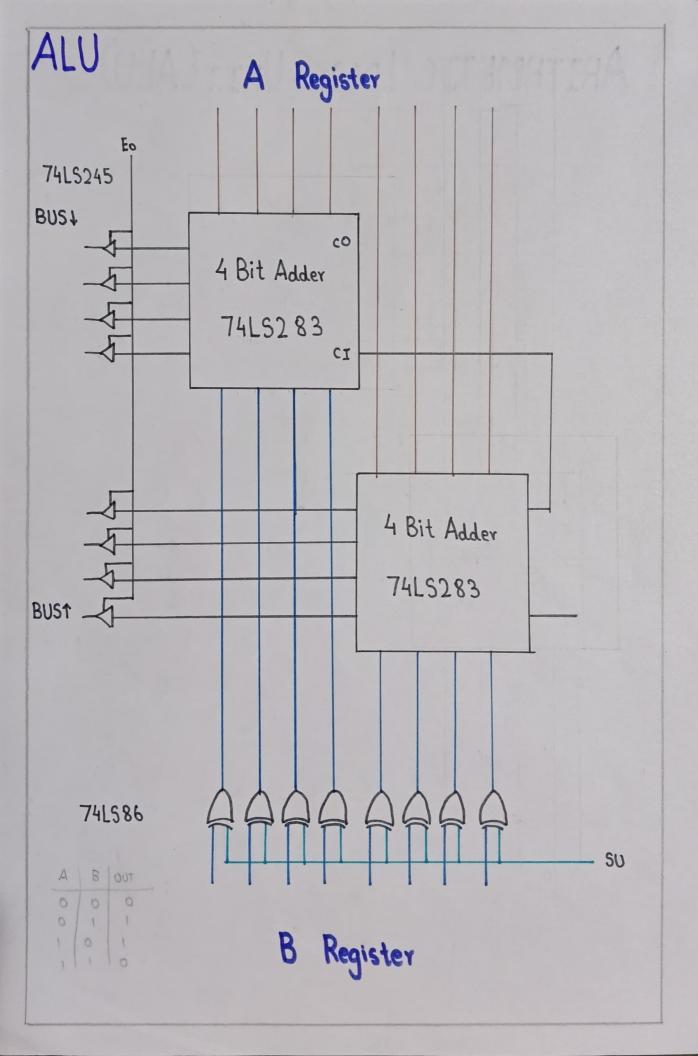


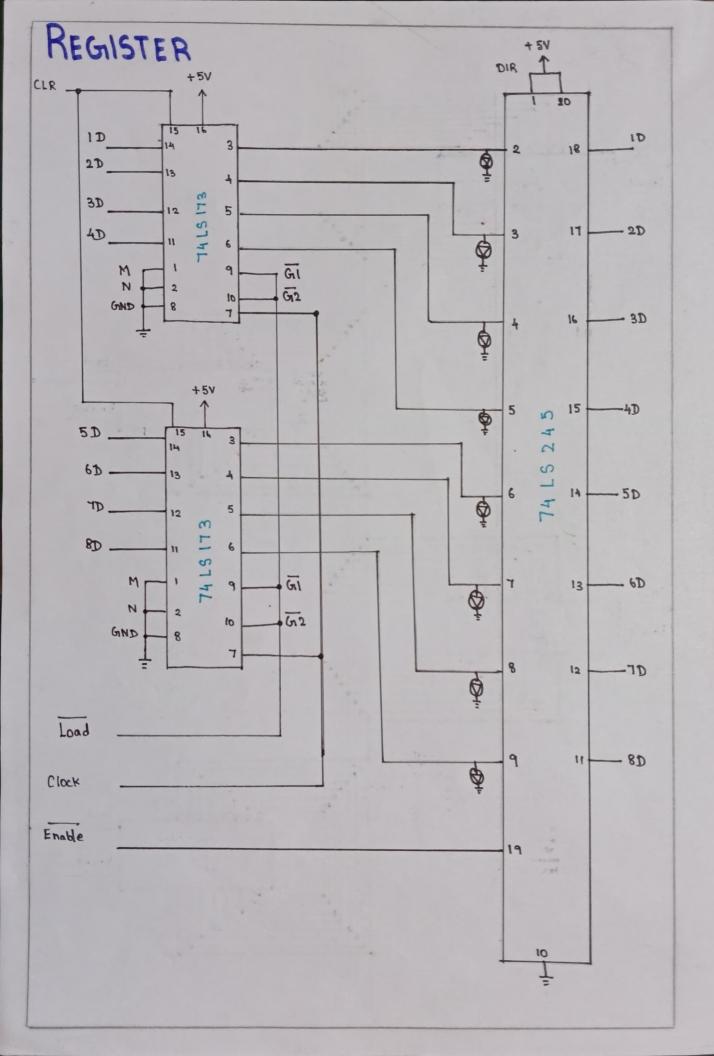


# ARITHMETIC LOGIC UNIT (ALU)



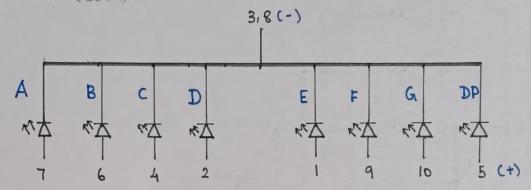
74LS283 4 Bit Binary Adder

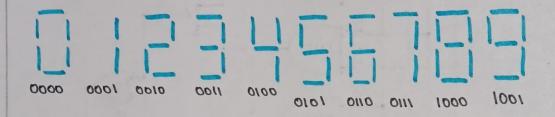


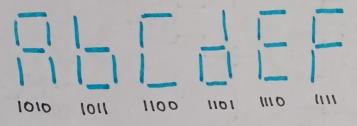


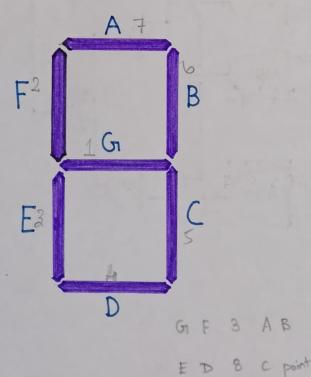
### 7 SEGMENT

Common Cathode (ISIII)

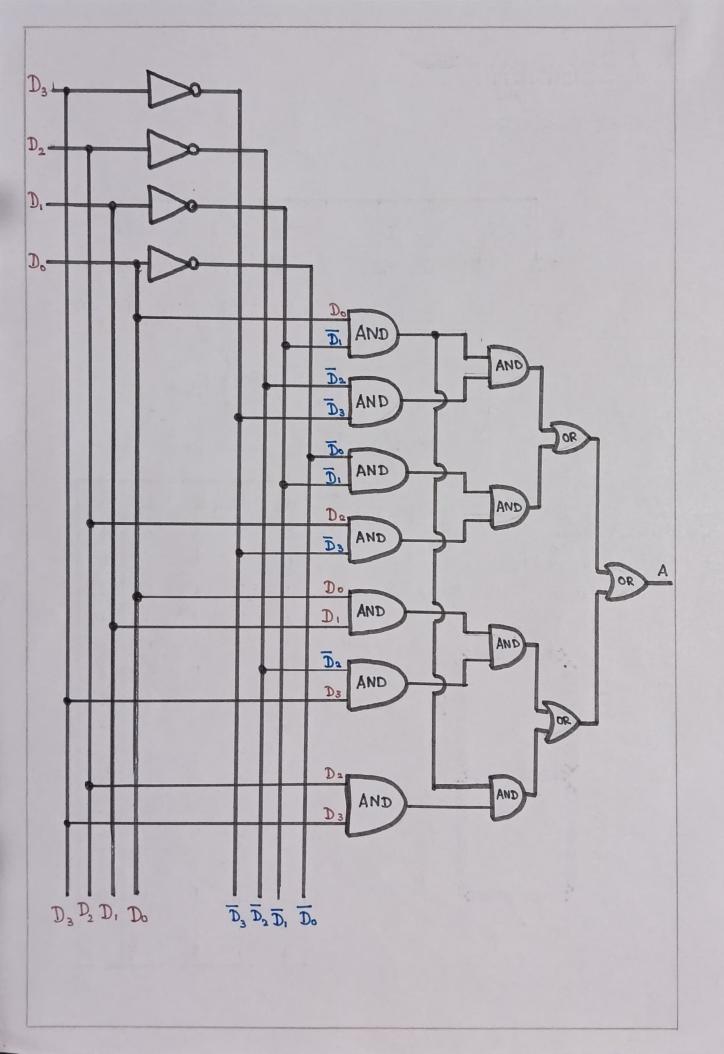








d3	d 2	dı	do	a	
0	0	0	0	1	
0	0	0	1	0	
0	0	1	0	ı	
0	0	1	ı	1	
0	1	0	0	0	
0	1	0	1	ı	
0	1	1	0	1	
0	1	1	1	ı	
1	0	0	0	ı	
1	0	0	1	1	
1	0	1	0	1	
1	0	1	1	0	
1	1	0	0	1	
1	1	0	ı	0	
1	- 1	1	0	1	
1	1	1	1	1	



-							-	-	-	-
d3	d2	d,	do	А	В	С	D	E	F	Gı
0	0	0	0	0	0	0	0	0	0	ı
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	١	0	0	1	0	0	1	1	0	0
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0	1	1	0	0	1	0	0	0	0	0
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1	1	0	0	0	1	1	0	0	0	1
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1	1	ι	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

### SIGN BIT

#### ONES COMPLEMENT