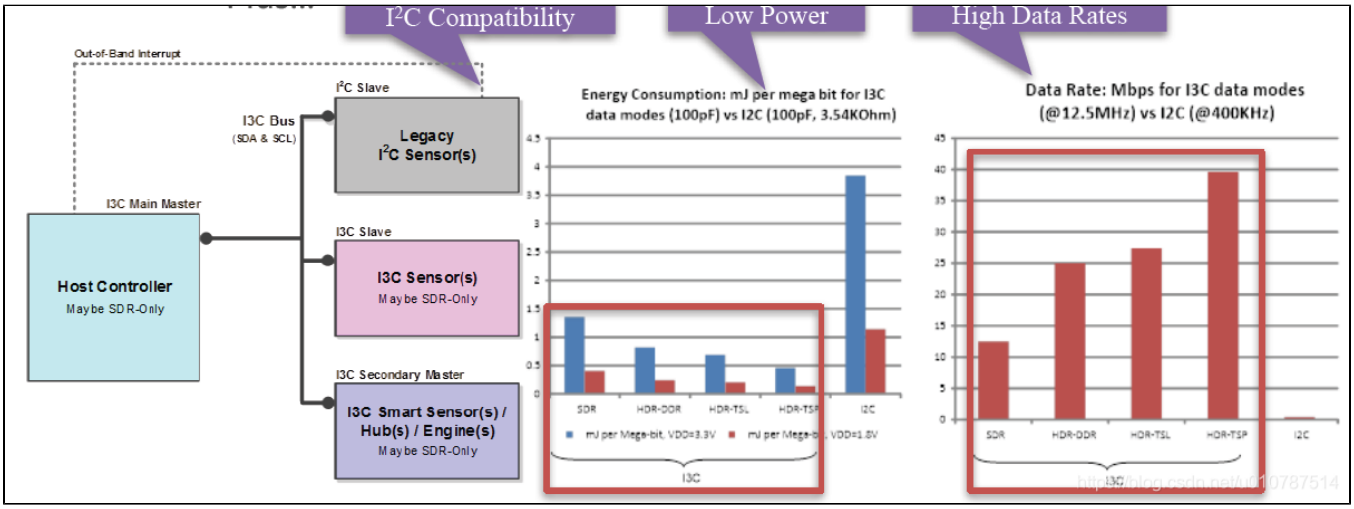
I3C

DDR5 sdieband access is based on the MIPI I3C sideband communication protocal with backward compatibility to I2C. Due to the growth in the number of active components on the DDR5 modules, a serial presence detect hub was intruduced. The SPD hub also contains the programmable read-only memory pertaining to the SPD. The I3C protocol also scales up the bandwidth on the sideband bus. RCD/PMIC /Sensors.



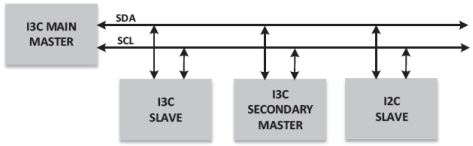
MIPI I3C Fact Sheet	
MIPI I3C Standardized Sensor Interface	
 Two-wire communication interface, clock (SCL) and data (SDA)	
Number of gates	< 2,000
Bandwidth	> 33 Mbps
Features	In-band interrupts In-band command codes Dynamic addressing Multi-master / multi-drop Hot-join support Backward compatible with I²C

Table 1: *MIPI I3C standardized sensor interface at a glance.*