

Chapter : 02
Architectural Details
Assembly Language Programming

An assembly language is a type of programming language that translates high-level languages into machine language. It is necessary bridge between software programs and their underlying hardware platforms. Assembly language relies on language syntax, tables, operations, and directives to convert code into executable machine instructions.

8085 microprocessor Architecture:

- ↳ 8-bit general purpose microprocessor
- ↳ capable of addressing 64K of memory (with 16 address lines).
- ↳ Has 40 pins DIP (Dual In-line Package)
- ↳ Requires +5V power supply
- ↳ Can operate with maximum 3MHz single phase clock and minimum 500 kHz clock.
- ↳ 8085 upward compatible (its instructions and features are available in 8086)
- ↳ It provides 74 instructions with 5 addressing modes.

Pin-diagram of 8085 up.

1 → X ₁	40 → V _{cc} (Power supply +5V)
2 → X ₂	39 → HOLD
3 → RESET OUT	38 → HLD _A
4 → SOD	37 → CLK (OUT)
5 → SID	36 → RESET IN
6 → TRAP	35 → READY
7 → RST 7.5	34 → I _O /M
8 → RST 6.5	33 → S ₁
9 → RST 5.5	32 → RD
10 → INTR	31 → WR
11 → INTA	30 → ALE
12 → AD ₀	29 → S ₀
13 → AD ₁	28 → A ₁₅
14 → AD ₂	27 → A ₁₄
15 → AD ₃	26 → A ₁₃
16 → AD ₄	25 → A ₁₂
17 → AD ₅	24 → A ₁₁
18 → AD ₆	23 → A ₁₀
19 → AD ₇	22 → A ₉
20 → V _{SS} → ground reference.	21 → A ₈

multiplexed
Address Data
Bus

[P₁₂ - P₁₉]

control and
status signal
[P₂₉ - P₃₄]

Address Bus
(P₂₁ - P₂₈)

8085 Pin configuration:

↳ Pins of 8085 are grouped in 6 categories.

1. ADDRESS BUS (P21-P28):

- 16 signal pins
- These lines are split into 2 segments A15-A8 and A07-A00.
- 8 signal lines, A15-A8 are unidirectional and are used for most significant bits, called higher order address of 16-bit address.

2. Multiplexed Address / Data Bus (P12-P19)

- They are time multiplexed address and data bus.
- The signal lines A07-A00 are bidirectional.
- serve dual purpose:

During execution of instruction cycle, these lines are used as lower address bus.

3. Control and status signals (P29-P34):

- This group includes:

2 control signals : RD and WR.

3 status signals : IO/M¹, SI and SO (to identify the nature of operation) and 1 control signal : ALE (to indicate the beginning of operation).

→ If IO/M¹ = 1, input-output operation is done.

→ If IO/M¹ = 0, memory operation is done.

These signals are combined with RD and WR control signals generate I/O and memory control signals (\overline{IOR} , \overline{IOW} , \overline{MEMR} , \overline{MEMW}).

SI	SO	operation
0	0	HLT (halt, termination)
0	1	Write (memory or I/O)
1	0	Read (memory or I/O)
1	1	(opcode fetch)

4. Power supply and frequency

- V_{cc}: +5V power supply
- V_{ss}: Ground Reference
- X₁, X₂: A crystal RL or RC network.

A frequency is internally divided by 2, so to operate a system at 3 MHz; the crystal should have a frequency of 6 MHz.

CLK (OUT) [P-37]

- used as a system clock for other devices.

5. Externally Initiated Signals, Including Interrupt:

- 8085 has 5 interrupt signals, 2 acknowledgement signals and 3 other signals.

Interrupt signals are:

RST 7.5 (among them the priority order is 7.5, 6.5 and 5.5)
RST 6.5 (Inputs)
RST 5.5

TRAP (highest priority) (Input)

INTR (lowest priority) (Input)

INTA (output) [P-21]

- Interrupt Acknowledgement signal.
- CPU sends this signal after receiving INTR signal.

READY (Input) [P-35]

- used to delay CPU Read or write cycles until a slow responding peripheral is ready to send or receive data.
- when this signal goes low CPU waits and as soon as it goes high it reads the data in bus or writes in it.

HOLD (Input)

- indicates that a peripheral device eg: DMA (Direct Memory Access) controller is requesting the use of address and data buses.

When this signal goes high, microprocessor stops the buses as soon as the current cycle is completed.

CPU regains it when HOLD signal goes low.

HOLD (output)

- This is Hold acknowledgement signal and acknowledges the HOLD request.
- Goes low when HOLD signal is removed and CPU takes over buses.

RESET-IN [P36]

- When the signal on this pin goes low, the Program Counter (PC) is set to zero.
- So CPU is reset.

RESET-OUT [P37]

- It indicates that the microprocessor is being reset.
- This signal can be used to reset other devices.

6. Serial I/O devices [P4 and P5]

- SID (Serial Input Data) to implement SOD (Serial Output Data) are used for serial transmission
- In serial transmission, data are sent over a single line, one bit at a time, e.g. telephone line.

Internal Architecture of 8085 CPU:

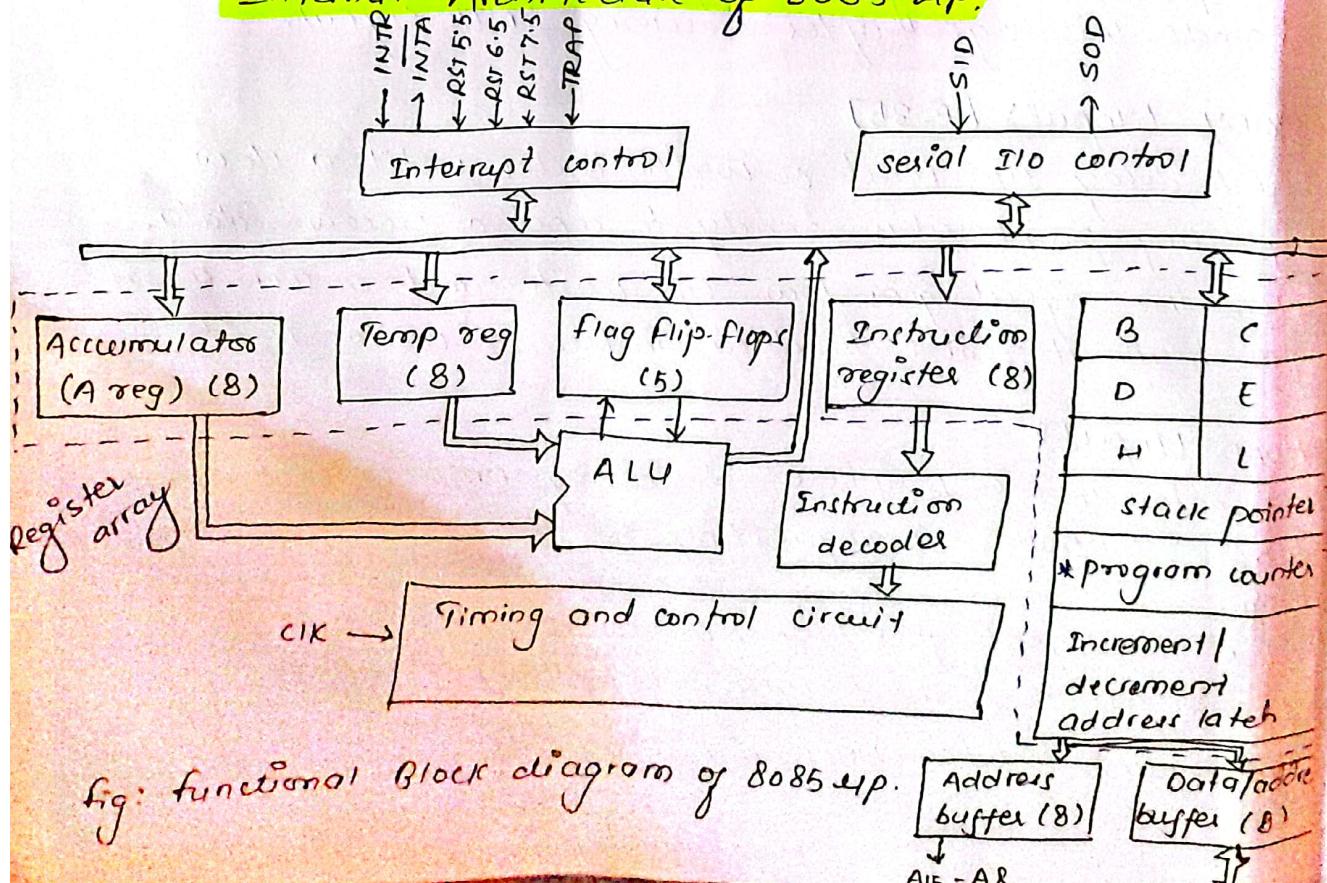


Fig: functional Block diagram of 8085 CPU.

The internal architecture of 8085 CPU consists of:

- i) ALU (Arithmetic and logical unit)
- ii) Register Array
- iii) Timing and control unit (CU)
- iv) Instruction Register (IR) and Decoder.
- v) Interrupt controller
- vi) Serial I/O control

1. Arithmetic and Logic Unit (ALU):

performs the computing functions. It includes:

- i) The Accumulator (A) - 8 bit special purpose register used in arithmetic, logic, load and store operations as well as I/O operations.
- ii) The temporary registers (8 bit register used to hold data temporarily during program execution and is not accessible to the programmer.)
- iii) The arithmetic and logical circuits
- iv) five flag flip-flop registers.

Flag Register:

- It is an 8 bit special purpose register (with 5 bits carrying significant information), that generally reflects the intermediate or final status of the result or conditions of data in the accumulator.

The result of every arithmetic and logical operations are stored in accumulator and the flags (flip-flops) are set or reset according to the result of the operation.

Thus helps in taking further decisions.

The bit position reserved for different flags in flag register array are as follows:

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
S	Z	X	A C	X	P	X	C Y

fig: Flag Register Array (where, X = don't care conditions)

a) S-sign flag: (for -ve no, $S=1$ and for +ve no $S=0$)

→ used for indicating the sign of the data in the accumulator
→ for signed numbers, if D₇ bit is 1, the number is viewed as negative number and if it is 0, the number is considered positive.

→ Thus after the execution of arithmetic or logic operation, sign flag is set for negative value and reset for positive value.

→ In arithmetic operations with signed numbers, bit D₇ is reserved for indicating the sign, and remaining 7 bits are used to indicate the magnitude of a number.

b) Z-zero flag (if result = 0, Z = 1, if result ≠ 0, Z = 0)

→ This flag is set if the result of the ALU operations is 0 and reset if the result is non-zero.
→ This flag is modified by the results in the accumulator as well as in other registers.

for eg:

$$\begin{array}{r} 10110011 \\ + 01001101 \\ \hline 10000000 \end{array}$$

Here, Z = 1 as the result of the operation (addition) is 00H.

→ zero flag is also set if data in register becomes 00H after increment or decrement operation.

c) AC-Auxiliary carry flag (AC = 1 if carry occurs from D₃ to D₄ during addition)

→ This flag is set whenever a carry occurs from lower nibble to upper nibble i.e. when a carry is generated from bit digit D₃ and passed onto digit D₄.

→ used for BCD operation.

⇒ P. parity flag ($P=1$ for even parity and $P=0$ for odd)
Parity is defined as the number of 1's in the data in accumulate after arithmetic and logical operations. If the result has even number of 1's, this flag is set and reset if it had odd number of 1's.

so. parity flag is set for even parity and reset for odd parity.

e.g. for data byte, 0000 0011, $P=1$, even no. of 1's
although magnitude of no. is odd.

⇒ C-carry flag ($C=1$ for overflow during addition and Borrow during subtraction)

- In an arithmetic operations such as addition and substr. action involving two 8 bit numbers, there is a situation when an add result is overflowing from highest order bit or a borrow may be required in subtraction.
- In both cases, the carry flag is set, otherwise it is reset.

$$\begin{array}{r} 1011\ 0101 \\ + 0110\ 1100 \\ \hline 10010\ 0001 \end{array}$$

Borrow: $\frac{1100\ 1100}{11010001}$

2. Register Array

- 8085 has 8 and 16 bit registers.
- 8 bit registers are B, C, D, E, H, L, Accumulator and Flag.
- There are two 16 bit registers.
 - is Program Counter (PC)
 - its Stack Pointer (SP) and.
- 8 bit general purpose registers can be used as 8-bit or 16-bit register pair.
- Registers pair HL may hold data pointer and is used in register indirect addressing mode.

Eg: MOV M, A (copies content of A to the memory contained by HL pair).

General purpose Registers (GPRs) are Accessible to the programmer.

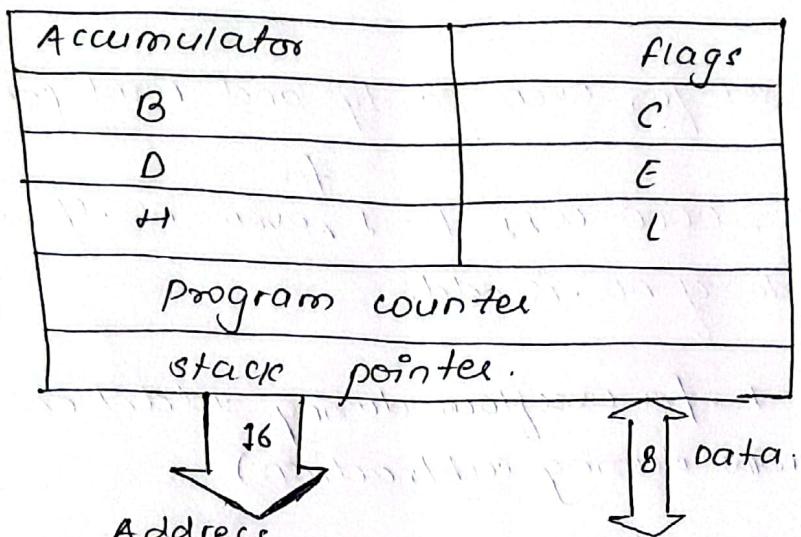


fig: Register array in 8085 up.

Temporary Registers W and Z:

- They hold 8-bit data during the execution of some instructions.
- They are used internally and are not available to the programmer.

Temporary Registers (near ALU):

- It is an 8-bit register and is used to hold data for brief time period during arithmetic logic operations.
- Not available to programmer.

16-bit Registers:

is Program Counter:

- Deals with sequencing and execution of instructions.
- contains 16 bit address of the next instruction to be executed.
- Acts as a pointer to the next instruction to be executed.
- It is operated by the processor and points instruction after the processor has fetched the previous one.

ii) stack pointer:

Stack is the area of Read/Write (RAM) memory used to hold data that will be retrieved soon.

The beginning of stack is defined by loading a 16 bit address in the stack pointer (SP).

The stack is usually accessed in FILO/LIFO basis.

Stack writing instructions fill the memory positions in progressively decreasing order.

Instructions for stack access: PUSH, POP

During Push operation, higher order register content is pushed first.

Eg: PUSH B, then B is pushed and then C.

3. Timing and Control unit:

This unit synchronizes all the bus operations with the clock and generates the control signals necessary for communication between the microprocessor and peripherals.

Eg: RD and WR are control signals indicating the availability of data on the data bus.

4. Instruction Register and Decoder:

When instruction is fetched from memory, it is loaded in the Instruction Register (IR). Then the decoder decodes the instruction and establishes the sequence of events to follow.

The instruction register is not programmable and cannot be accessed through any instruction.

5. Interrupt Control:

8085 has 5 interrupt signals: TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR.

INTA is Interrupt Acknowledgement signal.

Valid interrupt may occur for at least 160 ns.

6. Serial I/O control:

- ↳ The two 8085 pins : SID (serial Input Data) and SOO (serial output data) are specially designed for software controlled serial I/O.
- ↳ Data transfer is controlled through two instructions : SIM and RIM.
- ↳ These instructions are used for interrupt and serial I/O.
- ↳ SIM = Set Interrupt MASK [used for serial output data]
- ↳ RIM = Read Interrupt Mask. [used for serial input data]
- ↳ Bit D7 of RIM and SIM is separated for SID and SOO line respectively.

#. 8085 Bus configuration:

The 8085 microprocessor performs its functions, using three sets of communication lines, called buses.

- is The address Bus
- is The data Bus
- is The control Bus.

is Address Bus:

- It is a group of 16 lines generally identified as A0 to A15.
- The address bus is unidirectional, ie. bit flows in one direction from CPU to peripheral devices.
- Thus, MPU uses address bus to identify a peripheral or memory location.
- In a computer system, each peripheral or memory location is identified by a binary number, called an address, and the address bus is used to carry a 16-bit address.
- 16 address lines can address upto $2^{16} = 65,536$ memory locations or its memory addressing capability is $2^{16} = 64K$.

(ii) Data Bus:

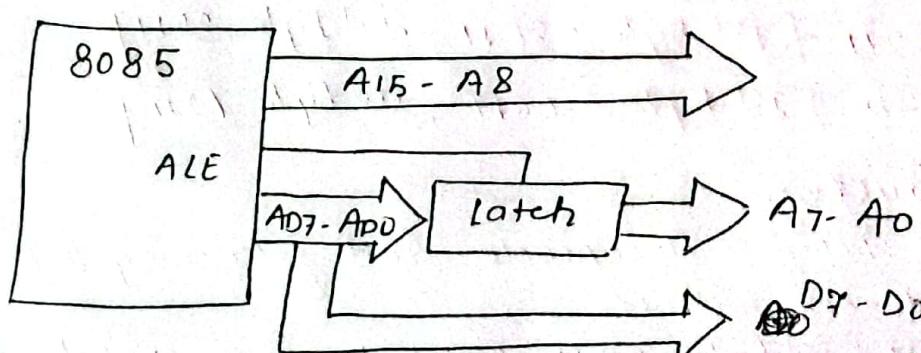
- It is a group of 8 lines used for data flow.
- These lines are bidirectional i.e. data flow in both directions between the MPU and memory and peripheral devices.
- MPU uses data bus to transfer information.
- The eight data lines enable the MPU to manipulate 8-bit data ranging from 00 to FF. ($2^8 = 256$)
- The largest number that can appear on data bus is $(1111\ 1111)_0 = (FF)_H = (255)_{10}$

(iii) Control Bus:

- It is composed of various signal lines that carry synchronization signals.
- MPU uses such lines to provide timing signals.
- MPU generates specific control signals for every operation (such as memory or I/O Read or Write) it performs.

Demultiplexing AD₇-AD₀ in 8085 microprocessor:

- AD₇-AD₀ lines in 8085 MP serve a dual purpose i.e. A₇-A₀ as address bits and D₇-D₀ as data bits.
- So they need to be demultiplexed to get all the information.
- The higher order bits of the address remain on the bus for 3 clock periods, but lower order bits remain only for 1 clock period and they would be lost if they are not saved externally.
- So to make them available for entire 3 clock period, the external latch is used and ALE signal is used to enable this latch.



When ALE = 1, the address can be latched and when ALE = 0, the address is saved.