# Lab 5: Binary Arithmetic

A. Objectives

- Understand the concept of binary addition and subtraction.
- Learn about half and full binary adders.
- Perform binary addition and subtraction using IC7483.
- Understand the concept of BCD addition and implement a BCD adder using IC7483

B. Theory

Digital computers perform a variety of information-processing tasks. Among the functions encountered are the various arithmetic operations. The most basic arithmetic operation is the addition of two binary digits. This simple addition consists of four possible elementary operations: $0 + 0 = 0$, $0 + 1 = 1$, $1 + 0 = 1$, and $1 + 1 = 10$. The first three operations produce a sum of one digit, but when both augend and addend bits are equal to 1, the binary sum consists of two digits. The higher significant bit of this result is called a **carry**. When the augend and addend numbers contain more significant digits, the carry obtained from the addition of two bits is added to the next higher order pair of significant bits. A combinational circuit that performs the addition of two bits is called a **half adder**. One that performs the addition of three bits (two significant bits and a previous carry) is a **full adder**. The names of the circuits stem from the fact that two half adders can be employed to implement a full adder.

Half Adder

$$S = x \oplus y$$
$$C = xy$$
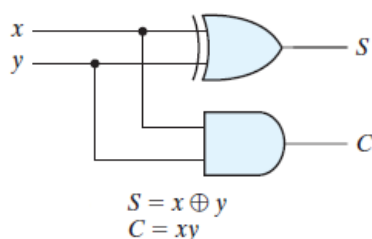
x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0
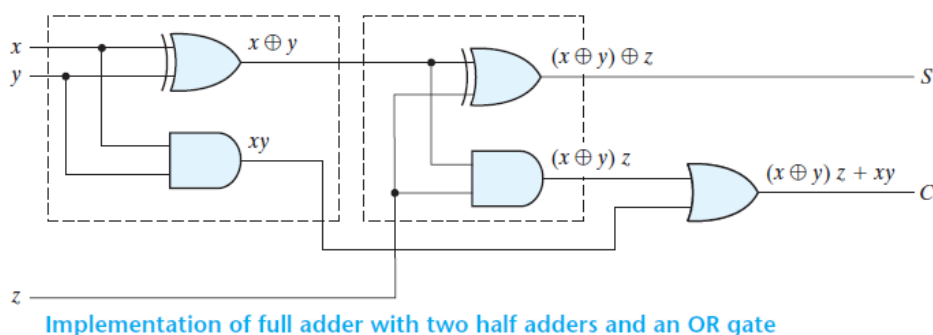
Implementation of full adder with two half adders and an OR gate

Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

New Apparatus:

IC 7483: The 16-pin 7483 IC is a 4-bit full adder. That means, it can take two 4-bit binary numbers ($A_4A_3A_2A_1$ and $B_4B_3B_2B_1$) and calculate the sum ($S_4S_3S_2S_1$). The input carry (if any) is connected to C_0 and the output carry is obtained from C_4. Unlike most other ICs used so far, in the 7483, the 5V V_{CC} needs to be connected to pin 5 and the ground to pin 12.

Two 7483 ICs can be cascaded to form an 8-bit ripple-through-carry adder. The lower 4 bits of each number is used as input for the first 7483 and the output carry is connected to the input carry of the next 7483. The higher 4 bits of each number is used as input for the second 7483. The first IC provides the lower 4 bits of the sum and the second one provides the upper 4 bits.

1	A4		B4	16
2	S3	I	S4	15
3	A3	C	C4	14
4	B3	7	C0	13
5	VCC	4	GND	12
6	S2	8	B1	11
7	B2	3	A1	10
8	A2		S1	9

Figure B1:
Pinout of IC7483

Experiment 1: Binary Adder-Subtractor

C.1 Apparatus

- Trainer board
- 1 x IC 7483 4-bit binary adder
- 1 x IC 7486 quadruple 2-Input XOR gates
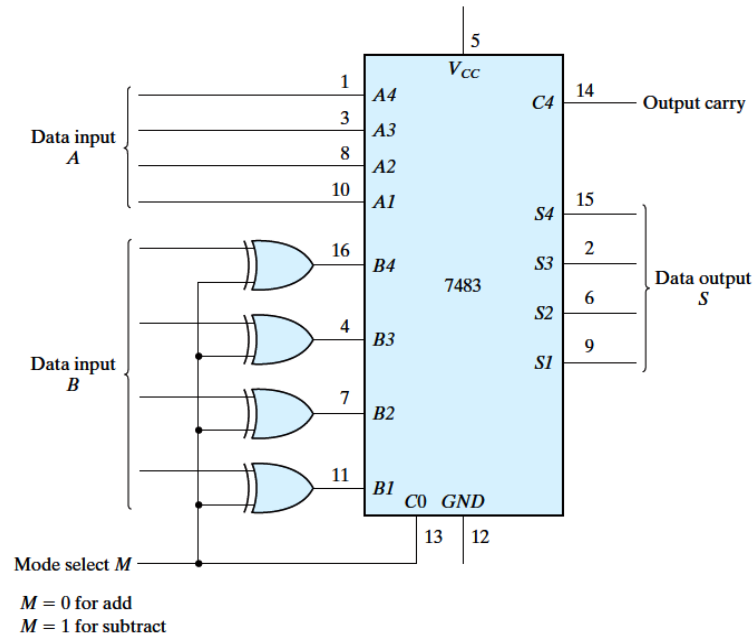
D.1 Procedure

Figure D.1.1 4-bit adder-subtractor

1. Construct the 4-bit adder-subtractor circuit of **Figure D.1.1**.
2. Complete the operations in **Table F.1.1**.
    - i.   For each operation, convert the first operand to binary as A, and the second operand as B.
    - ii. Write down the value of M required for the operation.
    - iii. Note down the values of the output carry C4 and data output S4-S1. Verify the results.

E.1 Report

1. Comment on the use of the XOR gates and the M bit of the 4-bit adder-subtractor.
2. Simulate a 4-bit adder in Logisim using basic logic gates. Provide a screenshot of the Logisim circuit schematic and truth table with your report.

Experiment 2: Ripple-Through-Carry Adder

C.2 Apparatus

- Trainer board
- 2 x IC 7483 4-bit binary adder

D.2 Procedure

1. Deduce the circuit diagram of an 8-bit ripple-through-carry binary adder using two 4-bit adders, clearly showing the pin numbers.
2. Construct the 8-bit adder.
3. Complete the operations in **Table F.2.1**

E.2 Report

1. Draw the IC diagram for the 8-bit ripple-through-carry adder.

Experiment 3: BCD Adder

C.3 Apparatus

- Trainer board
- 2 x IC 7483 4-bit binary adder
- 1 x IC 7408 quadruple 2-Input AND gates
- 1 x IC 7432 quadruple 2-Input OR gates

D.3 Procedure

1. Complete **Table F.3.1** for the BCD sum.

2. Construct the circuit of **Figure D.3.1**.
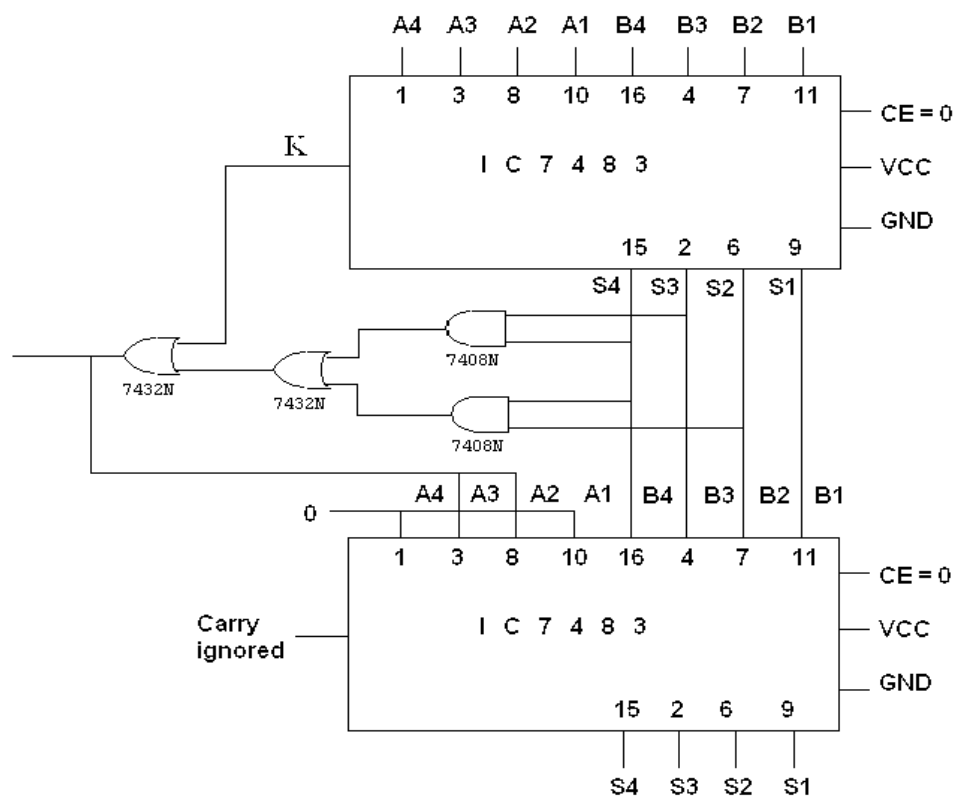
3. Verify the outputs in **Table F.3.2**

Figure D.3.1

E.3 Report

1. Derive the circuit for the BCD adder.

F.1 Experimental Data (Binary Adder-Subtractor):

Operation	M	A	B	C4	S4 S3 S2 S1
7 + 5					
4 + 6					
9 + 11					
15 + 15					
7 – 5					
4 – 6					
11 – 2					
15 – 15					

Table F.1.1

F.2 Experimental Data (Ripple-Through-Carry Adder):

Operation	A	B	Overflow Carry	Sum
7 + 5				
18 + 19				
72 + 83				
129 + 255				

Table F.2.1

F.3 Experimental Data (BCD Adder):

Decimal Value	Binary Sum					BCD Sum				
	K	Z_3	Z_2	Z_1	Z_0	C	S_3	S_2	S_1	S_0
0	0	0	0	0	0					
1	0	0	0	0	1					
2	0	0	0	1	0					
3	0	0	0	1	1					
4	0	0	1	0	0					
5	0	0	1	0	1					
6	0	0	1	1	0					
7	0	0	1	1	1					
8	0	1	0	0	0					
9	0	1	0	0	1					
10	0	1	0	1	0					
11	0	1	0	1	1					
12	0	1	1	0	0					
13	0	1	1	0	1					
14	0	1	1	1	0					
15	0	1	1	1	1					
16	1	0	0	0	0					
17	1	0	0	0	1					
18	1	0	0	1	0					
19	1	0	0	1	1					

Table F.3.1

Operation	A	B	Overflow Carry	Sum
9 + 0				
9 + 1		5		
9 + 2				
9 + 3				
9 + 4				
9 + 5				
9 + 6				
9 + 7				
9 + 8				
9 + 9				

Table F.3.2