LAB 3: Combinational Logic Design

A. Objectives

- Become familiarized with the analysis of combinational logic networks.
- Learn the implementation of networks using the two canonical forms.

B. Theory

Min terms and max terms
Analysis of combinational logic design
Canonical Forms

C. Apparatus

- Trainer Board
- 1 x IC 4073 Triple 3-input AND gates
- 2 x IC 4075 Triple 3-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)

D. Procedure

1. Write down all the min terms and max terms of three inputs ABC in Table F.1.
2. Write down the function F in 1st and 2nd Canonical Forms in in Table F.2
3. Draw the circuits for the 1st and 2nd canonical forms of function in Figure F.1, clearly indicating the pin numbers corresponding to the relevant ICs.
4. Construct the 1st canonical form of the circuit and test it with the truth table.
   i. Connect one min term at a time and check its output.
   ii. Once all min terms have been connected and verified, OR the min terms for the function output.
5. Construct the 2nd canonical form of the circuit and test it with the truth table.
   i. Connect one max term at a time and check its output.
   ii. Once all max terms have been connected and verified, AND the max terms for the function output.

E. Report

1. Draw the IC diagram for the 1st canonical form of the circuit in Figure F.1
2. Simulate the circuit for the 2nd canonical form in Figure F.1 in Logisim. Provide a screenshot of the Logisim circuit schematic and truth table with your report.

F. Experimental Data

Experiment conducted by:

Name	ID

Input Reference	$A\ B\ C$	F	Min term	Max term
0	0 0 0	0		
1	0 0 1	1		
2	0 1 0	1		
3	0 1 1	0		
4	1 0 0	0		
5	1 0 1	0		
6	1 1 0	1		
7	1 1 1	0		

Table F.1 Truth table to a combinational circuit

	Shorthand Notation	Function
1st Canonical Form	$F = \Sigma$	$F =$
2nd Canonical Form	$F = \Pi$	$F =$

Table F.2 1st and 2nd canonical forms of the combinational circuit of Table F.1

1st Canonical Form

2nd Canonical Form

Figure F.1 1st and 2nd canonical circuit diagrams of the combinational circuit of Table F.1