**SIMULATIONS of Lab-5**

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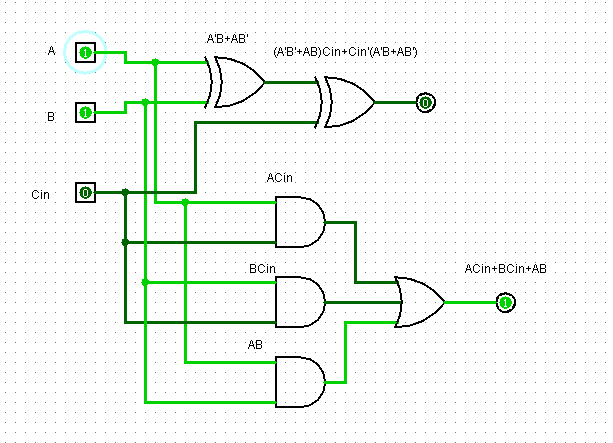


Figure: Full Adder Circuit

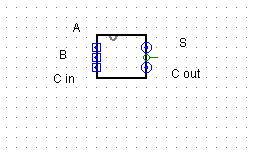


Figure: Full Adder Subcircuit

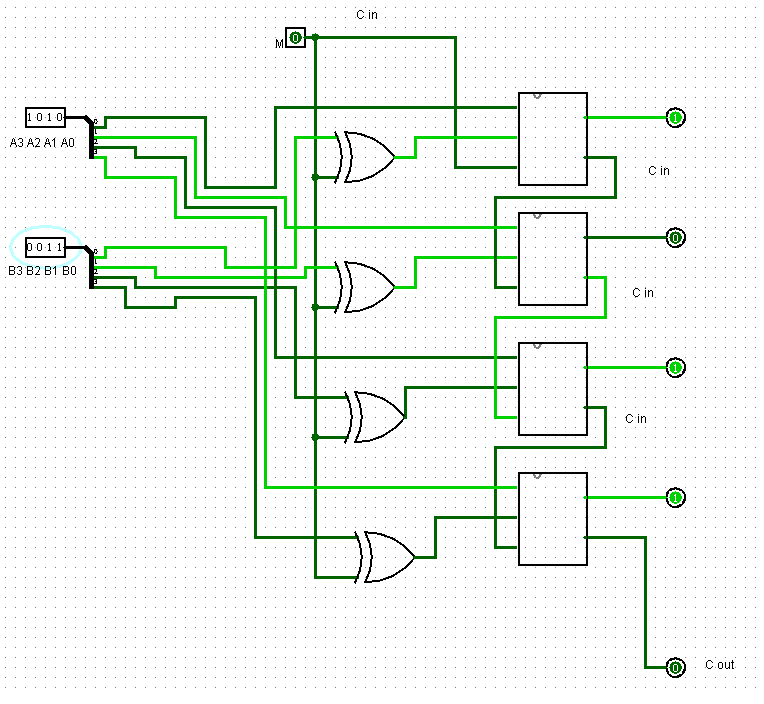


Figure: 4-bit binary Adder-Subtractor

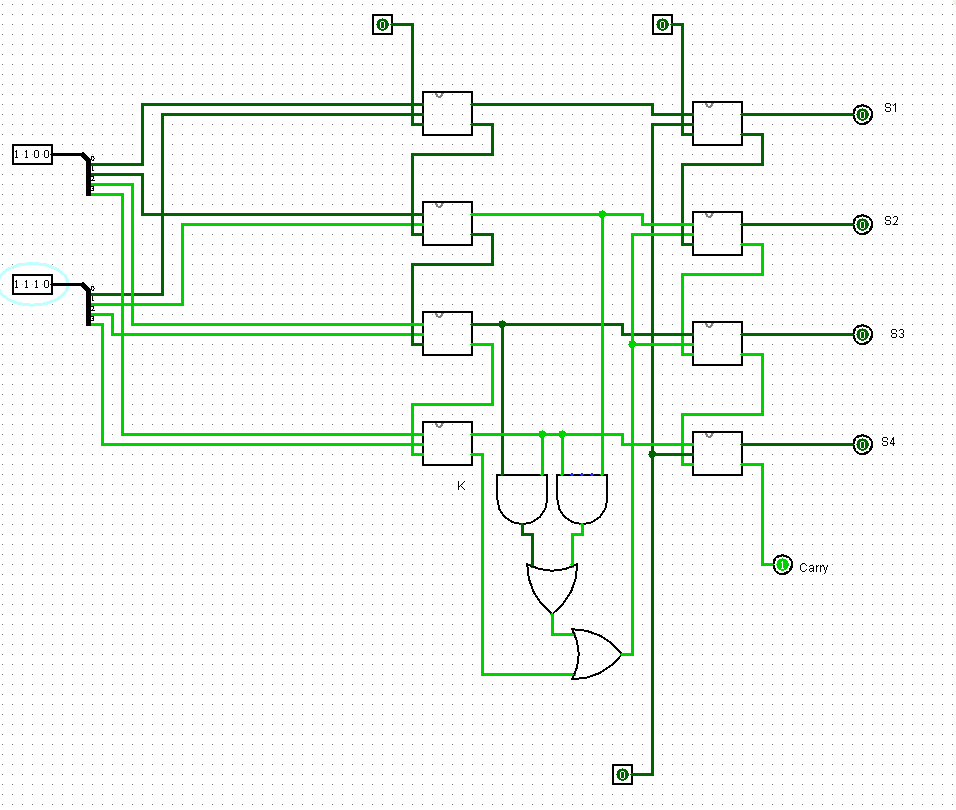


Figure: BCD Adder