

# *P300 Event Detection using Feature Extraction Technique in FPGA*

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**Abstract**—EEG signals are neuroelectric signals which helps in analyzing the brain state of the Human being. Extracting Features of EEG signal in real time is the most challenging task because of its high variability and complexity. In this paper we have used FPGA (Virtex-5) for extracting the features in real time for Brain Computer Interface applications. Nowadays, Brain Computer Interface (BCI) plays a major crucial role in helping the persons those who are partly or wholly incapable of movement. BCI system which depends on neural signals generated by the brain and these neural signals are recorded using Non Invasive or Invasive techniques. In non invasive technique like EEG (electroencephalography) recordings are taken from the scalp and it is used for analyzing the brain's activity. When compared to Invasive one, non-invasive techniques give a lesser accuracy and less harm to humans. To improve the accuracy and efficiency of the system, appropriate classification and feature extraction methods are chosen. Existing BCI feature extraction techniques, extracts many features such as band energies ,power spectral density etc., but achieving a good classification accuracy is a great challenge. In our paper, this problem is addressed by extracting only P300 event and a good classification accuracy is obtained. EEG signals are stored in internal Block RAM to reduce the design time and complexity. This Block RAM is easy to design and improves the processing speed. The features are extracted from EEG signal using Hanning filter and FIR filter. The performance of FIR and Hanning filter is compared in terms of classification accuracy, using Fisher Linear Discriminator. The area, power and delay are compared by implementing the proposed approach in Virtex-5. However, FIR filter occupies more area, it has very high classification accuracy. Since accuracy plays a major role in BCI applications such as P300 speller,Wheel chair control through EEG, Drivewaves, NeuroBrush, FIR is chosen as Feature extraction technique.

**Keywords**—Accuracy, Efficiency, Hanning filter, FIR filter, FPGA

## I. INTRODUCTION

Researches in Brain Computer interface were carried out decades ago to aid the disabled persons to interact with the

environment without any support. The initial step of the BCI is to record the brain waves generated by the neurons. The human brain consists of nearly  $10^{10}$  to  $10^{11}$  neurons [2]. Due to the burst of short electric pulse, signals are transmitted between neurons as action potential. The action potential of neuron creates electrical activity in the brain. The electrical activities are measured as EEG (Electroencephalography) waves. EEG is used both in clinical purpose as well as in research for evoked potential study. An EEG signal consists of different component with different characteristics large amount of data received from one single trial is very difficult to interpret. These recorded EEG waves originate from this neural communities differ by a number of characteristics such as amplitude, latency, firing rate, topographic location, etc., The specific components such as P300 events[1] are extracted and linked to the algorithms for classification purpose.

Many Researches have provided an approach to new efficient design algorithm to synthesize low complexity FIR filters, which has been applied to EEG signals feature extraction filter bank [3]. However the area consumption and power issues are not addressed in their approach. The feature extraction is done using DWT but which is not implemented in real time [4]. For BCI application, Common spatial method is used as feature extraction and Fisher Linear Discriminator is used as classifier [5], in which classification of hand movement in South –North direction is done with high accuracy. Classification of hand movement in other direction is done with low accuracy. The steady state evoked potential is classified and the results are used to control the vehicle [6]. It demonstrated the feasibility of using the human “mind” to control a vehicle at a speed ranging from 7.2 to 10.8 km/h. Even the same SSVEP is used with high accuracy for driving wheel chair. A wheelchair controlled by EEG signals with 95 % accuracy is obtained [7].

In this paper, features are extracted using a Hanning filter as well as an FIR band pass filter. Extracted features are used for EEG signal classification. This paper also discusses about the accuracy of classification power consumption, area occupied as well as delay of the proposed feature extraction technique. The proposed method is implemented in real time using FPGA.

The structure of the paper is as follows. Section II discusses about EEG data set processing. Section III explains the proposed method and algorithm used. Section IV discusses the result.

## II. EEG DATA SET

The EEG signals are recorded by placing the electrode in Occipital (O1) region with ear linked reference electrode. The artifacts in the EEG signals are removed. The recorded EEG sets are pre filtered to 0.1 to 70Hz [8]. The sampling rate is 250 Hz after band pass filter. There are totally 512 samples from a single data set. These samples are divided into pre-stimulations (256) and post-stimulations (256). The subjects are stimulated with oddball paradigm. Two different stimuli are given in pseudo random method or an oddball paradigm with both non-target and target stimuli. The subject ignores the non-target and counts the target stimuli.

## III. PROPOSED METHOD

The proposed method consists of EEG signal preprocessing followed by Feature extraction and Classification. The EEG data recorded from each electrode is predicted by SOFNN(Self Organized Fuzzy Neural Network).

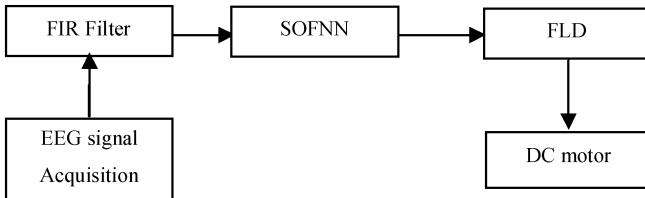


Figure 1. Proposed method

The flow model for BCI application is described in the Figure 1. The BCI application mentioned here is driving a DC motor. An Event-Related Potential (ERP) is the measured brain response due to specific sensory, cognitive, or motor event. P300 is a type of ERP. The P300 response occurs at around 300ms in the oddball paradigm. It occurs between the frequencies 0.5 – 8Hz.

### A. Internal Block RAM

Single Port Block RAM is arranged in 60 blocks, with the 36K Block RAM bits in the Virtex5. The on-chip embedded memory RAM is used to reduce the RAM memory design time and it is easy to implement in FPGA. The EEG database is loaded in the BLOCK RAM as shown in Figure 2.

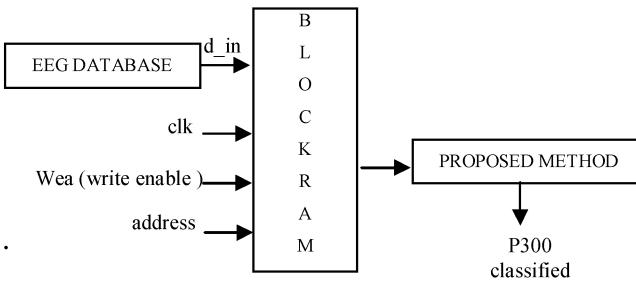


Figure 2. Internal BLOCK RAM

The EEG database is loaded as a COE file during initialization. Since the memory is loaded during initialization itself, only reading phase happens during simulation. The write enable is always tied to zero in this method. The address register will be incremented in each clock cycle and the corresponding memory output strobes out in the next clock cycle.

### B. FIR band pass filter

FIR filters are the most widely used DSP blocks because of its low coefficient sensitivity, guaranteed stability and linear phase property. The FIR filter plays a major role in image, video and signal processing applications. The P300 response occurs at around 300ms in the oddball paradigm. It occurs between the frequencies 0.5 -8Hz. FIR filter is implemented by convolving the input samples with coefficients as given in (1)

$$y(n) = \sum_{i=0}^n b_i x(n-i) \quad (1)$$

Where  $b_i$  is the  $i_{th}$  coefficient of FIR filter,  $y(n)$  and  $x(n)$  are output and input samples respectively.

The Figure 3 represents the FIR Filter realization structure. The output of a non-recursive filter is a function of the input signal. The response of the FIR filter to an impulse consists of a finite sequence of the  $M+1$  sample and those samples are the coefficients of FIR filters, where  $M$  is the filter order. Hence, the filter is known as a Finite-Duration Impulse Response (FIR) filters.

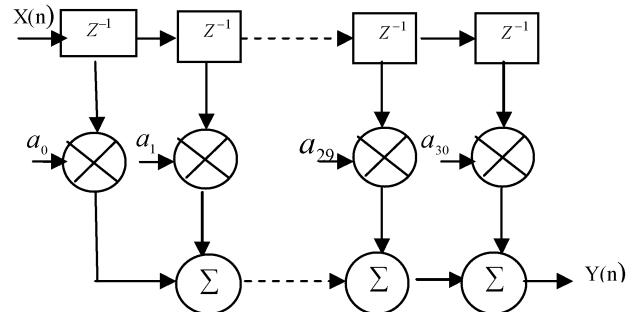


Figure 4. Hanning filter structure

Hanning filter is easy to implement. The structure is same as the FIR filter but the coefficients of the Hanning filter is set to one always. The output of the filter is shifted to find out the average. Hanning filter is easy to implement.

#### D. Self Organized Fuzzy Neural Network(SOFNN)

The EEG data recorded from each electrode is predicted by SOFNN. The features are extracted from Mean square error of predictions. The SOFNN is a multiple input single output mechanism .When a trial is given as input to SOFNN, features can be extracted by calculating Mean Squared Error of the actual prediction for a segment of a trial.

#### E. Fisher Linear Discriminator

The classifier used in this paper is Fisher Linear Discriminator. The local minima and local maxima of Region of interest are calculated. Their difference is used as the scaling factor as given in (3)

$$V_{i,scaled}(t) = \frac{V_i(t) - V_{i,min}}{V_{i,max} - V_{i,min}} \quad (3)$$

Where  $V_i(t)$  and  $V_{i,scaled}(t)$  denote the Event Related Potentials in the EEG dataset, at the location I before scaling and after scaling respectively. The values  $V_{i,min}$  and  $V_{i,max}$  are the minimum and maximum of the data set at the same location.

## IV. RESULTS

The EEG signals are stored in Internal Block Ram for fast processing. The input signal is as shown in Figure 5

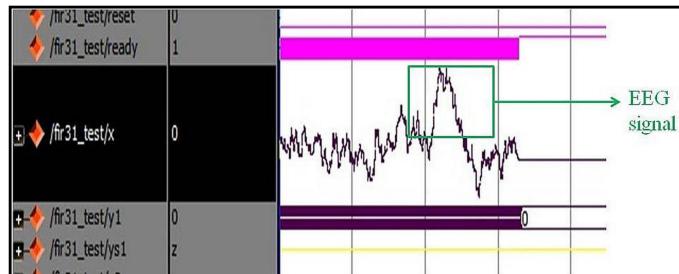


Figure 5. Simulation waveform of EEG signal

The FIR band pass filter coefficients are obtained from the MATLAB at a cutoff frequency at 0.5 and 0.8 Hz. The data's are sampled at the frequency of 250Hz. The 31-tap filter is designed in Verilog. The P300 occurs between 0.5 to 8 Hz. The EEG signal is filtered out to the expected frequency using the FIR filter coefficients  $a_0$  to  $a_{30}$  mention above. The output waveform of FIR filter is as shown in Figure 6

Moving window is framed to the size of eight and the average is calculated for the eight samples. The result of the Hanning filter will be smoother when compared to FIR filter output as shown in Figure 7



Figure 6. Output waveform of FIR filter

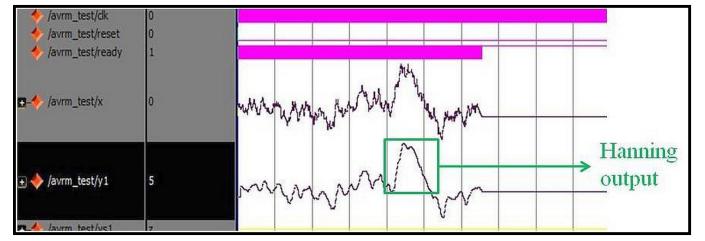


Figure 7. Output waveform of Hanning filter

The total number of samples taken in the database for a single trial is 512. The P300 occurs only after 300 samples (i.e.,300ms after stimuli) The Fisher Linear Discriminator is used for Classification and P300 is classified as shown in Figure 8.



Figure 8. Output waveform of Classifier

The proposed method is analyzed using 10 databases. The Figure 9 and Figure 10 show the classification of P300 event using FIR and Hanning filter for Data1 respectively. Both filters have classified the P300 event.

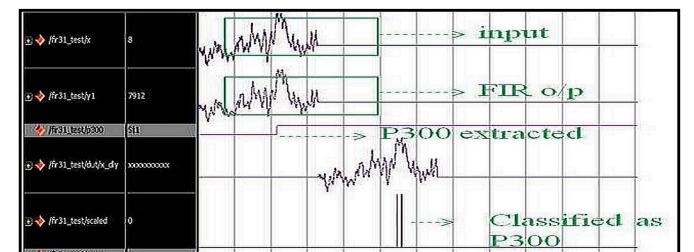


Figure 9. FIR for DATA1

The Figure 11 and Figure 12 shows the classification of the P300 event using FIR and Hanning filter for Data2 respectively. FIR classified the event but the Hanning filter misclassified the event as Non-P300 event.

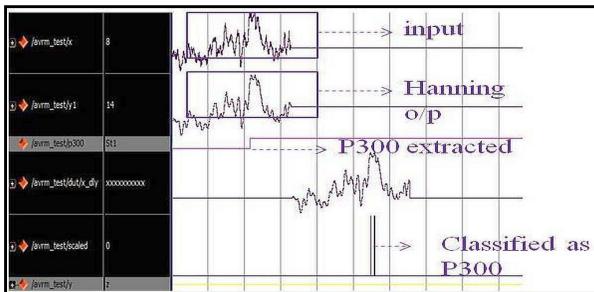


Figure 10. Hanning for DATA1



Figure 11. FIR for DATA2

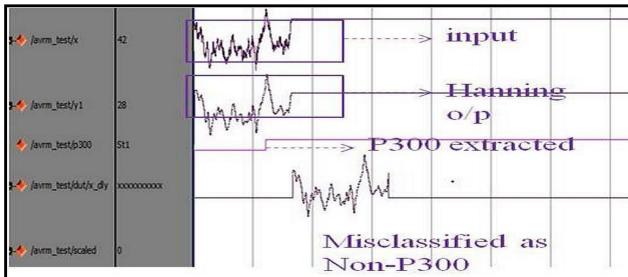


Figure 12. Hanning for DATA1

Current design trends are portable devices with high-performance and low power. Designing the low power boards addressing key issues to improve the performance is extremely challenging & demanding. Figure 13 and Figure 14 shows the graph which is plotted between power and function of the FIR and Hanning filter respectively. The logic power consumption and I/O power consumption is more in FIR compared to Hanning filter.

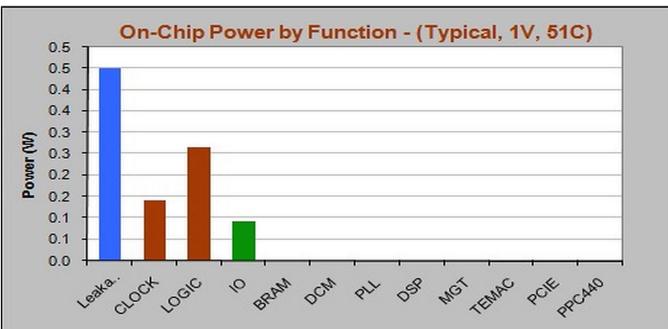


Figure 13. Power vs Function Graph for FIR

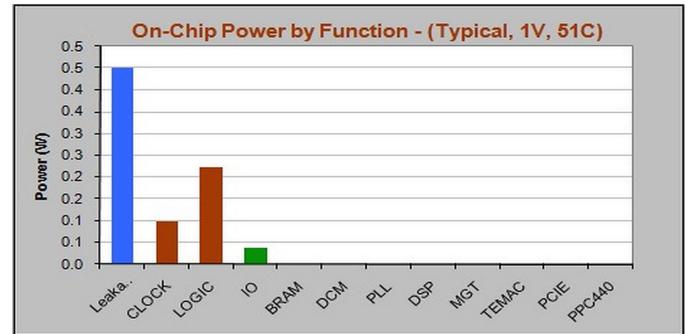


Figure 14. Power vs Function Graph for Hanning filter

Core voltage means that the chip is working on this voltage. VCCINT means a core voltage input, this pin needs to be connected to a specific voltage (2.5V for Virtex). The core voltage is named "VCC" for Xilinx and "VCCINT" for Altera. It is fixed for all FPGA. It is used to power the flip-flops and logic gates inside the FPGA. The core voltage was 5V for older version of FPGA generations, and for new generation it has been reduced (2.5v, 1.5V, 1.2V and lower for the latest devices). Figure 15 and Figure 16 shows the graph plotted across power and Vccint for FIR and Hanning respectively. The power consumption FIR is nearly 14 % more than Hanning filter.

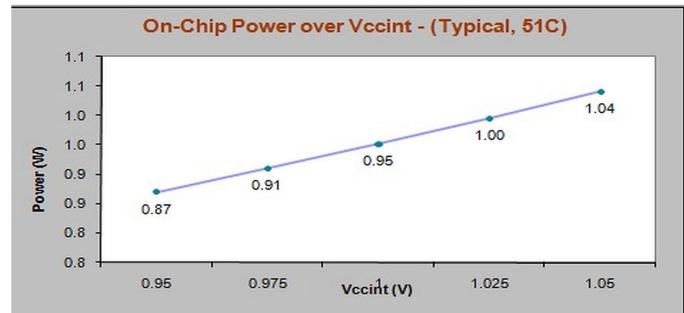


Figure 15. Power vs Vccint Graph for FIR filter

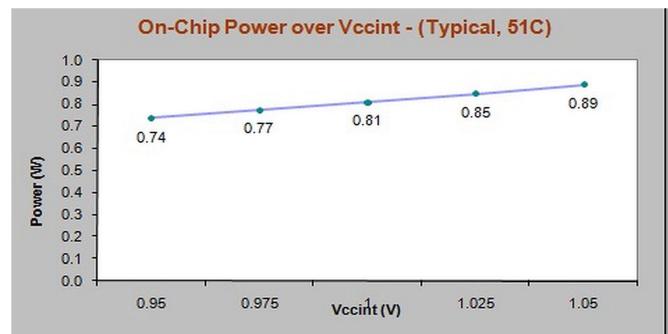


Figure 16. Power vs Vccint Graph for Hanning filter

The performance of the designs implanted using FPGAs are affected by Process-Voltage-Temperature (PVT) variation. The design should be operated under variation of different conditions simultaneously. Figure 17 and Figure 18 shows the graph plotted across typical power and maximum power is for FIR and Hanning filter respectively. As the temperature

increases, the power consumption of FIR filter increases more when compared to Hanning filter

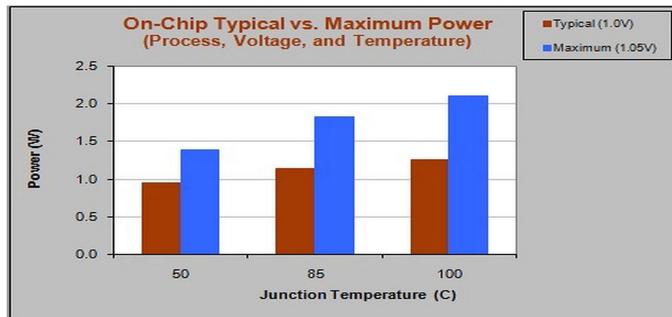


Figure 17. Typical Vs Maximum power for FIR filter

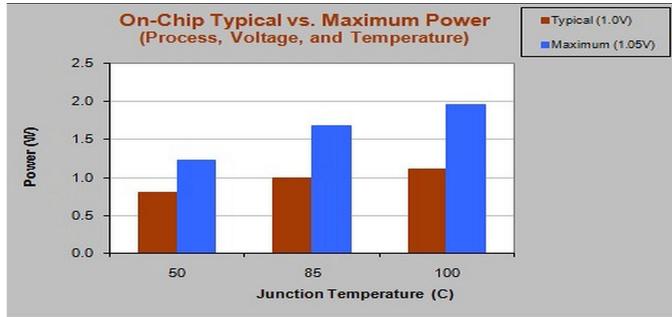


Figure 18.Typical Vs Maximum power for Median filter

Flash and Anti fuse technologies have relatively small increases in power with temperature. SRAM-based FPGAs will have a larger increase in power consumption for higher temperatures. Designs may run hotter than the expectation of designers, leading to surprises in power consumption. The power measured over temperature is plotted for FIR and Hanning filter as shown in Figure 19 and Figure 20

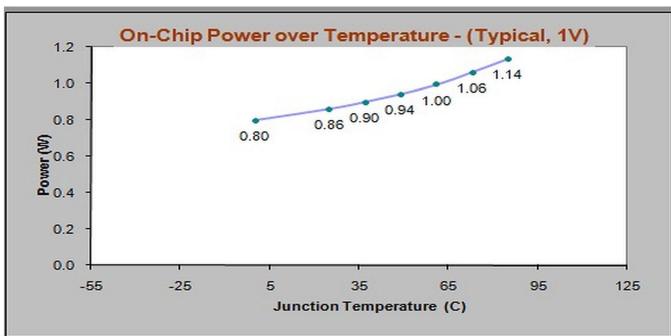


Figure 19. Power vs Temperature for FIR filter

Once the features are extracted from the two techniques, FIR band pass filter and Hanning filter, the extracted features are classified using Fisher linear discriminator. The proposed method is implemented in FPGA (Virtex-5).

The Xilinx Virtex-5 FPGAs offers a huge performance enhancement over previous FPGA generation. Improvements from previous version of FPGAs include special Digital Signal Processing slices for complex mathematical operations, six-input look-up tables (LUTs), and diagonally symmetric interconnect pattern. The area of resource utilization and

classification accuracy is compared for FIR and Hanning Filter and it is shown in Table 1.

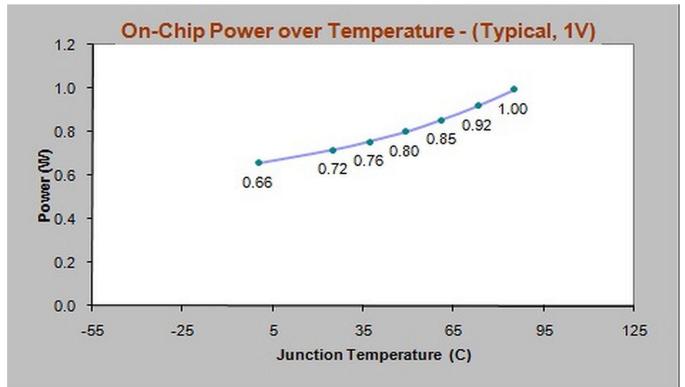


Figure 20.Power vs Temperature for Hanning filter

TABLE I Comparison Table

Comparison		
Parameters	FIR	Hanning
Design Complexity	Medium	Easy
Programming	Verilog	Verilog
Classification accuracy	90%	60%
No.of slice Registers Utilized	29%	19%
No.of LUT's utilized	61%	55%
No.of LUT FF pairs	44%	34%
No.of Block RAM	1	1
Maximum clock Frequency(MHz)	103.799	104.156
On-Chip Power	0.091(10%) 0.411(43%) 0.451(47%)	0.037(5%) 0.323(40%) 0.450(56%)

The Table 1 compares the various parameters between FIR and Hanning. From the Table 1, The Hanning filter is easy to design and the area utilization is less when compared to FIR. The FIR filter provides 30% more accuracy when compared to Hanning filter. The FIR filter occupies 10 % of register greater when compared to Hanning. The Hanning filter utilizes 6% LUT's and 10 % LUT FF pair lesser when compared to FIR filter. From the timing summary, the speed of the FIR is 0.3 % less when compared to Hanning filter. The Minimum time period of FIR filter design is 9.634ns and for the Hanning design it is 9.601ns. The Power consumption of the filters are analyzed. The Static power consumption is same for both Hanning and FIR filter. The Dynamic power consumption is more for FIR filter when compared to Hanning. However, Accuracy is the major parameter for BCI application, so FIR filter is chosen as the best for the proposed method for real time application.

## V. CONCLUSION

Two methods, FIR and Hanning filters are implemented for the feature extraction techniques. The design complexity of the FIR band pass filter is medium since both accumulators

and multipliers need to be designed. The Hanning filter is easy to design and implement, since multiplier operation is not needed. There is a tradeoff between area and accuracy. Classification Accuracy for FIR filter technique is better when compared to Hanning filter technique. The area utilization is smaller for Hanning filter compared to FIR. Even though Hanning filter occupies less area, consumes less power and operates with a speed greater than FIR, FIR is chosen as the best since it has high accuracy. The EEG database is taken offline and processed in this paper. The EEG database can be taken in real time by placing the electrodes on the scalp of the subject. The location of the electrodes should be chosen which gives high accuracy. The ADC needs to be designed and interfaced with the FPGA. The amplifier circuits need to be chosen and designed in such a way that it amplifies the very low voltage of EEG signals.

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