

# CS6135 VLSI Physical Design Automation

## Homework 1: P&R Tool

1. 112062525 蔡品棠

### 2. Comparison Table

core utilization: 0.6, clock period: 6ns

	(congestion-driven, timing-driven)					
	(L, off)	(L, on)	(M, off)	(M, on)	(H, off)	(H, on)
slack	0.011	0.025	0.010	0.001	0.010	0.001
total wire length (um)	111462.1050	112174.9700	112002.9350	113266.4600	112002.9350	113266.4600

(1) 在此 design 中，congestion-driven 對 slack 的影響比 timing-driven 多。從 timing-driven 設定相同時來看，congestion-driven 程度越高，slack 的值便越低；而 congestion-driven 設定相同時，則有開啟 timing-driven 時會增加 slack。但 congestion-driven level 為 Medium 和 High 時，因減少的 slack 比 timing-driven 增加的要多，才會呈現 timing-driven = off 時 slack 反而較高的現象。

(2) timing-driven 會較明顯增加 total wire length

congestion-driven 程度越高雖然也會增加 total wire length，但從 M 和 H 的 total wire length 相同可以知道影響程度較小；然而 timing-driven 有開啟的話就一定會增加 total wire length。

### 3. The difference(s) between the congestion-driven placement and timing-driven placement

congestion-driven placement: 主要目標是減少或最小化 chip 上的擁擠，確保 components 的放置和連線不會導致過多的交叉、過度擁擠的區域或無法滿足設計規格。

timing-driven placement: 目標是滿足時序要求，確保設計在 clock period 內能夠正確操作，並優化 critical path delays。

### 4. Why we insert filler cells

主要是為了解決 layout 階段中的製造相關問題。比如在 VLSI 設計中，晶片的外型和尺寸通常是固定的，但內部的電路佈局和連線可能會產生不均勻的空間分佈，此時加入 filler cells 可以用來均勻化晶片的 layout，

來確保所有區域都能被充分利用，並緩解擁擠問題。另外雖然 filler cells 增加了晶片的面積，但可以幫助減少不良晶片或低良率的狀況發生，進而有助於降低製造成本。

## 5. Best result

Setting		Result	
Clock period	8 ns	Slack	0.001
Core utilization	0.75	Total wire length	106149.1350 um
Congestion-driven	Low	Total area of chip	13787.525 um <sup>2</sup>
Timing-driven	off	DRC violation	0

clock period = 8 ns

```

design.sdc
design.sdc
1 #####
2
3 # Created by write_sdc on Fri Jan 14 18:07:42 2022
4
5 #####
6 set sdc_version 2.0
7
8 set_units -time ns -resistance MOhm -capacitance fF -voltage V -current mA
9 create_clock [get_ports clk] -name CLK -period 8 -waveform {0 4}

```

core utilization = 0.75

```

summary.rpt apr.tcl
D: > NTHU > Master > 11201 > VLSI PDA > apr.tcl
28 saveDesign setup
29 getIoFlowFlag
30 setIoFlowFlag 0
31 floorPlan -site FreePDK45_38x28_10R_NP_162NW_340 -r 1.0 0.75 4.0 4.0 4.0 4.0

```

congestion-driven = low, timing-driven = off

```

summary.rpt apr.tcl
D: > NTHU > Master > 11201 > VLSI PDA > apr.tcl
38 setNanoRouteMode -quiet -droutePostRouteSpreadWire 1
39 setNanoRouteMode -quiet -timingEngine {}
40 setUsefulSkewMode -noBoundary false -maxAllowedDelay 1
41 setPlaceMode -reset
42 setPlaceMode -congEffort low -timingDriven 0 -clkGateAware 1 -powerDriven 0 -ignoreScan 1 -reorderScan 1 -ignoreSpare 0 -placeIOPins 1 -moduleAw

```

slack time = 0.169

≡ apr.tcl	≡ timing.rpt ×
≡ timing.rpt	
14	Analysis View: generic_view
15	Other End Arrival Time 0.000
16	- Setup 0.173
17	+ Phase Shift 8.000
18	= Required Time 7.827
19	- Arrival Time 7.659
20	= Slack Time ..... 0.169

total wire length = 106149.1350 um

≡ apr.tcl	≡ summary.rpt ×
≡ summary.rpt	
1634	=====
1635	Wire Length Distribution
1636	=====
1637	Total metal1 wire length: 2303.0550 um
1638	Total metal2 wire length: 26921.4800 um
1639	Total metal3 wire length: 38520.7100 um
1640	Total metal4 wire length: 21722.1200 um
1641	Total metal5 wire length: 8301.9300 um
1642	Total metal6 wire length: 8379.8400 um
1643	Total wire length: 106149.1350 um

total area of chip = 13787.525 um<sup>2</sup>

≡ apr.tcl	≡ summary.rpt ×
≡ summary.rpt	
1613	Total area of Standard cells(Subtracting Physical Cells): 9717.778 um^2
1614	Total area of Macros: 0.000 um^2
1615	Total area of Blockages: 0.000 um^2
1616	Total area of Pad cells: 0.000 um^2
1617	Total area of Core: 11920.524 um^2
1618	Total area of Chip: 13787.525 um^2

0 drc violations

≡ apr.tcl	≡ drc.rpt ×
≡ drc.rpt	
14	VERIFY DRC ..... Thread : 3 finished.
15	VERIFY DRC ..... Sub-Area: {60.480 58.320 118.940 115.920} 4 of 4 Thread : 0
16	VERIFY DRC ..... Thread : 0 finished.
17	
18	Verification Complete : 0 Viols.
19	
20	*** End Verify DRC (CPU: 0:00:01.1 ELAPSED TIME: 1.00 MEM: 256.1M) ***

## 6. The final layout

