CS6135 VLSI Physical Design Automation

Homework 1: P&R Tool

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2. **Comparison Table**

core utilization: 0.6, clock period: 6ns

	(congestion-driven, timing-driven)					
	(L, off)	(L, on)	(M, off)	(M, on)	(H, off)	(H, on)
slack	0.011	0.025	0.010	0.001	0.010	0.001
total wire length (um)	111462.1050	112174.9700	112002.9350	113266.4600	112002.9350	113266.4600

(1) 在此 design 中，congestion-driven 對 slack 的影響比 timing-driven 多

從 timing-driven 設定相同時來看，congestion-driven 程度越高，slack 的值便越低；而 congestion-driven 設定相同時，則有開啟 timing-driven 時會增加 slack。但 congestion-driven level 為 Medium 和 High 時，因減少的 slack 比 timing-driven 增加的要多，才會呈現 timing-driven = off 時 slack 反而較高的現象。

(2) timing-driven 會較明顯增加 total wire length

congestion-driven 程度越高雖然也會增加 total wire length，但從 M 和 H 的 total wire length 相同可以知道影響程度較小；然而 timing-driven 有開啟的話就一定會增加 total wire length。

3. **The difference(s) between the congestion-driven placement and timing-driven placement**

congestion-driven placement: 主要目標是減少或最小化 chip 上的擁擠，確保 components 的放置和連線不會導致過多的交叉、過度擁擠的區域或無法滿足設計規格。

timing-driven placement: 目標是滿足時序要求，確保設計在 clock period 內能夠正確操作，並優化 critical path delays。

4. **Why we insert filler cells**

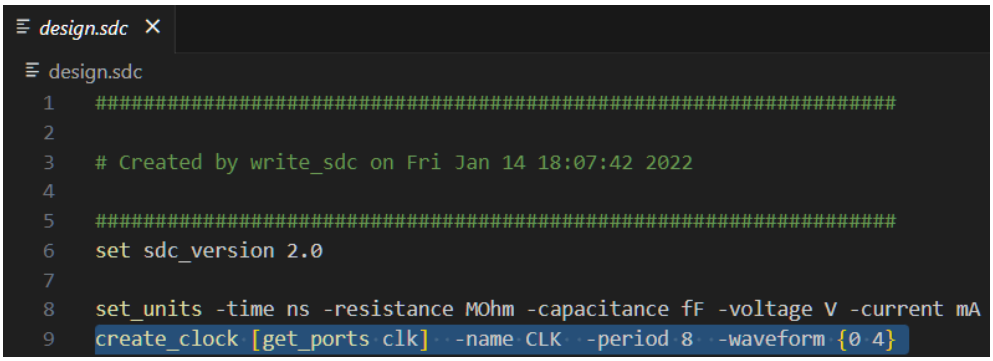
主要是為了解決 layout 階段中的製造相關問題。比如在 VLSI 設計中，晶片的外型和尺寸通常是固定的，但內部的電路佈局和連線可能會產生不均勻的空間分佈，此時加入 filler cells 可以用來均勻化晶片的 layout，

來確保所有區域都能被充分利用，並緩解擁擠問題。另外雖然 filler cells 增加了晶片的面積，但可以幫助減少不良晶片或低良率的狀況發生，進而有助於降低製造成本。

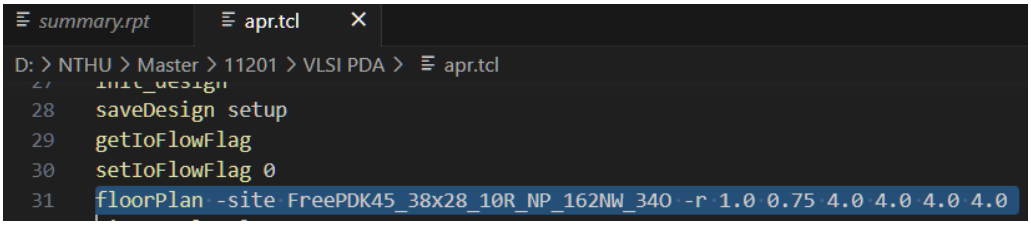
5. **Best result**

Setting		Result	
Clock period	8 ns	Slack	0.001
Core utilization	0.75	Total wire length	106149.1350 um
Congestion-driven	Low	Total area of chip	13787.525 um^2
Timing-driven	off	DRC violation	0

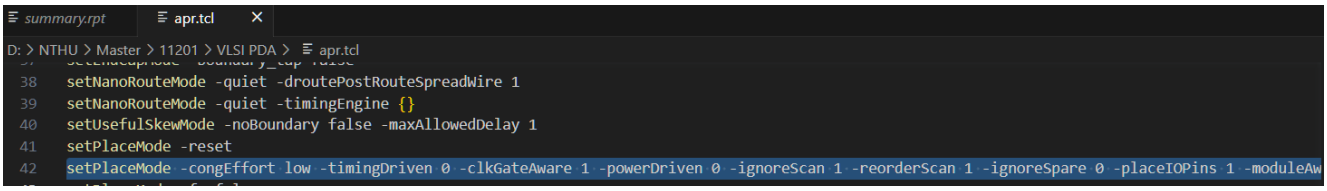
clock period = 8 ns



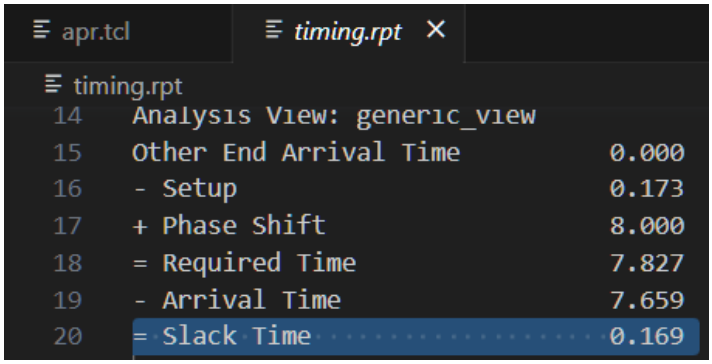
core utilization = 0.75



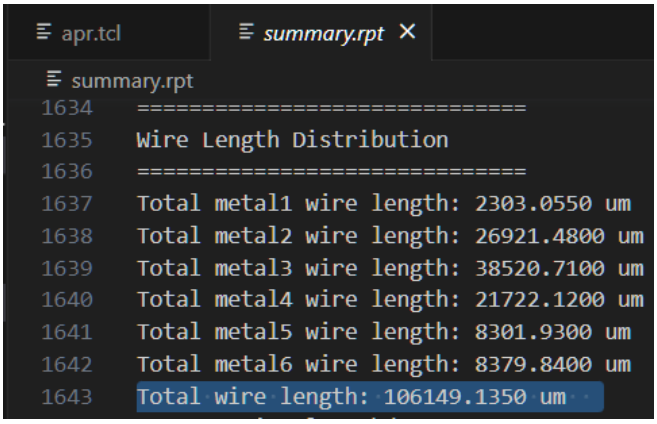
congestion-driven = low, timing-driven = off



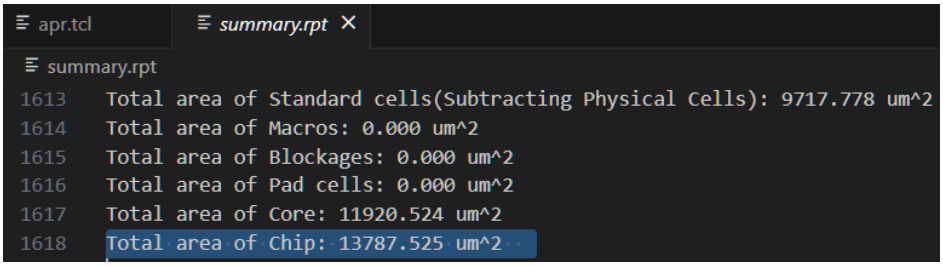
slack time = 0.169



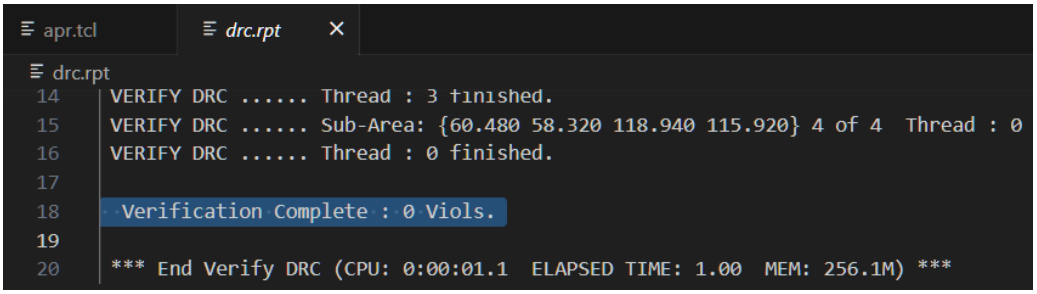
total wire length = 106149.1350 um



total area of chip = 13787.525 um^2



0 drc violations



6. **The final layout**