Mira220

Datasheet

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Mira220 1/2.7” 2.2 MP NIR enhanced global shutter image sensor

1 General description

Mira220 is a 2.2 MP NIR enhanced global shutter image sensor designed for 2D and 3D consumer and industrial machine vision applications. The sensor has a small 2.79 µm pixel size with high sensitivity made possible by a state of the art BSI technology. With an effective resolution of 1600 × 1400 and a maximum bit depth of 12 bits, the sensor supports on-chip operations like external triggering, windowing, horizontal or vertical mirroring. The maximum frame rate is 90 fps at full resolution and bit depth. The sensor has a MIPI CSI-2 interface to allow easy interfacing with a plethora of processors and FPGAs. On-chip registers can be accessed via the standard I²C interface for easy configuration of the sensor.

Due to its small size, configurability and high sensitivity both in visual as well as NIR, the Mira220 is well suited for 2D and 3D applications, which include Active Stereo Vision, Structured Light Vision for Robotics and AR/VR. High sensitivity in NIR enables increased measurement range and allows overall system power consumption optimization which is key for battery powered consumer and industrial applications.

1.1 Key benefits & features

The benefits and features of Mira220, 1/2.7” 2.2 MP NIR enhanced global shutter image sensor are listed below:

Table 1: Key benefits & features

Benefits	Features
Compact size with high resolution and bit depth	1/2.7” 1600 x 1400 8/10/12-bit 2.79 µm
High speed applications	90 fps global shutter with CDS
Use in low light conditions	High sensitivity
Compact size	Small die size achieved via state of the art BSI technology.
NIR enhanced with high sensitivity	Class leading QE at 940 nm combined with high sensitivity. Industry leading PLS at 940 nm.
On-chip noise reduction	Digital CDS and row noise correction
Reduced off-chip processing	• On-chip defect pixel detection and correction • On-chip image statistics generation
Extended battery operation	Low power consumption

1.2 Applications

- Mobile facial authentication
- Active stereo vision
- Structured light vision
- Smart home appliances
- Automatic identification and data capture (AIDC)
- QR readers
- Drones
- Smart wearable devices
- SLAM for robotics
- AR/VR

2 Ordering information

Product type	Ordering code	Type	Package	Glass	Protective film	Delivery form	MOQ
Mira220-2QM1WP	Q65114A0086	Mono	CSP	Plain	Yes	Tape and reel	Multiples of 2000
Mira220-2QM1WA	Q65114A0087	Mono	CSP	AR	Yes	Tape and reel	Multiples of 2000
Mira220-2QM1WO	Q65113A5069	Mono	CSP	Plain	No	Tape and reel	Multiples of 2000
Mira220-2QC1WP	Q65113A5403	RGB	CSP	Plain	Yes	Tape and reel	Multiples of 2000
Mira220-2QC1WA	Q65113A5404	RGB	CSP	AR	Yes	Tape and reel	Multiples of 2000
Mira220-2QC1WO	Q65113A5405	RGB	CSP	Plain	No	Tape and reel	Multiples of 2000
Mira220-2QI1WP	Q65113A5408	RGBIR	CSP	Plain	Yes	Tape and reel	Multiples of 2000
Mira220-2QI1WA	Q65113A5409	RGBIR	CSP	AR	Yes	Tape and reel	Multiples of 2000
Mira220-2QI1WO	Q65113A5410	RGBIR	CSP	Plain	No	Tape and reel	Multiples of 2000
Mira220-2QM1D0	Q65114A0085	Mono	RW	-	-	Reconstructed wafer	Contact Sales
Mira220-2QC1D0	Q65113A5399	RGB	RW	-	-	Reconstructed wafer	Contact Sales
Mira220-2QI1D0	Q65113A5406	RGBIR	RW	-	-	Reconstructed wafer	Contact Sales
Mira220-2QM1WP	Q65113A5999	Mono	CSP	Plain	Yes	Tape and reel	Multiples of 500
Mira220-2QM1WA	Q65113A6000	Mono	CSP	AR	Yes	Tape and reel	Multiples of 500
Mira220-2QC1WP	Q65113A5997	RGB	CSP	Plain	Yes	Tape and reel	Multiples of 500
Mira220-2QC1WA	Q65113A5998	RGB	CSP	AR	Yes	Tape and reel	Multiples of 500
Mira220-2QI1WP	Q65113A5995	RGBIR	CSP	Plain	Yes	Tape and reel	Multiples of 500
Mira220-2QI1WA	Q65113A5996	RGBIR	CSP	AR	Yes	Tape and reel	Multiples of 500

3 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2: Absolute maximum ratings of Mira220

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Electrical parameters						
VDD25	Analog and pixel supply voltage			3.63	V	
VDD18	I/O supply voltage			4.125	V	
VDD13A	Analog supply voltage			3.63	V	
VDD13D	Digital supply voltage			3.63	V	
VDD13P	MIPI, D-PHY and PLL supply voltage			3.63	V	
Digital I/O						
I_{SCR}	Input current (latch-up immunity)		± 100		mA	JEDEC JESD78D Nov 2011
Continuous power dissipation						
P_T	Continuous power dissipation		350		mW	At full resolution, bit depth and speed.
Electrostatic discharge						
ESD_{HBM}	Electrostatic discharge HBM		± 2		kV	MIL-STD-883J
ESD_{CDM}	Electrostatic discharge CDM		± 1000		V	JS-002-2018
Temperature ranges and storage conditions						
R_{THJP}	Junction to package thermal resistance			0.89	°C/W	
T_J	Operating junction temperature	-30		90	°C	
T_{BODY}	Package body temperature			260	°C	IPC/JEDEC J-STD-020(1)
	Number of reflow cycles			3		Due to the small pad pitch, standard reflow process may need to be adjusted to achieve reliable solder result.
T_{DRY}	Recommended dry bake temperature	105		125	°C	IPC/JEDEC J-STD-020(1)
t_{DRY}	Recommended dry bake time	8		24	h	125 °C
MSL	Moisture sensitivity level		3			Represents a floor life time of 168 h.
RH_{NC_CSP}	Relative humidity (non-condensing) for CSP	5		85	%	
RH_{NC_RW}	Relative humidity (non-condensing) for RW			30	%	N_2 stocker conditions

Symbol	Parameter	Min	Typ	Max	Unit	Comments
T_{STRG_CSP}	Storage temperature for CSP	-40		85	°C	
T_{STRG_RW}	Storage temperature for RW	17		28	°C	
t_{STRG_CSP}	Storage time for CSP			1	year	According to MSL3
t_{STRG_RW}	Storage time for RW			3	months	Refers to indicated date of packing.

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”. Use of underfill is recommended to ensure board level reliability requirements are met if components are mounted on application PCB.

4 Electrical characteristics

Table 3: Electrical characteristics of Mira220

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
Power supplies						
VDD25	Analog and pixel supply voltage		2.4	2.5	2.6	V
VDD18	I/O supply voltage		1.70	1.80	1.90	V
VDD13A	Analog supply voltage		1.25	1.35	1.45	V
VDD13D	Digital supply voltage		1.25	1.35	1.45	V
VDD13P	MIPI, D-PHY and PLL supply voltage		1.25	1.35	1.45	V
I_{VDD25}	Analog and pixel supply current(1)		-	-	168	mA
I_{VDD18}	I/O supply current(1)		-	-	0.6	mA
I_{VDD13A}	Analog supply current(1)		-	-	21	mA
I_{VDD13D}	Digital supply current(1)		-	-	42	mA
I_{VDD13P}	MIPI, D-PHY and PLL supply current(1)		-	-	6	mA
Digital I/O(2)						
V_{IH}	High level input voltage		0.7×VDD18	-	VDD18	V
V_{IL}	Low level input voltage		VSS	-	0.3×VDD18	V
V_{OH}	High level output voltage		0.8×VDD18	-	VDD18	V
V_{OL}	Low level output voltage		VSSIO	-	0.2×VDD18	V
t_{req_exp}	REQ_EXP pulse width(3)		10	-	-	µs
t_{req_frame}	REQ_FRAME pulse width(3)		0.1	-	-	µs
I²C SDA SCL						
V_{IH}			0.7×VDD18	-	VDD18	V
V_{IL}			VSS	-	0.3×VDD18	V
Reference clock						
f_{CLK_IN}	CLK_IN frequency		-	38.4	-	MHz
	CLK_IN accuracy		-	-	±50	ppm
DC_{CLK_IN}	CLK_IN duty cycle		45	50	55	%
$C\text{-}C_{jitter,CLK\_IN}$	CLK_IN cycle-to-cycle jitter		-	-	200	ps
$t_{rise/fall,CLK\_IN}$	Rise and fall transition time		-	10	-	ns

(1) Peak current. See application note AN001031 for current profiles.
(2) The section is not valid for CCI_SDA and CCI_SCL.
(3) See section 8.2.1.

5 Typical operating characteristics

5.1 Electro-optical characteristics

Below are the typical electro-optical specifications of the Mira220, measured in typical conditions.

Table 4: Optical features of Mira220

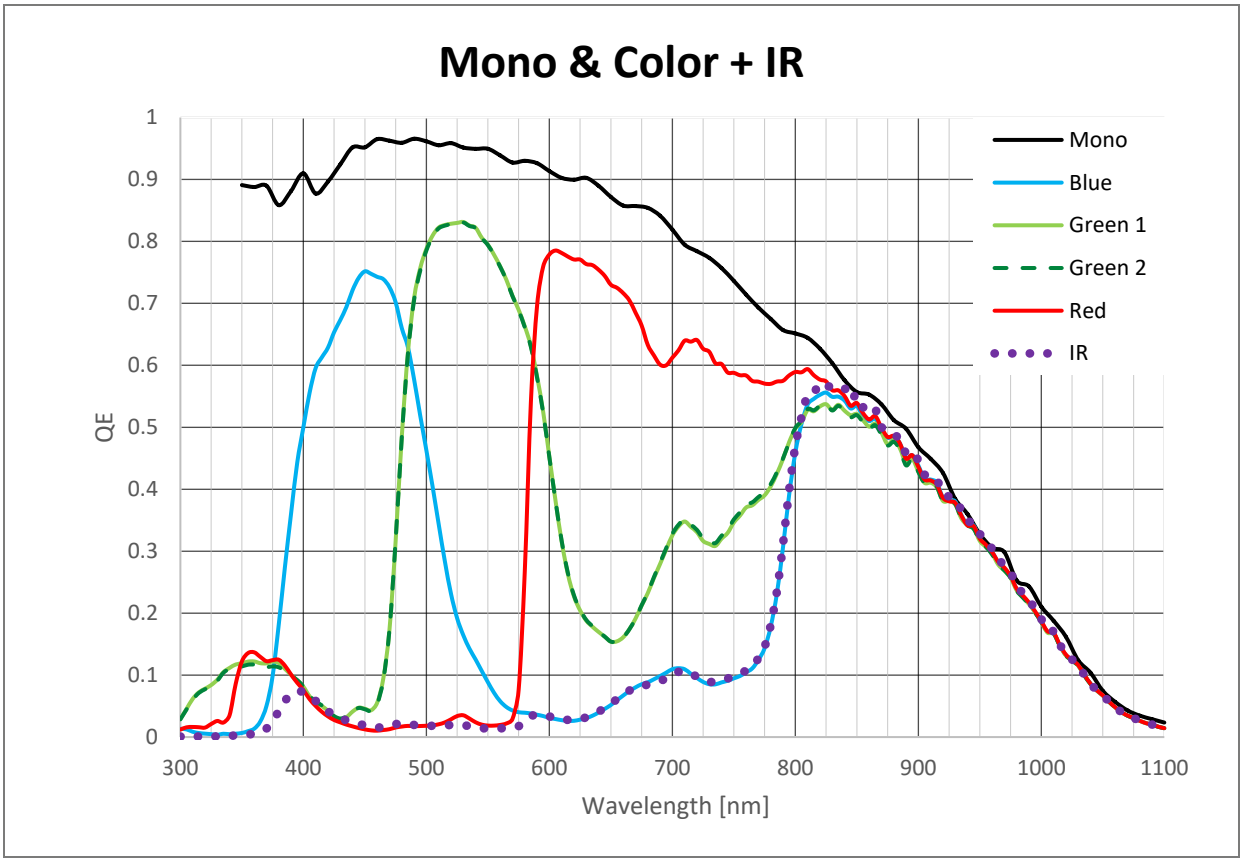
Parameter	Value	Remark
Active pixels	1600 (H) × 1400 (V)	
Pixel pitch	2.79 × 2.79 µm²	
Optical format	1/2.7”	
Pixel type	BSI global shutter	With fixed pattern noise correction and reset (kTC) noise canceling by correlated double sampling (CDS) coupled with high sensitivity.
Shutter type	Pipelined global shutter	Exposure of next image during readout of the previous image.

Table 5: Typical electro-optical characteristics

Parameter	Value	Remark
Full well charge (FWC)	10800 e-	Linear range
Dark temporal noise (DTN)	7.0 e-	
Dynamic range (DR)	63.7 dB	
SNR_{MAX}	40 dB	
Shutter efficiency (1/PLS)	95 dB	940 nm. Higher for visual spectrum.
Dark current (DC)	58 e-/s	60 °C
Color filters	RGB RGB-IR	
Supported lens chief ray angles (CRA)	0° to 30°	Extra wide acceptance angle of the Mira220 pixel means any lens profile with these CRA values would provide decent performance.
Quantum efficiency (QE) mono	95 / 56 / 36 %	550 / 850 / 940 nm
Quantum efficiency (QE) RGB and RGBIR	76 / 85 / 80 / 56 / 36 %	450 / 530 / 605 / 850 / 940 nm

5.2 Spectral characteristics

Figure 1: Quantum efficiency of the Mira220 mono and color



5.3 Functional characteristics

Table 6: Functional characteristics

Parameter	Value	Remark
Region of interests (ROI)	Flexible ROI setting in addition to three preconfigured window sizes 2.2 MP (1600 x 1400) 1.4 MP (1280 x 1120) VGA (640 x 480)	See Section 8.2.3.
Bit depth	12-bit 10-bit 8-bit	See Section 8.4.2.
Timing generation	On-chip	Possibility to control exposure time through external pin.
Programmable registers	Sensor parameters. E.g. Window coordinates, timing parameters, and exposure time.	See Section 8.2, 8.3.3.
Power consumption	168 mW | Active 30fps(1) 40 mW | Idle 4 mW | Sleep	Typical power consumption at full resolution.
Data interface standard	MIPI CSI-2 DPHY	
MIPI outputs	2 Data 1 Clock	Fewer outputs enabled results in a reduced frame rate.
Output interface bit rate	1.5 Gbit/s	Per data channel (maximum)
Frame rates	90 fps	At full resolution and bit depth. Faster rates possible with windowing.
Black sun protection	Yes	
Temperature sensor	Yes	
Context switching	Two register contexts	The system allows on the fly context switching.

(1) External power management is required to achieve this power consumption. See application note AN001027.

6 Functional description

This chapter gives a functional description of the sensor, its architecture, operating modes and readout format.

6.1 Sensor architecture

Mira220 is a high-speed global shutter CMOS image sensor for NIR consumer applications. It is a stacked sensor with optimized silicon layer for pixels (sensor layer) and readout/digital (readout layer). The image array consists of 2.79 µm global shutter pixels and has a resolution of 1600 x 1400 pixels. Figure 2 shows a high-level representation of the Mira220.

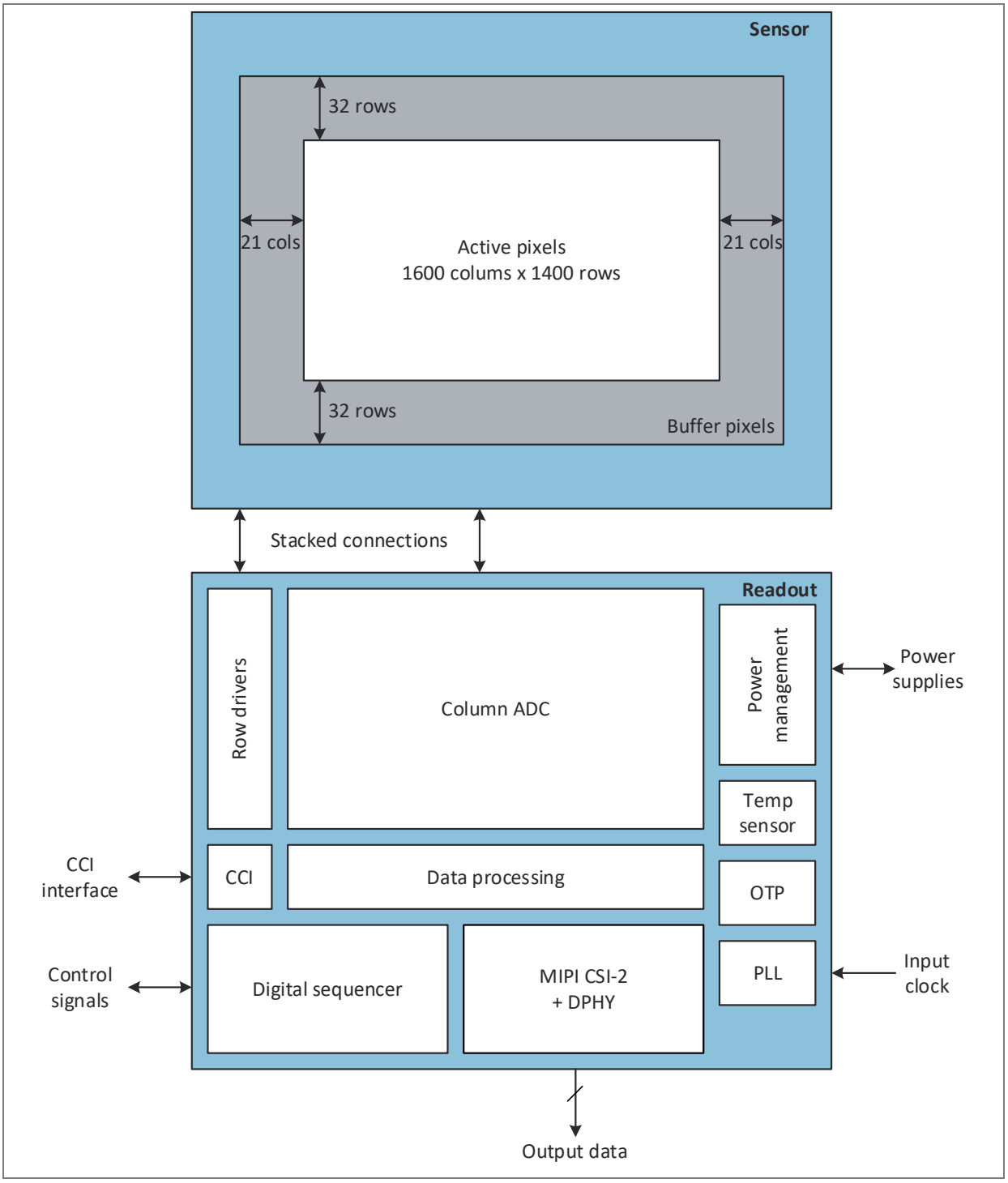
The sensor is compliant with the MIPI CSI-2 v1.3 protocol interface and the D-PHY v1.2 physical layer specifications. It transfers the data over two lanes to the host processor. Changing parameters of the sensor goes through the CCI built-in interface.

A programmable on-chip sequencer generates all internal exposure and readout timings. External triggering and exposure programming is possible.

The on-chip PLL transforms a low-frequency CMOS input clock into all high-frequency clocks needed to operate the sensor.

The sensor has special features to control other components in the system. It has dedicated outgoing signals for system synchronization between the image sensor itself and an external illumination component (i.e. a NIR laser).

Figure 2: Sensor architecture block diagram



6.2 Pixel array

Figure 2 shows the pixel array of Mira220. The resolution of the active pixel array is 1600 (H) x 1400 (V) pixels. However, the physical resolution of the complete pixel array is 1642 (H) x 1464 (V) pixels. Therefore, the pixel array can be split up in two parts: Active pixels and buffer pixels (around the active array). The buffer pixels are not accessible for readout. Micro-lenses are placed on the pixels for improved quantum efficiency.

6.3 Column ADC

The column ADC converts the analog pixel value into a digital value.

6.3.1 Black sun protection

The black sun protection circuit is used to avoid dark spots in the image, caused by high light levels in extremely oversaturated scenes.

6.4 Data processing

The data processing block performs digital operations on the pixel data. It is the complete path from reading the data from the ADC output memories up to the inputs of the MIPI block.

Among the different features, the data processing has implemented the following:

6.4.1 Digital correlated double sampling

The sensor supports digital correlated double sampling DCDS. If enabled the DCDS logic subtracts the value corresponding to reset level of the pixel from the value corresponding to signal level of the pixel in the digital domain. For details, please see section 8.4.3 on how to configure the sensor.

6.4.2 Row noise correction

The row noise generated by common references in the analog readout path is accurately measured on a row-by-row basis. Such noise is dynamically subtracted from all the pixels of the same row in digital domain. This operation results in a row noise value that is smaller than the read noise. Please see section 8.4.4 for information on how to configure the sensor.

6.4.3 Defect pixel detection and correction

The sensor supports the detection of defect pixels using neighboring pixels as reference and applies a correction to that pixel. Please see section 8.4.5 for details on configuration.

6.4.4 Image statistics

The image sensor can output the histogram and number of clipped pixels to reduce the post-processing load on any connected processor. See section 8.5.3.

6.5 CSI-2 data protocol handling & D-PHY communication interface

Data is transmitted off-chip according to the CSI-2 data protocol, as defined by MIPI in document [CSI-2-v1.3]. The physical layer is a D-PHY interface [DPHY-v1.2] with two data lanes and one clock lane.

6.6 Sequencer

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control signals. This sequencer can be activated and programmed through the CCI interface.

Among the different features, the sequencer has implemented the following:

- CCI protocol and register bank management
- Exposure and frame timing generation based on external inputs or internal settings
- Windowing/cropping
- Mirroring and flipping

6.7 CCI interface

The sensor operation must be configured by uploading register settings. These static register values control the behavior of the on-chip sequencer, analog and mixed-signal blocks. To write and read register settings, the CCI (Camera Control Interface) interface is used. This interface is fully compliant with CCI standard (refer to [CSI-2-v1.3]). The CCI consists of two wires, SCL and SDA, carrying the clock and data respectively. The Mira220 image sensor always operates as the CCI slave. See section 7.4.

6.8 PLL

Various clock frequencies are required internally to operate the sensor. These are derived from a single input clock using an on-chip PLL. See also section 7.3.

6.9 Temperature sensor

An on-chip thermal sensor is included in the readout layer. The temperature data can be read out through the CCI interface. See section 8.5.4 for more information on temperature calibration and 8.5.5 with OTP fields storing temperature calibration data.

6.10 OTP memory

A non-volatile, One Time Programmable memory is included on-chip. Part of the memory is used by ams OSRAM to store a unique device ID and sensor calibration data, another part is available to the customer. See section 8.5.5.

6.11 Illumination trigger

The ILLUM_TRIGGER output pin allows synchronizing an external light source to the exposure of the pixel matrix. Please see section 8.5.1 for further details.

6.12 Low power options

Multiple, fully configurable, power modes are available to minimize power consumption when operating and in idle. See sections 7.7 and 8.5.7.

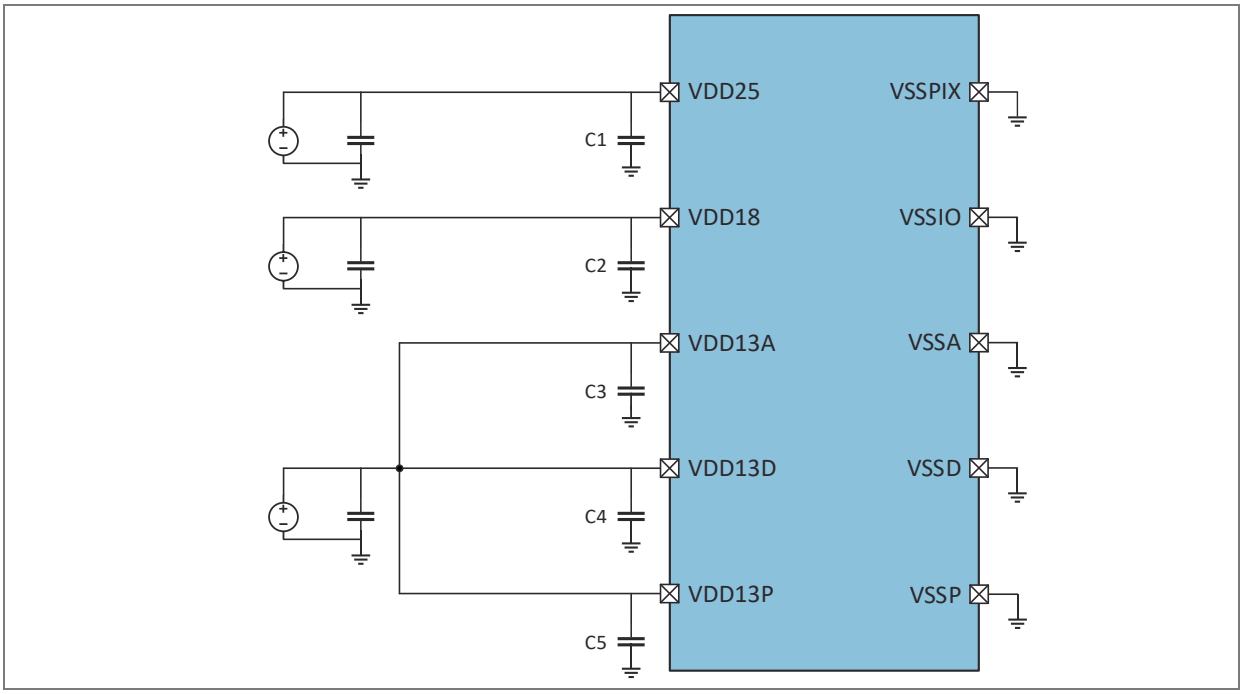
7 Operating the sensor

7.1 Power supplies

7.1.1 External power supplies

To power the sensor, three externally generated supplies are required. It is advisable to use sufficient bulk (at the regulators) and local (at the sensor pins) decoupling for optimal performance. In case of multiple pins for the same supply, local decoupling is needed for each pin. For optimal noise performance, it is advised to keep the analog and digital ground nets separated and connect them together as close as possible to the external supply regulators.

Figure 3: External power supplies



7.1.2 Biasing (On-Chip Regulators)

Operating the pixel and readout layer requires multiple supply levels. These levels can be generated using on-chip regulators. The regulator output voltages are controlled using the CCI interface.

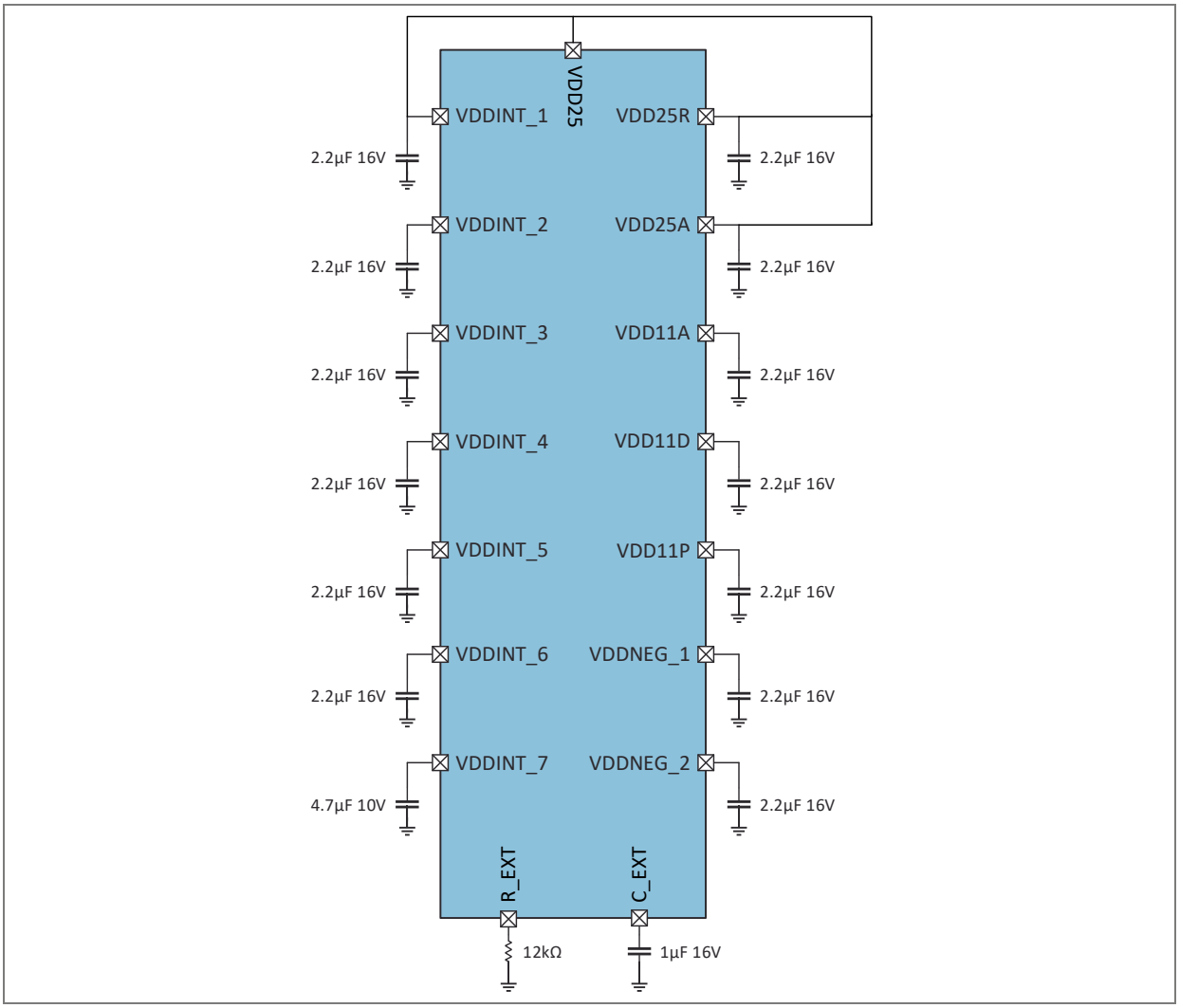
Connections have to be made on PCB level for all supplies. Each net of a supply regulator requires to be decoupled by a capacitor. The capacitor value and minimum voltage rating is shown in Figure 4. It is recommended to use X5R-rated ceramic capacitors to ensure temperature stability. To obtain an accurate bias reference in the sensor, an external bias resistor of 12 kΩ must be placed between R_EXT and ground. It is advised to use a low tolerance (± 0.1%) and low temperature coefficient (100 ppm/°C or better) resistor.

Figure 4 shows the voltage regulator and the bias connections.

Attention:

The external supply VDD25 is connected to VDD25A, VDD25R and VDDINT_1. Hence, the internally generated voltages are bypassed. Step 7 in the power-up sequence disables these internal voltages.

Figure 4: Regulator decoupling and biasing



7.2 Power-up/down sequence

A specific order and timing must be applied to the sensor supplies to guarantee a proper power-up/power-down sequence and to avoid peak currents. Figure 5 shows the power-up sequence. The power-down sequence is the inverse of the power-up sequence and is shown in Figure 6.

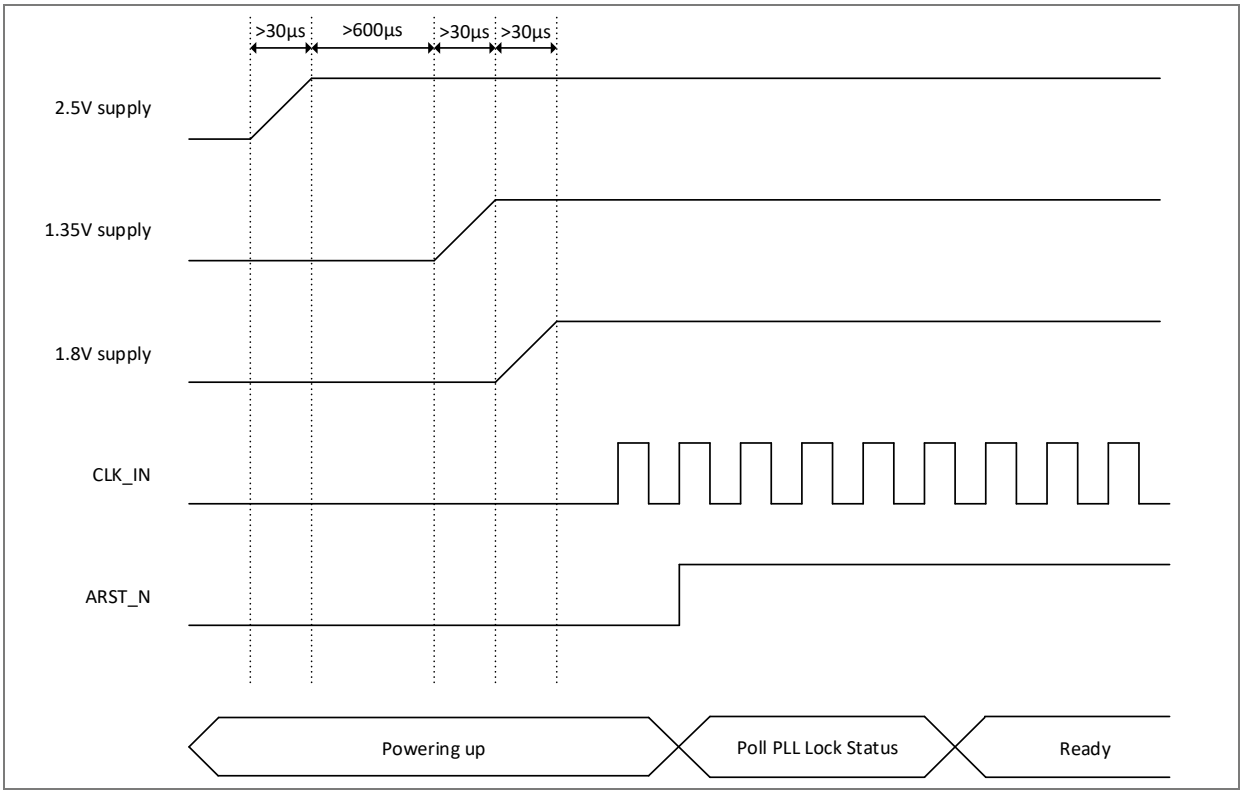
7.2.1 Power-up sequence

1. Apply 2.5 V power supply (VDD25). Supply ramp up should be greater than 30 µs. Allow the bandgap reference to settle (i.e. at least 600 µs).
2. Apply 1.35 V power supply (VDD13A, VDD13D and VDD13P). Supply ramp up time should be greater than 30 µs. Allow the supply to finish ramping up.
3. Apply 1.8 V power supply (VDD18). Supply ramp up time should be greater than 30 µs. Allow the supply to finish ramping up.
4. Apply the external clock on the CLK_IN clock input pin.
5. Release the hard reset signal on the ARST_N input pin. I²C communication is now available.
6. Wait for the PLL to lock. Check the lock bit in the read-only register **PLL_STATUS** through I²C read to verify that the PLL has locked.
7. Disable three internal LDOs by writing via I²C the value 0x02 to address 0x401E and the value 0x3B to address 0x4038.
8. Restore the LDO and gain calibration values stored in OTP, see section 8.5.5 and application note AN001030.
9. The sensor is now in its default state. The sensor can now be configured for image capture and pixel data output through CCI uploads.

Attention:

During startup, there is a min. startup current requirement of 350 mA on the VDD25 pin in the time between the 2.5 V supply ramp up and 1.35 V supply ramp up. An alternative startup sequence is possible if this current requirement cannot be met. More details on this alternative sequence can be seen in datasheet DS000642.

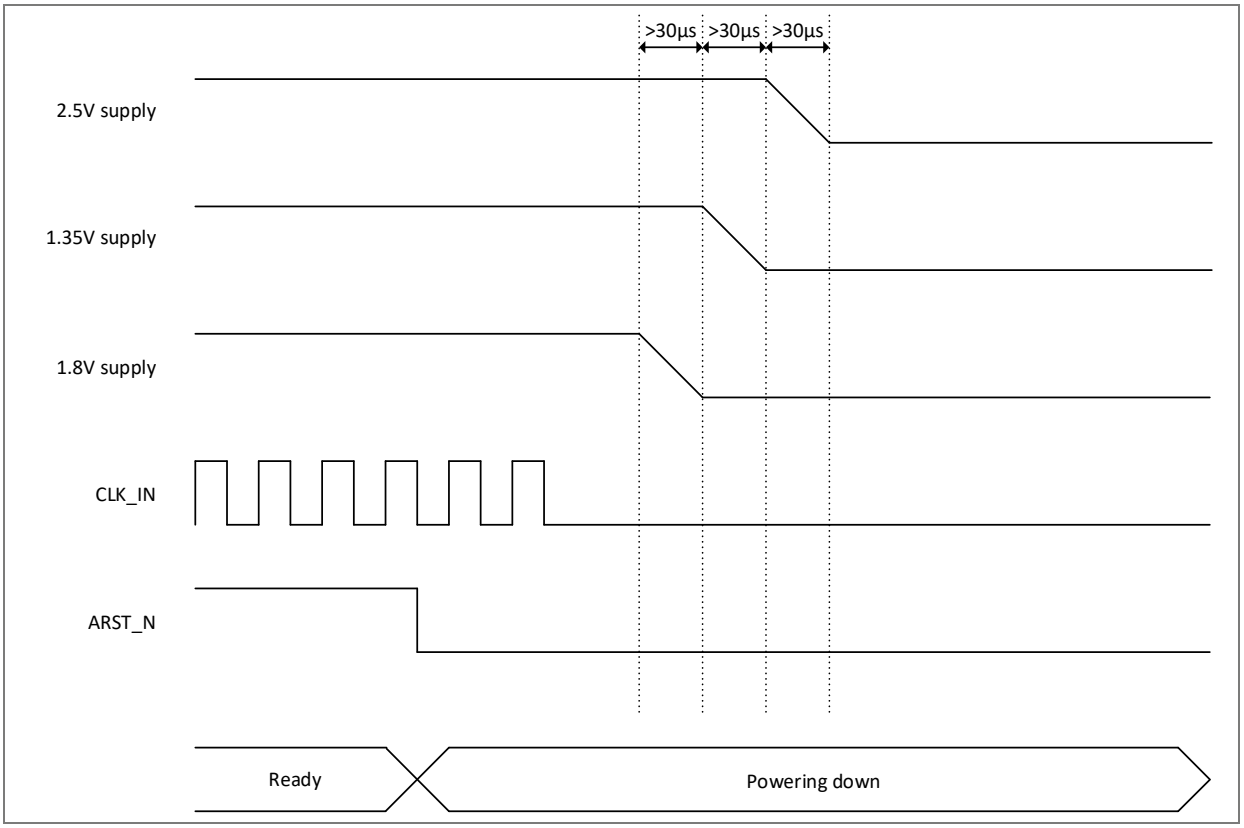
Figure 5: Power-up sequence



7.2.2 Power-down sequence

1. Stop all image capture processes.
2. Assert the hard reset signal on the ARST_N input pin.
3. The external clock can now be disabled on the CLK_IN input pin.
4. Disable 1.8 V power supply (VDD18). The supply ramp down should be greater than 30 µs.
5. Disable 1.35 V power supply (VDD13A, VDD13D and VDD13P). The supply ramp down should be greater than 30 µs.
6. Disable 2.5 V power supply (VDD25). The supply ramp down should be greater than 30 µs.

Figure 6: Power-down sequence



7.3 PLL and clocking

The sensor has two CMOS clock inputs: CCI_SCL and CLK_IN. CCI_SCL is part of the CCI used to configure the sensor. All other internal sensor clocks are derived from the PLL, taking CLK_IN as input clock.

Refer to section 4 for the electrical specifications of the input clocks.

Table 7: PLL registers

Register	Address	Position	Description
PLL_STATUS	0x50DC	[0]	Flag indicating PLL lock status
		[1]	Flag indicating reference clock missing
PLL_LOCK_CNT_RST	0x5013	[0]	1: Resets the PLL lock count
PLL_LOCK_RISE_CNT	0x5015	[7:0]	Number of PLL lock rising edges
PLL_LOCK_FALL_CNT	0x5016	[7:0]	Number of PLL lock falling edges

7.4 CCI and register access

7.4.1 CCI interface

The sensor operation is configured by uploading register settings. These static register values control the behavior of the sequencer on the chip, but also of all the analog and mixed-signal blocks. To write and read register settings the CCI (Camera Control Interface) interface is used. A CCI interface is derived from the I²C interface specification [I2C-v6]. It supports a subset of commands using 16-bit sub-addresses. The sensor supports both Standard Mode (100 kbit/s) and Fast Mode (400 kbit/s).

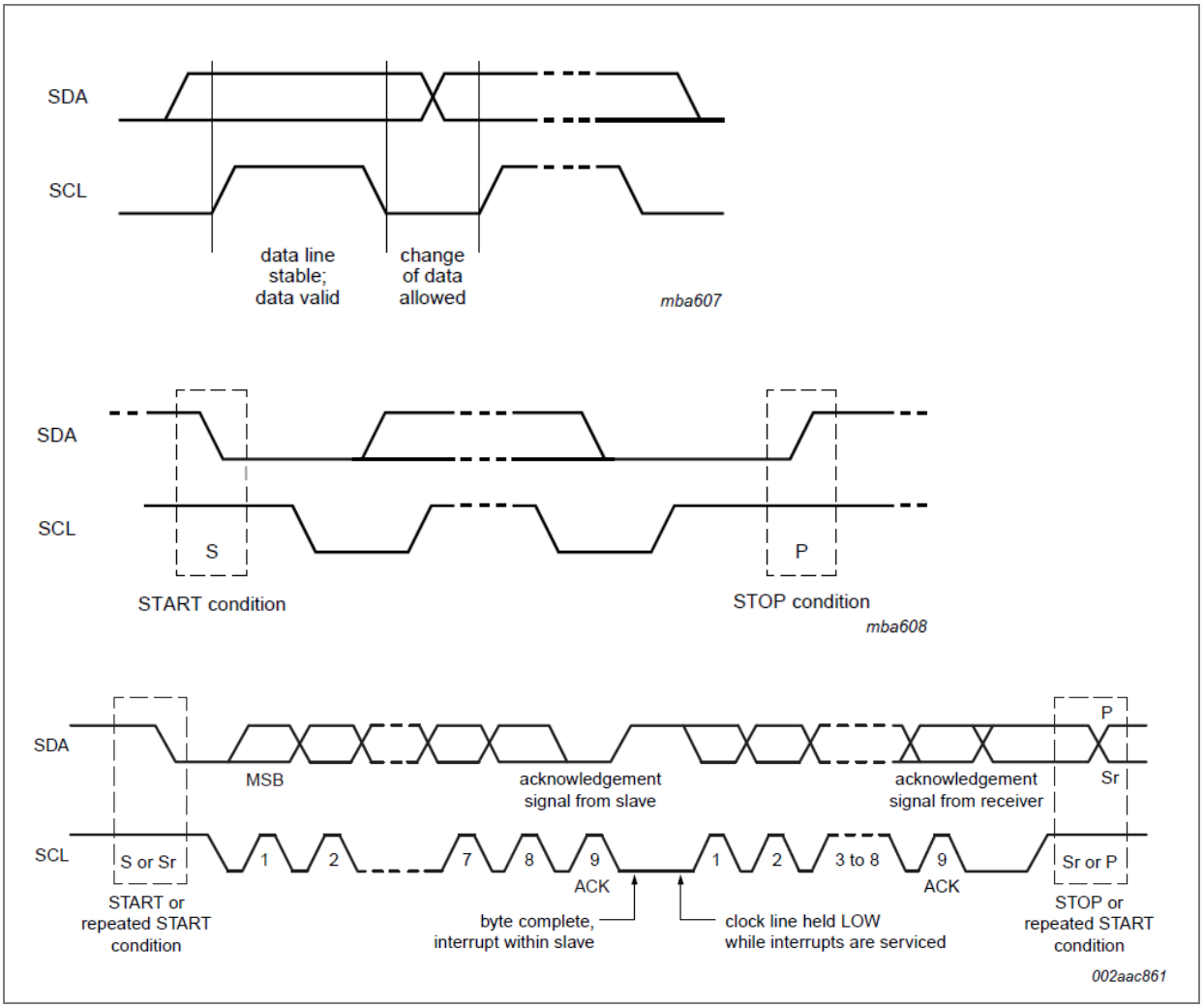
Each register contains an 8-bit word. If a register is not fully defined (e.g. a 6-bit register occupying an 8-bit word space), undefined bits are not writable (writing to them does not return an error but has no effect) and return ‘0’ when read back.

The sensor supports both single read/write and burst read/write.

The CCI has been defined according to the MIPI CSI-2 specification. For more information and electrical specifications, see document [CSI-2-v1.3].

Different conditions on the CCI interface lines are explained in Figure 7. The figures are taken from [I2C-v6] and are given here only as reference.

Figure 7: CCI interface conditions

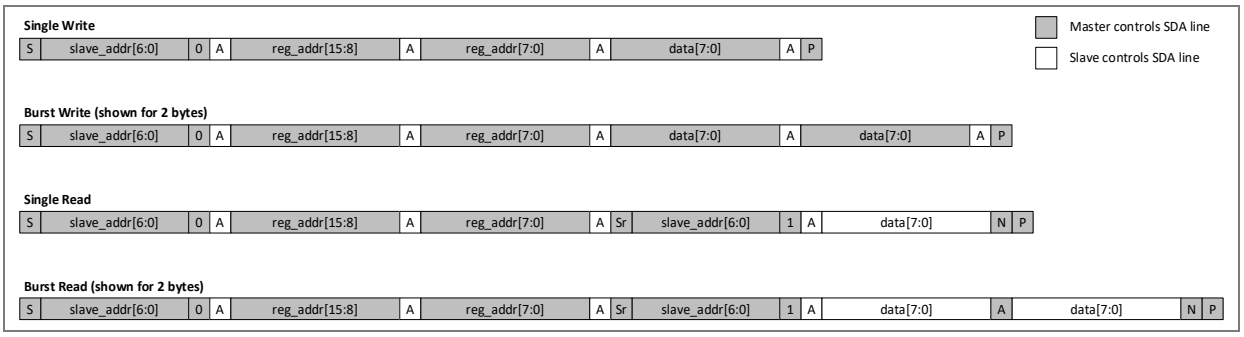


- S = Start Condition, Sr = Repeated Start Condition
  The master pulls the SDA line low, while SCL stays high, indicating it is ready to send data.
- A = Acknowledge (ACK), N = Not Acknowledge (NACK)A (N)ACK status is signaled by either a master or a slave device, depending on the scenario:
  – The master will check the (N)ACK after sending the slave address or register address. The master releases the SDA line and checks whether the slave pulls it low (ACK) or not (NACK). In case of a NACK, the SDA line will be high due to the pull-up.
  – The slave will check the (N)ACK after sending read-back register data to the master. The slave releases the SDA line and checks whether the master pulls it low (ACK) or not (NACK). In case of a NACK, the SDA line will be high due to the pull-up.

  - Note that a NACK is used to terminate all read transactions and is expected. For write transactions, a NACK is the result of a possible issue or miscommunication with the slave device (wrong slave address, not powered on …).
- P = Stop Condition
  The master releases the SDA line, while SCL stays high, meaning no more byte transfer will take place in this access.
- R/W bit: The bit after the slave address. ‘0’ indicates a write, ‘1’ indicates a read.

Figure 8 shows the different CCI write and read transactions to or from device slave_addr and register reg_addr. The master to slave direction is shaded. In case of a burst transaction, the reg_addr is automatically incremented after every ACK.

Figure 8: CCI transaction command format



7.4.2 CCI slave address

Every CCI slave has a unique 7-bit device address. The slave address of Mira220 is defined by the level on CCI_ADDR1 and CCI_ADDR0 input pins. This allows connecting up to four Mira220 sensors on a single CCI bus.

It is also possible to execute a global write to all Mira220 sensors on the CCI bus.

The 7-bit slave addresses are given in the table below with X_1 the level on pin CCI_ADDR1 and X_0 the level on pin CCI_ADDR0.

Table 8: CCI slave address

Action	Slave address (7-bit) + R/W bit
Local write	10101$X_1X_0$0
Local read	10101$X_1X_0$1
Global write	10100010
Global read	Not allowed

7.5 Reset

The sensor has an asynchronous reset input pin (ARST_N) and an asynchronous reset register (**CMD_SOFT_RESET**).

When combined, they have the following function:

1. **ARST_N:** Reset the entire sensor when low (active-low). This is considered a hard reset.
2. **CMD_SOFT_RESET:** Reset the entire sensor, except the CCI interface and register bank when high. This is considered a soft reset.

As long as RST_N is high, all registers retain their value when **CMD_SOFT_RESET** is high. The soft reset register is self-clearing.

Table 9: Reset configuration register

Register	Address	Position	Description
CMD_SOFT_RESET	0x0040	[0]	Software reset

7.6 Controlling exposure and readout

This section explains the important concepts of the frame-timing model.

7.6.1 Basic frame timing

During operation, the sensor can be in any of the following states:

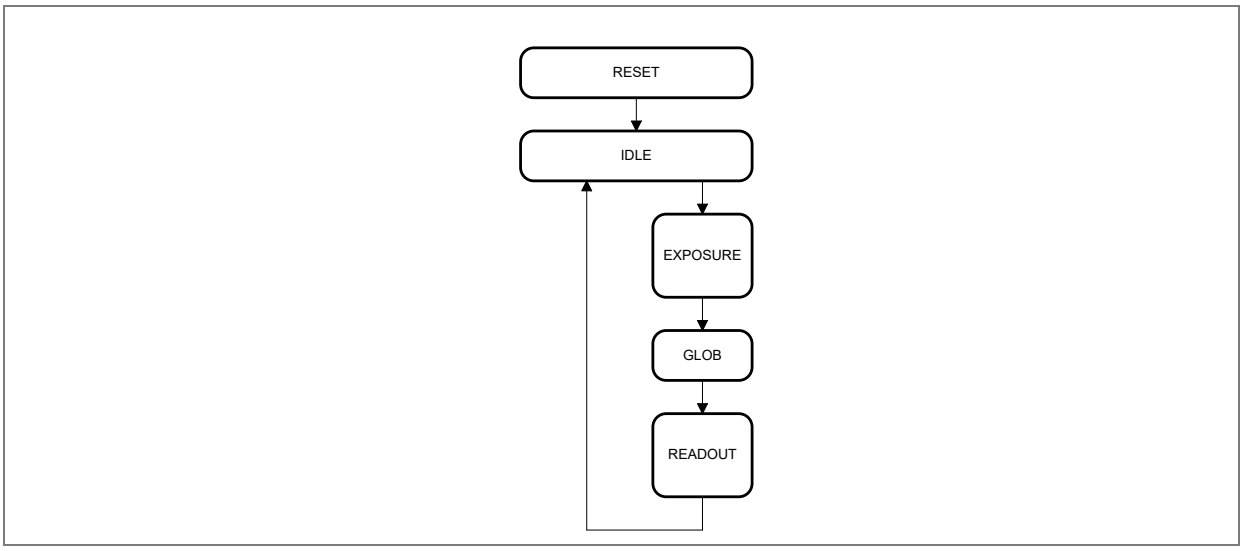
- **RESET**: Asynchronous sensor reset is low, disabling the sensor entirely.
- **IDLE**: Sensor performs no function as it awaits external requests.
- **EXPOSURE**: Light is being integrated in the pixels.
- **GLOB**: Closing global shutter by sampling all integrated pixel values.
- **READOUT**: Reading out the acquired frame plus metadata and mandatory overhead.

A distinction can be made between two basic frame timing operations (sequential and pipelined operation), as detailed in the following two sections.

7.6.2 Sequential operation

In sequential operation, the sensor goes through a sequential succession of EXPOSURE – GLOB – READOUT to grab a single image, as indicated in the figure below. When such a cycle is completed, the sensor is back in the IDLE state waiting for a new internal or external trigger.

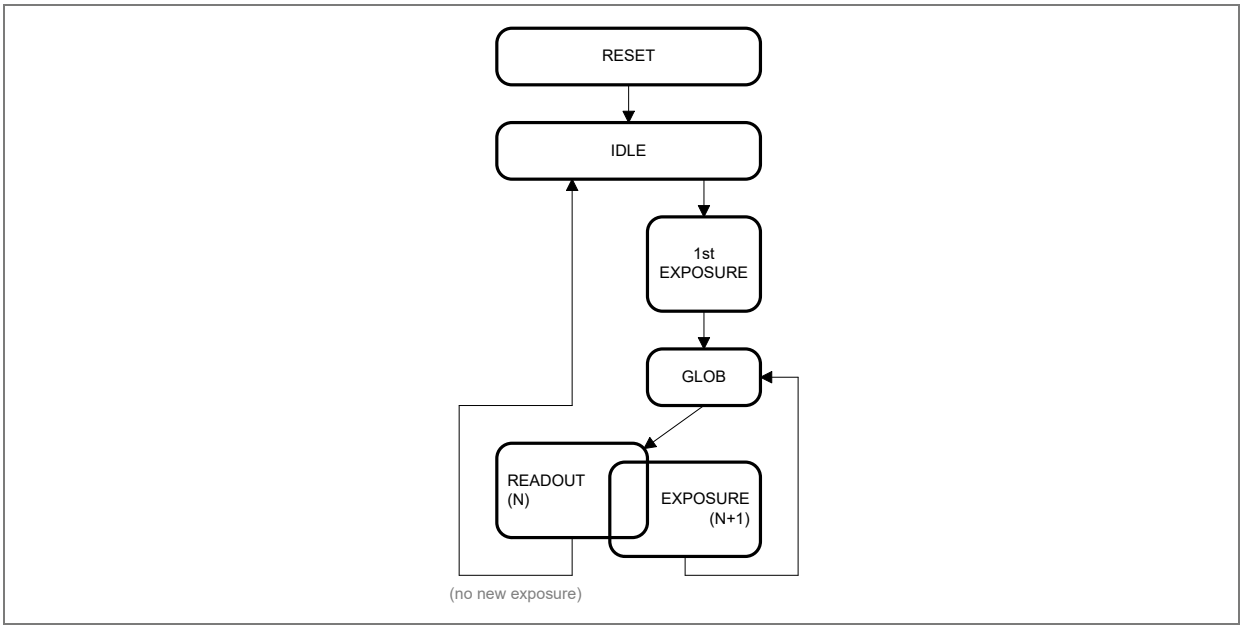
Figure 9: State chart – sequential operation



7.6.3 Pipelined operation

The main property of pipelined operation is that the sensor can be in the EXPOSURE state and READOUT state at the same time. This basically means that the readout of frame N can be busy while the EXPOSURE state of frame N+1 has already started. The EXPOSURE can fully or partially overlap with a READOUT state.

Figure 10: State chart – pipelined operation



When exiting IDLE state, the first EXPOSURE period starts. As in the sequential operation, this flows into a GLOB state, which in its turn starts the READOUT of a frame. Depending on the sensor control or configuration (see section 7.7 for details and options), a new EXPOSURE may start when the readout is still busy.

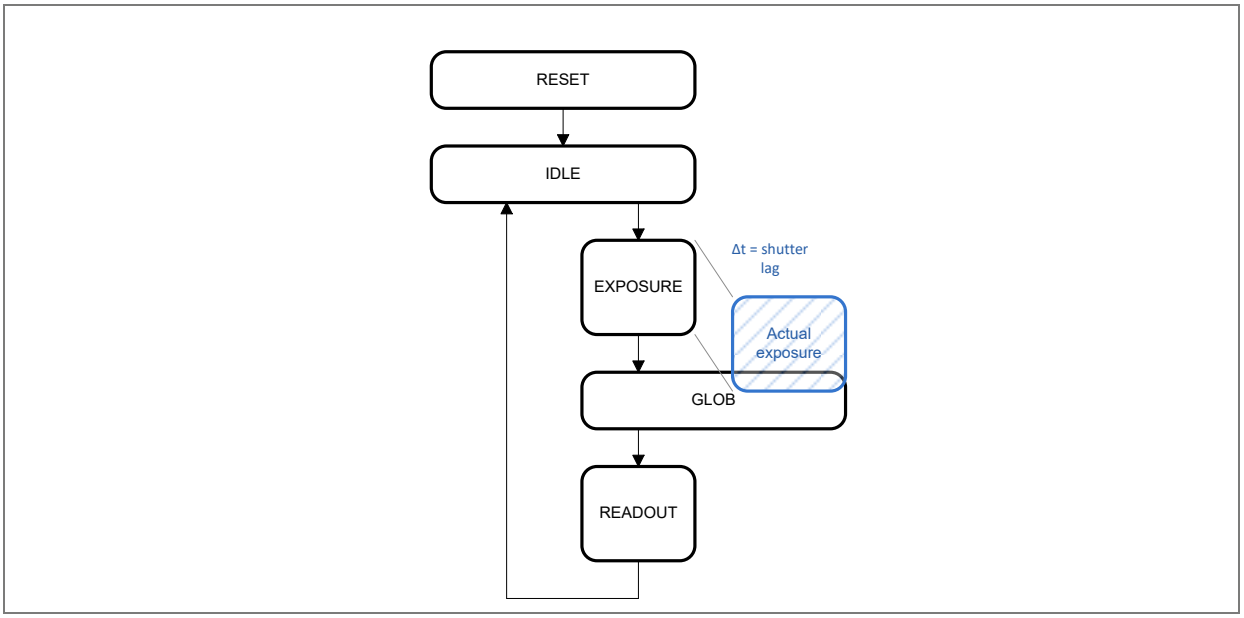
At the end of the READOUT period, there are two options:

- **No new EXPOSURE was started.** The sensor will return to IDLE.
- **A new EXPOSURE has started.** The sensor will wait until this new EXPOSURE finishes, before moving back to GLOB, which will always trigger a new READOUT.

7.6.4 Shutter lag

The shutter lag is the delay between the start and end of the **EXPOSURE state** and the start and end of the **actual exposure**. The actual exposure is the time where the sensor is actually capturing and integrating light. Figure 11 illustrates the shutter lag.

Figure 11: State chart – sequential operation with shutter lag



The distinction is important because the EXPOSURE state is the direct response of external control (through sensor I/O request or register settings), but it is the actual exposure that really matters to the user.

In the remainder of the document, when the concept of exposure or exposure time is mentioned, it will always be about the **EXPOSURE state**, unless stated otherwise. The reader should always bear in mind that the **actual exposure** is delayed with respect to this EXPOSURE state due to the shutter lag mechanism. The shutter lag is always present at the end of the EXPOSURE period, since part of the actual exposure time will always extend into the GLOB state. This is sometimes called “exposure overlap”.

Figure 11 shows the shutter lag under sequential operating conditions only, but note that the shutter lag is present in all operation modes. The shutter lag at the start of the exposure is 2.015 µs (rising edge exposure – actual start) and the shutter lag at the end of exposure is 20.11 µs (falling edge exposure – actual end). As a result, the length of the actual exposure time is larger than the length of the EXPOSURE state (the exposure overlap is added).

7.7 Sensor control modes

Stepping through the state charts in Figure 9 and Figure 10 can be externally controlled with the sensor inputs REQ_EXP and REQ_FRAME and with register settings (which will be detailed in further sections). This can be done in two different modes: Master mode or slave mode.

- Master Exposure Control Mode - Sensor controls its own timing.
- Slave Exposure Control Mode - Timing is controlled by an external component.

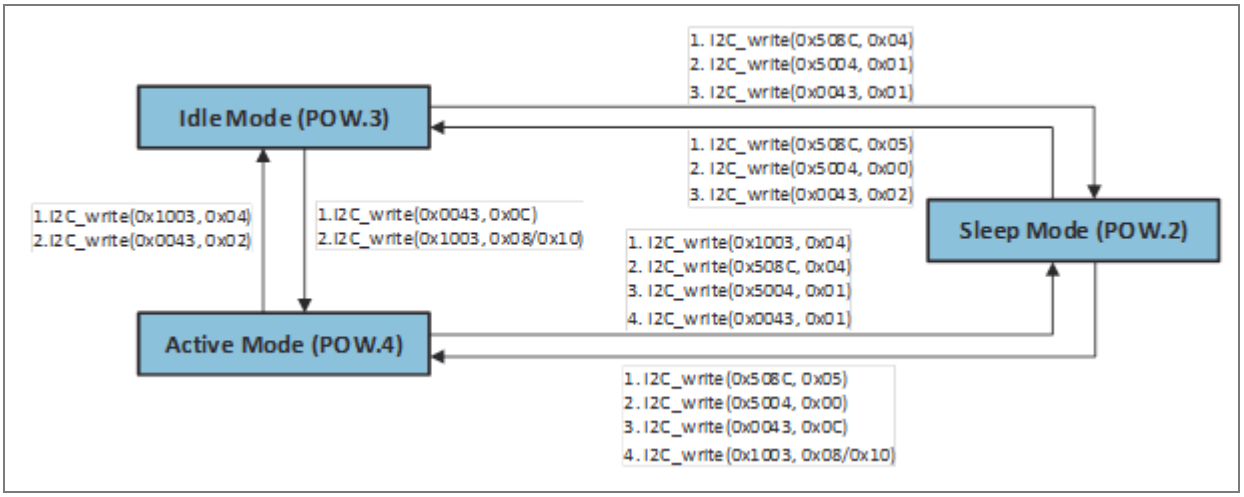
Register **IMAGER_STATE** can be used to stop any active sensor operation and return the sensor to the IDLE state, waiting for new requests. This register is a good way to get the sensor out of streaming mode without asserting any reset.

Table 10: Exposure control and readout configuration registers

Register	Address	Position	Description
IMAGER_STATE	0x1003	[5:0]	0x02: Stop at row boundary (internal counters are stopped and FSM switches to IDLE state) 0x04: Stop at frame boundary 0x08: Slave exposure control mode 0x10: Master exposure control mode 0x3F: Force imaging FSM to IDLE state
POWER_MODE	0x0043	[0]	Sleep power mode enable
		[1]	Idle power mode enable
		[2]	System clock enable
		[3]	SRAM clock enable

The idle power mode disables certain blocks, holds all settings in the sequencer and keeps the MIPI interface activated. While the sleep power mode also disables the PLL and MIPI.
Figure 12 shows how to switch between the several power modes.

Figure 12: Power mode switch



7.7.1 Master mode

In Master Exposure Control Mode, the frame and exposure timings of the sensor are pre-programmed into the sensor. The sensor runs autonomously after the start trigger based on these programmed settings. The sensor can grab a fixed amount of frames or take images continuously. No input pins are used in this mode. See section 8.2 for details on the exposure time and frame time registers.

Master Exposure Control Mode can perform sequential readout, in which a complete expose-sample-readout cycle is finished before the next one is started, and can perform pipelined readout, in which readout is done while the next frame is being captured by the pixel array (exposure).

Figure 13: Master exposure control mode

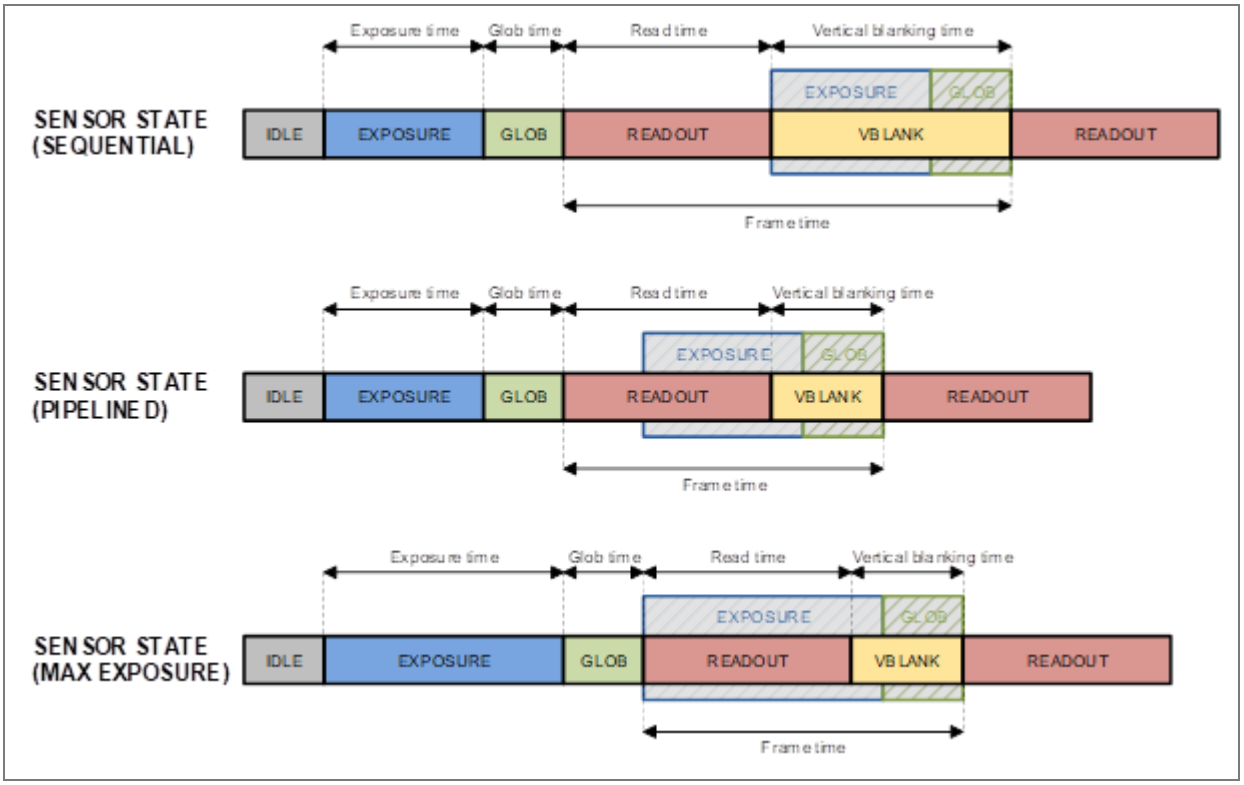


Table 11: Master mode configuration registers

Register		Address	Position	Description
IMAGER_RUN		0x10F0	[0]	Start the image acquisition (self-clearing)(1)
IMAGER_RUN_CONT		0x1002	[2]	Enable continuous running, not limited to number of frames
NB_OF_FRAMES(2)	[7:0]	0x10F2	[7:0]	Number of frames to capture
	[15:8]	0x10F3	[7:0]	

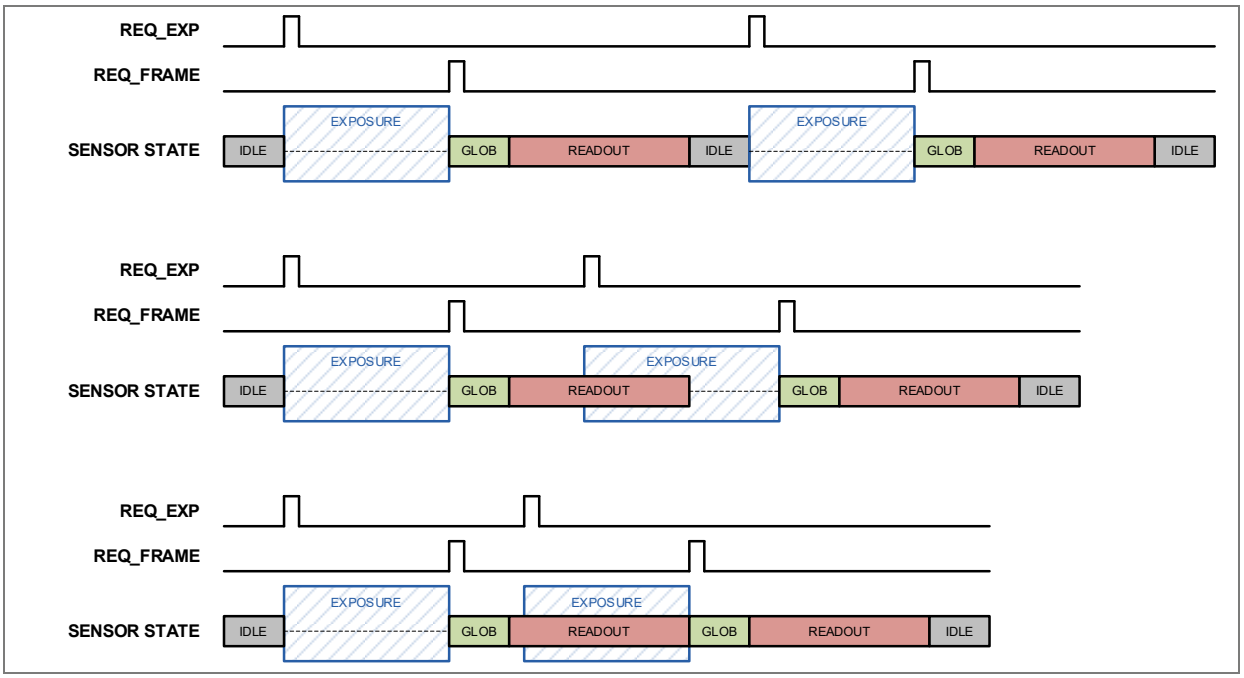
(1) Stop the acquisition with IMAGER_STATE. After NB_OF_FRAMES, the sensor will also go to the IDLE state.
(2) Only in Sequential Readout Operation. Parameter ignored in Pipelined Readout Operation.

7.7.2 Slave mode

In Slave Exposure Control Mode, the frame and exposure timings of the sensor are being completely controlled from the outside. Slave Exposure Control Mode can perform sequential readout, in which a complete expose-sample-readout cycle is finished before the next one is started, and can perform pipelined readout, in which readout is done while the next frame is being captured by the pixel array (exposure).

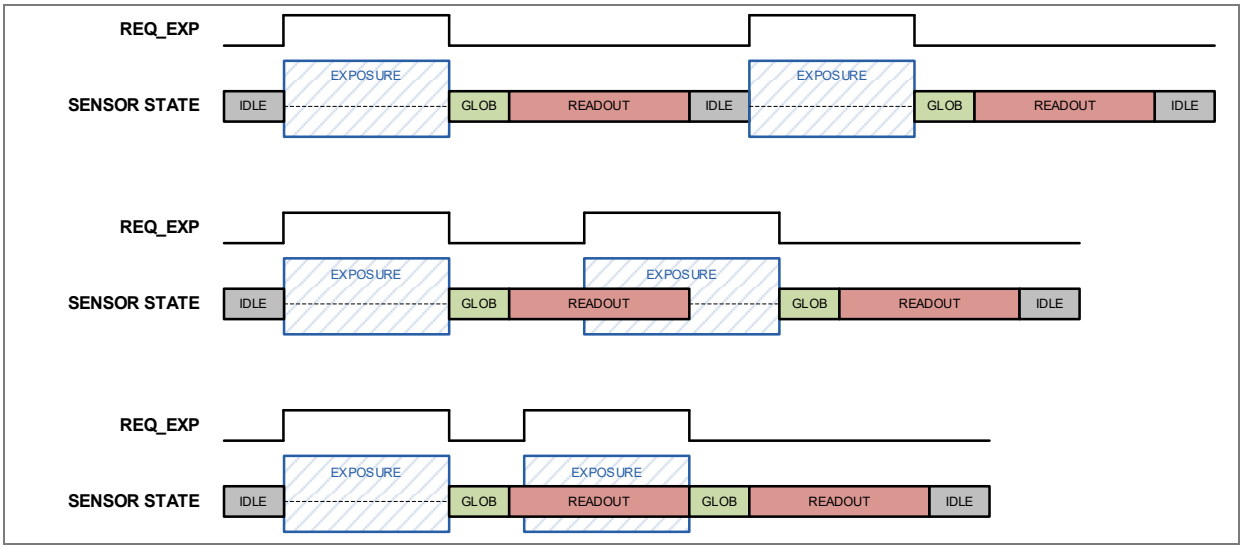
In Slave Exposure Control Mode, two methods of operation are possible: Exposure and readout are controlled by two separate pins or by a single pin. This last method will be referred to as ‘single pin exposure’. When using two pins, a rising edge on the REQ_EXP pin triggers exposure, while a rising edge on the REQ_FRAME pin triggers the readout.

Figure 14: Two pins slave exposure



In single pin exposure, a rising edge on the REQ_EXP pin triggers exposure, while a falling edge on the REQ_EXP pin triggers the readout.

Figure 15: Single pin slave exposure



The following registers configure the slave mode.

Table 12: Slave mode configuration register

Register	Address	Position	Description
EXT_EVENT_SEL	0x1001	[6]	0: REQ_EXP starts readout (single pin exposure) 1: REQ_FRAME starts readout
CMD_REQ_EXP	0x0041	[0]	Same function as REQ_EXP pin
CMD_REQ_FRAME	0x0042	[0]	Same function as REQ_FRAME pin

The register bits **CMD_REQ_EXP** and **CMD_REQ_FRAME** are equivalent to their sensor pin counterparts REQ_EXP and REQ_FRAME. The sensor REQ_EXP and REQ_FRAME pins can therefore be tied low to use the register uploads for frame timing control. By using these registers together with **CMD_SOFT_RESET**, the sensor can in theory be controlled with just the CCI interface plus 2 timing inputs (ARST_N and CLK_IN) at the cost of a slightly reduced timing accuracy (because the registers are loaded via the CCI interface).

7.8 IO drive strength

All digital IO and CCI interface pins have a programmable drive strength.

Table 13: Sensor I/O drive strength

Register	Address	Position	Description
DRIVE_STRENGTH	0x0012	[1:0]	0x0: 2 mA drive strength digital output. 0x1: 4 mA drive strength digital output. 0x2: 8 mA drive strength digital output. 0x3: 12 mA drive strength digital output.
		[2]	0x0: 4 mA sink current CCI interface. 0x1: 20 mA sink current CCI interface.

8 Configuring the sensor

8.1 Operation modes

The sensor supports different operation modes, listed per category in Table 14 allowing for a large number of possible combinations.

Table 14: Operation modes

Mode	Description
Power modes	
POW.1	Hard reset mode
POW.2	Sleep mode
POW.3	Idle mode
POW.4	Active mode
Data multiplexing modes	
MUX.1	Single data lane MIPI
MUX.2	Two data lanes MIPI
Sensor control modes	
SEN.1	Master exposure control mode
SEN.2	Slave exposure control mode
Image modes	Preconfigured ROI modes. Custom ROIs supported. See 8.2.3.
IMG.1	Full ROI; 1600 (H) x 1400 (V)
IMG.2	1.4 MP resolution (central ROI; 1280 (H) x 1120 (V))
IMG.3	VGA resolution (central ROI; 640 (H) x 480 (V))
Bit depth	
ADC.1	12-bit A/D conversion
ADC.2	10-bit A/D conversion
ADC.3	8-bit A/D conversion
Frame rate	Maximum frame rate is dependent on ROI selection
SPEED.1	Max fps 90 fps IMG.1 || 110 fps IMG.2 || 255 fps IMG.3
SPEED.2	60 fps
SPEED.3	30 fps
SPEED.4	15 fps

Information:

The information in the section above needs to be aligned with the sensor configuration as provided in the common upload file. Make sure to check the latest version of the common upload file on the ams OSRAM product page under Tools & Resources or ask the FAE.

8.2 Configuring readout and exposure

8.2.1 Frame time and exposure time

The frame time T_{frame} is defined as (the frame rate is the inverse of T_{frame}):

Equation 1:

Slave exposure mode

$$T_{frame} > t_{GLOB} + T_{CLK\_IN} * ROW\_LENGTH * VSIZE$$

Master exposure mode

$$T_{frame} = T_{CLK\_IN} * ROW\_LENGTH * (VSIZE + VBLANK)$$

With,

t_{GLOB}	: Glob time is 1928 × T_{CLK_IN}
T_{CLK_IN}	: Period of reference clock CLK_IN
ROW_LENGTH	: Row length (see section 8.2.2)
$SIZE$	: Numbers of rows in window (see section 8.2.3)
$VBLANK$	: Number of blanking rows

In Slave Exposure Mode, the frame rate is controlled by the external pin REQ_EXP. The minimum pulse period is the lower limit of T_{frame}.

In Master Exposure Mode, the frame rate can easily be adjusted with the **VBLANK** parameter. The operation mode is always pipelined except if you make **VBLANK** long enough to have a sequential operation. Equation 2 shows the minimal **VBLANK**, exposure time and the maximal exposure time in Master Exposure Mode.

Equation 2:

$$VBLANK_{min} = \left\lceil \frac{t_{GLOB}}{T_{CLK\_IN} * ROW\_LENGTH} \right\rceil + 11$$

$$t_{EXP} = EXP\_TIME * T_{CLK\_IN} * ROW\_LENGTH$$

$$t_{EXP,max} = T_{frame} - t_{GLOB}$$

Table 15: Frame time configuration registers

Register		Address	Position	Description
EXP_TIME	[7:0]	0x100C	[7:0]	Exposure time in row lengths.
	[15:8]	0x100D	[7:0]	
VBLANK	[7:0]	0x1012	[7:0]	Vertical blanking in row lengths.
	[15:8]	0x1013	[7:0]	
EXT_EXP_PW_SEL		0x1001	[0]	0: Length of exposure with external pulse width 1: Length of exposure with EXP_TIME register
EXT_EXP_DELAY	[7:0]	0x10D0	[7:0]	Sets the delay between request for exposure and actual exposure in row lengths in slave mode (see section 7.6.4).
	[15:8]	0x10D1	[7:0]	

Figure 16: Delay between REQ_EXP and actual exposure in single pin slave exposure mode including shutter lag

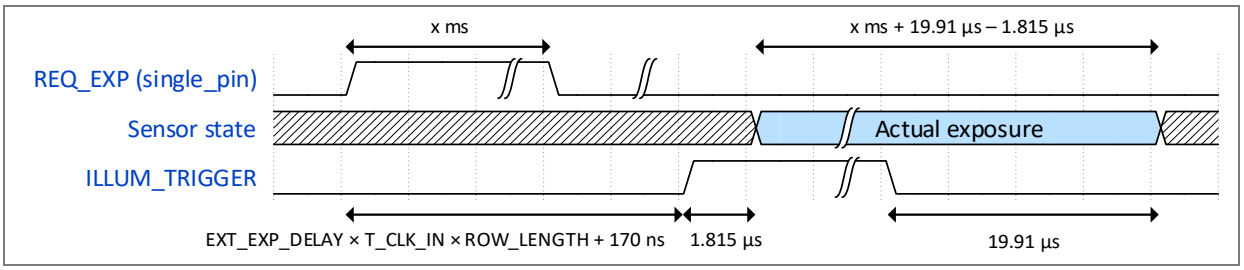


Table 16: Pre-defined frame rate configurations with minimum ROW_LENGTH of 304

ROI resolution	Frame rate	VBLANK[15:0]
2.24 MP	90	0x0016
	60	0x02DD
	30	0x0B32
	15	0x1BDD
1.4 MP	110	0x002B
	60	0x03F5
	30	0x0C4A
	15	0x1CF5
VGA	255	0x0015
	60	0x0675
	30	0x0ECA
	15	0x1F75

Information:

It is not possible to increase the frame rate by reducing ROI horizontal dimension (amount of columns).

8.2.2 Row length

Table 17: Row length configuration registers

Register		Address	Position	Description
ROW_LENGTH	[7:0]	0x102B	[7:0]	Sets the duration of the row length in clock cycles of CLK_IN.
	[15:8]	0x102C	[7:0]	

The row length defines the line rate of the sensor. It is programmed in number of CLK_IN cycles with the **ROW_LENGTH** register. Changing this value has an impact on all settings that are expressed in row lengths, for example: exposure time, blanking time, readout speed, illumination trigger, etc.

The row length has a minimum value because a number of processes in the sensor need to be completed within one row length. The minimum row length is 304 when both D-PHY lanes are running at 1.5 Gbit/s per lane. The maximal row length value is only limited by the size of the 16-bit register.

When the sensor is configured to use only one D-PHY lane then the row length should be doubled. In addition, the row length should be changed when a slower D-PHY data rate is preferred, see section 8.3.4.

8.2.3 Region of interest (Windowing or Cropping)

The windowing function is available in both vertical and horizontal directions. The only limitation in horizontal direction is that the window is around the centerline of the active pixel array. See Figure 18 for a graphical explanation. See also section 8.5.7 for power saving options in reduced Region of Interest (ROI).

Up to three vertical regions can be defined as shown in Figure 19. All regions must have the same width and should not overlap. The different regions are streamed out as a single image.

Figure 17: Windowing example

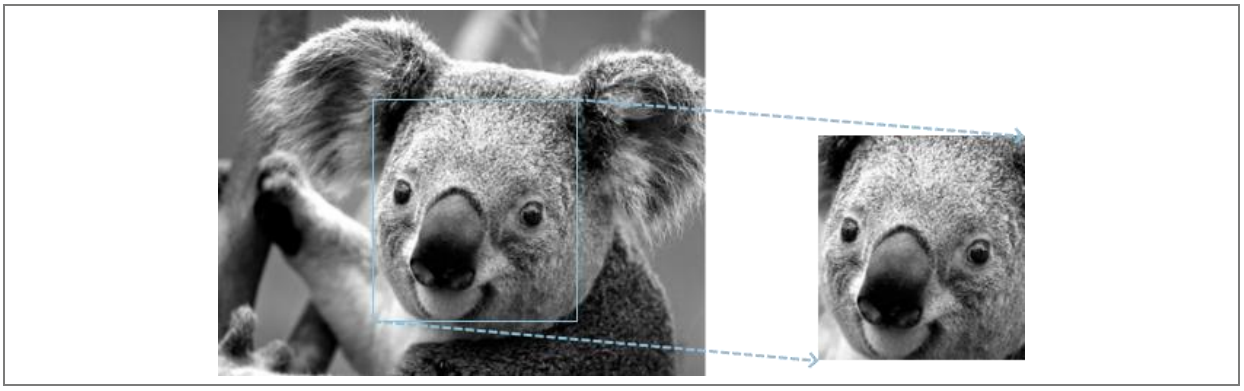


Figure 18: Windowing configuration parameters (Single ROI)

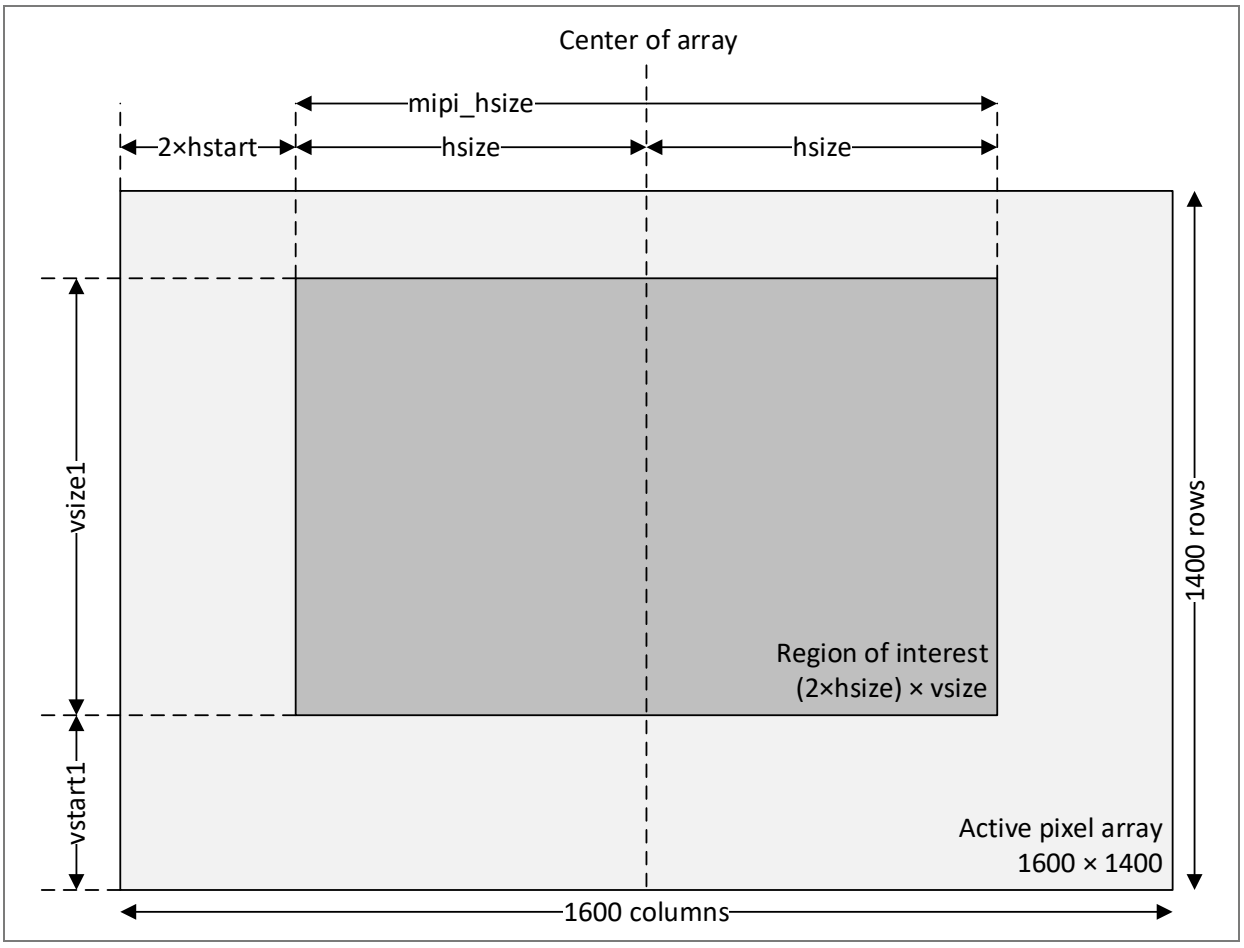


Figure 19: Windowing configuration parameters (Multi ROI)

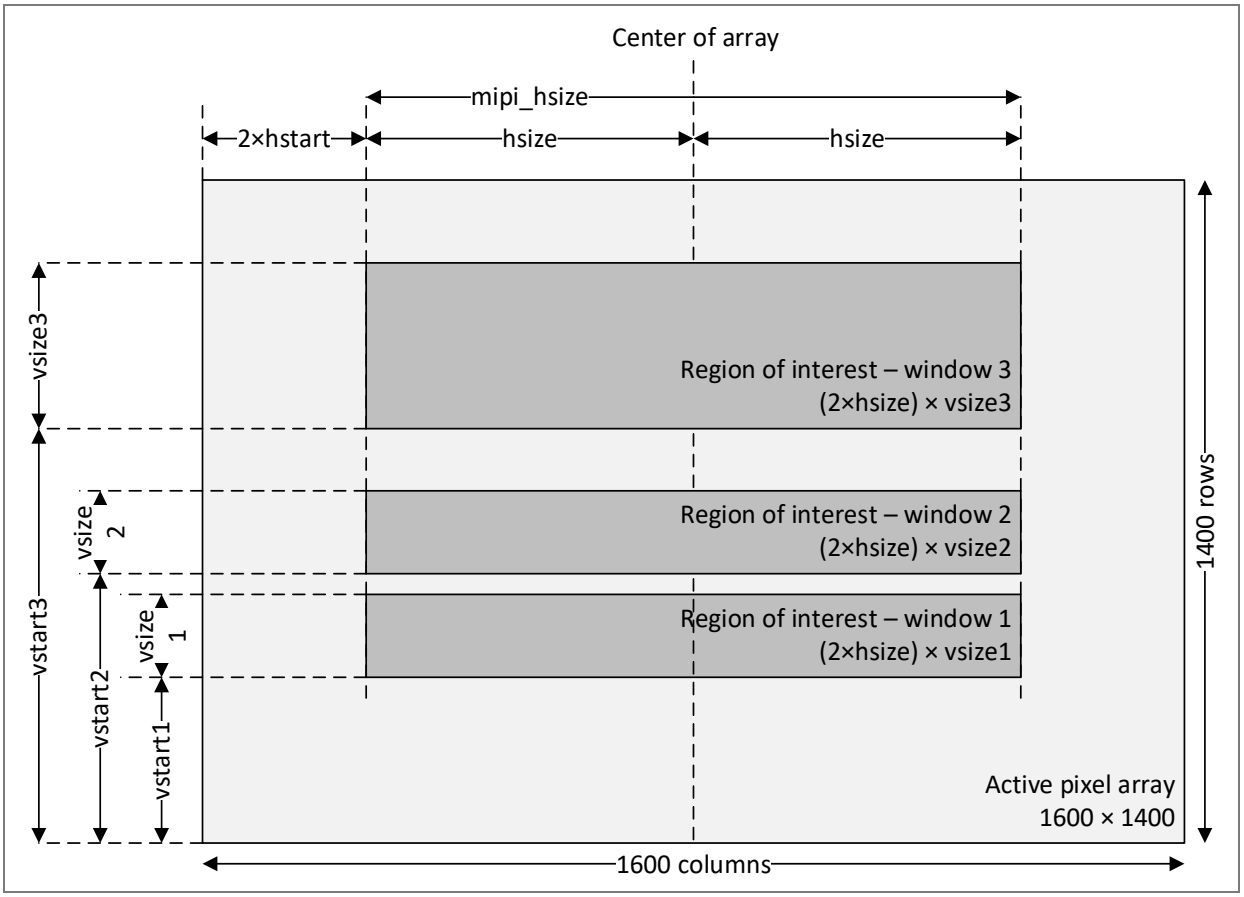


Table 18: Windowing configuration registers

Register		Address	Position	Description
VSIZE	[7:0]	0x1087	[7:0]	[10:0] – VSIZE1 Number of rows in window 1 [21:11] – VSIZE2 Number of rows in window 2 (put 0 if not used) [32:22] – VSIZE3 Number of rows in window 3 (put 0 if not used)
	[15:8]	0x1088	[7:0]	
	[23:16]	0x1089	[7:0]	
	[31:24]	0x108A	[7:0]	
	[32]	0x108B	[0]	
VSTART	[7:0]	0x107D	[7:0]	[10:0] – VSTART1 Start row of window 1 [21:11] – VSTART2 Start row of window 2 (put 0 if not used) [32:22] – VSTART3 Start row of window 3 (put 0 if not used)
	[15:8]	0x107E	[7:0]	
	[23:16]	0x107F	[7:0]	
	[31:24]	0x1080	[7:0]	
	[32]	0x1081	[0]	
HSIZE	[7:0]	0x2008	[7:0]	Number of columns in window / 2
	[9:8]	0x2009	[1:0]	
HSTART	[7:0]	0x200A	[7:0]	Start column of window / 2
	[9:8]	0x200B	[1:0]	
MIPI_HSIZE	[7:0]	0x207D	[7:0]	Number of columns in window (= 2 × HSIZE)
	[15:8]	0x207E	[7:0]	

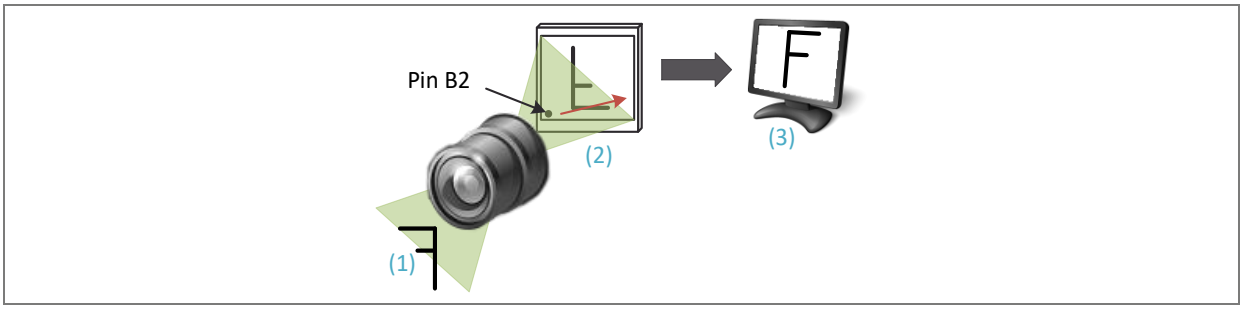
Table 19: Pre-defined window configurations

Predefined ROI	VSIZE1	VSTART1	HSIZE	HSTART	MIPI_HSIZE
2.24 MP 1600 x 1400	1400	0	800	0	1600
1.4 MP 1280 x 1120	1120	140	640	80	1280
VGA 640 x 480	480	460	320	240	640

8.2.4 Mirroring and flipping

The sensor is able to read from top to bottom, left to right or any other combination as shown in Figure 21. The default frame orientation (includes 180° rotation due to lens) is depicted in Figure 20.

Figure 20: Frame orientation for default mode



1 A normally orientated letter “F” in the scene.
2 How it projects onto the sensor (includes the point-mirroring of the lens). The view is from the top of the sensor (no pins). The red arrow shows the readout order when mirror and flip is disabled. The start of the red arrow is pixel (0, 0).
3 What the sensor outputs.

Table 20: Mirroring and flipping configuration registers

Register	Address	Position	Description
HFLIP	0x209C	[0]	Horizontal mirroring enable
VFLIP(1)	0x1095	[0]	Vertical flip enable
BIT_ORDER	0x2063	[0]	0: Normal 1: Reversed order, MSB becomes LSB and vice versa

(1) When using multiple ROI’s, only vertical flip within the ROI. The order of ROI’s is not changed.

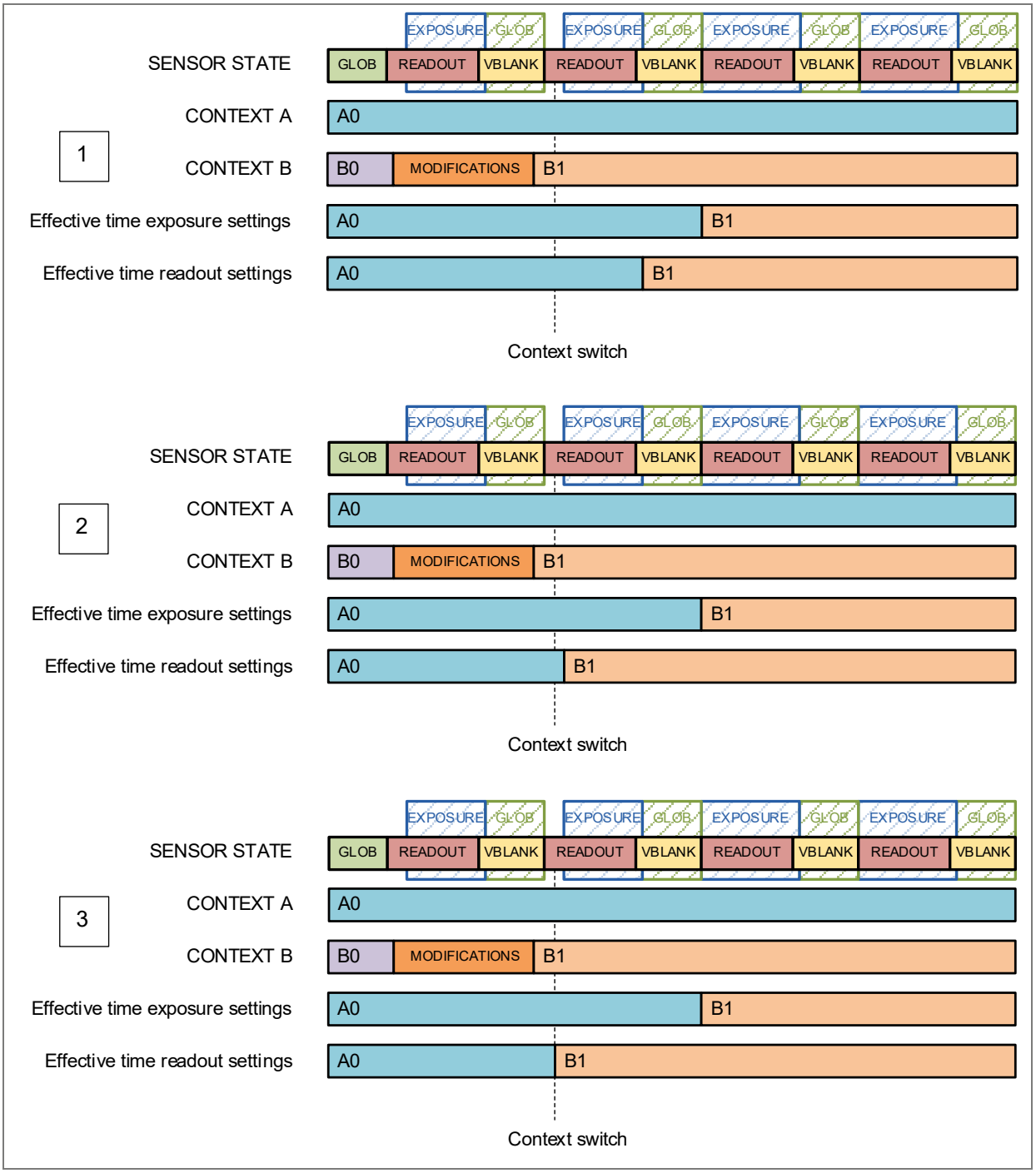
Figure 21: Mirroring and flipping

8.2.5 Context switching

Selected registers related to exposure and readout can be set to define two different modes of operation or contexts. Switching between the two contexts can happen on the fly. The registers in Table 21 control the mechanism.

When dynamic switching is disabled, the selection of a different context will take place right away after programming **CONTEXT_SEL**[0]. When dynamic switching is enabled, **CONTEXT_SW_SEL** will control when the changes are executed either before start-of-integration (SOI) or at end-of-integration (EOI).

Figure 22: Context switching procedure



1 Dynamic switching enabled, **EXP_TIME** on SOI and **HFLIP** on EOI. The effective exposure will change on the next SOI because an exposure time bigger than the frame time is not allowed in master mode.
2 Dynamic switching enabled, **EXP_TIME** on SOI for exposure settings and **HFLIP** on SOI for readout settings.
3 Immediate switching (readout settings will take effect immediately after switch, exposure settings will take effect at appropriate time in the next frame).

Table 21: Context switching configuration registers

Register	Address	Position	Description
CONTEXT_SEL	0x1100	[0]	Context selection: 0-Context A, 1-Context B
		[1]	Dynamic context switching enable
CONTEXT_SW_SEL	0x1101	[0]	Switch context for **VBLANK**: 1-SOI, 0-EOI
		[1]	Switch context for **VSTART**: 1-SOI, 0-EOI
		[2]	Switch context for **VSIZE**: 1-SOI, 0-EOI
		[4]	Switch context for **NB_OF_FRAMES**: 1-SOI, 0-EOI
		[5]	Switch context for **ROW_LENGTH**: 1-SOI, 0-EOI
		[6]	Switch context for **EXP_TIME**: 1-SOI, 0-EOI
		[7]	Switch context for **HSIZE**, **HSTART**, **HFLIP** 1-SOI, 0-EOI

Available registers with dual contexts and the corresponding addresses are listed in Table 22.

Table 22: Registers with dual context and corresponding address

Register	Position	Address context A	Address context B
VBLANK	[7:0]	0x1012	0x1103
	[15:8]	0x1013	0x1104
VSTART	[7:0]	0x107D	0x1105
	[15:8]	0x107E	0x1106
	[23:16]	0x107F	0x1107
	[31:24]	0x1080	0x1108
	[32]	0x1081	0x1109
VSIZE	[7:0]	0x1087	0x110A
	[15:8]	0x1088	0x110B
	[23:16]	0x1089	0x110C
	[31:24]	0x108A	0x110D
	[32]	0x108B	0x110E
NB_OF_FRAMES	[7:0]	0x10F2	0x1111
	[15:8]	0x10F3	0x1112
ROW_LENGTH	[7:0]	0x102B	0x1113
	[15:8]	0x102C	0x1114
EXP_TIME	[7:0]	0x100C	0x1115
	[15:8]	0x100D	0x1116
HSIZE	[7:0]	0x2008	0x2098
	[9:8]	0x2009	0x2099
HSTART	[7:0]	0x200A	0x209A
	[9:8]	0x200B	0x209B
HFLIP	[0]	0x209C	0x209D

Information:

The **MIPI_HSIZE** is not part of the context switching, which results in an extra I²C write when changing the horizontal ROI between contexts.

8.3 Configuring the output data format

8.3.1 CSI-2 layers

The sensor supports these CSI-2 protocol layer features:

- 1 or 2 data lane configuration with maximum data transfer of 1.5 Gbit/s per lane
- Continuous or non-continuous clock mode
- General and accurate frame formats

The protocol layer supports some features of the D-PHY layer. More details on these can be found in section 8.3.2:

- Ultra low power state (ULPS)
- Initial skew calibration
- Periodic skew calibration

The next sections provide some more detail on the different layers above the Physical Layer.

8.3.1.1 Application layer

The Application Layer is what is produced as data to be transmitted over the MIPI interface. The applications are:

- Pixel data
- Statistics information (see section 8.5.3).

8.3.1.2 Pixel to byte packing formats

The image pixel data from the device can have different formats. See Table 23 for available options and corresponding data types.

The Image Statistics Data from the device (see section 8.5.3) is transmitted as “Generic Long Packet” with Data Type “Embedded 8-bit non Image Data” (0x12) [CSI-2-v1.3].

Table 23: MIPI layer data format

Description	Data type
RAW8	0x2A
RAW10	0x2B
RAW12	0x2C

8.3.1.3 Low level protocol

Two packet types can be distinguished. The Short Packet Format is used for Synchronization Packets: FS, FE, LS and LE (Frame Start, Frame End, Line Start and Line End) from [CSI-2-v1.3]. The Long Packet Format is used for “RAW data” and “User Defined Byte Based Data” as specified in [CSI-2-v1.3].

Each packet consists of a header, data and footer. The table below gives on overview of the position and information contained in these different parts for different packet types.

Table 24: Packet format overview

Main part(1)	Byte field	Bit field	Long packet	Short packet	Functionality
PH	DI (Data ID)	VC	Y	Y	Virtual Channel Identifier, 2 bits
PH	DI (Data ID)	DT	Y	Y	Data Type, 6 bits
PH	WC (Word Count)		Y	N	Word Count, 16 bits
PH	Short packet data field		N	Y	LS, LE: Line number, 16 bits FS, FE: Frame number, 16 bits
PH	ECC		Y	Y	Error Correction Code, 8 bits
Packet data			Y	N	Packet Data, “WC” number of bytes
PF	CS (Checksum/CRC)		Y	N	Checksum, CRC, 16 bits

(1) Explanation of abbreviations:
PH Packet Header
PF Packet Footer

8.3.1.4 Lane management layer

The Lane Management Layer controls the number of active lanes over the MIPI interface and the associated Lane Distribution Function as defined in [CSI-2-v1.3]. The sensor supports both single and dual lane configurations.

8.3.1.5 Programming guidelines

The CSI-2 transmitter, to become operational, requires the following registers to be programmed. The CSI-2 Transmitter works in either Generic Mode or Accurate Mode.

The sequence below is for basic operation:

- Program Virtual Channel ID (**VC_ID**)
- Program horizontal active number of pixels during line blanking
- Provide data type value during line blanking
- Program **FRAME_MODE**: Frame mode register bit to ‘0’ selects generic mode and ‘1’ selects accurate mode.
- Program Lane registers (**LANE**). This will specify CSI-2 transmitter to use 1 or 2 lanes to transmit on MIPI lanes. Note that the **ROW_LENGTH** should be changed, see section 8.2.2.
- **FRAME_COUNTER** register to set the limitation of maximum frame number value.
- Program **TX_CTRL_EN** register to ‘1’ after programming all the other registers.

8.3.2 Physical layer (D-PHY)

The physical output interface consists of one clock lane and two data lanes [DPHY-v1.2]. Each lane consists of two output pins (D_P and D_N) that operate in either High Speed Mode (differential, low swing) or Low Power Mode (non-differential, high swing, slow signal).

8.3.2.1 High speed (HS) clock and data transmission

The High Speed (HS) data transmission mode transports the data packets supplied by the CSI-2 protocol handler over the interface in bursts.

8.3.2.2 Low power (LP) mode

The Low Power (LP) mode is a mode where the data or control is transmitted at a lower speed or where there is no transmission at all, allowing less power to be used. Both lines of a data output pair are used independently and have a higher voltage swing (see section 4). Specific transitions are foreseen between the LP mode and the HS mode.

- Transition between LP and HS modes: See [DPHY-v1.2]
- Electrical characteristics: See section 4 and [DPHY-v1.2]
- “Global Operation Timing Parameters”: See section below and [DPHY-v1.2]
- Slew rate control is available for LP data transmission.

8.3.2.3 Ultra low power state (ULPS)

In this state, the power is limited to a minimum by transmitting LP-00 (both lines of a data pair are transmitting a “0”).

Information:

The imager needs to be stopped before going into ULPS with **IMAGER_STATE.**

8.3.2.4 High speed skew calibration

The sensor supports both initial skew calibration and periodic skew calibration as defined in [DPHY-v1.2]. The skew calibration is used to guarantee a bit-error free sampling point of the output data.

The skew calibration sequences are generated automatically, and they are controlled through registers.

8.3.3 CSI-2 and D-PHY configuration registers

Table 25: CSI-2 and D-PHY configuration registers

Register		Address	Position	Description
VC_ID		0x207C	[1:0]	MIPI virtual channel ID
FSYNC_SOF_MAX_CTR	[7:0]	0x2064	[7:0]	Start of Frame (SOF) sequence length.
	[15:8]	0x2065	[7:0]	
FSYNC_EOF_MAX_CTR	[7:0]	0x2066	[7:0]	End of Frame (EOF) sequence length.
	[15:8]	0x2067	[7:0]	
FSYNC_EOL_MAX_CTR	[7:0]	0x2068	[7:0]	End of Line (EOL) sequence length.
	[15:8]	0x2069	[7:0]	
FSYNC_START_PW		0x206A	[3:0]	Frame timing pulse width.
FSYNC_PULSES_EN		0x206B	[0]	Vertical start after SOF event pulse enable.
			[1]	Vertical end after EOF event pulse enable.
			[2]	Horizontal start after SOF event pulse enable.
			[3]	Horizontal start after EOL event pulse enable.
			[4]	Horizontal end after EOL event pulse enable.
			[5]	Horizontal start for statistics after EOF event pulse enable.
			[6]	Data start for statistics after EOF event pulse enable.
			[7]	Horizontal end for statistics after EOF event pulse enable.
FSYNC_SOF_VSTART_ST	[7:0]	0x206C	[7:0]	MIPI vsync_start_pulse start during SOF sequence.
	[15:8]	0x206D	[7:0]	
FSYNC_EOF_VEND_ST	[7:0]	0x206E	[7:0]	MIPI vsync_end_pulse start during EOF sequence.
	[15:8]	0x206F	[7:0]	
FSYNC_SOF_HSTART_ST	[7:0]	0x2070	[7:0]	MIPI hsync_start_pulse start during SOF sequence.
	[15:8]	0x2071	[7:0]	
FSYNC_EOL_HSTART_ST	[7:0]	0x2072	[7:0]	MIPI hsync_start_pulse during EOL sequence.
	[15:8]	0x2073	[7:0]	
FSYNC_EOL_HEND_ST	[7:0]	0x2074	[7:0]	MIPI hsync_end_pulse start during EOL sequence.
	[15:8]	0x2075	[7:0]	
FSYNC_EOF_HSTART_EMB_ST	[7:0]	0x2076	[7:0]	MIPI hsync_start_pulse start for statistics data during EOF sequence.
	[15:8]	0x2077	[7:0]	

Register		Address	Position	Description
FSYNC_EOF_DSTART_EMB_ST	[7:0]	0x2078	[7:0]	MIPI Data transmission start pulse for statistics data during EOF sequence.
	[15:8]	0x2079	[7:0]	
FSYNC_EOF_HEND_EMB_ST	[7:0]	0x207A	[7:0]	MIPI hsync_end_pulse start for statistics data during EOF sequence.
	[15:8]	0x207B	[7:0]	
MIPI_SOFT_RESET		0x5004	[0]	D-PHY soft reset
			[1]	Pixel clock soft reset
			[2]	Lane clock soft reset
			[3]	Byte clock soft reset
			[4]	Escape clock reset
			[5]	APB clock reset
MIPI_PWR_DWN		0x5006	[0]	Power down enable
			[4]	0: Fast-suspend settings 1: Standby settings
MIPI_RST_CFG		0x5011	[2:0]	0x0: Active 0x1: Suspend 0x2: Standby
MIPI_VCTRL		0x5099	[4:0]	0x00: Normal mode 0x01: LP RX DC test 0x02: LP TX DC 1 0x03: LP TX DC 0 0x04: HS TX DC 1 0x05: HS TX DC 0 0x09: LP TX parbert data burst 0x0A: LP TX parbert data continuous 0x0B: LP TX fixed data burst 0x0C: LP TX fixed data continuous 0x0D: HS TX skewcal + fixed data burst 0x0E: HS TX skewcal + fixed data continuous 0x0F: HS TX fixed data with burst 0x10: HS TX fixed data with continuous 0x11: HS TX skewcal + parbert continuous 0x12: HS TX skewcal + PRBS9 continuous 0x13: HS TX skewcal + parbert burst 0x14: HS TX skewcal + PRBS9 burst 0x15: HS TX parbert burst 0x16: HS TX PRBS9 burst 0x1B: HS TX parbert continuous 0x1C: HS TX PRBS9 continuous 0x1D: HS TX internal loopback 0x1E: ULPS 0x1F: Suspend mode
DPDN_SWAP		0x50D9	[2:0]	Enable DP/DN swap function.
TINIT	[15:8]	0x6001	[7:0]	

Register		Address	Position	Description
	[7:0]	0x6002	[7:0]	Initialization period. After power-up, TxRequestHSC will be asserted after this Tinit time to initiate HS clock transmission by PHY.
TX_CTRL_EN		0x6006	[0]	0: Controller not ready 1: Controller ready to transfer This bit needs to be set after all other registers are programmed.
FRAME_MODE		0x6010	[0]	0: General frame format 1: Accurate frame format
			[1]	0: General embedded frame format 1: Accurate embedded frame format
POLARITY(1)		0x6011	[0]	Data Enable Polarity (0-Active high)
			[1]	HSYNC polarity (0-Active high)
			[2]	VSYNC polarity (0-Active high)
LANE		0x6012	[0]	0: 1 lane 1: 2 lanes
CLK_MODE(2)		0x6013	[0]	0: Continuous PHY clocking 1: Non-continuous PHY clocking.
ULPS		0x6014	[0]	Puts clock lane in ULPS Mode.
			[1]	Exits clock lane out of ULPS Mode.
		0x6015	[0]	Puts Data_0 in ULPS mode.
			[1]	Exit Data_0 out of ULPS mode.
			[2]	Puts Data_1 in ULPS mode.
			[3]	Exits Data_1 out of ULPS mode.
FRAME_COUNTER	[15:8]	0x6016	[7:0]	If 0, frame number is disabled. Otherwise, the frame number periodically resets to 1 after FRAME_COUNTER value is reached.
	[7:0]	0x6017	[7:0]	
LINE_COUNT_RAW		0x6037	[0]	RAW8: 0-disable; 1-line counter increments with 1.
			[1]	RAW10: 0-disable; 1-line counter increments with 1.
			[2]	RAW12: 0-disable; 1-line counter increments with 1.
LINE_COUNT_USER_DEF		0x6038	[0]	UDT1, 0-disable, 1- += 1
			[1]	UDT2, 0-disable, 1- += 1
			[2]	UDT3, 0-disable, 1- += 1
			[3]	UDT4, 0-disable, 1- += 1
			[4]	UDT5, 0-disable, 1- += 1
			[5]	UDT6, 0-disable, 1- += 1

Register		Address	Position	Description
			[6]	UDT7, 0-disable, 1- += 1
			[7]	UDT8, 0-disable, 1- += 1
LINE_COUNT_EMB		0x6039	[0]	Enable line counter for embedded data.
INTERRUPT_EN		0x6018	[0]	Enable interrupt to indicate CCI read command is received.
			[1]	Enable interrupt to indicate CCI write command is received.
INTERRUPT_STATUS		0x6019	[0]	Asserted by the controller when CCI read command is received.
			[1]	Asserted by the controller when CCI write command is received.
TWAKE_TIMER	[15:8]	0x6065	[7:0]	Timer that TX drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS. Protocol waits for a time Twake and then drives TxRequestEscx (TxUlpsClk) inactive to return the lane to stop state. This timer runs in TxClkEsc.
	[7:0]	0x6066	[7:0]	
SKEW_CAL_EN		0x601C	[0]	Enable periodic skew calibration TxSkewCalHS0 PPI signal during Frame blanking.
SKEW_COUNT	[11:8]	0x601D	[3:0]	Time duration of skew calibration pattern in the periodic skew calibration during Frame blanking.
	[7:0]	0x601E	[7:0]	
SCRAMBLING_EN		0x601F	[0]	Scrambling enable
INIT_SKEW_EN(3)		0x6003	[0]	Enable initial skew calibration assert PPI signal during initialization.
INIT_SKEW	[15:8]	0x6004	[7:0]	Time duration of initial skew-calibration pattern. Value denotes number of byte clocks.
	[7:0]	0x6005	[7:0]	

(1) Before programming, reset should apply.
(2) Program after the common upload file is written to the sensor.
(3) Program before setting register TX_CTRL_EN.

8.3.4 MIPI data rate

By default, after power-up the MIPI transmitter is configured in 1.5 Gbit/s transmission mode. To configure MIPI transmitter into different data rates, the following values from Table 26 should be written in the same order.

Table 26: MIPI data rate configuration sequence (in Gbit/s per lane)

Address	1.5	1.4	1.3	1.2	1.1	1	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2	0.1	0.08
0x5004	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01
0x5086	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x5087	0x4E	0x48	0x43	0x3E	0x39	0x34	0x2E	0x53	0x48	0x7D	0x68	0x53	0x7D	0x53	0x53	0x42
0x5088	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x5090	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x02	0x02	0x04	0x04	0x04	0x06	0x06	0x08	0x08
0x5091	0x08	0x07	0x07	0x06	0x06	0x05	0x05	0x09	0x08	0x0E	0x0C	0x0A	0x11	0x0C	0x10	0x0E
0x5092	0x14	0x14	0x12	0x11	0x0F	0x0E	0x0D	0x17	0x14	0x23	0x1D	0x18	0x25	0x1B	0x21	0x1D
0x5093	0x0F	0x0E	0x0D	0x0D	0x0C	0x0B	0x0A	0x10	0x0F	0x17	0x14	0x11	0x19	0x13	0x17	0x15
0x5094	0x06	0x06	0x05	0x05	0x04	0x04	0x03	0x07	0x06	0x0A	0x09	0x07	0x0A	0x07	0x07	0x05
0x5095	0x32	0x2F	0x2C	0x28	0x25	0x22	0x1F	0x35	0x2F	0x50	0x42	0x35	0x50	0x35	0x35	0x2B
0x5096	0x0E	0x0E	0x0D	0x0C	0x0B	0x0B	0x0A	0x0F	0x0E	0x15	0x12	0x0F	0x15	0x0F	0x0F	0x0D
0x5097	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x01	0x01	0x03	0x03	0x03	0x07	0x07	0x0F	0x0F
0x5098	0x11	0x10	0x0F	0x0F	0x0E	0x0D	0x0C	0x18	0x16	0x2B	0x28	0x25	0x45	0x3F	0x73	0x71
0x5004	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x2066	0x6C	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x2067	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x10	0x14	0x18	0x28	0x30	0x40	0x40	0x50	0x60
0x206E	0x7E	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x206F	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0E	0x13	0x16	0x20	0x28	0x30	0x38	0x4C	0x58
0x20AC	0x7E	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x20AD	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0E	0x13	0x16	0x20	0x28	0x30	0x38	0x4C	0x58
0x2076	0xC8	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0xC8
0x2077	0x00	0x04	0x05	0x05	0x06	0x06	0x07	0x09	0x11	0x12	0x1A	0x22	0x24	0x30	0x44	0x50
0x20B4	0xC8	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0xC8
0x20B5	0x00	0x04	0x05	0x05	0x06	0x06	0x07	0x09	0x11	0x12	0x1A	0x22	0x24	0x30	0x44	0x50
0x2078	0x1E	0x1E	0x5E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E
0x2079	0x04	0x05	0x05	0x05	0x06	0x06	0x07	0x09	0x11	0x12	0x1A	0x22	0x24	0x34	0x44	0x54
0x20B6	0x1E	0x1E	0x5E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E
0x20B7	0x04	0x05	0x05	0x05	0x06	0x06	0x07	0x09	0x11	0x12	0x1A	0x22	0x24	0x34	0x44	0x54
0x207A	0xD4	0xA0	0xE0	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4
0x207B	0x04	0x05	0x05	0x05	0x06	0x06	0x07	0x09	0x11	0x12	0x1A	0x22	0x24	0x34	0x44	0x54
0x20B8	0xD4	0xA0	0xE0	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4	0xD4
0x20B9	0x04	0x05	0x05	0x05	0x06	0x06	0x07	0x09	0x11	0x12	0x1A	0x22	0x24	0x34	0x44	0x54

The row length needs to be adapted based on the required MIPI speed and rounded up to ensure the row time is long enough to transmit all the data. E.g. the MIPI data rate is set to 0.8 Gbit/s then the row length must increase to [304*1.5/0.8] = 563 = 0x0233. The frame rate and exposure time would be limited due to this row time increase.

8.4 Configuring the on-chip data processing

8.4.1 Black sun protection

The black sun protection is used to avoid dark spots in the image, caused by high light levels in extremely oversaturated scenes.

Table 27: Black sun protection configuration registers

Register	Address	Position	Description
BSP	0x4006	[3:0]	0xF: Disable BSP 0x8: Enable BSP

8.4.2 Bit depth

The sensor supports different image bit depths. Please note that the correct MIPI data type should be selected for each bit depth.

Table 28: Image bit depth configuration registers

Register	Address	Position	Description
BIT_DEPTH	0x209E	[2:0]	0x2: 12-bit
			0x4: 10-bit
			0x6: 8-bit
CSI2_DTYPE	0x208D	[2:0]	0x4: 12-bit
			0x2: 10-bit
			0x1: 8-bit

8.4.3 Digital correlated double sampling

The sensor supports Digital Correlated Double Sampling (DCDS). If enabled, DCDS logic subtracts the pixel signal value from the pixel reset value.

Table 29: Digital CDS configuration registers

Register	Address	Position	Description
CDS_RNC	0x2045	[0]	Row noise correction column CDS enable
CDS_IMG	0x2048	[0]	Image column CDS enable

8.4.4 Row noise correction

The sensor supports row noise correction. Refer to application note AN001032 when changing the flat field target value.

Table 30: Row noise correction configuration registers

Register		Address	Position	Description
RNC_EN		0x204B	[1:0]	0x0: Disable row noise correction 0x3: Enable row noise correction
RNC_DARK_TARGET	[7:0]	0x205B	[7:0]	Flat field target value
	[11:8]	0x205C	[7:0]	

8.4.5 Defect pixel detection and correction

An investigated pixel (A) can be detected as a defect and corrected by the use of four surrounding pixels (v, w, x and y). These four pixels are located next to A in two dimensions or on a line. The two modes are illustrated in Figure 23 and Figure 24. Other pixels are not taken into account. For the 2D mode, the pixels from the first and last columns and rows are not corrected. For the 1D mode, the pixels from the first two and last two columns are not corrected.

Figure 23: Defect pixel mode 2D

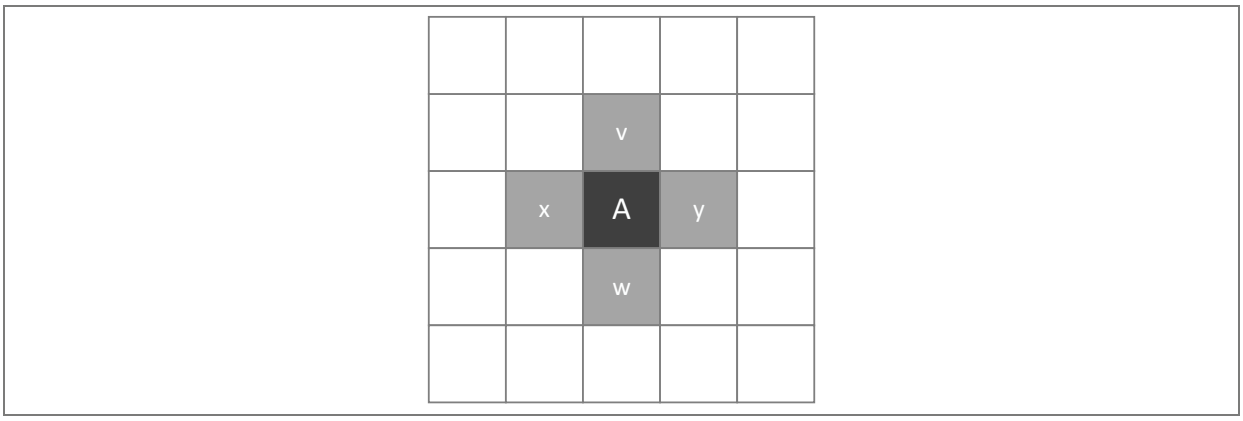
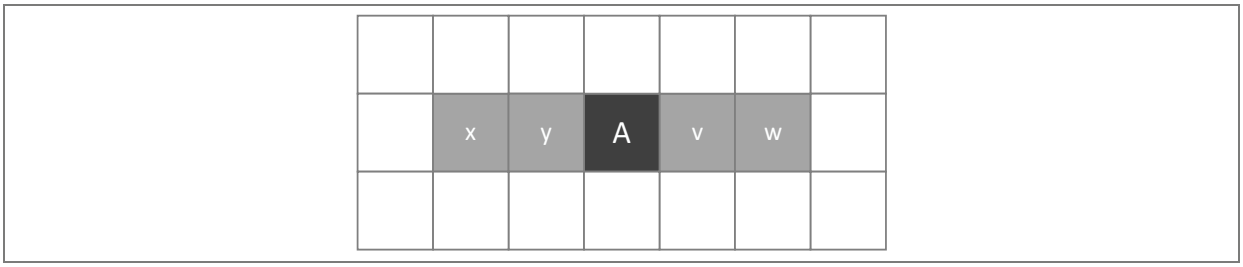


Figure 24: Defect pixel mode 1D



From the four pixels, the minimal and maximal value are taken. These values are used as inputs for the pixel defect detection limits:

- The minimal value (MIN) is used for the calculation of the lower limit.
- The maximal value (MAX) is used for the calculation of the higher limit.
- A defect pixel is detected as being defective when its value is outside the limits mentioned above. When it is detected, it can be corrected.

The **DC_LIMIT_LOW** and **DC_LIMIT_HIGH** are used for this calculation, but two modes are possible for the higher limit. The selection between both is done with the **DEFECT_LIMIT_HIGH_MODE** setting.

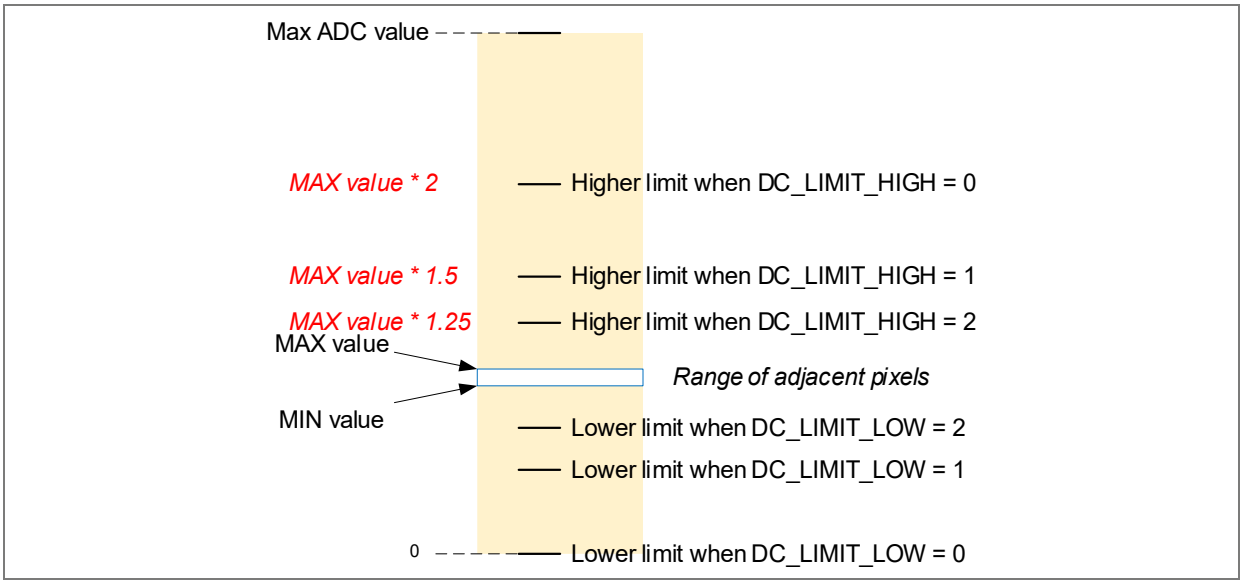
The lower and higher limits are calculated as follows and shown in Figure 25 and Figure 26:

$$lower\ limit = MIN \cdot (1 - 2^{-DC\_LIMIT\_LOW})$$

$$higher\ limit = \begin{cases} MAX \cdot (1 + 2^{-DC\_LIMIT\_HIGH}), & DC\_LIMIT\_HIGH\_MODE = 0 \\ MAX + (NOT\ MAX) \cdot 2^{-DC\_LIMIT\_HIGH}, & DC\_LIMIT\_HIGH\_MODE = 1 \end{cases}$$

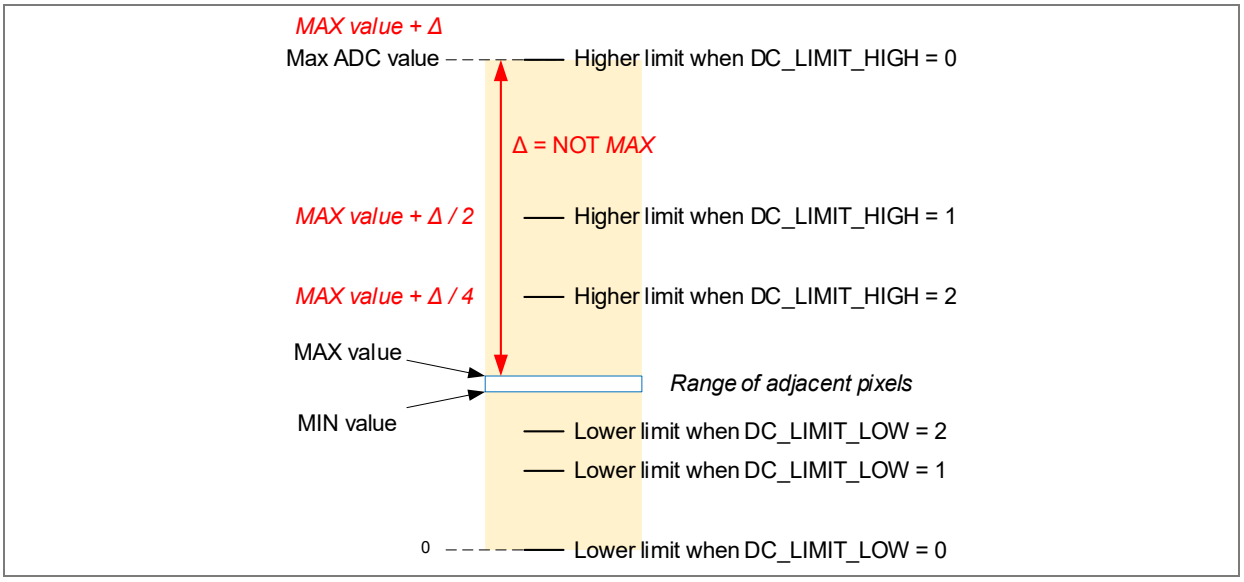
with 'NOT MAX' = bit-per-bit inversion of the MAX value.

Figure 25: Defect high limit calculation (Mode 0)



The higher limit calculated in this way is relative to the effective value of the MAX value and can maximally be the double of the MAX value. This can be a problem for low values or "black" where the limit will be too tight to the pixel value.

Figure 26: Defect high limit calculation (Mode 1)



This higher limit calculation is leading to levels that are “symmetrical” to the behavior of the lower limit calculation. Here, the highest value is the maximal pixel value.

Following algorithms are supported for the pixel corrections where A is replaced by:

- Median(v, w, x, y)
- Mean(v, w, x, y)
- Min(mean(v, w), mean(x, y))
- Max(mean(v, w), mean(x, y))

Table 31: Defect pixel correction configuration registers

Register	Address	Position	Description
DC_CFG	0x24DC	[0]	Defect correction enable
		[1]	Mode 0: 2D 1: 1D
		[5:4]	Replacement value 0x0: Median 0x1: Mean 0x2: Minimum 0x3: Maximum
DC_LIMIT_LOW	0x24DD	[3:0]	Low limit
DC_LIMIT_HIGH	0x24DE	[3:0]	High limit
DC_LIMIT_HIGH_MODE	0x24DF	[0]	High limit mode

8.5 Additional features

8.5.1 Illumination trigger

A trigger signal or a sequence of trigger signals on the external pin ILLUM_TRIGGER can be sent off chip by the sensor to activate an external component such as a flash or illumination device (VCSEL). The trigger signal is synchronized to the sensor exposure moment. The trigger signal can be enabled or disabled.

Figure 27: Illumination trigger timing

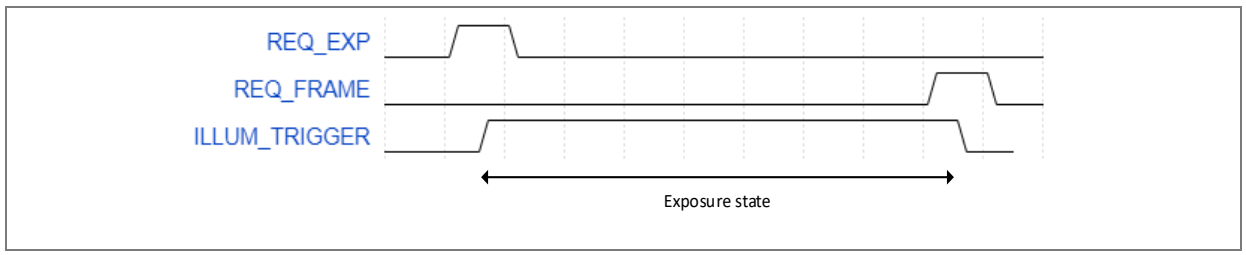


Table 32: Illumination trigger configuration registers

Register	Address	Position	Description
ILLUM_EN	0x10D7	[0]	Illumination trigger enable
ILLUM_POL	0x10D8	[1]	Polarity

8.5.2 Read trigger

The sensor sends a trigger signal off chip on the external pin READ_TRIGGER. This trigger signal is synchronized to the sensor readout moment.

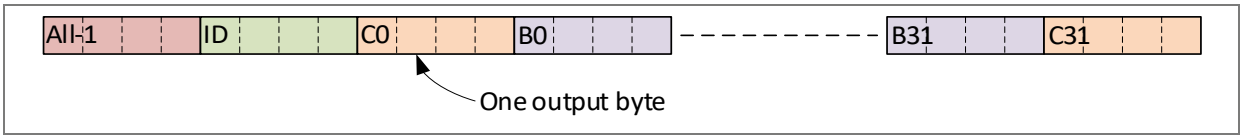
8.5.3 Image statistics

The value of the pixels of a frame can be statistically investigated and gathered into a histogram containing 32 bins. Next to the 32 equally distributed bins, also the number of clipped black and clipped white pixels are separately gathered and sent out.

The histogram is packed into a data-byte oriented CSI-2 packet which is sent over the D-PHY at the end of the transmission of the frame. The sensor will send out the Image Statistics Data as a CSI-2 Generic Long Packet with Data Type “Embedded 8-bit non Image Data” (0x12) and with the currently used Virtual Channel ID.

The Image Statistics Histogram Data format is shown in Figure 28. The data part of a packet consists of 36 groups of each 4 bytes. The first element will contain all-1s (start of sequence marker), the histogram ID will be all-0s, then followed by the bin data.

Figure 28: Histogram data formatting



The bin data is structured as follows:

1. “C0”: Bin containing the number of pixels that are 0 (black pixels)
2. “B0” – “B31”: 32 equally sized histogram bins spread over the entire output range
3. “C31”: Bin containing the number of pixels that have the maximum value (white pixels). All pixels in bin “C0” are also part of bin “B0”. All pixels in bin “C31” are also part of bin “B31”.

It is possible not to include all pixels in the statistic gathering. The spatial distribution is configured by register settings. Since the data path processes and operates on two pixels simultaneously, the spatial distribution keeps two neighboring pixels and skips by multiple number of groups of two pixels as shown in Figure 29. This is done for each row of the pixel array.

Figure 29: Histogram spatial distribution of input data

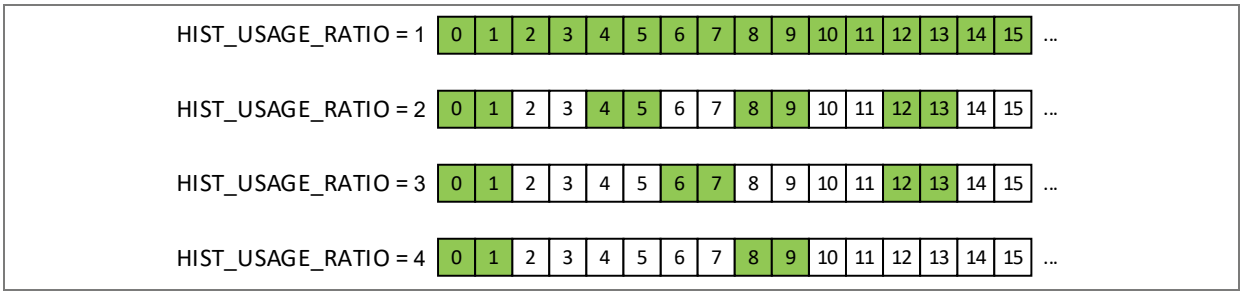


Table 33: Image statistics configuration registers

Register	Address	Position	Description
HIST_EN	0x205D	[0]	Enable image statistics calculation
HIST_USAGE_RATIO	0x205E	[7:0]	Spatial distribution configuration
PIXEL_DATA_SUPP	0x2063	[1]	0: Send both pixel data and statistics 1: Send only statistics
		[2]	0: Statistic transmission disabled 1: Statistic transmission enabled

8.5.4 Temperature sensor

The sensor contains a temperature sensor in the readout layer. The temperature sensor produces a voltage proportional to the temperature (VPTAT) and a temperature invariant reference voltage (VREF). An ADC converts the output of the temperature sensor to a 22-bit digital gray code. This ADC is identical to the ADC's used for pixel conversions. The temperature sensor output is updated once per row length during readout and is available over the CCI interface and during the readout of image data.

Table 34: Temperature sensor registers

Register		Address	Position	Description
TSENS_SIG	[7:0]	0x3188	[7:0]	Temperature sensor signal value (VPTAT)
	[11:8]	0x3189	[3:0]	
TSENS_RST	[7:0]	0x318E	[7:0]	Temperature sensor reset value (VREF)
	[9:8]	0x318F	[1:0]	

8.5.4.1 Uncalibrated temperature measurement

The temperature sensor typically produces a differential voltage, VREF - VPTAT, of 140 mV at 25 °C with a slope of 1.63 mV/°C. The conversion of the register value to degrees Celsius is shown in the following equation.

Equation 3:

$$T[°C] = \frac{[gray\_to\_decimal(TSENS\_SIG) - gray\_to\_decimal(TSENS\_RST)] * 0.181 - 140}{1.63} + 25$$

8.5.4.2 Calibrated temperature measurement

The accuracy of temperature measurements can be improved after performing a single-point calibration. During wafer test, the temperature is measured in a controlled environment. Calibration data is written to the OTP memory of the sensor (see 8.5.5). The calibrated temperature is calculated using the following equation.

Equation 4:

$$T_{cal}[°C] = \frac{T_{wafer,expected}[°C]}{T_{wafer,measured}[°C]} \cdot T_{uncal,x}\ [°C]$$

Which uses the following parameters:

- $T_{wafer,expected}$: The expected temperature at wafer test, which is 60 °C. The exact value is stored in OTP register “Chuck temperature”.
- $T_{wafer,measured}$: The measured (uncalibrated) temperature sensor value at wafer test. The value can be calculated based on the temperature sensor readout values TSENS_SIG and TSENS_RST stored in OTP registers. This calibration gain coefficient is fixed and only needs to be calculated once.

8.5.5 OTP memory

A non-volatile, one time programmable memory is included on-chip. The OTP memory is organized in 1024 addresses of 32 bits each. Part of the memory (0x000 - 0xFF) is used by ams OSRAM for a unique device ID and sensor calibration data. The sensor calibration data has to be read from the specified OTP addresses and written into specific registers as shown in Table 35 by the customer. The addresses not mentioned in the ams OSRAM space below are subject to change without notice. The remaining addresses of the OTP are available to the customer (0x100 - 0x3FF). For further details on reading calibration values on OTP please refer to AN001030.

Attention:

The OTP data on the same address location cannot be written more than three times. It is not recommended to do this because neighboring locations might be affected.

The OTP is not write protected. Hence, the customer is responsible for not overwriting the preprogrammed OTP data which is essential for calibration. Furthermore, the customer is responsible to ensure the integrity of the data they program themselves.

Table 35: Relevant OTP addresses

Address	Position	Description	Destination registers
0x00	[2:0]	Calibration bits for VDD11A	0x4015 [2:0]
0x01	[2:0]	Calibration bits for VDD11D	0x4016 [2:0]
0x01	[6:4]	Calibration bits for VDD11PLL	0x4016 [6:4]
0x04	[5:0]	Calibration bits for VDDNEG_2	0x403B [5:0]
0x05	[2:0]	Calibration bits for VDDINT_4	0x4040 [2:0]
0x05	[6:4]	Calibration bits for VDDINT_5	0x4040 [6:4]
0x06	[2:0]	Calibration bits for VSEL_HI (not observable, programmed to 7)	0x4041 [2:0]
0x06	[6:4]	Calibration bits for VDDINT_2	0x4041 [6:4]
0x07	[2:0]	Calibration bits for VDDINT_3	0x4042 [2:0]
0x08	[6:0]	Calibration bits for VSEL_VREF	0x402A [6:0]
0x09	[6:0]	Calibration bits for VSEL_VOS	0x4029 [6:0]
0x0A	[5:0]	Calibration bits for RAMPGEN_TRIMM_X1 1x gain calibration	0x4009 [5:0]
0x0D	[4:0]	Calibration bits for VDDNEG_1	0x403E [4:0]
0x0E	[15:0]	Black level value	
0x19	[15:0]	Chuck temperature [°C]	
0x1B	[11:0]	TSENS_SIG at 60 °C	
0x1C	[9:0]	TSENS_RST at 60 °C	
0x1D	[31:0]	Unique device ID(1)	
0x1E	[23:0]		
0x25	[7:0]		
0x3A	[7:0]	Revision number of the sample	
0x3E	[31:0]	SAP material code	

(1) The order is 0x1D, 0x1E, 0x25. For example 07:E4:0C:09:09:08:22:00.

Table 36: OTP configuration registers

Register		Address	Position	Description
OTP_CMD		0x0080	[0]	Write (self-clearing)
			[1]	Read (self-clearing)
			[2]	Power up (self-clearing)
			[3]	Power down (self-clearing)
			[4]	Deep standby ON (self-clearing)
			[5]	Deep standby OFF (self-clearing)
OTP_STATUS		0x0081	[0]	Status bit: 1-OTP is ready for next command
			[1]	Power status: 0-OFF, 1-ON
			[2]	Standby status: 0-OFF, 1-ON
OTP_RDATA	[7:0]	0x0082	[7:0]	Read data
	[15:8]	0x0083	[7:0]	
	[23:16]	0x0084	[7:0]	
	[31:24]	0x0085	[7:0]	
OTP_ADDR	[7:0]	0x0086	[7:0]	Address
	[9:8]	0x0087	[1:0]	
OTP_WDATA	[7:0]	0x0088	[7:0]	Write data
	[15:8]	0x0089	[7:0]	
	[23:16]	0x008A	[7:0]	
	[31:24]	0x008B	[7:0]	

The procedure to read an OTP address is as follows:

1. Power on: Write 0x04 to address 0x0080
2. Set address: Write OTP address to address 0x0086
3. Read OTP instruction: Write 0x02 to address 0x0080
4. Read data: Read from address 0x0082 to 0x0085
5. Power off: Write 0x08 to address 0x0080

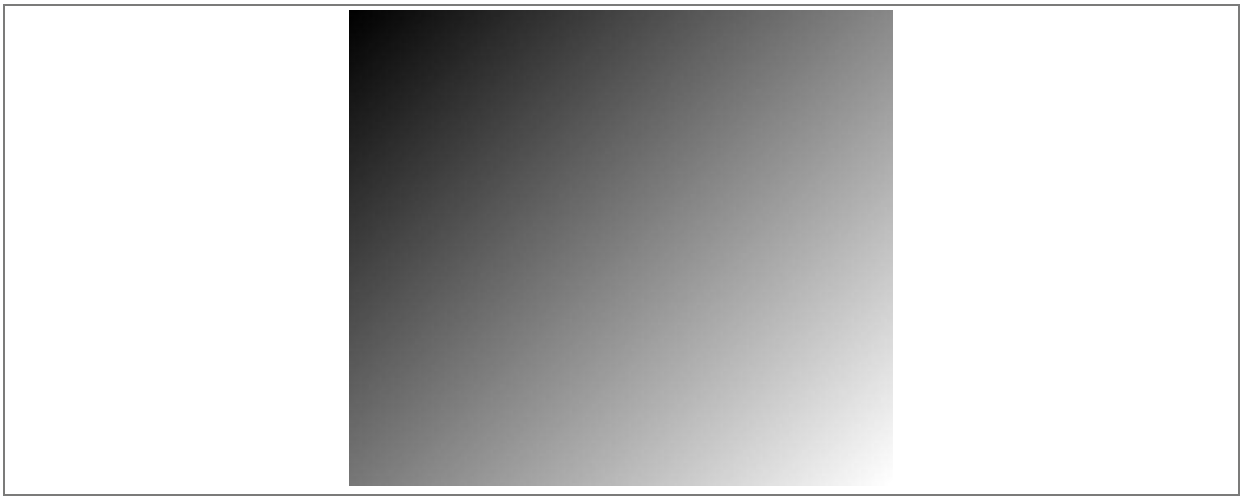
8.5.6 Test images

Different test images patterns are available: vertical gradient, diagonal gradient, walking 1's and walking 0's.

Table 37: Test image configuration registers

Register	Address	Position	Description
TEST_PATTERN_CFG	0x2091	[0]	Image test pattern enable
		[6:4]	0x0: Vertical gradient 0x1: Diagonal gradient 0x4: Walking 1's 0x5: Walking 0's

Figure 30: Test image diagonal gradient



8.5.7 Power modes and power saving options

8.5.7.1 Power modes

The sensor supports different fully configurable power modes. This allows putting the sensor in a low-power sleep mode when not used or activate all blocks again with a single CCI command, see section 7.7 and application note AN001027.

8.5.7.2 Power saving options

When using a reduced ROI, it is possible to disable parts of the readout circuit. Figure 31 shows the partitioning of the readout circuit.

Figure 31: Readout circuit partitioning

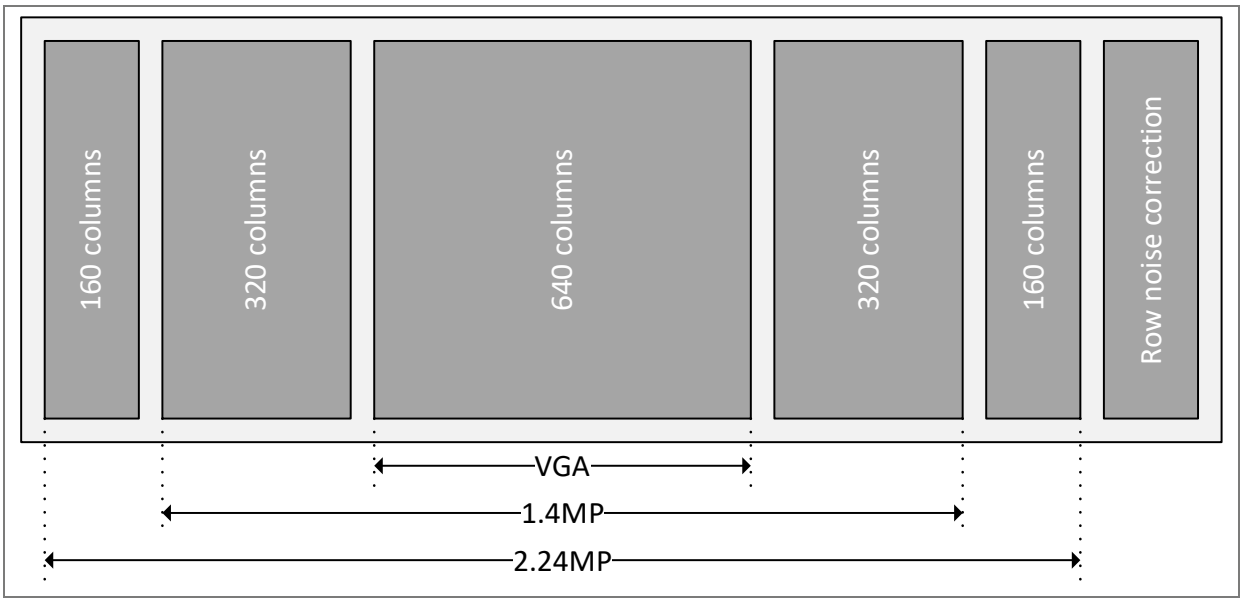


Table 38: Readout power saving configuration registers

Window	Address	Position	RNC enabled	RNC disabled
2.24MP	0x4006	[3:0]	0x8	0x8
	0x4007	[7:0]	0x00	0x88
	0x401C	[3:0]	0xF	0x7
1.4MP	0x4006	[3:0]	0xC	0xC
	0x4007	[7:0]	0x44	0xCC
	0x401C	[3:0]	0xB	0x3
VGA	0x4006	[3:0]	0xE	0xE
	0x4007	[7:0]	0x66	0xEE
	0x401C	[3:0]	0x9	0x1

9 Register description

Below is an overview of all registers, together with their default value after reset/startup. Some registers have to be changed to another fixed value after reset/startup, independent of the sensor control or modes. This value is in the last column.

Attention:

For register settings that require multiple addresses to be written, please ensure that the LSB is written before the MSB. For example, to change the exposure time first write 0x100c and then 0x100d.

Table 39: Register overview

Addr	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	Default	Fixed	Type
0x0012	-	-	-	-	-	DRIVE_STRENGTH			0x00	-	rw
0x0040	-	-	-	-	-	-	-	CMD_SOFT_RESET	0x00	-	strobe
0x0041	-	-	-	-	-	-	-	CMD_REQ_EXPOSURE	0x00	-	rw
0x0042	-	-	-	-	-	-	-	CMD_REQ_FRAME	0x00	-	strobe
0x0043	-	-	-	-	POWER_MODE				0x0C	-	rw
0x0080	-	OTP_CMD							0x00	-	strobe
0x0081	-	-	-	-	-	OTP_STATUS			0x00	-	ro
0x0082	OTP_RDATA								0x00	-	ro
0x0083									0x00	-	ro
0x0084									0x00	-	ro
0x0085									0x00	-	ro
0x0086	OTP_ADDR								0x00	-	rw
0x0087	-	-	-	-	-	-	OTP_ADDR		0x00	-	rw
0x0088	OTP_WDATA								0x00	-	rw
0x0089									0x00	-	rw
0x008A									0x00	-	rw
0x008B									0x00	-	rw
0x1001	-	EXT_EVENT_SEL	-	-	-	-	-	EXT_EXP_PW_SEL	0xD0	-	rw
0x1002	-	-	-	-	-	IMAGER_RUN_CONT	-	-	0x00	-	rw
0x1003	-	-	IMAGER_STATE						0x01	-	rw
0x100C	EXP_TIME								0xBC	-	rw
0x100D									0x02	-	rw
0x1012	VBLANK								0x06	-	rw

Addr	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	Default	Fixed	Type
0x1013									0x00	-	rw
0x102B					ROW_LENGTH				0x30	0x2C	rw
0x102C									0x01	0x01	rw
0x107D					VSTART1				0x00	-	rw
0x107E				VSTART2				VSTART1	0x00	-	rw
0x107F		VSTART3				VSTART2			0x00	-	rw
0x1080					VSTART3				0x00	-	rw
0x1081	-	-	-	-	-	-	-	VSTART3	0x00	-	rw
0x1087					VSIZE1				0x78	-	rw
0x1088				VSIZE2				VSIZE1	0x05	-	rw
0x1089		VSIZE3				VSIZE2			0x00	-	rw
0x108A					VSIZE3				0x00	-	rw
0x108B	-	-	-	-	-	-	-	VSIZE3	0x00	-	rw
0x1095	-	-	-	-	-	-	-	VFLIP	0x00	-	rw
0x10D0					EXT_EXP_DELAY				0x00	-	rw
0x10D1									0x00	-	rw
0x10D7	-	-	-	-	-	-	-	ILLUM_EN	0x01	-	rw
0x10D8	-	-	-	-	-	-	ILLUM_POL		0x02	-	rw
0x10F0	-	-	-	-	-	-	-	IMAGER_RUN	0x00	-	strobe
0x10F2					NB_OF_FRAMES				0x04	-	rw
0x10F3									0x00	-	rw
0x1100	-	-	-	-	-	-	CONTEXT_SEL		0x00	-	rw
0x1101					CONTEXT_SW_SEL				0x40	-	rw
0x1102	-	-	-	-	-	-	-	CONTEXT_SW_SEL	0x00	-	rw
0x1103					VBLANK_B				0x06	-	rw
0x1104									0x00	-	rw
0x1105					VSTART1_B				0x10	-	rw
0x1106				VSTART2_B				VSTART1_B	0x00	-	rw
0x1107		VSTART3_B				VSTART2_B			0x02	-	rw
0x1108					VSTART3_B				0x30	-	rw
0x1109	-	-	-	-	-	-	-	VSTART3_B	0x00	-	rw
0x110A					VSIZE1_B				0x0A	-	rw
0x110B				VSIZE2_B				VSIZE1_B	0xC0	-	rw
0x110C		VSIZE3_B				VSIZE2_B			0x00	-	rw
0x110D					VSIZE3_B				0x0E	-	rw
0x110E	-	-	-	-	-	-	-	VSIZE3_B	0x00	-	rw
0x1111					NB_OF_FRAMES_B				0x04	-	rw
0x1112									0x00	-	rw
0x1113					ROW_LENGTH_B				0x30	-	rw
0x1114									0x01	-	rw

Addr	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	Default	Fixed	Type
0x1115	EXP_TIME_B								0x0A	-	rw
0x1116									0x00	-	rw
0x2008	HSIZE								0x20	-	rw
0x2009	-	-	-	-	-	-	HSIZE		0x03	-	rw
0x200A	HSTART								0x00	-	rw
0x200B	-	-	-	-	-	-	HSTART		0x00	-	rw
0x2045	-	-	-	-	-	-	-	CDS_RNC	0x01	-	rw
0x2048	-	-	-	-	-	-	-	CDS_IMG	0x01	-	rw
0x204B	-	-	-	-	-	-	RNC_EN		0x03	-	rw
0x205B	RNC_DARK_TARGET								0x20	0x64	rw
0x205C	-	-	-	-	RNC_DARK_TARGET				0x00	0x00	rw
0x205D	-	-	-	-	-	-	-	HIST_EN	0x01	-	rw
0x205E	HIST_USAGE_RATIO								0x01	-	rw
0x2063	-	-	-	-	-	PIXEL_DATA_SUPP		BIT_ORDER	0x04	-	rw
0x2064	FSYNC_SOF_MAX_CTR								0xF8	-	rw
0x2065									0x07	-	rw
0x2066	FSYNC_EOF_MAX_CTR								0x6C	-	rw
0x2067									0x07	-	rw
0x2068	FSYNC_EOL_MAX_CTR								0x00	-	rw
0x2069									0x02	-	rw
0x206A	-	-	-	-	FSYNC_START_PW				0x04	-	rw
0x206B	FSYNC_PULSES_EN								0xFF	-	rw
0x206C	FSYNC_SOF_VSTART_ST								0x00	-	rw
0x206D									0x02	-	rw
0x206E	FSYNC_EOF_VEND_ST								0x7E	-	rw
0x206F									0x06	-	rw
0x2070	FSYNC_SOF_HSTART_ST								0x6A	-	rw
0x2071									0x07	-	rw
0x2072	FSYNC_EOL_HSTART_ST								0xC8	-	rw
0x2073									0x00	-	rw
0x2074	FSYNC_EOL_HEND_ST								0x64	-	rw
0x2075									0x00	-	rw
0x2076	FSYNC_EOF_HSTART_EMB_ST								0xC8	-	rw
0x2077									0x00	-	rw
0x2078	FSYNC_EOF_DSTART_EMB_ST								0x1E	-	rw
0x2079									0x04	-	rw
0x207A	FSYNC_EOF_HEND_EMB_ST								0xD4	-	rw
0x207B									0x04	-	rw
0x207C	-	-	-	-	-	-	VC_ID		0x00	-	rw
0x207D	MIPI_HSIZE								0x40	-	rw
0x207E									0x06	-	rw
0x208D	-	-	-	-	-	CSI2_DTYPE			0x04	-	rw

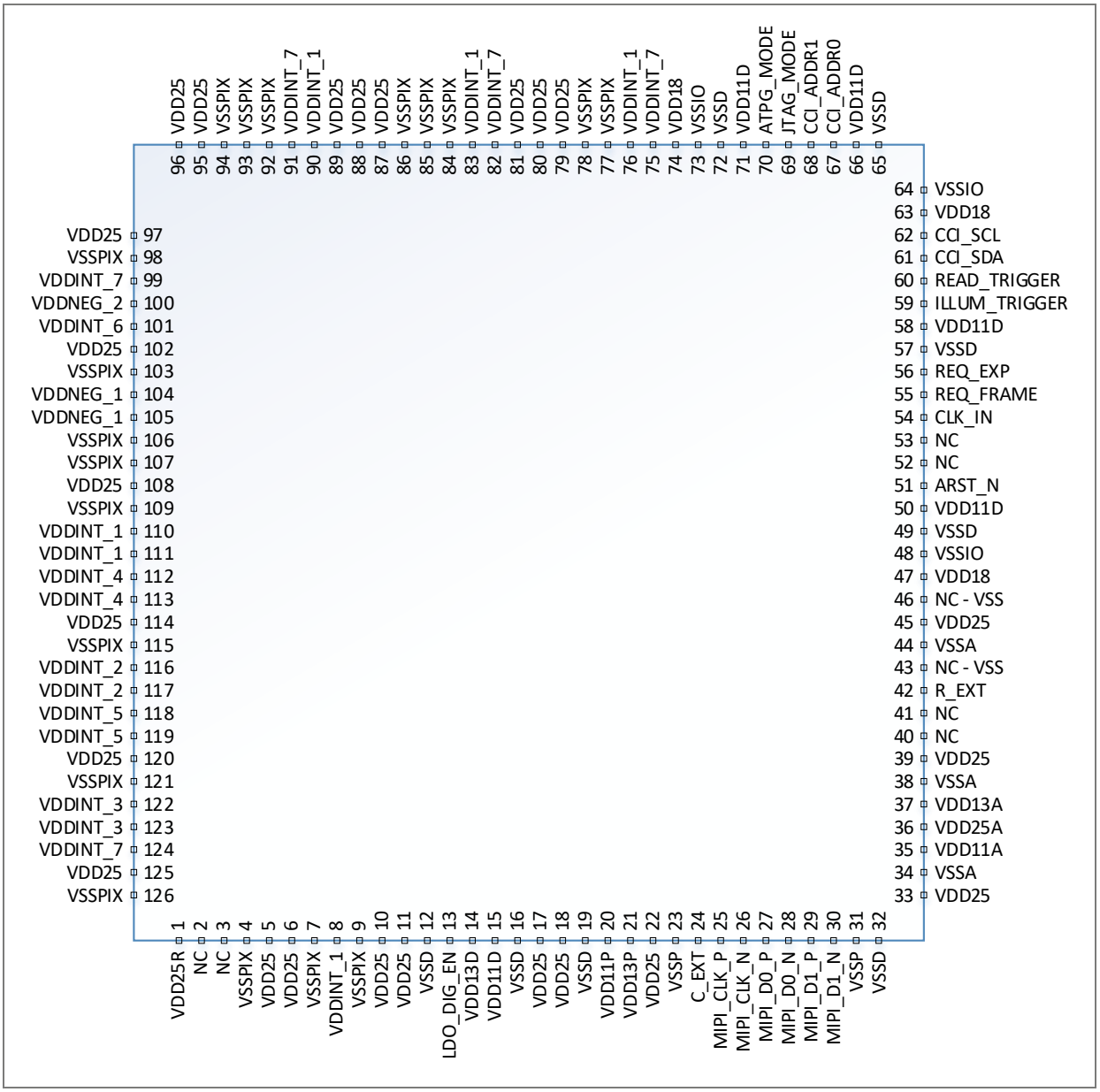
Addr	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	Default	Fixed	Type
0x2091	TEST_PATTERN_CFG							TEST_PATTERN_CFG	0x00	-	rw
0x2098	HSIZE_B								0x20	-	rw
0x2099	-	-	-	-	-	-	HSIZE_B		0x03	-	rw
0x209A	HSTART_B								0x40	-	rw
0x209B	-	-	-	-	-	-	HSTART_B		0x00	-	rw
0x209C	-	-	-	-	-	-	-	HFLIP	0x00	-	rw
0x209D	-	-	-	-	-	-	-	HFLIP_B	0x00	-	rw
0x209E	-	-	-	-	-	BIT_DEPTH			0x02	-	rw
0x24DC	-	-	DC_CFG		-	-	DC_CFG		0x01	-	rw
0x24DD	-	-	-	-	DC_LIMIT_LOW				0x00	-	rw
0x24DE	-	-	-	-	DC_LIMIT_HIGH				0x00	-	rw
0x24DF	-	-	-	-	-	-	-	DC_LIMIT_HIGH_MODE	0x00	-	rw
0x3188	TSENS_SIG								0x00	-	ro
0x3189	-	-	-	-	TSENS_SIG				0x00	-	ro
0x318E	TSENS_RST								0x00	-	ro
0x318F	-	-	-	-	-	-	TSENS_RST		0x00	-	ro
0x4006	-	-	-	-	BSP				0x0F	-	rw
0x4007	REG_READOUT_POWER_SAVING								0x00	-	rw
0x401C	-	-	-	-	REG_READOUT_POWER_SAVING				0x5F	0x6F	rw
0x5004	-	-	MIPI_SOFT_RESET						0x00	-	rw
0x5006	-	-	-	MIPI_PWR_DWN	-	-	-	MIPI_PWR_DWN	0x10	-	rw
0x5011	-	-	-	-	-	MIPI_RST_CFG			0x33	-	rw
0x5013	-	-	-	-	-	-	-	PLL_LOCK_CNT_RST	0x00	-	strobe
0x5015	PLL_LOCK_RISE_CNT								0x01	-	ro
0x5016	PLL_LOCK_FALL_CNT								0x00	-	ro
0x5099	-	-	-	MIPI_VCTRL					0x00	-	rw
0x50D9	-	-	-	-	-	DPDN_SWAP			0x00	-	rw
0x50DC	-	-	-	-	-	-	PLL_STATUS		0x00	-	ro
0x6001	TINIT								0x07	-	rw
0x6002									0xD8	-	rw
0x6003	-	-	-	-	-	-	-	INIT_SKEW_EN	0x01	-	rw
0x6004	INIT_SKEW								0x7A	-	rw
0x6005									0x12	-	rw
0x6006	-	-	-	-	-	-	-	TX_CTRL_EN	0x00	0x01	rw
0x6010	-	-	-	-	-	-	FRAME_MODE		0x00	-	rw
0x6011	-	-	-	-	-	POLARITY			0x00	-	rw
0x6012	-	-	-	-	-	-	-	LANE	0x00	-	rw
0x6013	-	-	-	-	-	-	-	CLK_MODE	0x00	-	rw

Addr	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	Default	Fixed	Type
0x6014	-	-	-	-	-	-	ULPS		0x00	-	rw
0x6015	-	-	-	-	ULPS				0x00	-	rw
0x6016	FRAME_COUNTER								0x00	-	rw
0x6017									0x3C	-	rw
0x6018	-	-	-	-	-	-	INTERRUPT_EN		0x00	-	rw
0x6019	-	-	-	-	-	-	INTERRUPT_STATUS		0x00	-	ro
0x601C	-	-	-	-	-	-	-	SKEW_CAL_EN	0x00	-	rw
0x601D	-	-	-	-	SKEW_COUNT				0x02	-	rw
0x601E	SKEW_COUNT								0x00	-	rw
0x601F	-	-	-	-	-	-	-	SCRAMBLING_EN	0x00	-	rw
0x6037	-	-	-	-	LINE_COUNT_RAW				0x0F	-	rw
0x6038	LINE_COUNT_USER_DEF								0xFF		rw
0x6039	-	-	-	-	-	-	-	LINE_COUNT_EMB	0x01	-	rw
0x6065	TWAKE_TIMER								0x4F	-	rw
0x6066									0x00	-	rw

10 Pin and package information

10.1 Bare die pin diagram

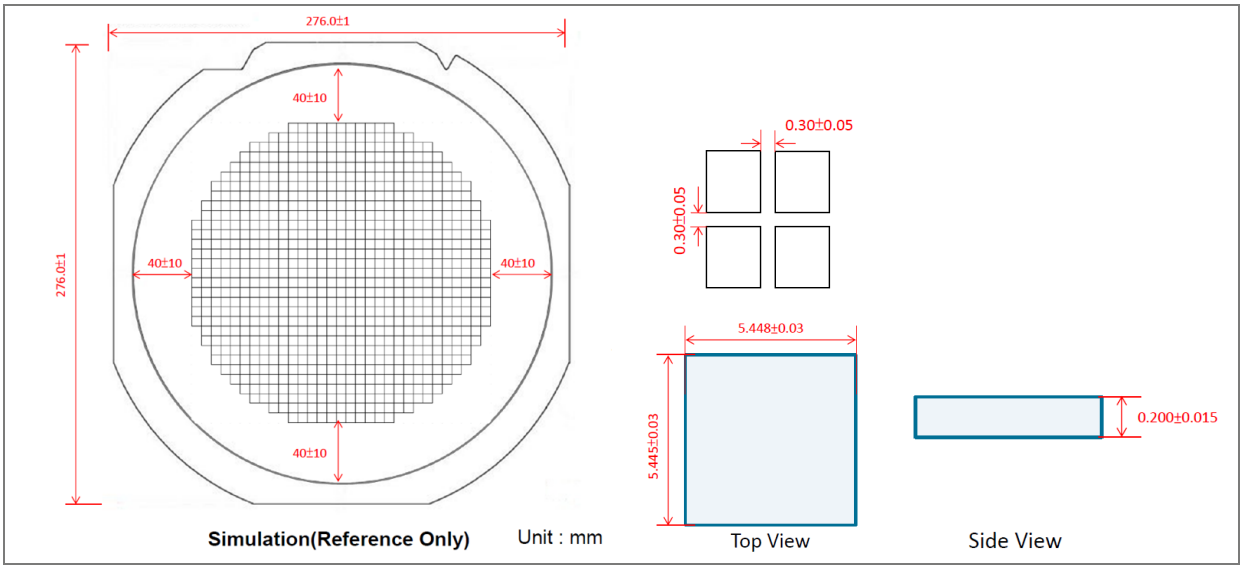
Figure 32: Bare die pin diagram (Top View)



(1) NC: No connect.

10.2 Reconstructed wafer dimensions (Bare Die)

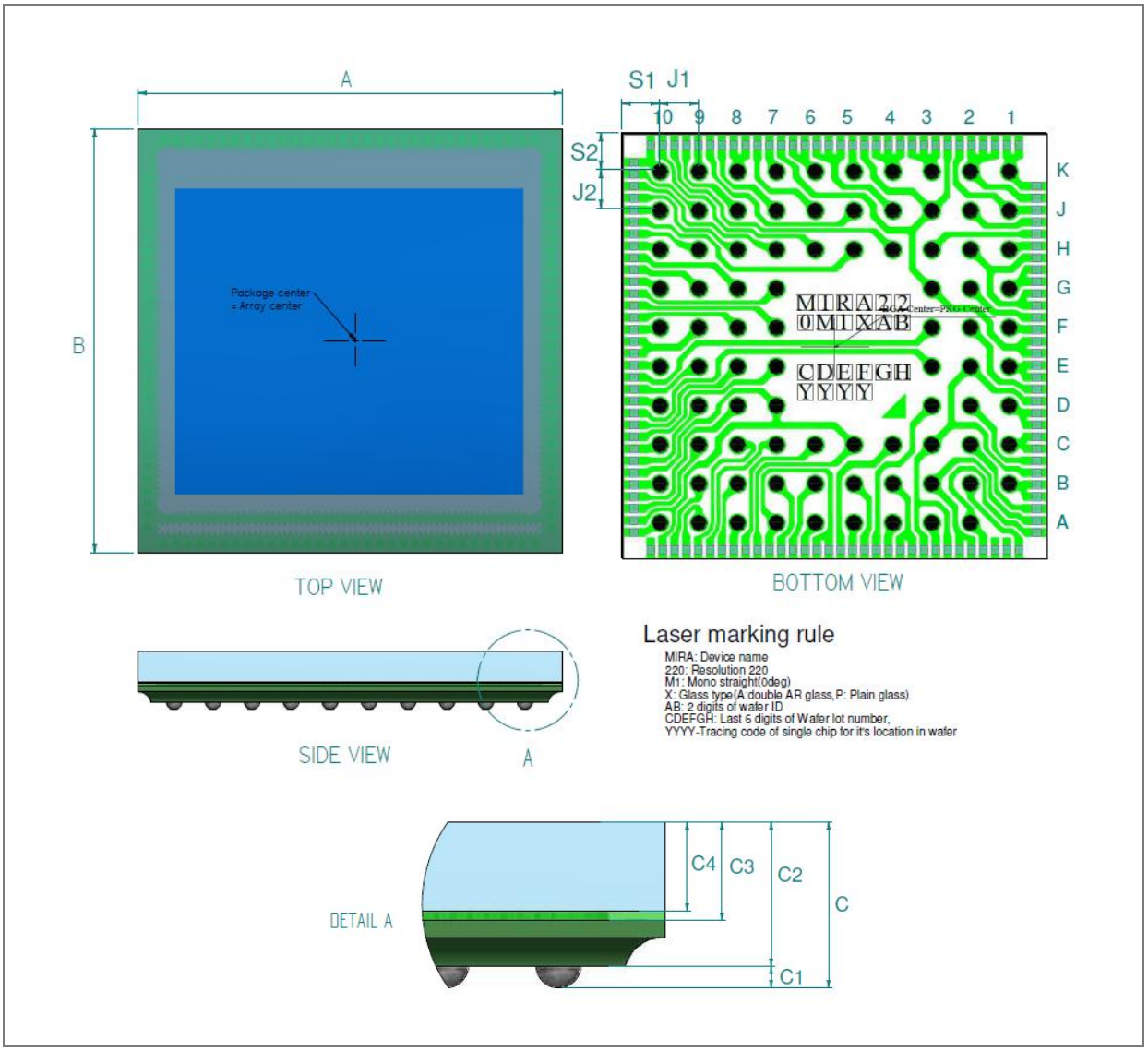
Figure 33: RW physical dimensions



10.3 CSP package information

For the orientation of the pixel array in relation to the pin-1A location, see section 8.2.4.

Figure 34: CSP package outline drawing



Attention:

The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” Use of underfill is highly recommended to ensure board level reliability requirements are met if components are mounted on an application PCB. Due to the small pad pitch, standard reflow process may need to be adjusted to achieve reliable solder result.

Table 40: CSP pin diagram (Top View)

	1	2	3	4	5	6	7	8	9	10
K	VDD25	VSSPIX	VDD25	VSSPIX	VDD_INT_7	VSSPIX	VDD_INT_7	VSSD/ VSSIO	JTAG_ MODE	VSSD/ VSSIO
J	VDDINT_7	VDDNEG_2	VDDINT_1	VDD25	ATPG_ MODE	VDD18	VDD11D	CCI_ ADDR1	VDD18	READ_ TRIGGER
H	VDD25	VSSPIX	VDDINT_6	CCI_ ADDR0	ILLUM_ TRIGGER	VDD11D	CCI_SCL	CCI_SDA	VDD11D	VSSD
G	VDDNEG_1	VDD25	VDDINT_1				NC	REQ_EXP	REQ_ FRAME	CLK_IN
F	VSSPIX	VDD25	NC - VSS				NC	ARST_N	VSSD/ VSSIO	VDD11D
E	VDDINT_4	VSSPIX	NC - VSS				NC	R_EXT	VDD25	VDD18
D	VDDINT_2	VDD25	LDO_DIG_ EN				VSSP/ VSSA	VDD25A	VDD25	VSSA
C	VDDINT_5	VDDINT_7	VSSPIX	VSSD	VSSP/ VSSA	C_EXT	MIPI_D0_P	MIPI_D0_N	VDD11A	NC
B	VDDINT_3	VDD25R	VDD25	VDD25	VDD13D	VDD11P	VDD13P	MIPI_ CLK_N	MIPI_D1_N	VDD13A
		VSSPIX	VDDINT_1	VSSD	VDD11D	VSSD	VDD25	MIPI_ CLK_P	MIPI_D1_P	VDD25

Table 41: CSP dimension information

Symbol	Description	Min [mm]	Typ [mm]	Max [mm]	Min [in]	Typ [in]	Max [in]
A	Package body dimension X	5.4226	5.4476	5.4726	0.21349	0.21447	0.21546
B	Package body dimension Y	5.4198	5.4448	5.4698	0.21338	0.21436	0.21535
C	Package height	0.6795	0.7395	0.7995	0.02675	0.02911	0.03148
C1	Ball height	0.0800	0.1100	0.1400	0.00315	0.00433	0.00551
C2	Package body thickness	0.5995	0.6295	0.6595	0.02360	0.02478	0.02596
C3	Thickness from top glass surface to wafer	0.4300	0.4450	0.4600	0.01693	0.01752	0.01811
C4	Glass thickness	0.3900	0.4000	0.4100	0.01535	0.01575	0.01614
D	Ball diameter	0.1700	0.2000	0.2300	0.00669	0.00787	0.00906
N	Total ball count		87				
J1	Pins pitch X axis		0.500				
J2	Pins pitch Y axis		0.500				
S1	Edge to pin center distance along X	0.4438	0.4738	0.5038	0.01747	0.01865	0.01983
S2	Edge to pin center distance along Y	0.4424	0.4724	0.5024	0.01742	0.01860	0.01978

10.4 Pin description

Table 42: Pin description of Mira220

Pin number		Pin name	Pin type[1]	Description
Bare die	**CSP**			
5, 6, 10, 11, 17, 18, 22, 33, 39, 45, 79, 80, 81, 87, 88, 89, 95, 96, 97, 102, 108, 114, 120, 125	A7, A10, B3, B4, D2, D9, E9, F2, G2, H1, J4, K1, K3	VDD25	S	2.5 V external supply
47, 63, 74	E10, J6, J9	VDD18	S	1.8 V external supply
14	B5	VDD13D	S	1.35 V external supply
21	B7	VDD13P	S	1.35 V external supply
37	B10	VDD13A	S	1.35 V external supply
1	B2	VDD25R	S	2.5 V external supply
36	D8	VDD25A	S	2.5 V external supply
15, 50, 58, 66, 71	A5, F10, H6, H9, J7	VDD11D	A	Internal supply
35	C9	VDD11A	A	Internal supply
20	B6	VDD11P	A	Internal supply
8, 76, 83, 90, 110, 111	A3, G3, J3	VDDINT_1	S	2.5 V external supply
116, 117	D1	VDDINT_2	A	Internal supply
122, 123	B1	VDDINT_3	A	Internal supply
112, 113	E1	VDDINT_4	A	Internal supply
118, 119	C1	VDDINT_5	A	Internal supply
101	H3	VDDINT_6	A	Internal supply
75, 82, 91, 99, 124	C2, J1, K5, K7	VDDINT_7	A	Internal supply
100	J2	VDDNEG_2	A	Negative internal supply
104, 105	G1	VDDNEG_1	A	Negative internal supply
34, 38, 44	C5, D7, D10	VSSA	G	Ground
12, 16, 19, 32, 49, 57, 65, 72	A4, A6, C4, F9, H10, K8, K10	VSSD	G	Ground
23, 31	C5, D7	VSSP	G	Ground
48, 64, 73	F9, K8, K10	VSSIO	G	Ground
4, 7, 9, 77, 78, 84, 85, 86, 92, 93, 94, 98, 103, 106, 107, 109, 115, 121, 126	A2, C3, E2, F1, H2, K2, K4, K6	VSSPIX	G	Ground
42	E8	R_EXT	A	Bias resistor connection
24	C6	C_EXT	A	Internal supply
54	G10	CLK_IN	DI	Reference clock
67	H4	CCI_ADDR0	DI	CCI device address bit 0
68	J8	CCI_ADDR1	DI	CCI device address bit 1
61	H8	CCI_SDA	DIO	CCI interface data lane

Pin number		Pin name	Pin type(1)	Description
62	H7	CCI_SCL	DIO	CCI interface clock lane
25	A8	MIPI_CLK_P	HSO	MIPI clock lane P
26	B8	MIPI_CLK_N	HSO	MIPI clock lane N
27	C7	MIPI_D0_P	HSO	MIPI data lane 0 P
28	C8	MIPI_D0_N	HSO	MIPI data lane 0 N
29	A9	MIPI_D1_P	HSO	MIPI data lane 1 P
30	B9	MIPI_D1_N	HSO	MIPI data lane 1 N
69	K9	JTAG_MODE	DI	Not used. Connect to ground
70	J5	ATPG_MODE	DI	Not used. Connect to ground
55	G9	REQ_FRAME	DI	Request Frame
56	G8	REQ_EXP	DI	Request Exposure and Frame
59	H5	ILLUM_TRIGGER	DO	Illumination trigger signal
60	J10	READ_TRIGGER	DO	Readout trigger signal
51	F8	ARST_N	DI	Asynchronous hard reset pin
13	D3	LDO_DIG_EN(2)	DI	Digital LDO (VDD11D) enable
40, 41, 52, 53	C10, E7, F7, G7	No connect	NC	Should be left open
43, 46	E3, F3	No connect - VSS	NC	Connect to ground
2, 3	/	No connect	NC	Should be left open

(1) Explanation of abbreviations:

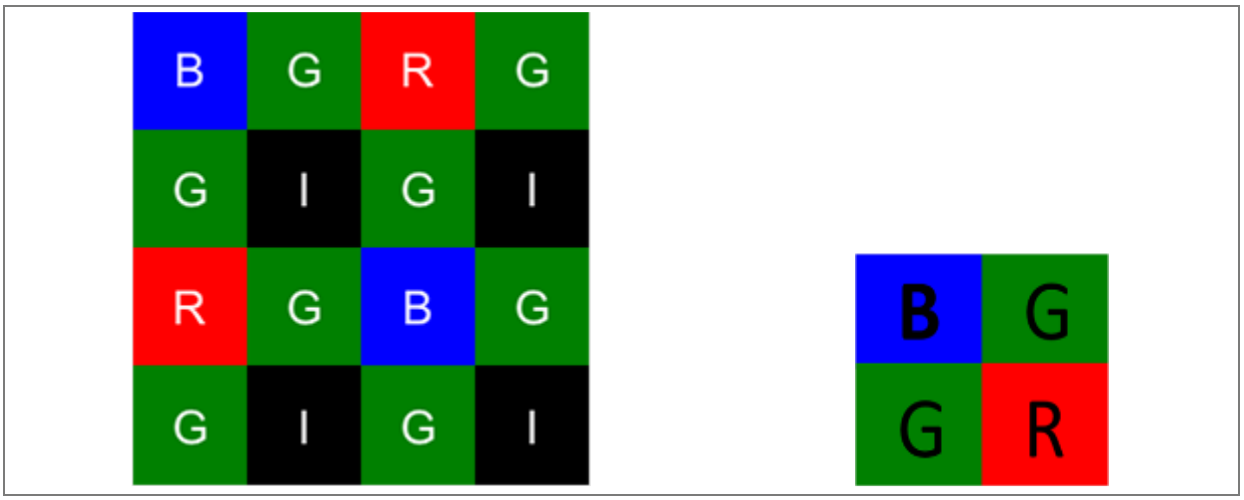
S	Supply
G	Ground
DI	Digital Input
DO	Digital Output
DIO	Digital Input-Output
A	Analog reference
HSO	High Speed Output
NC	No connect

(2) Optional, can be left unconnected. Internal pull-up to VDD25.

11 Color filter information

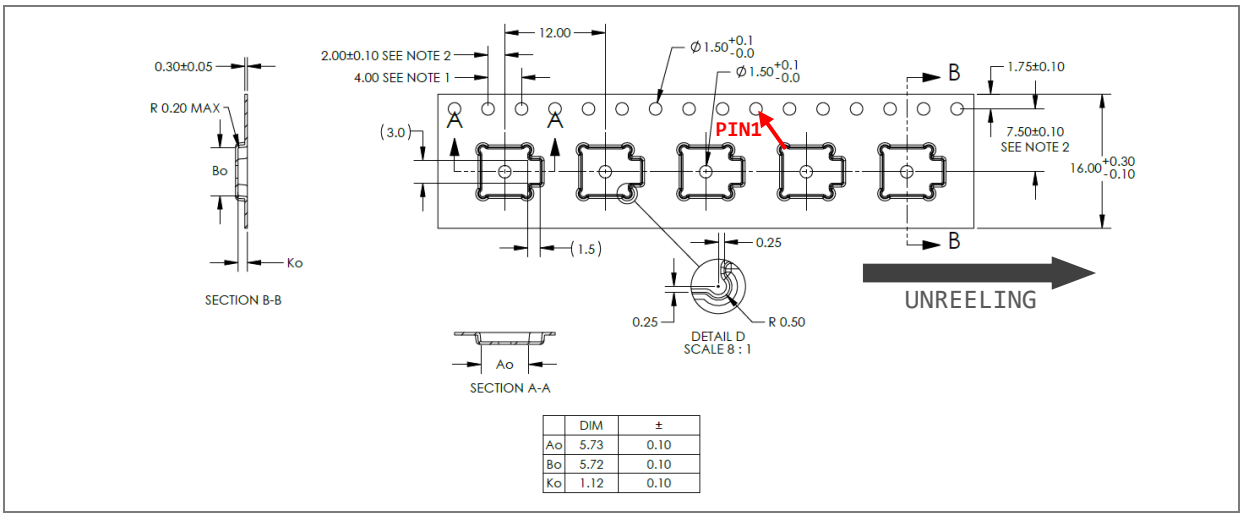
The following figure shows the color filter configuration used on the Mira220 both for RGB and RGBIR versions of the sensor. The first readout pixel is highlighted below.

Figure 35: Color filter configurations for RGBIR (left) and RGB (right)



12 Tape & reel information

Figure 36: Tape and reel dimensions (for CSP only)



	DIM	±
Ao	5.73	0.10
Bo	5.72	0.10
Ko	1.12	0.10

(1) 10 sprocket hole pitch cumulative tolerance ±0.2
(2) Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
(3) Ao and Bo are measured on a plane at a distance "R" above the bottom of the pocket.
(4) All dimensions are in millimeters.

13 Appendix

13.1 Reference documents

Table 43: Referenced documents

Reference	Document title	Revision / Date
[CSI-2-v1.3]	MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2)	1.3
[DPHY-v1.2]	MIPI Alliance Specification for D-PHY	1.2
[I2C-v6]	I²C bus specification and user manual www.nxp.com/docs/en/user-guide/UM10204.pdf	v6 / April 2014

13.2 Glossary

Table 44: Glossary

Abbreviation	Definition
ACK	Acknowledge
ADC	Analog to Digital Convertor
AR	Augmented Reality
BSI	Back-Side Illumination
BSP	Black Sun Protection
CCI	Camera Control Interface
CDS	Correlated Double Sampling
CMOS	Complementary Metal-Oxide Semiconductor
CRA	Chief Ray Angle
CRC	Cyclic Redundancy Check
CS	Checksum
CSI	Camera Serial Interface
CSP	Chip Scale Package
DC	Dark Current
DCDT	Dark Current Doubling Temperature
DCDS	Digital Correlated Double Sampling
D-PHY	MIPI Physical Layer Protocol
DR	Dynamic Range
DSNU	Dark Signal Non Uniformity
DTN	Dark Temporal Noise
ECC	Error Correction Code
EOF	End of Frame
EOI	End of Integration
EOL	End of Line
ESD CDM	Electrostatic Discharge Charge Device Model
ESD HBM	Electrostatic Discharge Human Body Model
FE	Frame End
FPS	Frames per Second
FS	Frame Start
FWC	Full Well Capacity
GLOB	Closing global shutter state by sampling all integrated pixel values
HS	High Speed
IO	Input-Output
LP	Low Power
LS	Line Start

Abbreviation	Definition
LSB	Least Significant Bit
MIPI	Mobile Industry Processor Interface
MP	Megapixel
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
NACK	Not Acknowledge
NIR	Near Infrared
OTP	One Time Programmable
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PLS	Parasitic Light Sensitivity
PRNU	Pixel Response Non-Uniformity
QE	Quantum Efficiency
RH	Relative Humidity
RMS	Root Mean Square
RNC	Row Noise Correction
ROI	Region of Interest
RW	Reconstructed Wafer
SCL	Serial Clock
SDA	Serial Data
SNR	Signal-to-Noise Ratio
SOF	Start of Frame
SOI	Start of Integration
ULPS	Ultra-Low Power State
VC	Virtual Channel
VPTAT	Voltage Proportional to the Temperature
VR	Virtual Reality

14 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Changes from previous released version to current revision v9-00	Page
Corrected description of Table 40	82

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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