





ECE532 Project: Linear Programming Solver

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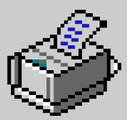



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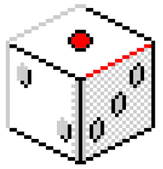
Topics Covered

What are we doing?

Proposed System and Progress



Challenges so far

What’s left to do?

Start

What are we doing?

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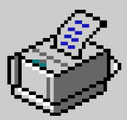
Implement a linear programming solver on an FPGA

Solve such problems using an implementation of the Simplex Method



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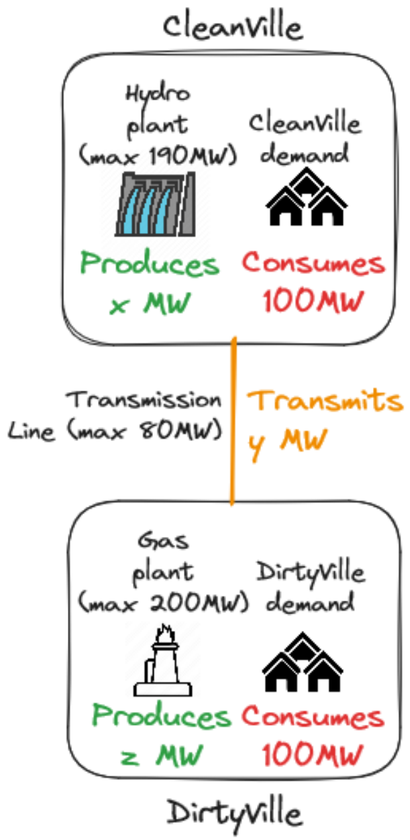
Minimize Costs of Electricity Grids

The Electricity Grid



The Equivalent Linear Program

Minimize cost:

$$30 * x + 50 * z$$

Such that:

CleanVille's power is balanced

$$x - y = 100$$

DirtyVille's power is balanced

$$y + z = 100$$

The hydro plant operates within its limits

$$0 \leq x \leq 190$$

The gas plant operates within its limits

$$0 \leq z \leq 200$$

The transmission line is within its limits

$$-80 \leq y \leq 80$$

*This is one of many possible models!
Depending on your application you might want to consider transmission losses, intracity distribution networks, etc.

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Proposed System and Progress

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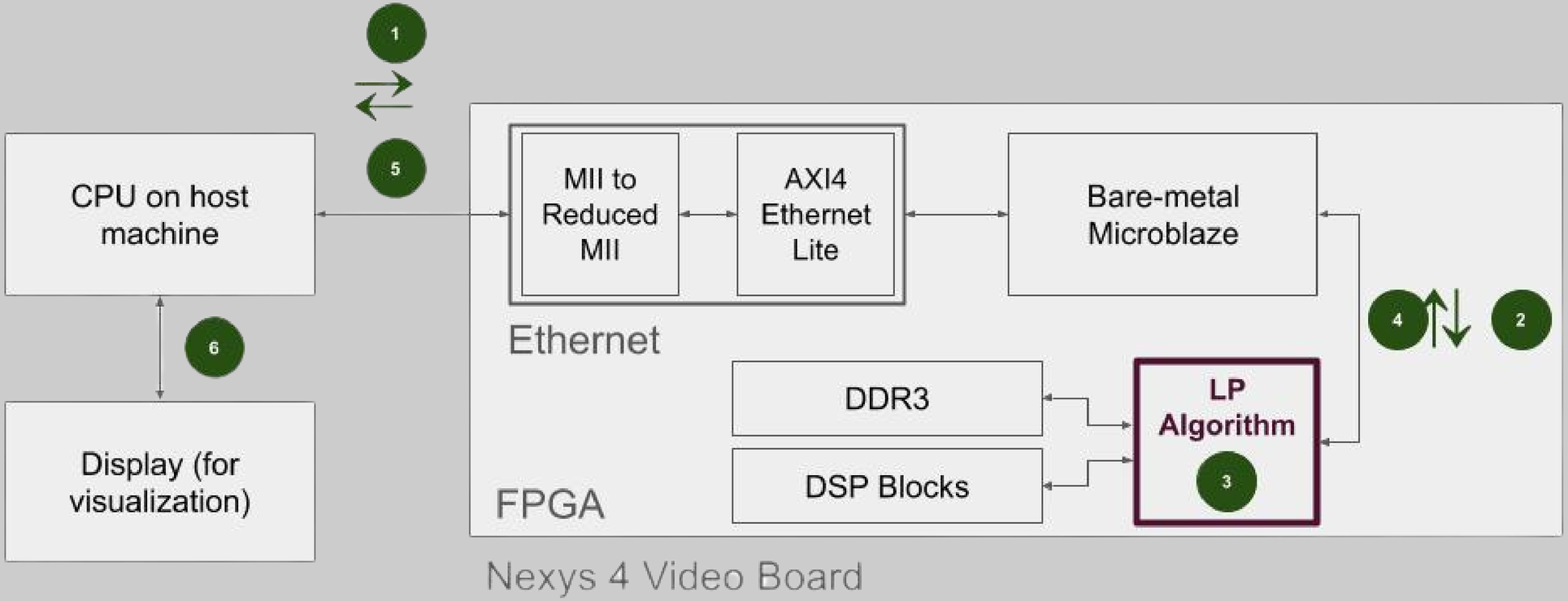
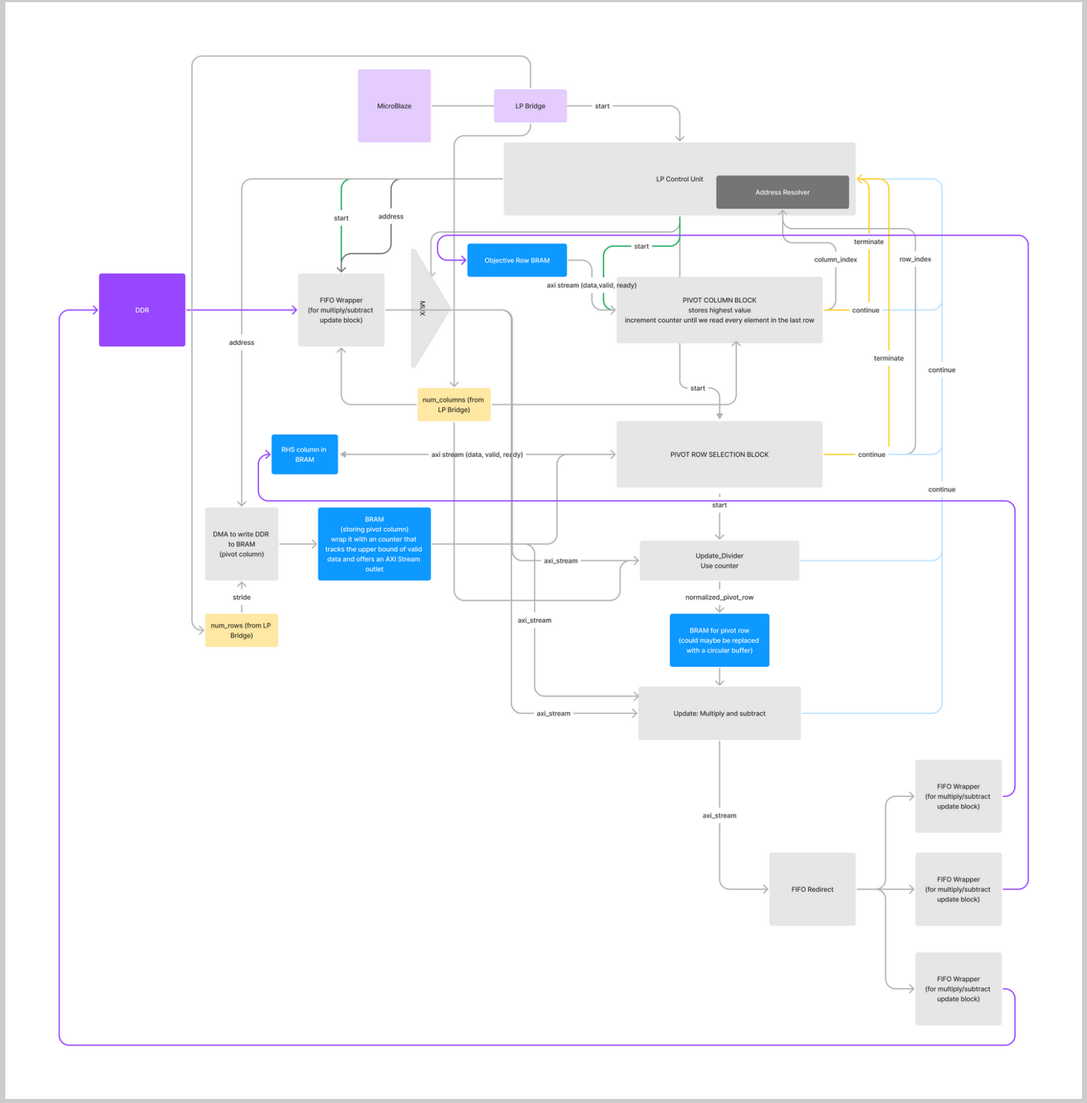
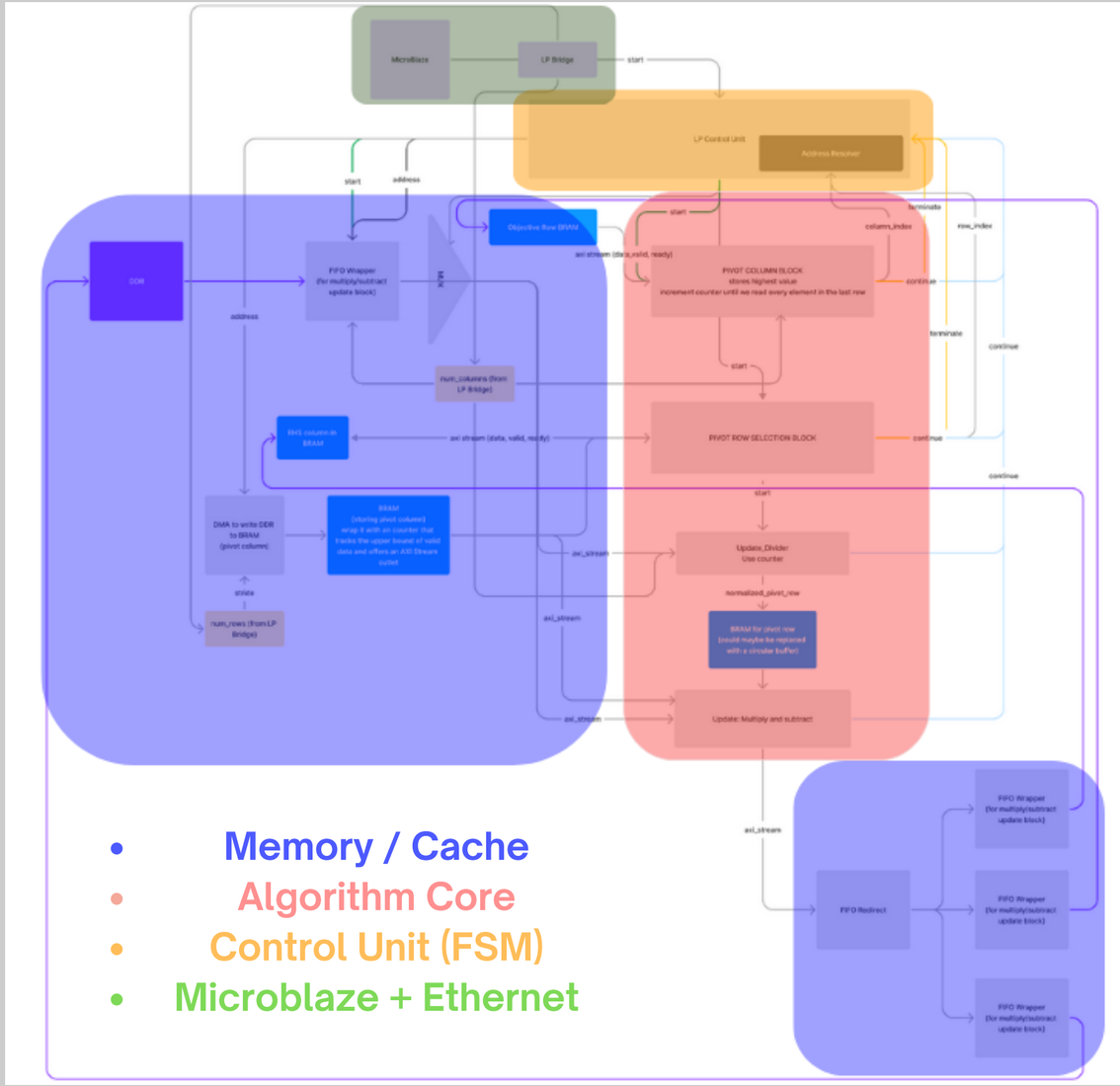
Initial Proposal



Current Proposal - LP Subsystem Link





What we've done

Problem Setup

- Converting real energy model into equations
- Converting equations into standard matrix

Data Transfer

- After setting up tableau:
  a. We send elements over Ethernet
  b. Store them in DDR and other caches
  c. Notify LP control unit (LPC) to start
- We were able to reduce time it takes to send 100MB sample problem from 30m to less than 4m
- Read & write interfaces for memory components with FIFOs to stream in data to/from LP Core Modules.

Control & BRAM

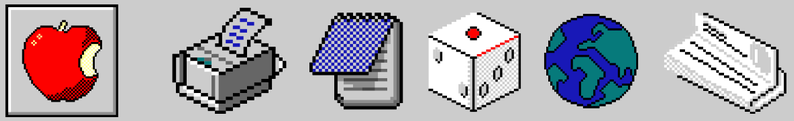
- BRAM blocks for caching data associated with each LP core
- Control Unit to steer data and logic throughout the LP Subsystem
- Initiating DMA data transfers to/from DDR

LP Core Modules

Four modules:

1. Choose pivot column
2. Choose pivot row
3. Update pivot row
4. Update tableau

Software simulation for all modules



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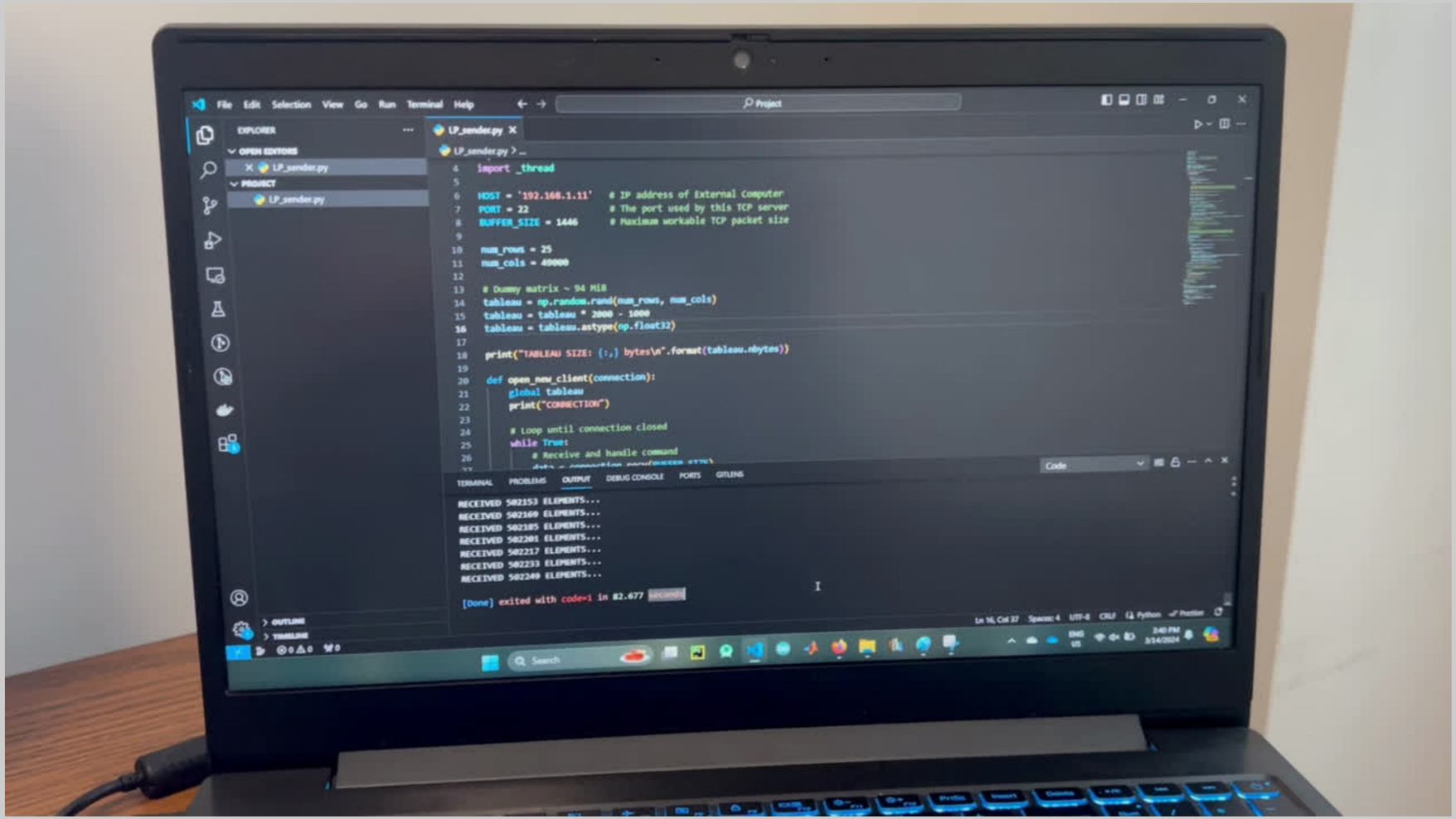
Mid-project demo (video)



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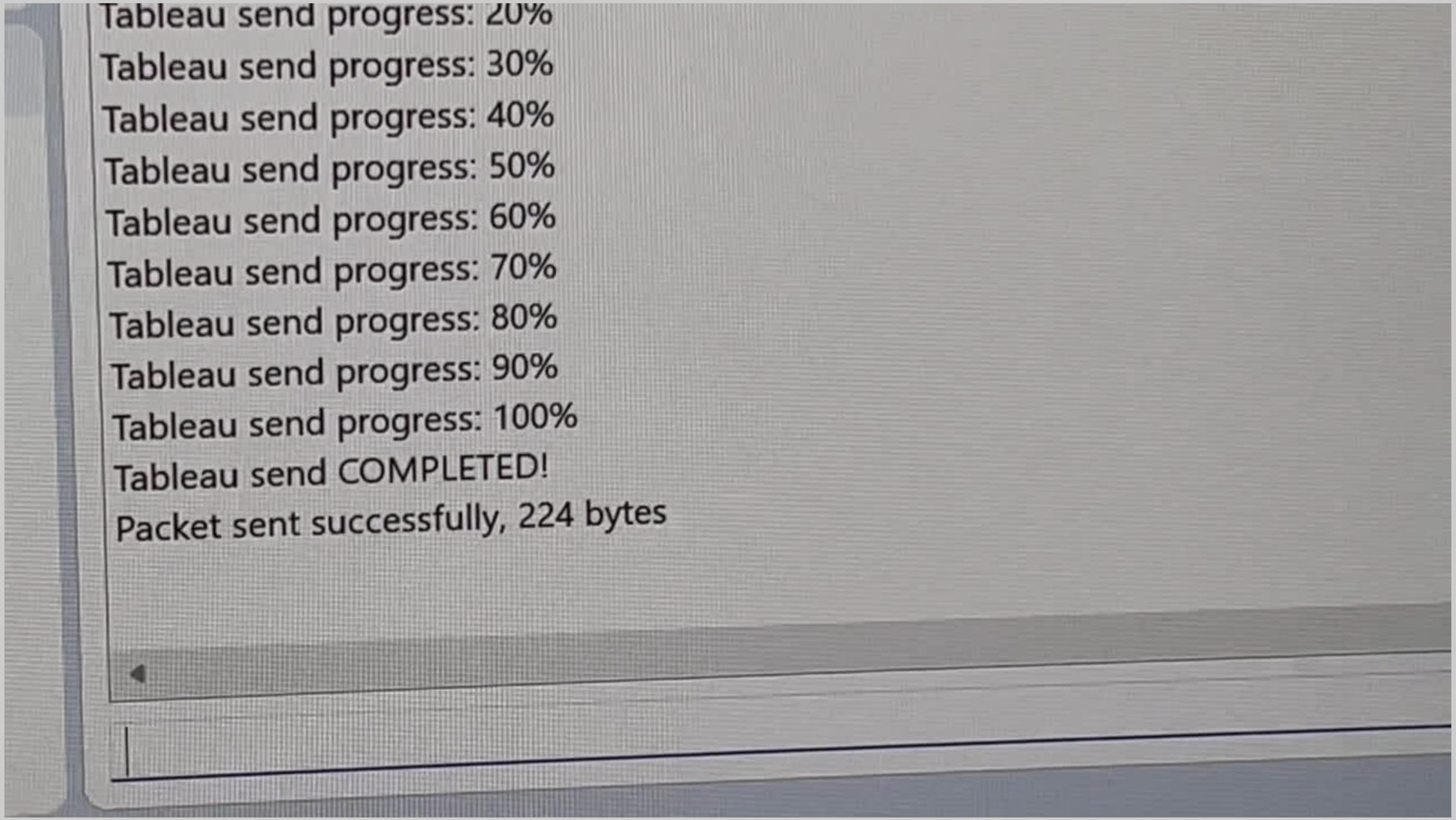

Challenges So Far

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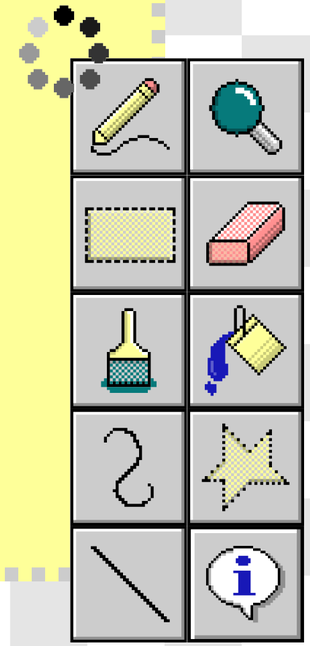


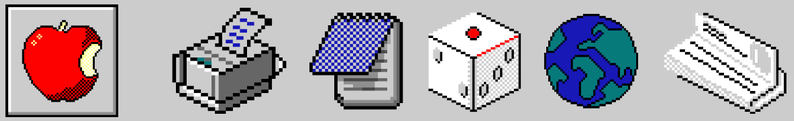
Here's what challenged us...

Adapting Simplex to HW

- Deciding how much can be parallelized
- Replacing high-latency operations e.g. division replaced with multiplication
- Supporting floating point
- Pipelining modules

Memory Interfacing

- A lot of data in flight
- Caching on-chip: Deciding when to write to DDR versus writing to BRAM
- Weird behaviour with simultaneous reading/writing to DDR



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What's Left To Do?

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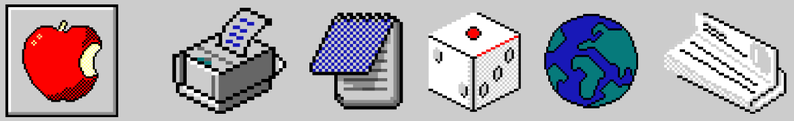
This is what's left...

System Integration/Testing

- We have the ethernet subsystem working, and the LP subsystem is undergoing integration with the ethernet subsystem, control, and LP modules designed
- We are still in progress on some of the LP modules, with testing and integration happening in parallel
- Once all modules have been fully integrated, full-scale testing of the system, synthesis, etc, will follow

GUI Visualization

- As part of our final milestone(s), we wanted to design a GUI to visualize our problem being solved
- With the work being done on the system, these was identified as a stretch goal early on and as of right now, has not been worked on.



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Final Demo Plan: Demonstrate a problem solution in flight

Solve such problems using an implementation of the Simplex Method, and demonstrate visualization capabilities of solution






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Thank you!

All Questions are Welcome!