ECE532 Project: Linear Programming Solver

Adham Ragab, Martin Staadecker, Ahmed Hamoda, Abnash Bassi

Group 1

nda • Agenda • Agenda • Agenda • Agenda • Agenda • Agenda • Agenda • Agenda • Agenda • Agenda • Agenda • Agenda • Ager

Agenda

Topics Covered

Start

What are we doing?

Initial Goals

Final Design & Difficulty Score

Future Work & Demo

What are we doing?

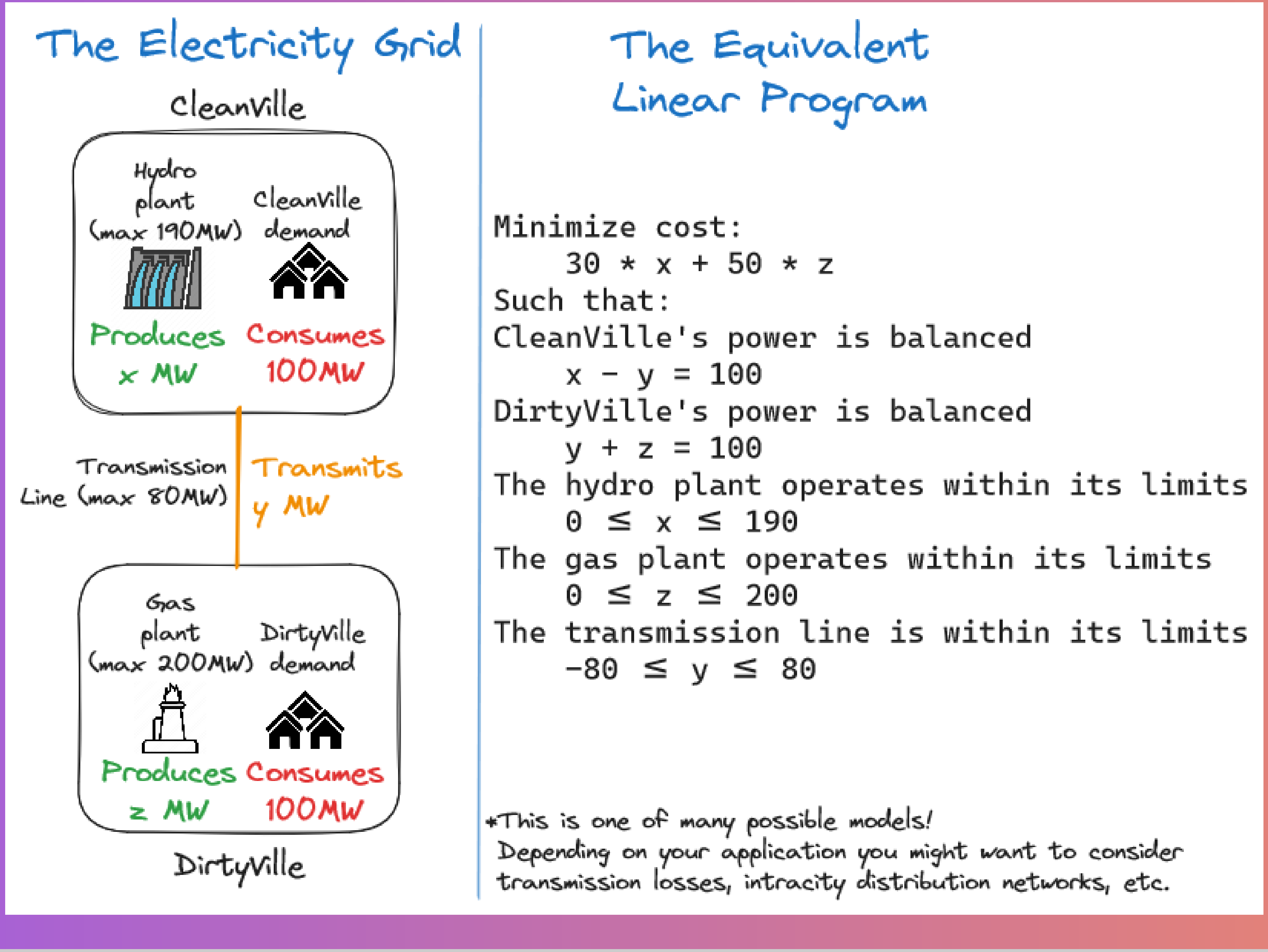
Back to Agenda Page

Implement a linear programming solver on an FPGA

Solve such problems using an implementation of the Simplex Method

Back to Agenda Page

Minimize Costs of Electricity Grids



The Electricity Grid

The Equivalent Linear Program

```
Minimize cost:
    30 * x + 50 * z
Such that:
CleanVille's power is balanced
    x - y = 100
DirtyVille's power is balanced
    y + z = 100
The hydro plant operates within its limits
    0 ≤ x ≤ 190
The gas plant operates within its limits
    0 ≤ z ≤ 200
The transmission line is within its limits
    -80 ≤ y ≤ 80
```

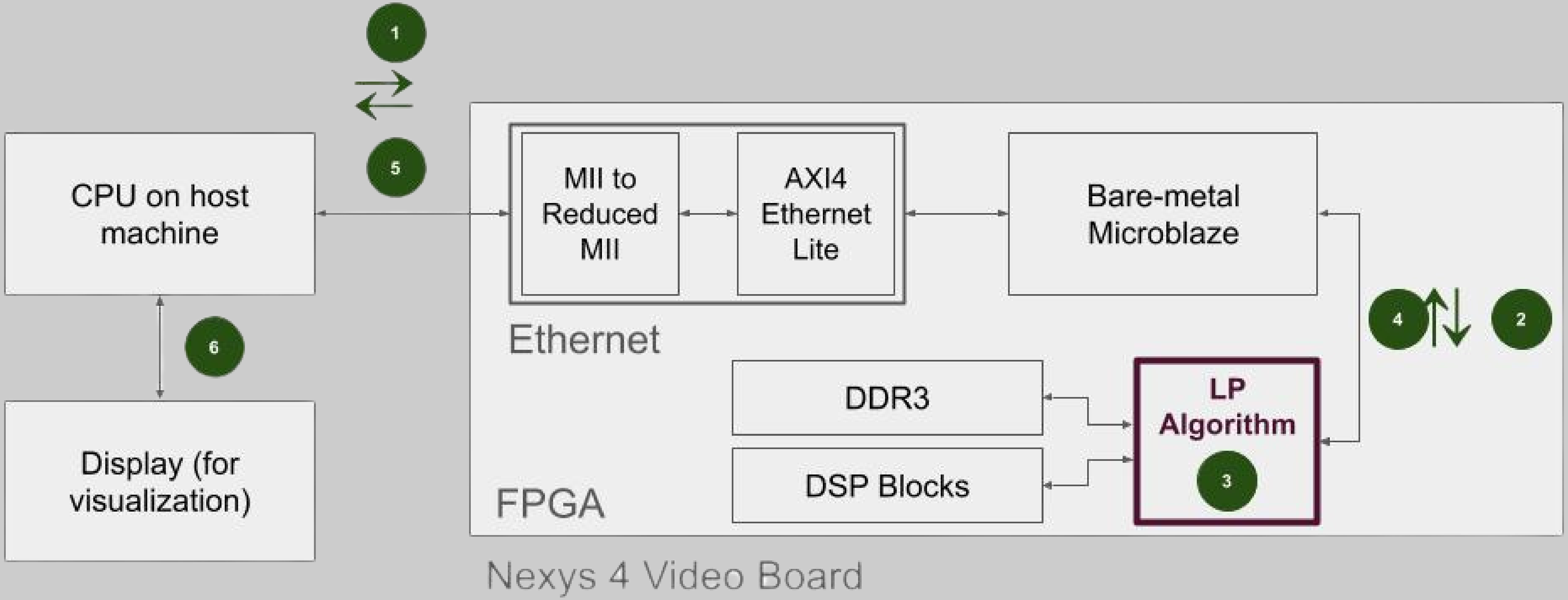
*This is one of many possible models!
Depending on your application you might want to consider transmission losses, intracity distribution networks, etc.

Back to Agenda Page

Initial Proposal

Back to Agenda Page

Initial Proposal



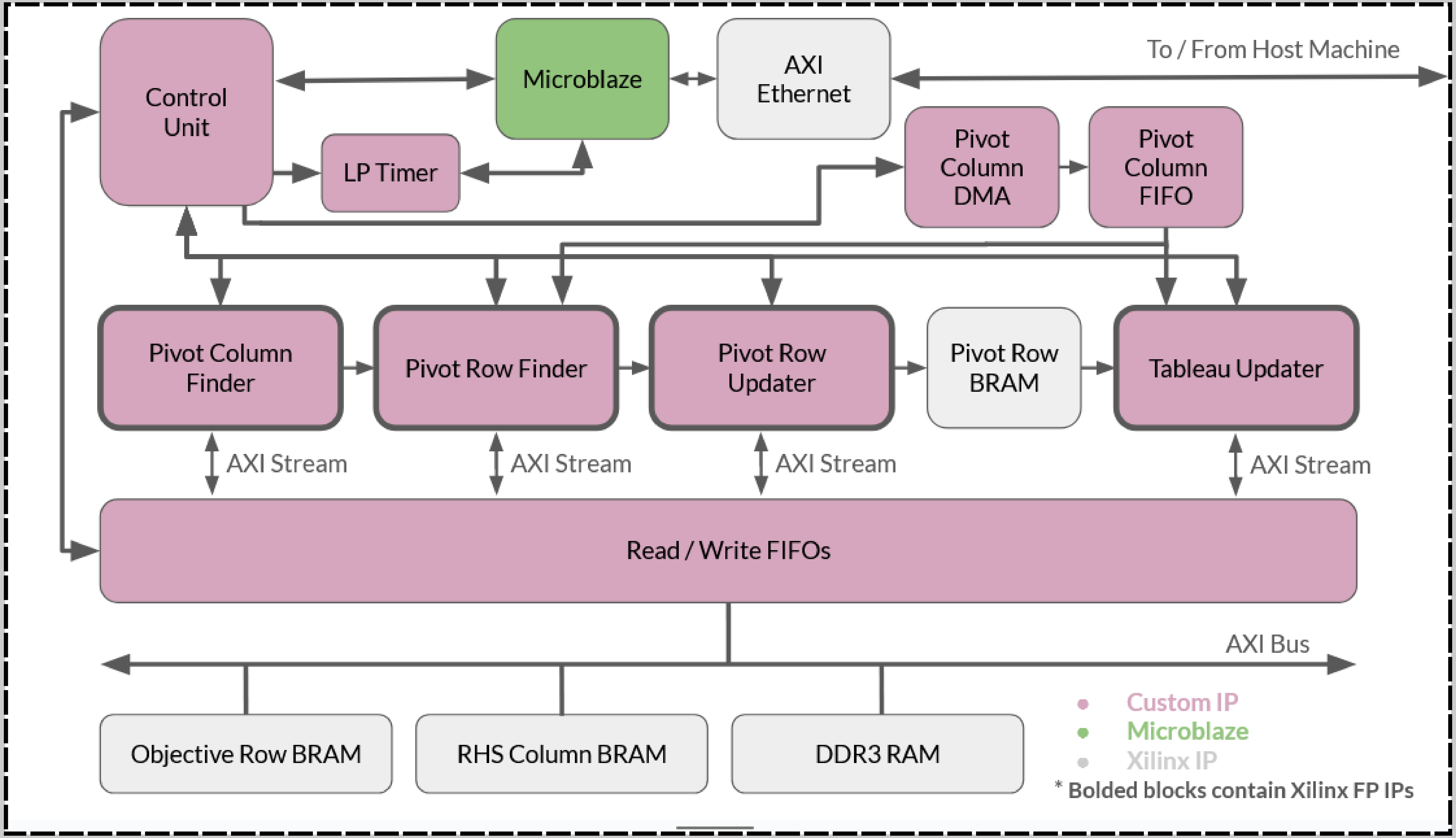
esign • Final Design • Final Design • Final Design • Final Design • Final Design • Final Design • Final Design • Final Design • Final D

Final Design

Back to Agenda Page

nal Design • Final Design • Final Design • Final Design • Final Design • Final Design • Final Design • Final Design • Final Design • F

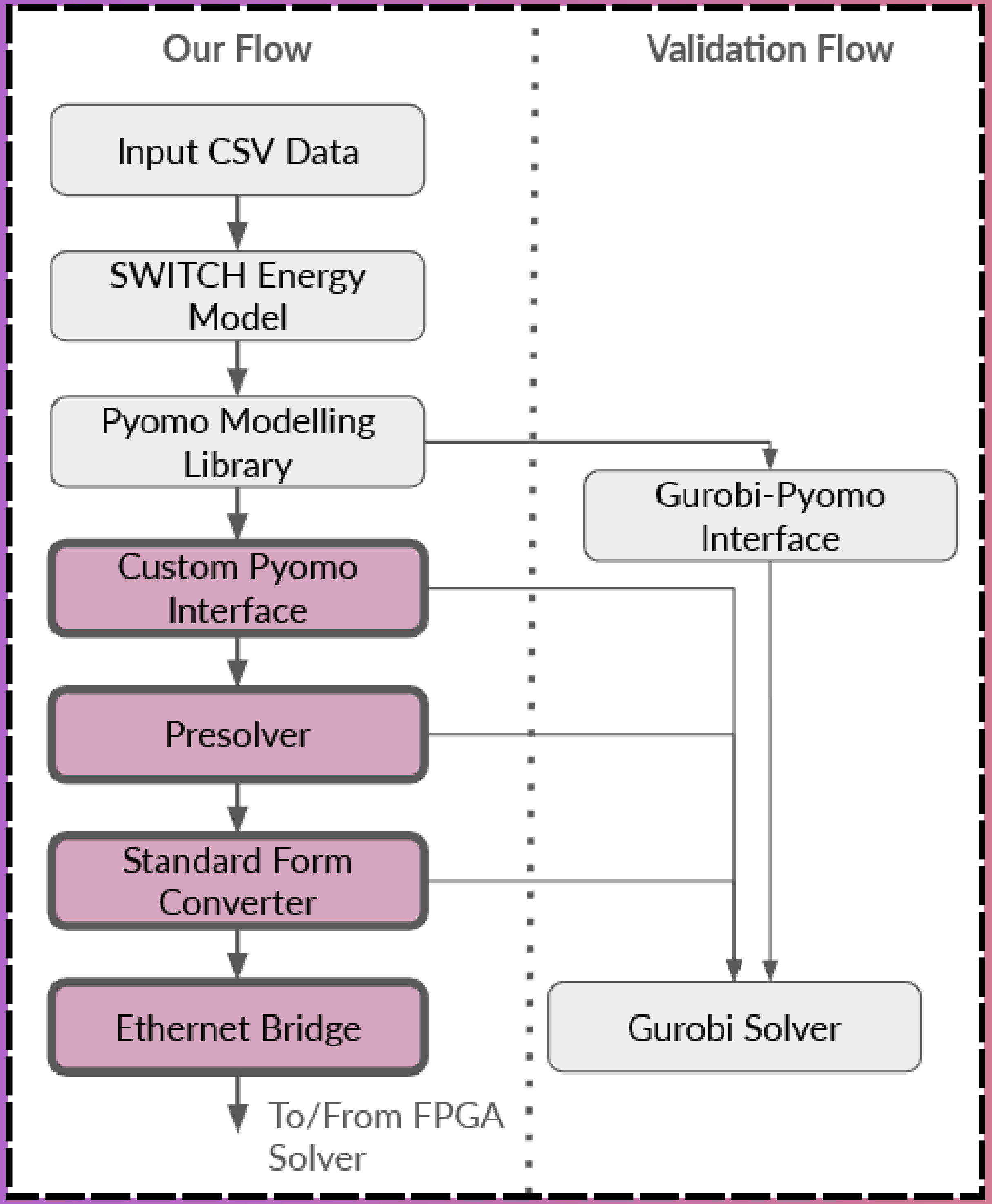
Final Design



Major Components: Problem Setup

Problem Setup

- Converting real energy model into equations
- Converting equations into matrix
- Presolving matrix
- Converting matrix to standard form



Presolver

- Remove empty rows
- Remove unused variables
- Remove variables fixed by constraint
- Remove variables fixed by bounds
- Convert constraints to bounds
- Remove variables by snapping to bound or constraint
- Tighten inequalities to equalities
- Remove equality constraints
- Remove weak constraints

Back to Agenda Page

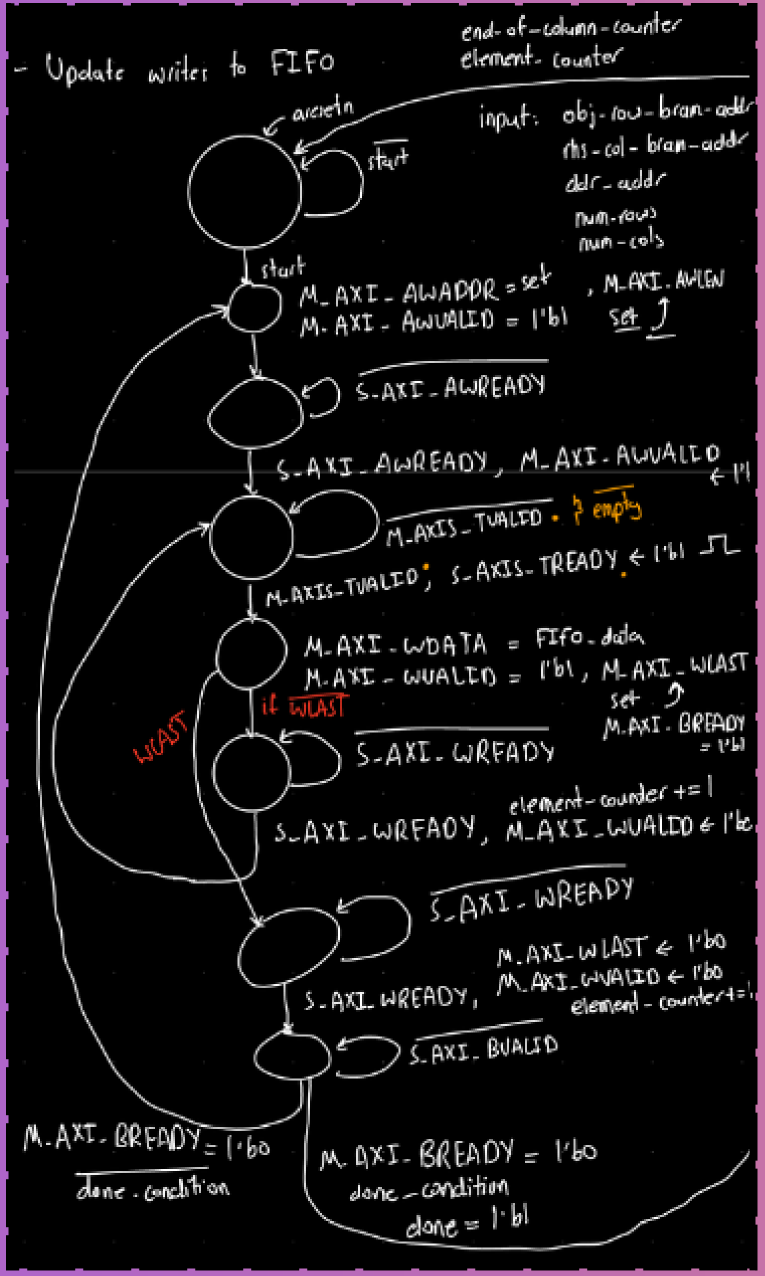
Major Components: Data Transfer

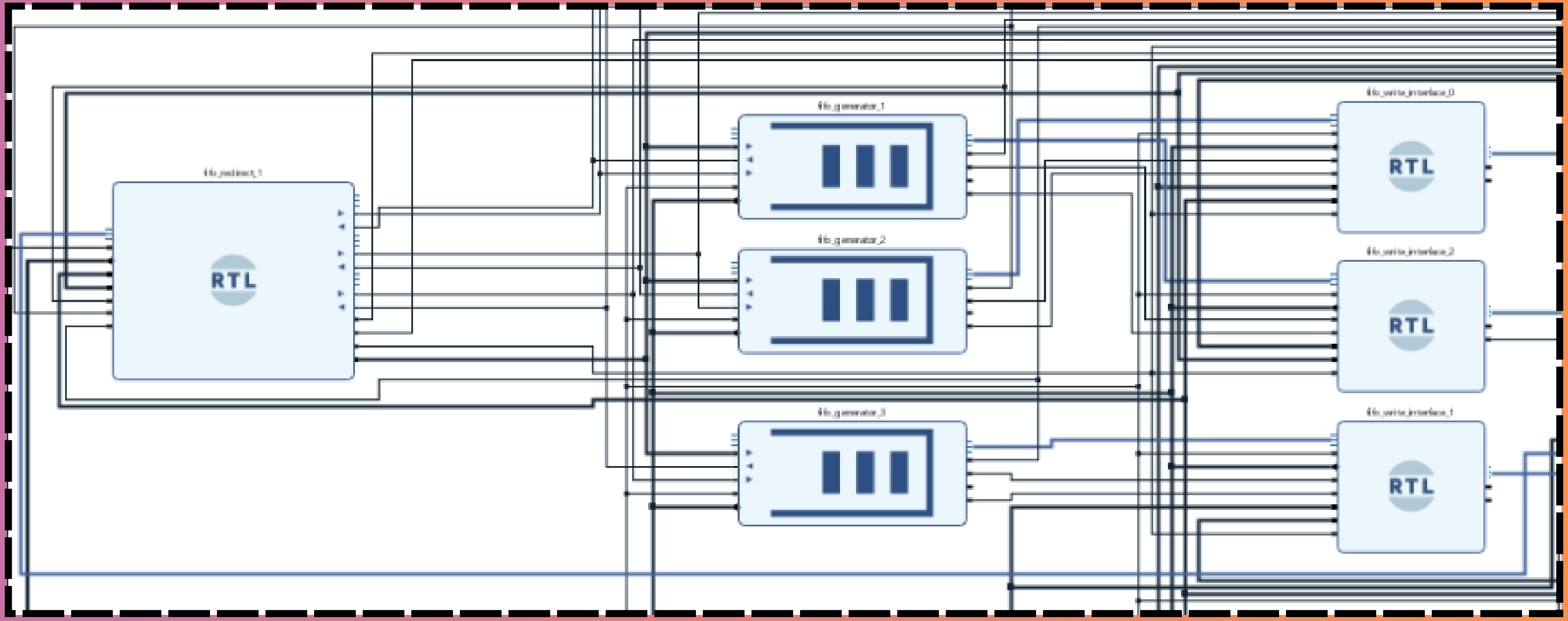
Data Transfer

- After setting up tableau:
    a. We send elements over Ethernet
    b. Store them in DDR and other caches
    c. Notify LP control unit (LPC) to start

- We were able to reduce time it takes to send 100MB sample problem from 30m to less than 4m

- Read & write interfaces for memory components with FIFOs to stream in data to/from LP Core Modules.





Back to Agenda Page

Major Components: Control, Caching, and Buffering

Control

- Control Unit to steer data + logic throughout the LP Subsystem
- Responsible for driving progress from solving core to solving core + data transfer to/from BRAM blocks and DDR

Caching

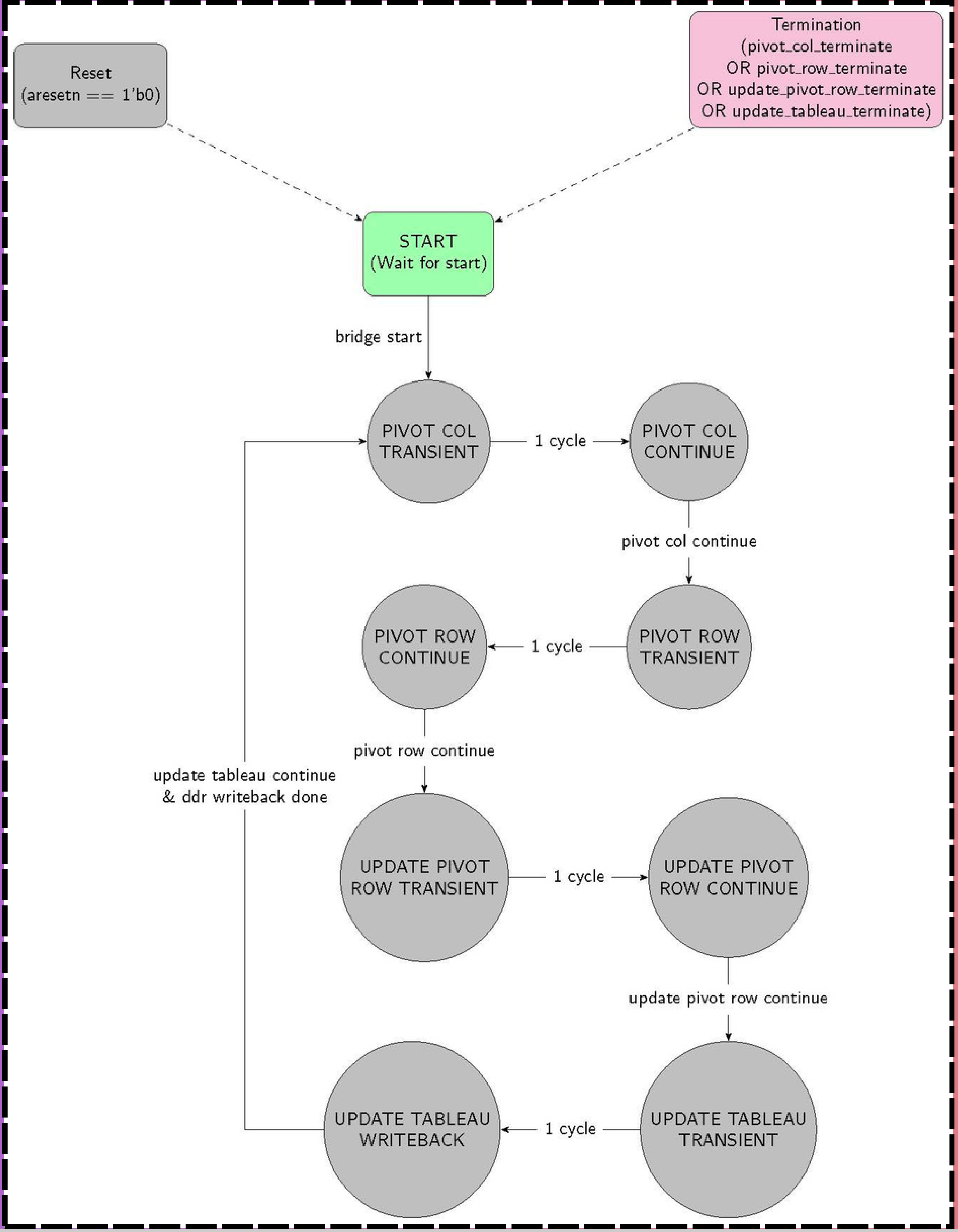
- BRAM blocks to cache rows and cols to use in solving cores without having to fetch from DDR each time

Buffering

- FIFOs for streaming data to/from solving cores
- Ensure cores can start processing data without having to wait for all elements to arrive

Back to Agenda Page

Control Unit Diagram



Back to Agenda Page

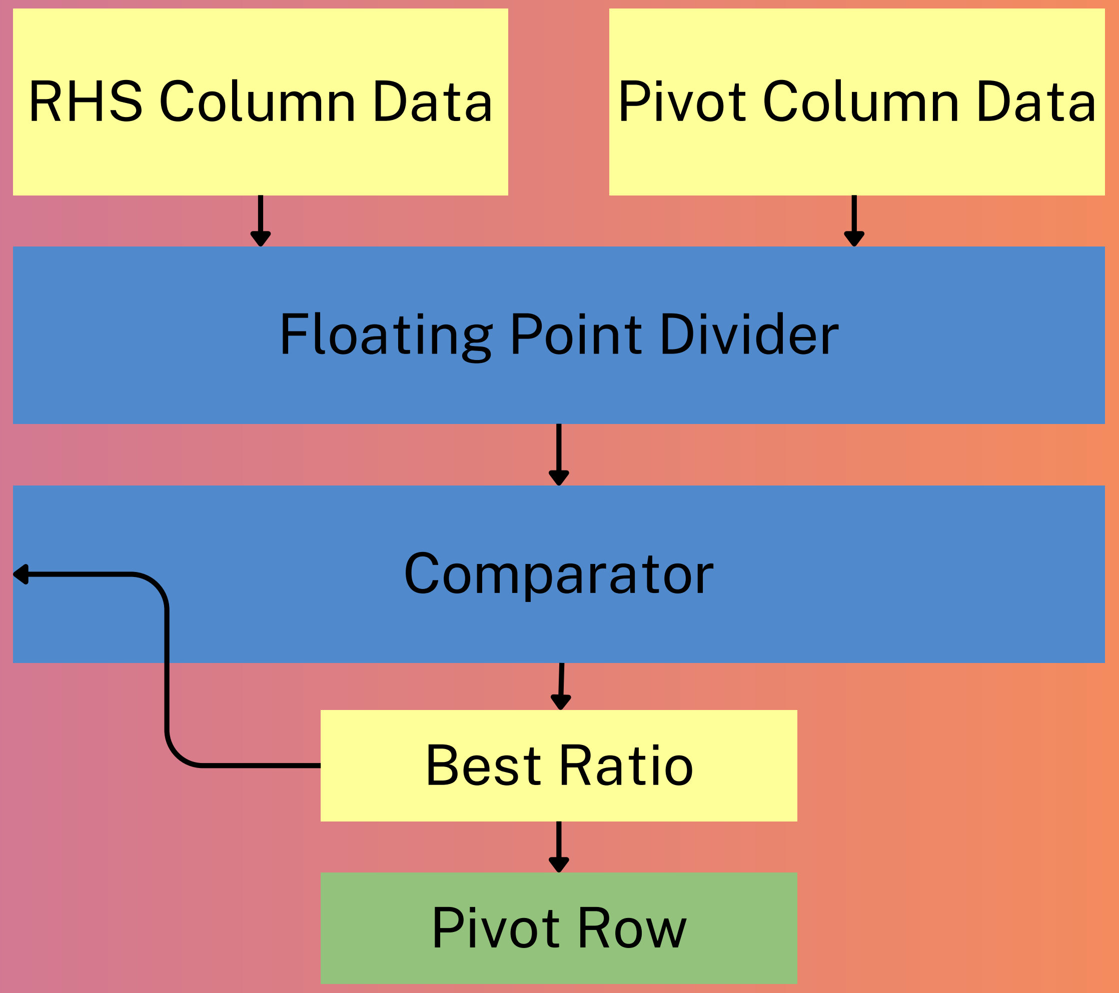
LP Core Modules

Four modules:

1. Choose pivot column
2. Choose pivot row
3. Update pivot row
4. Update tableau

1	2	1	0	0	0	16
1	1	0	1	0	0	9
3	2	0	0	1	0	24
-40	-30	0	0	0	1	0

Choose Pivot Row Module::



RHS Column Data

Pivot Column Data

Floating Point Divider

Comparator

Best Ratio

Pivot Row

Computed Difficulty Score

Component	Complexity Score
Custom LP Algorithm Solver Cores	3.00
Application-Level Ethernet Protocol for Sending/Receiving Data	0.25
LP Control Unit	0.50
Buffering (FIFO) IP Cores	0.75
TOTAL	**4.75**

Back to Agenda Page

Future Work

More Optimized (But Complex) LP Modules

- We designed multi-stage choose_pivot_row module with cross-mult --> too complex for project timeline
- Experiment with other architectures for LP modules
- Try third-party FP IP

Alternative LP Algos

- We implemented Simplex
- Alternative algorithms exist for exploration such as Revised Simplex

Multi-Iteration Parallelism in Control

- Control flow runs each algorithm iteration sequentially
- Could experiment with running specific independent stages in parallel

Back to Agenda Page

Demo

Back to Agenda Page

Thank you!

All Questions are Welcome!